UNIVERSITY OF CALIFORNIA, SAN DIEGO

Phase Shifter Approaches for Compact Low-Power Phased Array Transmitters

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronics Circuits and Systems)

by

Sunghwan Kim

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2010

The dissertation of Sunghwan Kim is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2010

DEDICATION

To my parents,

my wife Shohyun and daugher Claire.

EPIGRAPH

" *Only two things are infinite, the universe and human stupidity,*

and I'm not sure about the former."

—Albert Einstein (1879-1955)

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The text of Chapter Two, Three, Four and Five, in part of in full, is a reprint of the material as it appears in the following publications or as it has been submitted for publication in IEEE Transactions on Microwave Theory and Techniques and IEEE Radio Frequency Integrated Circuits (RFIC) Symposium.

- Sunghwan Kim, Jawad H. Qureshi, Koen Buisman, Lawrence E. Larson and Leo C. N. de Vreede, "A Low-Distortion, Low-Loss Varactor Phase-Shifter Based on Silicon-on-Glass Technology", *IEEE Radio Frequency integrated Circuits (RFIC) Symposium*, June 2008.

- Sunghwan Kim, Jawad H. Qureshi, Koen Buisman, Lawrence E. Larson and Leo

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- Sunghwan Kim and Lawrence E. Larson "A 44-GHz SiGe BiCMOS Phase-Shifting Sub-Harmonic Up-Converter for Phased Array Transmitters", *IEEE Transactions. on Microwave Theory and Techniques*, May 2010.

- Sunghwan Kim, Prasad Gudem, and Lawrence E. Larson, "A 44-GHz 8-Element Phased Array SiGe HBT Transmitter RFIC with an Injection-locked Quadrature Frequency Multiplier", *IEEE Radio Frequency integrated Circuits (RFIC) Symposium*, 2010.

The dissertation author was the primary researcher and the first author listed in these publications. He directed and supervised the research which forms the basis for these chapters.

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ABSTRACT OF THE DISSERTATION

Phase Shifter Approaches for Compact Low-Power Phased Array Transmitters

by

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Professor Lawrence E. Larson, Chair

One of the challenges in implementing phased array systems is to implement high performance phase shifters. This dissertation presents highly linear phase shifters for 2GHz wireless mobile applications and millimeter-wave phased array transmitters with active phase shifters. Different architectures of phased array systems pursue different aspects of phase shifters.

In the first part of the dissertation, a low-loss, low-distortion passive variable phase shifter on Silicon-on-Glass (SOG) process will be presented. Schottky diodes in the SOG process enables very high quality factor of varactor diodes and on-chip passive inductors. A novel passive variable phase shifter with varactors and inductors presented in the dissertation has very low third-order intermodulation distortion (IMD3) and low insertion loss, which make it suitable for transmitter front-end applications in mobile devices working at CDMA bands.

In the second part, two generations of integrated phased array upconverters at millimeter-wave frequencies with LO-path phase shifting will be presented. The phase-shifting is achieved by the vector summation of the I/Q LO signals in the LO path. The

first version adopts a frequency doubler followed by a polyphase filter to generate the I/Q basis LO signals. The principal of the active phase shifter operation and frequency doubler are explained. The phase error due to amplitude and phase mismatch of the polyphase filter is discussed. The upconverter can achieve -5dBm maximum output power at 45GHz with 1GHz baseband signal bandwidth.

The eight-element phased-array transmitter is implemented in a $0.18\mu m$ SiGe BiCMOS process in the later version. To reduce dc power consumption, a localized frequency doubling injection-locked quadrature oscillator is used to ease LO signal distribution. Measured conversion gain over frequency and IF signal is presented. Array beam scanning pattern is also presented based on the measured phase and power for each channel.

Chapter 1

Introduction

1.1 The Growth of Wireless Data Communication

A huge growth in the wireless communication market was observed during the last several decades as mobile data and voice become ubiquitous. This explosion has been fueled by the low cost integration of wireless ICs on silicon processes, which provide sufficiently high-frequency performance through device scaling. The integration of RF ICs on silicon with CMOS and BJT devices now dominates in the mobile wireless transceivers market operating below 5GHz.

Nevertheless, the demand for increasing number of subscribers and data rates for data-intensive wireless applications is exploding. Data transfer from high resolution digital cameras, transfer of music and video and other multimedia content between a computer and a portable device, such as the ubiquitous iPod, are some obvious examples. Emerging applications also include transmission of uncompressed video (Wireless HD [1]) between a multimedia device and an HD flat screen television or projector supporting multi-Gb/s data rate. This market demand leads designers to explore frequency reuse with multiple antenna systems and wider frequency bandwidth in the higher fre-

quencies.

Andrew Viterbi – founder of Qualcomm Inc.– stated:

"*Spatial processing remains as the most promising, if not the last frontier, in the evolution of multiple access systems.*" [2]

Spatial processing is one of the most practical solutions to these challenges. Spatial processing — or filtering — is the core idea of "smart antenna" systems, which was first used during World War II with the Bartlett beamformer [3]. Smart antenna systems are used to enhance the performance of wireless communications and radar systems under various names, such as beam-forming arrays, phased arrays, and MIMO transceivers. Even nowadays, the use of phased arrays is the most widespread in the realm of defense, with warships and fighter planes using phased array antennas for communications and radar applications.

1.2 Principal of Phased Array Antenna Systems

The fundamental concept of an phase array system is illustrated in Fig. 1.1, which shows a simplified N-element linear phased array system. The principle of operation of phased array antennas system is the same for receivers and transmitters.

For uniformly illuminated phased array, the difference in propagation distance between adjacent elements (mostly antennas) for signals arriving with an incident angle of θ is $d \sin\theta$. Then, in a narrow band system, the phase difference of the incoming signals between adjacent antenna is given by $\Delta\phi = \left(\frac{2\pi}{\lambda}\right) d \sin\theta$, where λ is the wavelength of the signals. The voltage sum of all the signals from the individual elements can be written by

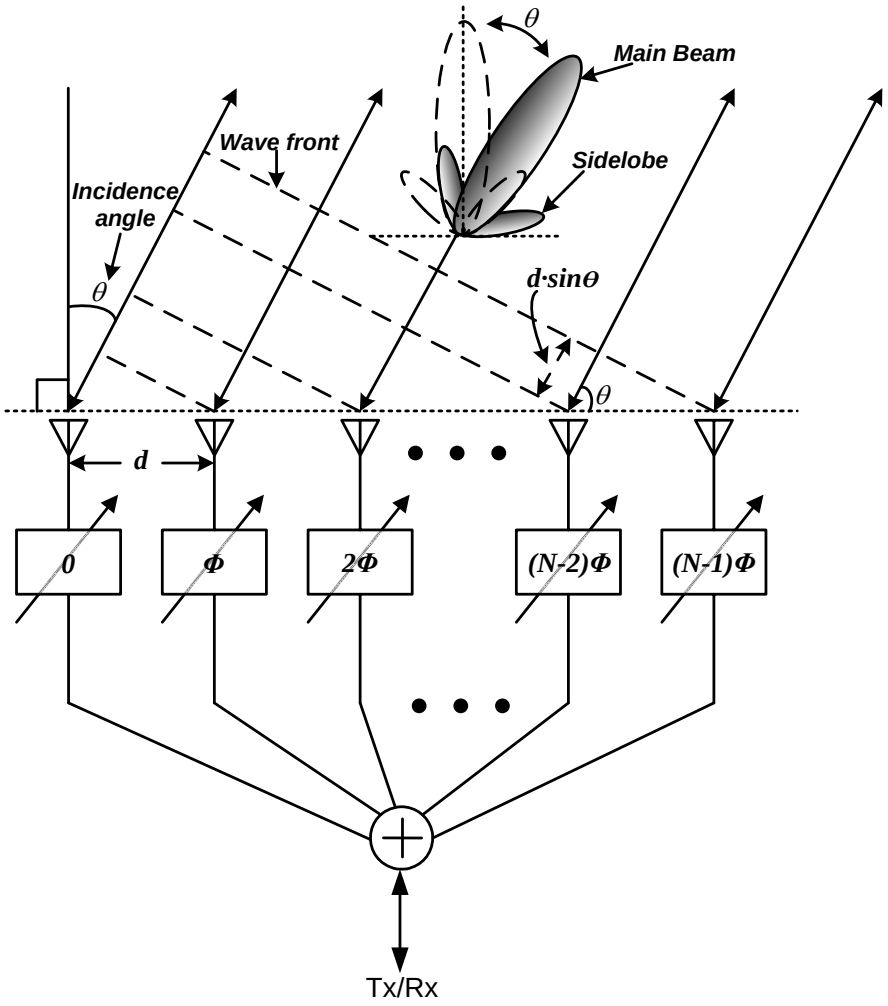


Figure 1.1: An N-element phased array antenna system.

$$S_t = A_m \sum_{k=0}^{N-1} \sin\left(\omega t + k\Delta\phi\right). \tag{1.1}$$

The sum can be simplified as

$$S_t = A_m \sin\left(\omega t + (N-1)\,\frac{\Delta\phi}{2}\right)\left(\frac{\sin\left(N\Delta\phi/2\right)}{\sin\left(\Delta\phi/2\right)}\right). \tag{1.2}$$

The magnitude of (1.2) is given by

$$\left|S_t\left(\theta\right)\right| = A_m \left|\frac{\sin\left[N\left(\frac{\pi}{\lambda}\right)d\sin\theta\right]}{\sin\left[\left(\frac{\pi}{\lambda}\right)d\sin\theta\right]}\right|, \tag{1.3}$$

which is also called the field-intensity pattern. Eq.(1.3) has its maximum at

$$\theta = \sin^{-1}(n\lambda/d), n = 0, 1, 2, \ldots. \tag{1.4}$$

The incoming signal incident angle θ can be controlled by placing phase shifters in the signal path to compensate for the phase difference of the path. At its maximum, coherent addition of the signal occurs, and hence there is an increase in the power radiated or received in the desired direction. On the other hand, in other directions, incoherent addition of the signal reduces the transmitting or receiving power. The array pattern can be expressed by a normalized radiation pattern, which is called the *array factor*. For isotropic antennas, the array factor is

$$AF\left(\theta\right) = \frac{\left|S_t\left(\theta\right)\right|^2}{A_m^2 N^2} = \frac{\sin^2\left[N\left(\frac{\pi}{\lambda}\right)d\sin\theta\right]}{N^2\sin^2\left[\left(\frac{\pi}{\lambda}\right)d\sin\theta\right]}. \tag{1.5}$$

The simulated array factor of omnidirectional eight antennas with beam angle from 20°

to 160° with antenna spacing of $\lambda/2$ are shown in Fig. 1.2. The 3dB beamwidth of this

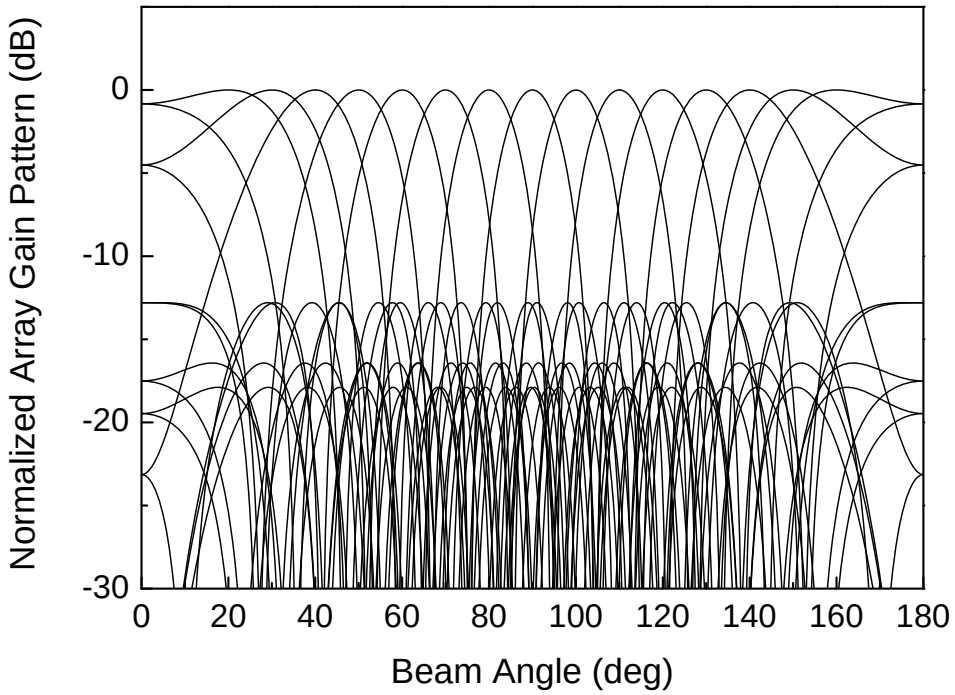


Figure 1.2: The Array Factor of an 8 element linear phased array. The beam angle is from 20° to 160°.

uniformly illuminated linear phased array of N elements is approximately

$$\theta_B = \left(\frac{50.8\lambda}{N \cdot d}\right)^{\circ}. \tag{1.6}$$

Eq. (1.6) tells us that the azimuth resolution is inversely proportional with the wavelength and hence proportional to the frequency. High-frequency phased arrays systems are suitable for applications that require the ability to differentiate two close objects. The first (and largest) sidelobes for the phased array are 13.2dB below the main beam maximum value. Hence, phased array systems works as a spatial filter.

In transmitters, the *effective isotropic radiated power* (EIRP) in the main beam

direction is improved by phased array antennas. EIRP is defined as [1]

$$EIRP = P_T - L_c + G_a, \tag{1.7}$$

where P_T is the transmitting power in dBm, L_c is the cable loss in dB, and G_a is the antenna gain expressed in dBi. When each transmitter element radiates X watts through isotropic antennas, roughly N^2X watts power is radiated in the main beam. Therefore, there is $10\log_{10}(N^2)$ improvement in EIRP by phased array antennas. This is particularly useful in high frequency applications since the signal suffers high attenuations in the air and substrate loss in silicon integration.

1.3 An Overview of Phased Array Transmitter Architectures

Phased arrays are one of multiple antenna systems that can electronically change the direction of transmission and reception of the electromagnetic beam in a particular direction by constructive signal addition, while simultaneously blocking it to other directions by destructive signal cancellation. This can be done by introducing a variable time delay in each signal path to compensate for the path differences in free space. In narrowband systems, the required variable time delay element can be substituted by a variable phase shifter.

The variable phase shifter required to achieve phased array functionality can be incorporated in different parts of the transmitter/receiver chain. Although all schemat-

[1] The amount of power that a theoretical isotropic antenna (which evenly distributes power in all directions) would emit to produce the peak power density observed in the direction of maximum antenna gain.

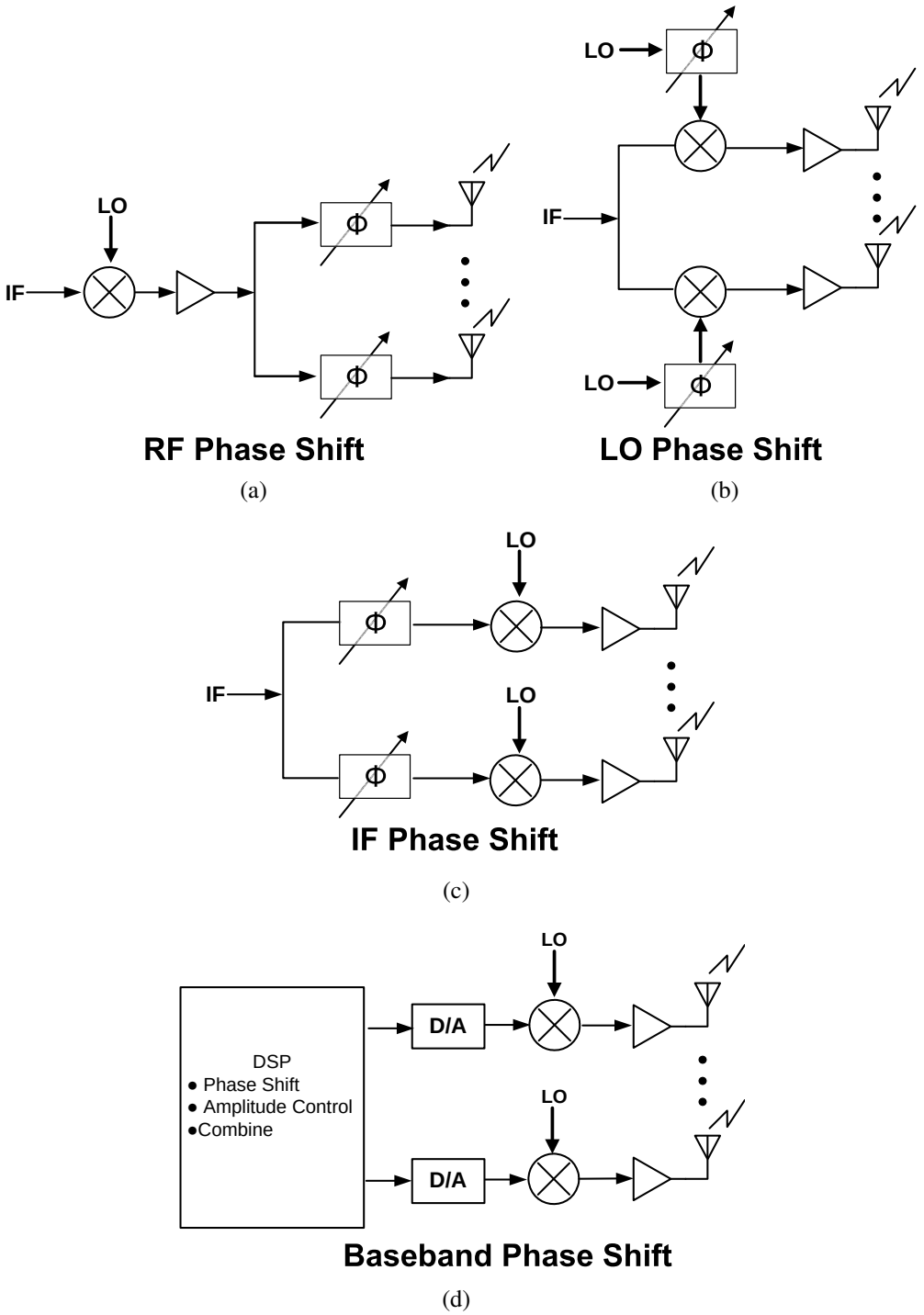


Figure 1.3: (a) RF phase shifting (b) LO phase shifting (c) IF phase shifting (d) baseband phase shifting architectures.

ics (Fig. 1.3(a)-(d)) represent transmitter arrays, the fundamental principles apply to receiver arrays as well. In fact, the receiver architecture is the reciprocal of transmitter.

Fig. 1.3(a) illustrates the RF phase-shifting architecture for phased array transmitters. In a receiver architecture, the received signals in the distinct channel are phase shifted and combined in the RF territory. Then, this combined signal is downconverted to baseband by frequency conversion blocks (which is usually a mixer). In the transmitter architecture as shown in the Fig. 1.3(a), the upconverted signal from a baseband is divided into each phase shifter in the RF domain. The RF phase shifting architecture has been the most popular phased array architecture in tradition. This is because of its high signal-to-interferer ratio (SIR). When the in-band interferer is incident along a null direction the signal combining occurs prior to downconversion in this architecture, and the interfere is cancelled prior to the downconversion mixer. This high SIR alleviates the linearity and dynamic range requirement of the downconversion mixer and the following blocks such as A/D converter. On the other hand, the performance of the phase shifter directly affects the data signal. The insufficient linearity of the phase shifter often negates the advantage of the RF phase shift architecture. Passive implementations of the phase shifter achieves higher linearity than active phase shifters at the expense of the loss of passive phase shifter. In addition, low noise performance of the phase shifter is essential as the phase shifter lies in the RF signal path and hence, it can degrade the system noise figure. In the transmitter architectures, low-loss, high-linearity performance of the phase shifter at large signal regime is demanded, in order not to degrade the system linearity and output signal power level. High performance passive phase shifters can be implemented with the power amplifier unit, which typically uses compound (III-V) process technologies such as GaAs or InP, or silicon-on-insulator (SOI) process technologies.

Fig. 1.3(b) illustrates the LO phase-shifting architecture for phased arrays. Phase-shifting of the LO of each signal path is equivalent to phase-shifting the RF signal since the mixing of the RF signal with the LO results in an addition or subtraction of their phases. In this architecture, in both receiver and transmitter, the linearity, gain and noise performance of the phase shifter no longer directly affect the system performance. However, in receivers, in-band interferers are cancelled after the downconversion mixer, which requires the high dynamic range of the mixers to tolerate the interferers. In millimeter-wave applications, on-chip implementations of the high performance passive phase shifter are much harder than in lower frequency, e.g. below 10GHz. For that reason, the LO phase-shifting architecture is sometimes preferred in mm-wave frequency ICs, since the required performance specification of the active phase shifters in the LO path is relaxed.

In the IF phase-shifting architecture, the phase shifters are implemented in the IF band (Fig. 1.3(c)). Due to low operating frequency, the circuit implementation can be relatively easier. However, the size of passive component in the phase shifters are consequently large.

In the baseband phase shifting architecture (Fig. 1.3(d)), a digital signal processor synthesize the phase shift at baseband frequency. It it a very versatile architecture for receivers and transmitters, since the system can be configured for different types of signals. However, the required processing power of the digital signal processor and high dynamic range of the A/D converters makes designers to hesitate to use this architecture.

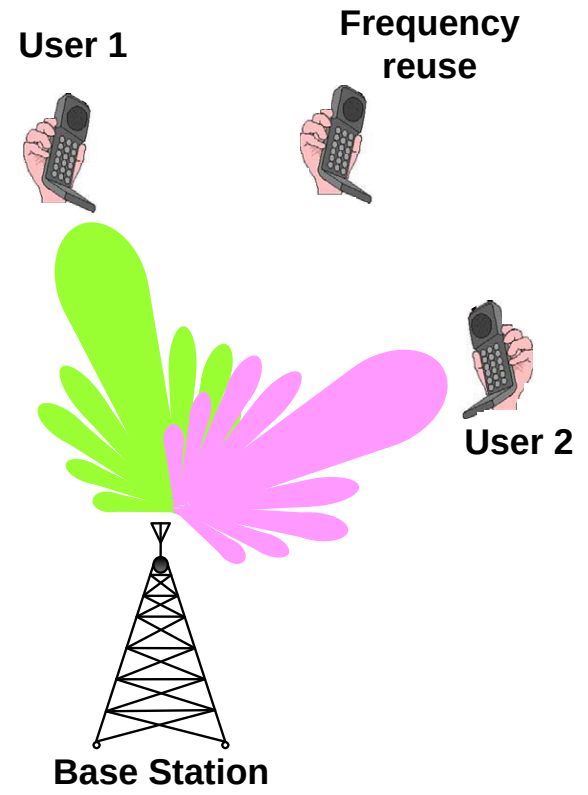
1.4 Phased Array Applications

Recently, phased arrays are gaining the spotlight for consumer mobile communications such as cellular telephones, WiMax/Wi-Fi wireless networking and internet

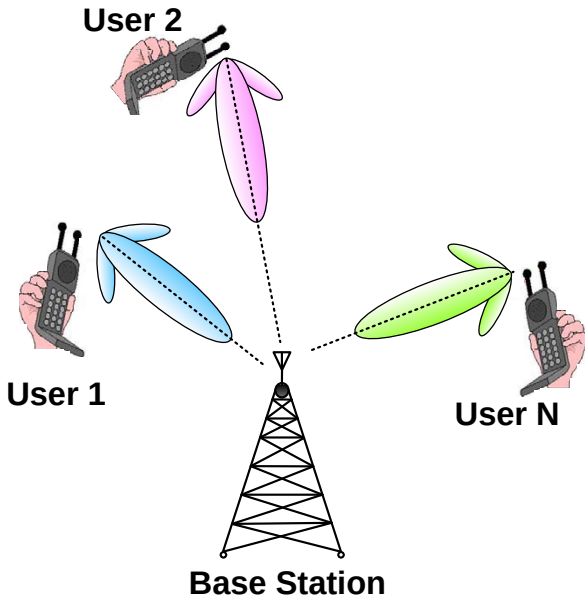
access (802.11 and IEEE 802.16 standards). One example of phased array antenna systems to improve spectral efficiency in a conventional cellular wireless communication system is shown in Fig. 1.4(a). The high directional beam pattern in phased array antenna systems allows interference reduction/mitigation and allows increased number of subscribers to share or reuse the same available resources such as frequency, time and codes [4]. This improved spectral efficiency introduces a new multiple access scheme that exploits the space domain, space division multiple access (SDMA).

Phased array antenna systems have been considered mostly for base stations so far due to high system complexity and high power consumption. Recently, phased array antenna techniques begin to be applied to mobile stations or handsets [5, 6] to further suppress the interference signal and improve multipath fading problem (Fig. 1.4(b)). Also, one of the third generation wireless personal communication systems, third generation partnership project (3GPP), WCDMA system [7], requires antenna diversity at base stations and optionally at mobile stations. Because of the compact size and the limited battery capacity of the handset, phased array antennas at handsets should dissipate low power with simple circuity without compromising high performance gain.

In satellite communication systems such as IRIDIUM ([8]) and Globalstar([9]) (personal communication) and Military Strategic and Tactical Relay (Milstar) (Defense satellite communications), the same problem — interference and multipath fading — remain challenges for reliable reception of signals [10, 11, 12]. Hence, phased array antennas were adopted earlier than cellular communication systems to tackle those problems.



(a)



(b)

Figure 1.4: (a) Beamforming in cellular wireless communication system. Beam is formed by the base station and (b) handset beamforming in cellular wireless communication system. Dual antennas are adopted in mobile handsets.

1.5 Millimeter-wave Wireless Communication

Shannon's theorem tells us that channel capacity is proportional to bandwidth and a logarithmic function of SNR [13].

$$C = BW \cdot \log_2(1 + SNR) \tag{1.8}$$

The thirst for higher data rate encouraged wider bandwidth and complex modulation schemes to compress as many bits-per-second/Hz as possible. Low GHz wireless communications standards such as the IEEE 802.11(a,b,g,n), Bluetooth, and Zigbee suffer from the limited data transfer rate — a few hundreds of Mega Bits Per Second (Mbps) — in its 2.4GHz and 5GHz frequency band. Fig. 1.5 shows the data rates and range requirements for number of wireless local area network (WLAN) and wireless personal area network (WPAN) systems [14]. IEEE802.15.3c group developed a millimeter-wave-based alternative physical layer for the existing 802.15.3 WPAN standard operating in clear band including 57-64 GHz unlicensed band defined by FCC 47 CFR15.225.

The key advantage of mm-wave wireless communications comes from the wide unlicensed bandwidth available in the 60GHz range, e.g. 57-64GHz unlicensed band in the U.S. Millimeter-wave frequencies also have a wider bandwidth than lower carrier frequencies for the same fractional bandwidth; hence, higher data rate transmission is possible. This increased bandwidth can also simplify the signal modulation hardware, since a sophisticated baseband signal modulation scheme is less demanding.

The wavelength of an electromagnetic wave decrease with increasing frequency. For example, a 60 GHz quarter-wave length ($\lambda/4$) electromagnetic wave in silicon diox-

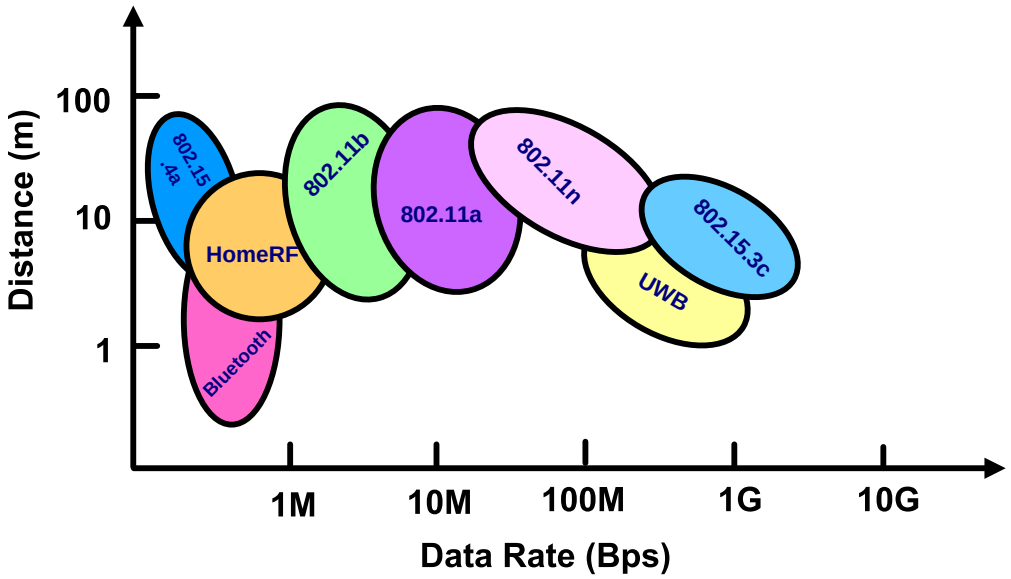


Figure 1.5: Data rates and range requirements for WLAN and WPAN standards and applications. Millimeter wave technology, IEEE 802.15.3c is aiming for very high data rates.

ide dielectric is 600μm, whereas it is 15mm at 2.4GHz. In mm-wave wireless systems, the size of antenna and passive elements can be reduced, decreasing the size of the form factor and the manufacturing cost.

However, mm-wave signal propagation at the 60GHz band highly is attenuated due to oxygen absorption (Fig. 1.6) [15]. Short range applications, such as WPAN, benefit from this atmospheric absorption, which provides natural spatial isolation. The spatial isolation/direction leads to less interference and hence higher data rates of transmission. On the other hand, the high atmospheric attenuation can be an obstacle for long range applications. Phased array antennas are an attractive solution to expand the range by directional beamforming to the desired target direction. In another point of view, by combining the signals from different channels in the air, directivity can be increased. This directional beamforming is an attractive solution to expand its range for high frequency, long range applications. In particular, power amplifier output power

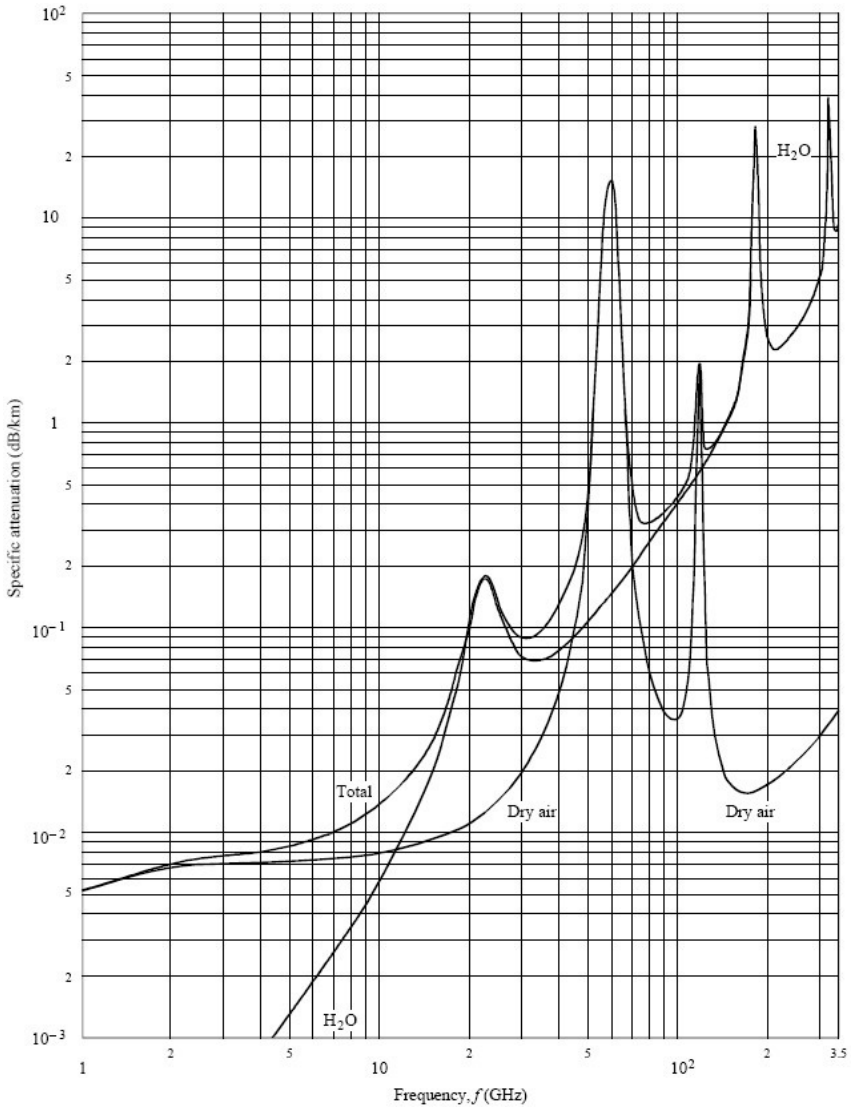


Figure 1.6: Specific attenuation for atmospheric gases as a function of frequency.

requirement can be relieved by distributing the total output power to smaller distributed power amplifiers (PAs) in each channel. This is also beneficial for PAs with CMOS technology with low breakdown voltages as the size of the transistors is reduced.

1.6 Dissertation Objectives and Organization

This dissertation can be divided into two broad sections. The first part of this dissertation focuses on phase shifter implementation in the RF path. While it is implemented with passive components, it has a superior performance in terms of gain and linearity, which again makes it suitable for the RF path phase shifting architecture of phased array transmitter, in conjunction with its scalability over phase shift variation. While the linearity has been studied extensively for active phase shifters, the linearity analysis of passive phase shifter with varactor diodes has not been explored thus far. The third-order intermodulation distortion was analyzed by a Volterra series considering memory components in the passive phase shifters such as variable capacitors and inductors.

In Chapter 2, a new variable passive phase shifter based on an all-pass network is presented. The variable phase shifter was implemented on silicon-on-glass technology, which accommodates a high quality factor varactor diode. Circuit design procedure and the linearity and phase variation measurement are presented. Its high-linearity and low-loss performance is compared with recently published phase shifters.

In Chapter 3, the linearity of the phase shifter introduced in Chapter 2 is discussed and extensively analyzed for the several cases of configuration of diodes. A closed-form third-order intermodulation distortion is presented and compared with simulation results.

The second part of this dissertation focuses on the design of a mm-wave phased

array upconverter with an active phase shifter implemented in the LO path.

In Chapter 4, a 44GHz phase-shiting sub-harmonic upconverter implemented in $0.18\mu m$ SiGe BiCMOS is presented. For active phase shifting functionality, variable gain amplifiers are designed. For quadrature signal generation, a two-stage RC polyphase filter followed by a frequency doubler is presented. The Chapter discusses the design, optimization, and performance trade-offs of each building block. The Phase error out of the RC polyphase filter and the operation of the frequency doubler is analyzed.

In Chapter 5, an eight-element phased array transmitter with an injection-locked quadrature frequency multiplier is presented. This novel architecture help to reduce the required LO signal power from the phase-locked loop (PLL) and provides wider frequency tunability through wide frequency locking range of the ring oscillator. Its measured result and calculated array patterns are presented.

Chapter 6 summarize the whole research work.

Chapter 2

A Low-Distortion, Low-Loss Varactor Phase-Shifter

2.1 Introduction

A phase-shifter is a critical component in the transmit and receive paths of phased-array radar and communication systems, which requires high data rates such as multiple-input multiple-output (MIMO) technology [16, 17, 18, 19]. The performance requirements in these systems are stringent; the phase shifters should be highly linear to prevent signal distortion and they should be compact for a small form factor. They are also required to have low dc power consumption and low insertion loss. MEMS phase shifters are excellent candidates for phased array antenna systems, since they demonstrate outstanding performance in many applications in terms of low insertion loss and high linearity [20, 21].

However, phase shifters based on MEMS varactor loaded transmission lines still suffer from relatively high cost due to non-standard processing and hermetic packaging. An alternative to MEMS varactors would be varactor diodes, and the linearity and loss

of varactor diodes were recently improved using uniformly doped Schottky diodes in anti-series configuration associated with a dedicated silicon-on-glass technology [22, 23].

A varactor-loaded transmission-line based phase-shifters are one popular type, and were presented in [24, 25]. Lumped element transmission-lines are widely used in this type of phase shifters to reduce chip size. However, the size of transmission-line inevitably becomes large inversely proportional to the desired working frequency.

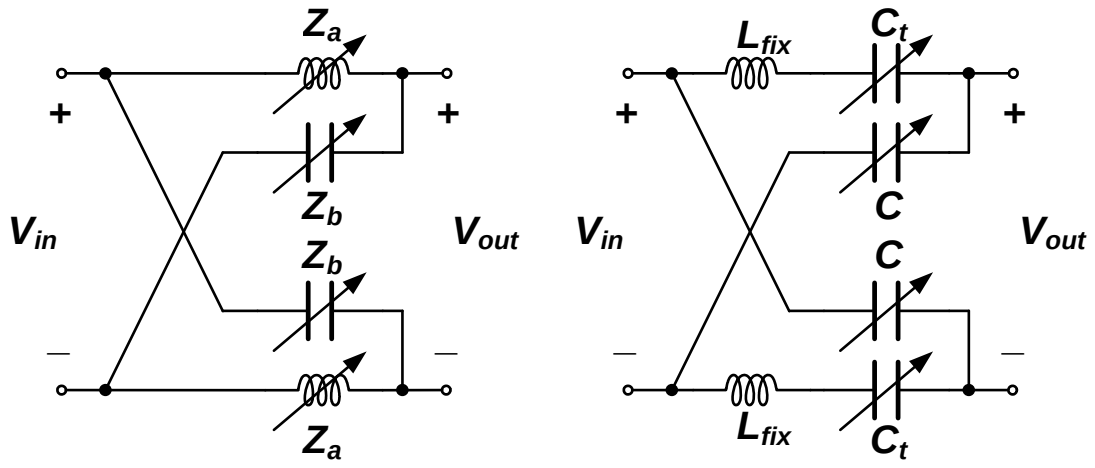
Active variable resonance circuits based and vector-modulator type phase shifters [26, 27] have fairly good gain at the expense of dc power consumption. Typically, its linearity was reported relatively low.

In this work, a high-performance varactor based phase shifter is introduced. Section 2.2 shows the properties of all-pass networks. Section 2.4 explains the circuit design of the phase shifter based on an all-pass network. Section 3.1 analyze the linearity of the phase shifter with Volterra series approach. The measured results and conclusion are followed in Sections 2.5 and 2.6.

2.2 Design Theory

Lossless all-pass networks are ideal candidates for phase shifters, since they vary the phase of a signal without affecting its magnitude. One simple implementation is shown in Fig. 2.1(a) [28, 29]. If the reactance components are designed such that

$$Z_a \cdot Z_b = R_L^2, \tag{2.1}$$



(a) (b)

Figure 2.1: (a) Schematic of an all-pass network with LC reactance component and (b) schematic of a proposed all-pass network phase shifter.

where R_L is the load resistance, then the input impedance of the circuit is R_L and the voltage transfer function of the circuit is

$$\frac{V_o(s)}{V_{in}(s)} = \left(\frac{1 - Z_a(s)/R_L}{1 + Z_a(s)/R_L}\right) \tag{2.2}$$

From (2.2), the phase shift of this network is given by

$$\angle\left(\frac{V_o}{V_{in}}\right) = \Delta\phi = -2\arctan(\omega R_S C), \tag{2.3}$$

where $L/C = R_S^2$. R_S is the source impedance and the phase shifter is designed such that $R_L = R_S$. From (2.3), a variable phase shift can be achieved by tuning the capacitance and inductance. Over a small frequency bandwidth, a variable inductance can be approximated by a fixed inductor in series with a variable capacitance C_t. The proposed circuit is introduced in Fig. 2.1(b).

In order to find appropriate values of capacitors, we set the capacitance C_t to be

α times larger than C. The capacitance tuning ratio r, given by C_{max}/C_{min}, is limited by the process technology. The reactance of the series combination of L_{fix} and C_t can be expressed as

$$X_L = \omega L_{fix} - \frac{1}{\omega C_t}. \tag{2.4}$$

The reactance X_L and $1/\omega C$ change in the opposite direction satisfying the condition (2.1), i.e.,

$$X_L|_{max} \cdot \left.\frac{1}{\omega C}\right|_{min} = X_L|_{min} \cdot \left.\frac{1}{\omega C}\right|_{max} = R_S^2 \tag{2.5}$$

For a given C_{min} and capacitance tuning range (r),

$$\alpha = r^{-1}\left(\omega R_S C_{min}\right)^{-2} \tag{2.6}$$

$$L_{fix} = (1+r)R_S^2 C_{min} \tag{2.7}$$

For a 50Ω source and load impedance, and a varactor tuning ratio r of 4:1 given by the process technology, the ratio of C_t to C, and the necessary inductance L, can be obtained as a function of the minimum capacitance C_{min} as shown in Fig. 2.2. As C_{min} decreases, the achievable phase shift increases by (2.3) and the lower inductance shrinks the entire chip size. However, it also increases the size of C_t. An optimum value of C_{min} of $260fF$ is chosen in this case. The corresponding maximum achievable change in phase shift per section can be calculated from (2.3), which is approximately 48°.

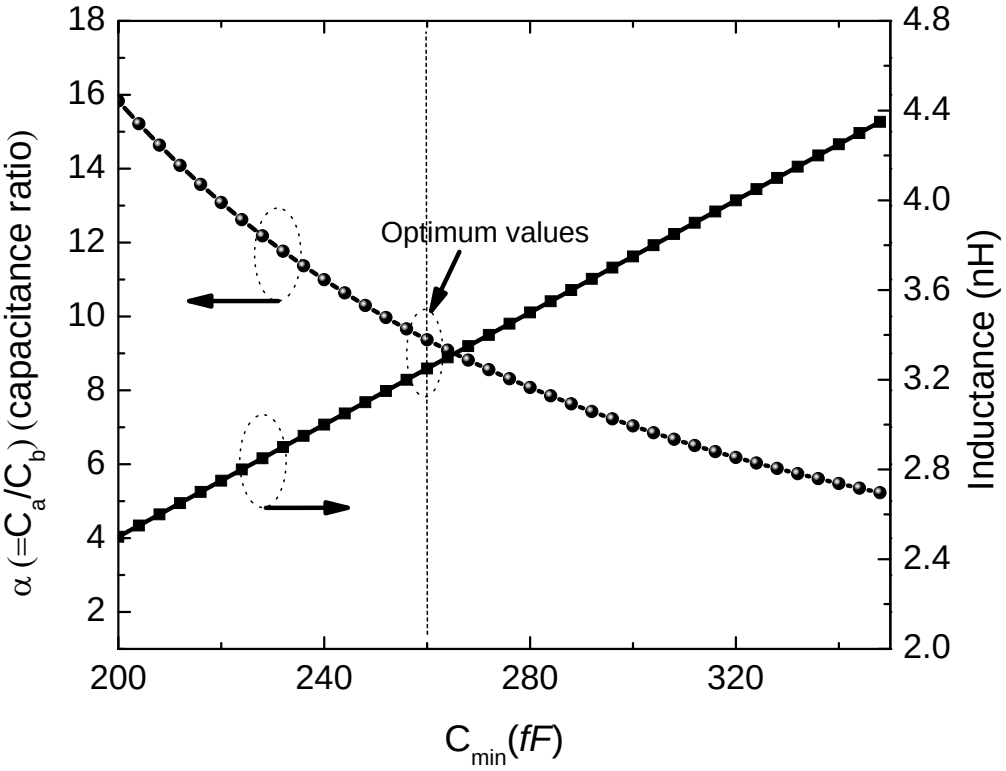


Figure 2.2: Simulated value of α (=C_t/C) and required inductance as a function of minimum capacitance C_{min} at 2GHz (capacitor tuning ratio r is 4:1).

2.3 Process Technology

In order to design a phase shifter based on the all-pass network, high-performance variable capacitors are necessary. In this study, a dedicated silicon-on-glass technology, which was developed at the Delft University of Technology is employed [30]. This technology provides a low-loss substrate and patterning of both the front and back sides of the wafer, so the intrinsic varactor can be directly contacted by thick metal on both sides (Fig. 2.3). This removes the need for a buried layer or finger structures, as would be the case in conventional integrated varactor implementations [22]. Moreover, this technology presents a very high performance Schottky varactor diode; quality (Q) factor ranges typically from 50 to 300 at 2GHz and the effective capacitance tuning range

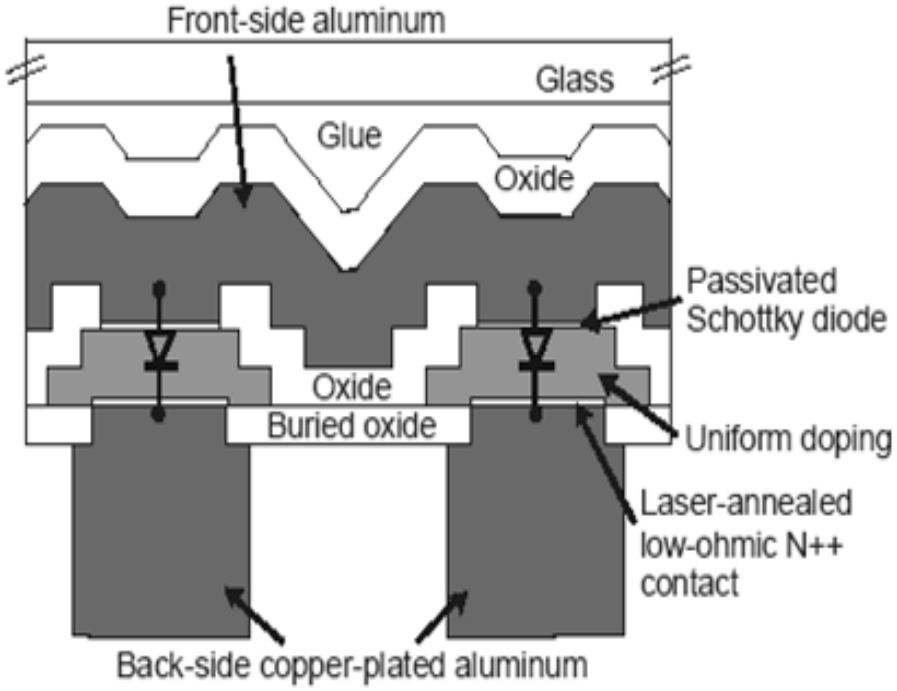


Figure 2.3: Cross section of the silicon-on-glass varactor technology.

of the uniformly doped diodes is approximately 4:1.

2.4 Phase Shifter Circuit Design

2.4.1 Variable Capacitor Design

A schematic of a single phase shifter stage based on anti-series varactors is shown in Fig. 2.4. As was explained in [22, 24, 31, 32], for uniformly doped anti-series diodes with a sufficiently high center-tap impedance, the varactor is ideally "distortion-free". The impedance of the dc biasing network should be significantly larger than the reactance of the varactor diodes at baseband. Otherwise, RF current will leak through the dc biasing network. 120kΩ center-tap resistors are used. Anti-parallel diode pairs can be used to further increase the center-tap impedance. 120kΩ resistors are also con-

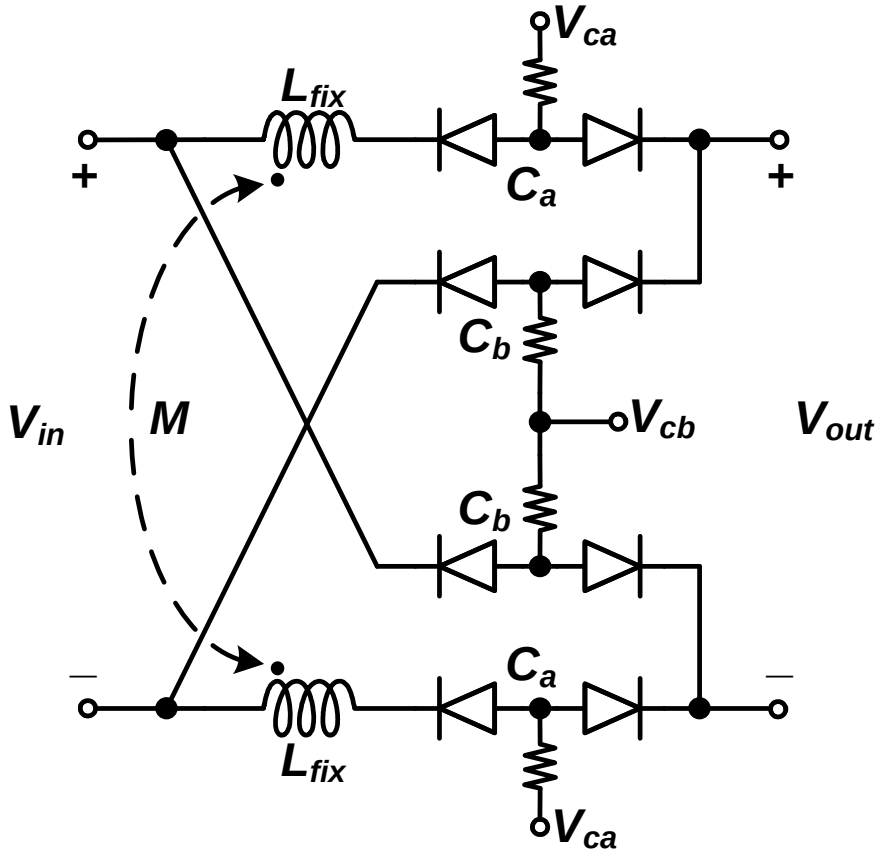


Figure 2.4: Schematic of the phase shifter with distortion-free diode varactors and magnetically coupled inductors.

nected at the input and output of each stage to provide dc ground for the varactor diodes. Varactor diode pairs C_a and C_b have zero bias capacitance of 10pF and 1pF, respectively.

2.4.2 Inductor Design and Layout

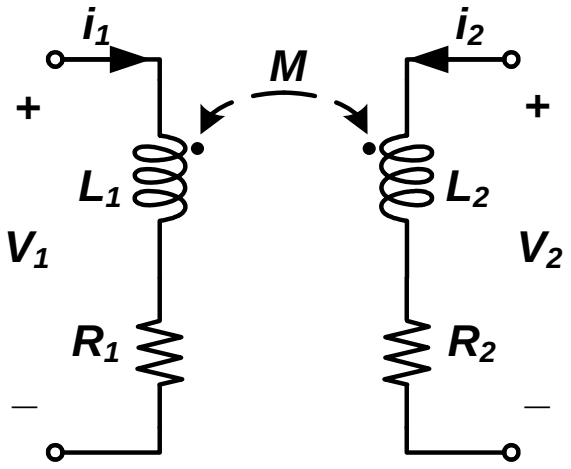


Figure 2.5: Magnetically coupled inductors.

The two separated fixed inductors are substituted with magnetically coupled inductors in order to increase the *effective* inductance. The V-I relationship for two magnetically coupled inductors (Fig. 2.5) can be written as

$$\begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} = \begin{bmatrix} sL_1 + R_1 & sM \\ sM & sL_2 + R_2 \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix}, \tag{2.8}$$

where M=$k\sqrt{L_1 L_2}$, k is the coupling coefficient, and R_1 and R_2 are parasitic resistances. For 1:1 coupled inductors in the phase shifter, we can assume $L_1 = L_2 = L_{fix}$ and $R_1 = R_2 = R$. If $i_2/i_1 = Ae^{j\theta}$, then the V-I relationship at the primary and

secondary ports can be expressed as

$$V_1 = [j\omega L_{fix}(1 + kA\cos\theta) + (R - \omega kAL_{fix}\sin\theta)]\, I_1 \tag{2.9a}$$

$$V_2 = \left[j\omega L_{fix}(1 + kA^{-1}\cos\theta) + (R + \omega kA^{-1}L_{fix}\sin\theta)\right] I_2 \tag{2.9b}$$

For a balanced differential signal applied at the input of the phase shifter, $A = 1$, $\theta = 180°$. Consequently, (2.9) becomes

$$V_1 = [j\omega L_{fix}(1 - k) + R]\, I_1 \tag{2.10a}$$

$$V_2 = [j\omega L_{fix}(1 - k) + R]\, I_2 \tag{2.10b}$$

Therefore, the effective inductance is given by

$$L_{eff} = L_{fix}(1 - k) \tag{2.11}$$

By substituting L_{fix} in (2.7) with L_{eff} in (2.11),

$$L_{fix} = \left(\frac{1 + r}{1 - k}\right) R_S^2 C_{min} \tag{2.12}$$

For $k < 0$, the required inductance L_{fix} decreases as $|k|$ increases.

As shown in Fig. 2.6, the 1:1 interleaved transformer is designed on the top-level metal layer of the process. This type of transformer is best suited for four-port

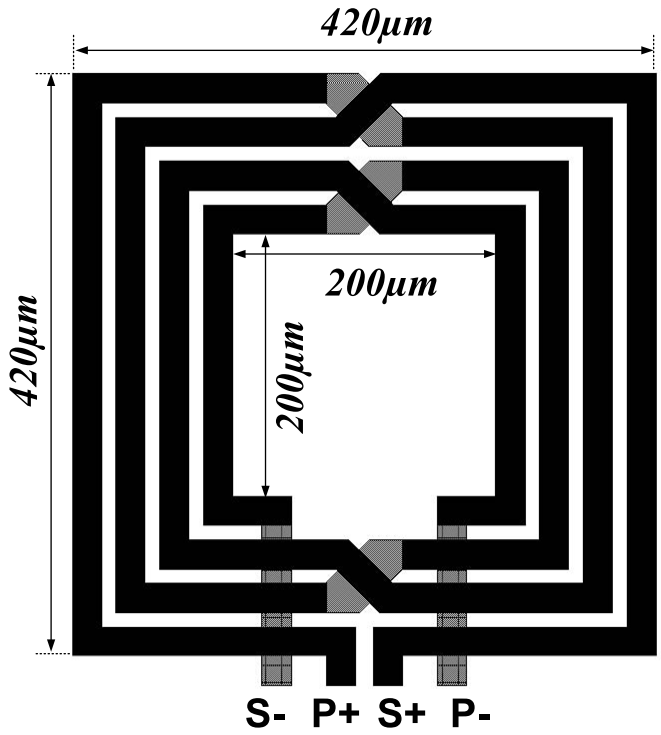


Figure 2.6: Layout of the magnetically coupled inductors in the phase shifter.

applications that demand symmetry, since the electrical characteristics of the primary and secondary are identical when they have the same number of turns [33, 34]. The outer diameter of the transformer is 420μm and the inner diameter is 200μm. A full EM-simulation was performed, and a coupling coefficient of -0.6, with self-inductance of 2.1nH, was obtained.

2.4.3 Cascaded Phase Shifter Architecture

As discussed earlier, the proposed all-pass network phase shifters have a limited phase variation of approximately 48°. Four identical phase shifters, which are connected in sequence as shown in Fig. 2.7 to achieve a total phase variation of 180°, can overcome the limited phase shift of each stage. Since (2.1) is maintained during normal operation,

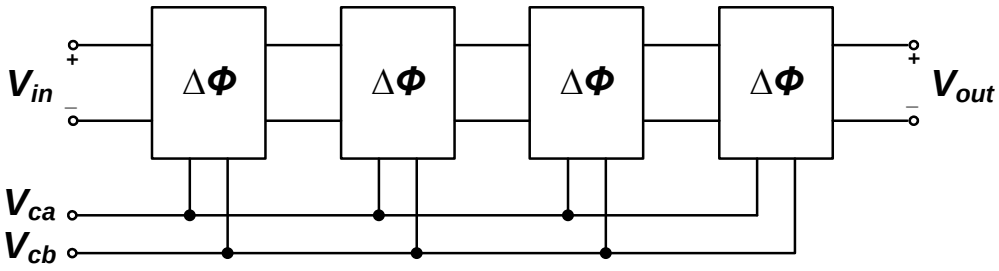


Figure 2.7: Four stages phase shifter architecture.

the input impedance of the first stage duplicates the load resistance R_L. Tuning voltage nodes V_{ca} and V_{cb} are connected separately so that only two tuning voltages are required.

2.5 Experimental Results

A microphotograph of the phase shifter is shown in Fig. 2.8. Differential two-

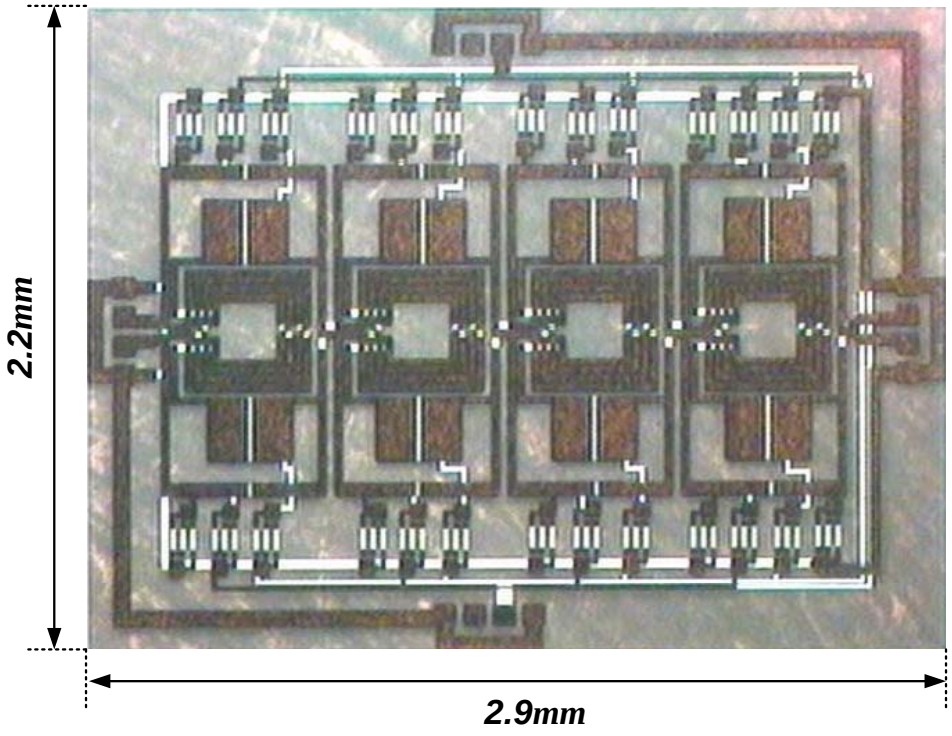


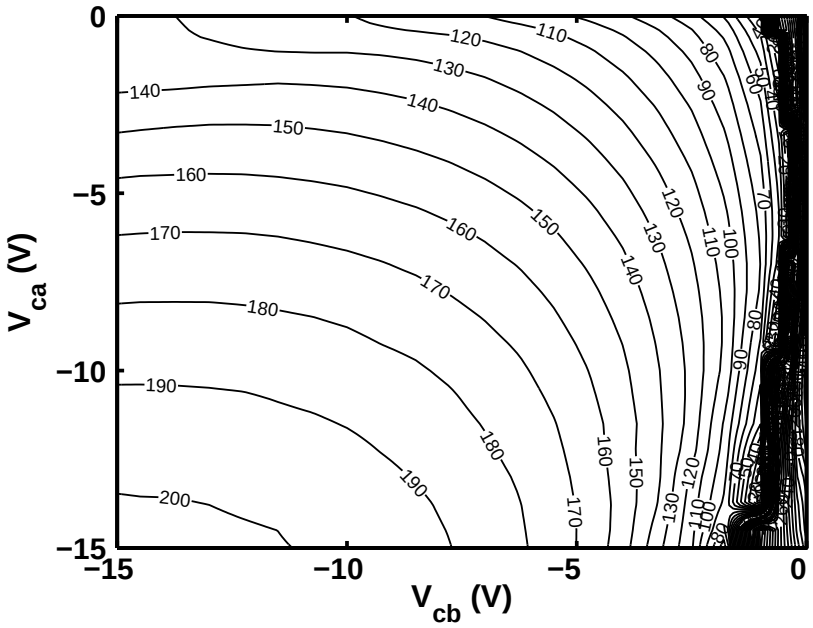
Figure 2.8: Microphotograph of the phase shifter realized in silicon-on-glass technology.

port S-parameter measurements were performed after LRM calibration. The two dc control voltages were swept to find optimum pairs of V_{ca},V_{cb}. The measured phase shift (=$\angle S_{21}$) and insertion loss at 2GHz are shown in Fig. 2.9(a) and (b) in the form of contour lines. It must be noted that although the dc control voltages are quite high, very little dc current (on the order of 10μA), which is the total leakage current of the realized varactor diodes, is required. This phase shifter can achieve continuous phase shift up to 180° with insertion loss less than 3.7dB as shown in Fig. 2.10.

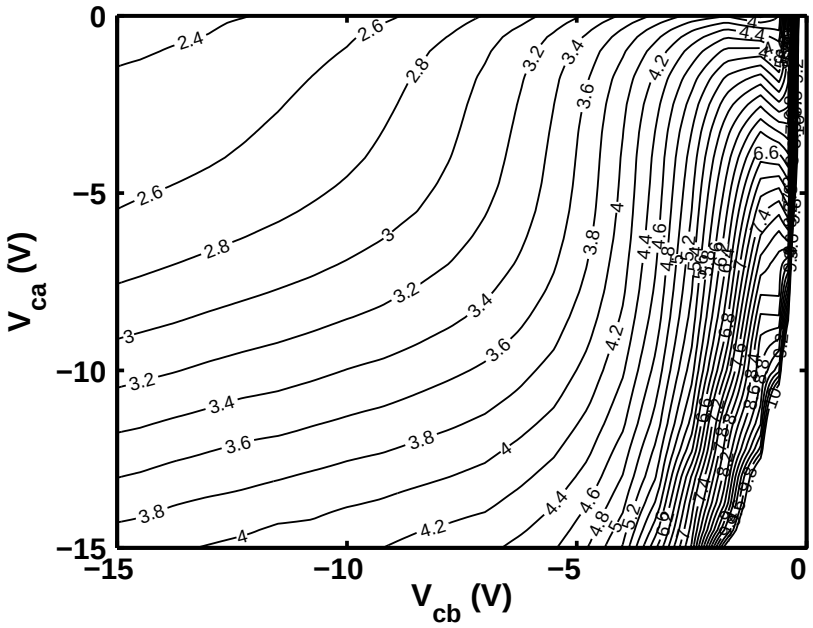
The variation of the insertion loss with phase shift is due to the Q factor variation of the varactors with bias. The higher than expected insertion loss is due to the Q factor of the varactor diodes being slightly lower than the desired value for this wafer. The measured phase shifter return losses for three different phase shifts ($\Delta\phi$=160°, 180° and 200°) are shown in Fig. 2.11 and are better than -10dB.

A two-tone test was performed on the phase shifter at 2GHz using a 50Ω differential two-port measurement fixture. For the calibrated power measurement of all frequency components of interest, the linearity of the phase shifter was measured with the load pull system of [40]. Fig. 2.12 gives the measured IM3 components as function of input power for three different tone-spacings (Δf=1MHz, 10MHz and 100MHz) for a target phase shift of 80°. IM3 components are less than -70dBm and -85dBm for 1MHz and 10MHz tone-spacing at P_{in}=10dBm, respectively.

This corresponds to an IIP3 better than +45dBm for 1MHz tone-spacing and +52dBm for 10MHz tone-spacing. The phase shifter circuit has been fabricated in the high performance silicon-on-glass technology. A performance summary of this variable phase shifter and its comparison to other works in the same band is shown in Table 2.1.



(a) Phase shift contour



(b) Loss contour

Figure 2.9: (a) Measured phase shift contour lines and (b) measured loss contour lines as a function of control voltages V_{ca} and V_{cb} at 2GHz.

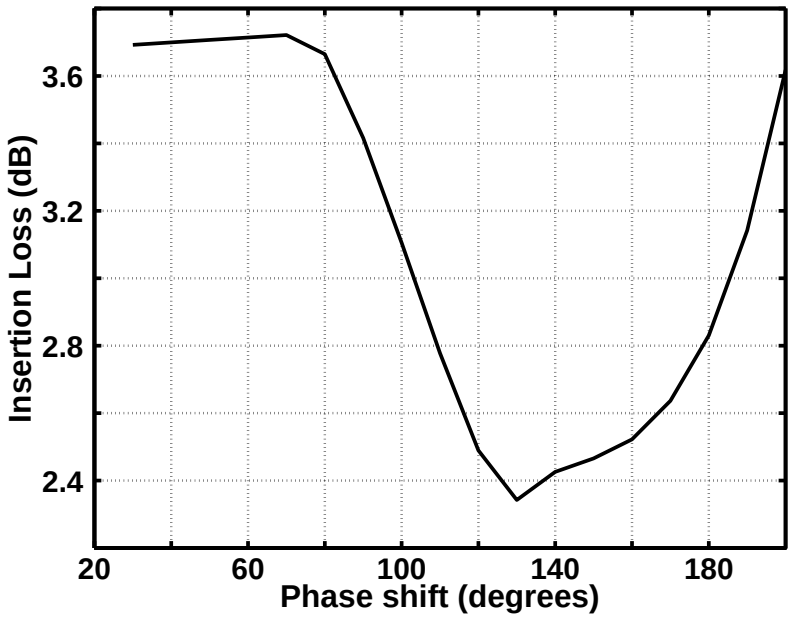


Figure 2.10: Minimum loss vs. phase shift at 2GHz.

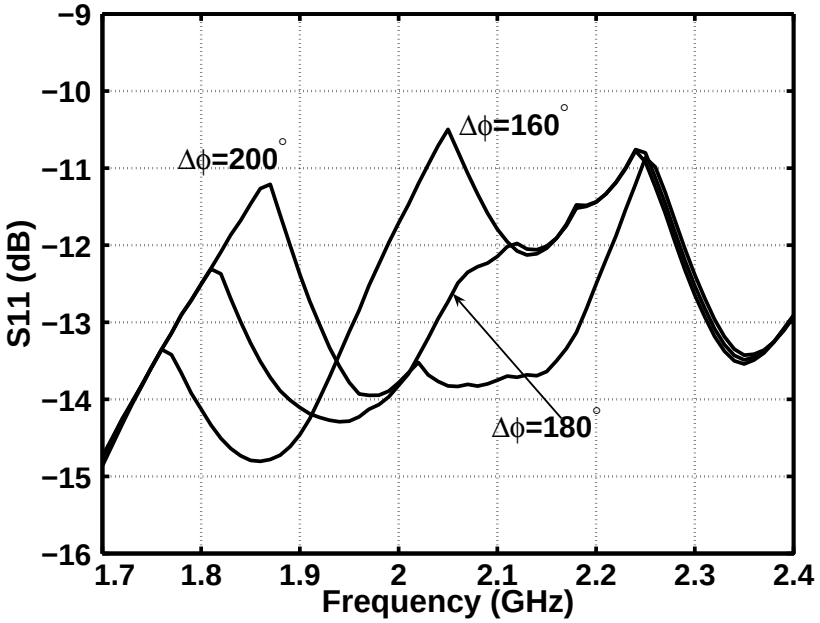


Figure 2.11: Measured $\mid S_{11} \mid$ of the phase shifter at optimum tuning voltage pairs.

Table 2.1: Comparison of continuously adjustable phase-shifter

Ref.	[26]	[27]	[35]	[36]	[37]
Freq.	2.4GHz	0.GHz8	2.4GHz	2.4GHz	2.4GHz
Phase var.	360°	120°	105°	120°	255°
Gain	2±0.7dB	1.6±0.6dB	-4.6dB	-5dB	-3.75dB
Linearity	-12dBm (IIP3)	-2.5dBm (IIP3)	10dBm (P1dB)	6dBm (P1dB)	n.a.
Power con.	90mW	9mW	18mW	111mW	∼0mW
Circuit area	2.3mm^2	0.81mm^2	1.08mm^2	0.357mm^2	5.72mm^2
Technology	0.3μm GaAs MESFET	0.6μm GaAs MESFET	0.18μm CMOS	0.18μm CMOS	BST on sapphire
Principle	active variable resonance circuit	active vector modulator	reflective type	reflective type	active all-pass network

Ref.	[38]	[24]	[39]	This work
Freq.	2.4/5.5GHz	1GHz	2.4/3.5/5.8GHz	2GHz
Phase var.	360°	180°	180°	180°
Gain	4dB	-1.2dB	-6.6dB	-3±0.7dB
Linearity	1dBm (IIP3)	45dBm (IIP3)	n.a.	53dBm (IIP3)
Power con.	28.8mW	∼0mW	45mW	∼0mW
Circuit area	6mm^2	n.a.	2.76mm^2	6.38mm^2
Technology	0.18μm CMOS	Schottky on SOI	0.18μm CMOS	Schottky on SOI
Principle	forward-type	lumped element transmission line	lumped element transmission line	passive all-pass network

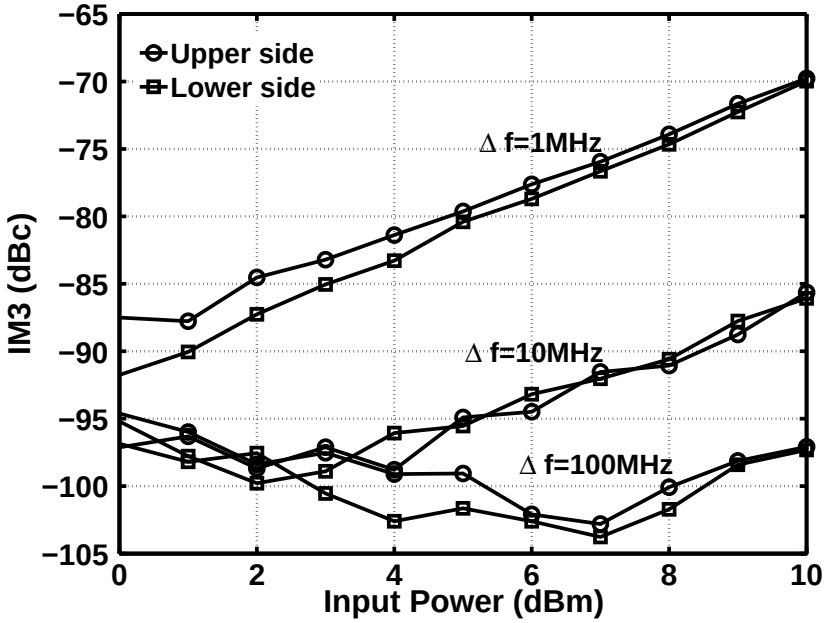


Figure 2.12: Measured IM3(dBc) versus frequencies at three different tone-spacings (1MHz, 10MHz and 100MHz).

This phase shifter shows superior linearity performance.

2.6 Conclusion

This Chapter presented a low-distortion phase shifter design based on transformers and low-loss varactor diodes. A very compact, low-power, differential phase shifter has been implemented, which shows a very high linearity of IIP3 $\geq$ 52dBm. Limited phase variation can be overcome cascading additional phase shifter block without buffering circuits between phase shifters. Linearity analysis of the phase shifter is presented in the next Chapter. This makes it possible for this phase shifter to be applied to various demanding applications such as phased array transmitter systems.

This chapter, in part or in full, is a reprint of the material as it appears in the following publications:

- Sunghwan Kim, Jawad H. Qureshi, Koen Buisman, Lawrence E. Larson and Leo C. N. de Vreede ”Analysis of a Low-Distortion, Low-Loss Varactor Phase-Shifter Based on Silicon-on-Glass Technology”, submitted to *IEEE Transactions On Microwave Theory and Techniques*, 2010.

- Sunghwan Kim, Jawad H. Qureshi, Koen Buisman, Lawrence E. Larson and Leo C. N. de Vreede, ”A Low-Distortion, Low-Loss Varactor Phase-Shifter Based on Silicon-on-Glass Technology”, *IEEE Radio Frequency integrated Circuits (RFIC) Symposium*, June 2008.

The dissertation author was the primary researcher and the first author listed in these publications.

Chapter 3

Linearity Analysis of the Varactor Based Phase Shifter

3.1 Varactor Capacitance Dependence on Voltage

The capacitance of a semiconductor diode can generally be expressed by

$$C(V) = \frac{K}{(\phi + V_r)^n}, \tag{3.1}$$

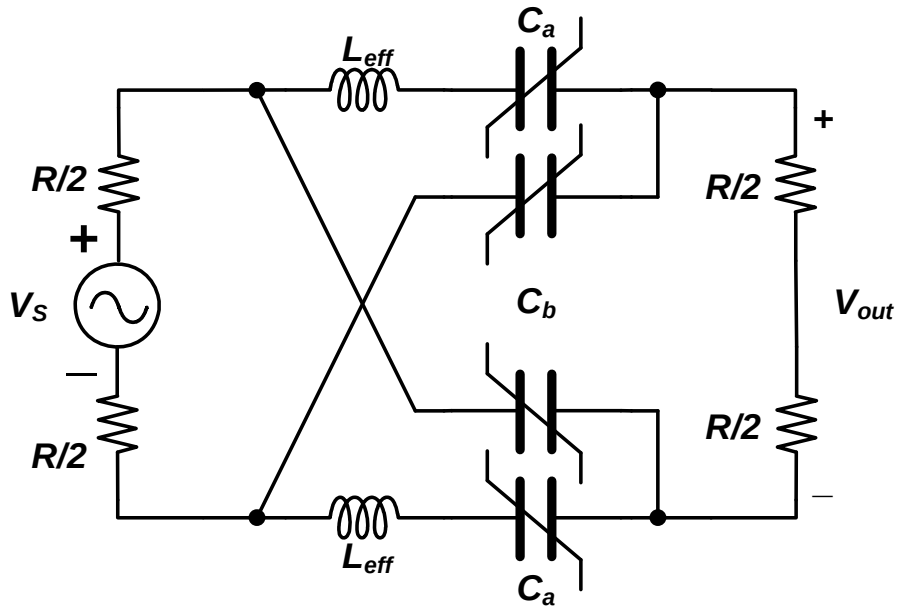
where ϕ is the built-in potential of the varactor diode, V_r is the applied reverse voltage, n is the power law exponent of the diode capacitance, and K is the capacitance constant. In this work, $n \approx 0.5$ for uniformly doped junctions and ϕ is 0.83V. Each incremental capacitance C_a and C_b in the phase shifter can be expressed in the form of Taylor polynomials shown in [32],

$$C_a(v_a) = C_{a0} + C_{a1}v_a + C_{a2}v_a^2 + \dots \tag{3.2a}$$

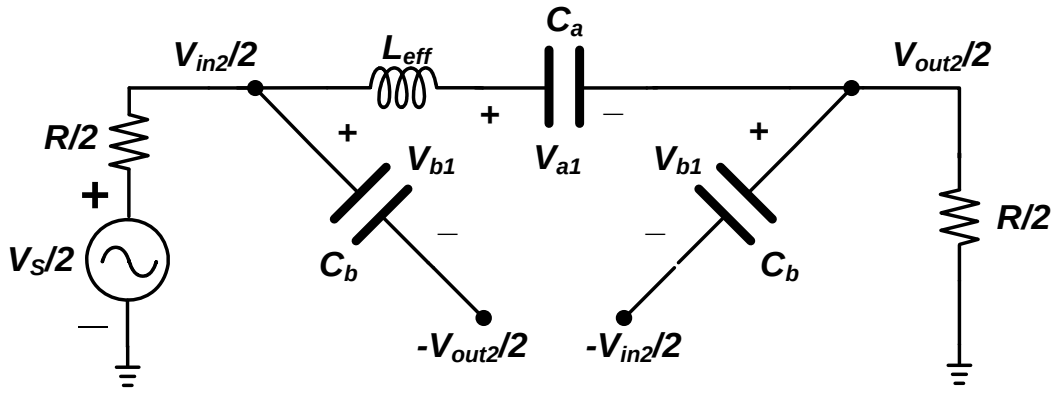
$$C_b(v_b) = C_{b0} + C_{b1}v_b + C_{b2}v_b^2 + \dots, \tag{3.2b}$$

where v_a and v_b are incremental voltages across C_a and C_a, respectively. Assuming C_a and C_b to be a weakly nonlinear capacitance, the fourth and higher-order terms in (3.2) can be ignored.

In order to simplify the linearity analysis, anti-series diodes in Fig. 2.4 are simplified as a single nonlinear capacitor as shown in Fig. 3.1(a).

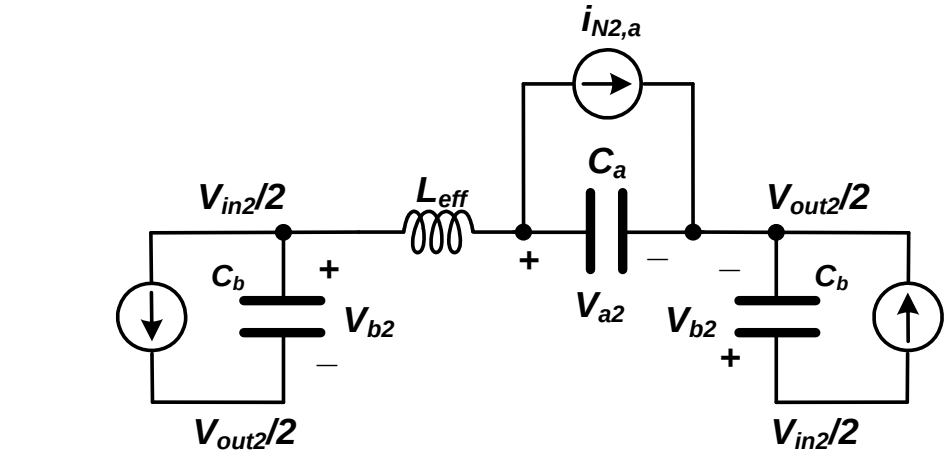


(a)

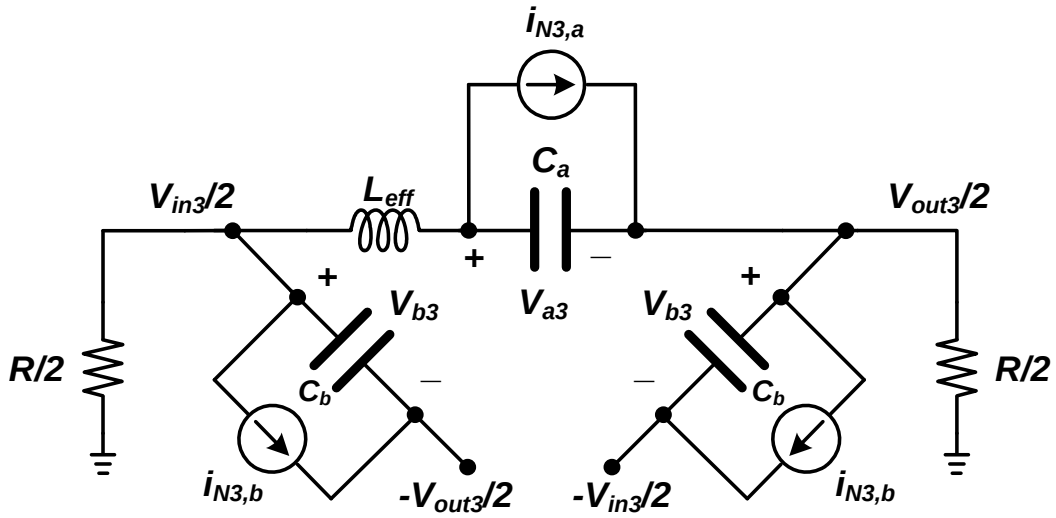


(b)

Figure 3.1: (a) A phase shifter with simplified nonlinear capacitors. (b) single-ended equivalent circuit of the phase shifter.



(a)



(b)

Figure 3.2: (a) Schematic for computation of the second-order Volterra kernels. (b) schematic for computation of the third-order Volterra kernels.

The output voltage and the voltage across each nonlinear capacitor can be represented as the truncated Volterra series in terms of the excitation voltage v_s. Thus,

$$\begin{aligned} v_{out}(s) =& H_{1,v_{out}}(s) \circ v_s + H_{2,v_{out}}(s_1, s_2) \circ v_s^2 \\ &+ H_{3,v_{out}}(s_1, s_2, s_3) \circ v_s^3 \end{aligned} \tag{3.3a}$$

$$\begin{aligned} v_a(s) =& H_{1,v_a}(s) \circ v_s + H_{2,v_a}(s_1, s_2) \circ v_s^2 \\ &+ H_{3,v_a}(s_1, s_2, s_3) \circ v_s^3 \end{aligned} \tag{3.3b}$$

$$\begin{aligned} v_b(s) =& H_{1,v_b}(s) \circ v_s + H_{2,v_b}(s_1, s_2) \circ v_s^2 \\ &+ H_{3,v_b}(s_1, s_2, s_3) \circ v_s^3, \end{aligned} \tag{3.3c}$$

where $H_{n,x}(s1, s2, \cdots, s_n)$ is the Laplace transform of the nth-order Volterra kernel at node x. The operator "$\circ$" scale the magnitude and phase of each component of v_s^n by the magnitude and phase of $H_{n,x}(s1, s2, \cdots, s_n)$ [41].

For a differential input signal, the phase shifter can be simplified to its single-ended first-order equivalent model as in Fig. 3.1(b). The first-order Volterra kernels $H_{1,v_a}(s)$, $H_{1,v_b}(s)$ and $H_{1,v_{out}}(s)$ in (3.3) are the transfer functions of the phase shifter from the input to the voltage across the capacitors and the output, respectively. Therefore, from Fig. 3.1(b)

$$H_{1,v_a}(s) = (1 - X_{ab}(s))(Z_a(s) - sL_{eff})/4Z_a(s) \tag{3.4a}$$

$$H_{1,v_b}(s) = (1 + X_{ab}(s))/4 \tag{3.4b}$$

$$H_{1,v_{out}}(s) = X_{ab}(s)/2, \tag{3.4c}$$

where

$$Z_a(s) = sL_{eff} + \frac{1}{sC_{a0}} \tag{3.5a}$$

$$Z_b(s) = \frac{1}{sC_{b0}} \tag{3.5b}$$

$$X_{ab}(s) = \frac{R(Z_b(s) - Z_a(s))}{2Z_aZ_b + R(Z_b(s) - Z_a(s))}. \tag{3.5c}$$

The second-order Volterra kernels can be obtained from Fig. 3.2(a). Then, organized equations to compute of the second-order Volterra kernel corresponds to the matrix equation (3.6).

$$\begin{bmatrix} (s_1+s_2)C_{a0} & (s_1+s_2)C_{b0} \\ \frac{1}{(s_1+s_2)L} + (s_1+s_2)C_{a0} & -\frac{1}{(s_1+s_2)L} \end{bmatrix} \begin{bmatrix} H_{2,v_a}(s_1,s_2) \\ H_{2,v_b}(s_1,s_2) \end{bmatrix} = \begin{bmatrix} -(i_{N2,a}(s_1,s_2) + i_{N2,b}(s_1,s_2)) \\ -i_{N2,a}(s_1,s_2) \end{bmatrix} \tag{3.6}$$

The second-order nonlinear current source is a function of the first-order Volterra kernels, and is given by [42]

$$i_{N2,a}(s_1,s_2) = (s_1+s_2)C_{a1}H_{1,v_a}(s_1)H_{1,v_a}(s_2) \tag{3.7a}$$

$$i_{N2,b}(s_1,s_2) = (s_1+s_2)C_{b1}H_{1,v_b}(s_1)H_{1,v_b}(s_2). \tag{3.7b}$$

In the second-order Volterra kernel calculation, the source (V_s) is set to zero and only the second-order nonlinear current from the nonlinear varactors are applied to the circuit. The linearized circuit for the calculation of the second-order Volterra kernel is simplified as shown in 3.2(a). The second-order Volterra kernels of the voltage across C_a (V_a) and

$C_b\left(V_b\right)$ are calculated as follows.

$$
\begin{aligned}
&H_{2,v_a}\left(s_1,s_2\right)= \\
&-\frac{1}{4}\Big\{C_{a1}\left(1+s_1C_{b0}R\right)\left(1+s_2RC_{b0}\right)\left(1+\left(s_1+s_2\right)^2LC_{b0}\right) \\
&\qquad +C_{b1}\left(1+s_1C_{b1}\left(R+s_1L\right)\right)\left(1+s_2C_{a0}\left(R+s_2L\right)\right)\Big\} \\
&\quad\Big\{\left(2+s_1C_{b0}R+s_1C_{a0}\left(R+2s_1L+s_1^2LC_{b0}R\right)\right) \\
&\qquad\cdot\left(2+s_2C_{b0}R+s_2C_{a0}\left(R+2s_2L+s_2^2LC_{b0}R\right)\right) \\
&\qquad\cdot\left(C_{b0}+C_{a0}\left(1+\left(s_1+s_2\right)^2LC_{a0}\right)\right)\Big\}^{-1}
\end{aligned}
\tag{3.8}
$$

$$
\begin{aligned}
&H_{2,v_b}\left(s_1,s_2\right)= \\
&-\frac{1}{4}\Big\{C_{b1}\left(1+s_1C_{b1}\left(R+s_1L\right)\right)\left(1+s_2C_{a0}\left(R+s_2L\right)\right) \\
&\cdot\left(1+\left(s_1+s_2\right)^2LC_{b0}\right)+C_{a1}\left(1+s_1C_{b0}R\right)\left(1+Rs_2C_{b0}\right)\Big\} \\
&\quad\Big\{\left(2+s_1C_{b0}R+s_1C_{a0}\left(R+2s_1L+s_1^2LC_{b0}R\right)\right) \\
&\qquad\cdot\left(2+s_2C_{b0}R+s_2C_{a0}\left(R+2s_2L+s_2^2LC_{b0}R\right)\right) \\
&\qquad\cdot\left(C_{b0}+C_{a0}\left(1+\left(s_1+s_2\right)^2LC_{a0}\right)\right)\Big\}^{-1}
\end{aligned}
\tag{3.9}
$$

In a similar fashion, the third-order nonlinear current of capacitors can be com-

puted with the second-order Volterra kernels $H_{2,v_a}(s_1, s_2)$ and $H_{2,v_b}(s_1, s_2)$.

$$\begin{aligned} & i_{N3,a}(s_1, s_2, s_3) \\ & \quad = (s_1 + s_2 + s_3) C_{a2} H_{1,v_a}(s_1) H_{1,v_a}(s_2) H_{1,v_a}(s_3) \\ & \quad\quad + 2(s_1 + s_2 + s_3) C_{a1} \overline{H_{1,v_a}(s_1) H_{2,v_a}(s_2, s_3)} \end{aligned} \tag{3.10a}$$

$$\begin{aligned} & i_{N3,b}(s_1, s_2, s_3) \\ & \quad = (s_1 + s_2 + s_3) C_{b2} H_{1,v_b}(s_1) H_{1,v_b}(s_2) H_{1,v_b}(s_3) \\ & \quad\quad + 2(s_1 + s_2 + s_3) C_{b1} \overline{H_{1,v_b}(s_1) H_{2,v_b}(s_2, s_3)}, \end{aligned} \tag{3.10b}$$

where the bar indicates the symmetrization of the corresponding transfer function over all possible permutations of the Laplace variables [43].

As in the second-order Volterra kernel calculation, a matrix equation for third-order Volterra kernels can be formed (3.11) from which the third-order Volterra kernel for V_{out} can be calculated.

$$\begin{bmatrix} -(s_1 + s_2 + s_3) C_{a0} & (s_1 + s_2 + s_3) C_{b0} & \frac{1}{R} \\ \frac{1}{(s_1 + s_2 + s_3) L} & -\frac{1}{(s_1 + s_2 + s_3) L} & \frac{1}{(s_1 + s_2 + s_3) L} \\ +(s_1 + s_2 + s_3) C_{a0} & & \\ -\frac{1}{(s_1 + s_2 + s_3) L} & \frac{1}{(s_1 + s_2 + s_3) L} + (s_1 + s_2 + s_3) C_{b0} + \frac{2}{R} & -\left(\frac{1}{R} + \frac{1}{(s_1 + s_2 + s_3) L}\right) \end{bmatrix}$$
$$\cdot \begin{bmatrix} H_{3,v_a}(s_1, s_2, s_3) \\ H_{3,v_b}(s_1, s_2, s_3) \\ H_{3,v_{out}}(s_1, s_2, s_3) \end{bmatrix} = \begin{bmatrix} i_{N3,a}(s_1, s_2, s_3) - i_{N3,b}(s_1, s_2, s_3) \\ -i_{N3,a}(s_1, s_2, s_3) \\ -i_{N3,b}(s_1, s_2, s_3) \end{bmatrix} \tag{3.11}$$

3.2 Third-Order Intermodulation Distortion

Intermodulation is calculated for the case of two equal amplitude sinusoid signals at two different frequencies ω_a and ω_b applied to the phase shifter input:

$$v_s(t) = A_m \left[\cos\left(w_a t\right) + \cos\left(w_b t\right)\right]. \tag{3.12}$$

Then, the in-band third-order intermodulation products are at frequencies $2\omega_a - \omega_b$ and $2\omega_b - \omega_a$. In terms of Volterra kernels the third-order intermodulation (IMD3) is given by

$$IMD_3 = \frac{3}{4} A_m^2 \left| \frac{H_3, v_{out}(s_b, s_b, -s_a)}{H_1, v_{out}(s_b)} \right|. \tag{3.13}$$

The first-order $H_1, v_{out}(s_a)$ is found from (3.4c) by setting $s_1 = s_a$. $H_3, v_{out}(s_a, s_a, -s_b)$ can also be calculated. In practice, two-tone measurements occurs when the frequency separation between the two input signals is very small, i.e., $s_a \approx s_b \approx s$. From this assumption that $\Delta s \equiv |s_a - s_b| \rightarrow 0$, the third-order Volterra kernel of V_{out} can be calculated. And the ratio of the third-order Volterra kernel to the first-order Volterra kernel can be further approximated removing trivial terms. The resultant IMD3 in terms of the circuit components is shown (3.14). This expression can be used to estimate the nonlinearity of the phase shifter when the nonlinear coefficients are known.

$$
\begin{aligned}
&IMD_3 \approx \\
&-\frac{A_m^2}{16}\Bigg|\Big\{3C_{a2}(-1+sC_{b0}R)(C_{a0}+C_{b0}+4s^2LC_{a0}C_{b0}) \\
&\qquad\qquad -6C_{a1}^2(-1+sC_{b0}R)(1+4s^2LC_{b0}) \\
&\quad +\big[\,\big(4s^2L(2C_{a0}C_{b1}^2+6C_{b0}C_{b1}^2-3C_{a0}C_{b0}C_{b2}-3C_{b0}^2C_{b1}) \\
&\qquad\qquad -3\left(C_{b2}(C_{a0}+C_{b0})-2C_{b1}^2\right)\big)\,\big] \\
&\quad \cdot(1+sC_{a0}\,(R+sL))^3\,(-1+sC_{a0}(R-sL)) \\
&\quad +4sC_{a1}C_{b1}R(1+8s^2LC_{b0})(1+sC_{a0}(R+sL))(C_{b0}+C_{a0}(-1+s^2LC_{b0}))\Big\} \\
&\quad \cdot\Big\{(C_{a0}+C_{b0}+4s^2LC_{a0}C_{b0})(1+sC_{a0}(R+sL))(C_{b0}+C_{a0}(-1+s^2LC_{b0})) \\
&\qquad \cdot(-2+sC_{b0}R+sC_{a0}(R-2sL+s^2LC_{b0}R)) \\
&\qquad\qquad \cdot\,(2+sC_{b0}R+sC_{a0}(R+2sL+s^2LC_{b0}R))^2\Big\}^{-1}\Bigg| \qquad (3.14)
\end{aligned}
$$

3.3 Linearity Performance of Single Varactor Diode

For a single varactor diode configuration, the nonlinear terms are no longer zero and are given by (3.15). And, the nonlinear terms can be calculated with Taylor series expansion as (3.1), (3.2).

$$C_{a0} = \frac{K_a'}{(\phi+V_r)^{0.5}} \qquad (3.15a)$$

$$C_{b0} = \frac{K_b'}{(\phi+V_r)^{0.5}} \qquad (3.15b)$$

Third order intermodulation distortion (IMD3) of the phase shifter from ADS

simulation and calculation (3.14) one are compared. First, when input power is swept, IMD3 from theory and simulation are shown in Fig. 3.3. The simulation with an ideal transformer, which has an infinite Q factor, shows excellent agreement with theoretical value. Even with non-ideal transformer, which is modeled with a S-parameters from ADS Momentum simulation, the difference from the calculated value is only approximately 2.5dB.

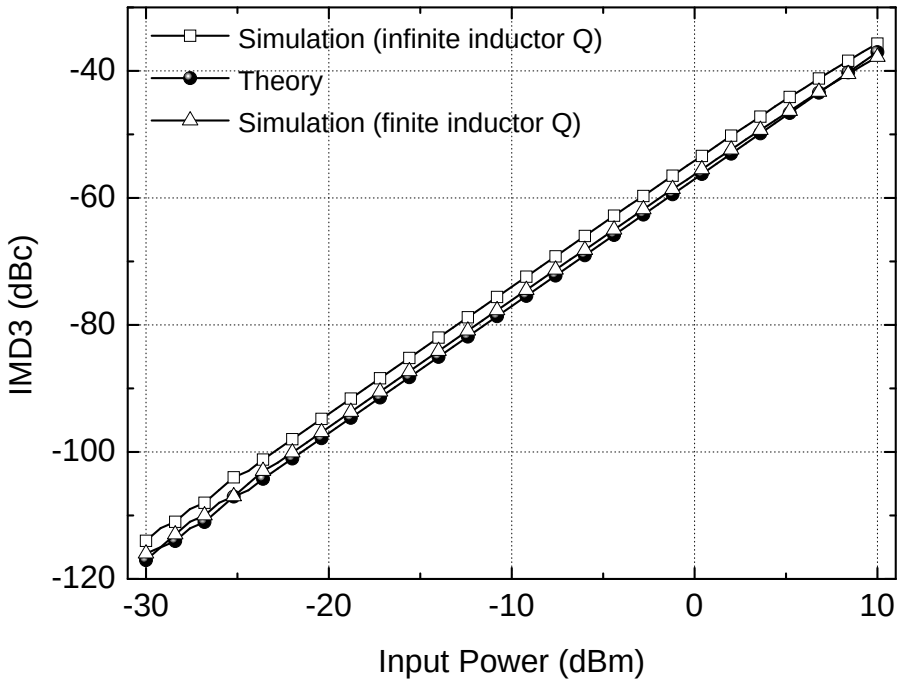
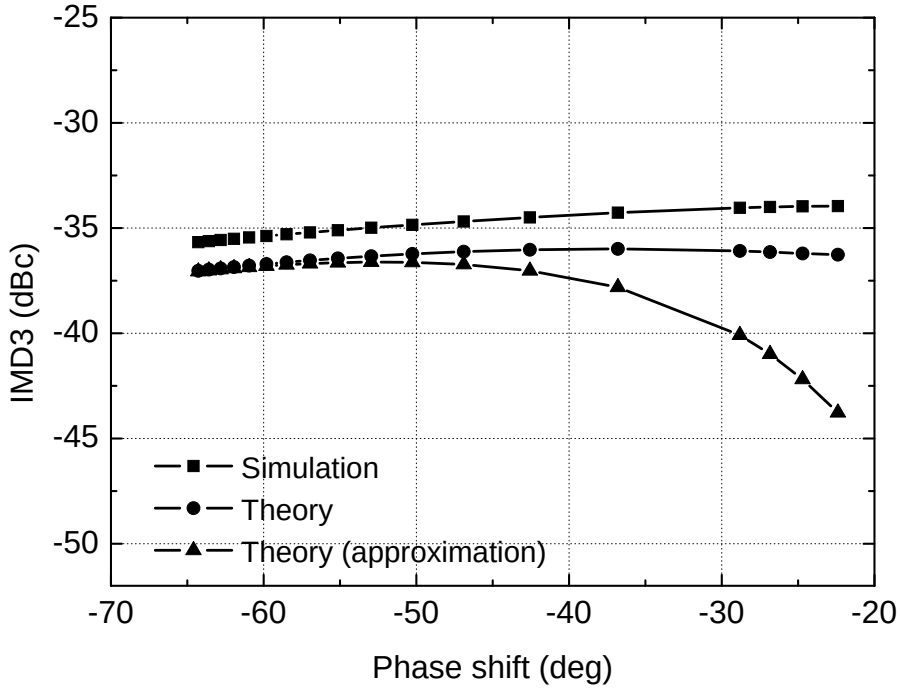


Figure 3.3: Simulated and calculated IMD3 when $\phi = -64^{\circ}$.

IMD3 is also simulated on different phase variations and compared with calculated values when the input power is 10dBm. Calculated IMD3 expressions with(app.) and without(exact) approximation are simulated together to see the validity of the simplified approximated IMD3. IMD3(exact), IMD3(app.), and simulated IMD3 with ideal transformer are shown in Fig. 3.4(a). The difference between simulation and theory (both IM3(exact) and IM3(app.)) are well below 2dB when the phase shift is approximately -60°. Beyond -30° phase shift, the IMD3(app.) shows increasing difference

from the simulated IMD3, while the IMD3(exact) maintaions its value to the simulation.

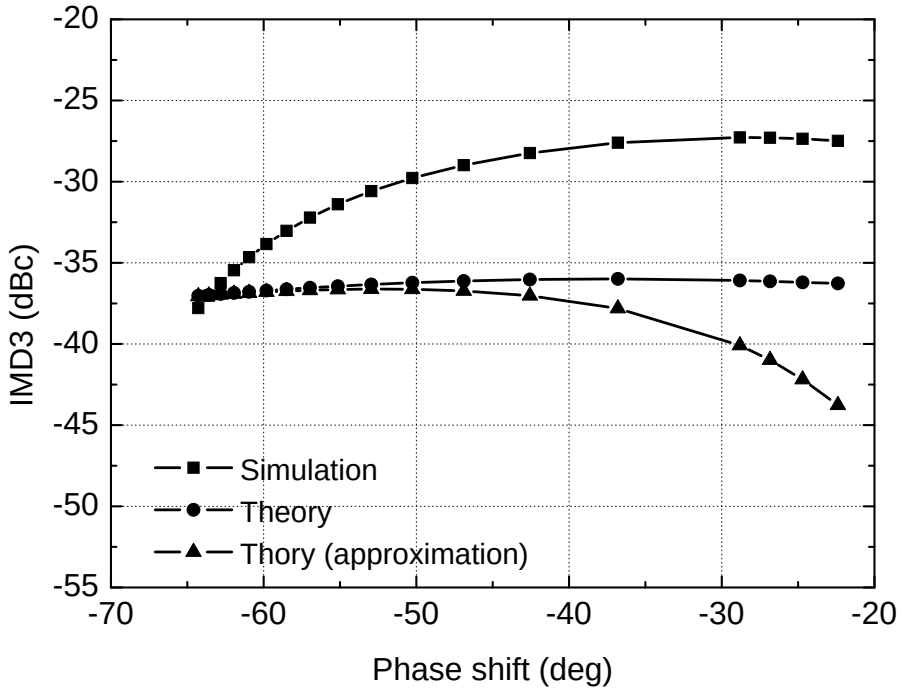
Simulated IMD3 with a finite Q factor transformer is also compared with calculated



(a)

Figure 3.4: (a) Simulated and calculated 3rd order intermodulation distortion and (b) its difference with ideal transformer.

IMD3 as shown in Fig. 3.5(a). Because parasitic resistance and capacitance in the magnetically coupled inductors break the assumption that the phase shifter input impedance matching is pefect in the calculation of the IMD3, the difference between theory and simulation is larger in this simulation. However, with marginal phase shift range, it still provides predictable IMD3 values.



(a)

Figure 3.5: (a) Simulated and calculated 3rd order intermodulation distortion and (b) its difference with parasitic extracted transformer.

3.4 Linearity Performance of Anti-series Two Connected Diodes

For anti-series connection of varactor diodes (Fig. 3.6), the nonlinear terms of the capacitance become zero, i.e. $C_{a1} = C_{a2} = 0$, $C_{b1} = C_{b2} = 0$ [22] when the ratio of the diode areas $\eta = D_x/D_y$ is unity. Then, the third-order Volterra kernel of V_{out} and $IMD3$ (3.13) are zero.

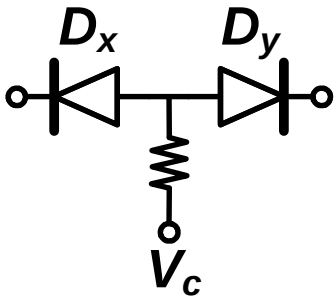


Figure 3.6: Anti-series connection of varactor diodes.

However, the ratio of the diode areas, η can deviate from the design value due to process variations. As a result, $C_{a1,b1}$ and $C_{a1,b1}$ are no longer zero and are given by

$$C_{a1,b1}/C_{a0,b0} = \frac{(1-\eta)}{2\,(1+\eta)\,(\phi+V_r)} \tag{3.16a}$$

$$C_{a2,b2}/C_{a0,b0} = \frac{3}{4}\left[\frac{(1-\eta)}{(1+\eta)\,(\phi+V_r)}\right]^2. \tag{3.16b}$$

Fig. 3.7 shows the normalized $C_{a1,b1}, C_{a2,b2}$ and IMD3 when η deviates from the ideal value. A 10% variation η degrades IMD3 to approximately -25dB.

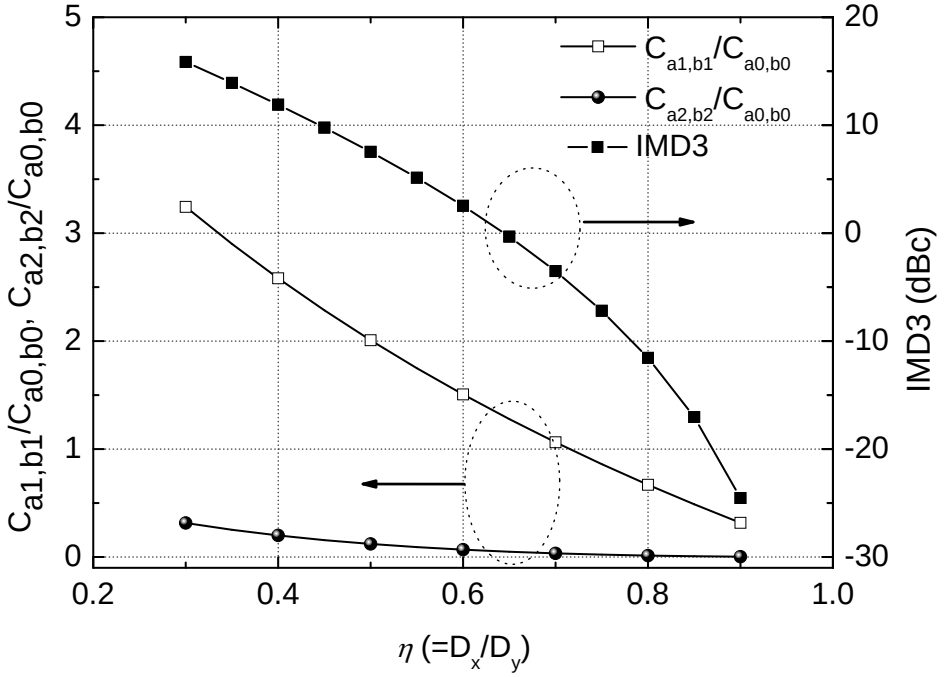


Figure 3.7: Relative 2nd, 3rd-order distortion and IMD3 on $\eta(= D_x/D_y)$ change P_{in}=10dBm).

3.5 Conclusion

Closed-form expressions have been presented for the third-order intermodulation product of the phase shifter using a Volterra series analysis, and are found to be in close agreement with the simulated response.

This chapter, in part or in full, is a reprint of the material as it appears in the following publication:

- Sunghwan Kim, Jawad H. Qureshi, Koen Buisman, Lawrence E. Larson and Leo C. N. de Vreede "Analysis of a Low-Distortion, Low-Loss Varactor Phase-Shifter Based on Silicon-on-Glass Technology", submitted to *IEEE Transactions On Microwave Theory and Techniques*, 2010.

- Sunghwan Kim and Lawrence E. Larson "A 44-GHz SiGe BiCMOS Phase-Shifting

Sub-Harmonic Up-Converter for Phased Array Transmitters", *IEEE Transactions. on Microwave Theory and Techniques*, May 2010.

The dissertation author was the primary researcher and the first author listed in the publication.

Chapter 4

SiGe HBT SubHarmonic Upconverter for Phased Array Transmitters

4.1 Introduction

Phased array systems are common in military radars to achieve electronic beam scanning and beam directivity control [44]. Traditionally, these systems were based on individual transmit/receive modules, which increased the cost and complexity and frequently required specialized discrete components. At high frequencies, GaAs technology was used to implement phased array transceivers.

As silicon technologies evolve, the f_T and f_{MAX} of CMOS and SiGe BiCMOS technologies exceeds 200GHz, which enables integration of millimeter-wave transceivers on chip [45]. In this case, commercial applications of phased array transceivers such as automotive collision avoidance and high data-rate directional point-to-point wireless communication networks operating at millimeter-wave frequencies become cost effective for the first time.

Recently, many highly integrated phased array transceivers were reported [46,

47, 48, 49, 50]. There are a variety of well-known architecture choices for these transceivers. The variable phase shift can be implemented in theLO-path [51, 46, 16], the RF-path [50, 18] or the IF-path [52, 53]. For any highly integrated transmitter, a zero-IF upconversion is preferred, despite some intrinsic drawbacks [54], because of its well known ease of filtering, low spurious emissions, and straightforward frequency agility. In phased array transmitters, the variable phase LO-path approach reduces the bandwidth, amplitude matching and linearity requirements on the phase shifter compared to implementation of a phase shifter in the RF-path. For zero-IF systems, a phase shifter in the IF-path would require a Hilbert transform, which is complicated to implement over a wide bandwidth. As a result of these considerations, an LO phase-shifting zero-IF upconverter is an attractive approach for future phased array transmitters. In the transmitter system of Fig. 4.1, a phase-shifting upconverter integrates upconversion I/Q mixers and an LO-path phase shifter. This architecture provides the potential for high flexibility as well as a small die area.

4.2 Transmitter Architecture

Fig. 4.1 shows a simplified architecture of the LO-path phase-shifting phased array transmitter. In this work, one element of the phase-shifting upconverter is implemented and analyzed in detail. The goal of the architecture is to minimize the distribution of high frequency signals on the silicon substrate. To reduce the LO signal loss in the distribution path and ease the LO distribution, the $\mathrm{LO}/2$ signal is distributed to the transmitter and then locally doubled. Baseband I/Q data is directly upconverted through direct upconversion mixers. Fig. 4.2 shows the block diagram of the 44GHz phase-shifting direct upconverter. It consists of a frequency doubler, polyphase (PP)

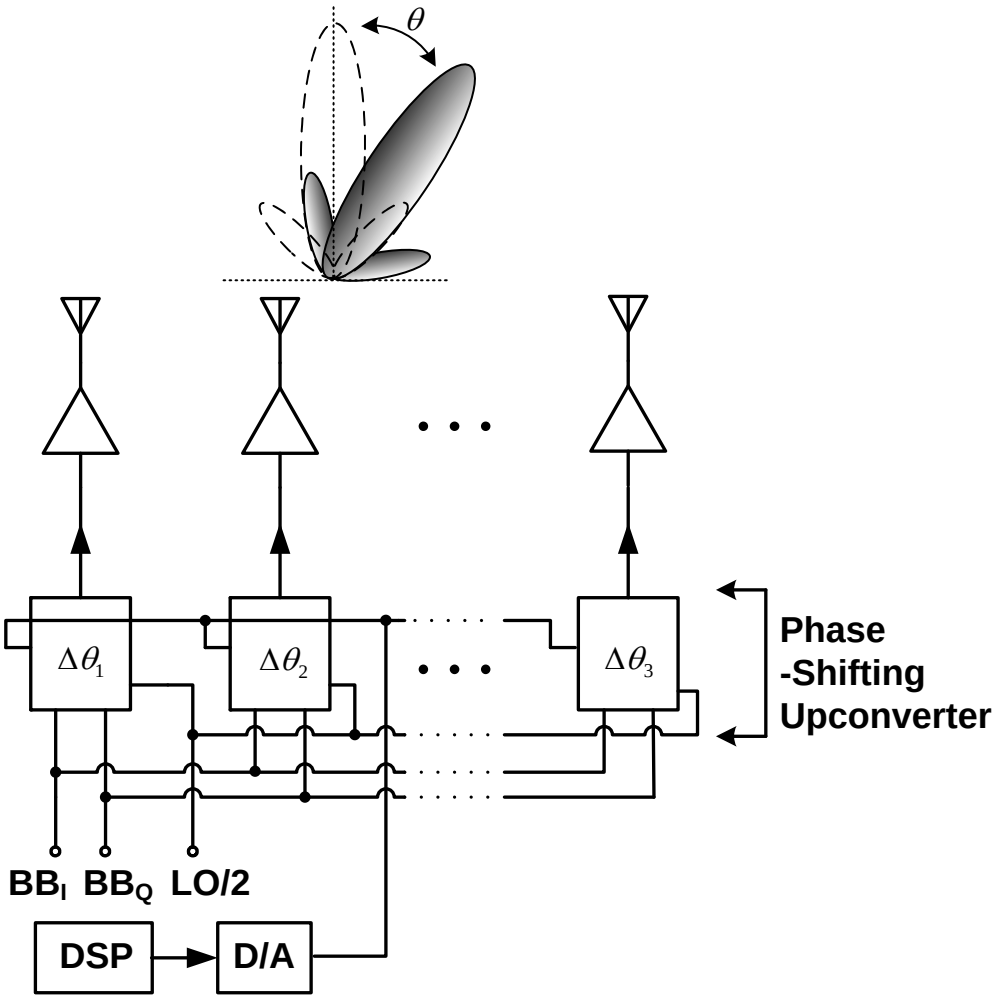


Figure 4.1: Architecture of the phased array transmitter.

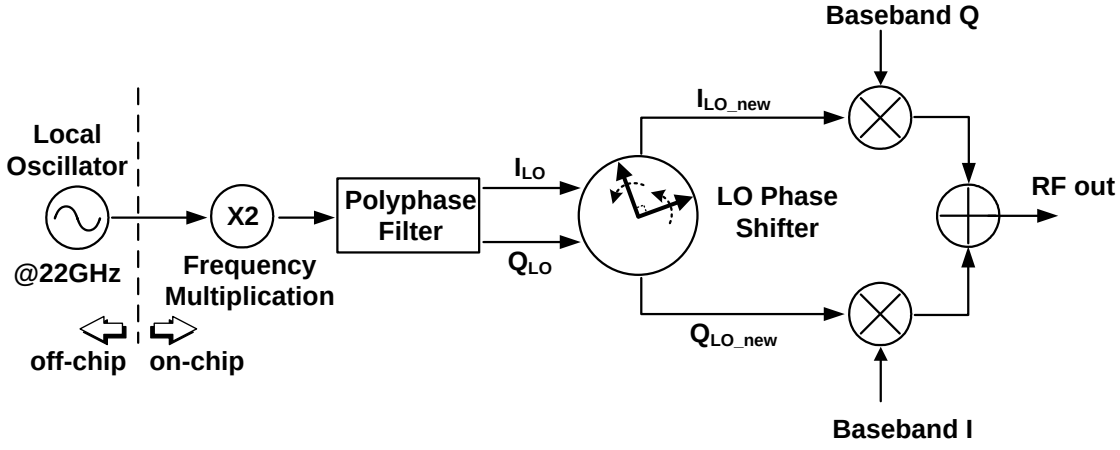


Figure 4.2: Block diagram of the proposed upconverter.

filter, LO phase shifter, I/Q mixers and differential-to-single-ended converter. A differential 22GHz LO signal is externally provided.

One of many design challenges in the integration of multiple transmitters for beamforming applications is to distribute the LO signals to each block of the transmitter. Amplitude and phase mismatches of the LO signals can be overcome through gain tuning of VGAs in the LO phase shifter in the transmitters. However, signal loss in the distribution lines is inevitable, and even worse at high frequencies. The conductive silicon substrate is a well-known cause of signal loss [55, 56]. Transmission lines and passive devices with shielding methods have been suggested to minimize the RF energy loss coupled into the substrate [57, 58, 59]. A sub-harmonic mixer can be a good solution to reduce the LO signal loss [60]. However, it requires 45°-phased LO signals, since the phase difference between I/Q paths is doubled. As an alternative, a frequency doubling circuit is adopted in the LO signal path. The new phase is achieved by adding two weighted quadrature vector signals. Several methods of quadrature signal generation have been developed; multistage (i.e., quadrature) voltage-controlled LC oscillators (VCO) [61, 62], a quadrature ring oscillator [63], a frequency multiplier and a divider in cascade [64], and a $\lambda/4$ transmission line. In a frequency multiplier-divider architecture, the output frequency of the frequency multiplier must be twice that of the LO signal. As a result, the size of the transmission line, as well as the inductors in LC oscillators, is large. Oscillator-based I/Q generation suffers from LO pulling by the PA's [65]. A polyphase (PP) filter consumes little physical area and generates I/Q LO signals. It is connected after the frequency doubler in the LO signal path.

4.3 LO Phase Shifter

4.3.1 Basic Concepts and Operations

To implement the I/Q upconverter, two *phase-shifted* quadrature LO signals are needed. These signals can be generated by the summation of two weighted orthogonal vectors, as shown in Fig. 4.3 [48, 66, 67].

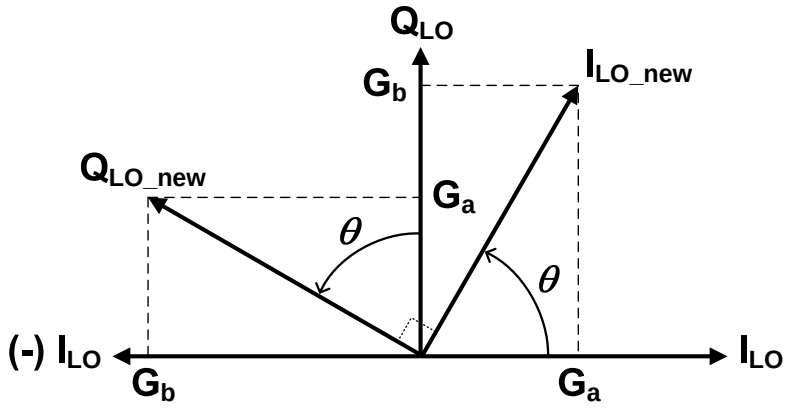


Figure 4.3: A vector with phase θ can be generated from two quadrature vectors.

The polyphase filter converts the differential LO into quadrature differential signals [68]. The quadrature differential signals at the output of the polyphase filter can be expressed as

$$[B_{pp}] = \begin{bmatrix} I_+ & I_- \\ Q_+ & Q_- \end{bmatrix} = A_{pp} \begin{bmatrix} \cos(\omega_{LO}t) & -\cos(\omega_{LO}t) \\ \sin(\omega_{LO}t) & -\sin(\omega_{LO}t) \end{bmatrix}, \tag{4.1}$$

where A_{pp} is the output amplitude. The desired phase shift is equivalent to rotation of

the basis vectors by θ $(0 \leq \theta < 2\pi)$ as shown in Fig.4.3. So the output is

$$\begin{aligned}\begin{bmatrix} Io_+ & Io_- \\ Qo_+ & Qo_- \end{bmatrix} &= G_v \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} [B_{pp}] \\ &= A_{pp} \begin{bmatrix} G_a & G_b \\ -G_b & G_a \end{bmatrix} \begin{bmatrix} \cos(\omega_{LO}t) & -\cos(\omega_{LO}t) \\ \sin(\omega_{LO}t) & -\sin(\omega_{LO}t) \end{bmatrix}, \end{aligned} \tag{4.2}$$

where G_v is the gain of the vector processing circuit and

$$\begin{aligned} G_a &= G_v \cos\theta \\ G_b &= G_v \sin\theta \end{aligned} \tag{4.3}$$

The operation of (4.2) can be realized with four VGAs as shown in Fig. 4.4(a).

4.3.2 Implementation of the LO Phase Shifter

The variable gain amplifier/summer is implemented with Gilbert cells as shown in Fig. 4.4(b). Two Gilbert cells share one differential inductor at the output of each I/Q path. Differential voltages V_{conta} and V_{contb} control the dc currents flowing through Q_1-Q_8. The control voltages do not change the dc bias current through the RF input devices (Q_9-Q_{12}), so the input impedance stays constant. The LO phase shifter is followed by common-collector (CC) stages, which raise the input impedance of the LO port.

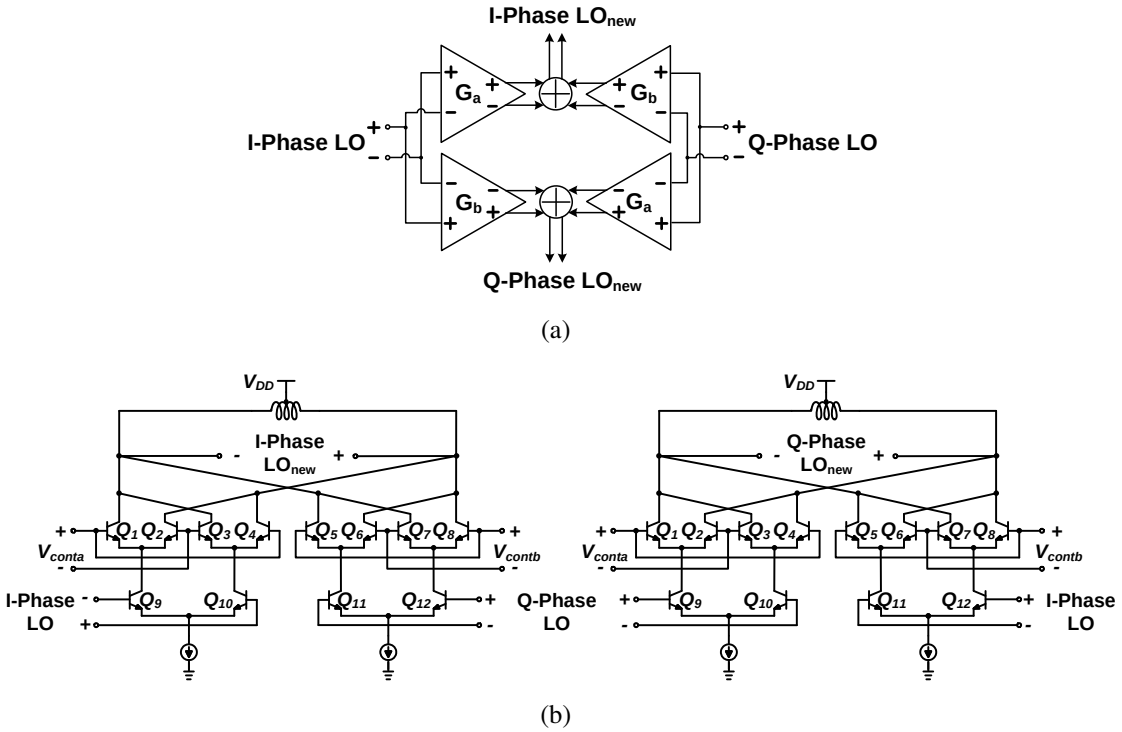


Figure 4.4: (a) Block diagram of the vector LO phase shifter and (b) circuit implementation of the vector LO phase shifter.

4.4 Error Analysis of the Phase Shifter

4.4.1 Quadrature Phase Error due to Polyphase Filter Phase Error

Random mismatches of the polyphase filter components are unavoidable, and become one source of quadrature phase error. To investigate this, let $\Delta\phi$ be the quadrature phase mismatch at the output of the polyphase filter. Then the basis vector $[B_{pp}]$

from (4.1) can be represented by its baseband equivalent as

$$[B_{pp}]_{\Delta\phi} = \begin{bmatrix} I_+ & I_- \\ Q_+ & Q_- \end{bmatrix} = A_{pp} \begin{bmatrix} e^{j0} & e^{j\pi} \\ e^{j(\pi/2+\Delta\phi)} & e^{j(3\pi/2+\Delta\phi)} \end{bmatrix} \tag{4.4}$$

By substituting $[B_{pp}]$ with $[B_{pp}]_{\Delta\phi}$ in (4.2), the output signal becomes

$$\begin{bmatrix} Io_+ & Io_- \\ Qo_+ & Qo_- \end{bmatrix}_{\Delta\phi} = G_{vs} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} [B_{pp}]_{\Delta\phi}$$
$$= A_{pp} G_{vs} \begin{bmatrix} \sqrt{1-\epsilon_A} e^{j\theta_I} & \sqrt{1-\epsilon_A} e^{j(\theta_I+\pi)} \\ \sqrt{1+\epsilon_A} e^{j\theta_Q} & \sqrt{1+\epsilon_A} e^{j\left(\theta_Q+\pi\right)} \end{bmatrix}, \tag{4.5}$$

where

$$\epsilon_A = \sin 2\theta \sin\Delta\phi \tag{4.6}$$

$$\theta_I = \pm\cos^{-1}\left(\frac{\cos\theta - \sin\theta\sin\Delta\phi}{\sqrt{1-\epsilon_A}}\right) \begin{cases} (+) : 0 \le \theta < \pi \\ (-) : \text{otherwise} \end{cases} \tag{4.7}$$

$$\theta_Q = \pm\left[\pi - \cos^{-1}\left(\frac{\sin\theta + \cos\theta\sin\Delta\phi}{\sqrt{1+\epsilon_A}}\right)\right] \tag{4.8}$$

$$\begin{cases} (-) : \pi/2 \le \theta < 3\pi/2 \\ (+) : \text{otherwise} \end{cases} \tag{4.9}$$

The phase mismatch of the PP filter ($\Delta\phi$) introduces a finite phase error θ_{err} at the output of the vector summation circuit, which is given by

$$\theta_{err}(\theta, \Delta\phi) = \left| \frac{\pi}{2} - |\theta_Q - \theta_I| \right| \tag{4.10}$$

The phase error $\theta_{err}(\theta, \Delta\phi)$ increases as the phase mismatch of the PP filter $\Delta\phi$ increases for a typical value of θ. The calculated phase error $\theta_{err}(\theta, \Delta\phi)$ along with a SPECTRE^{TM} simulation is plotted in Fig. 4.5(a), and the agreement is excellent. The maximum values of θ_{err} occur when $\theta = \frac{n\pi}{2}(n = 0, 1, 2, \ldots)$ while minimum values of θ_{err} occur when $\theta = \frac{\pi}{4} + \frac{n\pi}{2}(n = 0, 1, 2, \ldots)$.

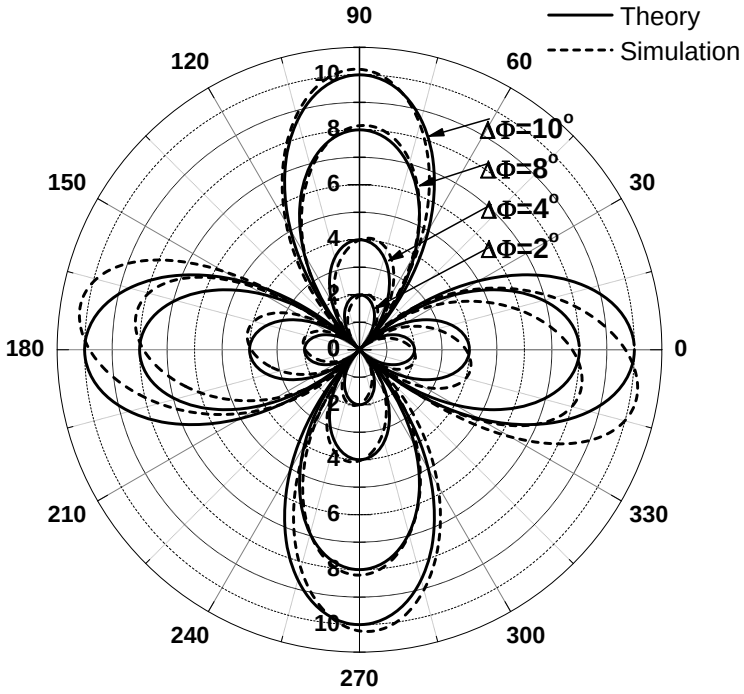
4.4.2 Phase Error due to Amplitude Mismatches

In addition to the quadrature phase mismatch, amplitude mismatch also affects the quadrature phase error.

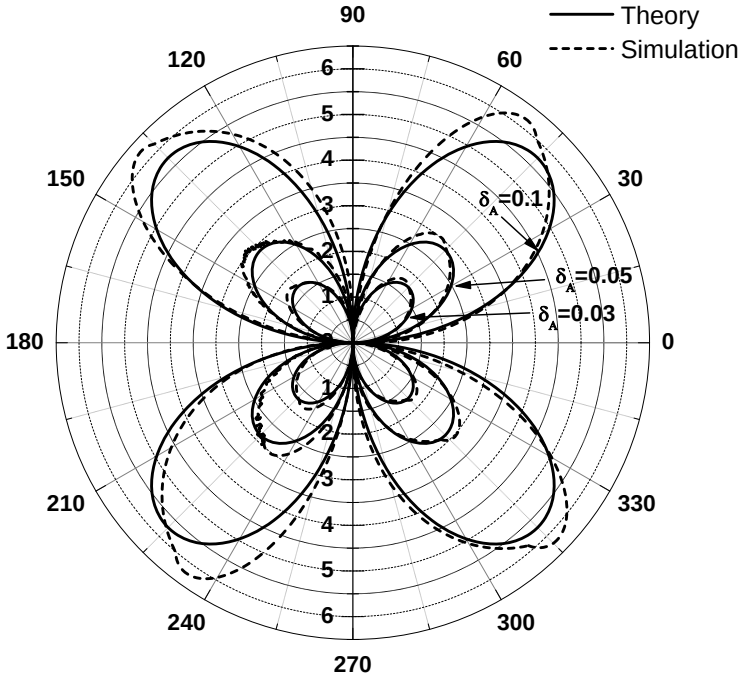
The mechanism of the phase error generation due to the amplitude mismatch can be analyzed as before. Let α be the ratio of the amplitude of the in-phase signal to the amplitude of the quadrature-phase signal, then the basis vector $[B_{pp}]$ can be modified as

$$[B_{pp}]_\alpha = \begin{bmatrix} I_+ & I_- \\ Q_+ & Q_- \end{bmatrix} = A_{pp} \begin{bmatrix} \alpha & -\alpha \\ j & -j \end{bmatrix}, \tag{4.11}$$

where $0 < \alpha \leq 1$. By substituting $[B_{pp}]$ with $[B_{pp}]_\alpha$ in (4.2), the output signal vectors



(a)



(b)

Figure 4.5: Simulated and calculated quadrature phase error at the output of the LO phase shifter as a function of the target phase θ (a) when $\Delta\phi = 2°$, $4°$, $8°$ and $10°$ and (b) when $\delta_A = 0.03, 0.05$ and 0.1.

become

$$\begin{aligned}\begin{bmatrix} Io_+ & Io_- \\ Qo_+ & Qo_- \end{bmatrix}_{\alpha} &= G_{vs} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} [B_{pp}]_{\alpha} \\ &= A_{pp} \begin{bmatrix} R_I e^{j\theta_I} & R_I e^{j(\theta_I+\pi)} \\ R_Q e^{j\theta_Q} & R_Q e^{j\left(\theta_Q+\pi\right)} \end{bmatrix}, \end{aligned} \tag{4.12}$$

where

$$R_I = \sqrt{(\alpha^2-1)\cos^2\theta + 1} \tag{4.13}$$

$$R_Q = \sqrt{(\alpha^2-1)\sin^2\theta + 1} \tag{4.14}$$

$$\theta_I = \pm\cos^{-1}\left(\frac{\alpha\cos\theta}{R_I}\right) \qquad \begin{cases} (+) : 0 \le \theta < \pi \\ (-) : \text{otherwise} \end{cases} \tag{4.15}$$

$$\theta_Q = \pm\left[\pi - \cos^{-1}\left(\frac{\alpha\sin\theta}{R_Q}\right)\right] \begin{cases} (-) : \pi/2 \le \theta < 3\pi/2 \\ (+) : \text{otherwise} \end{cases} \tag{4.16}$$

The amplitude mismatch introduces a finite phase error $\theta_{err}(\theta,\alpha)$, which is given by

$$\theta_{err}(\theta,\alpha) = \left|\frac{\pi}{2} - |\theta_Q - \theta_I|\right| \tag{4.17}$$

We define the amplitude mismatch as

$$\begin{aligned}\delta_A &= \frac{|A_I - A_Q|}{(A_I + A_Q)/2} \\ &= 2\left(\frac{1-\alpha}{1+\alpha}\right), \end{aligned} \tag{4.18}$$

where A_I and A_Q are the amplitudes of the in-phase and quadrature-phase signals, re-

spectively. Fig. 4.5(b) shows the simulated and calculated phase error as function of the target phase θ assuming 3%, 5% and 10% ($\delta_A = 0.03, 0.05$ and 0.1) amplitude mismatches. A 10% ($\delta_A = 0.1$) amplitude mismatch translates into 5.7° of the worst-case phase error at the output of the vector LO phase shifter.

4.5 Polyphase Filter Design

An RC polyphase (PP) filter is used, as shown in Fig. 4.6. Ideally, a one stage RC PP filter has 3dB voltage loss if an identical stage loads the output without buffering [68]. To make the filter less sensitive to RC variations, two or more stages can be chosen. In this case, a two-stage RC PP filter has 6dB voltage loss when an identical stage loads the output. Two of the input ports are grounded in the designed two-stage RC PP filter (Fig. 4.6).

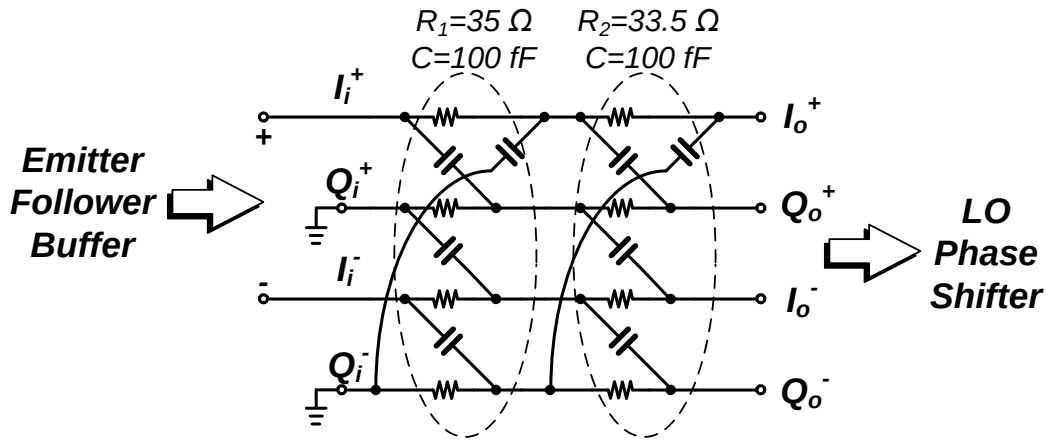


Figure 4.6: Schematic of two stage polyphase filter.

To compensate for the losses of the frequency doubler, a common-emitter (CE) stage with an inductive load, followed by an emitter-follower, is connected to the PP filter input.

At the pole frequency $\omega_\circ$, the RC product is expressed as

$$\frac{1}{\omega_\circ} = RC = \left[R_s \times \left(\frac{L_R}{W_R}\right)\right] \left[C_d \times L_C W_C\right], \tag{4.19}$$

where L_R and W_R are the length and width of the resistor, L_C and W_C are the length and width of the capacitor, C_d and R_s are MIM capacitor density, and the sheet resistance of the resistor, respectively. The approximate size of the PP filter is given by

$$S \cong 8\left(L_R W_R + L_C W_C\right). \tag{4.20}$$

From (4.19),

$$S(L_R, W_R) = 8W_R\left(L_R + \frac{1}{\omega_\circ R_s C_d L_R}\right). \tag{4.21}$$

Resistance variation occurs mainly because of width variation (ΔW_R) in the fabrication process. With large W_R, $\Delta W_R/W_R$ can be minimized, and so W_R=10μm is chosen. The minimum size of the PP filter (S_{min}) can be calculated from

$$\frac{\partial S(L_R, W_R)}{\partial L_R} = 0, \text{ then} \tag{4.22}$$

$$S_{min} = 16 W_R L_R, \tag{4.23}$$

when $L_R = 1/\sqrt{\omega_\circ R_s C_d}$. C_d is 1.0fF/μm^2 and R$_s$ is approximately 26$\Omega/\square$. From (4.23), L_R=12μm. As a result, R and C are approximately 30Ω and 120fF, respectively.

The input and output admittance of the PP filter is $(1+j)/R$ at the pole frequency $\omega_\circ$ [69]. The value of an inductor to resonate out this capacitance from the preceding

stage is given by

$$L = \frac{1}{\omega_\circ^2 C_{in}} = \frac{R}{\omega_\circ} \tag{4.24}$$

For $R = 30\Omega$, L becomes 110pH from (4.24). However, taking account of parasitic capacitance and the minimum inductance, it is necessary to increase L. Therefore, a slightly larger R and, consequently, a smaller C is chosen for the RC PP filter. The first and second stage have two different pole locations for wider bandwidth, at the expense of a small amplitude mismatch. Values of $R = 35\Omega$ at the first stage and $R = 33.5\Omega$ at the second stage are chosen.

4.6 Sensitivity of the Polyphase Filter

The variation of resistors and capacitors in the polyphase filter produces amplitude and phase errors at the output. To predict the statistical variation of the phase and amplitude mismatches, a Monte Carlo analysis including process and mismatch errors was carried out.

The simulated statistical distribution of the relative phase and gain of the quadrature outputs at 44GHz is shown in Fig. 4.7. The mean value of the I/Q phase difference is approximately 90° (Fig. 4.7(a)). However, the mean value of the relative gain ($|\frac{V_Q}{V_I}|$) corresponds to approximately 1.2% (Fig. 4.7(b)). A small gain error at 44GHz results from the fact that the first and second stage's pole frequencies were placed at the passband extremes centering 44GHz to increase the bandwidth [69].

Fig. 4.8 shows the simulated worst-case and average value of the relative phase and gain errors. The polyphase filter has good phase matching at the passband center (44GHz) — the mean value of the I/Q phase difference is 90°– with maximum phase

error of 2.2° at 44GHz (Fig. 4.8(a)). The gain is well matched at the two pole frequencies while the gain error is maximum around the center of the passband (Fig. 4.8(b)). The worst-case gain error is 1.8%.

The worst-case amplitude error in the passband results in a maximum phase error of 1.0° at $\theta = \frac{\pi}{4} + \frac{n\pi}{2}, (n = 0, 1, \ldots)$ at the output of the LO phase shifter. On the other hand, the worst-case phase error results in a maximum phase error of 2.2° at $\frac{n\pi}{2}, (n = 0, 1, \ldots)$ at the output of the LO phase shifter.

4.7 Frequency Conversion Circuits

4.7.1 Frequency Doubler

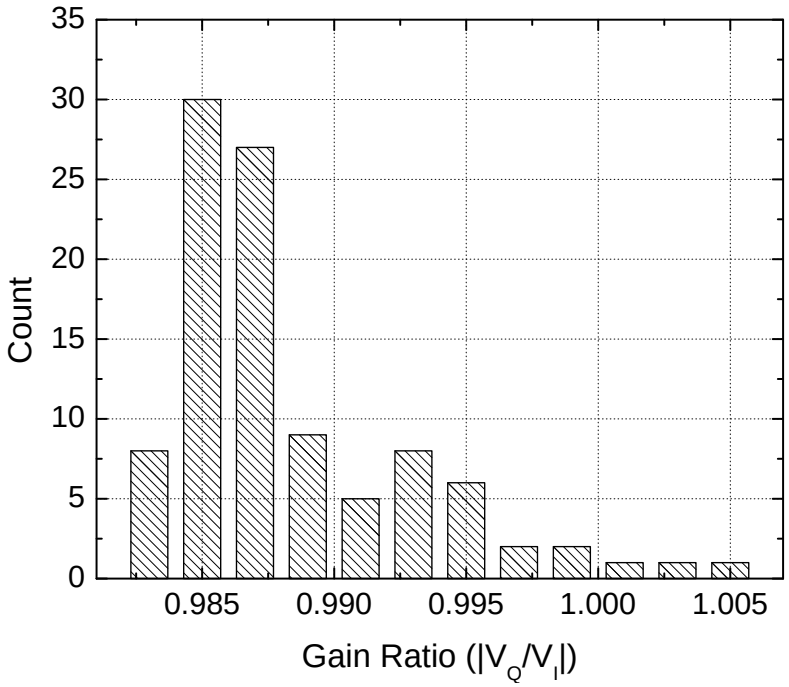
To convert the external 22GHz signal to 44GHz, a frequency doubler is implemented in Fig. 4.9. Since both the collectors and the emitters are tied together, odd harmonic currents of the transistors cancel out and only even harmonic currents exist. Assuming negligible base currents of Q_1 and Q_2,

$$I_{c1}(t) + I_{c2}(t) = 2I_{dc} + C_p \frac{\partial v_p}{\partial t}. \tag{4.25}$$

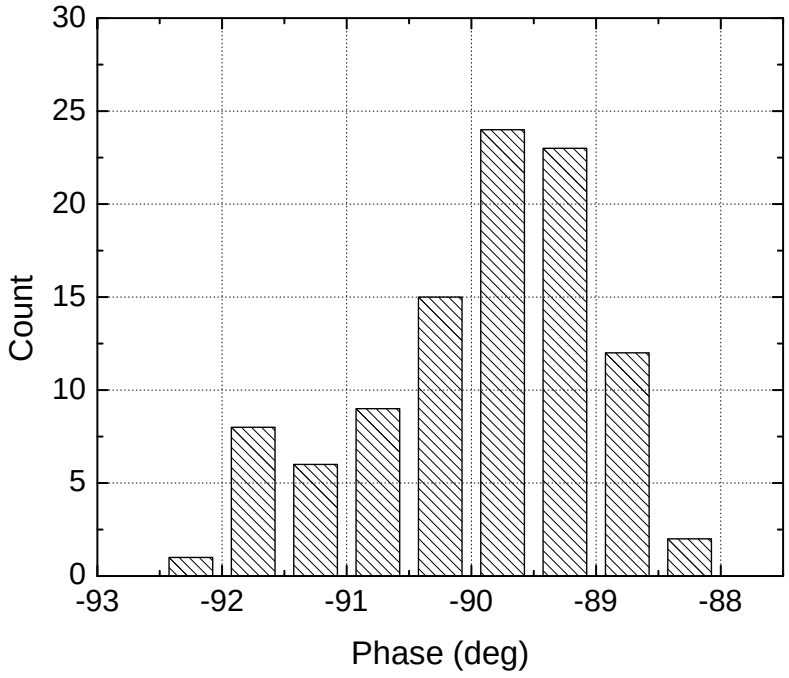
The left hand side of (4.25) can be expressed as

$$I_{c1}(t) + I_{c2}(t) = I_{dc} e^{-v_p(t)/V_T} \left[e^{v_{in}(t)/V_T} + e^{-v_{in}(t)/V_T} \right], \tag{4.26}$$

where $v_{in}(t)$ is the differential ac input voltage and $v_p(t)$ is the ac voltage at node P. For a sinusoidal input voltage, we assume that $v_{in}(t) = A_{in} V_T \cos(\omega t)$. Then, (4.26)

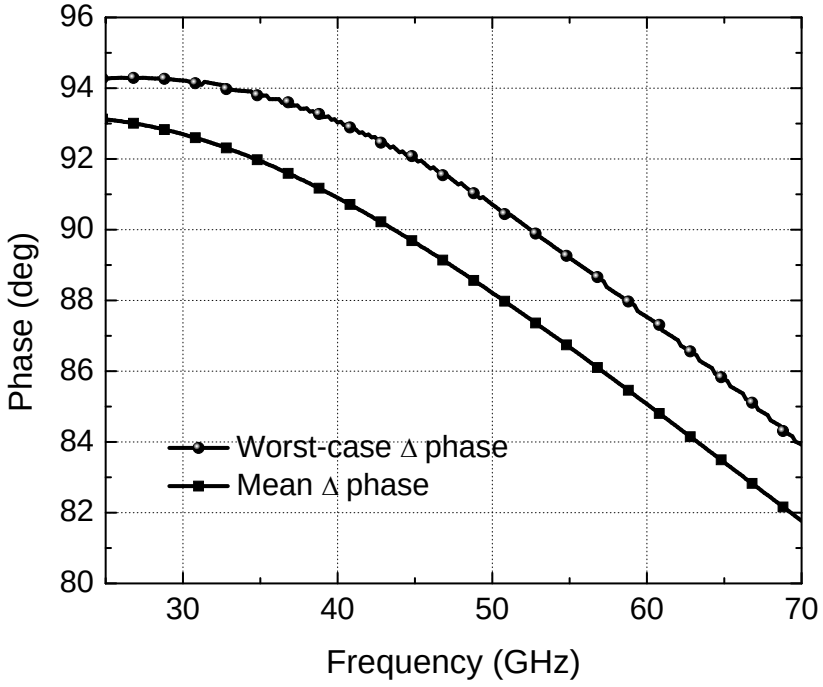


(a)

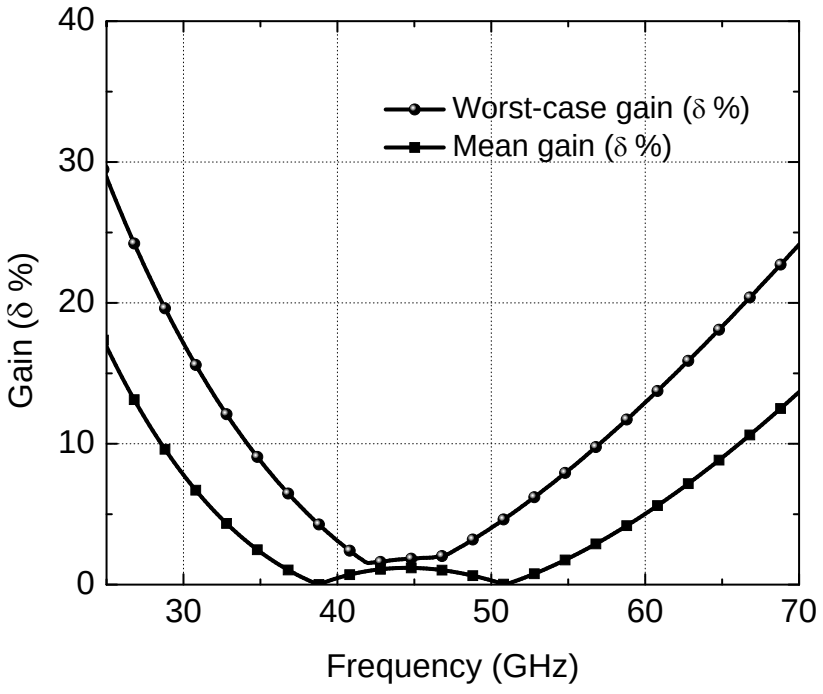


(b)

Figure 4.7: Histogram of the relative phase and gain of the polyphase filter at 44GHz. (a) phase error and (b) gain error.



(a)



(b)

Figure 4.8: Mean and worst-case Monte Carlo simulation results for the polyphase filter. (a) phase error and (b) gain error.

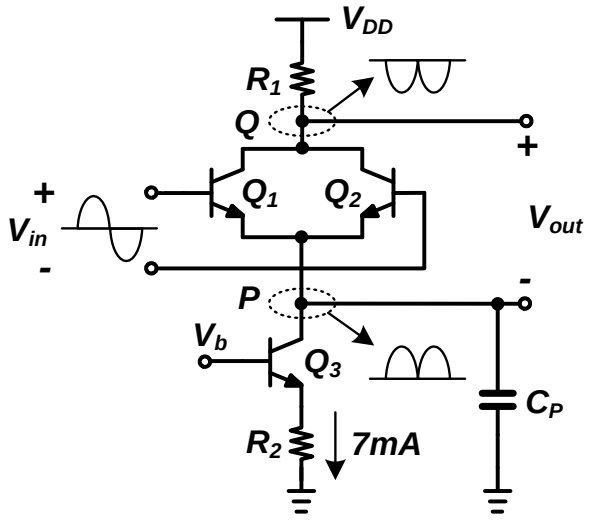


Figure 4.9: Schematic of the frequency doubler.

becomes

$$I_{c1}(t) + I_{c2}(t) = I_{dc} e^{-v_p(t)/V_T} \left[e^{A_{in}\cos(\omega t)} + e^{-A_{in}\cos(\omega t)} \right]. \tag{4.27}$$

Expansion of $e^{A_{in}\cos(\omega t)}$ gives

$$e^{A_{in}\cos(\omega t)} = I_0(A_{in}) + 2\sum_{n=1}^{\infty} I_n(A_{in}) \cos(n\omega t), \tag{4.28}$$

where the $\mathrm{I}_n(A_{in})$ are modified Bessel functions of the first kind of order n [70]. Then, the second term of the right hand side of (4.27) can be expanded in terms of the cosine function.

$$\begin{aligned} I_{c1}(t) + I_{c2}(t) = {} & 2I_{dc} e^{-v_p(t)/V_T} \\ & \times \left[I_0(A_{in}) + 2\sum_{n=1}^{\infty} I_{2n}(A_{in}) \cos(2n\omega t) \right]. \end{aligned} \tag{4.29}$$

For small $v_p(t)$, $e^{-v_p(t)/V_T}$ can be approximated by a series, and $v_p(t) = P_2 V_T \cos(2\omega t + \theta)$ can be assumed. Then,

$$I_{c1}(t) + I_{c2}(t) \approx 2I_{dc}(1 - P_2 \cos(2\omega t + \theta)) \times \left[I_0(A_{in}) + 2\sum_{n=1}^{\infty} I_{2n}(A_{in}) \cos(2n\omega t) \right]. \quad (4.30)$$

Expanding (4.30), the coefficients of $\cos(2\omega t)$, $\sin(2\omega t)$ are

$$I_{c1}(t) + I_{c2}(t) = 2I_{dc}[(2I_2 - P_2(I_0 + I_4)\cos\theta)\cos(2\omega t) + P_2(I_0 - I_4)\sin\theta \sin(2\omega t) + \ldots], \quad (4.31)$$

where the terminology $I_n = I_n(A_{in})$ has been adopted. So, neglecting higher order terms, (4.25) becomes

$$2I_{dc} + C_p \frac{\partial v_p}{\partial t} = 2I_{dc} - 2\omega C_p V_T P_2 \sin\theta \cos(2\omega t) - 2\omega C_p V_T P_2 \cos\theta \sin(2\omega t). \quad (4.32)$$

From (4.31) and (4.32),

$$2I_{dc}I_2 - I_{dc}P_2(I_0 + I_4)\cos\theta = -\omega C_p V_T P_2 \sin\theta \quad (4.33a)$$

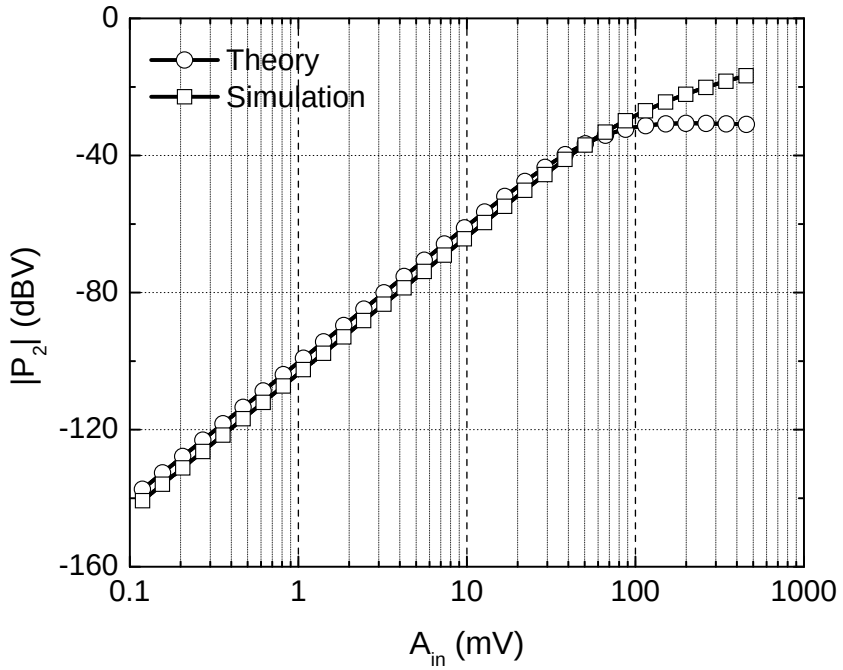
$$I_{dc}P_2(I_0 - I_4)\sin\theta = -\omega C_p V_T P_2 \cos\theta \quad (4.33b)$$

and therefore

$$|P_2| = 2I_{dc}I_2\frac{\sqrt{I_{dc}^2\left(I_0-I_4\right)^2+\left(\omega C_pV_T\right)^2}}{I_{dc}^2\left(I_0^2-I_4^2\right)+\left(\omega C_pV_T\right)^2} \tag{4.34}$$

$$\theta = \cos^{-1}\left[\frac{1}{P_2}\cdot\frac{2I_2\left(I_0-I_4\right)}{(I_0^2-I_4^2)+(\omega C_p/g_m)^2}\right]. \tag{4.35}$$

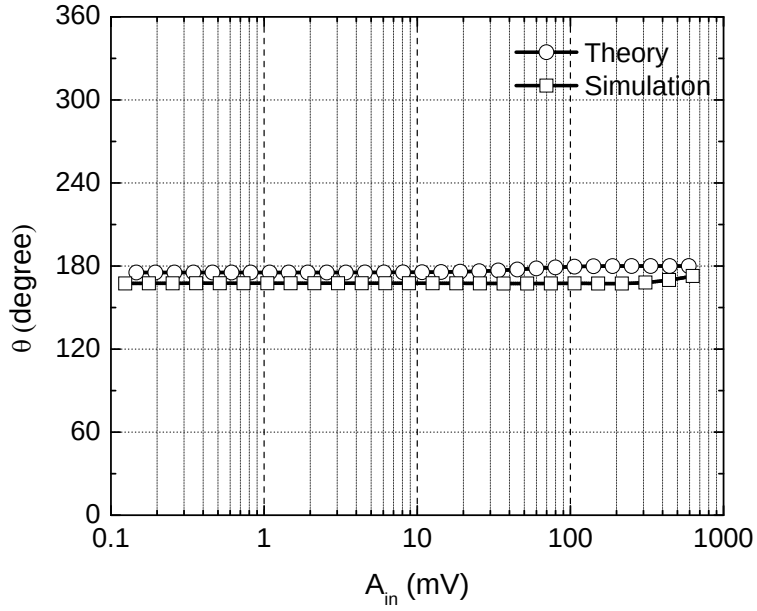
C_p determines the pole location for the second harmonic for a given bias and input



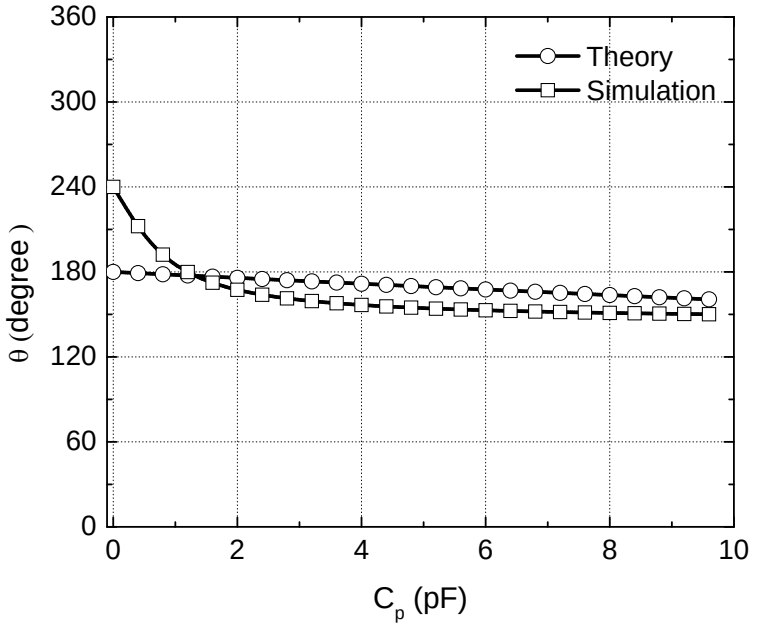
(a)

Figure 4.10: Second harmonic term P_2 at node P (v_p) as a function of A_{in} with C_p=100fF.

signal level. Fig. 4.10(a) shows the calculated and simulated values of P_2 versus A_{in}, and the agreement is excellent. The difference between the theoretical and simulated value of P_2 at high signal levels is attributed to the intrinsic base and emitter resistance and parasitic capacitance of the transistors, which was not included in the derivation. Up to 200fF of C_p, the variation of V_p is less than 2dB. Fig. 4.11(a) and Fig. 4.11(b)



(a)



(b)

Figure 4.11: (a) θ as a function of A_{in} with C_p=2pF and (b) θ versus C_p with A_{in}=50mV.

show the calculated and simulated values of θ versus A_{in} and C_p, respectively. It also shows good agreement.

Fig. 4.12(a) shows the simulated output harmonics. Fundamental and third harmonic tones (22GHz, 66GHz) are well suppressed compared to the even harmonics. The undesired fourth-harmonic tone (88GHz) increases faster than the second-harmonic tone as the input power increases, but it is suppressed in the following stage's inductive load.

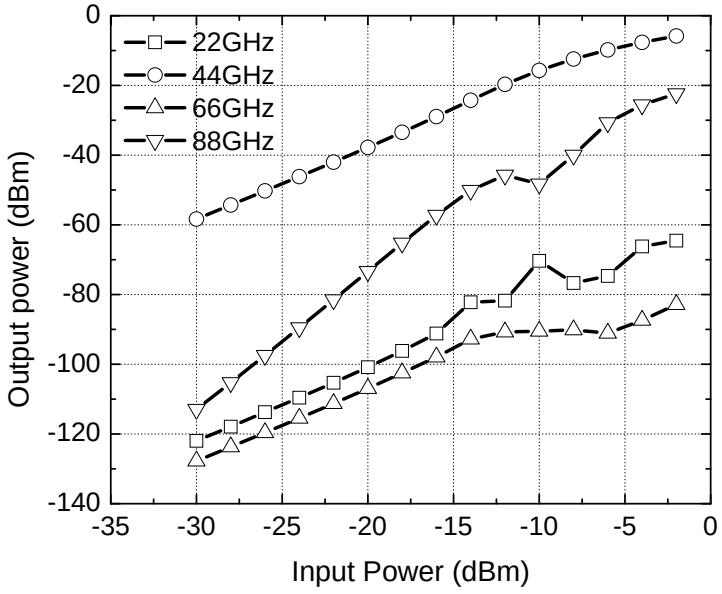
Due to imbalance in the impedance seen at the collector and the emitter at high frequencies, there are inevitable phase and amplitude imbalances. As shown by Fig. 4.12(b), simulations indicate approximately 9° phase error and 1dB amplitude imbalance at the carrier frequency for the second harmonic output. To reduce this effect, a balanced CE stage follows to diminish common-mode signals.

In order to minimize the area occupied by the frequency doubler, a resistive load is used rather than a passive on-chip inductor, at the expense of voltage headroom.

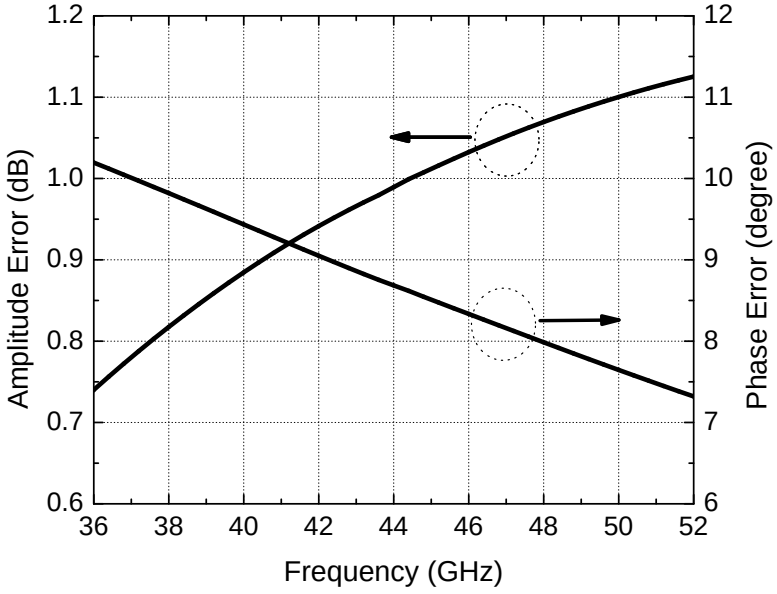
4.7.2 Upconversion Mixers

A double-balanced Gilbert-Cell mixer with an inductive load is implemented, as shown in Fig. 4.13. Once the dc bias current level is determined, the size of IF stage transistors are determined and the switching quad transistors are roughly half the size of the IF transistors for increased f_T to ensure fast switching. Differential resistive degeneration is employed to improve the linearity of the transconductor stages. The outputs of the mixer are tied together and connected to a CC buffer to reduce the loading effect of the following stages.

The switching quad transistors Q_1-Q_8 are sized 4.5μm $\times$ 0.2μm. And the transconductor transistors Q_9-Q_{12} are sized 5.4μm $\times$ 0.2μm. To resonate out the para-



(a)



(b)

Figure 4.12: (a) Simulated output signal harmonics versus input power in dBm for the stand-alone frequency doubler test circuit for f_{in}=22GHz and (b) simulated amplitude and phase error.

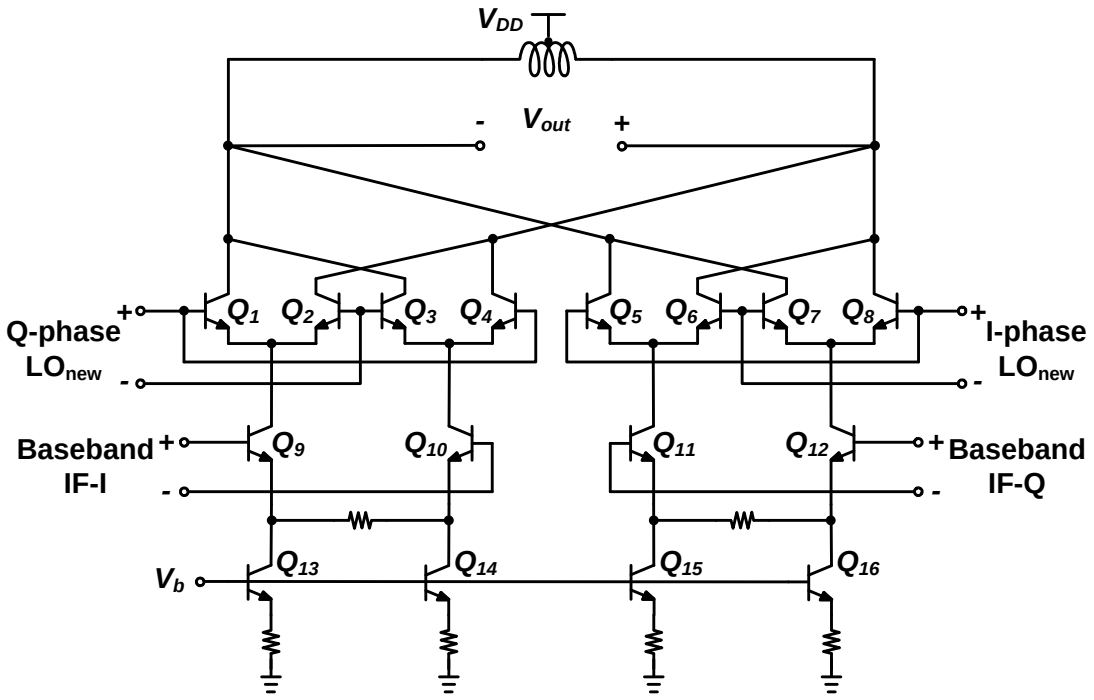
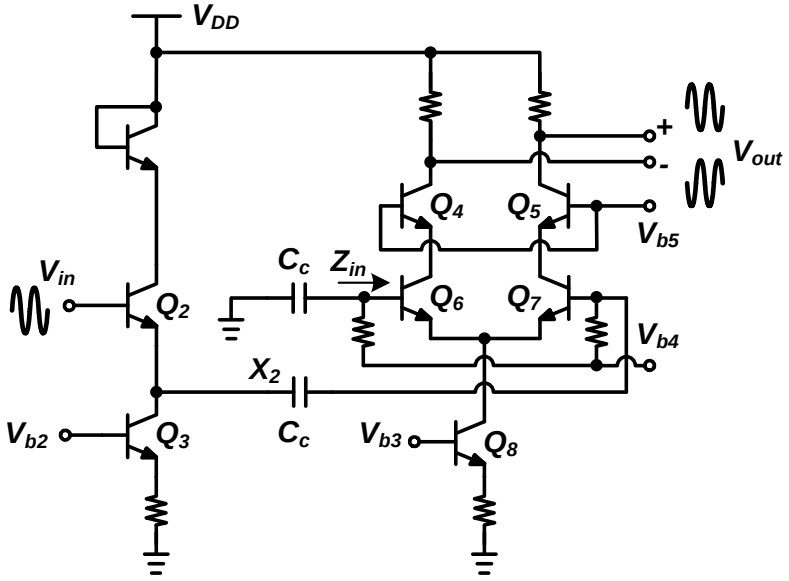


Figure 4.13: I/Q up-conversion mixer schematic diagram.

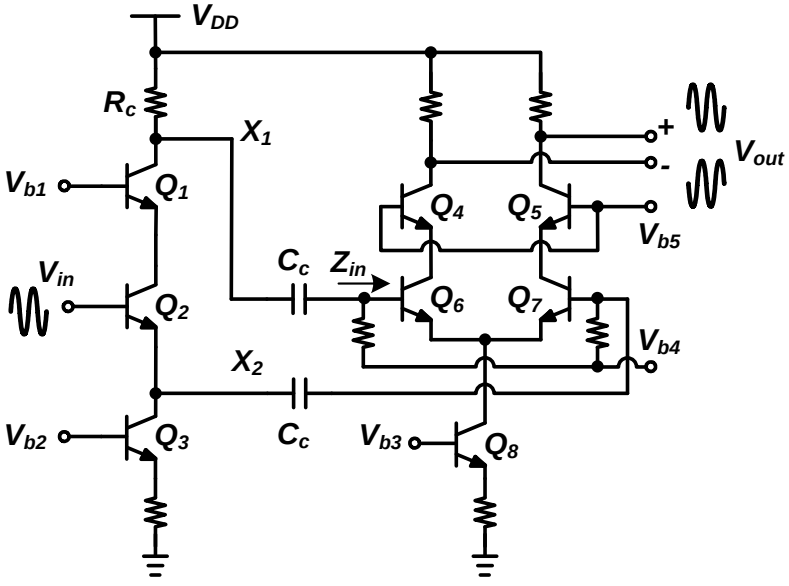
sitic capacitances at the output due to many switching quad transistors, 120pH inductors are connected at each output port. The bias current of each mixer is 9.8mA.

4.8 Input/Output Buffers

The phase-shifting upconverter includes a 22GHz single-ended-to-differential phase splitter at the LO input. An active balun can be obtained from the outputs of a differential CE stage as shown Fig. 4.14(b). In a conventional high-frequency active balun (Fig. 4.14(a)), transistors Q_2 and Q_3 compose an emitter-follower stage to reduce the return loss of the LO input port. In order to improve the gain of the active balun while maintaining dc bias current, transistor Q_1 is added as shown in Fig. 4.14(b). Assuming that the size of the transistors Q_2, Q_6 and Q_7 are the same, the voltage gain from the



(a)



(b)

Figure 4.14: (a) Typical active balun and (b) modified active balun.

input to the nodes X_1 and X_2 is given by

$$\frac{V_{X1}}{V_{in}} \approx -\left(\frac{R_c}{R_c + Z_{in}}\right)\left(\frac{\beta(\omega)}{2+\beta(\omega)}\right)\left(\frac{\beta(\omega)}{1+\beta(\omega)}\right) \tag{4.36}$$

$$\frac{V_{X2}}{V_{in}} \approx \frac{1+\beta(\omega)}{2+\beta(\omega)} \tag{4.37}$$

where $\beta(\omega) = \omega_T/j\omega$, R_c is the load resistance of the first stage in Fig. 4.14(b) and Z_{in} is the single input impedance of the differential CE stage in Fig. 4.14(b). Then, the gain improvement can be calculated as follows.

$$\begin{aligned} G_{imp} &= \left|\frac{(V_{X1} - V_{X2})/V_{in}}{V_{X2}/V_{in}}\right| \\ &= \left|1 + \left(\frac{R_c}{R_c + Z_{in}}\right)\left(\frac{\beta(\omega)}{1+\beta(\omega)}\right)^2\right|. \end{aligned} \tag{4.38}$$

For a 22GHz LO signal, the gain is roughly doubled. The simulated gain improvement is shown in Fig.4.15. The actual gain improvement is degraded because intrinsic emitter resistances and parasitic collector capacitances were not taken into account in the calculations. The phase difference between X_1 and X_2 deviate from 180° due to unequal impedances at nodes X_1 and X_2. The dc bias current for the active balun is 13mA.

A 44GHz differential-to-single-ended output buffer, which is shown in Fig. 4.16, is implemented at the output of the upconverter. A 12Ω resistor is placed between the emitter of Q_1 and the output in order to improve S_{22} at the cost of reduced gain. The resulting VSWR is approximately 1.3:1 with 10% fractional bandwidth. The dc bias current is 8mA.

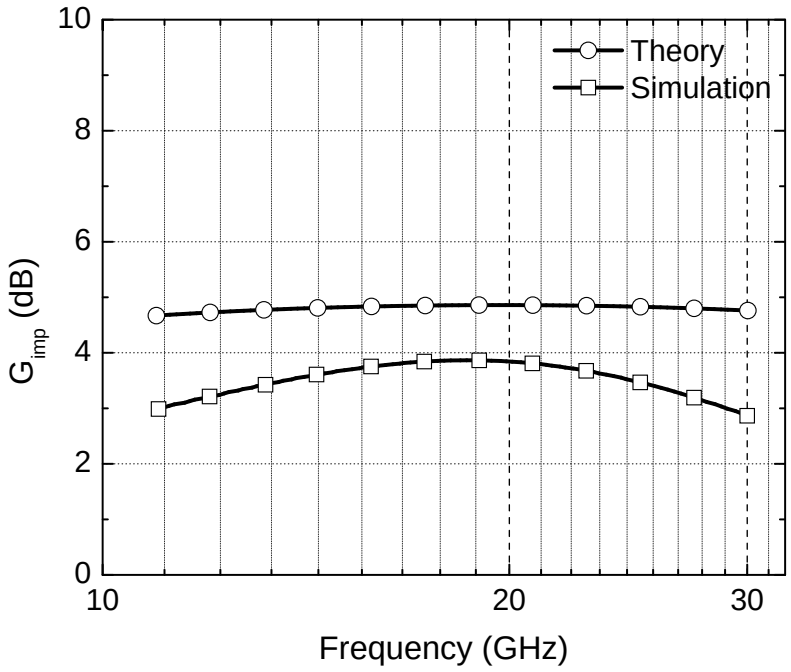


Figure 4.15: Gain improvement of Fig. 4.14(b) compared to Fig. 4.14(a).

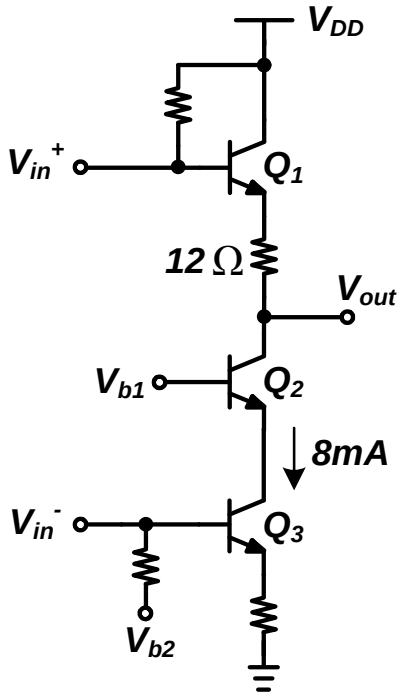


Figure 4.16: Differential-to-single-ended converter at the system output.

4.9 Experimental Results

This phase shifting upconverter has been designed using 0.12μm BiCMOS process (SBC18HX) from Jazz Semiconductor, which features a peak f_T and f_{MAX} of the SiGe HBT of nearly 150GHz and 200GHz, respectively [71]. The process has six metal layers with two thick 1.6μm and 2.8μm aluminum layers as top metals. The breakdown voltages are BV_{CEO} $\approx$ 2.2 V and BV_{CBO} $\approx$ 7 V. The substrate resistivity is 8 Ω·cm.

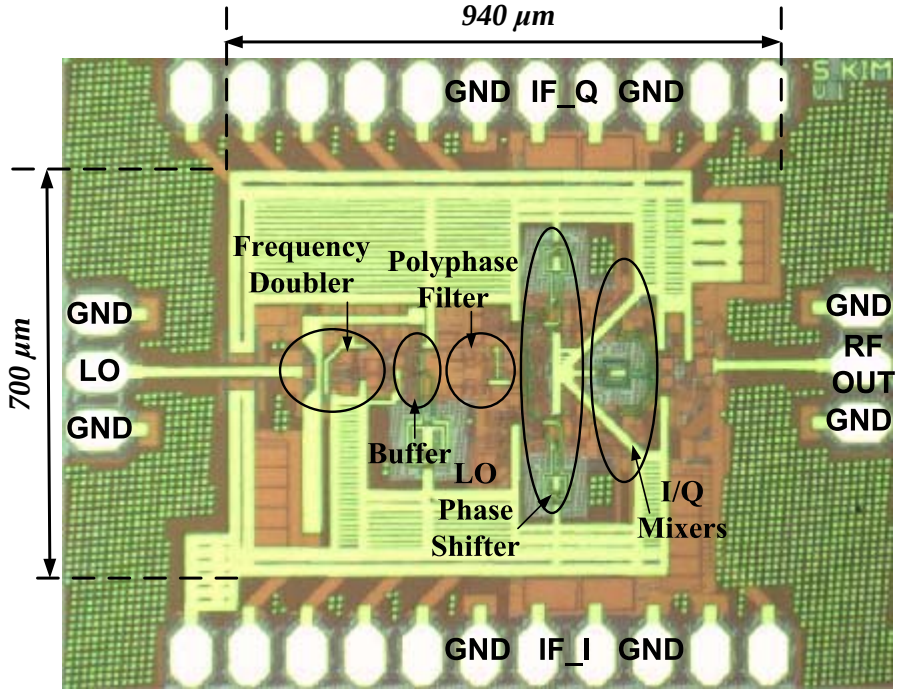


Figure 4.17: Microphotograph of the phase-shifting upconversion mixer

The microphotograph of the fabricated die is shown in Fig. 4.17. The core size, excluding the pads and on-chip coupling capacitors for IF I/Q inputs is 940 $\times$ 700 μm^2. The measurement setup is shown in Fig. 4.20. And Fig. 4.21 shows a microscope picture

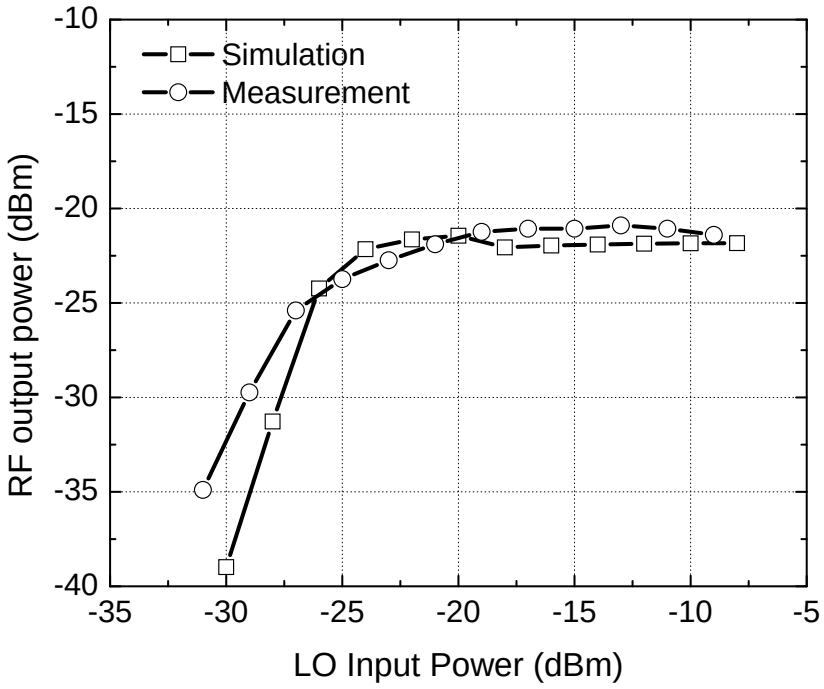


Figure 4.18: Output power(dBm) versus LO power(dBm) at 45GHz, Pif=-38.5dBm, f_{LO}=22GHz

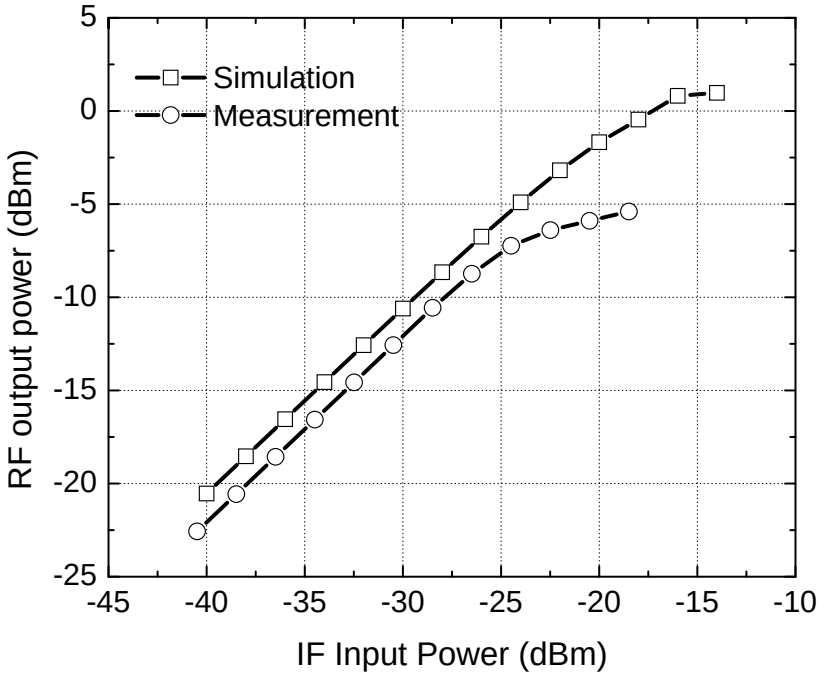


Figure 4.19: Output power(dBm) versus input power(dBm) at 45GHz

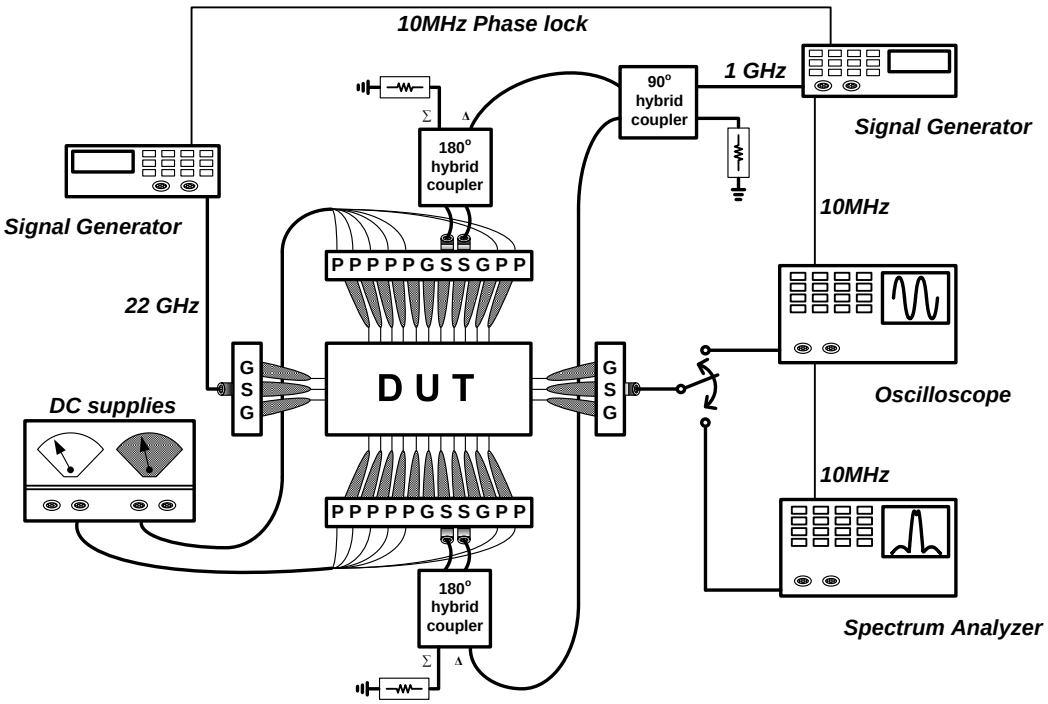


Figure 4.20: Measurement setup of the upconverter

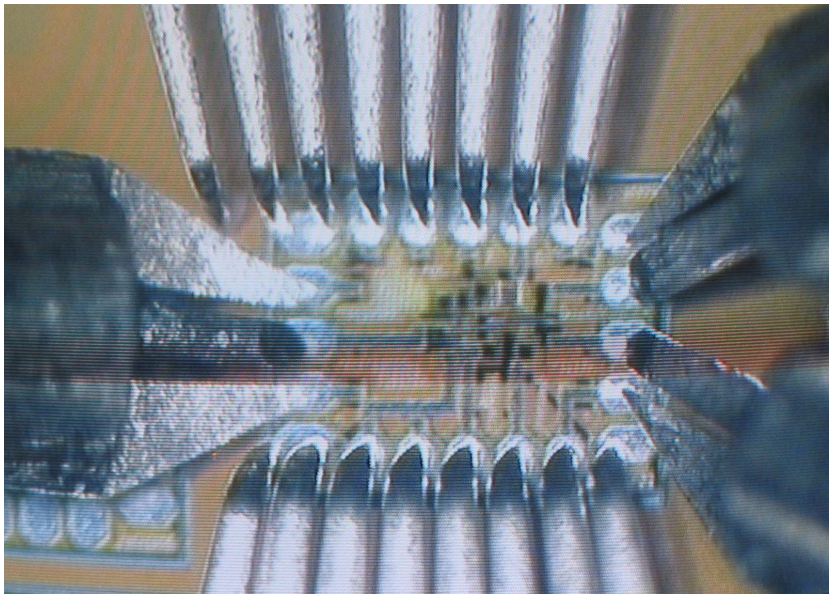


Figure 4.21: Probe measurement: probes contacting each pad.

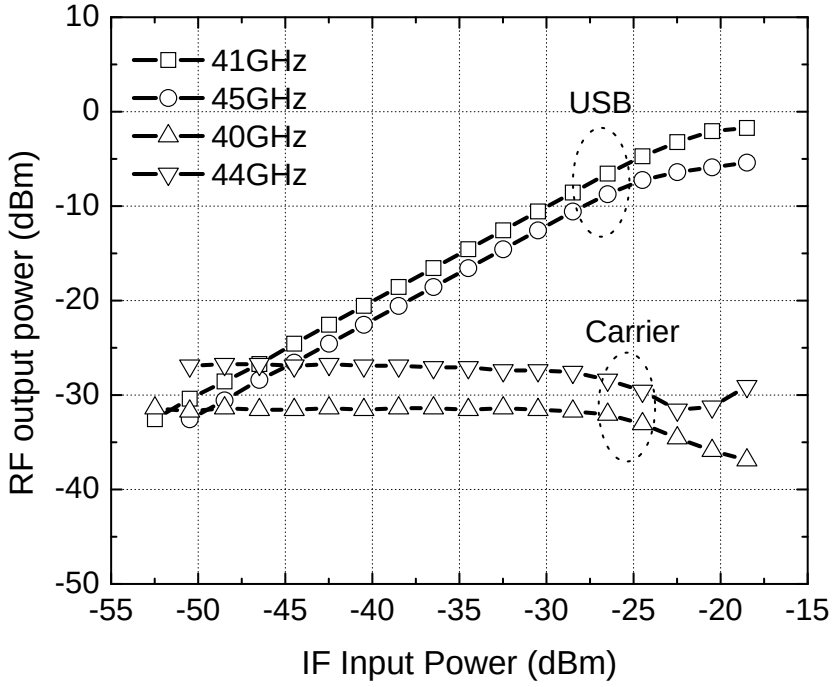


Figure 4.22: Measured output power(dBm) versus input power(dBm) at LO=22GHz, 20GHz.

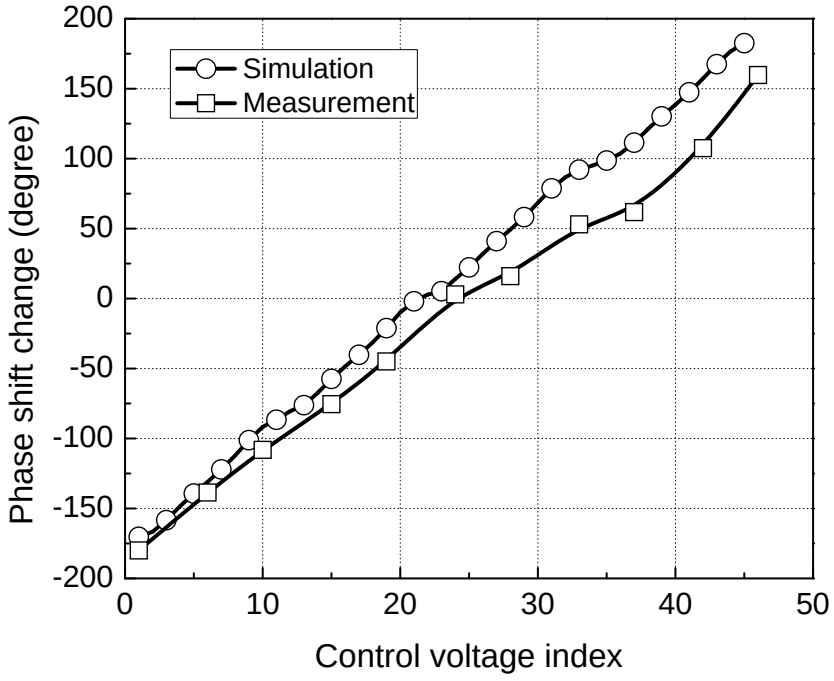


Figure 4.23: Measured and simulated output phase shift at 45GHz as a function of control voltage.

of probes contacting each I/O pad. The IF-RF gain is maximized with a minimum LO power of -25dBm, as shown in Fig. 4.18 The measured conversion gain of the SSB direct upconverter is approximately 15dB as shown in Fig. 4.19, and its peak RF output power at 45GHz is -5dBm. The LO leakage at 44GHz was also measured and is approximately -30dBm as shown in Fig. 4.22. The LSB suppression is greater than 12dB, and was limited by imperfect I/Q LO phase match. At 41GHz, its peak RF output power is -1.7dBm and the conversion gain is 18.3dB. Roughly 340° phase-shift variation with little amplitude variation is confirmed. The measured and simulated phase shift are plotted in Fig. 4.23. The partial disagreement between simulated and measured phase shift can be reduced after a calibration of the control voltages.

4.10 Conclusion

A 44GHz phase-shifting sub-harmonic upconverter block for phased array transmitters based on a direct conversion architecture and LO phase-shifting has been presented in a SiGe HBT technology. Phase errors in the LO phase shifter due to I/Q mismatches of RC PP filter were investigated. It was demonstrated that a continuous 360° phase shift could be achieved with a direct frequency conversion through two external control voltages. The circuit demonstrated -5dBm output power with a compact die area of 940$\times$ 700 μm^2 at a dc power consumption of 786mW. The measurements confirm that the proposed phase-shifting upconverter approach may potentially play an important role in applications with phased array transmitters. It also confirms that SiGe HBT process technology is useful and attractive for millimeter-wave applications.

This chapter, in part or in full, is a reprint of the material as it appears in the following publication:

- Sunghwan Kim and Lawrence E. Larson ”A 44-GHz SiGe BiCMOS Phase-Shifting Sub-Harmonic Up-Converter for Phased Array Transmitters”, *IEEE Transactions. on Microwave Theory and Techniques*, May 2010.

The dissertation author was the primary researcher and the first author listed in the publication.

Chapter 5

An 8-Element Phased Array Transmitter with an Injection-locked Quadrature Frequency Multiplier

5.1 Introduction

Several monolithic millimeter-wave phased array transmitter IC's have been demonstrated recently for radar and communications applications [48, 72, 18, 73, 52, 53, 17]. These transmitters often require variable phase shifters in the RF, LO or IF-path, which should exhibit low loss and low dc power consumption. Typically, RF and LO-path phase shifters require a low-loss transmission line structure along with amplifiers to compensate for power loss during signal distribution, which increases at higher working frequencies. In the previous work, a frequency doubler was used to multiply the LO frequency, which would be distributed from a system phase-locked loop (PLL). The frequency doubler suffered significant power loss while LO distribution at half the carrier frequency allows less signal loss during feeding to each element. In addition to

that, a polyphase filter followed by the frequency doubler to generate quadrature signals is a lossy passive component.

TO further reduce the power loss of the frequency doubler and the polyphase filter, a frequency doubling injection-locked quadrature oscillator, which can be used at each transmitter element to reduce power consumption and LO signal loss during distribution, is proposed. Specifically, this oscillator functions as a quadrature frequency doubler, which generates differential quadrature outputs from a single differential signal input. The frequency doubler and the polyphase filter in the previous work are substituted with this single oscillator. Each gain stage in the oscillator works as a frequency doubler while four stages structure of the oscillator enables differential quadrature signals at the output. Regenerative operation of the oscillator enables the frequency multiplication with smaller LO input power, and hence reduce overall LO power loss. This work describes a millimeter-wave phased array transmitter with a new injection-locked quadrature frequency doubler.

5.2 Phased Array Transmitter Architecture

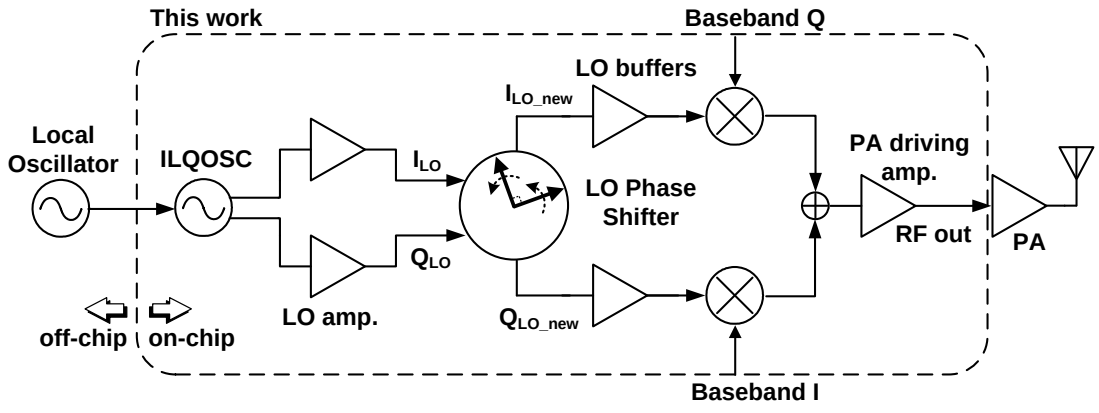


Figure 5.1: Architecture of one proposed transmitter element (of eight).

Fig. 5.1 shows the architecture of the proposed transmitter. A differential LO signal is converted to differential I/Q signals at twice the LO input frequency in the injection-locked quadrature frequency doubler. An active phase shifter, which is composed of four independently controlled VGA's, uses the I/Q signals to generate phase-shifted I/Q LO signals for the up-conversion mixers. Eight of these proposed phased array transmitters are integrated on-chip. One differential LO input port and one I/Q baseband input are shared for the phased array transmitter.

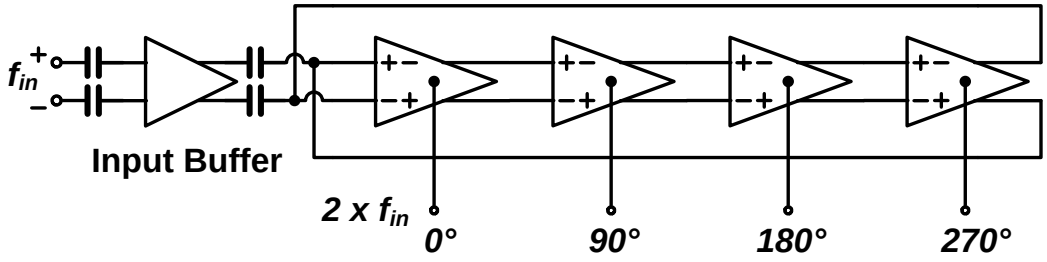
5.3 Circuit Design

5.3.1 Injection-locked Quadrature Oscillator

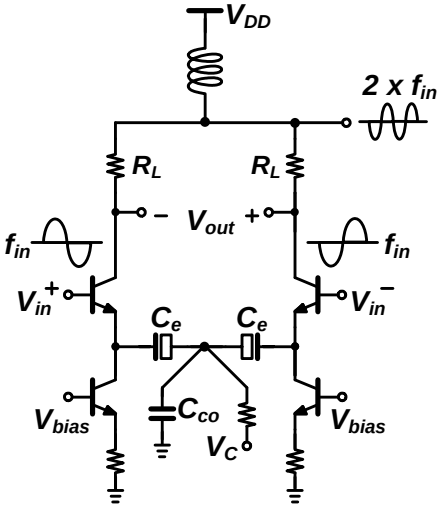
In the injection-locked quadrature oscillator, resistively loaded differential amplifiers are connected in a ring as shown in Fig. 5.2(a). The first stage is also connected to an LO input buffer to lock the oscillator to the off-chip LO signal.

While each differential amplifier in the ring is operating at f_{in} under injection-locked conditions, the second harmonic tone is extracted at the common-collector node, with an inductive load, as shown in Fig. 5.2(b). Since the phase shift across each stage is 45° under locked conditions, the phase difference across each stage for the *second-harmonic* tone (at 2xf_{in}) is 90°. Hence, the first (second) and third (fourth) stage's output form a differential output at the doubled frequency and differential I(Q) are obtained. The inductor in the first (second) and the third (fourth) stage's 2xf_{in} port are merged into one transformer to save chip area. The fact that the injection-locked quadrature oscillator is oscillating at half the LO frequency also mitigates the VCO pulling problem [74].

One potential limitation of this approach is the limited frequency locking range



(a)



(b)

Figure 5.2: (a) Block diagram of the injection-locked quadrature ring oscillator, (b) schematic of a differential gain stage with capacitive degeneration.

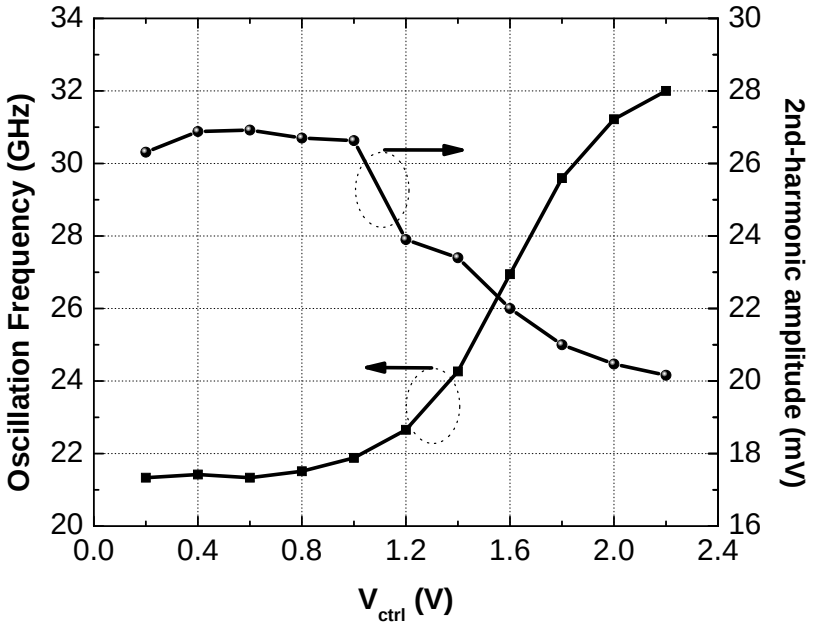


Figure 5.3: Simulated oscillation frequency and second-harmonic output amplitude variation with control voltage.

of the oscillator. While a wider locking range can be achieved by increasing the injection power [74] or multiple injection points [75], these techniques involve design challenges such as power loss during distribution of the larger injected signal and more complicated routing when multiple injection-locked oscillators share a common LO input.

A wider input bandwidth for the frequency multiplier can be achieved as shown in Fig. 5.2(b) by tuning the free-running frequency, by changing the pole location of each gain stage.

The capacitively-degenerated gain stage has a negative input resistance,

$$R_m \cong -\left|\beta(\omega)\right| / \left(\omega \left(C_e \| C_{co}\right)\right). \tag{5.1}$$

The free-running frequency is given by

$$f_o \cong \frac{(1+Q_{in}^2)}{2\pi Q_{in}^2 \left[R_L \| \left(r_b + R_m\right)\left(1+Q_{in}^2\right)\right] C_t}, \tag{5.2}$$

where $Q_{in} = \left[\omega \left(r_b + R_m\right) C_t\right]^{-1}$, R_L is the load resistance of the gain stage, r_b is the base resistance, and C_t is $(C_\pi \| C_e \| C_{co})$. By adjusting the variable degeneration capacitors (C_e), the total resistance — and hence the free-running frequency — of the oscillator changes. Fig. 5.3 shows how the free-running oscillation frequency and the amplitude of the second-harmonic output signal changes with MOS varactor tuning.

A small capacitor (C_{co}) is added at the node formed between the two degeneration capacitors (see Fig. 5.2(b)) to increase second-order harmonic currents at the output node. However, the capacitance must be properly sized to prevent common-mode oscillations.

5.3.2 LO Amplifier

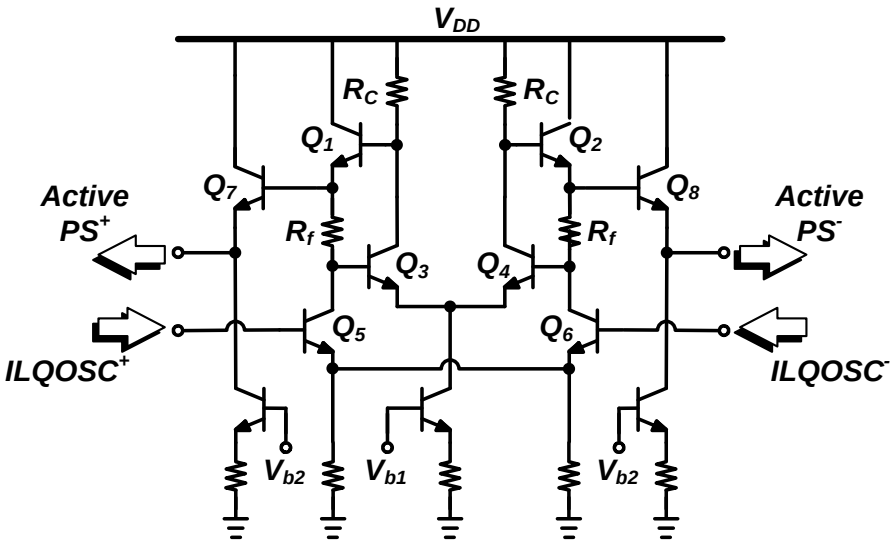


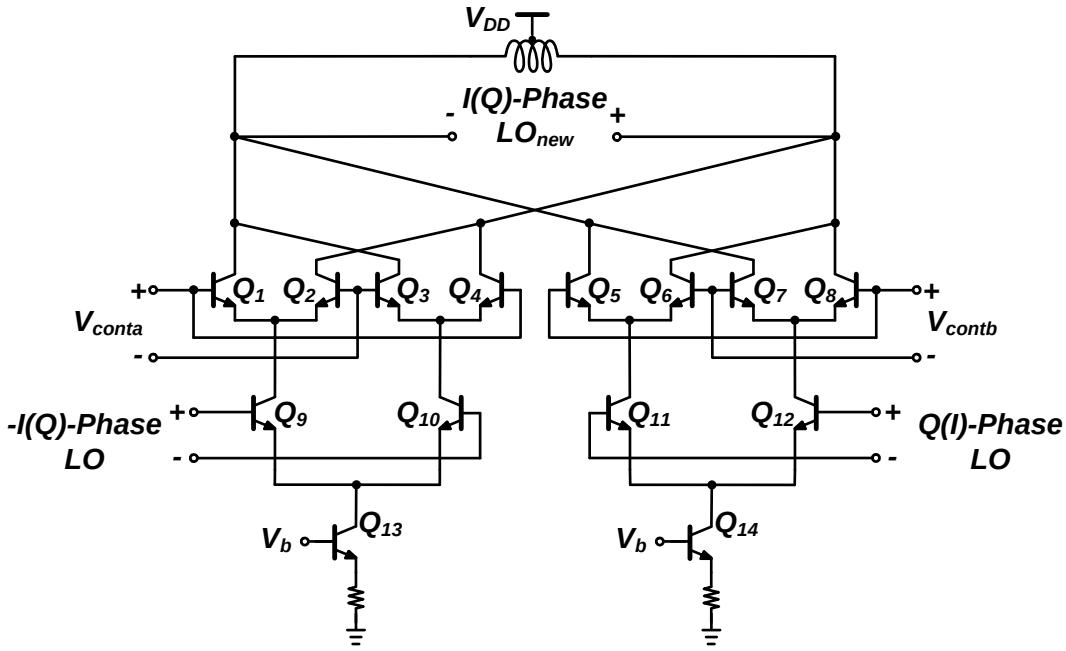
Figure 5.4: Schematic of LO boosting amplifier.

An LO amplifier follows the injection-locked quadrature oscillator. A conventional common-emitter amplifier with an inductive load would have a relatively narrow bandwidth. To reduce chip area and power-consumption, a negative feedback Cherry-Hooper topology [76] was adopted, as shown in Fig. 5.4. Negative feedback formed by Q1 (Q2) and R_f enhances the bandwidth up to the carrier frequency 50GHz. The bias current of this amplifier is 8.8mA from the 3.2V power supply voltage.

5.3.3 Active LO Phase Shifter

The active LO phase shifter is implemented using an orthogonal vector summation technique, which is based on the summation of two weighted quadrature vector signals [17]. The preceding injection-locked quadrature oscillator generates differential I/Q signals for this vector summation. The variable gain amplifier (VGA) is implemented with Gilbert cells as shown in Fig. 5.5(a). Two Gilbert cells share one differential inductor at the output of each I/Q path. Differential voltages V_{conta} and V_{contb} control the dc currents flowing through Q_1-Q_8.

For target phase shifts, both I-VGA and Q-VGA keep the same values of V_{conta} and V_{contb} when the quadrature signal from the injection-locked quadrature oscillator has no I/Q phase mismatches. The moderate I/Q phase mismatch due to PVT variation can be corrected by tuning I-VGA and Q-VGA independently. The control voltages do not change the dc bias current through the RF input devices (Q_9-Q_{12}), so the input impedance stays constant. The bias current of each VGA is 9mA from the 3.2V power supply voltage.



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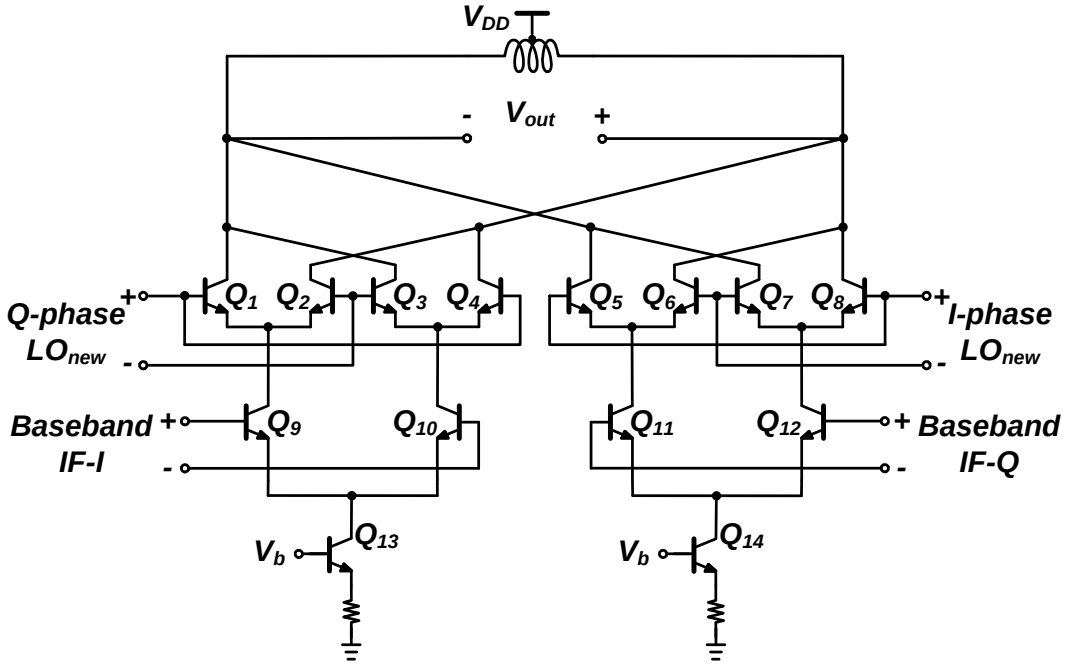
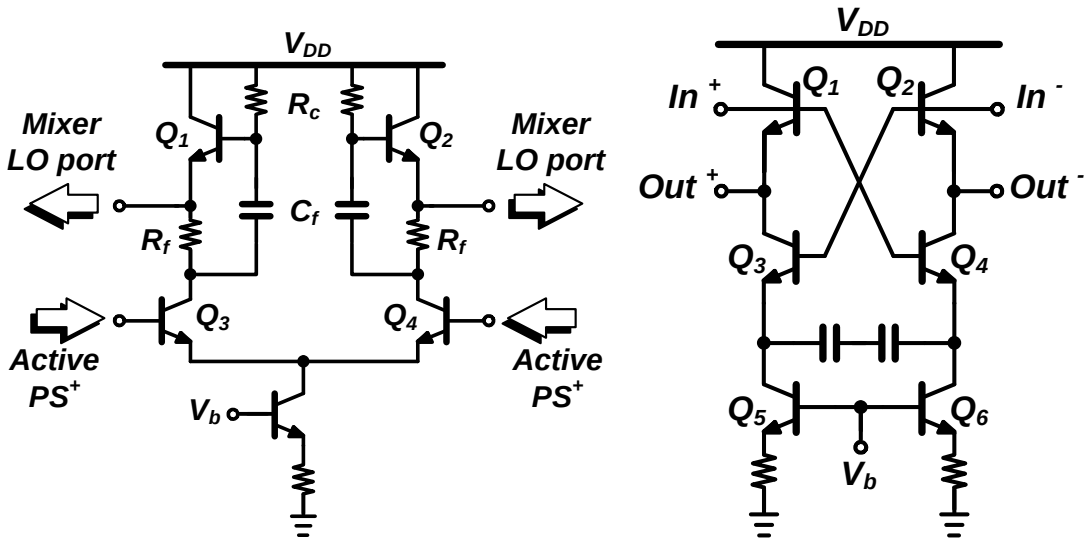


(b)

Figure 5.5: (a) Active phase shifter (b) double balanced mixer (c) LO Buffer with improved stability and (d) output amplifier.



(a) (b)

Figure 5.6: (a) Active phase shifter (b) double balanced mixer (c) LO Buffer with improved stability and (d) output amplifier.

5.3.4 Up-conversion Image Rejection Mixer

A double-balanced Gilbert-Cell mixer with an inductive load is implemented, as shown in Fig. 5.5(b). The switching quad transistors are roughly half the size of the IF transistors for increased f_T to ensure fast switching. The outputs of the mixer are tied together and are connected to the output amplifier. To resonate out the parasitic capacitances, a 150pH differential inductor is connected at the output. The bias current of each mixer is 9.5mA from the 3.2V power supply voltage.

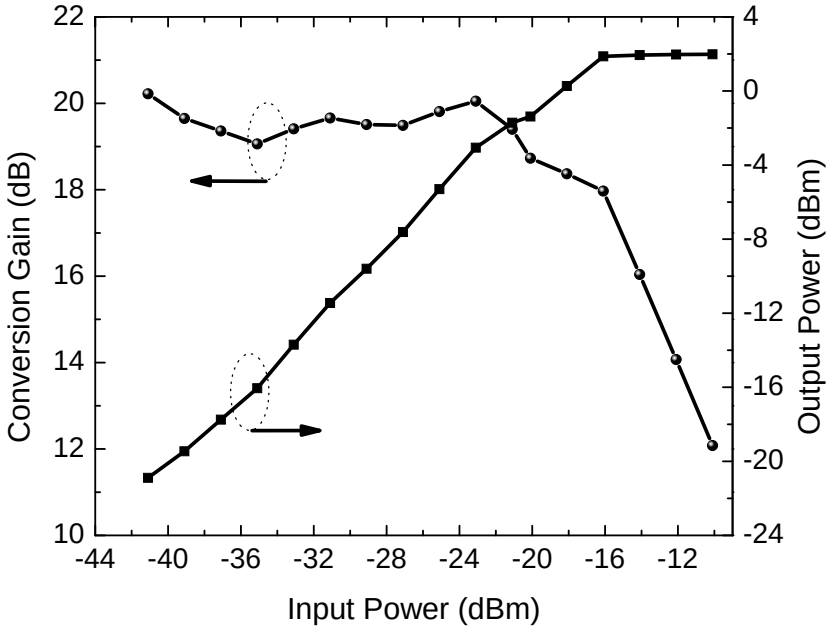
5.3.5 LO Buffer and Output Amplifier

A cascade of common-emitter (CE) and common-collector (CC) stage is a widely used topology to drive switches in active current steering mixers. Due to the high quality factor of the passive inductor load of the active phase shifter, a CC stage followed by the active phase shifter would be prone to instability due to the potentially negative real

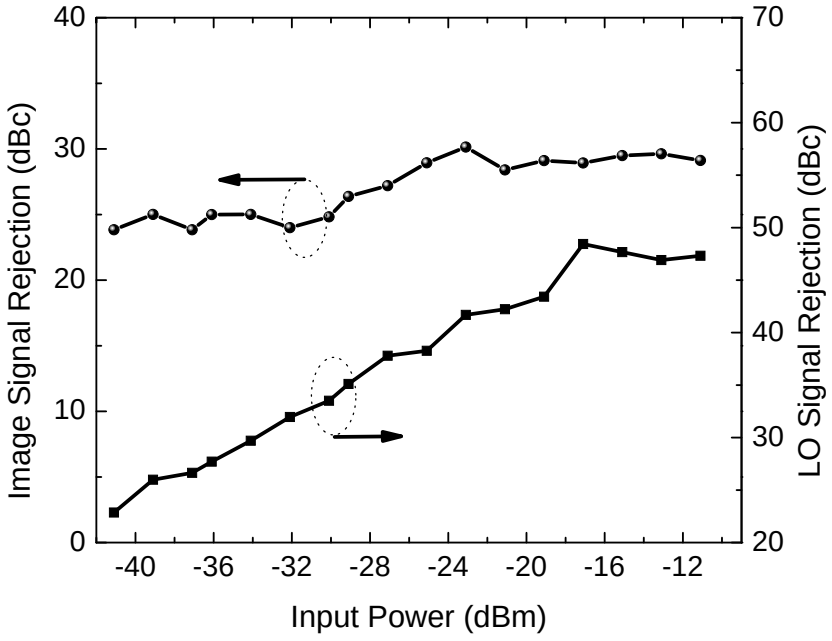
input impedance of the CC stage.

By combining the two topologies into one (see Fig. 5.6(a)), current can be recycled and better reverse isolation can be achieved while still maintaining a low output impedance. The finite base resistance of the input transistor in Fig. 5.6(a) helps to lower the Q factor in the LC tank and its bandwidth is expanded.

A CC stage follows the mixer output to drive a 50Ω off-chip load. For a balanced differential signal and higher gain, current sources in the CC stage are coupled to the opposite phase input signals as shown in Fig. 5.6(b).

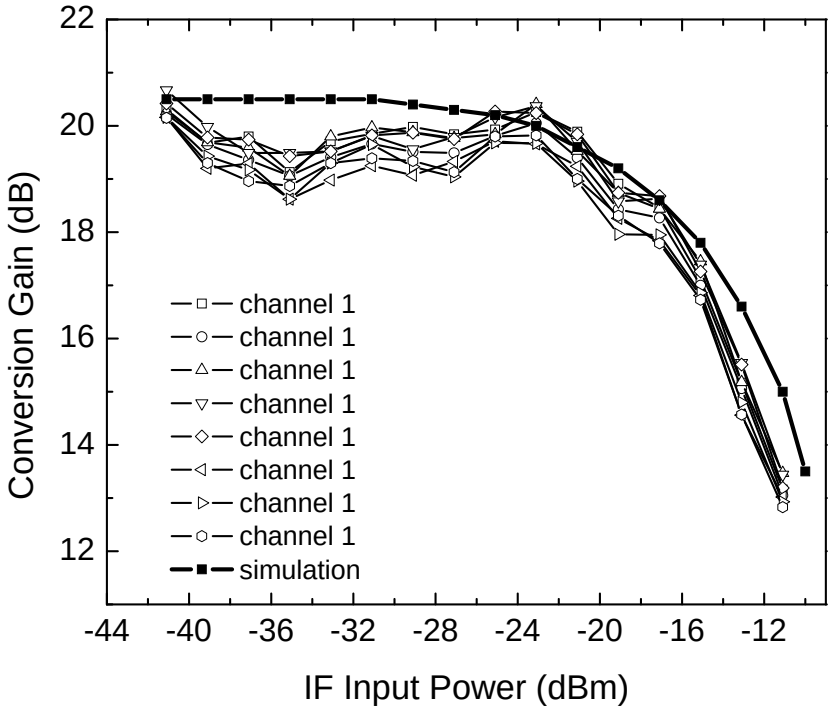


(a)

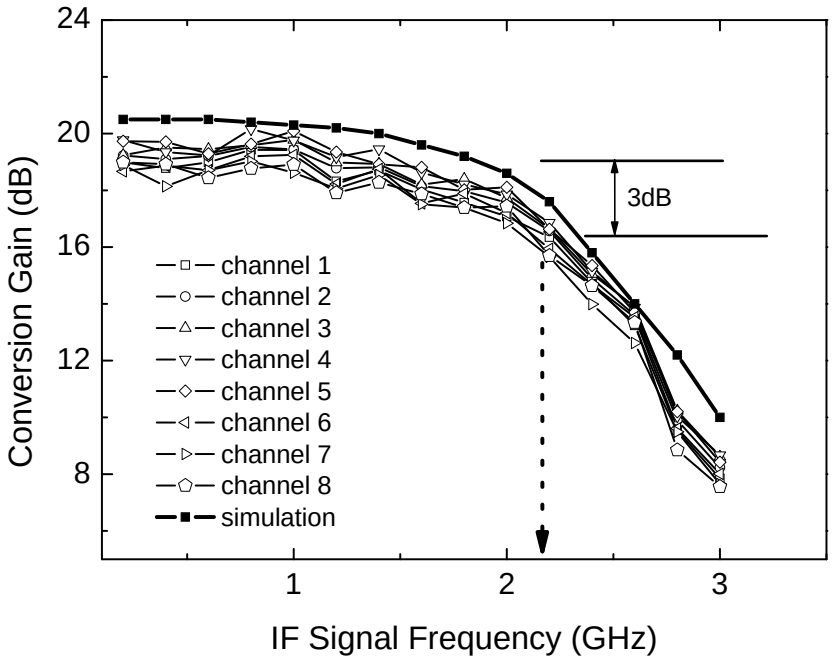


(b)

Figure 5.8: (a) conversion gain and RF output power and (b) image and LO rejection ratio after calibration with I/Q VGA tuning.



(a)



(b)

Figure 5.9: Simulated and measured conversion gain at 45GHz with IF input (a) power sweep and (b) frequency sweep.

5.4 Measured Results

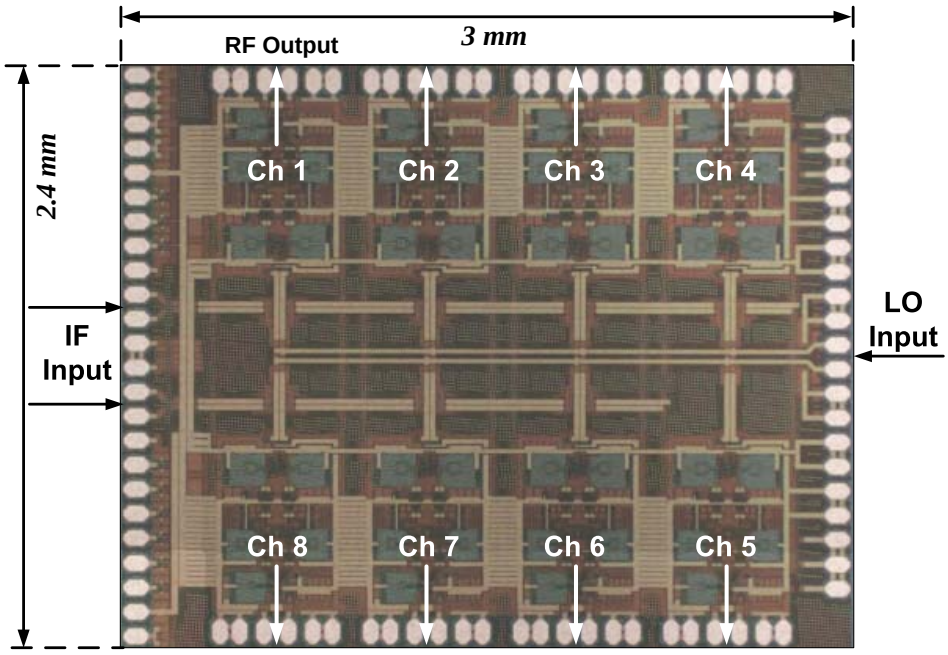


Figure 5.7: Microphotograph of the phased array transmitter.

This phase shifting upconverter was implemented in a 0.18μm BiCMOS process from TowerJazz Semiconductor, which features a peak f_T and f_{MAX} of the SiGe HBT of nearly 150GHz and 200GHz, respectively [71]. The microphotograph of the fabricated die is shown in Fig. 5.7, and the chip size, including the pads is 3$\times$2.4 mm^2. Eight transmitters are integrated on one chip, while all dc control nodes and LO input ports were tied together. The 8-elements consumes 1.0A from the 3.2V power supply voltage for amplification of LO signals and up-conversion mixers, and 150mA from a 2.4V power supply voltage for the injection-locked quadrature oscillators.

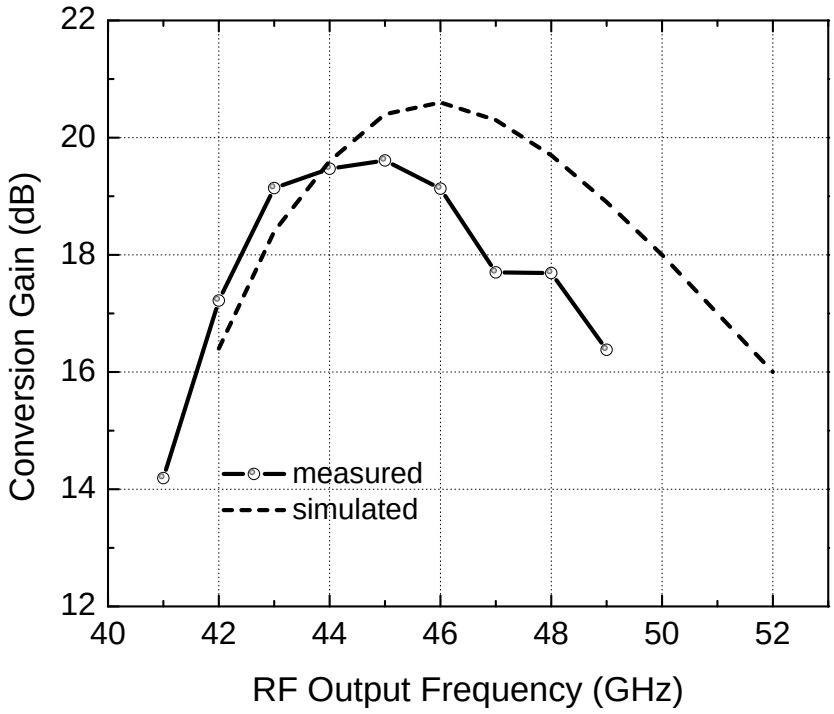


Figure 5.10: Conversion gain change with injection-locked LO frequency sweep (f_{if}=1GHz).

On-wafer measurements were carried out to characterize the performance of the transmitter. After calibration, the conversion gain, output power, image rejection ratio, and LO leakage ratio were as shown in Fig. 5.8(a) and (b).

The conversion gain is approximately 20dB with maximum output power of 2dBm. Both Image rejection and LO leakage ratio are better than 20dBc. The measured conversion gain of each element is shown in Fig. 5.9(a) and (b). The conversion gain variation between transmitter elements is less than 2dB. The 3dB bandwidth of the IF input is 2.2GHz.

The bandwidth of the injection-locked quadrature oscillator and LO path were measured for different LO frequencies. The varactor tuning voltage was also adjusted depending on the LO input frequency. Measured and simulated conversion gain over LO frequency change is shown in Fig. 5.10. The 3dB bandwidth of 7GHz was achieved

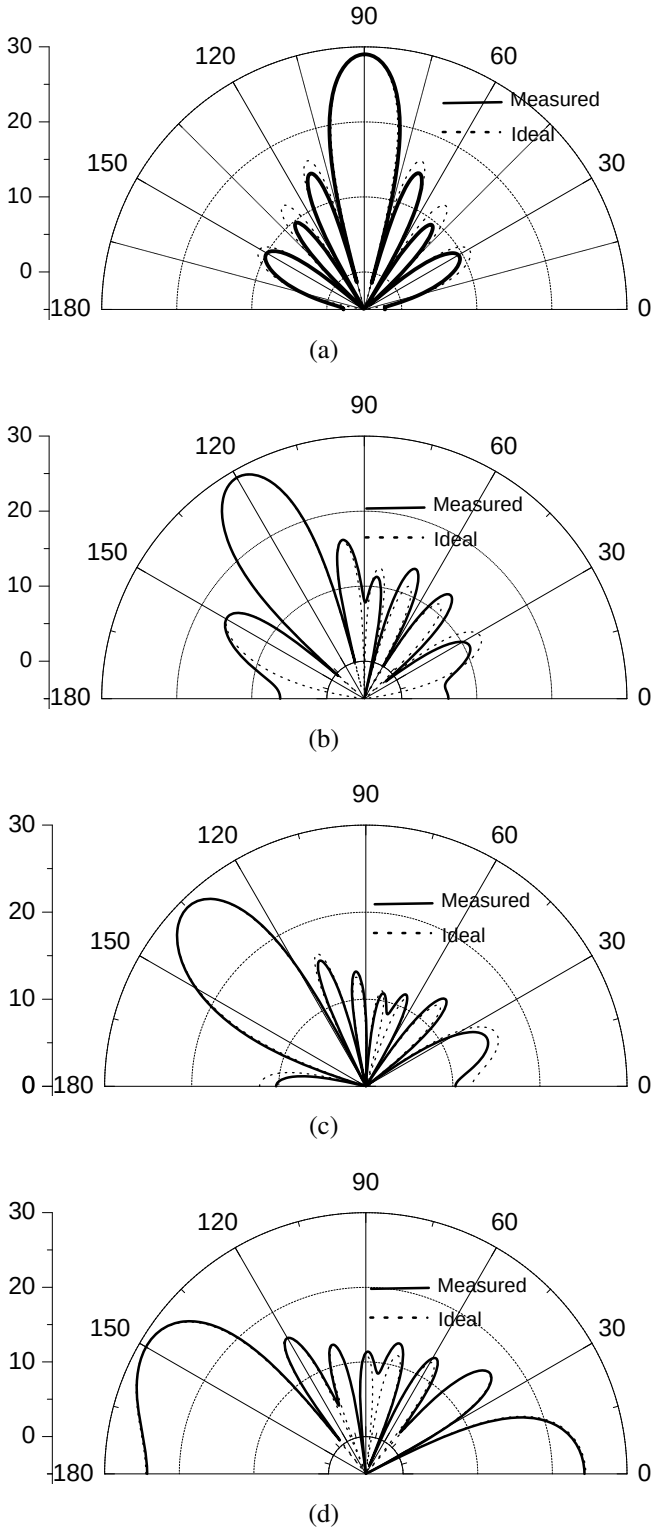
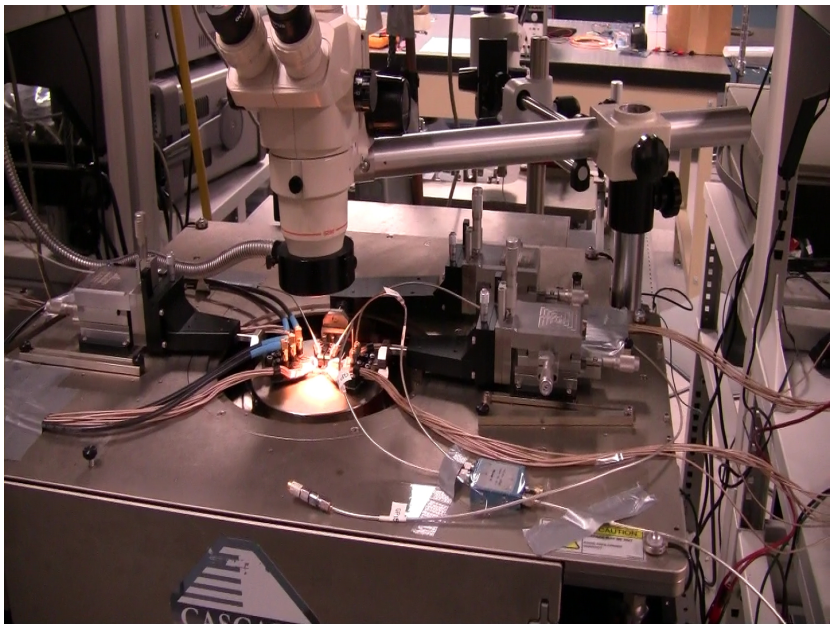
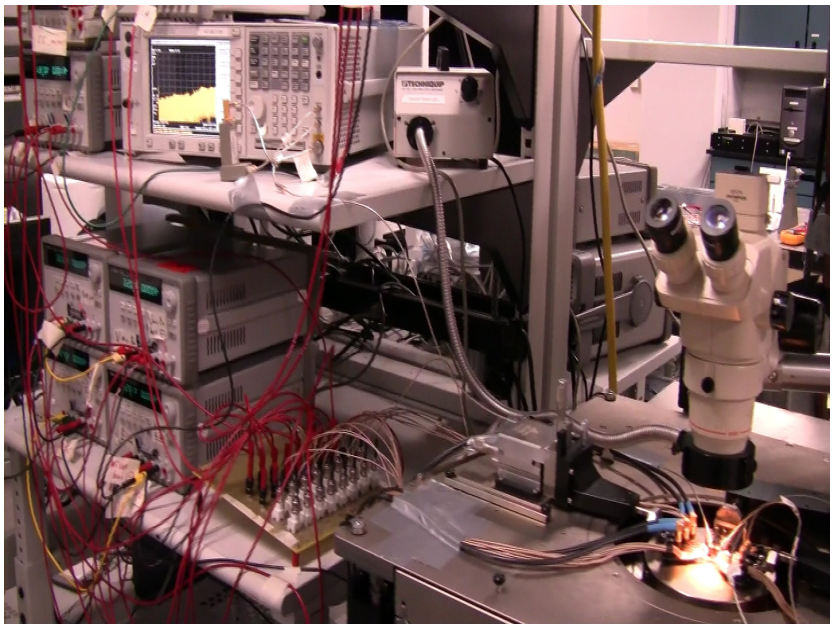


Figure 5.11: Calculated array beam scanning pattern (a) 0° (b) 30° (c) 45° (d) 60° scan angle.



(a)



(b)

Figure 5.12: Measurement setup

with minimum LO input power of -12dBm.

In order to construct phased array patterns, the phase shift of the LO signal at each element was measured. The phased array patterns (array factor) were generated using ADS at 45GHz (carrier freq.=44GHz, IF freq.=1GHz) based on the measured phase shift and LO power under an assumption of a standard linear array with isotropic radiators. The resultant 0° and 45° angle beam were created as shown in Fig. 5.11(a) and (b).

Table 5.1: Performance Summary

Conversion Gain	20 (per ch.)	dB
Max Output Power	2 (per ch.)	dBm
1dB Compression	-16 (per ch.)	dBm
LO Input Power (min)	-12	dBm
Phase Shift	360 (continuous)	degrees
Image Rejection	> 20	dBc
LO leakage	> 20	dBc
LO Input Freq. BW	41 49	GHz
LO, RF port Return loss	< 20	dB
Chip Size (including pads)	3 X 2.4	mm2
Process	0.18um SiGe BiCMOS (ft=150GHz)	
Power Consumption	128mA @ 3.2V per ch.	
	18mA @ 2.4V (OSC) per ch.	

5.5 Conclusion

A 44GHz phase-shifting transmitter based on a direct conversion architecture and LO phase-shifting has been presented in a SiGe HBT technology. This demonstrated an 8-element phased array transmitter for millimeter-wave applications. The transmitter is based on a new architecture, with an injection-locked quadrature oscillator, which enables simpler LO distribution, wider LO frequency bandwidth, and excellent scalability to larger phased array applications. The measured lower sideband and

carrier suppression exceed 20dB after calibration. 7GHz carrier and 2.2GHz IF signal frequency bandwidth are achieved with a conversion gain of 20dB at 45GHz.

This chapter, in part or in full, is a reprint of the material as it appears in the following publication:

- Sunghwan Kim, Prasad Gudem, and Lawrence E. Larson, "A 44-GHz 8-Element Phased Array SiGe HBT Transmitter RFIC with an Injection-locked Quadrature Frequency Multiplier", *IEEE Radio Frequency integrated Circuits (RFIC) Symposium*, 2010.

The dissertation author was the primary researcher and the first author listed in the publication.

Chapter 6

Conclusion

This dissertation focused on finding suitable phase shifters for different applications. For low frequency RF path phase shifters, a new passive variable phase shifter is presented and its linearity is analyzed in detail.

For RF path phase shifters in the transmitter, the linearity, maximum output power, and insertion loss are key performance parameters to avoid degrading a overall system performance. Highly linear, low loss phase shifters were implemented with passive varactor diode and on-chip inductors. Passive varactor diodes are connected in anti-series so that nonlinear current generated by each nonlinear varactor can be cancelled. IMD3 analysis based on Volterra series shows its superb IMD3 performance even when there is marginal mismatches of the size of the two anti-series varactor diode. Its low insertion loss is due to low parasitic loss (high quality factor) of the varactor diode, which Silicon-on-Glass technology provides. This technology provides thick metal connection through the both sides of the wafer so that less parasitic loss is possible. Constant input impedance feature of the phase shifter enable simple cascade of phase shifters to accomplish wider phase shift variations.

In mm-wave applications, it is challenging to make highly linear, low loss phase

shifters in the RF path. In addition, the performance of the phase shifter such as linearity, insertion loss, and noise figure directly affect the data signal. An LO-path active phase shifter is implemented for mm-wave upconverter. The phase-shifting is achieved by the vector summation of the I/Q LO signals in the LO path. A frequency doubler followed by a polyphase filter is used in the first version of upconverter. The frequency doubler multiplies the frequency to the carrier frequency 44GHz. Using half the carrier frequency has some advantages over the full carrier frequency in terms of LO signal loss during distribution and high gain in buffering circuit. Conversion gain of the frequency doubler is analyzed and a closed-form solution is presented. Theory and simulation are compared and they matched well. A two-stage RC polyphase filter followed by a frequency doubler was designed to the generate quadrature signal. Design procedures under chip size constraints and was presented. On-chip single-ended-to-differential and differential-to-single-ended converters, and their gain were implemented and analyzed. Comparison with a conventional converter is also shown. The active area of chip is 940 X 700 μm^2 and the total current consumption is 180mA from 4.4V power supply.

A novel phased array architecture with an injection-locked quadrature oscillator in each channel, to further decrease dc power consumption and loss of LO signal distribution was presented. Eight-elements of upconverters were integrated in one chip with a $0.18\mu m$ SiGe BiCMOS process. Each element had its own localized injection-locked oscillator, which generated four phase signal from a differential signal at the second harmonic frequency. The functions of the frequency doubler and polyphase filter in the previous upconverter implementation are merged into one injection-locked oscillator. The oscillator is based on resistive-loaded four gain stage ring oscillator with capacitive emitter degeneration technique. Its wide locking range and conversion gain for each channel are measured. The measured maximum output power 2 dBm and conversion

gain is 20dB. Each element consumes 450mW out of 3.2V power supply. The chip size including the pads is 3x2.4 mm^2. The calculated array beam scanning pattern shows the successful implementation of low-power phased array transmitter.

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