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A CMOS Fully Integrated 120-Gbps RF-64QAM F-band Transmitter with an On-Chip Antenna for 6G Wireless Communication

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Abstract — **This paper presents a single-chip bits-to-antenna transmitter (TX) for >100 Gbps in 45nm CMOS SOI. The construction of the 64QAM constellation is achieved directly in the RF domain by utilizing three QPSK sub-TXs with weighted amplitude. This method significantly reduces the need to address power amplifier nonlinear effects in high-order modulation, thereby creating room for TX enhancements in both bandwidth and output power. To further improve TX performance, multi-step phase alignment strategies, and a local oscillator leakage suppression technique have been incorporated. With 40-GHz RF bandwidth, the RF-64QAM TX prototype is able to achieve a measured data rate of 120 Gbps with 15 dBm effective isotropic radiated power (EIRP).**

Keywords — **RF-64QAM, transmitter, mm-wave, 6G**

I. INTRODUCTION

Expanding the next-generation wireless communication landscape, 6G ambitiously targets data rates reaching hundreds of gigabits per second (Gbps), promising to revolutionize data transmission technologies [1]. This pursuit has spotlighted a broad and contiguous bandwidth available within the (sub-)terahertz spectra [2]. Concurrently, higher-order modulation techniques boost the data rate through improved spectral efficiency. However, conventional transmitter (TX) architectures encounter formidable challenges when targeting data rates above 100 Gbps. A key impediment resides in the power amplifier (PA) design, experiencing significant efficiency degradation and unwanted AM-PM distortion, especially within the context of higher-order modulation such as 64QAM. Additionally, the nonlinearity prevents the PA from reaching complete saturation, resulting in diminished TX output power—an issue exacerbated at mm-wave, owing to limited f_{max} and G_{max}. Alternative approaches, such as RF-DAC, also confront unmitigated challenges to achieve a high signal-to-noise-and-distortion ratio (SNDR), essential for wideband higher-order modulation at mm-wave.

To counter these challenges, a recent analytical study indicated that the nonlinear backoff problem in the PA can be fundamentally mitigated by embracing both symbol generation/formation and upconversion concurrently in analog/RF domain [3]. This approach, as detailed in Fig. 1(a), constructs a 64QAM signal using three weighted-amplitude QPSK signals, which allows each PA to process a constant-envelope RF signal. This ensures that PAs operate consistently at their saturation power, effectively avoiding AM-PM distortion and nonlinear suppression issues. Consequently, realizing modulation directly in analog/RF simplifies the complex multi-dimensional PA design challenge into a more manageable three-dimensional problem focusing

on bandwidth, saturation power P_{sat}, and stability. This is particularly beneficial at mm-wave frequencies, laying the groundwork for a new methodology for 6G PA design [4]. Moreover, it has been demonstrated that the total error vector magnitude (EVM) of 64QAM realized this way is primarily determined by the QPSK sub-constellation with the largest amplitude. Remarkably, if these three QPSK signals have the same EVM, the overall EVM of a 64QAM TX equals that of a single QPSK [3].

Given the substantial advantages in output power, linearity, and EVM, this work embraces the direct-RF modulation scheme for 64QAM generation, called RF-64QAM, at sub-terahertz frequencies. Notably, it presents the first fully integrated sub-terahertz TX incorporating high-order QAM, spanning from bit generation to antenna, that achieves a wirelessly measured data rate of 120 Gbps. This paper is structured as follows: Section II illustrates the TX system-level structure and elucidates key implemented circuit blocks. Section III presents the continuous wave and modulation measurement results. Finally, Section IV provides concluding remarks, summarizing the contributions and implications of this research.

II. SYSTEM ARCHITECTURE AND CIRCUIT BLOCKS

A. System Architecture, Phase Alignment, and LO Leakage Suppression

The proposed RF-64QAM TX architecture is detailed in Fig. 1(a), incorporating six on-chip pseudorandom binary sequence (PRBS) generators with a pattern of $2^9 - 1$ for testing purposes, each driven by a clock running up to 20 GHz. Each PRBS is fed to a switched-RC network, which provides elementary pulse shaping. The on-chip TX local oscillator (LO) chain begins by doubling a 30 GHz off-chip single-tone signal to 60 GHz. This signal is then distributed to three sub-TXs and a phase calibration block using Wilkinson power splitters. Each sub-TX features a doubler-to-buffer chain to produce a 120 GHz LO. A transmission-line-based IQ hybrid coupler within each sub-TX path creates the local IQ signal, which, after being boosted by 120 GHz buffers, is used in the QPSK modulator for baseband-to-RF upconversion. To simplify the design process, the same PA topology is adopted in all sub-TXs, but configured with different DC bias conditions. As a result, the three PAs achieve different output saturation power levels with 6 dB difference in P_{sat}. A 3-way transmission-line-based recombinant power combiner finally forms the 64QAM signal and feeds it to an on-chip backside radiation antenna. An embedded coupler sends part of the signal back to an on-chip mixer for phase calibration.
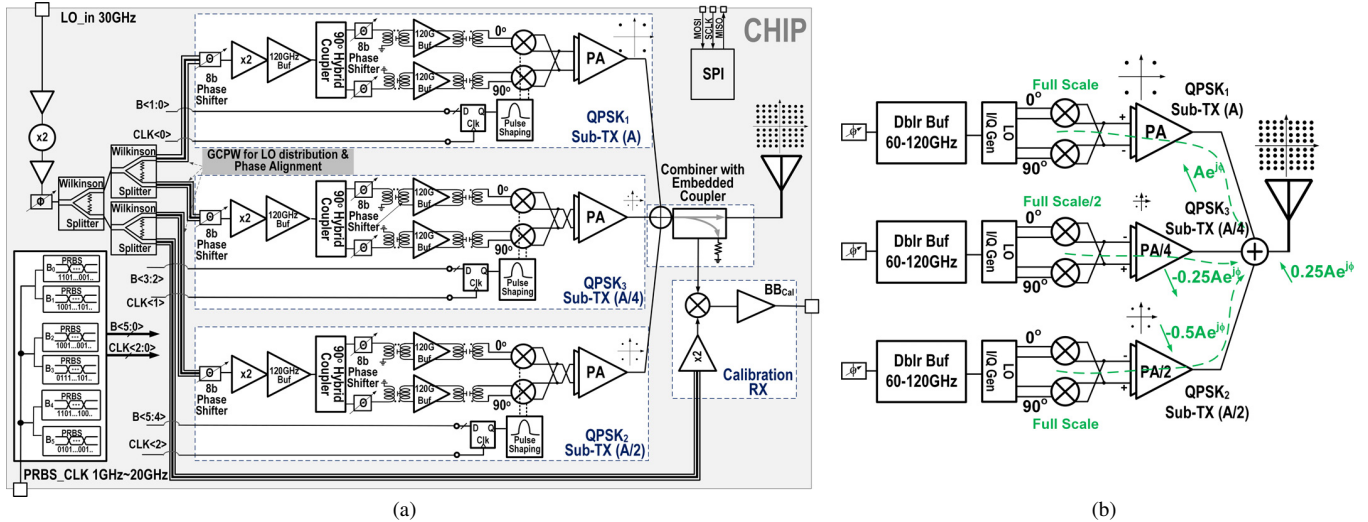
Fig. 1. (a) System Architecture of the proposed RF-64QAM TX.(b) Proposed LO leakage suppression technique in RF-64QAM TX.

Phase accuracy is crucial for 64QAM signal construction. This issue is addressed by performing a three-step phase alignment. The first step involves aligning the phase offsets of all three carrier signals and synchronizing the phases of all baseband signals in the three constituent QPSK sub-TX paths during the design phase. Owing to varied bias conditions in the three PAs, each sub-TX exhibits a unique phase response. The unwanted phase differences are calibrated by careful length adjustment of grounded coplanar waveguides (GCPWs) carrying the 60 GHz LO from the output terminals of Wilkinson power splitter to the input of each sub-TX chain. The on-chip interconnects carrying the high-speed baseband signals from PRBS generators are also EM-simulated to ensure phase alignments at the three modulator inputs. In the second step, an on-chip calibration receiver (RX) (Fig. 1(a)) at the TX output is implemented to compensate for process-voltage-temperature (PVT) variations. During this phase, the 60 GHz LO signal, doubled after Wilkinson splitting, feeds a mixer to downconvert the signal coupled from the front-end combiner's output. Each sub-TX is then activated in turn, and the DC output (BB_{Cal}) of the calibration RX is measured. By adjusting the 8-bit-tunable $\pm10°$ range 60-GHz phase shifters at each sub-TX input, the BB_{Cal} for each sub-TX is calibrated to a 0-V DC voltage. This step achieves phase alignment across all sub-TXs.

The third phase-alignment step addresses the IQ phase mismatch, which is resolved by utilizing a pair of 8-bit $10°$ range phase shifters operating at 120 GHz, positioned after the 90-degree hybrid coupler in each sub-TX (Fig. 1(a)). A one-time calibration for each sub-constellation is conducted, effectively mitigating process-induced variations and mismatches during the formation of the 64QAM signal.

In addition to the previously mentioned attributes, the RF-64QAM scheme also inherently lends itself to LO leakage suppression, resulting in an overall improvement in the TX dynamic range and linearity. This is readily achieved by swapping the input connections to each of the two PAs in the lower-amplitude sub-TXs (Fig. 1(b)). Assuming identical mismatches and parasitic couplings in the three sub-TXs, configuring the TX as shown in Fig. 1(b) results in a 75% reduction in LO leakage amplitude corresponding to 12 dB

reduction of LO leakage power.

B. Block Level Design Consideration

1) On-chip Wideband Antenna

Transmitting a wideband sub-terahertz modulated signal wirelessly from a chip, while ensuring signal integrity, presents significant challenges. Wirebonding of an above-100-GHz wideband output port is impractical due to losses from bonding wires and packaging, affecting signal quality. A flip-chip approach, though feasible, incurs challenges associated with high-frequency signal feeds through copper pillars or C4 balls and interposers to an off-chip antenna. Considering these factors, this study adopts an on-chip antenna approach. Nonetheless, an on-chip antenna with an on-chip ground shield is not conducive to wideband applications due to the large interlayer capacitances arising from the dense metal stackup in CMOS technology. Without the ground shield, the antenna naturally radiates about 97% of its power into the silicon substrate, owing to the significant dielectric-constant disparity between air and silicon [5]. Therefore, a back-side radiation method using a silicon lens is pursued. Specifically, a square spiral antenna [6], [7] with a CPW feeding line for input matching is engineered that spirals down from M7 to M6, as shown in Fig. 2(b). To increase gain and maintain electrical field continuity at the ground strips of the single-end CPW feed, the signal is bifurcated into two symmetrical sub-spirals for effective spatial power combining. The antenna is modeled in HFSS with its diced wafer substrate and silicon lens. The simulated radiation pattern and a microphotograph of the fabricated antenna are presented in Fig. 2(a)-(b). Additionally, the HFSS-simulated performance of the standalone antenna is shown in Fig. 2(c). The antenna achieves a gain of around 15 dBi and maintains an efficiency of 70% across the 100-to-140-GHz range, along with a strong matching indicated by $S_{11} < -10$ dB.

2) Wideband PA Design

As outlined in Section I, by placing the PA before the power combiner in the proposed RF-64QAM TX, the focus of the PA design lies exclusively on bandwidth and P_{sat}, assuming stability. This strategic placement significantly

(a)   (b)   (c)
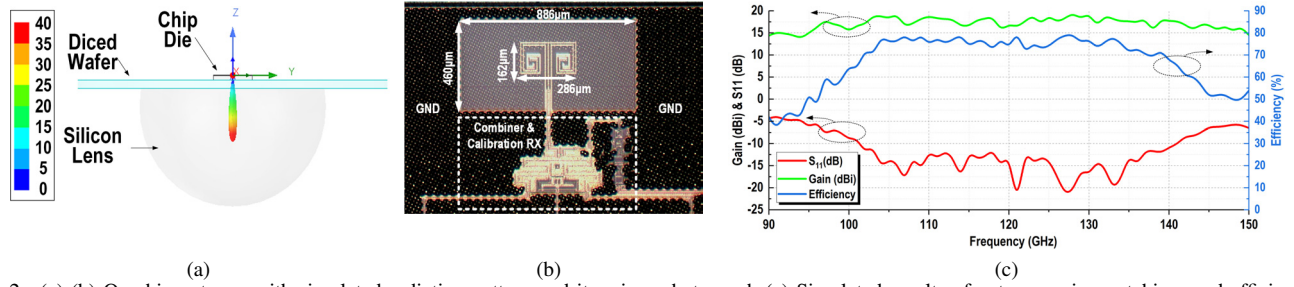
Fig. 2. (a) (b) On-chip antenna with simulated radiation pattern and its micro-photograph (c) Simulated results of antenna gain, matching, and efficiency.
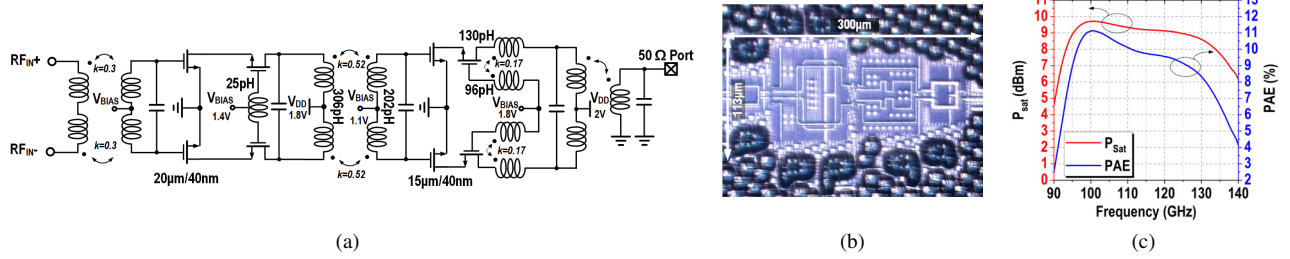

(a)   (b)   (c)

Fig. 3. (a) Schematic of wideband PA. (b) Micro-photograph of the fabricated PA. (c) Simulated P_{sat}, PAE.

reduces the need to combat nonlinear effects, making it possible to arrive at PA designs with wider bandwidth and higher output power. The 2-stage PA schematic with interstage transformer matching is shown in Fig. 3(a). The PA's output stage incorporates a pair of mutually coupled inductor pair with a coupling factor of ~0.2, one at the gate and the other at the drain of the cascode device. This arrangement improves both the gain and the gain flatness across the bandwidth of interest. Additionally, this inductive coupling reduces the V_{GD} dynamically during the PA operation and enables the transistor to operate under a higher V_{DD}, thus increasing P_{sat} without risking PA breakdown. The entire PA occupies an area of $300 \times 113 \mu m^2$ (Fig. 3(b)), and achieves a P_{sat} higher than 9 dBm with a 3-dB bandwidth exceeding 40 GHz, as depicted in Fig. 3(c).

III. MEASUREMENT RESULTS

Shown in Fig. 4(a) is the die photo of the TX prototype fabricated in a 45-nm CMOS SOI technology, occupying an area of $4.5 \times 2.8mm^2$. A continuous wave test was conducted for the chip mounted on a 3D rotatable holder at a distance of 10 cm to evaluate the TX radiation pattern at the carrier frequency of 120 GHz, as shown in Fig. 4(b). The measured effective isotropic radiated power (EIRP), after de-embedding the path loss and antenna gain, is approximately 15 dBm.

Hartley tests were performed on the TX by transmitting IQ single-tone signals from an arbitrary waveform generator (AWG) and bypassing the on-chip PRBS blocks. The measured results for the image rejection ratio (IRR) and LO leakage are presented in Fig. 4(c). An exemplary down-converted spectrum[1] is shown on the left of Fig. 4(c), from which we can see the proposed LO leakage cancellation method improved the overall LO feedthrough by $7 \sim 10$ dB in the RF-64QAM scheme compared to a single QPSK sub-TX. Furthermore, the measured IRR for this prototype is > 32 dB.

Following the approach in [8], we measured the TX bandwidth by turning on only one sub-TX and sending a 1 GHz PRBS signal. The measured QPSK spectrum in Fig. 5(a) showed a 3 dB attenuation at 20 GHz compared to the ideal Sinc function, indicating a 40 GHz RF bandwidth.

Fig. 5(b) displays the measured spectrum at 30-cm TX-RX distance for the downconverted 64QAM signals at 8 GBd and 20 GBd. A closer look at the spectrum reveals that the beating frequency pattern aligns with the designed $2^9 - 1$ PRBS pattern. Additionally, a 3 cm wireless link measurement was performed by downconverting the signal through an F-band balanced mixer[2], followed by demodulation using a 70 GHz real-time oscilloscope. The measured eyediagrams, utilizing the oscilloscope's built-in continuous-time linear equalizers (CTLE) and decision feedback equalizers (DFE), are depicted in Fig. 5(c). The distinct eye-openings at 48 Gbps and 120 Gbps affirm the performance of the proposed RF-64QAM TX. Furthermore, the equalized 64QAM constellation diagram at 120 Gbps exhibited an $\mathrm{EVM_{rms}}$ of -18.6 dB. A comprehensive performance summary of the RF-64QAM prototype, alongside a comparison with state-of-the-art, is presented in Table 1. This prototype represents a complete fully integrated bits-to-antenna transmitter capable of >100 Gbps transmission for 64QAM, paving the way for next-generation wireless communication.

IV. CONCLUSION

A comprehensive CMOS single-chip solution for >100 Gbps 64QAM tailored for 6G applications was presented. The F-band RF-64QAM TX prototype was fabricated in 45 nm CMOS SOI. The demonstrated performance showcased 120 Gbps wirelessly measured data rate with an $\mathrm{EVM_{rms}}$ of -18.6 dB. The measured EIRP was reported to be approximately 15 dBm, coupled with a power efficiency of 7.3 pJ/b. Additionally, this TX successfully achieved an LO

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[1]A signal at 1+120=121 GHz was down-converted by a $9.8 \times 12 = 117.6$ GHz signal from the VDI signal generator frequency extender.

[2]Short distance results from absence of LNA in the off-the-shelf RX, constrained by integrated noise level for distinct eye-opening at 40GHz RF bandwidth.
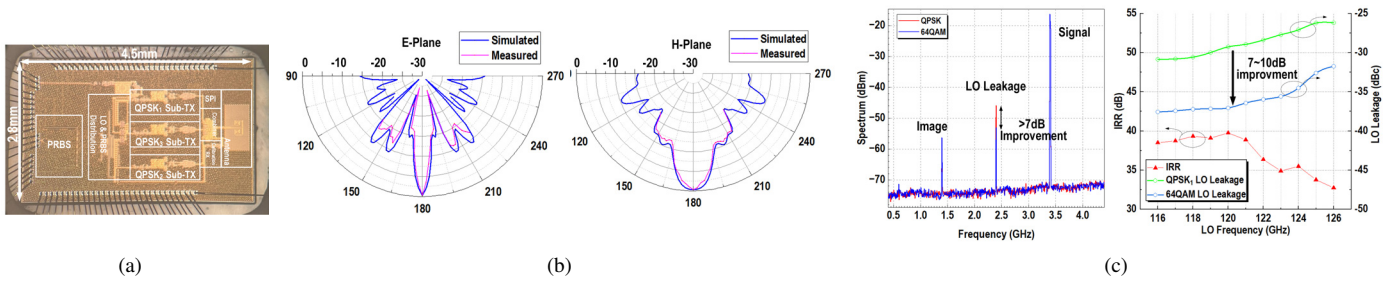
Fig. 4. (a) Micro-photograph of the RF-64QAM TX, and the measured (b) normalized radiation pattern at carrier frequency, (c) LO leakage nd IRR results.
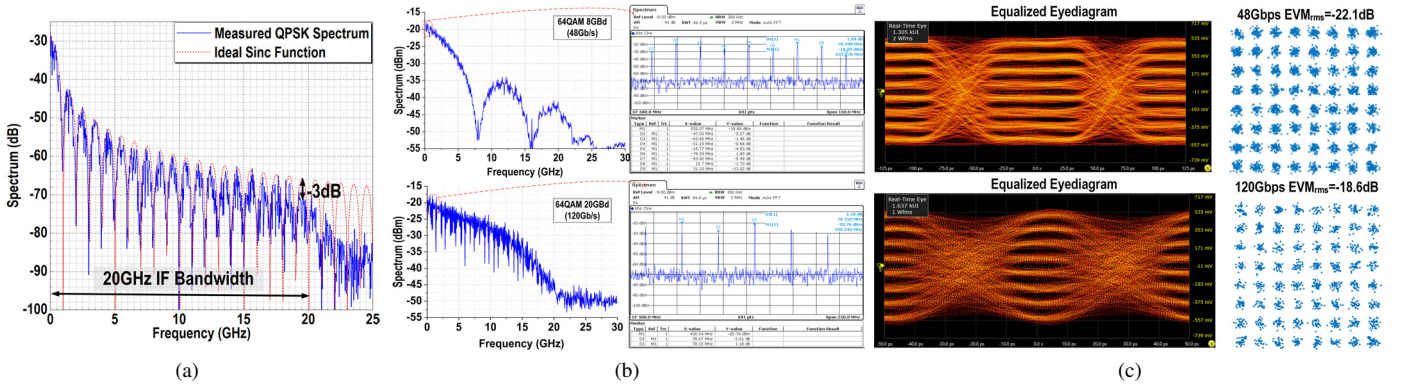

Fig. 5. Measured results for modulated signals:(a) Downconverted zero-IF spectrum of 1 GBd QPSK signal. (b) Downconverted 64QAM spectrum for 8 GBd and 20 GBd.(c) Eyediagrams and constellations of 64QAM signal with EVM_{rms} for 8 GBd and 20 GBd.

Table 1. Performance comparison of the prototype with state-of-the-art.

	This Work	[9]	[8]	[10]
Tech.	**45nm SOI**	28nm CMOS	22nm FinFET	45nm SOI
Arch.	**Direct RF**	Direct RF	I/Q RF-DAC	BB I/Q DAC
D/A I/F	**Integrated 1-bit**	Integrated 1-bit	Integrated 2-bit ★	External AWG
Mod.	**64QAM**	16QAM	16QAM	64QAM
Freq.	**120 GHz**	135 GHz	140 GHz	149 GHz
Antenna	**On-chip + Silicon Lens**	Off-chip	No antenna	Off-chip
EIRP	**15 dBm**	8 dBm	-	8.3 dBm
P_{out}	**2 dBm**	0 dBm	0.8 dBm	0.1 dBm
DR	**120 Gbps**	32 Gbps	160 Gbps†	84.48 Gbps
P_{DC}	**875 mW**	287 mW	173 mW	420 mW
Eff.	**7.3 pJ/b**	9 pJ/b	1.1 pJ/b	4.97 pJ/b

★ Insufficient SQNR for practically attainable EVM and INL/DNL [3].
†No wireless meaurement.

leakage cancellation of over 7 dB, further enhancing the overall performance of the proposed system.

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