UNIVERSITY OF CALIFORNIA SAN DIEGO

Advances in SiGe, CMOS RFSOI and Phase-Change Circuits for High Performance Phased-Arrays

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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Professor Gabriel M. Rebeiz, Chair
Professor Gert Cauwenberghs
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Professor Brian Keating
Professor Daniel Sievenpiper

2022

The dissertation of Dimitrios Baltimas is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2022

DEDICATION

To my beloved family and friends

EPIGRAPH

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Wisdom begins in wonder.

-Socrates

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Chapter 2, in part, is a reprint of the material as it appears in: D. Baltimas and G. M. Rebeiz, "A 25–50 GHz Phase Change Material (PCM) 5-Bit True Time Delay Phase Shifter in a Production SiGe BiCMOS Process," 2021 IEEE MTT-S International Microwave Symposium (IMS), 2021, pp. 435-437, doi: 10.1109/IMS19712.2021.9574891. The dissertation author was the primary investigator and author of this paper.

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Chapter 3, in full, is being prepared to be submitted for publication of the material as it may appear in: D. Baltimas, Hyunchul Chung and G. M. Rebeiz, "K-Band SiGe BiCMOS High Linearity T/R Beamformer Channel with $>$ 0 dBm IIP3 and $<$ 7.2 dB NF", in *IEEE Microwave and Wireless Component Letters*. The dissertation author was the primary investigator and author of this paper.

Chapter 4, in full, is being prepared to be submitted for publication of the material as it may appear in: D. Baltimas, Siwei Li and G. M. Rebeiz, "A 132-142 GHz RF Beamforming Phased Array Receiver Channel with 7 dB NF in 45nm RFSOI", in *IEEE Microwave and Wireless Component Letters*. The dissertation author was the primary investigator and author of this paper.

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ABSTRACT OF THE DISSERTATION

Advances in SiGe, CMOS RFSOI and Phase-Change Circuits for High Performance Phased-Arrays

by

Dimitrios Baltimas

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2022

Professor Gabriel M. Rebeiz, Chair

Although electronically steered arrays are a century old concept, the research and development interest was primarily driven by the defense industry and radio astronomy without any room for potential commercial applications due to the insurmountable cost. The insufficient beamformer chip performance made the implementation of large phased arrays with high effective isotropic radiated power (EIRP) and increased sensitivity prohibitive. Only with the recent advancements in silicon technologies was the cost barrier reduced to an extent that large phased array systems can be employed in a multitude of commercial applications. Particularly, developments in silicon beamformer chips have enabled the commercialization of phased arrays for 5G wireless

communications, satellite communications (SATCOM) and $>$ 100 GHz communication links.

This dissertation focuses on the implementation of high performance beamformer chips in different technologies for low-cost and high performance phased array systems. It presents several implementations of ultra wideband switches along with a true-time delay unit from DC-67 GHz using a novel phase change material (PCM) switch that is utilized for the achievement of large instantaneous bandwidths. The presented TTD unit achieves a record 124 ps relative true time delay reported on an IC from DC-67 GHz.

This dissertation also presents a K-Band 19-22 GHz Tx/Rx beamformer channel with a state of the art linearity and sensitivity performance. The chip can achieve a very competitive OP_{1dB}/IIP3 (8 dBm / 0 dBm) while its NF is 7 dB leading to state-of-the-art sensitivity performance in K-Band.

Finally, this dissertation presents a D-band full RF beamforming Rx channel at D-band. The full RF implementation of the phase shifter and the VGA is introduced at 140 GHz with a NF performance that substantiates this architecture as a potential candidate for D-band phased arrays along with its competitive phase, amplitude control and power dissipation.

All presented beamformer chips, illustrate significant advancements in various performance aspects and can be utilized for the implementation of high performance phased arrays.

Chapter 1

Introduction

In the past decade, the ever-increasing demand for high data rates (Figure 1.1), data capacity and low latency has driven the wireless industry's efforts in research and development for the fifth generation (5G) wireless communication networks [1]. Various bands of interest across the mm-wave spectrum, such as 28 GHz, 39 GHz, and 60 GHz have been assigned and licensed for the 5G networks.

In addition, the global pandemic has pushed a bigger part of the daily life engagements to the virtual domain leading to an even higher demand of fast, broadband internet connectivity with low latency. Especially, under-served rural areas with low population density require an immediate answer to the lack of infrastructure problem [2]. New business models with Low-Earth-Orbit satellite constellations, have attracted funding, in order to provide feasible solutions for internet in the absence of fixed cable infrastructure. Hence, the significant interest in the design of Ku and K-band SATCOM terminals using high performance beamformer chips for the design of phased-array systems.

Endeavors for further increasing the data-rate capability of short-range links have lead to the exploration of D-band as potential candidate for next generation networks (beyond 5G / 6G) [3]. In that regard, the design of functional beamformer channels that can be utilized for

the design of large phased-arrays with sufficient effective isotropic radiated power (EIRP) and antenna gain at D-band becomes critical.

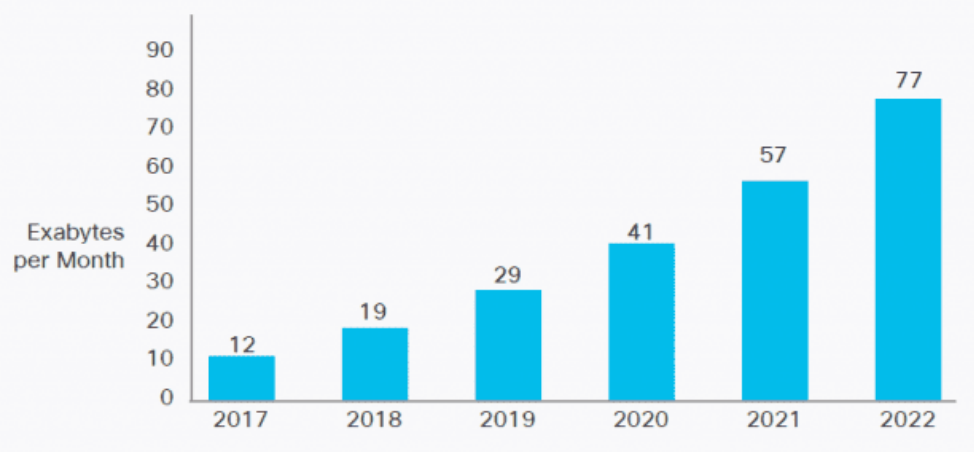

Figure 1.1: Cisco wireless data consumption forecast [4]

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1.1 True-Time Delay Units

One popular technique to increase the data rate without increasing the modulation complexity is to increase the instantaneous bandwidth of operation, or the effective channel bandwidth associated with each sub-carrier. However, there is an upper limit in the effectiveness of this technique due to the system level limitations imposed by the so-called beam squint effect.

In order to explore the challenges introduced by the beam squint effect we need to analyze how the beamformer channels introduce the progressive phase shift between each element of a phased-array.

For this purpose we present the array factor expression when each element is excited using a progressive phase shift that is constant within the selected instantaneous bandwidth.

$$AF = \sum_{n=1}^{N} I_n e^{-jk_{f_o}(x_n sin\theta_s cos\phi_s + y_n sin\theta_s sin\phi_s + z_n cos\theta_s)} e^{jk_{f_o \pm \Delta f}(x_n sin\theta_s cos\phi_s + y_n sin\theta_s sin\phi_s + z_n cos\theta_s)}$$

Where AF is the array factor, N is the number of elements of the linear array (N^2 for the 2-D array), f_o is the center frequency at which the phase shifter setting is calculated, $2\Delta f$ is the instantaneous bandwidth, x_n, y_n and z_n the loci of the elements on the 2-D array and ϕ_s, θ_s the selected scan angle.

The key observation is that the phase shifter is set at frequency f_o but the same phase shifter setting is used throughout the instantanous bandwidth. This leads to a deviation in the selected scan angle since the wavenumber changes linearly versus frequency but the progressive phase shift remains constant.

$$k = \frac{2\pi}{c} f$$

We can write, for a linear array on the y-axis with N elements, that its array factor is:

$$AF = \sum_{n=1}^{N} I_n = A_n e^{jn(kdcos\theta_s + a)} = \sum_{n=1}^{N} I_n = A_n e^{jn\Psi}$$

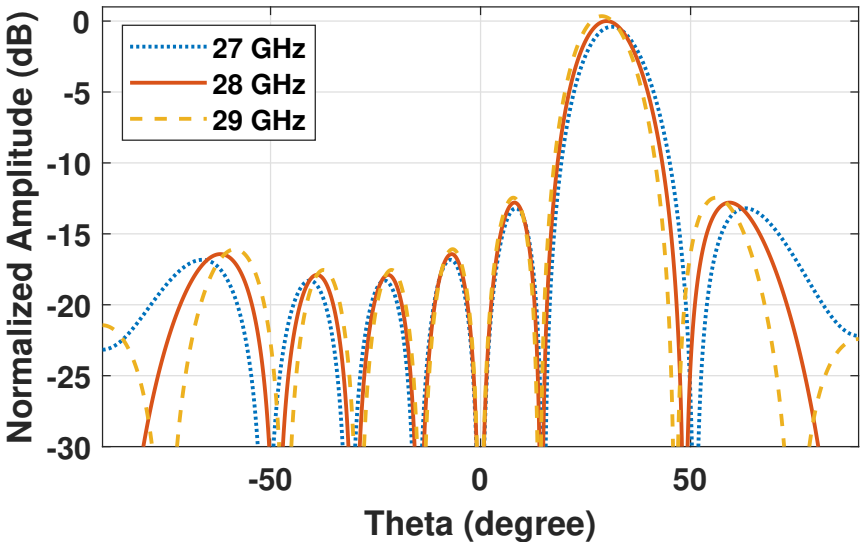
The array factor get its maximum value when $\Psi = 0$, which entails that for a scanning array at angle θ_s we need to impose a progressive phase shift equal to:

$$a = -kdcos\theta_s \Longrightarrow a = -\frac{2\pi d}{c} cos\theta_s f_o \Longrightarrow \frac{\partial a}{\partial \omega} = -\frac{d}{c} cos\theta_s$$

This indicates that in order to retain the desired scan versus frequency we need to apply a phase shift that is linearly proportional to frequency.

The angular resolution variation can be quantified as:

$$\Delta\theta_s = \arcsin\left(\frac{f_o \pm \Delta f}{f_o} sin\theta_s\right) - \theta_s$$



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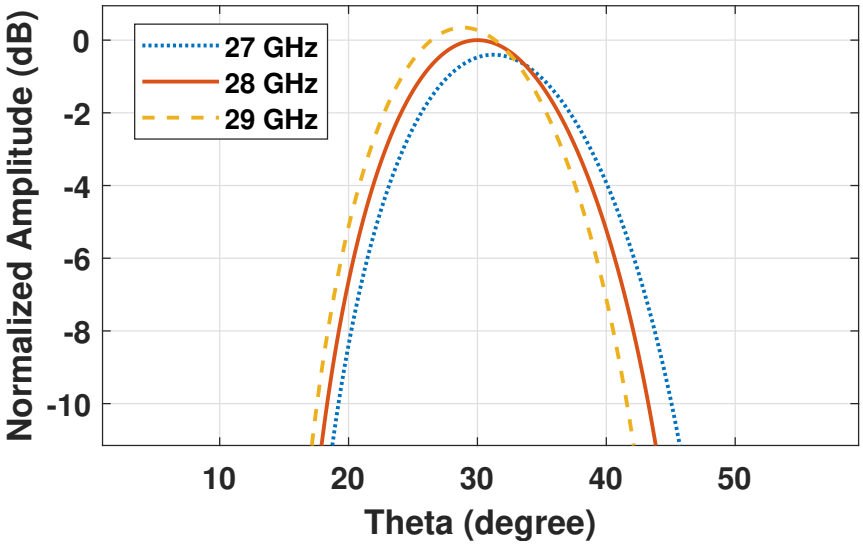


(b)

Figure 1.2: Beam Squint effect on a 2-D array scanned at 30 °

The previous derivations illustrate the system level constrains imposed by beamformer architectures that introduce constant phase shift versus frequency. For a certain instantaneous bandwidth, a constant phase shift beamformer will lead to a phased array with frequency dependent angular resolution or in other words the phased-array gain will become a function of frequency. If the gain imbalance becomes higher than 0.5 dB within the instantaneous bandwidth, the system level functionality is compromised. Also, the phenomenon becomes more intense as the scan angle increases.

To illustrate the problem we simulate the array factor of a 2-D 8x8 phased array using a 2 GHz instantaneous bandwidth from 27 to 29 GHz (Figure 1.2a-Figure 1.2b). The simulation results confirm the expected gain variation.

Our target, within this work is to utilize advancements in phase change material (PCM) technology and integration that will allow for the design of competitive TTD units in order to minimze the beam squint problem, as it will be presented in Section 2.

1.2 Sensitivity and Dynamic Range

In non-linear systems, the dynamic range is quantified as the ratio between the largest and smallest signal power that the system can properly demodulate (in the case of a receiver). Te smallest power level is determined by the system's sensitivity and the largest by the system's non-linear behavior.

For the first part we can write that the system's sensitivity is given by:

$$Sensitivity = -174\frac{dBm}{Hz} + 10log(BW) + NF + SNR_{min}$$

For the second part we can further determine the maximum power level based on different approaches. In the first the maximum tolerable power is based on a single tone test approach

which makes:

$$P_{max} = IP_{1dB}$$

This leads to a definition of the system's dynamic range as:

$$DR(dB) = IP_{1dB} + 174\frac{dBm}{Hz} - 10log(BW) - NF - SNR_{min}$$

The definition becomes stricter using a 2-tone test to determine the maximum tolerable power as the input power level for which the 3_{rd} order intermodulation products become equal to the integrated noise level. This leads to a definition of the system's dynamic range (usually referred to as spurious free dynamic range) as:

$$SFDR(dB) = \frac{2(IIP3 + +174\frac{dBm}{Hz} - 10log(BW) - NF)}{3} - SNR_{min}$$

The previous derivation indicates that from a dynamic range perspective the noise figure contribution is equal to the linearity performance achieved.

High dynamic range beamformers are extremely important in applications that the received signal is accompanied by large interferers.

As an instance, RX desensitization is a critical problem in FDD systems where signal transmission and reception happens simultaneously. In this case, the received signal will be accompanied by strong interferers from the leaked TX signal (Figure 1.3).

We can express the small signal gain experienced by the signal in the RX band, under the presence of a large interferer at the TX band as:

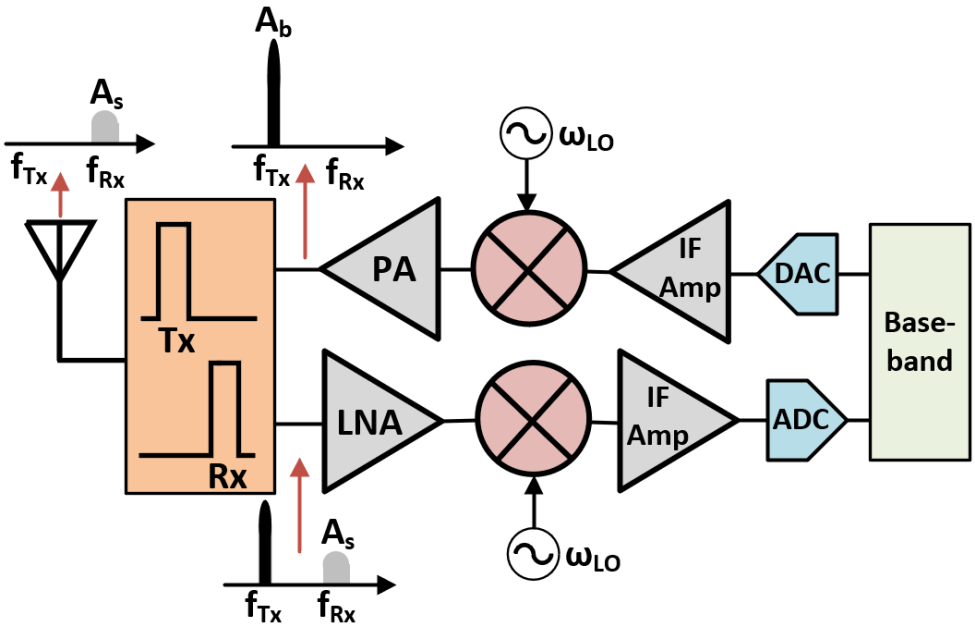


Figure 1.3: Receiver desensitization in FDD architectures.

$$y = (a_1 A_s + \frac{3}{2} a_3 A_b^2) A_s cos\omega_{R_x} t + \ldots$$

If the receiver experiences compressive behavior ($a_1 a_3 < 0$) then the receiver small signal gain will deteriorate as the interferer increases or as the system's non-linear behavior (quantified by its IIP3) becomes worse.

From a system level perspective, in order to improve the overall dynamic range our target is to improve both the NF performance and along with increasing its linearity. The receiver linearity can also help alleviate system level considerations like the duplexer attenuation at the TX band.

Our target, within this work is to demonstrate circuit level and system level techniques that can lead to the implementation of a state-of the-art k-band Rx/Tx common leg beamformer channel, as it will be presented in Section 3.

1.3 D-Band Beamformers

Besides 5G allocated bands up to 60 GHz, frequency bands at 77 GHz and 94 GHz have been utilized for autonomous radar and short-range imaging systems. In an effort to investigate the potential to establish ultra high data rate communication links the Federal Communications Commission (FCC) moved to open spectrum above 95 GHz for new technologies, that can potentially lead to 5G+ or 6G wireless networks.

(a) (b)

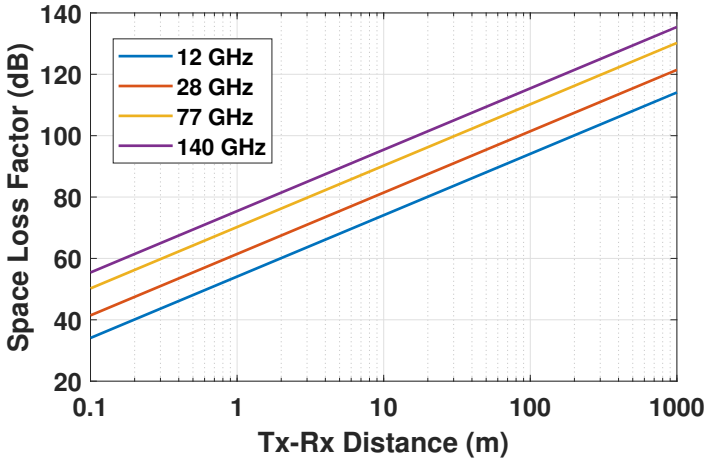
Figure 1.4: Industrial IoT and imaging applications at D-band [5]- [6].

Communication systems at $>$ 100 GHz can utilize the large unlicenced and unallocated spectrum resources for ultra-high data-rate links. Many applications specifications for increased data rates and reduced latency force for innovation at D-band. For example, industrial IoT [5] (Figure 1.4a), in the form of machine to machine real time interaction and virtual/augmented reality and imaging applications (Figure 1.4b) [6].

In order to design functional systems at D-band the free space loss considerations need to be properly accounted for (Figure 1.5a). In particular, the 130-150 GHz frequency range, which is a sub-band within D-band, presents potential for longer-range wireless links due to reduced atmospheric absorbtion an this range, as it lies in-between oxygen and water molecules absorption

points.(Figure 1.5b)

Finally, commericially available, advanced silicon nodes such as SiGe BiCMOS and CMOS SOI typically exhibit $>$ 300 GHz f_T and f_{max} leading to enough intrinsic gain and sufficient performance at the 140 GHz range.



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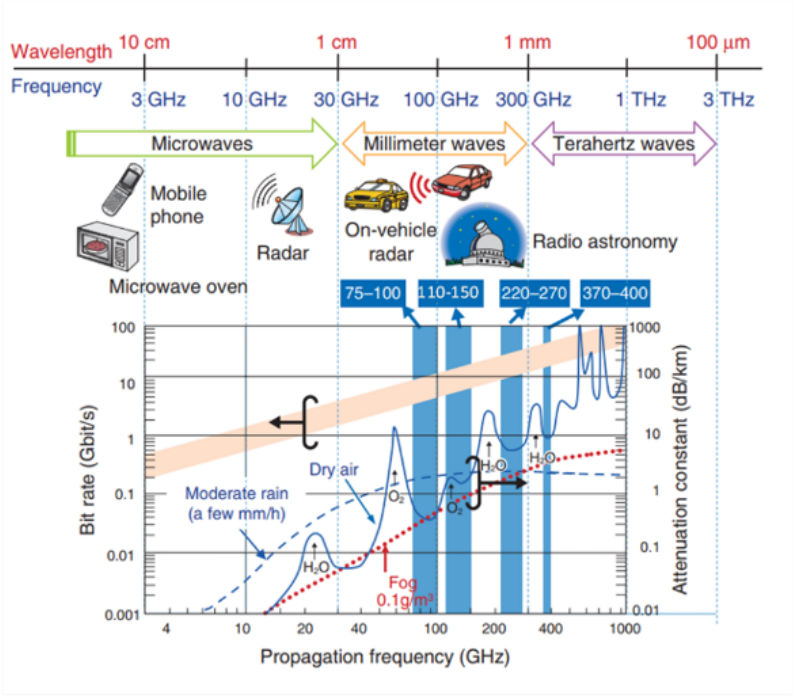


(b)

Figure 1.5: Free space loss and atmospheric absorption.

1.4 Thesis Overview

This thesis encapsulates circuit and system level advancements in the implementation of high performance beamformers for the design of phased arrays from 2-140 GHz. Phase change material switches, along with SiGe BiCMOS and CMOS SOI technologies are utilized for the design of an ultra wideband true-time delay unit, an ultra high-linearity and dynamic range K-band beamformer channel and a D-band Rx beamformer channel with full beamforming integration at 140 GHz. All designs illustrate advancements in critical aspects of beamformer design at different frequency ranges.

Chapter 2 presents the design and implementation of 4 ultra-wideband RF switches based on a phase change material single-pole-single-throw (SPST) switch, which is integrated in the back-end-of-line (BEOL) of a standard SiGe BiCMOS process from Tower Semiconductor. A series-shunt SPST, a single-pole-double-throw (SPDT) and a single-pole-four-throw (SP4T) switch are presented. The switches' measured performance validates the record on-chip Figure of Merit (FoM) of 12 fs leading to ultra-wideband insertion loss, matching and isolation performance all the way to $>$ 67 GHz. Using the same PCM switch at its core, the design of a TTD unit is also illustrated. The chip uses a variable true time delay architecture through progressively increasing true time delay paths selected using cascaded PCM switches. To the best of our knowledge, the chip illustrates the largest relative group delay on a silicon IC of 124 ps along with excellent matching and insertion loss performance from 2-65 GHz, which make it an excellent candidate for ultra wideband instantaneous bandwidth applications.

Chapter 3 presents a 19-22 GHz high linearity SiGe BiCMOS Rx/Tx beamformer channel with 16.5 dB of midband gain, 7.2 dB NF and an IIP3 $>$ 0 dBm. The beamformer integrates 5-bits of phase and gain control (true-monotonical phase control and 15.5 dB of total attenuation) and achieves an OP_{1dB} of 8 dBm and an OP_{sat} of 9.5 dBm for a 240 mW DC consumption from a 2.4 V supply. For the design of the active stages the npn device of the 0.12 μm SiGe

BiCMOS node was used and for the passive components (passive phase shifters and attenuators) the triple-well MOS device. The presented results correspond to a wirebonded version of the channel, used for probe measurements. However, the implementation also included a flip-chip version of the channel. The chip is redesigned to accomodate the insertion of the meatal balls and its functionality (16 dB gain, 7 dB NF and $>$ 0 dBm IIP3) is maintained and demostrated through connectorized measurements. The design integrates an in-house fully functional SPI control scheme and biasing circuits, enabling the C4 implementation to be readily used in the design of high-performance phased arrays at K-band.

Chapter 4 presents a 132-142 GHz Rx beamformer channel with fully integrated phase and gain control at D-band. The channel's measurements showed 19 dB of midband gain at 137 GHz, 7 dB NF, OP_{1dB} of 2.5 dBm along with 4-bit phase control and 3-bit gain control (true-monotonical phase control and 5.6 dB of total attenuation) with 105 mW peak power consumption. The channel integrates a D-band vector-modulator based phase shifter along with a D-band variable gain amplifier (VGA). The VGA is based on a transformer coupled neutralized pseudo-differential pair, a modified version of a previously developed D-band LNA from TICS-G lab. The D-band NF and large signal results are validated through waveguide measurements in our lab. To our knowledge this is the first D-band Rx channel with fully integrated phase shifter and VGA and a NF of 7 dB and competitive power consumption, pushing the envelope in the potential architectures for D-band beamforming, making this design a potential candidate for the design of large phased arrays at 140 GHz.

Chapter 5 concludes the dissertation and discusses future work.

Chapter 2

DC-67 GHz Phase Change Material (PCM) Switches and a 5-Bit True Time Delay Unit in a SiGe BiCMOS Process

2.1 Introduction

2.1.1 RF Switch Technologies

RF switches are ubiquitous in modern communication system-on-chip implementations. As the need for higher integration of multi-band systems on chip [7] is increasing (Figure 1.2b) in order to reduce the cost, so does the need for highly competitive RF switches. The issue becomes even more challenging at mm-wave frequencies where the switch FoM becomes tremendously important for the system level considerations. The trade-off between insertion loss, isolation, linearity and size becomes more critical as the frequency increases.

Wideband switches with reduced insertion loss and high isolation at microwave and millimeter wave frequencies are increasingly desirable to accommodate a multitude of potential applications spanning from 1:N switch networks [10]- [11]- [12] to transmit and receive switches.

Switches with reduced IL can significantly relax system specifications [13], and T/R switches with increased isolation can alleviate system problems in tranceivers [13]- [14].

State-of-the-art switch implementations in silicon offer a figure of merit $R_{ON}C_{OFF}$ of 120-150 fs, with regard to the intrinsic device performance. Several wideband switches using these processes are presented in literature but the fundamental trade-off between the large device area needed to implement a low IL switch and the associated capacitance per unit area is limiting the isolation performance at mm-wave frequencies.

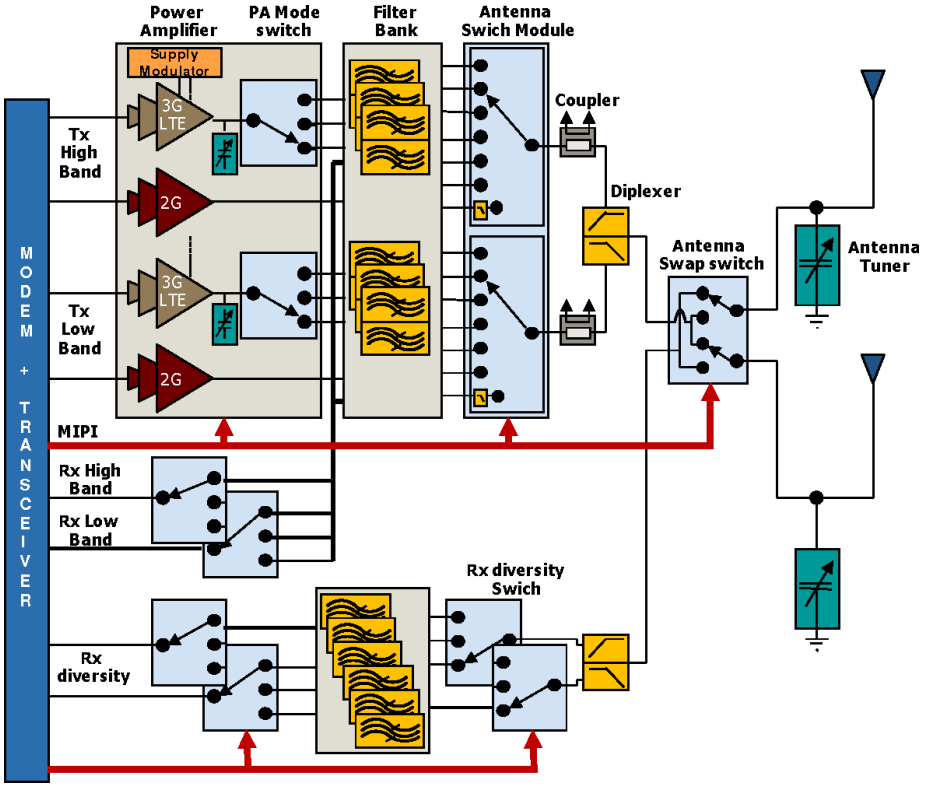


Figure 2.1: Functional Diagram of LTE Front-End Module [7].

The FoM has not improved with process nodes, and CMOS switches built using 130nm, 90nm and 40nm CMOS have nearly the same FoM. 45RFSOI and 22FDX, both based on silicon-on-insulator process have slightly better FoM, but still in the 120 fs range [29]- [30]. The main advantage of RF-SOI switches is not only their FoM, but also the capability of high power handling due to device stacking [31]- [32].

In an effort to break the FoM trade-off between the insertion loss and isolation performance, various alternatives are presented in literature, each with its own advantages and drawbacks. RF MEMS switches with very low FoM (8-16 fs) are illustrated in literature [33] but can only be used in specific applications due to their integration limitations.

Another potential candidate are switches based on Phase Change Materials (PCM). PCM switches illustrate a FoM that is an order of magnitude less than their most competitive antagonists [34]- [39] (Figure 2.2) in both silicon and other technologies (GaN, InP, GaAs etc.). Other than the FoM improvement, the PCM switch power handling is also far superior to its CMOS counterparts. The PCM switch can handle very high RF power levels at its ON-state (33 dBm) [45] without stacking and a degradation in its FoM due to connection parasitics. The presented IP3 in literature is 72 dBm [42].

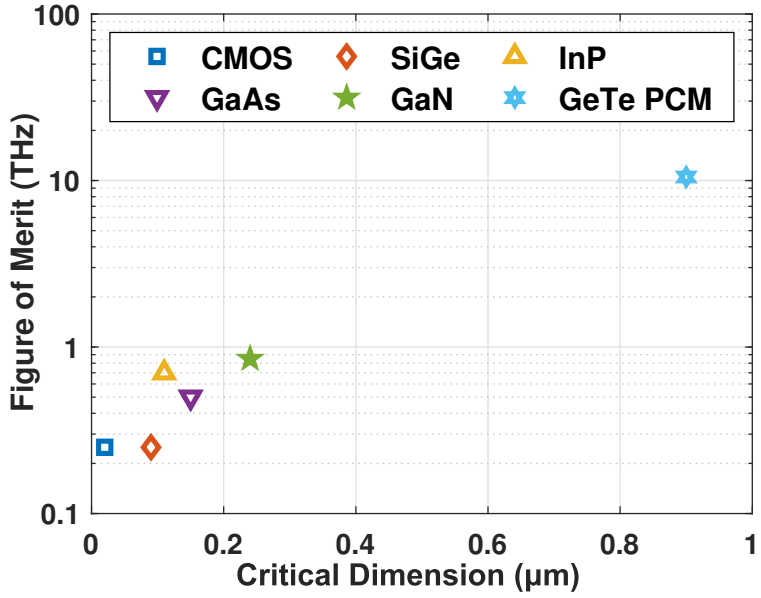


Figure 2.2: Comparison of switch technology FoM ($F_{co} = \frac{1}{2\pi R_{ON} C_{OFF}}$) and critical dimension [8].

Figure 2.3a-Figure 2.3b clearly illustrate the superiority of the GeTe PCM crystal versus all technology nodes, both from an isolation and insertion loss perspective.

The PCM switch integration in a commercial SiGe BiCMOS process [40]- [44] by Tower

Semiconductor allows for the utilization of the tremendous improvement in the FoM in actual performance at millimeter wave either from multi-pole switches or in the switch utilization in passive true time delay unit implementations. The switch can now be used as a building block from designers along with all the other advantages offered in the BEOL and front-end of the SiGe BiCMOS SBC18H3 process.

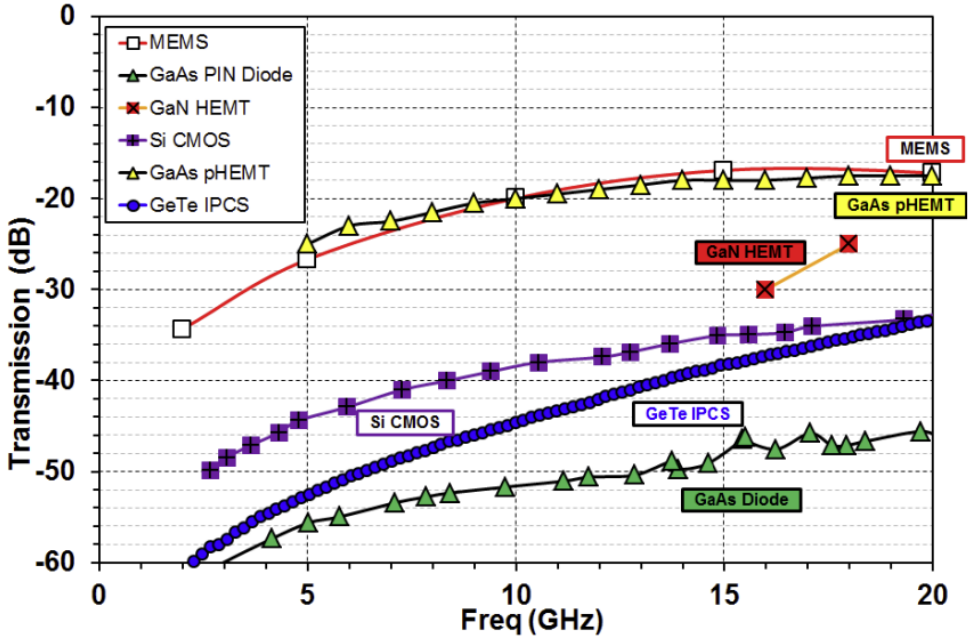
2.1.2 True Time Delay Architectures

TTD units provide a variable group delay within a frequency band and can be used in wideband phased arrays, radars and imaging or tracking sensors [16]- [17]. Other application areas involve wideband phased-arrays requiring TTD units at the element level while TTD units are also placed on sub-arrays for pattern alignment required in GHz-wide instantaneous bandwidths [18].

There have been several illustrations of TTD units in literature. Initially, varactor-based transmission line implementations are used to modify the effective capacitance per unit length of the transmission line leading to an effective modification of the phase velocity [19]- [20]- [21]. This allows for continuous group delay control with the drawback of achieving small maximum relative group delay.

Low loss and high isolation switches can also be utilized for path selecting applications, including variable attenuators [15] and variable group delay paths. Depending on the selected route, the signal propagates through different group delay paths leading to an N-bit TTD unit [22]- [24], [27]. Finally, all-pass networks have also been utilized in TTD units [17], [25].

This chapter presents the utilization of a commercially available PCM switch integrated in a production scale SiGe BiCMOS process for the design of ultra wideband and higher complexity switches along with a state-of-the-art true time delay unit using a transmission-line based implementation. Section 2.1 introduces the PCM switch and showcases its integration in the BEOL of SBC18H3 process. Sections 2.2 present4 the design and measurement results of the



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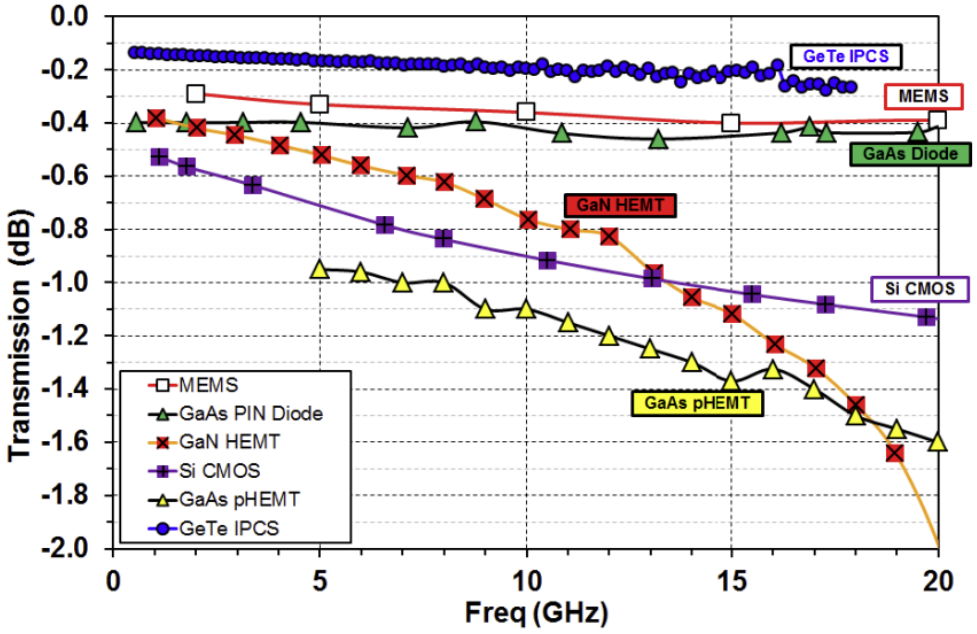


(b)

Figure 2.3: Insertion loss and isolation performance of various technology nodes [8].

wideband PCM-based switches. Section 2.3 presents the TTD unit design considerations and the measurement results. Sections 2.4 and 2.5 conclude this chapter.

2.1.3 Global Foundries SBC18H3PCA Process

The PCM switch used in this work is developed by Tower Semiconductor and is integrated in the BEOL of a 0.18 μm SiGe BiCMOS node (SBC18H3PCA). It is similar in integration as shown in Figure 2.4 but does not incorporate an SOI substrate and instead uses a standard low resistivity p-type substrate. The distance between the thick top metals is increased from 2 μm to 6.5 μm so that the PCM core can be integrated [43]. The switch RF and control terminals can be accessed through metal contacts located on M6. The PCM switch size is 20 μm x 25 μm. All other specifications of the back-end and the front-end of the process remain the same [44].

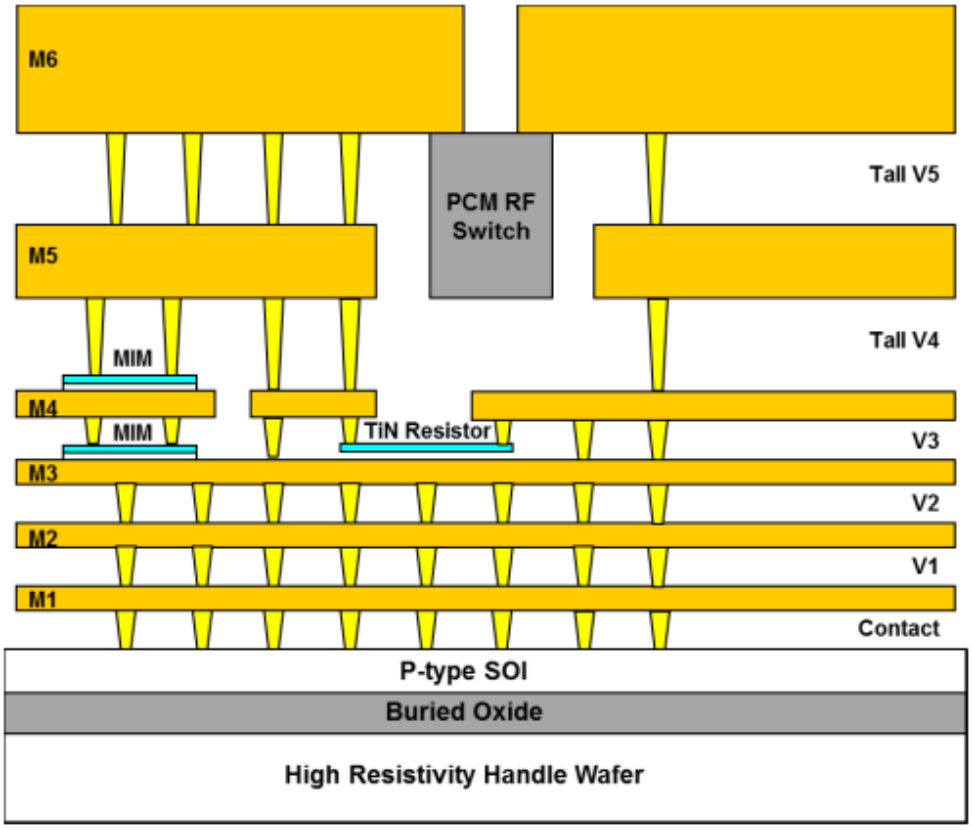


Figure 2.4: Cross-section of the SiGe BiCMOS SBC18H3PCA process where the PCM RF switch is monolithically integrated between M5 and M6 [43].

2.1.4 PCM Switch Characteristics

The switch is fundamentally a chalcogenide-based (GeTe) crystal that possesses a high resistivity amorphous state and a low resistivity crystallic state . The switch comes naturally in the low-resistivity, crystallic state (ON-state). For the switch to transition to the OFF-state, a voltage pulse needs to be applied on the heater resistor that is integrated within the PCM crystal core for the crystal to amorphize. In order for it to get back to its ON state, another pulse with different characteristics needs to be re-applied.

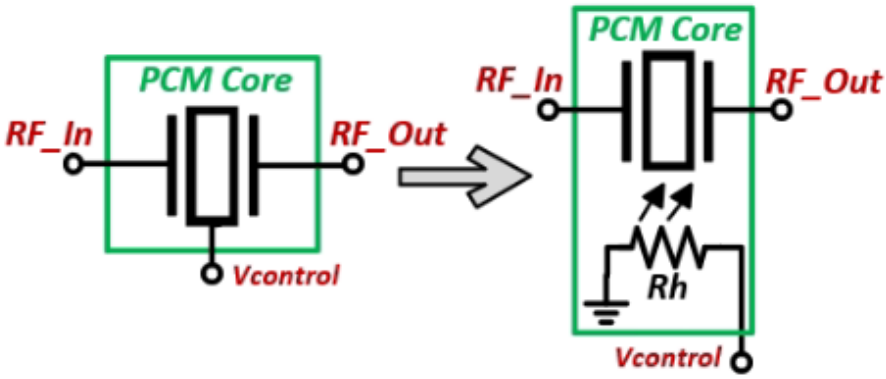
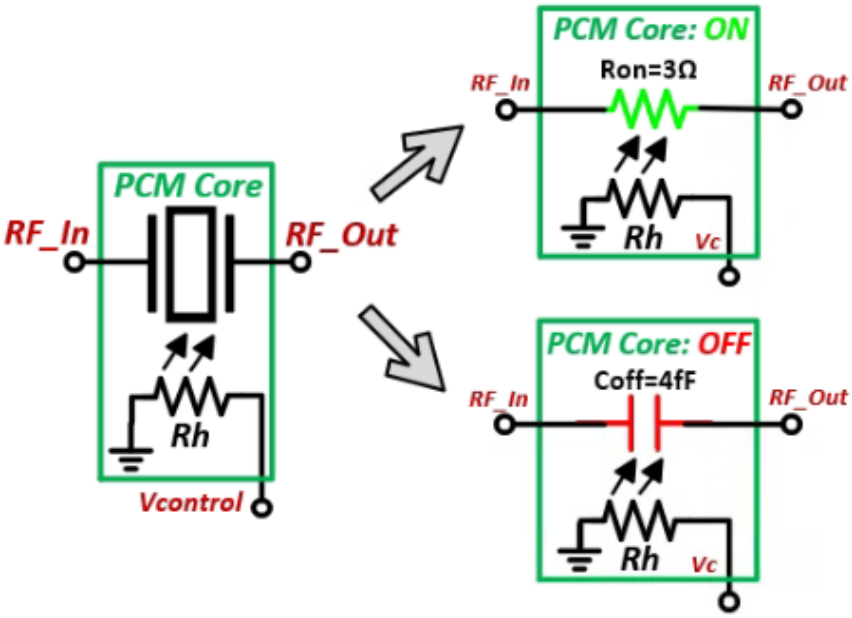


Figure 2.5: (a) PCM switch RF and control terminals.

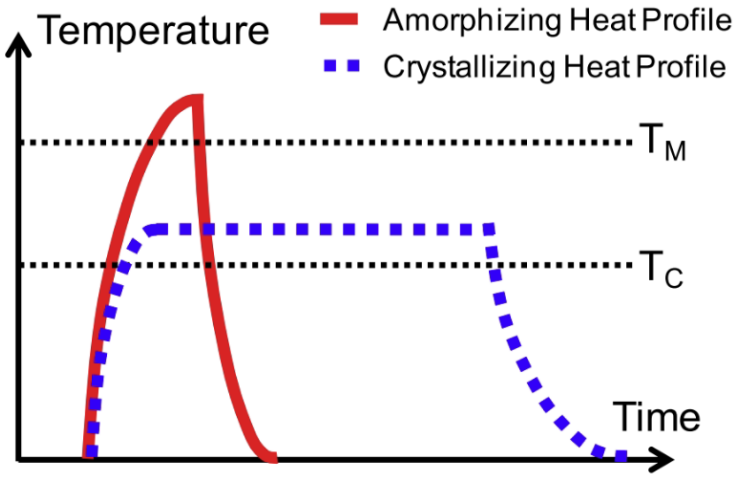
2.1.5 PCM Switch Actuation

Transitioning between the amorphous (insulating) and crystalline (conductive) states is accomplished through controlled heat excitation of the crystal core [40]. When the PCM is in the crystalline state, the transition to the amorphous state is achieved by heating it beyond its melting temperature (TM), and quenching it to solidify the atoms in the amorphous state (red solid line in Figure 2.6b). When the PCM is in the amorphous state, the transition to the crystalline state is achieved by heating the material above its re-crystallization temperature (TC), which is the temperature at which nucleation and growth of crystalline grains is enabled (blue dashed line in Figure 2.6b) [44].

Thermal excitation works as the actuator for the PCM crystal from its ON ($R_{ON} = 3\ \Omega$) to its OFF ($C_{OFF} = 4$ fF) state. The PCM switch is also naturally non-volatile, meaning that it can retain its phase state indefinitely [40].



(a)



(b)

Figure 2.6: (a) PCM switch resistive and capacitive state. (b) Voltage pulse characteristics for PCM switch actuation.

2.2 Wideband PCM Switches

In the following subsections the design considerations and suggested implementations of the wideband PCM switches will be presented along with the measurement results.

2.2.1 SPST PCM Switch

This section presents an SPST switch (Figure 2.7) using the PCM switch at its core (20 μm x 25 μm). The control terminals are tied to DC pads to externally provide the voltage excitation. Due to the low C_{off}, no inductive matching is used and the switch is directly connected to 52 Ω coplanar waveguide transmission lines.

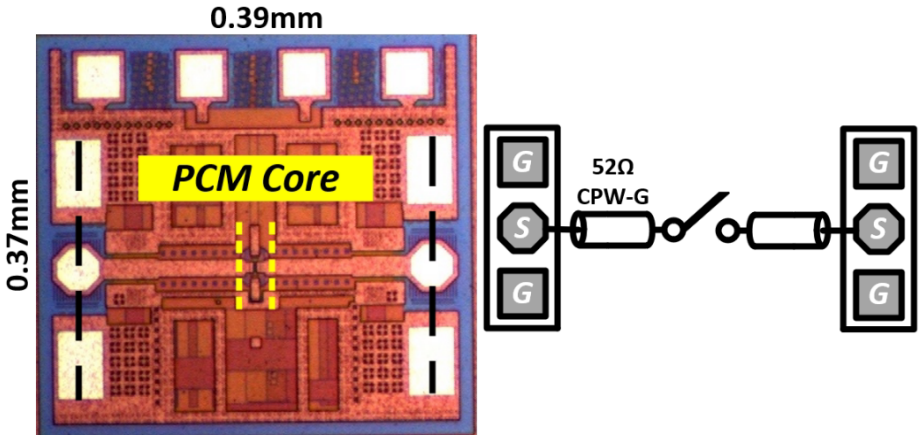
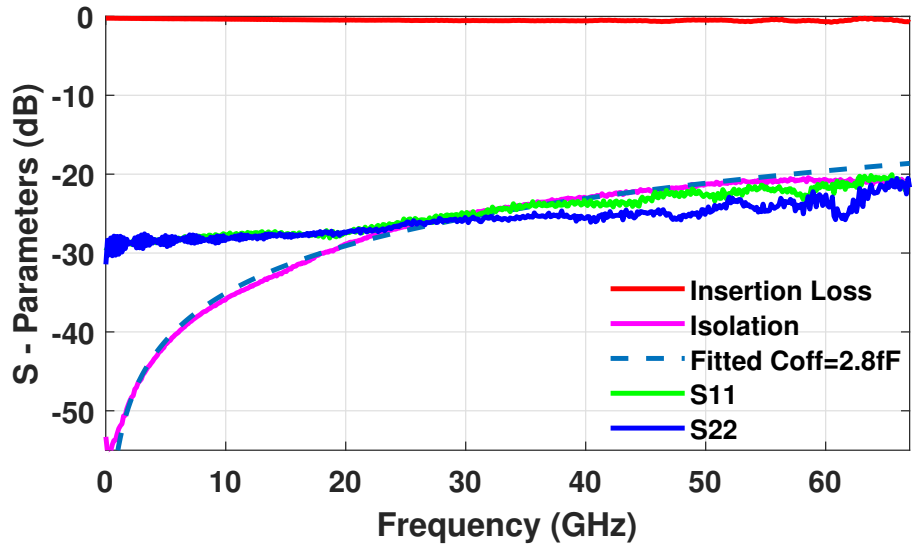


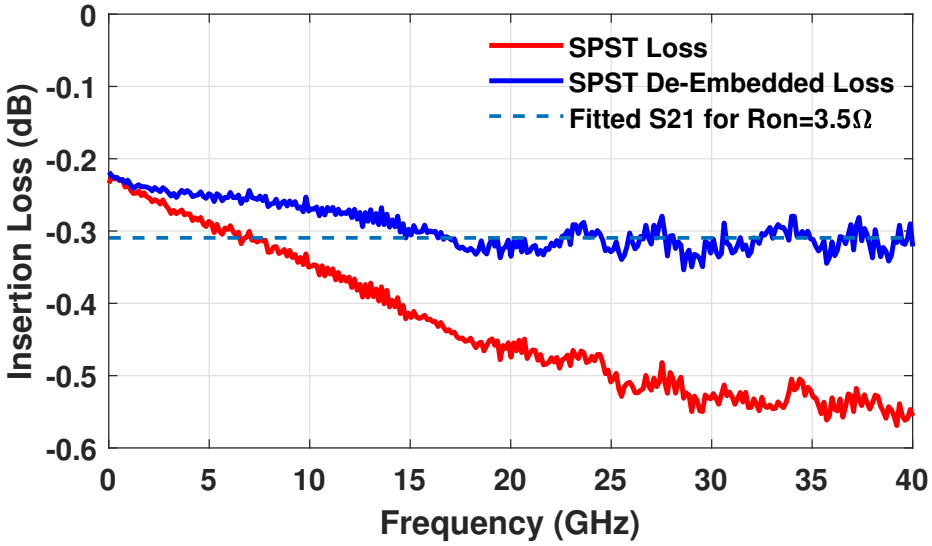
Figure 2.7: (a) Layout and schematic of the SPST switch.

Measurements are done using the Keysight PNA-X with GSG probe-tip calibration. This design achieves an insertion loss of 0.55 dB at 30 GHz and an isolation of 25 dB at 30 GHz (Figure 2.8a), when referenced to the GSG pads. When the transmission lines are de-embedded, the SPST switch achieves an IL of 0.25-0.3 dB and is approximately frequency independent (Figure 2.8b). This IL agrees with the expected value of:

$$S_{21} \approx 1 - \frac{R_{on}}{2Z_o} = -0.3dB \text{ with } R_{on} = 3.5\Omega$$



(a)



(b)

Figure 2.8: (a) Measured S-parameters. (b) Measured insertion loss.

The measured isolation is easily fitted to:

$$S_{21} \approx 2\omega Z_o C_{off} \text{ with } C_{off} = 2.8fF$$

This leads to a measured FoM of 9.8 fs, close the nominal value of 12 fs. The switch is well matched up to 67 GHz due to its low C_{off}. Through this set of measurements the anticipated value of the PCM switch FoM is validated.

2.2.2 Series-Shunt SPST PCM Switch

In order to increase the switch isolation, a series-shunt SPST is presented in (Figure 2.9) (50 μm x 50 μm). The shunt switch is placed in one arm of the CPW line (in the gap) and additional isolation could be potentially obtained if two shunt switch places are used in the CPW-G line.

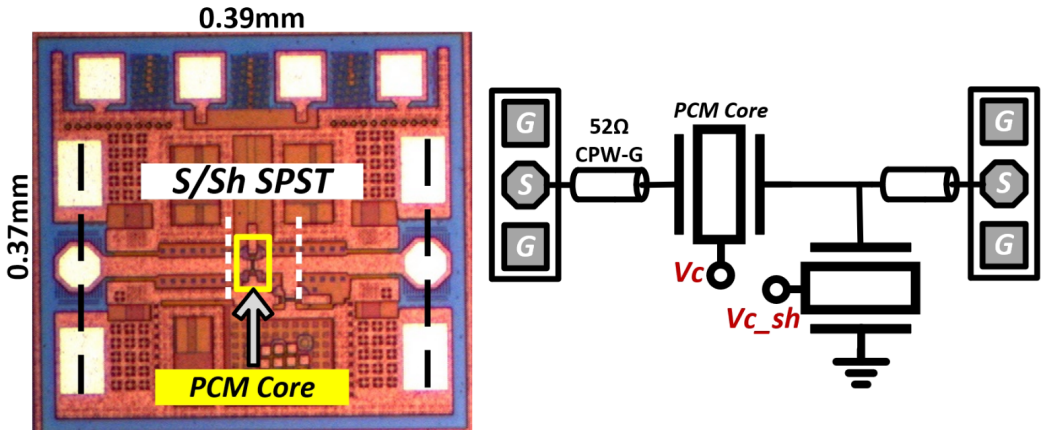


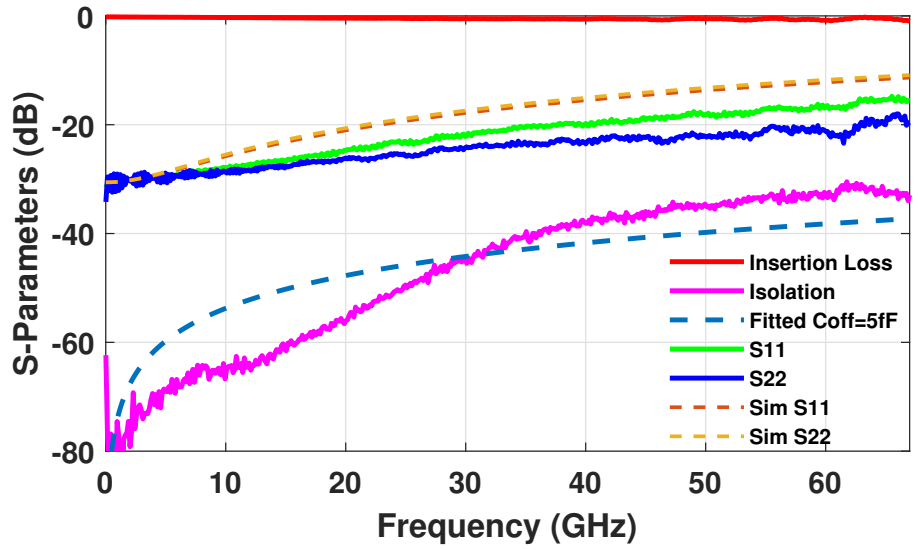
Figure 2.9: (a.) Layout and schematic of the series-shunt SPST switch.

In the OFF state, the shunt switch is turned ON, providing a low-impedance path to ground thus increasing the isolation. The series-shunt isolation is given by:

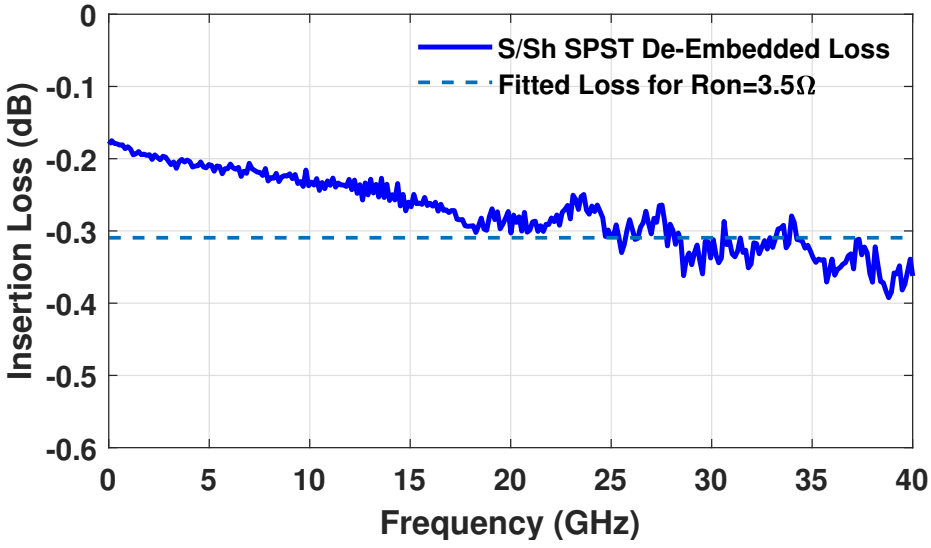
$$S_{21} = 2\omega R_{on} C_{off}$$

The measured isolation is 45 dB at 30 GHz and agrees well with $C_{off} = 5$ fF and R_{on} = 3.5 Ω (Figure 2.10a). The leakage (worse isolation) above 30 GHz is due to only one gap being shorted and not both in the G-CPW line. In the ON-state, the series-shunt switch has the same IL

as the standard series switch due to the low Coff of the shunt arm which will start affecting the IL at very high frequencies, and the measured IL is 0.3 dB when referenced to the switch core (Figure 2.10b).



(a)



(b)

Figure 2.10: (a) Measured S-parameters. (b) Measured insertion loss.

2.2.3 SPDT PCM Switch

The high-isolation series-shunt switch is utilized as a building block for a wideband SPDT switch (Figure 2.11). 90 pH series inductors with a Q of 12 at 30 GHz are used at the input and output port to tune out the added SPST capacitance of the inactivated path. The SPDT switch is 300 μm x 160 μm, with the area equally distributed between the PCM switch core and the inductors. Small CPW-G transmission lines lead to the GSG pads.

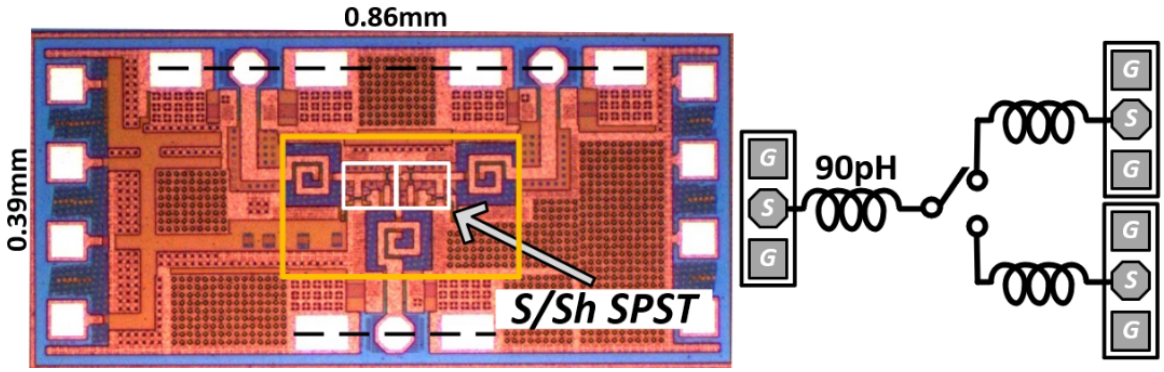
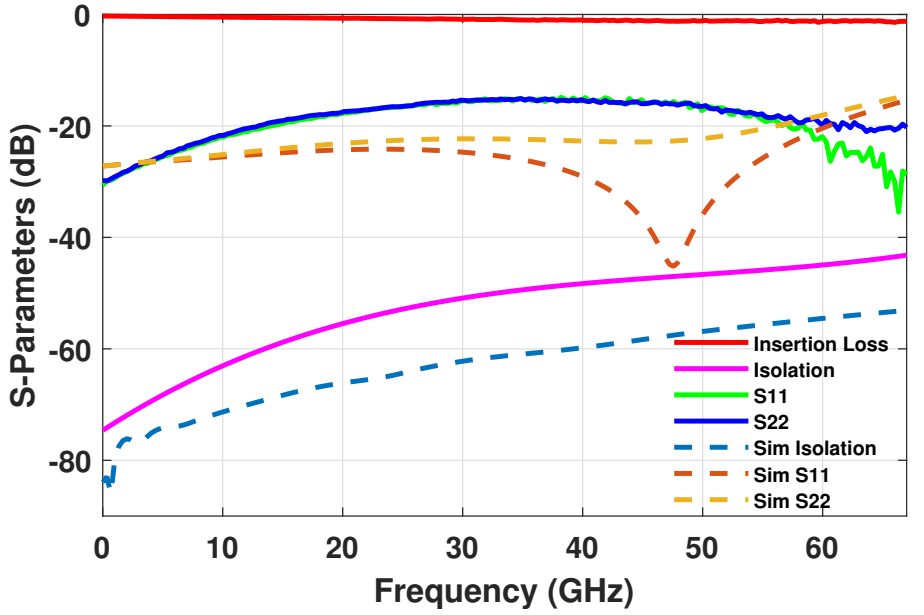


Figure 2.11: (a) Layout and schematic of the SPDT switch.

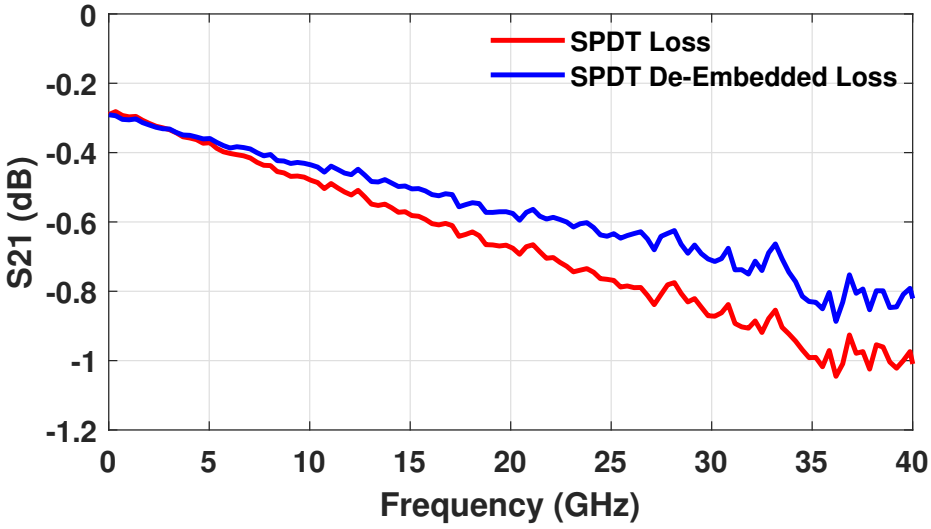
The measured SPDT results in an isolation of 45 dB at 30 GHz (as expected from the SPST measurements), good impedance matching ($S_{11}, S_{22} <$ -15 dB from 0-67 GHz) and an isolation of 45 dB at 30 GHz Figure 2.12a.

The SPDT switch insertion loss, when referenced to the inductors (switch ports) is 0.6 dB at 30 GHz Figure 2.12b. The increase in the switch IL can be traced to the inductor resistance (1.5 Ω at 30 GHz), which results in an additional 0.3 dB loss due to the use of two inductors. The other 0.1 dB discrepancy is due to the reflected power (S_{11} of -17 dB at 30 GHz).

The excellent performance of the SPDT switch, both in insertion loss and isolation, will allow for its use as a building block in the design of the TTD unit.



(a)



(b)

Figure 2.12: (a) Measured S-parameters. (b) Measured insertion loss.

2.2.4 SP4T PCM Switch

The SP4T employs 4 series-shunt SPST switches as shown in Figure 2.13. 100 pH inductors are added at the input at output ports to tune out the OFF-state capacitances of the inactivated paths, leading to a size of 360 μm x 210 μm.

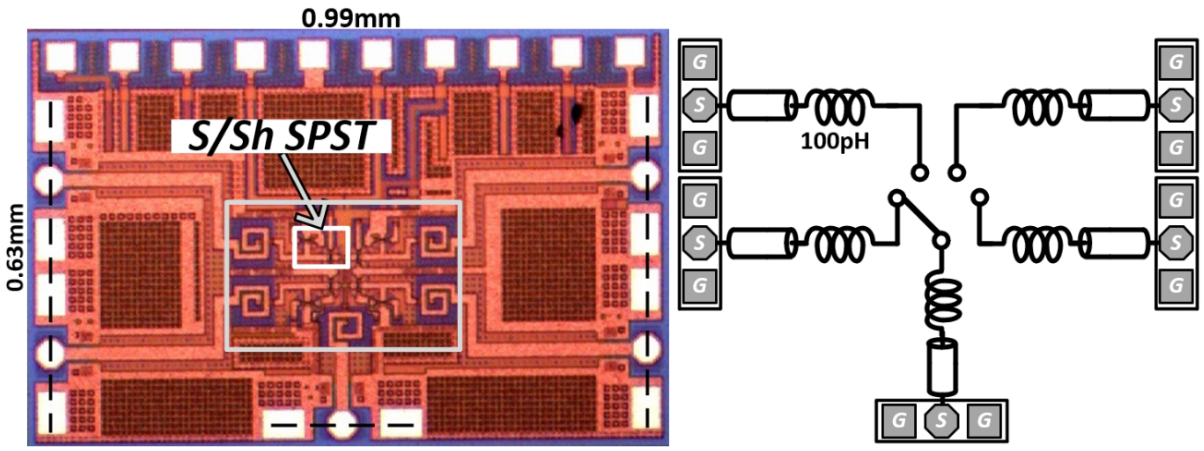


Figure 2.13: (a) Layout and schematic of the SP4T switch.

The resulting SP4T switch has excellent impedance matching to 67 GHz, with an isolation of 40 dB at 30 GHz (Figure 2.14a), while the de-embedded IL at the reference planes is 0.8 dB at 30 GHz (Figure 2.14b), with 0.3 dB due to the switch core, 0.35 dB due to the inductors and 0.1 - 0.15 dB due to matching loss.

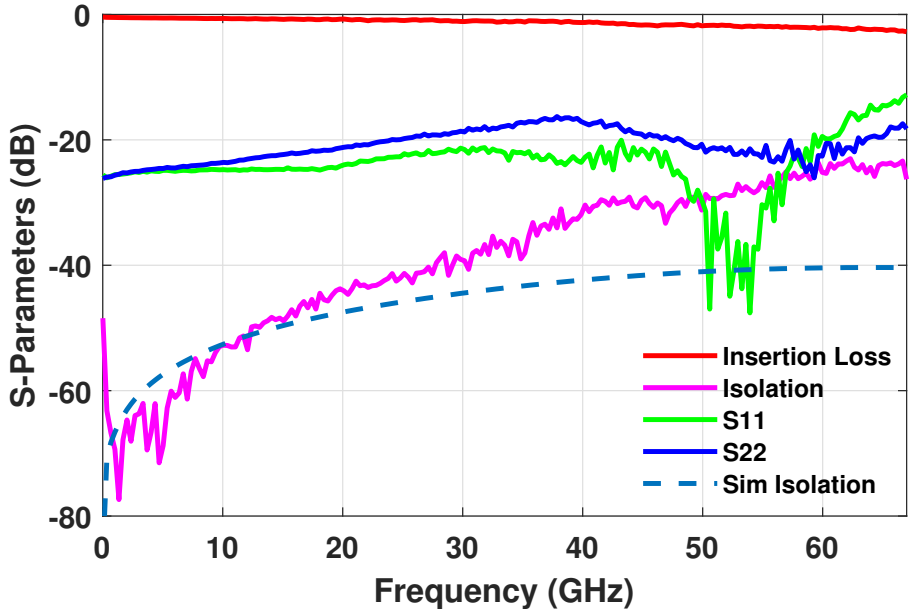
2.3 5-Bit True-Time-Delay Unit

In this section, the wideband SPDT PCM switch will be utilized along with coplanar waveguide and microstrip transmission lines to design a 5-bit variable path group delay unit.

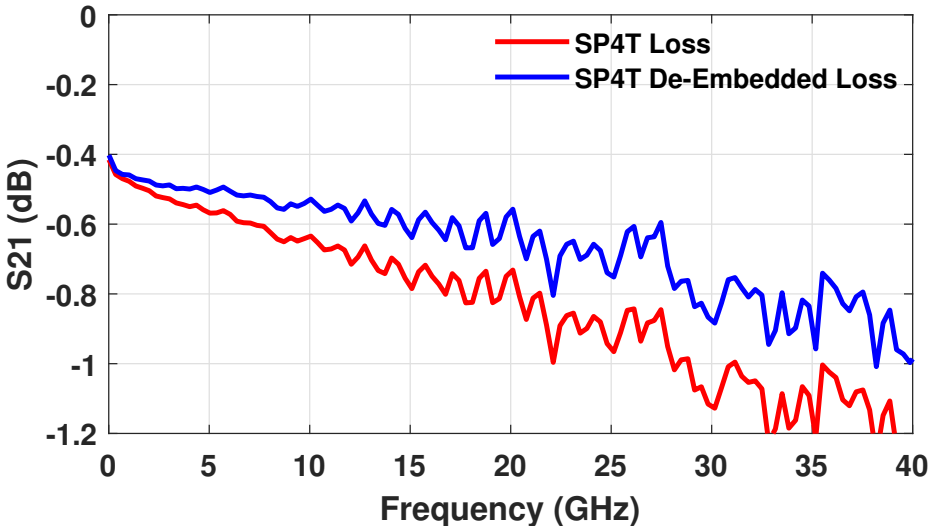
2.3.1 Transmission Line Design

The ground CPW lines are routed on the top thick metal, which is also the metal on which the PCM switch RF terminals lie. The CPWG has a signal metal width of 15 µm on M6 with a gap of 15 µm and M4 metal as ground plane, constituting a reference interface of 52Ω (Figure 2.15a). The measured insertion loss per mm and 100 ps is 0.35 dB and 4.5 dB, respectively (Figure 2.15b).

The presented measured results for the CPW-G loss are generated from measurements on 2 small transmission line test cells. Due to the absolute value of the relative loss difference



(a)



(b)

Figure 2.14: (a) Layout and schematic of the SP4T switch (b) Measured S-parameters. (c) Measured insertion loss.

between the 2 different transmission lines being comparable to the calibration error, the presented results may be $\pm 20\%$ off from the actual values.

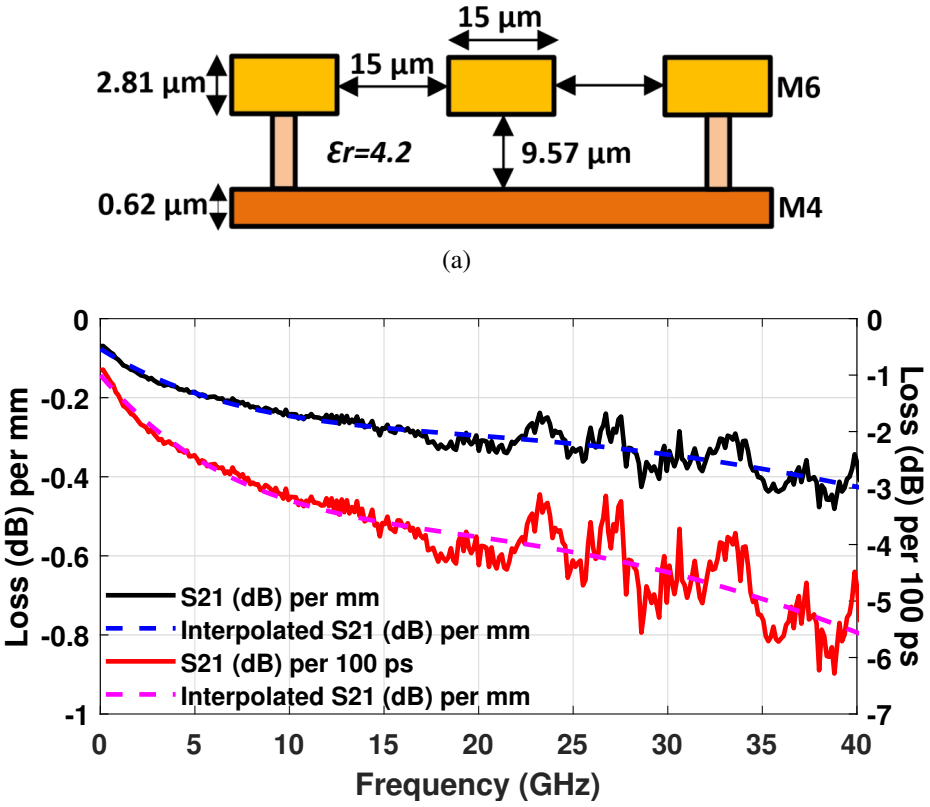


Figure 2.15: (a) 52 Ω G-CPW dimensions. (b) Loss per mm and per 100 ps of group delay.

2.3.2 Layout Considerations

The TTD unit employs cascaded SPDT switches and 50 Ω G-CPW and microstrip transmission lines of binary-weighted group delay lengths (Figure 2.16). Functionally, each of the 5 bits is comprised of two back-to-back series-shunt SPDT switches and two transmission lines, a reference and a delay line, with the smallest delay state introducing a 4 ps relative group delay with respect to the refence state. Other delays states are 8, 16, 32 and 64 ps. The input and output GSG pads lie on the same side of the die in order to accommodate the transmission line layout (Figure 2.17).

The reference line is not a design parameter. It is determined by the TTD unit layout and care is taken to make a compact design with the shortest line lengths. This led to a design where the SPDT switches were positioned in a back-to-back configuration, in order to avoid excess

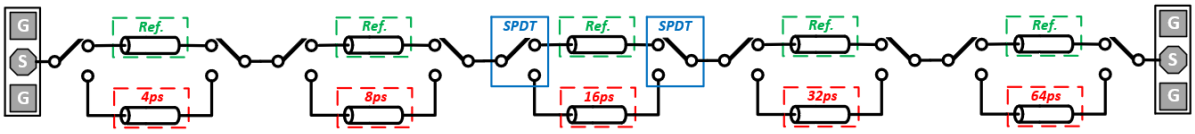


Figure 2.16: Schematic representation of the 5-bit TTD unit.

transmission line loss on the reference state. The lowest TTD loss is given by the SPDT loss (10 units) and the reference line loss, which is 1.1 mm long and corresponds to 6.7 ps of group delay. This reference state loss is equal to 6.5 dB at 30 GHz and is attributed almost entirely to the 10 activated SPDT switches in the signal path.

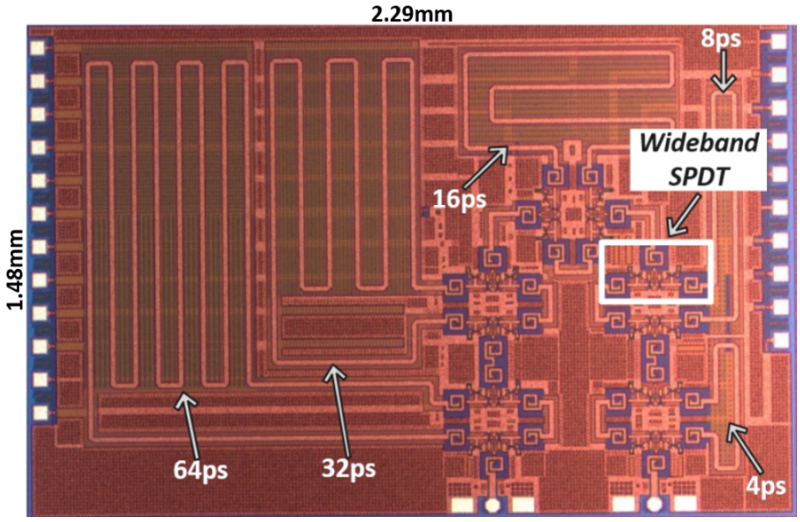


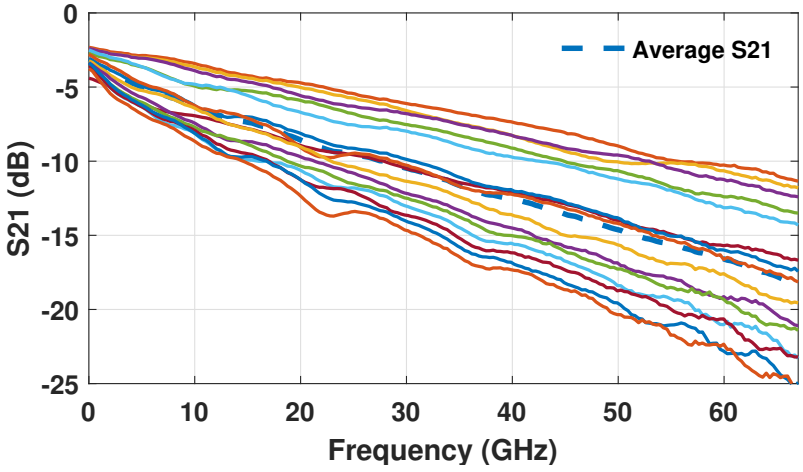
Figure 2.17: Layout of the 5-bit TTD phase shifter.

In order to save area, the signal path transmission lines were folded for the 16, 32 ps and 64 ps TLs. A distance of at least 50 μm between the alternating paths was selected to avoid cross-coupling which can lead to a modification of the transmission line characteristic impedance which leads to increased reflections and affects the group delay flatness. The simulated coupling between the branches of the 64 ps TL is less than -35 dB at 30 GHz.

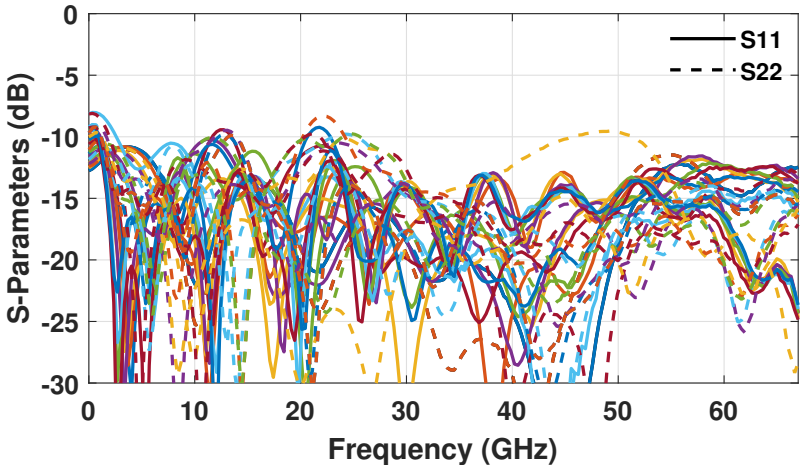
This proposed layout leads to a fabricated chip with a total area of 3.39 mm^2, where a small part of the area corresponds to the DC pads needed for the control of all the PCM switches involved in the signal path.

2.3.3 Measurements

The TTD unit measurements used on-wafer GSG probes and Keysight's N5247B 2-port 10 MHz - 67 GHz PNA-X. All measurements for loss and group delay correspond to reference planes on the input and output GSG pads.



(a)



(b)

Figure 2.18: (a) Insertion loss over group delay states. (b) Measured S-parameters over group delay states.

The measured insertion loss per group delay state and the input and output impedance matching performance are presented in Figure 2.18a-Figure 2.18b. The 5-bit TTD insertion loss varies between 6.5 dB (minimum group delay state) to 15.5 dB (116 ps group delay state) at 30

GHz. The additional 9 dB of insertion loss is due to the added transmission-line loss.

The PCM SPDTs allow for high isolation up to 67 GHz, between the activated and de-activated RF paths, thereby eliminating S_{21} resonances which can appear in TTD units [24]. Also, the excellent impedance matching between the cascaded SPDT switches and the meticulous EM simulations in the transmission lines to provide a constant impedance across the variable signal path, allows for excellent impedance matching across all group delay states.

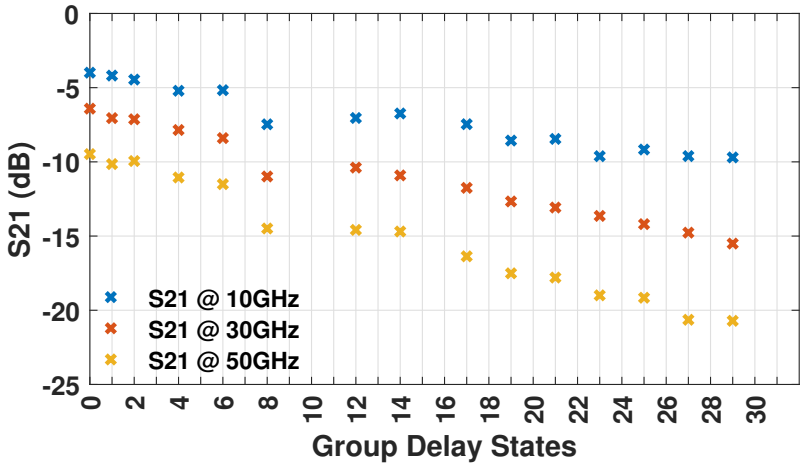


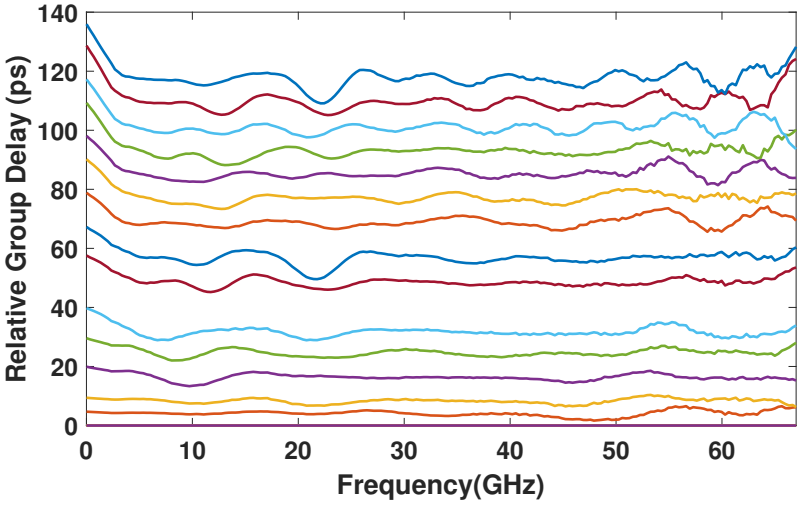
Figure 2.19: Measured S_{21} versus group delay states at 10, 30 and 50 GHz.

Table 2.1: TTD Insertion Loss Breakdown at 30 GHz

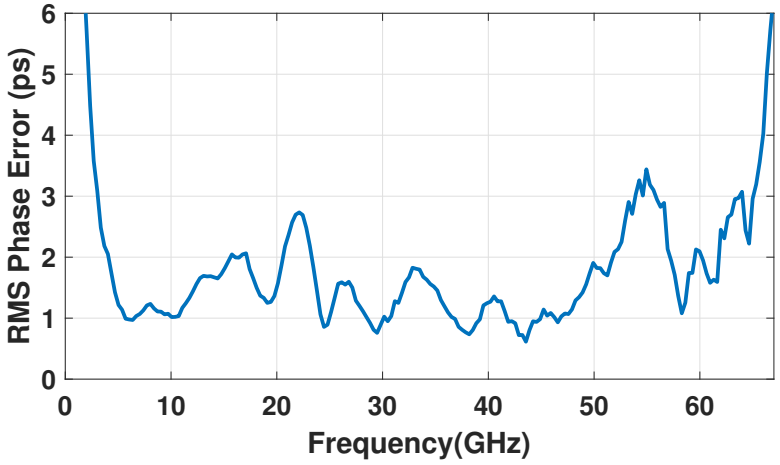
Abslolute GD (ps)	Measured Loss (dB)	Simulated Loss (dB)
0	-6.5	-7
56	-11.4	-9.8
116	-15.5	-12.3

Figure 2.19 presents the insertion loss performance across all group delay state for 3 frequency points, illustrating the expected trend of the insertion loss that widens at higher frequency across the same group delay state. (Table 3.1)illustrates the measured and simulated insertion loss versus group delay states for, which are in good agreement, given the uncertainty in the transmission line loss calculation due to calibration inaccuracies, that become more significant as the transmission line length increases.

Another interesting note that arises from our design choices is that if this design was to be used for a beamformer design the RMS gain error across the group delay states would progressively increase versus frequency, which is sub-optimal. In this implementation, our target is to have a proof of concept and this was a secondary issue. However in future implementations, the design can be modified to intentionally introduce loss in the reference path to match the loss or the selected group delay. This can be achieved through matched attenuators that will only introduce loss and not introduce group delay variation in the signal path.



(a)



(b)

Figure 2.20: (a) Measured relative group delay states. (b) RMS group delay error.

Figure 2.20a-Figure 2.20b present the measured relative group delay states and flatness versus frequency along with the RMS group delay error. The results indicate no visible resonant points leading to abrupt changes in the group delay response. The PCM SPDTs allow for high isolation up to 67 GHz, between the activated and de-activated RF paths, thereby eliminating S_{21} resonances which can appear in TTD units [24].

Also, the excellent impedance matching between the cascaded SPDT switches and the off-state paths across the signal path allow for the reflected waves to minimally impact the group delay flatness. As a result the measured group delay flatness is 1-2 ps across the 2 - 65 GHz range with 2 frequency points at 22 GHz and 55 GHz that becomes 2-3 ps. We attribute the 20-24 GHz region to a calibration error as we see such a discrepancy in other component tests in our lab. The 55 GHz region also appears to be setup related. The monotonic behavior of the TTD unit is also shown in Figure 2.21, where the average group delay is super-imposed on the ideal group delay, illustrating good agreement.

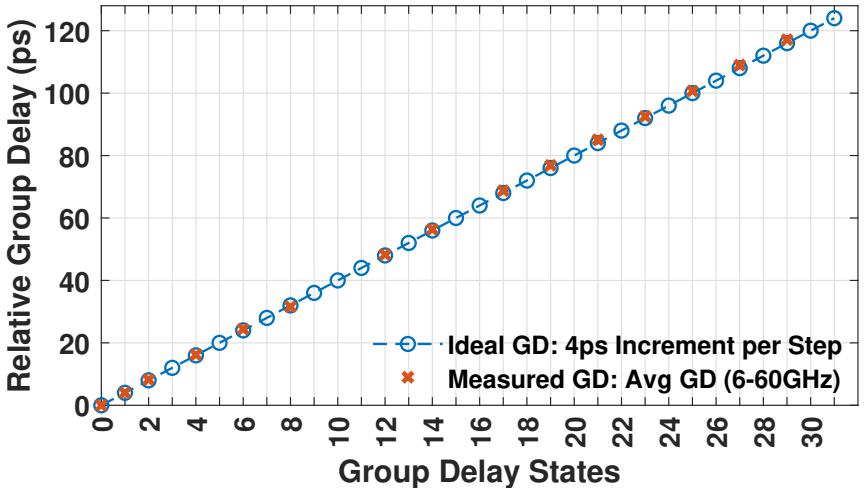


Figure 2.21: Monotonically increasing states.

Note that not all states were activated in the measurements as the TTD unit requires a complex activation scheme with on/off pulses given to 20-40 switches. In the future, a decoder and a pulser will be integrated on the TTD chip in order to resolve this issue.

2.3.4 TTD Unit Low Frequency Performance

In all group delay measurements presented, the low frequency response exhibits a divergent behavior below 2.3 GHz. This limits the TTD unit from reaching a true DC to 65 GHz performance.

The divergent behavior is attributed to the absence of the skin effect component on the transmission line resistance per unit length at frequencies lower than 2.3 GHz. Specifically, the skin effect will stop contributing to the top metal (M6) resistance at the frequency point where δ becomes equal to half the thickness of M6 ($t = 2.81\ \mu m$). In this case, when δ becomes 1.4 μm, the G-CPW line characteristic impedance will start diverging from its 52 Ω nominal value.

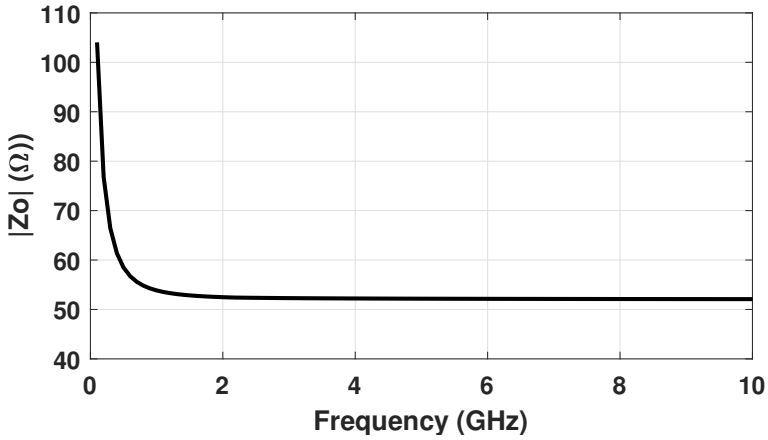
The governing equation of Z_o is:

$$Z_o = \sqrt{\frac{Rs + j\omega L}{G + j\omega C}}$$

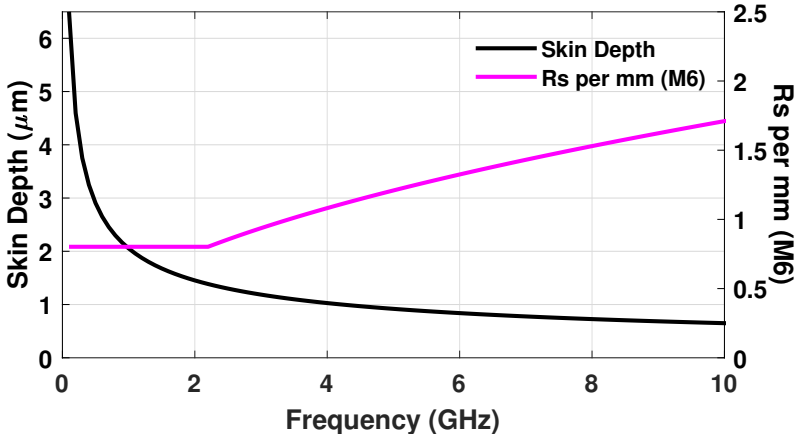
Assuming that G is negligible, Z_o can be written as:

$$Z_o \approx \sqrt{\frac{Rs + j\omega L}{j\omega C}} = \sqrt{\frac{Rs}{j\omega C} + \frac{L}{C}} \Longrightarrow |Im(Z_o)| >> 0 \text{ for } f < 2.3 \text{ GHz}$$

This ensues that for frequencies lower than 2.3 GHz ($\delta > 1.4\ \mu$m), Rs will become frequency independent and the Zo term will incur an increasing imaginary term as the frequency approaches DC, which changes the magnitute of Zo (Fig. 11). This in turn affects the group delay below 2 GHz. The only solution is to use thicker metal lines, which is typical in printed-circuit boards (30-40 μm of copper), but RFIC back-ends limit the top metal to $\sim 3\ \mu$m, thus limiting the TTD operation to 2 GHz.



(a)



(b)

Figure 2.22: (a) Simulated Zo versus frequency - frequency point of divergence agrees well with the measured GD divergence at $\sim$ 2.3 GHz. (b) Simulated skin depth and sheet resistance per mm on M6.

2.4 Conclusion

This section presented four DC-67 GHz PCM-based switches in different configurations (SPST, series-shunt SPST, SPDT and SP4T) and a miniature 5-bit transmission line-based TTD phase shifter.

Table 2.2-Table 2.4 compare the measured performance of the series-shunt SPST, SPDT and SP4T switches with other wideband switches. The combination of low loss and high isolation from DC to $>$ 67 GHz, exhibited by the PCM switches, is the best reported in literature.

Table 2.2: Comparison with wideband SPST switches

	This Work	[46]	[47]	[48]	[49]	[50]	[51]	[33]
IC Process	**PCM***	PCM*	PCM*	PCM*	65nm CMOS	22nm FDSOI	22nm FDSOI	RF MEMS
Frequency (GHz)	**DC-67**	DC-40	DC-25	DC-67	DC-94	10-110	DC-220	DC-40
Nom. Insertion Loss (dB)	**0.2-0.35**	0.2	0.3	0.1-0.4	0.2-1.6	0.3-1.8	0.2-3.1	0.2-0.8
Isolation (dB)	> 32	> 20	> 20	> 16	19-30.2	17-23	22-58	15-50
Core Area (mm^2)	**0.0025**	0.0009	N/A	N/A	0.151	N/A	0.026	N/A

Table 2.3: Comparison with wideband SPDT switches

	This Work	[46]	[52]	[53]	[54]	[55]	[56]	[58]
IC Process	**PCM***	PCM*	PCM*	PCM*	0.13μm SOI	90nm CMOS	45nm SOI	90nm CMOS
Frequency (GHz)	**DC-67**	DC-40	DC-65	DC-20	DC-50	DC-110	DC-50	50-70
Nom. Insertion Loss (dB)	**0.2-0.8**	0.2-0.6	0.5-2.1	2	0.5-2.1	1-5.5	0.5-1.1	1.5-2
Isolation (dB)	**>40**	>20	>25	>18	>27	>40	>20	>25
Core Area (mm^2)	**0.048**	N/A	0.085	N/A	0.068	0.067	0.004	0.27

Table 2.4: Comparison with wideband SP4T switches

	This Work	[46]	[52]	[54]	[57]	[33]
IC Process	**PCM***	PCM*	PCM*	0.13μm SOI	0.13μm CMOS	RF MEMS
Frequency (GHz)	**DC-67**	DC-40	DC-65	DC-35	DC-70	DC-15
Nom. Insertion Loss (dB)	**0.4-1.3**	0.2-1	0.3-1.1	1.1-2.6	1-3.5	0.3-0.8
Isolation (dB)	**>25**	>20	>25	>30	>25	>22
Core Area (mm^2)	**0.076**	N/A	0.167	0.068	0.055	N/A

Table 2.5 presents the comparison on the TTD unit presented in this chapter and other state of the art implementations. To our knowledge, the TTD unit presented in this work achieves the higher relative group delay on a silicon IC, along with widest frequency of operation and lowest loss when measured by (mid-loss value)/(mid-TTD-value). The TTD unit size of 2.29 x 1.48 mm makes it ideal for 2-D phased-arrays with 0.5λ spacing up to 60 GHz and with wideband instantaneous bandwith.

Table 2.5: Performance comparison of TTD units

	This Work	[22]	[23]	[24]	[26]	[27]	[28]
IC Process	**PCM***	0.25um CMOS	0.13um CMOS	RF MEMS	28nm CMOS	PCM*	65nm CMOS
Frequency (GHz)	**3-65**	10-50	15-40	2-18	3-30	26-34	20-30
Max. Rel. G.D. (ps)	**124**	32.8	42	100.8	68.5	19	35.2
Nominal I.L. (dB)	**10.4 at 30 GHz**	15.5 at 30 GHz	14 at 28 GHz	1.6 at 12 GHz	13.5 at 28 GHz	4.9 at 30 GHz	11 at 28 GHz
Loss (dB) per 100 ps	**14.9 at 30 GHz**	96.9 at 30 GHz	66.7 at 28 GHz	3.2 at 12 GHz	34.4 at 28 GHz	51.6 at 30 GHz	62.5 at 12 GHz
Resolution (ps)	**4**	Cont.	3	6.3	4.9	2	0.56
RMS G.D. Error (ps)	$<$ **3**	N.A	N.A	N/A	<2	N/A	N/A
Pdc (mW)	**Passive****	Passive	8.6-24.6	Passive	Passive	Passive**	Passive
Area (mm^2)	**3.39**	0.22	0.99	21.32	0.34	1.4	0.18

* GeTe PCM is integrated in 0.18 μm SiGe BiCMOS BEOL.

** PCM switches do not require constant DC voltage. Voltage is required for transition only.

2.5 Acknowledgment

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Chapter 2, in part, is a reprint of the material as it appears in: D. Baltimas and G. M. Rebeiz, "A 25–50 GHz Phase Change Material (PCM) 5-Bit True Time Delay Phase Shifter in a Production SiGe BiCMOS Process," 2021 IEEE MTT-S International Microwave Symposium (IMS), 2021, pp. 435-437, doi: 10.1109/IMS19712.2021.9574891. The dissertation author was the primary investigator and author of this paper.

Chapter 2, in full, is being prepared to be submitted for publication of the material as it may appear in: D. Baltimas and G. M. Rebeiz, "DC-67 GHz Phase Change Material (PCM)

Switches and a 5-Bit True Time Delay Unit in a SiGe BiCMOS Process", in *IEEE Transactions on Microwave Theory and Techniques*. The dissertation author was the primary investigator and author of this paper.

Chapter 3

K-Band SiGe BiCMOS High Linearity T/R Beamformer Channel with $>$ 0 dBm IIP3 and $<$ 7.2 dB NF

3.1 Introduction

Satellite communication (SATCOM) has emerged as a key solution to providing broadband connection services in low-density rural areas. The non-line-of-sight (NLOS) communication using SATCOM has also advanced significantly [59]. The driving force behind this development is multi-channel SiGe and CMOS beamformer chips that have recently been developed and allow for low-cost phased-array implementations. The K-band SATCOM in silicon is a promising solution due to the wide available bandwidth and global coverage [60]. In this section, we demonstrate 2 implementations of a very high linearity beamformer channel in the K SATCOM band implemented in GF8HP 0.12 μm SiGe BiCMOS process with a 5-bit phase and gain control. The implementation achieves a midband NF of 7.2 dB and an IIP3 $>$ 0 dBm with an OP1dB of $>$8 dBm with a 5-bit gain and phase control.

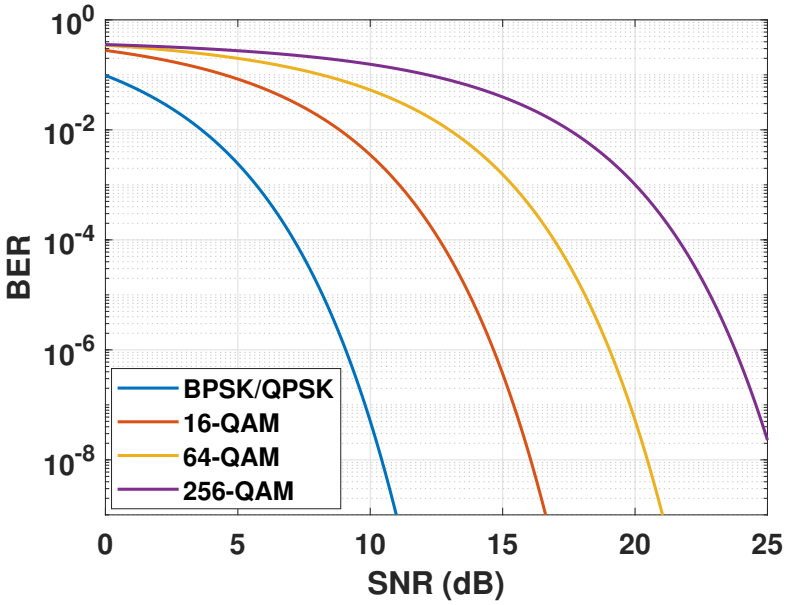


Figure 3.1: m-QAM modulation BER vs SNR.

In Figure 3.1, the minimum SNR needed for different m-QAM constellations is presented. Given the sensitivity and dynamic range definitions presented in the introductory section, we can calculate the SFDR of the receiver presented in this section.

$$Sensitivity = -174\frac{dBm}{Hz} + 10log(BW) + NF + SNR_{min}$$

$$SFDR(dB) = \frac{2(IIP3 + +174\frac{dBm}{Hz} - 10log(BW) - NF)}{3} - SNR_{min}$$

Table 3.1: High-Linearity Channel Spurious-Free Dynamic Range

Modulation	SNR_{min} @ **BER =** 10^{-4} **(dB)**	**SFDR** $(\frac{dB}{MHz})$
BPSK/QPSK	7.1	64.1
16-QAM	12.6	58.6
64-QAM	16.9	54.3
256-QAM	21.6	49.6

This table illustrates that the resented channel can achieve a SFDR from 50 to 65 dB per MHz of integrated bandwidth, leading to a state-of-the-art dynamic range performance.

3.2 Global Foundries 8HP Process

3.2.1 Back-End-Of-Line

The beamformer has been implemented in Global-Foundries' 0.12 μm SiGe BiCMOS 8HP Process (GF8HP). This process offers a 7-metal layer back-end that includes 3 top thick metal layers that can be used for the design of high-Q inductors and transmission lines and 4 thinner lower metals that can be used for low-frequency or digital routing and bias lines (Figure 3.2). A typical 50 Ω microstrip transmission line uses the MQ layer as RF ground providing 9.6 μm of signal line to ground distance. The process also integrates a MIM cap between the top 2 metals (LY-AM).

The process includes both a high f_t SiGe npn and a triple-well MOS device. The first will be used in all active stages of the design to utilize the high f_t/f_{max} performance and the second in all passive stages (phase shifters and attenuators) as a low insertion loss SPST.

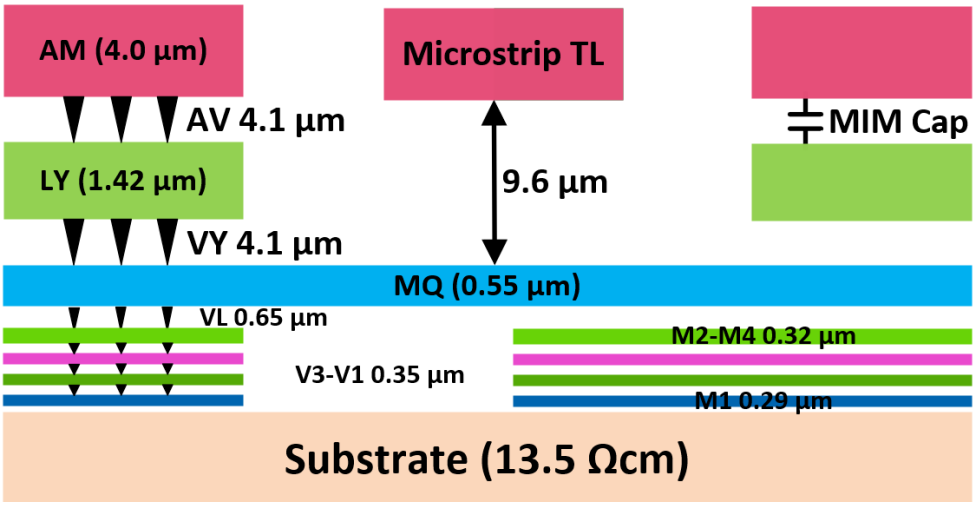
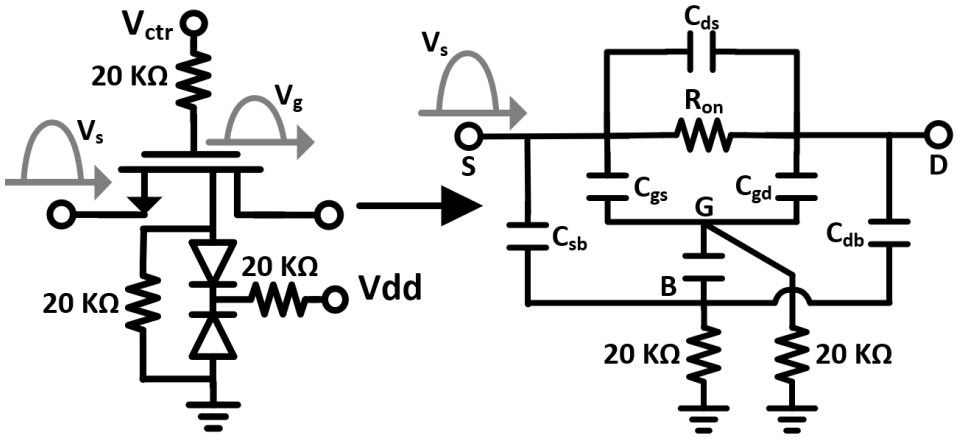


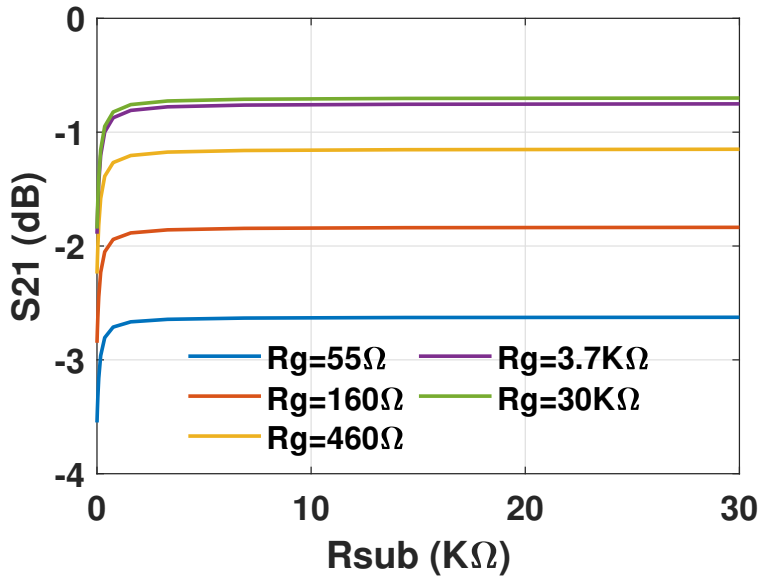
Figure 3.2: Back-end-of-line for the 0.12 μm GF8HP SiGe BiCMOS process.

3.2.2 MOS Triple-Well Device

The nmos triple-well device is the ideal candidate for the design of all the passive components of the channel. Particularly, the triple well device offers a design knob for insertion loss minimization by using external resistors to connect the p-well bulk and deep n-well to ground and V_{cc}, respectively (Figure 3.3a), in a bootstrapped fashion.



(a)



(b)

Figure 3.3: (a) Schematic of the triple-well device and the external resistors used to reduce the insertion loss. (b) Simulated insertion loss of the reference 100 μm triple-well nmos device.

For a square-law device operating in deep triode, the ON resistance can be quantified, to the first order, as:

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th} - V_{DS})}$$

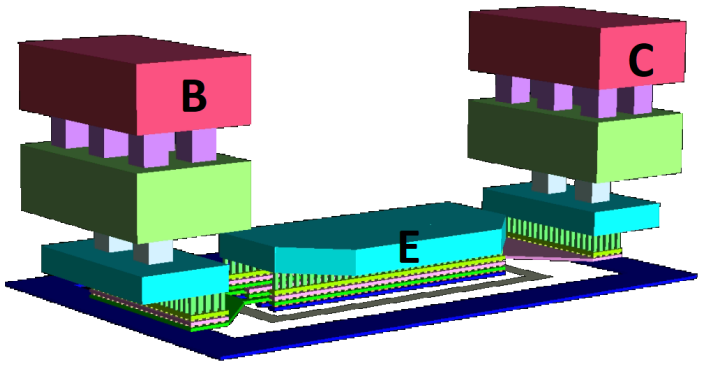
This entails that using a high-value resistance in series to the gate, bulk and deep n-well nodes will generate a high impedance to ground, allowing for a constant gate-source voltage across the RF swing. Based on simulation results, a resistor in the KΩ range achieves the insertion loss improvement. A 20 KΩ resistor was selected for this purpose and was used in all the SPSTs of the passive blocks (Figure 3.3b).

This improvement in the insertion loss performance of the unit SPST switch is very important for the system design. If the attenuation or phase shift functionality came at a very steep reference loss, achieving a high linearity system design would require a very power hungry design.

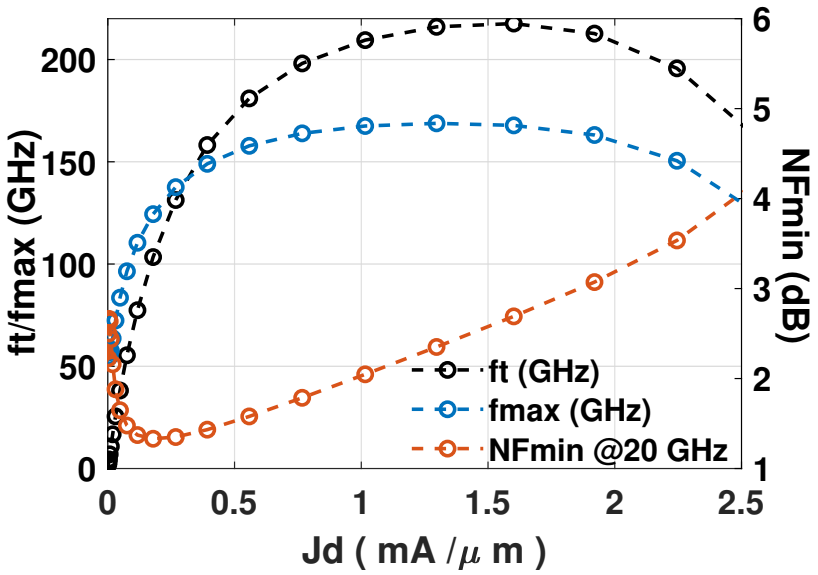
3.2.3 Bipolar Device

GF8HP process integrates a high performance npn device. For the design purposes of this work, the npn device was used in all amplifier designs as in the layout presented in Figure 3.4a. As expected, in Figure 3.4b the npn device peak f_t and f_{max} occur at a current density of 1.3-1.6 $\frac{mA}{\mu m}$, with peak values of 220/170 GHz, providing with sufficient intrinsic gain to work with at K-band. The NF_{min} performance of the device occurs at a bias current of 0.2-0.3 $\frac{mA}{\mu m}$.

All amplifier stages are cascode or pseudo-cascode. The layout of the common gate device is similar to the one presented for the common source, with a target to minimize the interconnection inductance.



(a)



(b)

Figure 3.4: (a) Layout of the npn device. (b) Simulated f_t, f_{max} and NF_{min} of a 13 μm npn device layout.

3.3 Common Leg Noise and Linearity Optimization

The target of the design is to simultaneously optimize the NF and IIP3 performance of the channel in order to maximize its dynamic range performance. To achieve this we need to examine the fundamentals of cascaded noise and IIP3 performance of noisy and non-linear cascaded sub-circuits.

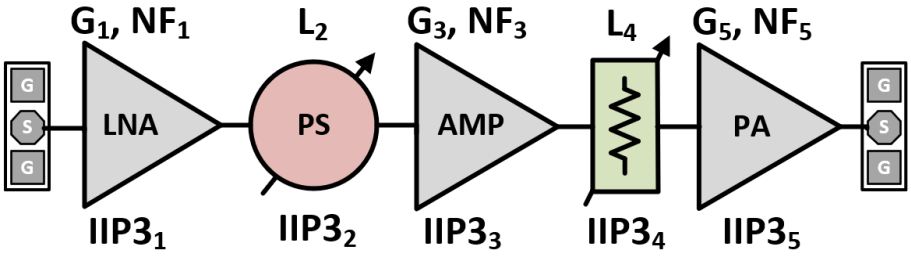


Figure 3.5: Noisy and non-linear beamformer channel.

3.3.1 Cascaded Noise Figure Optimization

A structure with cascaded noisy components Figure 3.5 will have a noise factor of:

$$F_{system} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 L_2} + \frac{F_4 - 1}{G_1 L_2 G_3} + \ldots$$

This indicates the dependence of the system noise figure from the first stages of the chain. However, it also indicates that in a cascaded system that involves lossy components along the signal path, it is critical to properly distribute the loss across the chain in order to compensate its effect on the noise figure.

3.3.2 Cascaded Linearity Optimization

A system of cascaded non-linear sub-circuits (Figure 3.5) will exhibit a cascaded IIP3 of:

$$IIP3_{system} = \frac{1}{\frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 L_2}{IIP3_3} + \frac{G_1 L_2 G_3}{IIP3_4} + \ldots}$$

The system level linearity is dominated by the latter stage. Overall, the preceeding stages need to be linear enough so as to drive the upcoming stages without introducing compression to the system. However, this fundamental target can lead to power greedy designs if the gain and loss distribution is not distributed wisely across the chain.

3.3.3 Optimal Architecture

In order to determine the optimal architecture for the K-band beamformer, we first need to determine the passive components loss. For a design that involves a 5-bit phase shifter and a 5-bit gain control of 15.5 dB in total, we need to determine the loss penalty that will be introduced in order to achieve the desired functionality (RMS gain and phase error).

Using the triple well device to create the SPST switch core and EM simulations for the needed inductors, we are able to determine the expected loss of the passive components. After simulations the overall loss that needs to be distributed across the channel is 18.3 dB (11.6 dB for the phase shifter and 6.7 dB for the reference state of the attenuator).

Using this number as a reference, along with our desired specifications of > 0 dBm IIP3, NF of 6 dB and $OP_{1dB} > 10$ dBm for an overall gain of 20 dB, we present two possible implementations.

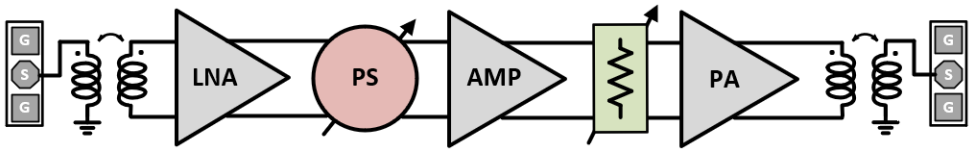


Figure 3.6: Case study 1

As seen in (Figure 3.6), the first configuration involves a 5-bit phase shifter and a 5-bit attenuator with a driver amplifier in between. Given that, after simulations, the loss of the phase shifter is significantly higher than the attenuator, the placement shown in this topology will compromise the cascaded noise figure of the system, as it will be impossible to make a very high gain LNA to compensate the loss without severely limiting the linearity of the LNA, as we will need to operate at a relatively low bias point for NF considerations.

As seen in (Figure 3.7), the second topology places the attenuator first and the phase shifter before the PA. This configuration relaxes the specification for the gain of the LNA since the attenuator loss is significantly lower that the phase shifter. However, the line amplifier needs to

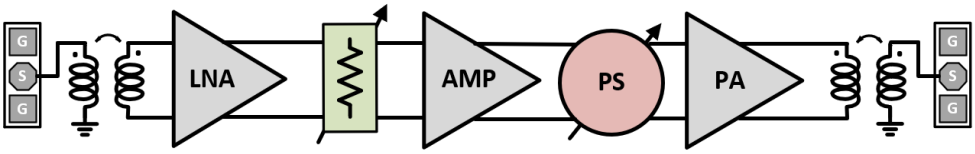


Figure 3.7: Case study 2

be able to drive the PA in addition to the phase shifter loss in order not to introduce compression to the cascaded system, which will lead to a very power hungry stage.

The previous analysis indicated that we are incentivized to explore configurations with multiple line amplifiers in order to break the trade-off between the NF and linearity and the strain created either onto the LNA design or onto the line amplifier design.

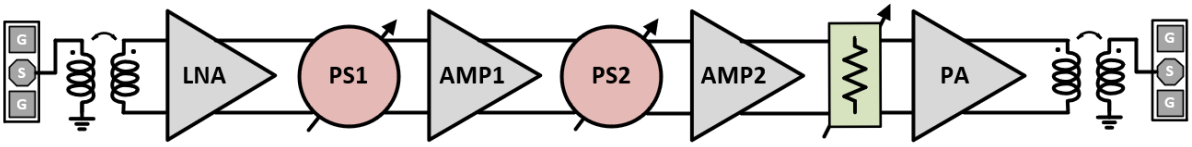


Figure 3.8: Case study 3 - Multiple line amplifiers

As seen in Figure 3.8, by using 2 line amplifiers and breaking the loss involved with the passive phase shifters onto two different blocks, we are able to distribute the loss and gain in a more uniform way across the chain leading to relaxed specifications for each block.

In particular, the phase shifter loss is around 6 dB per stage. This leads to an LNA design that can balance both a relatively low NF along with good linearity performance. On the output side, the second line amplifier will need to drive the smaller loss of the attenuator plus the needed power to compress the PA, which helps significantly reduce its power consumption.

Another design parameter, is the fully differential implementation selected. EM related considerations lead to this design choice which leads to the introduction of a input balun that directly affects the system's NF. On the other hand, RF ground definition problems are severely alleviated, reducing the risk for discrepancies between simulated and measured results.

In conclusion, the NF performance is directly affected by the input balun loss and the LNA NF performance. The LNA gain is not fully optimized in order not to reduce its IP1dB.

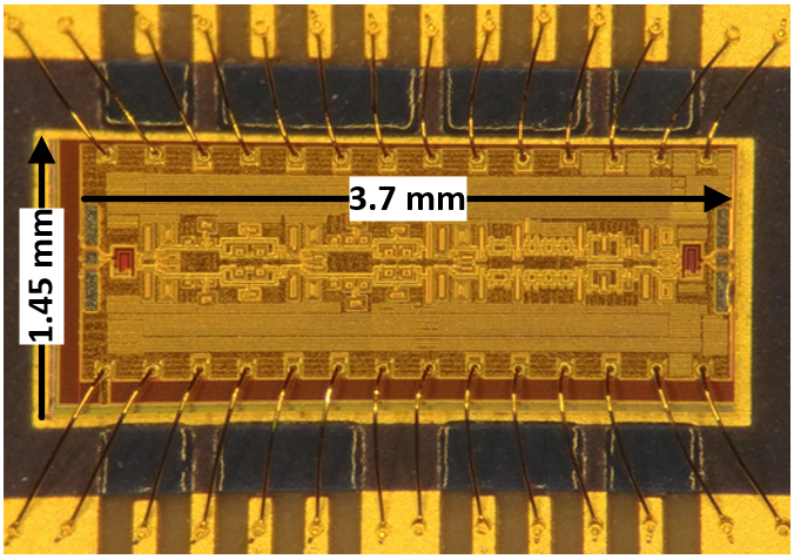


Figure 3.9: High linearity channel wirebond implementation.

On the other hand, the linearity will be heavily dominated by the PA's compression assuming that all other amplifiers have been designed to operate sufficiently at back-off in order to provide linear power to the succeeding stage. However, the last point cannot be fully satisfied due to the trade-off between the power consumption and the compression point that forces us to introduce some compression before the PA.

The implemented chip is shown in Figure 3.9, along with the wirebonds around it that end to the DC board that allows for the biasing and SPI control of the phase and gain states.

3.4 Passive Components Design

For the passive components design the triple well device will be utilized, in order to optimize the SPST switch insertion loss. All phase shifter blocks are based on conventional LC structures with high pass - low pass networks that will introduce the necessary relative phase shift. The attenuators will be based on phase corrected pi-type structures.

3.4.1 Pi-Type Attenuators

For the attenuator cells, a pi-type resistive matched attenuator structure was used. The RF signal will either propagate from the SPST switch or from the resistive attenuator strucure in parallel to the SPST (Figure 3.10).

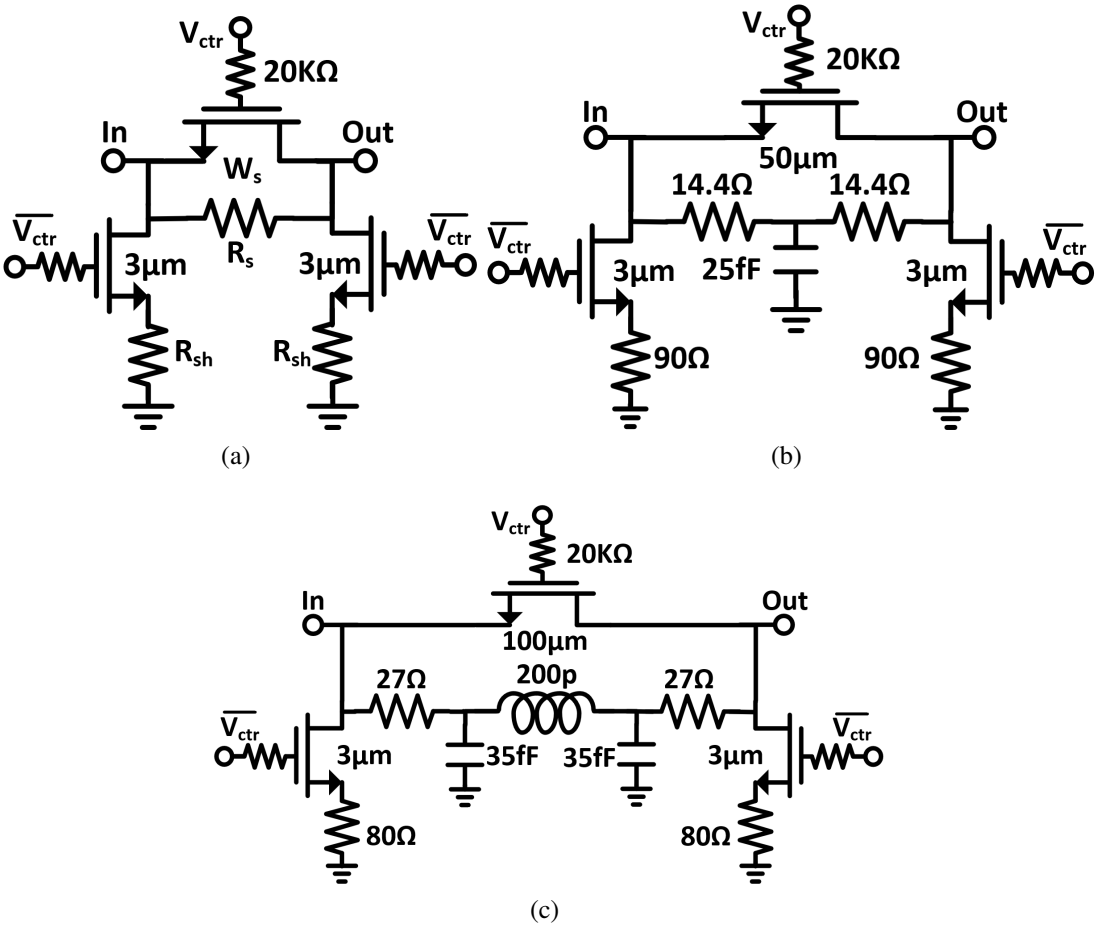


Figure 3.10: (a-c.) 0.5-1-2, 4 and 8 dB attenuator cells.

Table 3.2: 0.5,1 and 2-dB cells schematic component values

Atten. (dB)	W_s (μm)	R_s (Ω)	R_{sh} (KΩ)
0.5	40	4	1.1
1	50	7.5	0.76
2	40	14.5	0.19

The design challenge with the pi-type structures lies in the phase imbalance introduced between the reference and attenuation states, which deteriorates as the desired attenuation becomes higher. This issue will give rise to significant system level degradation if it is not addressed in circuit level.

The fundamental reason is that the attenuation is used to enable tapering across the elements of a phased array in order to reduce the sidelobe levels. If the phase imbalance issue is not addressed, when the system employs a deep taper along with a specific phase setting that will result in a particular scan angle, the phase imbalance due to the tapering will introduce unwanted phase distortion at the edge elements leading to significant degradation in the angular resolution of the system. Typically, the target is to make the gain related phase imbalance to be < 0.5 LSB, in this case $6°$, in order to assure the monotonical performance of the phase shifter even under heavy attenuation.

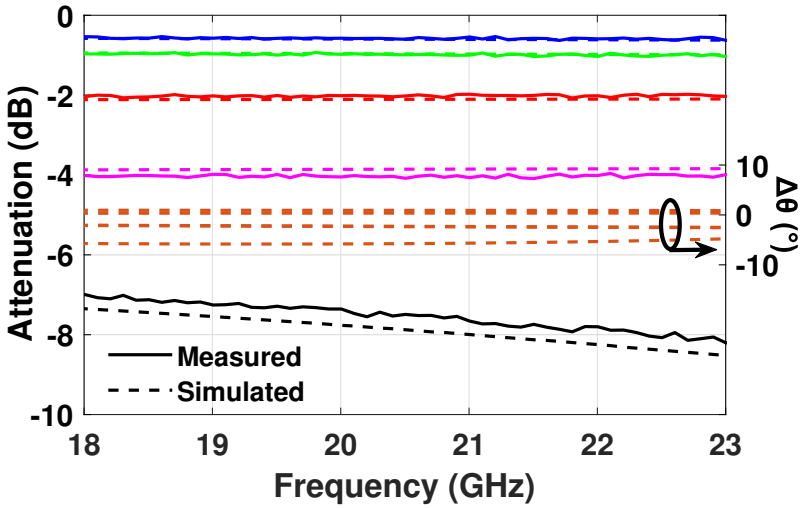


Figure 3.11: (a) Measured and simulated gain steps and phase variation in breakout attenuator cells.

To alleviate this problem, the presented 4 and 8 dB attenuator cells include low-pass phase correction networks in the attenuation state, leading to a significant improvement in the overall system phase variation over all the gain states ($< \pm 5°$), with the cost of increased reference loss (Figure 3.11) [61]- [62]- [63].

3.4.2 LC-Type Phase Shifters

For the phase shifter cells, various topologies are used in order to achieve all goals, i.e. low and balanced insertion loss between the reference and phase-shift state, good impedance matching and flat phase difference across the frequency band of interest.

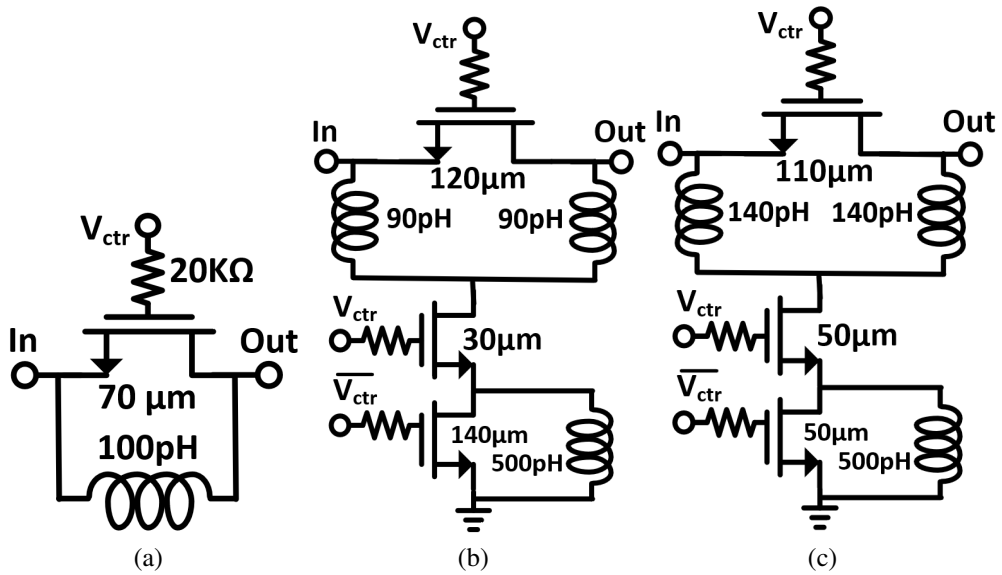
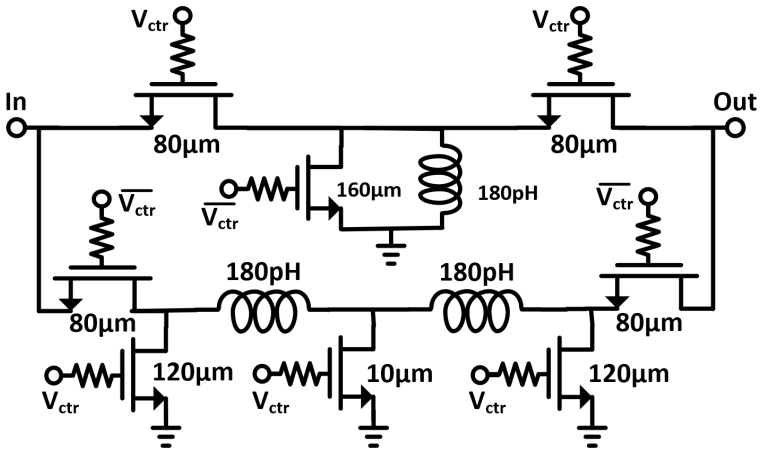


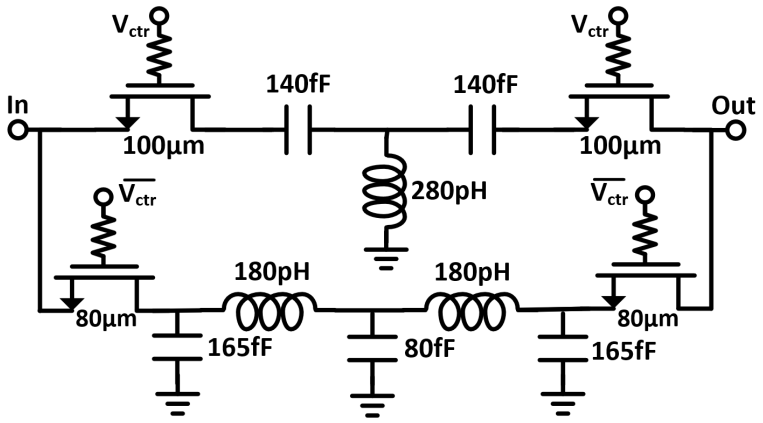
Figure 3.12: (a-e) 11, 22 and 45 degree phase shifter cells [64], [67].

For the lower phase shift cells (11°, 22° and 45°) an SPST switch in shunt with a phase introducing network is used (Figure 3.12). For the 11° cell (Figure 3.12a), a simple inductor is used to resonate the off-capacitance of the SPST switch and introduce the phase shift. However, this structure cannot be used for high relative phase shift due to poor relative phase flatness versus frequency.

For this reason more complex shunt structures are used, for all higher relative phase shift cells (Figure 3.12-Figure 3.13). These structures create a high-pass/low pass reference and phase shift path leading to increased phase flatness versus frequency since both states present a frequency dependent phase response leading to relatively constant relative phase shift versus frequency.



(a)

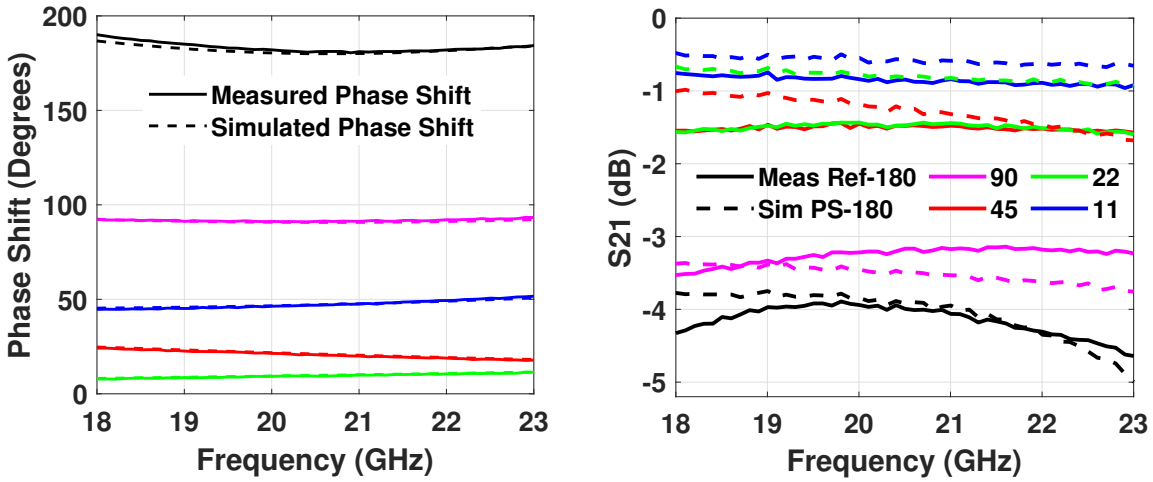


(b)

Figure 3.13: (a-b) 90 and 180 degree phase shifter cells [64], [67].

Another design aspect from a circuit perspective is that the reference and phase shift paths need to introduce similar insertion losses (and as small as possible). This is an extra parameter for the design that needs to be carefully examined in order to optimize the beamformer's RMS gain error performance, which should ideally be less than half the least significant bit of the attenuator, in order to maintain a monotonical gain decrease from the attenuator.

Figure 3.14a shows excellent agreement between the simulated and measured phase response, while Figure 3.14b shows good agreement for the insertion loss response (relative insertion loss between simulated and measured reference and phase shift state) as well, with the smaller phase shift cells suffering more, since the reference state only involves an SPST switch.



(a) (b)

Figure 3.14: (a) Measured vs simulated phase shift. (b) Measured vs simulated loss in breakout phase shifter test cells.

The overall reference state loss for all the passive components is presented in Figure 3.15, illustrating good agreement between measurements and simulations with the small discrepancies related to the modeling of the SPST insertion loss which compounds as more SPSTs are involved in the signal path. On another note, the attenuator insertion loss versus frequency is naturally degrading because of the effect of the shunt parasitic capacitance. This needs to be compensated through the active design to maintain a 3-dB bandwidth from 19-22 GHz.

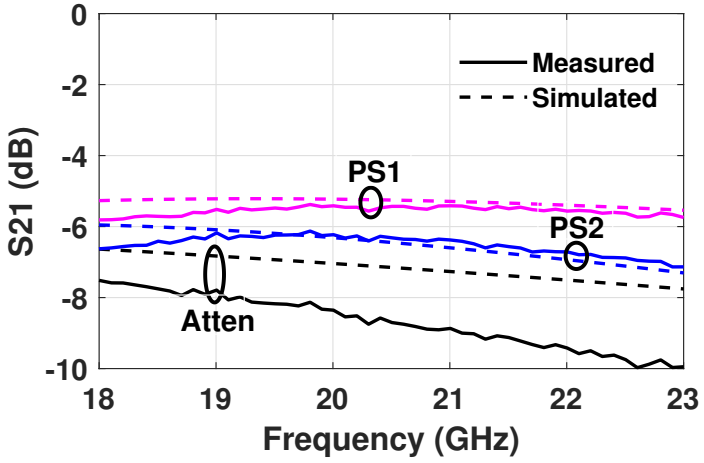


Figure 3.15: (a) Passive components measured vs simulated refernce state insertion loss.

3.5 Active Components Design

3.5.1 LNA and Line Amplifier Design

For the amplifiers, two different approaches were used. For the LNA and the line amplifier, a cascode structure with a current mirror at the tail was used to externally control the current density and provide some flexibility to control the gain of each stage Figure 3.16.

From a schematic perspective, a differential cascode structure with inductive degeneration was selected to help with the input impedance matching. The cascode structure was necessary to boost the gain and improve the reverse isolation. Finally, intentional de-Q of the output matching network was used to increase the 3-dB bandwidth of each stage.

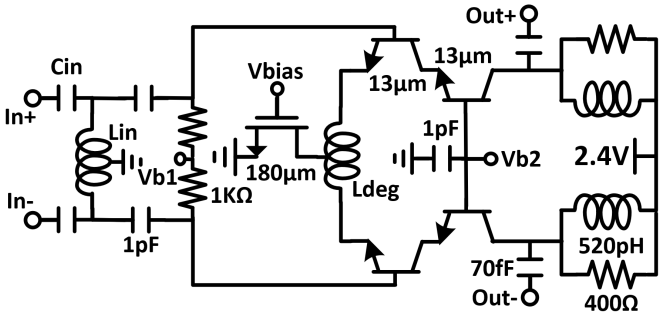


Figure 3.16: (a) LNA and line amplifier schematic.

Table 3.3: LNA and Line Amplifier Component Values

Amplifier (dB)	C_{in} (fF)	L_{in} (pH)	L_{deg} (pH)
LNA	140	800	200
Amp1	90	900	540

The inductive degeneration, other than the advantages if offers with regard to the creation of a controllable real impedance at the device input, was also used as a linearization knob. Increasing the degeneration inductance for the same RF input swing, reduces the effective swing across the base and emitter terminals, leading to an increase of the $IP1_{dB}$ point of operation of each stage.

3.5.2 Driver Amp and PA Design

For the the design of the driver amplifier and the PA the current mirror device was removed in order to increase the voltage headroom available for the RF voltage swing at the common gate device collector, while the gate resistance is reduced in order to allow for the amplifiers to increase their base bias current as needed to self-bias when getting close to the class-AB regime.

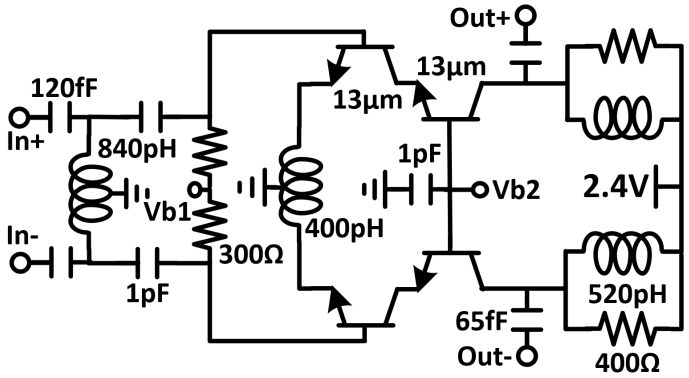


Figure 3.17: Driver amplifier schematic.

In the PA design, the de-Q resistor is removed in order to avoid the RF current being wasted onto the resistor, thus improving both the power and efficiency of the PA. The PA's output impedance was co-optimized along with the output balun. Also, the power amplifier small-signal gain was tuned higher than the center frequency on order to partially compensate for the attenuator gain drift versus frequency.

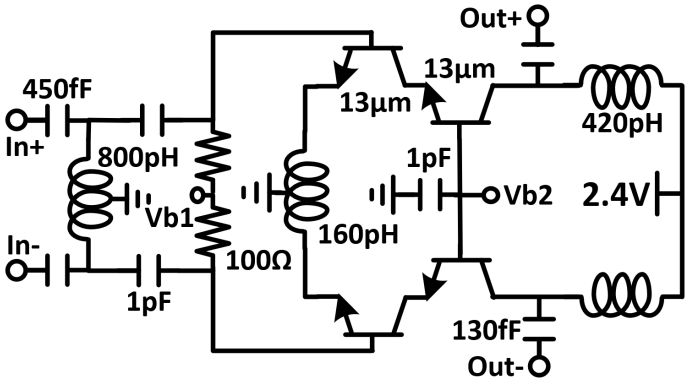
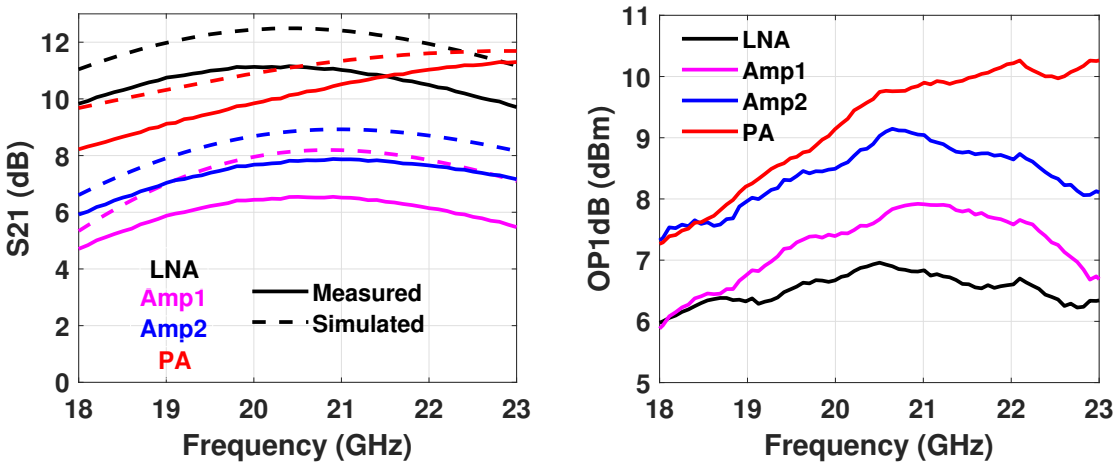


Figure 3.18: PA schematic.

The simulated and measured results of the small-signal and large signal for each ampifier are presented. The results present good agreement in the center frequency of each amplifier with a small gain reduction in the measurements. The design intention was to have sufficient gain on the LNA, while using enough gain across the following amplifiers to maintain the system linearity.



(a) (b)

Figure 3.19: (a) Measured S_{21} of the 4 amplifiers. (b) Measured OP_{1dB} of the 4 amplifiers.

3.6 Beamformer Channel Measurements

3.6.1 Wirebond Channel Measurements

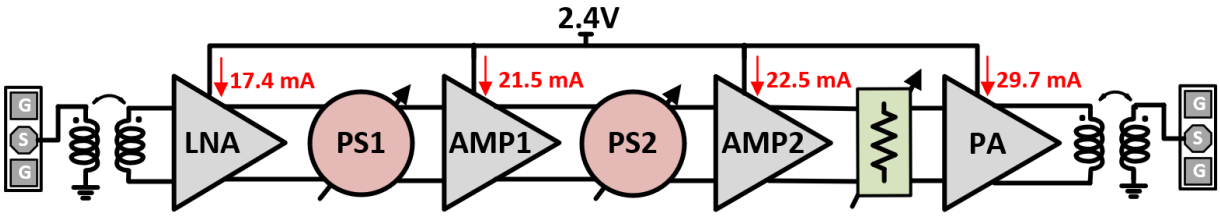
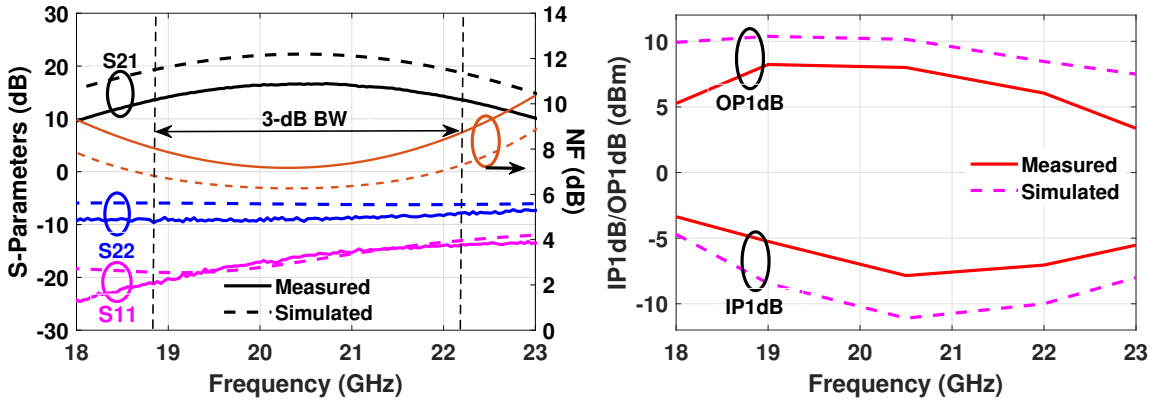


Figure 3.20: Wirebond channel bias point for small signal-measurements.

In (Figure 3.21a), the measurement results of the wirebonded implementation of the beamformer are presented. The S_{21} is centered at 20.5 GHz while the 3-dB bandwidth is identical

to the simulated (18.8 - 22.2 GHz). The drop in the simulated S_{21} is due to the measured discrepancy in the S21 of the amplifiers ant the attenuator cell loss.

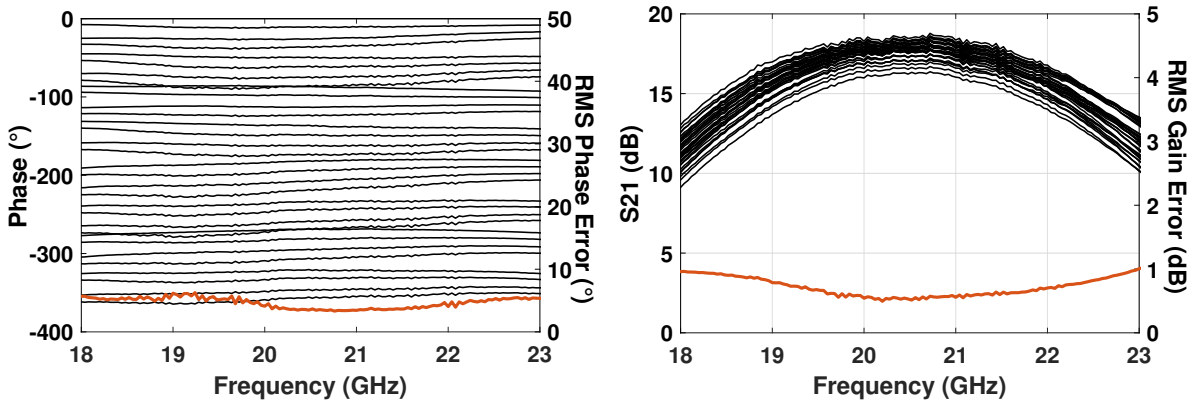
The NF performance is slightly worse due to the increased loss of the input balun and of PS1 right after the LNA, which contributes to the system NF since the LNA gain is also slightly lower than expected. The input compression point and the output power at compression are close to the simulated with their discrepancies being attributed to the increased loss of the attenuator stage. This directly affects the output power at compression since, for the same bias points, the driver amplifier will not be able to linearly drive the PA. On the other hand, this extra loss reduces the gain and thus increases the input compression point.



(a) (b)

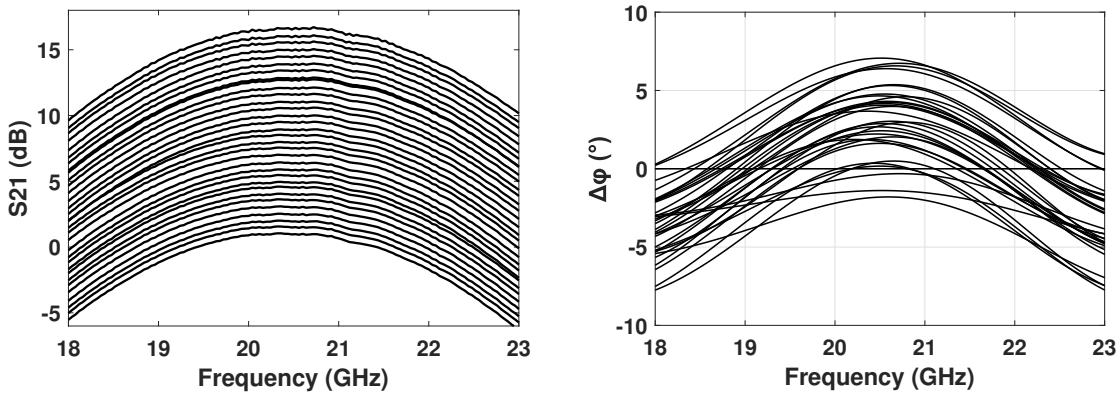
Figure 3.21: (a) Measured and simulated S-parameters and NF of the channel. (b)Measured and simulated IP_{1dB} and OP_{1dB} of the channel for a universal V_{cc}=2.4 V.

The beamformer incorporates 5 bits of gain and phase control with a total attenuation of 15.5 dB with a 0.5 dB step and a phase resolution of 11 degrees. In the system context, the gain variation between all 32 gain degrees, showing the effect of the employed phase balancing scheme used in the attenuator design. All the presented results correspond to a uniform Vcc of 2.4V and a power consumption of 240 mW.



(a) (b)

Figure 3.22: (a) Measured phase states and RMS phase error for all 32 states. (b) Measured gain variation for all 32 states and RMS gain error.



(a) (b)

Figure 3.23: (a) Measured gain states. (b) Measured phase variation for all 323 gain states.

3.6.2 C4/ Flip-Chip Channel Measurements

The beamformer channel was also implemented using the C4/flip-chip technique. For this purpose 50 μm metal balls are positioned in the specified openings of the control and RF pads (Figure 3.24). In order to model the insertion of the pads and the PCB interface, the stack-up used for the EM simulations was modified, in order to include the extra metals on top of the existing passivation layers. Due to this modification a small offset in the center frequency was introduced in the simulations of the channel, leading to minor redesign to meet the specifications.

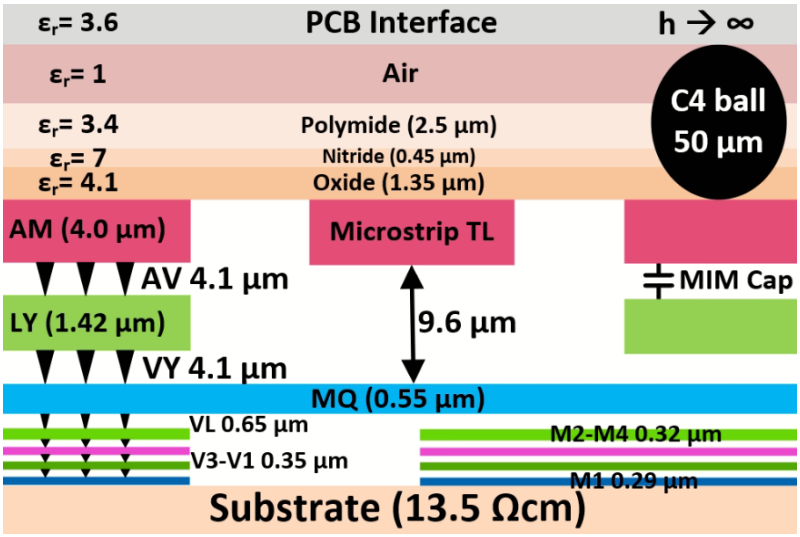


Figure 3.24: GF8HP stack-up modification for C4 ball incorporation.

The implemented connectorized board and flip chip are illustrated in Figure 3.25. The flip-chip input and output GSG pads are connected to the 2.92 mm RF connectors through a 50 Ω coplanar waveguide transmission line on the PCB. The RF connector and the input and output GSG pads will be used as the reference planes for all the connectorized measurements.

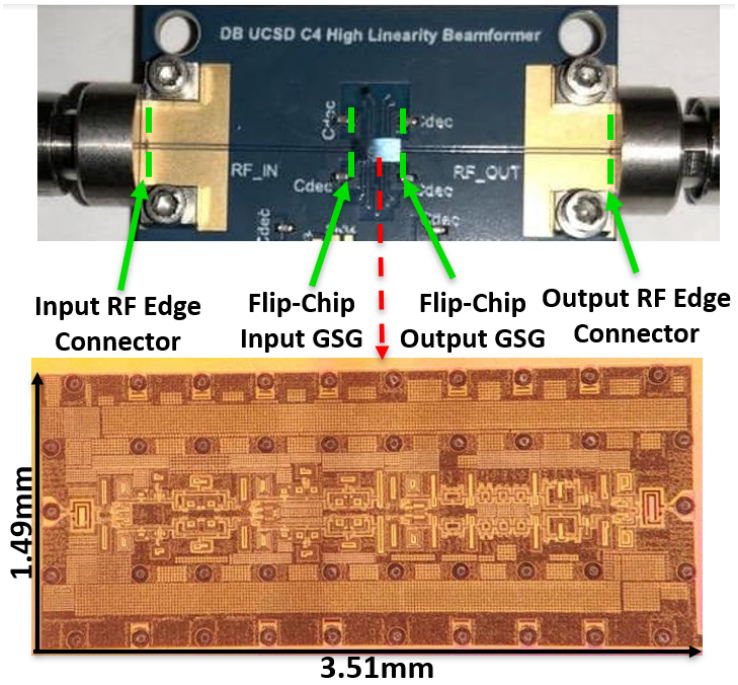


Figure 3.25: C4 flip chip channel and RF connectorized board.

The C4 small signal measurements are in good agreement with the wirebond results. The mid-band gain is 16 dB, the mid-band NF is 7 dB as seen in Figure 3.26.

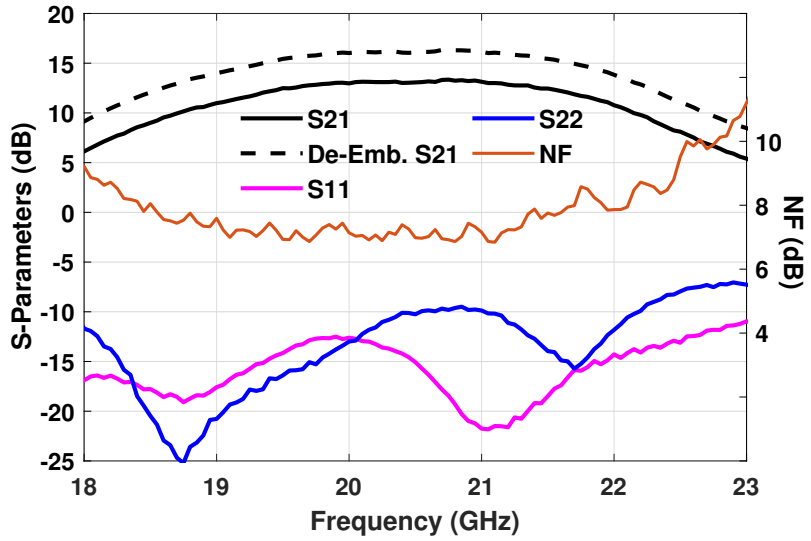


Figure 3.26: C4 conntectorized board measured S-parameters and NF.

The large signal measurements are also in good agreement with the wirebond channel (Figure 3.27). The input compression point is at -8 dBm and the OP_{1dB} 7 dBm, while the OP_{sat} is 8 dBm, defined at the IP_{1dB} + 3dB point.

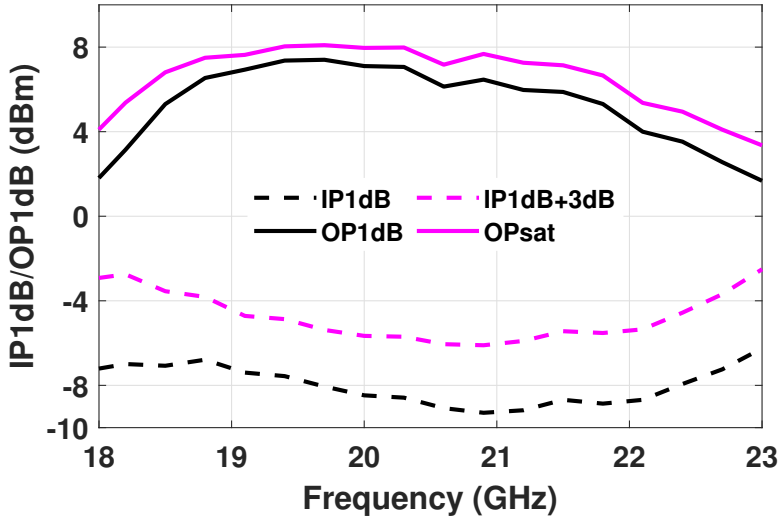


Figure 3.27: C4 channel large signal measurements.

The expected IIP_3 is verified by the measurements presented in Figure 3.28. Typically we expect the IIP_3 level to be 9 - 10 dB higher than IP_{1dB}, which is validated through measurements.

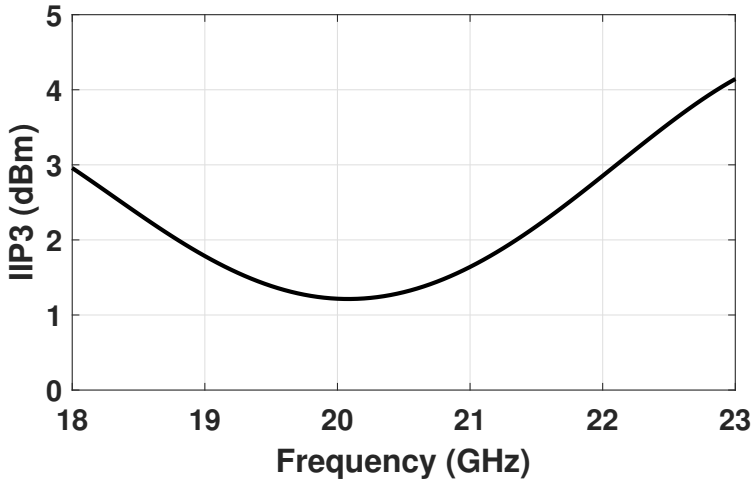
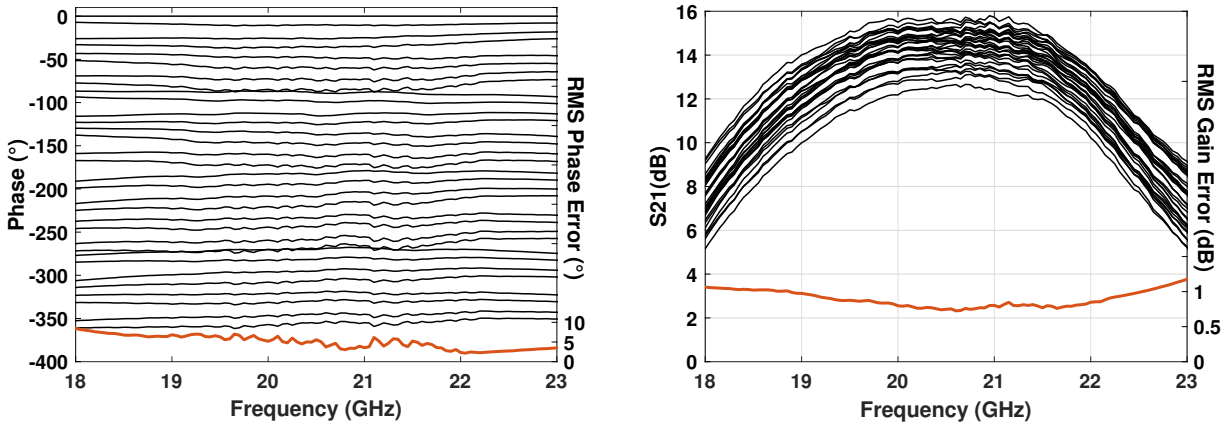


Figure 3.28: C4 channel IIP_3 measurements

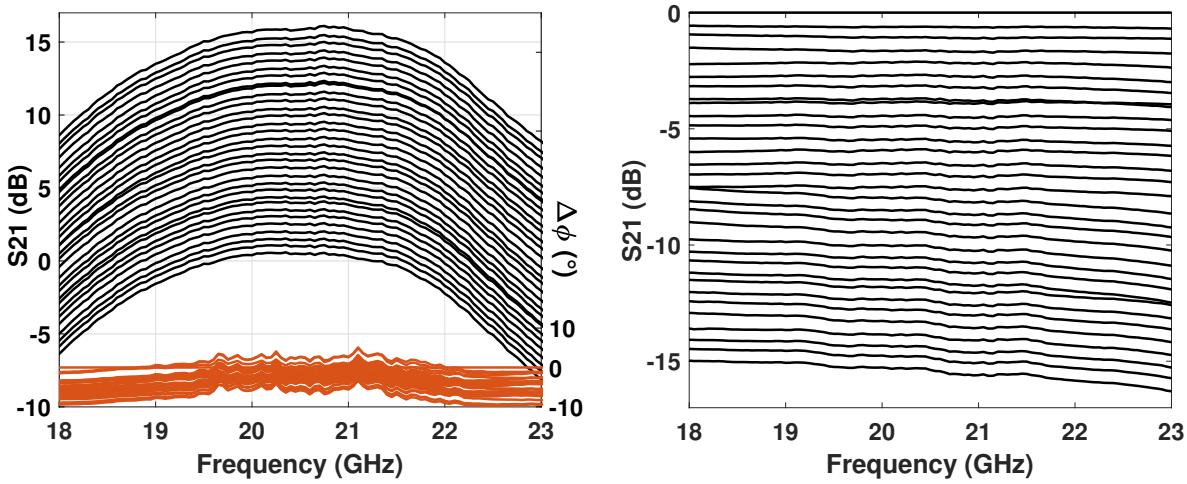
The phase shifter performance is illustrated in Figure 3.29. THe RMS phase error is less than half the least siginificant bit (6°), leading to a monotonical progressive phase step. The RMS gain error performance is also similar to the wirebond channel, illustrating that the redesign for the C4 ball integration was successful.



(a) (b)

Figure 3.29: (a) Phase states and RMS phase error. (b) S_{21} variation vs phase states.

The gain state performance is illustrated in Figure 3.30., where the results are similar to the wirebond case with a small change in the mid-band gain (16 dB for the C4 channel).



(a) (b)

Figure 3.30: (a) Absolute gain states and phase variation. (b) Relative gain states.

3.7 Conclusion

In this work, a high linearity and low NF beamformer with 5-bit of gain (15.5 dB total attenuation) and 5-bit of phase control is presented and that can be used for both receive and transmit applications. The high IIP3 in addition to the relatively low NF of the channel leads to a state of the art dynamic range performance. The channel functionality is illustrated in a wirebond and flip-chip implementation.

A comparison of the C4 chip performance with other state of the art dynamic range implementations is presented in Table 3.4. This work illustrates one of the highest dynamic range performances reported in literature along with a OPsat of 8 dBm.

The implementations compared in this section correspond to single-leg Tx/Rx implementations ([67]- [68]- [69]). Other implementations, that involve RF SPDTs and separate

Table 3.4: High linearity beamformer comparsion with the state-of-the-art

Parameter	**This work**		[67]		[68]	[69]
Technology	**0.12 µm SiGe BiCMOS**		45nm CMOS SOI		0.13 µm CMOS	45nm CMOS SOI
RF Freq. (GHz)	**18.8-22**		24-30		9-10	26-28
Operation Mode	**RX**	**TX**	RX	TX	RX	RX
Gain (dB)	**16.2**	**16.2**	16	16.5	11.5	12
NF (dB)	**7.2**	**-**	3.7	-	3	>4
IP_{1dB} **(dBm)**	**-8.2**	**-**	-15	-	-15	-8
IIP3 (dBm)	>1	**-**	-	-	-	0
OP_{1dB} **(dBm)**	**-**	**7**	-	8	3	-
OP_{sat} **(dBm)**	**-**	**8**	-	-	-	-
SFDR (dB)	**71.1**	-	68.8	-	64.7	73
RMS Gain Error (dB)	**0.7**		<0.8		<0.6	-
RMS Phase Error (°)	**<6**		<4		-	4
P_{dc} **(mW)**	**200**		54	100	19	42
Area (mm^2)	**2.46***		**3***		1.89*	1.75

optimization of the NF and OP1dB ([65]- [66]) will not be used for comparison purposes.

3.8 Acknowledgment

The authors would like to thank FirstRF and Global Foundry for the chip fabrication, Integrand Software, Inc., for access to the EMX electromagnetic simulator.

Chapter 3, in full, is being prepared to be submitted for publication of the material as it may appear in: D. Baltimas, Hyunchul Chung and G. M. Rebeiz, "K-Band SiGe BiCMOS High Linearity T/R Beamformer Channel with >0 dBm IIP3 and <7.2 dB NF", in *IEEE Microwave and Wireless Component Letters*. The dissertation author was the primary investigator and author of this paper.

Chapter 4

A 132-142 GHz RF Beamforming Phased Array Receiver Channel with 7 dB NF in 45nm RFSOI

4.1 Introduction

Advancements in millimeter-wave systems at $>$ 100 GHz range have provided a potential solution that enables ultra-high-data rates for short-range communication links [70]- [77]. Systems designed at this frequency range are excellent candidates to meet the ever-increasing demand for data, due to the wide unlicenced frequency bands with little to no interference with no limitations to channel capacity.

In order to compensate for the increased path loss at millimeter-wave bands, particularly at $>$ 100 GHz, phased-array systems need to be employed in both the transmit and receive end, in order to increase the equivalent isotropic radiated power (EIRP) and antenna gain, while providing electronic scanning capabilities.

In order to design high performance phased arrays at 140 GHz the architecture exploration

of the beamforming architectures to determine the best candidate is crucial. There are several potential candidates for D-band beamformer implementations, each with its advantages and drawbacks.

First, IF beamforming is a possible candidate (Figure 4.1). The integration of the beamforming functionality at a convenient IF frequency significantly reduces the beamforming circuit complexity and ensures very competitive RMS phase and gain performance. However, the system will employ one mixer and LO driver per channel, leading to increased layout complexity for LO signal distribution and symmetry, since the passive mixer gain will heavily depend on the LO driver level. The design complexity also involves the development of a high gain and low NF D-band LNA.

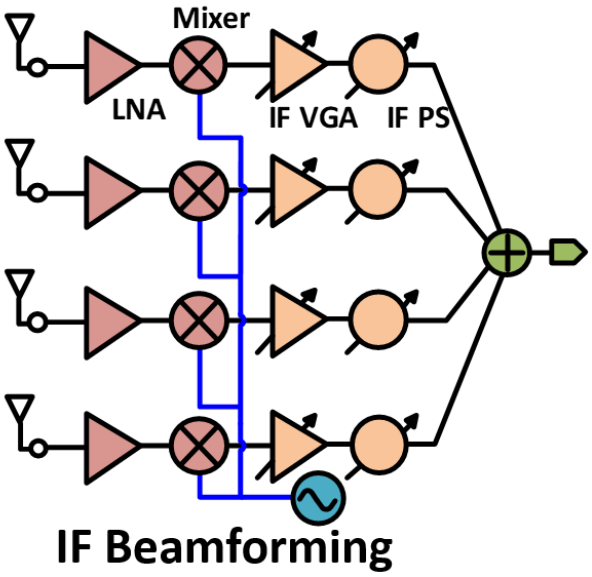


Figure 4.1: D-band IF beamforming architecture.

Second, digital beamforming is another potential candidate (Figure 4.2). This architecture also involves one mixer per channel and has the inherent disadvantage of requiring very high speed ADC per channel, making the scalability of this topology challenging due to power considerations.

Finally, the candidate that will be examined in this work is the full RF beamforming architecture (Figure 4.3). In this approach, the beamforming functionality is fully integrated in

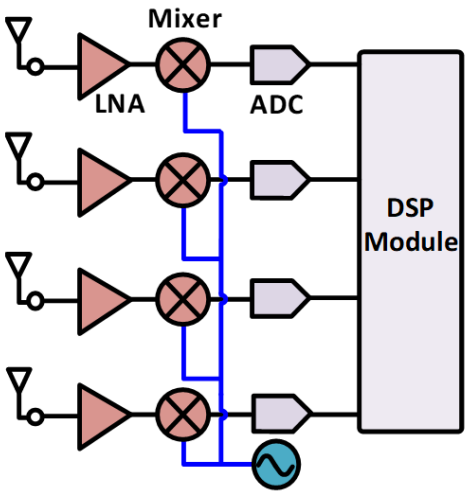


Figure 4.2: D-band digital beamforming architecture.

D-band, increasing the design and layout challenges for the phase shifter and VGA/attenuator. However, the design only involves one mixer solving the LO distribution issue.

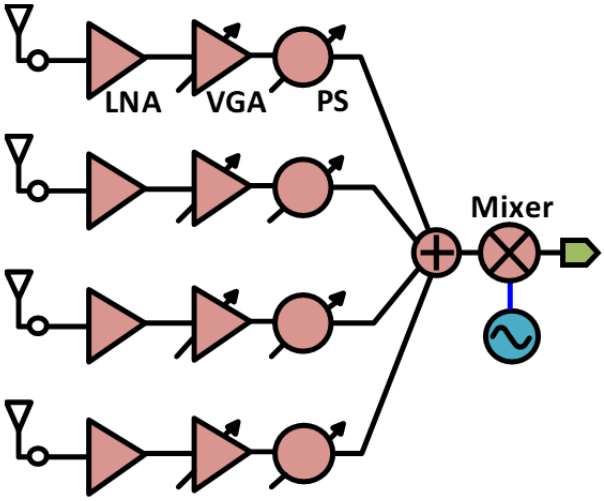


Figure 4.3: D-band RF beamforming architecture.

Our target in this work is to develop a full-RF D-band beamformer with 4-bit of phase and 3-bit of gain control that will have a comparable power consumption with its IF beamforming competitotrs. This will indicate that the full RF integration of the beamformer at D-band is a viable design option.

4.1.1 Global Foundries 45nm RFSOI Process

The full RF beamforming phased-array receive channel is designed in GlobalFoundries 45nm RFSOI process (Figure 4.4). This process has three ultra-thick metals (LD = 4.1 µm, OB and OA=3 µm), in which all inductors and transmission lines are implemented for reduced loss at 140 GHz.

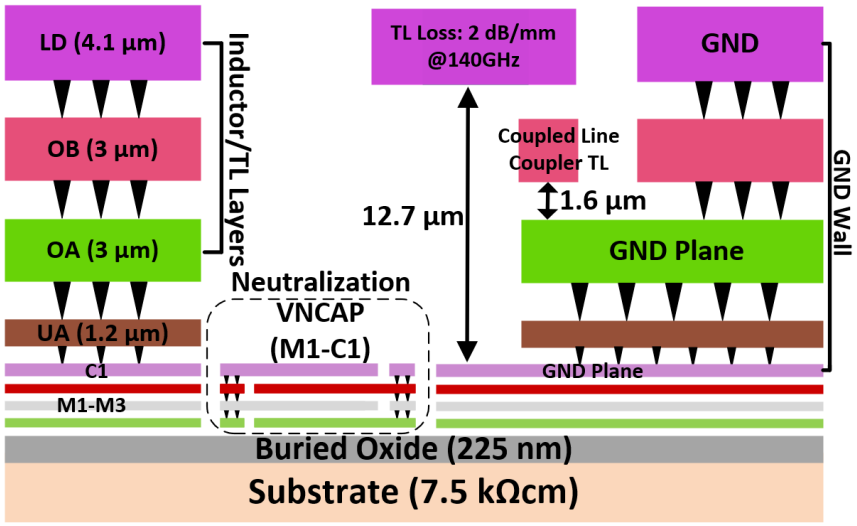
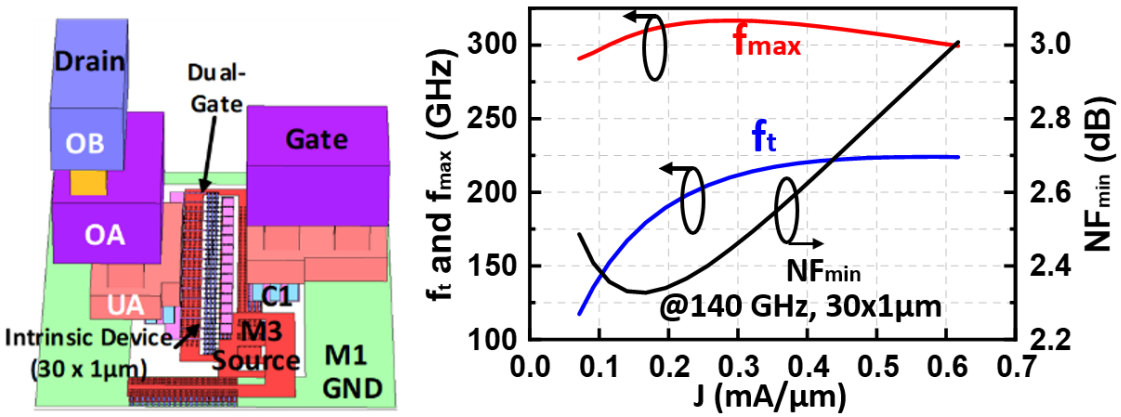


Figure 4.4: 45RFSOI back-end-of-line.

The floating-body RF NFET is selected for the design of the receiver, which provides a NF_{min} of 2.4 dB at 140 GHz at bias current density of J = 0.17 $\frac{mA}{\mu m}$ (used in the LNA design) while an increased current density of 0.2 - 0.25 $\frac{mA}{\mu m}$ is used for optimal ft/fmax performance in the phase shifter (Figure 4.5b).

A double-gate contact with high density poly-M1 vias is employed to reduce the gate resistance and a relaxed-pitch layout is chosen (Figure 4.5a) to reduce the parasitic capacitance [78]. A vertical natural capacitor (vncap) is provided and realized using metal fingers in a stacked fashion (bottom four metal layers (M1, M2, M3 and C1) [70].

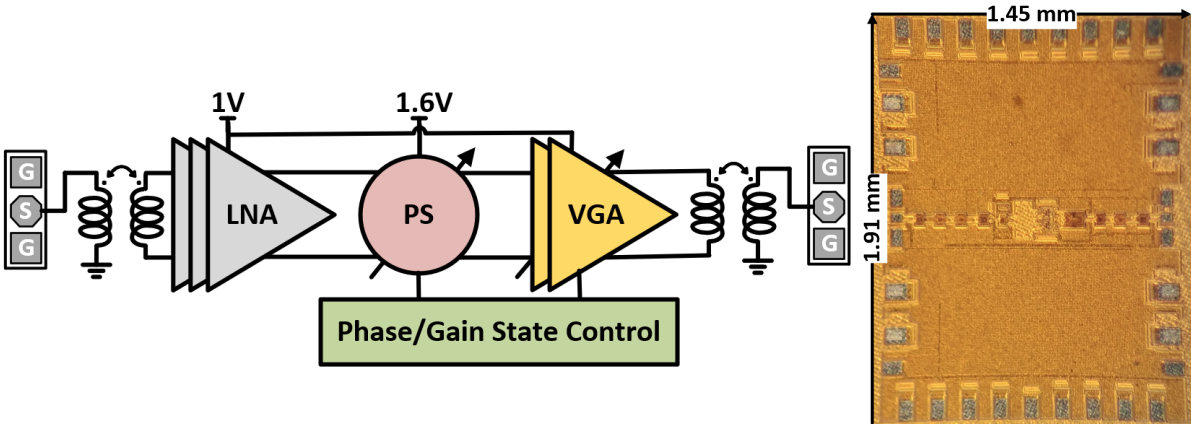


(a) (b)

Figure 4.5: (a) Reference floating body device layout. (b) Device characterization.

4.2 Full-RF Beamformer Receive Channel Architecture

The full RF beamformer phased-array receiver channel is comprised of a 3-stage transformer coupled LNA, a gilbert-cell based active phase shifter utilizing a passive coupled line I/Q generator along with a 2-stage transformer coupled VGA (Figure 4.6a). The design does not include SPI control leading to a large number of pads needed for its control. The implemented chip (Figure 4.6b), has an area of 2.77 μm^2.



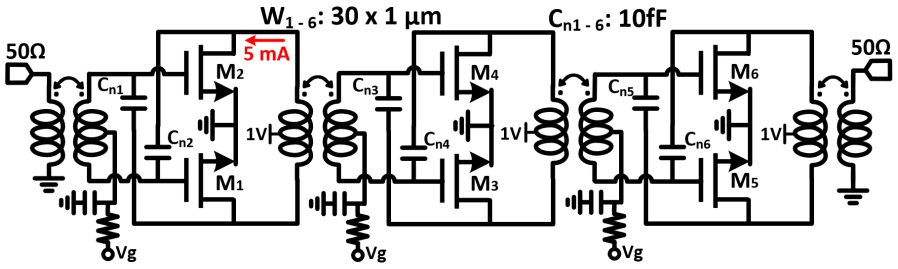
(a) (b)

Figure 4.6: (a) Proposed D-band receiver channel block diagram. (b) Implemented channel die microphotograph.

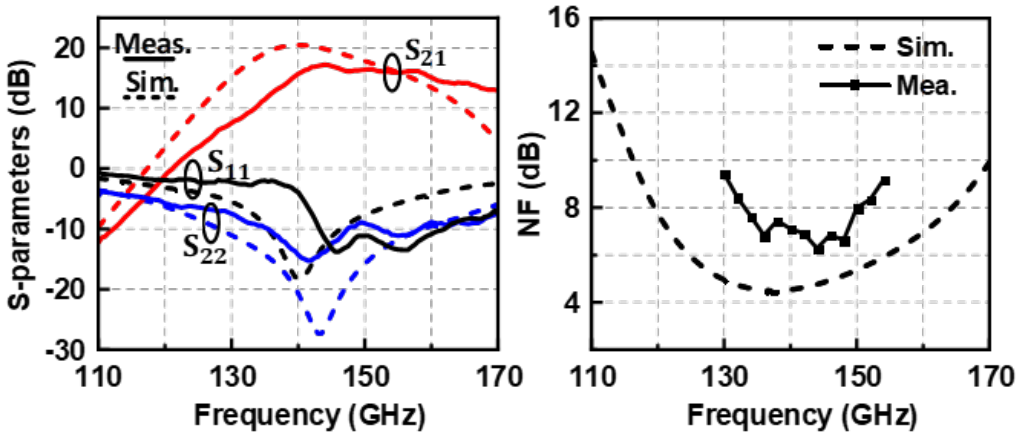
The channel is implemented in a fully-differential configuration in order to minimize the RF ground reference definition problem, particularly at 140 GHz. This steers part of the design complexity onto the design of 140 GHz balanced baluns.

4.3 D-Band LNA Design

A 3-stage fully differential transformer coupled LNA using cross-coupled pairs with neutralization capacitors to increase the maximum available gain (MAG) that has been presented in [70], is used. The neutralization uses vertical natural capacitors (vncap) with M3 - C1 layers (Figure 4.5a). 30x1 µm (30 fingers with 1 µm finger width) double-contact relaxed-pitch transistor pairs at bias condition of J = 0.17 $\frac{mA}{\mu m}$ are used for close noise/gain matching, low NF_{min} and high f_{max}.



(a)



(b)

Figure 4.7: (a) Transformer coupled LNA schematic. (b) LNA small signal measurement and simulation.

Figure 4.7 presents the measurement results of the design, which showcase a D-band LNA with 18 dB of gain at 140 GHz and 6.5 dB of NF. The measured results show a frequency of 3% due to EM modeling of the device and the interconnects.

4.4 D-Band Phase Shifter Design

The phase shifter is the most challenging component to design and implement due to the interconnect complexity, especially at 140 GHz. The proposed 4-bit implementation is based on a fully differential vector modulator with input and output baluns (Figure 4.8). The design involves a balanced input balun, an I/Q signal generator and a vector modulator that is used for proper summation of the I/Q currents at the output, to generate the desired phase shift.

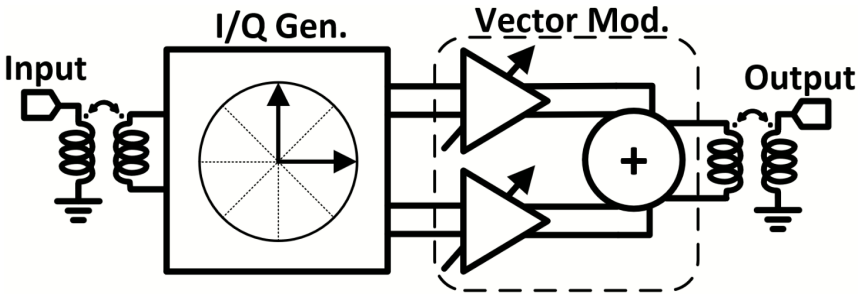


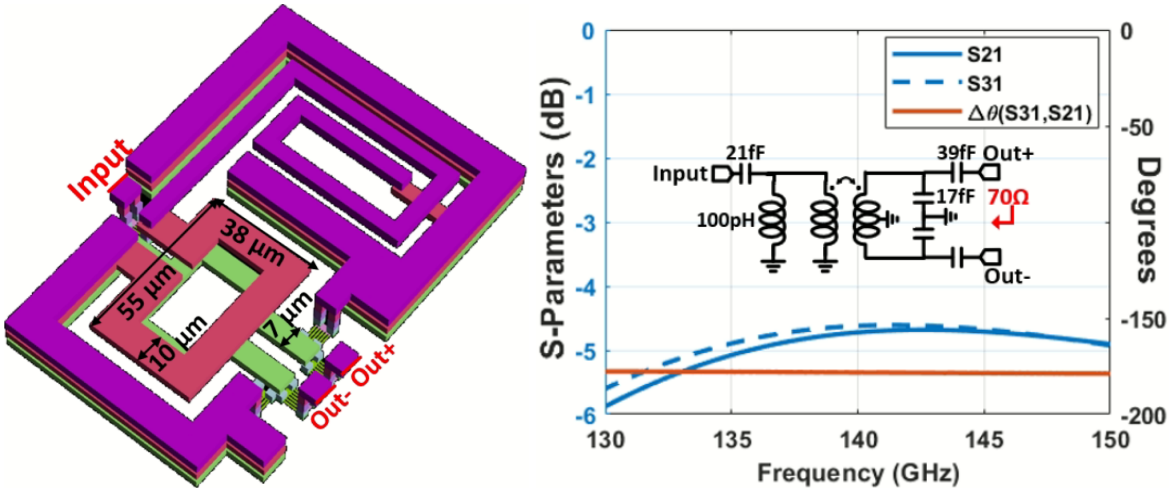
Figure 4.8: Proposed D-band phase shifter block diagram.

4.4.1 Balanced Balun Design

The design of a passive balun at 140 GHz is a challenging task, since phase and gain balance at the secondary ports requires extensive EM modeling and simulations to be achieved. This is a critical aspect of the design as gain and phase imbalances introduced before the I/Q signal summation will directly translate to an increase of the RMS phase and gain error of the phase shifter.

The passive balun transforms the single-ended 50 Ω to match the input impedance of the coupled line coupler (70 Ω) (Figure 4.9a- 4.9b). The design utilizes the OA-OB metals due to

their thickness and close vertical distance to increase the coupling factor and reduce the loss. The simulated S21 is 1.7 dB (plus the natural 3 dB split) and the phase difference is 178.5 degrees at 140 GHz.



(a) (b)

Figure 4.9: (a) Balun layout (b) Simulated balun amplitude and phase balance.

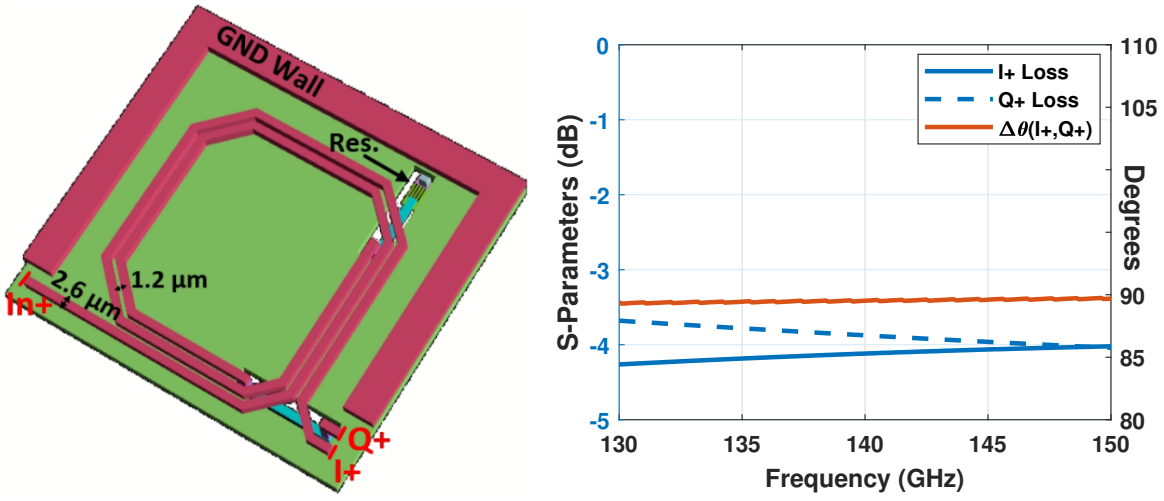
4.4.2 Coupled Line Coupler - I/Q Generator

After the passive balun, the input signal to the differential I/Q generator ideally has a 180° phase shift. The output of the coupled-line coupler will ideally be amplitude balanced and each port will have a ideal 90° separation. This is a crucial part of the design as any imbalances prior to the I/Q summation will compromise the RMS phase error.

The I/Q generator uses 2 single-ended $\frac{\lambda}{4}$ couplers, one for each polarity (Figure 4.10a). The coupler transmission lines are routed on the OB layer using the OA layer as ground. For a width of 2.6 μm and spacing of 1.2 μm the coupler has an input single ended impedance of 35 Ω (even/odd: 53/24 Ω).

Another design aspect for the design is the input impedance of the vector modulator, that is very low (3 - j15 Ω) at 140 GHz, leading to a very lossy impedance transformation if the

coupled line coupler input impedance is large (i.e. 50 Ω). However, due to DRC limitations the achieved minimum value of the output impedance while still retaining the phase and gain balance of the coupler is 35 Ω.



(a) (b)

Figure 4.10: (a) Coupled-line coupler layout. (b) Simulated coupler amplitude and phase balance.

The simulated results of the coupler illustrate excellent phase and gain balance at inverse and quadrature ports, will an exact 90° separation and a 0.3 amplitude imbalance, with 0.8 - 1 dB of excess insertion loss (after the natural 3-dB power split).

4.4.3 D-Band Vector Modulator

In the schematic representation of the design (Figure 4.11), we notice two copies of the single ended $\frac{\lambda}{4}$ coupled line coupler used as an I/Q generator, the input matching network of the vector modulator, based on LC matching, and the gilbert-cell based vector modulator along with the output matching network.

The vector modulator design uses higher V_{dd} due to the headroom considerations introduced by the need to stack 3 devices. The devices of the differential pair use capacitive neutralization (as in the LNA design) and operate at higher J_d of 0.2-0.25 $\frac{mA}{\mu m}$, in order to have

sufficient intrinsic gain.

Each differential pair is activated using the polarity control, in order to select the phase quadrant of operation (Table 4.1). The current mirror at the bottom is used to control the magnitude of the inverse or quadrature current that will be used in the output combining network.

For this purpose an external current DAC is designed with a target of providing the coarse and fine tuning required to achieve the exact I/Q ratios for the desired phase shift state. Both the polarity selection device and the current mirror device sizes are significantly higher than the g_m device in order to increase the available headroom for the g_m device.

Table 4.1: Phase quadrant selection control

Quadrant	**0-90** (°)	**90-180** (°)	**180-270** (°)	**270-360** (°)
C_{I+}	1	0	0	1
C_{I-}	0	1	1	0
C_{Q+}	1	1	0	0
C_{Q-}	0	0	1	1

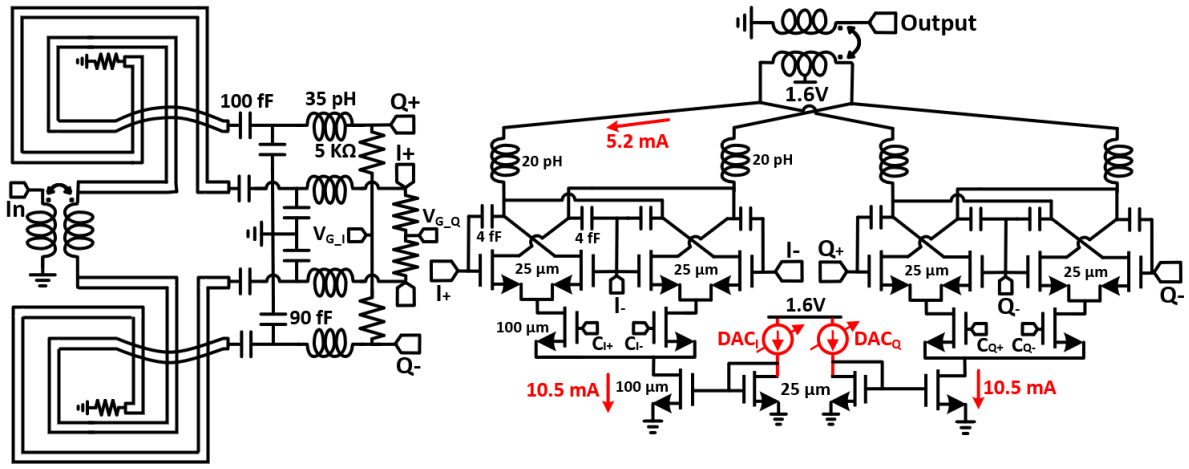


Figure 4.11: Full phase shifter schematic at balanced I/Q excitation (45 ° state).

In order to activate the appropriate phase state the following current ratios are used, along with the quadrant control sequence.

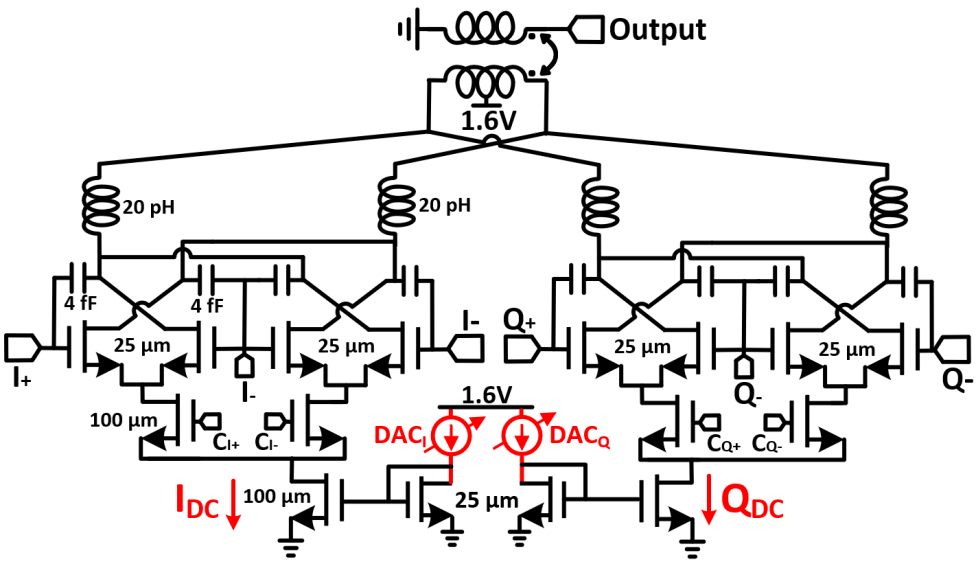


Figure 4.12: Phase shifter bias currents for different control settings.

Table 4.2: Phase state selection control

Quadrant	**0°**	**22°**	**45°**	**67°**	**90°**
$I_{DC}(mA)$	15.6	12.4	10.5	2.2	0
Q_{DC} **(mA)**	0	2.2	10.5	12.4	15.6
$I_{RF} + I_{bias}$ **(mA)**	19	17.8	25.5	17.8	19
P_{dc} **(mW)**	30.4	28.5	40.8	28.5	30.4

Table 4.2 indicates the power consumption per phase state. The design has different power consumption per selected state as this is a design selection in order to use the J_d knob to modify the effective g_m point of operation of this device in order to improve the RMS gain error performance of the beamformer channel.

The power consumption spans from 28.5 - 40.8 mW for a V_{dd} = 1.6 V. The rest of the states in the other quadrants are generated using the same truth table and mirroring the values of the dc currents accordingly. We notice that the 22 and 67 ° states require a 5.6 ratio between the I and Q bias currents.

4.5 D-Band VGA Design

The 3-bit VGA design uses 2 stages of the transformer-coupled differential pair used in the LNA design (Figure 4.13). The variable gain functionality stems from the modification of the f_t/f_{max} point of operation for each device, throught he control of the device V_{GS}. In order to have steep gain control the traversing of the f_t/f_{max} needs to happen at low current densities of 0.05-0.2 $\frac{mA}{\mu m}$ (Table 4.3).

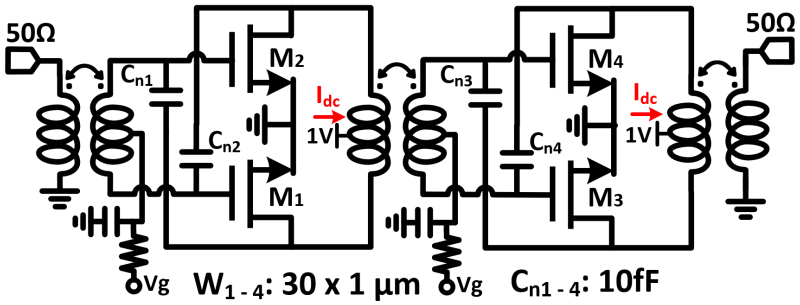


Figure 4.13: Transformer-coupled VGA schematic.

Another aspect of the design that makes the VGA integration at D-band challenging is the minimization of the phase variation across the different gain states. The Vgs knob was the best option for this purpose since the associated capacitances of the device do not illustrate significant variation across different bias points, as it can be shown in both simulation and channel measurements.

Table 4.3: VGA state control bias currents.

Attenuation	**0 dB**	**0.8 dB**	**1.6 dB**	**2.4 dB**	**3.2 dB**	**4 dB**	**4.8 dB**	**5.6 dB**
$I_{DC}(mA)$	23	18	15	13	11	10	8.5	7
J_D $(\frac{mA}{\mu m})$	0.192	0.15	0.125	0.108	0.092	0.083	0.071	0.058
P_{DC} **(mW)**	25.3	19.8	16.5	14.3	12.1	11	9.4	7.7

4.6 Measurements

All measurements are performed using on-chip probing with GGB GSG WR-6 and WR-5 waveguide probes. For the small-signal measurements, a Keysight E8364B network analyzer and OML WR6 VNA extension modules are used, together with on-chip TRL calibration. The reference planes are located at the waveguide probe tips.

4.6.1 S-Parameters

The measured peak gain is 19.2 dB at 137 GHz with a 3-dB bandwidth from 132 - 142 GHz (10 GHz). The mean gain is 16 dB at 137 GHz (Figure 4.14). The RMS gain error is 1.5 dB (Figure 4.14). It is clear that there is significant discrepancy between simulated and measured results. There are two main reasons for this discrepancy.

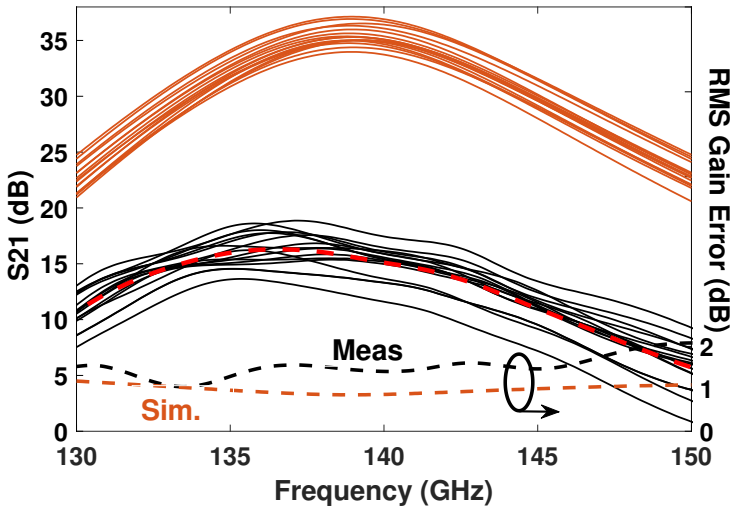
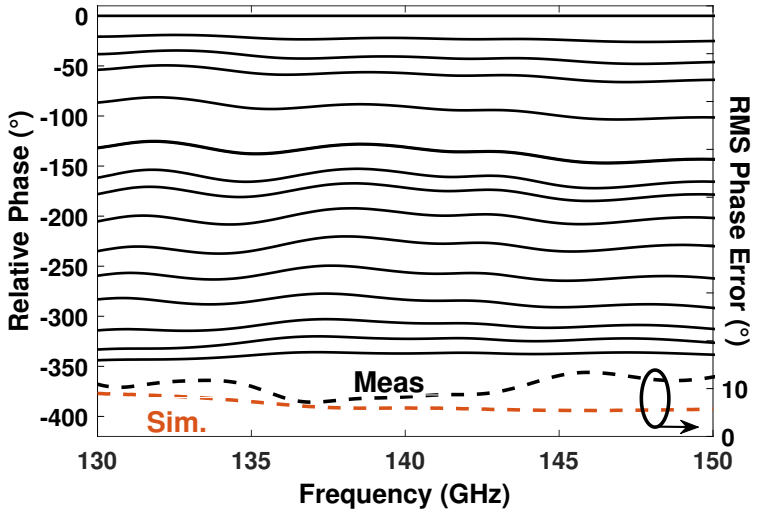


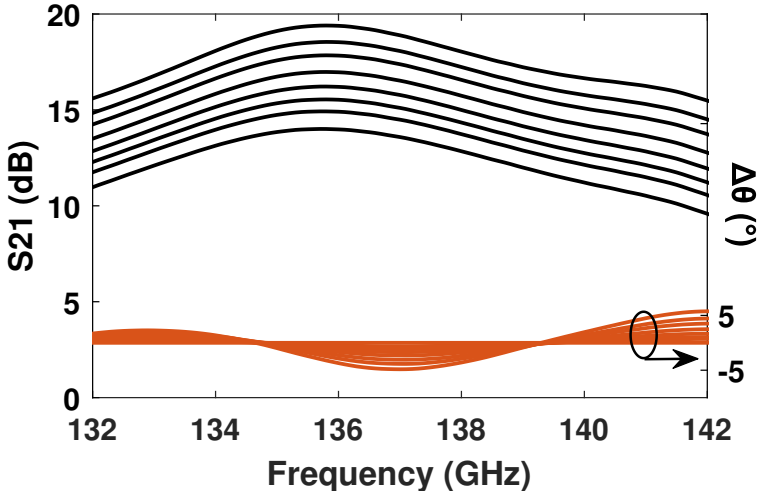
Figure 4.14: Measured gain variation vs phase states and RMS gain error.

First, the presented LNA measurements indicate an upward shift in the center frequency, leading to more than 10 dB of difference at 136 GHz with respect to the anticipated gain. Second, the EM simulations involved in the design of the phase shifter and the layout complexity lead to a discrepancy in the expected loss of the phase shifter by 5 dB. This leads to an overall S_{21}

difference of 15 dB at 137 GHz. Also, layout asymmetries that are not captured in the EM models generate a steeper gain variation than expected.



(a)



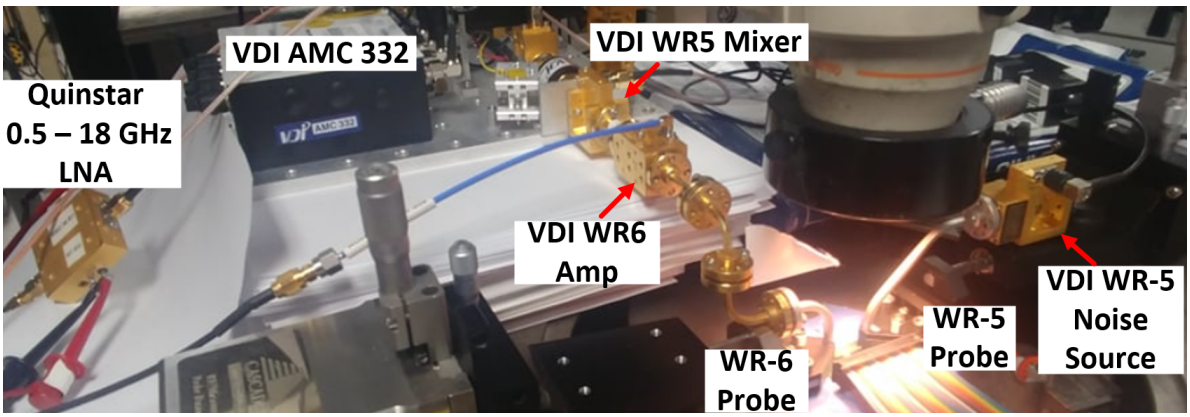
(b)

Figure 4.15: (a) Measured phase states and RMS phase error. (b) Measured gain states and phase variation vs gain states.

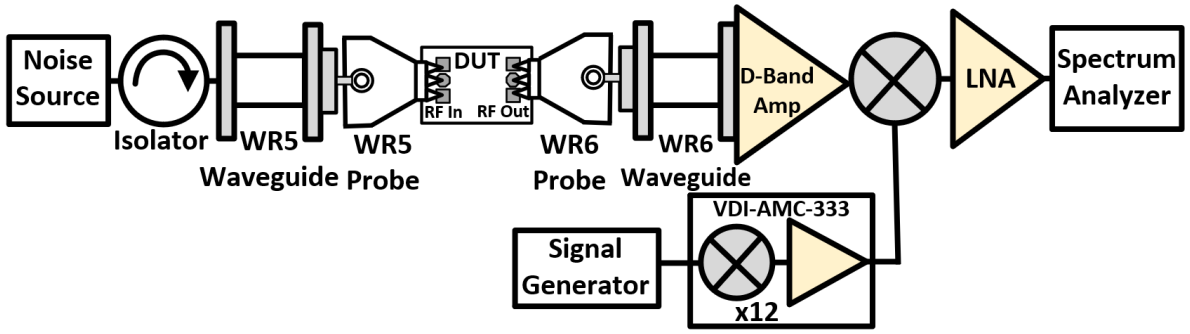
The RMS phase error is less than 11° leading to a monotonical, true 4-bit performance while the RMS gain error is 1.5 dB (Figure 4.15a). The VGA exhibits a 3-dB gain control with a $< 5°$ absolute phase variation versus gain states. (Figure 4.15b) for a total attenuation of 5.5 dB.

4.6.2 Noise Figure Measurements

The receiver channel noise figure is measured with the hot/cold Y-factor method using an external VDI WR5 noise source with an isolator. The noise source's ENR is characterized for frequencies higher than 140 GHz and for the purposes of this measurement it is assumed that it retains its noise characteristics at the 132-140 GHz range (specifically assume an ENR = 8.5 dB).



(a)



(b)

Figure 4.16: (a) Photograph of NF measurement setup. (b) Block diagram of NF measurement setup.

In Figure 4.16, the setup used for the NF measurements is presented. The WR-5 noise source is directly connected onto the WR-5 GGB probe which has a 4 dB insertion loss which is de-embedded from the measured NF to get the reference point to the probe tip. On the output side of the DUT a D-band amplifier with 20 dB of gain is used to compensate the loss of the WR5 VDI passive sub-harmonic mixer that is needed for the signal down-conversion.

The frequency downconversion of the noise signal is necessary as there are no available power meters at that would allow a direct measurement of the noise power levels at D-band. Then, the downconverted noise signal is amplified using an IF Quinstar 0.5 - 18 GHz LNA so that the power level can be increased above the sensitivity level of the spectrum analyzer. The measured NF is 6.5-8 dB from 132-142 GHz with an average NF of 7 dB (Figure 4.17).

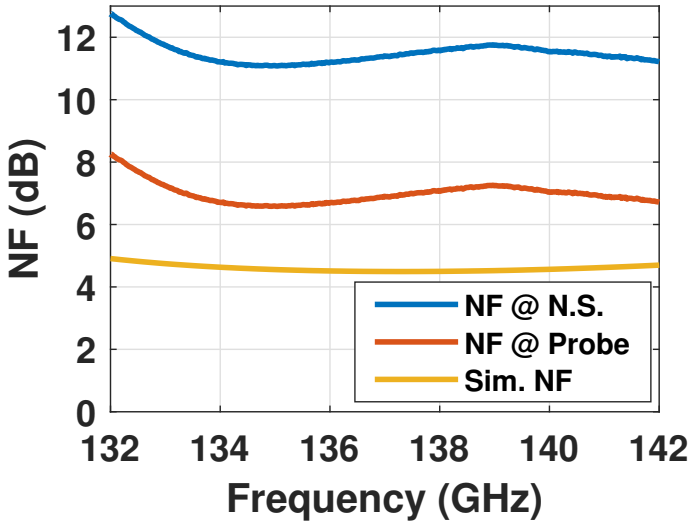
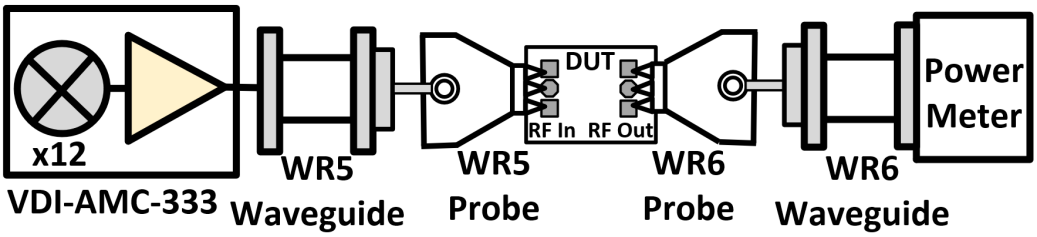


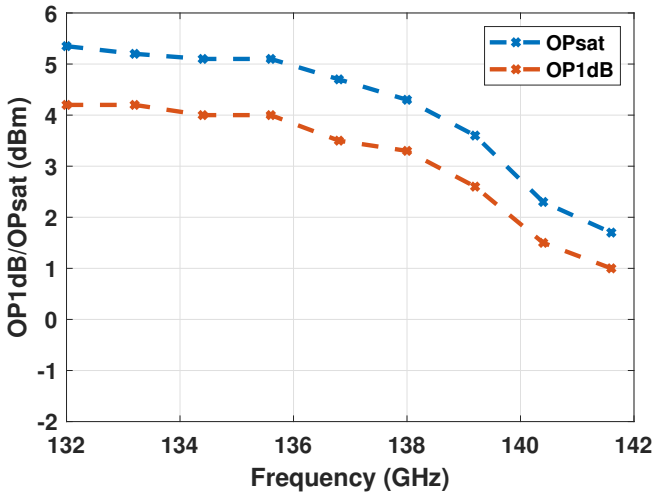
Figure 4.17: Beamformer channel NF measurement.

4.6.3 Large Signal Measurements

For the large singal measurements the VDI AMC-333 is used to provide the input power signal to the DUT. First, the AMC output power is characterized vs frequency and then the same power level is used as the input of the channel and the output power is monitored using the VDI PM4 power meter. The input and output probe losses are de-embedded in order to bring the reference points of the measurement to the probe tips. The measured OP_{1dB} is 0-3.5 dBm and the OP_{sat} is 0.5-5 dBm from 132-142 GHz.



(a)



(b)

Figure 4.18: (a) Large signal measurement setup (b) Beamformer channel power measurements.

4.7 Conclusion

A D-band full RF beamforming phased-array receive channel implemented in GF CMOS 45nm RFSOI is demonstrated. A design employing a transformer-coupled LNA with capacitive neutralization, a D-band vector modulator and VGA results in a phased-array receive channel with ultra-low-noise figure, very low RMS errors and competitive power consumption, which is an ideal candidate for large-scale phased-arrays at 140 GHz.

The design performance is compared with other state-of-the-art implementations in Table 4.4. The design exhibits the first reported D-band beamformer with full integration of the beamforming functionality at 140 GHz and a NF of 7 dB, along with a very competitive power consumption.

Table 4.4: Performance comparison of D-band CMOS receiver

	This Work	[70]	[71]	[72]	[73]	[74]
Technology	**45nm CMOS SOI**	45nm CMOS SOI	45nm CMOS SOI	28nm CMOS	22nm CMOS SOI	45nm CMOS SOI
Integration	**Full RF Beamforming**	FE+IF	FE + Zero-IF	FE + Zero-IF	FE+Zero-IF	Mixer + Zero-IF
RF Freq. (GHz)	**132-142**	137-151	140	102-128	135	150
Gain (dB)	**19.2**	26.5	18	36-39	27	23
NF (dB)	**6.6-8.2**	6.4-7.5	5.5[a]	8.4-10.1	8.5[a]	20[a]
IP1dB (dBm)	**-16 @136**	-28.5 @139	-	-35 @115	-30 @135	-
RMS Error (dB)	**1-1.5 (132-142)**	0.2-0.6 @(9.3-14.3)	-	-	-	-
RMS Error (°)	< 11 **(4-bit)**	-	-	-	-	-
Pdc (mW)	**105**[d]	133	125	51[c]	198	290[b]
Area (mm^2)	**1.2**[e]	0.71[e]	2.97[f]	0.89[h]	1.44[h]	3.9[g]

[a]simulated, [b]TRX, [c]no LO chain, [d]max P_{dc}, [e]core area, [f]RX die area, [g]TRX die area, [h]die area

4.8 Acknowledgment

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Chapter 4, in full, is being prepared to be submitted for publication of the material as it may appear in: D. Baltimas, Siwei Li and G. M. Rebeiz, "A 132-142 GHz RF Beamforming Phased Array Receiver Channel with 7 dB NF in 45nm RFSOI", in *IEEE Microwave and Wireless Component Letters*. The dissertation author was the primary investigator and author of this paper.

Chapter 5

Conclusion and Future Work

5.1 Dissertation Summary

Phase array development and deployment for large arrays with high effective isotropic radiated power (EIRP) has only been commercially feasible due to the advancements in silicon technologies. Particularly, developments in beamformer chips in various silicon-based technologies (SiGe, SOI) have enabled the commercialization of phased arrays for 5G wireless communications, satellite communications (SATCOM) and $>$ 100 GHz communication links.

This dissertation presented a multitude of circuit level advancements in phase change material, SiGe BiCMOS and SOI processes for the design and implementation of high performance beamformer channels that can then be utilized for the design of large phase arrays form DC to 140 GHz.

In chapter 2, an advanced PCM switch integrated in the BEOL of a commericially available SiGe BiCMOS process is utilized for the design of ultra-wideband multi-throw switches. The PCM switches are then used for the design on a state-of-the-art TTD block that can be used for extremely wideband instantaneous bandwidth applications. To the authors knowledge, this chip illustrates the largest relative group delay presented on an IC.

In chapter 3, A standard SiGe BiCMOS process (GF8HP), is utilized for the design of a 19-22 GHz high linearity beamformer channel with $>$ 8 dBm OP_{sat}, $>$ 0 dBm IIP3, a NF of 7 dB and 5-bit of phase and gain control leading to a very high dynamic range performance. The chip is also implemented as flip-chip and its measured performance is retained.

Finally, in chapter 4 a 132-142 GHz Rx beamformer channel with 4-bit of phase and 3-bit of gain control is presented. In this design, a full RF integration of the beamforming functionality at D-band is illustrated, leading to another potential candidate for the implementation of D-band phased-arrays. To the authors knowledge, this is the first D-band beamformer with integration of the phase shifter and VGA at 140 GHz and a 7 dB NF.

All presented beamformer chips, illustrate significant advancements in various performance aspects and can be utilized for the implementation of high performance phased arrays.

5.2 Future Work

The presented beamformer implementations presented in this dissertation may be expanded and improved in several aspects, in future work:

1) For the phase change material switches and the true time delay unit presented in section 2, the biggest step towards making this technology readily available for a multitude of applications is the integration of the control circuits needed for the switch actuation on chip. This will allow for the design of even more complex systems on chip using the switch. If this advancement is made, then the presented TTD unit can then be accompanied by an LNA, VGA and other front-end components using the SiGe BiCMOS front end offered by Tower Semiconductor SBC18H3 process, for the design of a cutting-edge beamformer that would achieve tremendous instantaneous bandwidths. One potential improvement on the TTD unit itself, is with regard to its RMS gain error performance, that is deteriorating versus frequency due to the transmission line loss dominating the overall loss. One potential solution to this issue is the intentional intriduction

of los in the reference signal path in order to maintain a competitive RMS gain error even if the loss of the long transmission lines increases.

2) For the K-band common-leg Rx/Tx channel presented in section 3, there are several aspects of the performance that can be improved. The noise figure of the channel can be reduced by 1-1.5 dB if the LNA implementation is single ended and then a balun is used directly after the LNA to proceed to the differential phase shifters and attenuators. Another potential improvement is with regard to the RMS gain error performance. In a re-design effort should be made so that the small phase shifter cells gain discrepancy is smaller and then the RMS phase erro of the beamformer can be improved by 0.25 dB.

3) For the full RF beamformer at D-band that is presented in section 4, several improvements can be made in the design. First of the integration of SPI control will significantly reduce the number of pads needed for its control that will directly translate to the reduction of the chip area, a key aspect for the utilization of the chip in actual phased array applications where the actual size of the beamformer may be limiting in the positioning of the elements at $\frac{\lambda}{2}$ distance apart. Other configurations can also be examined, for example passive phase shifters at 140 GHz may be feasible given the extremely high Q that the process offers even at 140 GHz. This would reduce the overall power consumption in half, and the drop in gain can be compensated using another amplifier at D-band.

Bibliography

[1] Qualcomm, “What is 5G: Everything you need to know About 5G: 5G FAQ,” May 2021. [Online]. Available: https://www.qualcomm.com/5g/what-is-5g

[2] C. Daehnick, I. Klinghoffer, B. Maritz, and B. Wiseman, "Large LEO satellite constellations: Will it be different this time?," McKinsey Company, 04-May-2020. [Online]. Available: https://www.mckinsey.com/industries/aerospace-and-defense/our-insights/large-leosatellite-constellations-will-it-be-different-this-time.

[3] FCC, Mar 2019. [Online]. Available: https://docs.fcc.gov/public/attachments/DOC-356297A1.pdf

[4] Cisco Annual Internet Report (2018–2023) White Paper, March 2020 [Online]. Available: https://www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.html

[5] E. Sisinni, A. Saifullah, S. Han, U. Jennehag and M. Gidlund, "Industrial Internet of Things: Challenges, Opportunities, and Directions," *IEEE Transactions on Industrial Informatics*, vol. 14, no. 11, pp. 4724-4734, Nov. 2018.

[6] Douglas L. McMakin, Paul E. Keller, David M. Sheen, and Thomas E. Hall "Dual-surface dielectric depth detector for holographic millimeter-wave security scanners", Proc. SPIE 7309, Passive Millimeter-Wave Imaging Technology XII, 73090G (29 April 2009).

[7] White Paper Innovative RF-SOI Wafers for Wireless Applications, 2013. [Online]. Available: https://www.soitec.com/media/files/soitec_rf-soi_substrates_wp.pdf

[8] N. El-Hinnawy P. Borodulin, E. B. Jones, B. P. Wagner, M. R. King, J. S. Mason, J. Bain, J. Paramesh, T. E. Schlesinger, R. S. Howell, M. J. Lee and R. M. Young, "12.5 THz Fco GeTe Inline Phase-Change Switch Technology for Reconfigurable RF and Switching Applications," 2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), 2014, pp. 1-3.

[9] D. Baltimas and G. M. Rebeiz, "A 25–50GHz Phase Change Material (PCM) 5-Bit True Time Delay Phase Shifter in a Production SiGe BiCMOS Process," *IEEE/MTT-S International Microwave Symposium (IMS)*, Dec. 2020.

[10] T. Singh and R. R. Mansour, "Miniaturized DC–60 GHz RF PCM GeTe-Based Monolithically Integrated Redundancy Switch Matrix Using T-Type Switching Unit Cells," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 12, pp. 5181-5190, Dec. 2019.

[11] T. Singh and R. R. Mansour, "Monolithic PCM Based Miniaturized T-type RF Switch for Millimeter Wave Redundancy Switch Matrix Applications," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019, pp. 658-660.

[12] T. Singh and R. R. Mansour, "Scalable Non-Volatile Chalcogenide Phase Change GeTe-Based Monolithically Integrated mmWave Crossbar Switch Matrix," in *021 IEEE MTT-S International Microwave Symposium (IMS)*, 2021, pp. 420-423.

[13] Z. Sun, H. Liu, H. Huang, D. Tang, D. Xu, T. Kaneko, Z. Li, J. Pang, R. Wu, W. Deng, A. Shirane and K. Okada, "A 0.85mm^2 BLE Transceiver Using an On-Chip Harmonic-Suppressed RFIO Circuitry With T/R Switch," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 1, pp. 196-209, Jan. 2021.

[14] M. Lokhandwala, L. Gao and G. M. Rebeiz, "A High-Power 24–40-GHz Transmit–Receive Front End for Phased Arrays in 45-nm CMOS SOI," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 11, pp. 4775-4786.

[15] T. Singh and R. R. Mansour, "Miniaturized Reconfigurable 28 GHz PCM-Based 4-bit Latching Variable Attenuator for 5G mmWave Applications," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020, pp. 53-56.

[16] T. Chu and H. Hashemi, "A true time-delay-based bandpass multi-beam array at mm-waves supporting instantaneously wide bandwidths," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, 2010, pp. 38-39.

[17] S. K. Garakoui, E. A. M. Klumperink, B. Nauta and F. E. van Vliet, "Compact Cascadable g m -C All-Pass True Time Delay Cell With Reduced Delay Variation Over Frequency," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 3, pp. 693-703, March 2015.

[18] T. Chu and H. Hashemi, "True-Time-Delay-Based Multi-Beam Arrays," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 8, pp. 3072-3082, Aug. 2013.

[19] S. Barker and G. M. Rebeiz, "Distributed MEMS true-time delay phase shifters and wide-band switches," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 11, pp. 1881-1890, Nov. 1998.

[20] D. Kuylenstierna, A. Vorobiev, P. Linner and S. Gevorgian, "Ultrawide-band tunable true-time delay lines using ferroelectric varactors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 6, pp. 2164-2170, June 2005.

[21] J. S. Hayden, A. Malczewski, J. Kleber, C. L. Goldsmith and G. M. Rebeiz, "2 and 4-bit DC-18 GHz microstrip MEMS distributed phase shifters," in *2001 IEEE MTT-S International Microwave Symposium Digest* (Cat. No.01CH37157), 2001, pp. 219-222 vol.1.

[22] Q. Ma, D. Leenaerts and R. Mahmoudi, "A 10–50GHz True-Time-Delay phase shifter with max 3.9% delay variation" in *IEEE Radio Frequency Integrated Circuits Symposium*, Tampa, FL, 2014, pp. 83-86, 2014.

[23] S. Park and S. Jeon, "A 15–40 GHz CMOS True-Time Delay Circuit for UWB Multi-Antenna Systems," *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 3, pp. 149-151, March 2013.

[24] Guan-Leng Tan, R. E. Mihailovich, J. B. Hacker, J. F. DeNatale and G. M. Rebeiz, "Low-loss 2- and 4-bit TTD MEMS phase shifters based on SP4T switches," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 1, pp. 297-304, Jan. 2003.

[25] S. K. Garakoui, E. A. M. Klumperink, B. Nauta and F. E. van Vliet, "Compact Cascadable g m -C All-Pass True Time Delay Cell With Reduced Delay Variation Over Frequency," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 3, pp. 693-703, March 2015.

[26] M. Jung and B. -W. Min, "A Compact 3–30-GHz 68.5-ps CMOS True-Time Delay for Wideband Phased Array Systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 12, pp. 5371-5380, Dec. 2020.

[27] T. Singh and R. R. Mansour, "Loss Compensated PCM GeTe-Based Latching Wideband 3-bit Switched True-Time-Delay Phase Shifters for mmWave Phased Arrays," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 9, pp. 3745-3755, Sept. 2020.

[28] W. Lee and S. Hong, "Ka-Band Inductor-Shared SP *n* T DP *n* T Switches and Their Applications to TTD Phase Shifter," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 2546-2554, July 2019.

[29] F. Gianesello, A. Monroy, V. Vialla, E. Canderle, G. Bertrand, M. Buczko, M. Coly, J. Nowakowski, N. Revil, L. Rolland, D. Gloria, A. Juge, S. Gachon, J. P. Aubert and E. Granger, "Highly linear and sub 120 fs Ron × Coff 130 nm RF SOI technology targeting 5G carrier aggregation RF switches and FEM SOC," in *2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2016, pp. 9-12.

[30] M. Jaffe, M. Abou-Khalil, A. Botula, J. Ellis-Monaghan, J. Gambino, J. Gross, Z. -X. He, A. Joseph, R. Phelps, S. Shank, J. Slinkman and R. Wolf, "Improvements in SOI technology for RF switches," in *IEEE 15th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2015, pp. 30-32.

[31] C. S. Levy, P. M. Asbeck and J. F. Buckwalter, "A CMOS SOI Stacked Shunt Switch with Sub-500ps Time Constant and 19-Vpp Breakdown," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2013.

[32] C. Li, G. Freeman, M. Boenke, N. Cahoon, U. Kodak and G. Rebeiz, "1W $<$ 0.9dB IL DC-20GHz T/R switch design with 45nm SOI process," in *IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2017.

[33] C. D. Patel and G. M. Rebeiz, "A High-Reliability High-Linearity High-Power RF MEMS Metal-Contact Switch for DC–40-GHz Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 10, pp. 3096-3112, Oct. 2012.

[34] G. Slovin, M. Xu, J. Paramesh, T. E. Schlesinger and J. A. Bain, "AlN Barriers for Capacitance Reduction in Phase-Change RF Switches," in *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 568-571, May 2016.

[35] G. Slovin, M. Xu, R. Singh, T. E. Schlesinger, J. Paramesh and J. A. Bain, "Design Criteria in Sizing Phase-Change RF Switches," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4531-4540, Nov. 2017.

[36] T. Singh and R. R. Mansour, "Characterization, Optimization, and Fabrication of Phase Change Material Germanium Telluride Based Miniaturized DC–67 GHz RF Switches," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 8, pp. 3237-3250, Aug. 2019.

[37] T. Singh and R. R. Mansour, "A Miniaturized Monolithic PCM Based Scalable Four-Port RF Switch Unit-Cell," in *2019 49th European Microwave Conference (EuMC)*, 2019, pp. 180-183.

[38] M. Wang, Y. Shim and M. Rais-Zadeh, "A Low-Loss Directly Heated Two-Port RF Phase Change Switch," in *IEEE Electron Device Letters*, vol. 35, no. 4, pp. 491-493, April 2014.

[39] A. Crunteanu, A. Mennai, C. Guines, D. Passerieux and P. Blondy, "Out-of-plane and inline RF switches based on Ge2Sb2Te5 phase-change material," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 1-4.

[40] N. El-Hinnawy, P. Borodulin, B. Wagner, M. R. King, J. S. Mason, E. B. Jones, S. McLaughlin, V. Veliadis, M. Snook, M. E. Sherwin, R. S. Howell, R. M. Young and M. J. Lee, "A Four-Terminal, Inline, Chalcogenide Phase-Change RF Switch Using an Independent Resistive Heater for Thermal Actuation," *IEEE Electron Device Letters*, vol. 34, no. 10, pp. 1313-1315, Oct. 2013.

[41] N. El-Hinnawy, P. Borodulin, B. Wagner, M. R. King, J. S. Mason, E. B. Jones, S. McLaughlin, V. Veliadis, R. S. Howell, R. M. Young and M. J. Lee, "A 7.3 THz Cut-Off Frequency, Inline, Chalcogenide Phase-Change RF Switch Using an Independent Resistive Heater for Thermal Actuation," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Monterey, CA, 2013.

[42] N. El-Hinnawy, P. Borodulin, E. B. Jones, B. P. Wagner, M. R. King, J. S. Mason, J. Bain, J. Paramesh, T. E. Schlesinger, R. S. Howell, M. J. Lee and R. M. Young, "12.5 THz Fco GeTe Inline Phase-Change Switch Technology for Reconfigurable RF and Switching Applications,"

in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, La Jolla, CA, 2014, pp. 1-3.

[43] G. Slovin, N. El-Hinnawy, C. Masse, J. Rose and D. Howard, "Monolithic Integration of Phase-Change RF Switches in a Production SiGe BiCMOS Process with RF Circuit Demonstrations," in *IEEE/MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA, USA, 2020, pp. 57-60.

[44] N. El-Hinnawy, G. Slovin, J. Rose and D. Howard, "A 25 THz F_{CO} (6.3 fs $R_{ON} * C_{OFF}$) Phase-Change Material RF Switch Fabricated in a High Volume Manufacturing Environment with Demonstrated Cycling $>$ 1 Billion Times," in *IEEE/MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA, USA, 2020, pp. 45-48.

[45] S. H. Hawasli, L. De La Cruz, N. El-Hinnawy, P. Borodulin, M. King, R. M. Young, M. Zaghloul and T. G. Ivanov, "Investigation of on-state power handling dependence on number of cycles for germanium telluride RF switches," in *IEEE MTT-S International Microwave Symposium (IMS)*, 2017, pp. 292-295.

[46] F. Amin, T. Beglin, N. Edwards, N. El-Hinnawy, G. Slovin, D. Howard, D. Nichols and R. M. Young, "Wideband SPDT and SP4T RF Switches using Phase-Change Material in a SiGe BiCMOS Process," in emph2021 IEEE MTT-S International Microwave Symposium (IMS), 2021, pp. 431-434.

[47] T. Singh and R. R. Mansour, "Chalcogenide Phase Change Material GeTe Based Inline RF SPST Series and Shunt Switches," in *2018 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, 2018, pp. 1-3.

[48] T. Singh and R. R. Mansour, "Reconfigurable PCM GeTe-Based Latching 6-Bit Digital Switched Capacitor Bank," in *2020 15th European Microwave Integrated Circuits Conference (EuMIC)*, 2021, pp. 93-96.

[49] A. Tomkins, P. Garcia and S. P. Voinigescu, "A 94GHz SPST Switch in 65nm Bulk CMOS," in *IEEE Compound Semiconductor Integrated Circuits Symposium*, 2008, pp. 1-4.

[50] R. Ciocoveanu, R. Weigel, A. Hagelauer and V. Issakov, "A Low Insertion-Loss 10–110 GHz Digitally Tunable SPST Switch in 22 nm FD-SOI CMOS," in *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2018, pp. 1-4.

[51] L. Wu, H. Y. Hsu and S. P. Voinigescu, "A DC to 220-GHz High-Isolation SPST Switch in 22-nm FDSOI CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 6, pp. 775-778, June 2021.

[52] G. Slovin, N. El-Hinnawy, C. Masse, J. Rose and D. Howard, "Multi-Throw SPNT Circuits Using Phase-Change Material RF Switches for 5G and Millimeter Wave Applications," in emph2021 IEEE MTT-S International Microwave Symposium (IMS), 2021, pp. 428-430.

[53] A. Hariri, A. Crunteanu, C. Guines, C. Hallepee, D. Passerieux and P. Blondy, "Double-Port Double-Throw (DPDT) Switch Matrix Based on Phase Change Material (PCM)," in *2018 48th European Microwave Conference (EuMC)*, 2018, pp. 479-482.

[54] B. Yu, K. Ma, F. Meng, K. S. Yeo, P. Shyam, S. Zhang and P. R. Verma, "Ultra-Wideband Low-Loss Switch Design in High-Resistivity Trap-Rich SOI With Enhanced Channel Mobility," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 10, pp. 3937-3949, Oct. 2017.

[55] H. Chang and C. Chan, "A Low Loss High Isolation DC-60 GHz SPDT Traveling-Wave Switch With a Body Bias Technique in 90 nm CMOS Process," *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 2, pp. 82-84, Feb. 2010.

[56] C. Li, B. Ustundag, A. Kumar, M. Boenke, U. Kodak and G. Rebeiz, "$<$ 0.8dB IL 46dBm OIP3 Ka band SPDT for 5G communication," in *IEEE 18th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2018, pp. 1-3.

[57] B. Cetinoneri, Y. A. Atesal and G. M. Rebeiz, "A miniature DC-70 GHz SP4T switch in 0.13-µm CMOS," in *IEEE MTT-S International Microwave Symposium Digest*, 2009, pp. 1093-1096.

[58] M. Uzunkol and G. Rebeiz, "A Low-Loss 50–70 GHz SPDT Switch in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 10, pp. 2003-2007, Oct. 2010.

[59] S. Vaccaro, L. Diamond, D. Runyon and M. C. Vigano, “Ka-Band Mobility Terminals Enabling New Services,” in *IEEE EuCAP*, Apr. 2014, pp. 2617–2618.

[60] G. M. Rebeiz and L. M. Paulsen, “Advances in SATCOM phased arrays using silicon technologies,” in *IEEE IMS*, Jun. 2017, pp. 1877–1879.

[61] L. Zhang, C. Zhao, X. Zhang, Y. Wu and K. Kang, "A CMOS K-Band 6-bit Attenuator With Low Phase Imbalance for Phased Array Applications," in *IEEE Access*, vol. 5, pp. 19657-19661, 2017.

[62] M. Davulcu, C. Caliskan, I. Kalyoncu, M. Kaynak and Y. Gurbuz, "7-Bit SiGe-BiCMOS Step Attenuator for X-Band Phased-Array RADAR Applications," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 8, pp. 598-600, Aug. 2016.

[63] B. Ku and S. Hong, "6-bit CMOS Digital Attenuators With Low Phase Variations for *X*-Band Phased-Array Systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 7, pp. 1651-1663, July 2010.

[64] M. Hangai, M. Hieda, N. Yunoue, Y. Sasaki and M. Miyazaki, "*S* - and *C* -Band Ultra-Compact Phase Shifters Based on All-Pass Networks," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 1, pp. 41-47, Jan. 2010.

[65] Y. Wang, D. You, X. Fu, T. Nakamura, A. A. Fadila, T. Someya, A. Kawaguchi, J. Pang, K. Yanagisawa, B. Liu, Y. Zhang, H. Zhang, R. Wu, A. Shirane, S. Masaki, D. Yamazaki and K. Okada, "A CMOS Ka-Band SATCOM Transceiver with ACI-Cancellation Enhanced Dual-Channel Low-NF Wide-Dynamic-Range RX and High-Linearity TX," in *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2020, pp. 355-358.

[66] C. Liu, Q. Li, Y. Li, X. -D. Deng, H. Tang, R. Wang, H. Liu and Y. -Z. Xiong, "A Ka-Band Single-Chip SiGe BiCMOS Phased-Array Transmit/Receive Front-End," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 11, pp. 3667-3677, Nov. 2016.

[67] U. Kodak and G. M. Rebeiz, "A 5G 28-GHz Common-Leg T/R Front-End in 45-nm CMOS SOI With 3.7 dB NF and 30-dBc EVM With 64-QAM/500-MBaud Modulation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 1, pp. 318-331, Jan. 2019.

[68] D. Shin and G. M. Rebeiz, "Low-power low-noise 0.13 μm CMOS X-band phased array receivers," in *IEEE MTT-S International Microwave Symposium*, 2010, pp. 956-959.

[69] U. Kodak and G. M. Rebeiz, "A 42mW 26–28 GHz phased-array receive channel with 12 dB gain, 4 dB NF and 0 dBm IIP3 in 45nm CMOS SOI," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2016, pp. 348-351.

[70] S. Li and G. M. Rebeiz, "A 134-149 GHz IF Beamforming Phased-Array Receiver Channel with 6.4-7.5 dB NF Using CMOS 45nm RFSOI," in 2020 *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2020, pp. 103-106.

[71] A. Simsek, S. Kim, and M.J.W .Rodwell, "A 140 GHz MIMO Tranceiver in 45nm SOI CMOS," in 2018 *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, San Diego, CA, USA, 2018, pp. 231-234.

[72] T. Heller, E. Cohen, and E. Socher, "A 102-129-GHz 39-dB Gain 8.4- dB Noise Figure I/Q Receiver Frontend in 28-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 5, pp. 1535-1543, May 2016.

[73] A. A. Farid, A. Simsek, A. S. H. Ahmed and M. J. W. Rodwell, "A Broadband Direct Conversion Transmitter/Receiver at D-band Using CMOS 22nm FDSOI," in 2019 *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Boston, MA, USA, 2019, pp. 135-138.

[74] Y. Yang, S. Zihir, H. Lin, O. Inac, W. Shin and G. M. Rebeiz, "A 155 GHz 20 Gbit/s QPSK transceiver in 45nm CMOS," in 2014 *IEEE Radio Frequency Integrated Circuits Symposium*, Tampa, FL, 2014, pp. 365-368.

[75] Y. Zhao, E. Ojefors, K. Aufinger, T. F. Meister and U. R. Pfeiffer, "A 160-GHz Subharmonic Transmitter and Receiver Chipset in an SiGe HBT Technology," *IEEE Transactions on Microwave Theory and TechnI/Ques*, vol. 60, no. 10, pp. 3286-3299, Oct. 2012.

[76] N. Sarmah, J. Grzyb, K. Statnikov, S. Malz, P. Rodriguez Vazquez, W. Föerster, B. Heinemann and U. R. Pfeiffer, "A Fully Integrated 240-GHz Direct-Conversion Quadrature Transmitter and Receiver Chipset in SiGe Technology," *IEEE Transactions on Microwave Theory and TechnI/Ques*, vol. 64, no. 2, pp. 562-574, Feb. 2016.

[77] P. Rodríguez-Vázquez, J. Grzyb, N. Sarmah, B. Heinemann and U. R. Pfeiffer, "A 65 Gbps QPSK one meter wireless link operating at a 225–255 GHz tunable carrier in a SiGe HBT technology," in 2018 *IEEE Radio and Wireless Symposium (RWS)*, Anaheim, CA, 2018, pp. 146-149.

[78] O. Inac, M. Uzunkol and G. M. Rebeiz, “45-nm CMOS SOI technology characterization for millimeter-wave applications,” IEEE Transactionsm on Microwave Theory and TechnI/Ques, vol. 62, no. 6, pp. 1301-1311, June 2014.