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HIGH RESOLUTION THERMOREFLECTANCE IMAGING OF POWER TRANSISTORS AND NANOSCALE PERCOLATION NETWORKS

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Abstract

High Resolution Thermoreflectance Imaging of Power Transistors and Nanoscale Percolation Networks

by

Kerry Maize

Performance, efficiency, and reliability of modern high power, high speed microelectronics and nanoscale structures are strongly influenced by device self-heating on the micron and nanometer scale. Local temperature "hotspots" on a chip indicate areas of high power density and possible failure locations. This dissertation presents results of case studies using high resolution thermoreflectance imaging microscopy to characterize self-heating in high power silicon transistor arrays, gallium nitride high electron mobility power transistors (HEMTs), electrostatic discharge protection structures, and nanoscale percolation network devices. Thermoreflectance imaging microscopy was performed with submicron spatial resolution, 800 ps time resolution, and 50 mK temperature resolution.

Thermoreflectance imaging of silicon transistor arrays revealed nonuniform self-heating greater than a factor of two due to electrical debiasing. At low bias ($12\,\mathrm{mA/mm_{GATE\ WIDTH}}$), temperature distribution matched state of the art electrothermal simulation. At high bias ($47\,\mathrm{mA\,mm^{-1}}$), however, measured self-heating diverged significantly from simulation despite inclusion of temperature dependent material properties in the thermal model. Hotspots with temperature change of 70 K were observed.

Results demonstrate nonlinear dependence of current distribution on bias for complex arrayed power devices.

Transient thermoreflectance imaging of GaN HEMTs revealed for the first time temperature gradients as large at 60 K and 80 K between critical gate, channel, and contact features within the first few microseconds of pulsed electrical excitation at 19 W mm^{-1}. Fast transient self-heating gradients in the HEMT were confirmed with 5 ns time resolution using an 800 ps pulsed probe laser.

Transient thermoreflectance imaging was also used to measure self-heating distribution in an electrostatic discharge (ESD) protection structure based on a multiple finger semiconductor controlled rectifier design (SCR). Thermoreflectance imaging under fast, high current simulated ESD pulses revealed non-simultaneous, nonuniform triggering of individual device fingers both as a function of current level and at different times in the electrical pulse. Local hotspots on the SCR were visible within the first 300 nanoseconds of the simulated ESD pulse, with temperature change in excess of 400 K at 30 microseconds into the pulse.

Thermoreflectance imaging revealed nonuniform self-heating in nanoscale percolation network devices consisting of disordered 90 nm diameter silver nanowires. Microscopic hot-spots at selected nanowire-nanowire junctions in the network exhibited nonlinear thermal properties, with temperature dependence of current exceeding the prediction of Joule self-heating for bulk materials. Results encourage a fundamental reevaluation of the transport models and characterization results for network based percolating conductors.

The optical, non-contact thermoreflectance imaging microscopy method quickly measures self-heating distribution on the surface of integrated structures with 50 mK temperature resolution. Transient capable implementations with 50 ns and 800 ps temporal resolution were used to image fast pulsed transient temperature rise and fall in high frequency power integrated devices. The method is capable of submicron spatial resolution, enabling measurement of smaller device temperature features than can be achieved with similar thermal imaging techniques, such as infrared thermal microscopy. Self-heating in silver nanowire networks was imaged with 300 nm spatial resolution.

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Part I

Introduction and Experiment Method

Chapter 1

Introduction

Optimizing performance and reliability of modern and future integrated electronics will require an understanding of thermal properties of these systems. Performance and reliability in modern high speed, high power integrated circuits and novel nanoscale electronic devices are strongly related to device self-heating. Self-heating describes the increase in device temperature when it undergoes electrical excitation. Self-heating is generally an unavoidable consequence of normal device electrical operation. If temperature exceeds a safe threshold anywhere in the device, the device will fail. Device failure is often thermal in origin. [70]

Thermal analysis of these systems today and in the future will necessitate characterization methods with superior capabilities in several respects. It has been shown that temperature distribution in integrated structures is generally not spatially uniform. [14, 75, 89, 90] Localized self-heating hot spots often determine the peak operating temperature, even though the average die temperature can be significantly lower.

Figure 1.1 shows an example of a local hotspot in a high power, large NMOS transistor array under standard operating DC current bias of 1.4 A. Nonuniform current and temperature distribution are especially problematic in power devices with complex geometries. Current crowding and resulting local hot spots can impose unexpected constraints on the electrical safe operating area (SOA) or reduce device lifetime. Therefore it is important to understand the full spatial temperature distribution throughout the device. Because many modern integrated systems are designed for high speed operation, it is also important to understand fast transient self-heating effects. Integrated power technologies such as high electron mobility transistors designed for high power density and megahertz switching induce thermal and stress gradients on nanosecond time scales. [43, 44] The promising field of nanoscale integrated devices will present new and unique self-heating challenges. Temperature dependent material and contact properties become critical at smaller dimensions. Studying self-heating for the scenarios described above will require versatile thermal characterization methods that combine high temperature resolution, time resolution, and spatial resolution.

No single method for thermal metrology of microscale devices is ideal for all measurement scenarios. Choosing the optimal experiment technique must be evaluated on a per case basis. Often multiple complementary methods must be employed. Thermoreflectance imaging microscopy is part of an expanding set of experiment characterization methods that have proven useful in thermal metrology of advanced microscale and nanoscale integrated systems. Thermoreflectance imaging microscopy combines several excellent measurement capabilities, including 10 millikelvin temperature resolution,

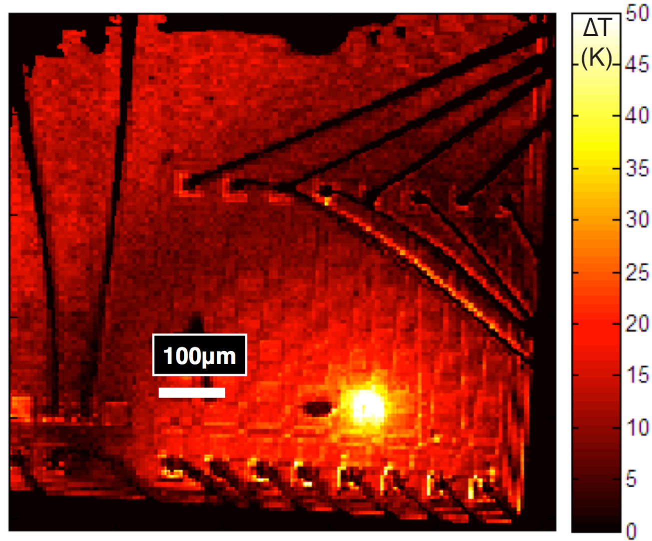

Figure 1.1: Thermoreflectance image of hotspot in wire bonded power NMOS transistor array under standard operating DC current bias of 1.4 A.

submicron spatial resolution, and subnanosecond transient time resolution. [7,47,93] The method is versatile and measurements are relatively easy to perform. Advancement in imaging sensors and illumination sources in recent years has extended the capabilities thermoreflectance imaging microscopy. These improvements motivated new studies using thermoreflectance imaging to measure thermal performance and thermal properties in novel microscale and nanoscale electronic, optoelectronic, photonic, and thermoelectric devices and materials.

Thermoreflectance measurement is based on the change in light reflected by a material interface as that interface undergoes a change in temperature. Thermoreflectance imaging microscopy records a camera image of the change in light reflected from a device under test as that device is electrically and thermally cycled. The resulting image contains a map of reflectance change across the surface of the device, which is

converted to a map of temperature change using material thermoreflectance coefficient values obtained in a separate experiment calibration process. Measurement produces megapixel images corresponding to the full microscope field of view, showing temperature distribution across the device under test. The method is valid for a broad range of materials used in microfabrication, including most metals and semiconductors. The method is optical and therefore fully non-contact, except for electrical excitation signal applied to the device. No special preparation is required for the device under test. Because the method uses an imaging array sensor, thermal measurement of the full microscope field of view is acquired simultaneously. Consequently thermoreflectance imaging measurements are often obtained in shorter time than methods that require scanning a point sensor across the sample.

This dissertation summarizes four experiment case studies applying thermoreflectance imaging microscopy to characterize self-heating in modern integrated technologies. Chapter 3 explores steady state self-heating in high power silicon transistor arrays. Thermoreflectance imaging of active transistor arrays reveal significant nonuniform temperature distribution over large area structures with complex metal interconnect systems. Hotspot locations are validated against coupled electrothermal simulation. The study demonstrates the effectiveness of thermoreflectance imaging to characterize temperature distribution over large regions of microelectronic structures with complex layout topology. Chapters 4 and 5 emphasize the fast time resolution capabilities of transient thermoreflectance imaging. Chapter 4 focuses on nanosecond and subnanosecond pulsed transient thermoreflectance imaging of self-heating in high speed gallium nitride

based high electron mobility transistors. Measurement revealed significant self-heating temperature gradients between critical HEMT features under megahertz switching conditions. Chapter 5 discusses self-heating in electrostatic discharge (ESD) protection devices. Transient thermoreflectance images revealed non-simultaneous triggering of individual device fingers in the presence of fast, high current simulated ESD pulses. Chapter 6 examines self-heating in nanoscale conducting networks built from disordered silver nanowires with 90 nanometer diameter. This study emphasizes the submicron spatial resolution of thermoreflectance imaging, a capability essential to characterize thermal properties and performance at length scales anticipated in future generation technologies.

1.1 Overview of microscale thermal characterization methods

There are several proven experiment methods for thermal characterization of integrated devices at the micron and submicron length scales. Methods vary greatly in experiment configuration and also in the physical principle employed to accomplish the measurement. Each method provides a unique set of strengths and limitations and it is generally accepted that no single thermal characterization method is ideal for a majority of measurement requirements. Researchers and designers are encouraged to evaluate the available methods and choose the method best suited to the specific test scenario. Often this is accomplished by incorporating multiple techniques that yield complemen-

tary thermal information. The following is a survey of established techniques used in research and industry to measure temperature of integrated structures with micron and submicron spatial resolution. The order of presentation is loosely arranged with methods of high prevalence and general purpose discussed first, followed by methods with increasing specialization or unique application. Many of the methods provide complementary capabilities. Thermoreflectance imaging applications in the context of these alternative measurement options is discussed later in this section.

Electrical methods are among the most common and long-standing techniques for thermal characterization of integrated circuits, used in both research and especially in industry. Electrical methods are based on selection and measurement of a temperature sensitive electric parameter (TSEP). [4] This parameter can be associated with electrical elements inherent to the device under test, for example the temperature dependence of current or voltage in a transistor. Alternatively the TSEP can be associated with an explicit electrical sensor, typically a diode, embedded in the integrated device during fabrication or attached to the chip package for the express purpose of temperature measurement. The electrical test die method [27, 28] extracts absolute thermal resistance, measured from device junction to the device case or package, by means of a diode in thermal contact with the package surface. Temperature is measured from the diode temperature dependence of current for constant voltage, which is calibrated in a separate experimental procedure. The electrical test die experiment apparatus is simple to construct. Temperature measurement is straightforward, repeatable, and easily scales to large numbers of samples. However, the method provides temperature

information only at the location in immediate proximity to the diode sensor, which may not represent the critical temperature of the active junction. Also, the method provides an average temperature of the chip, and cannot observe critical hotspots that may be distributed nonuniformly throughout the structure. [4] A variation on the electrical test die method is to embed diode sensors on the integrated circuit as close to the active elements and junctions as possible during fabrication. This approach can yield more accurate measurement of junction temperature. However embedded diodes require additional consideration at the design stage and fabrication stages, can consume limited chip space, and are not always compatible with the primary function of the integrated device. One key advantage temperature sensitive electrical parameters is that temperature can be measured for package devices, whereas many alternative methods require bare chips or de-capped packages to permit access for optical or scanning probes.

Infrared thermal microscopy imaging is one of the most ubiquitous methods in use for thermal characterization of microstructures. The method measures temperature dependent radiation from semiconductors and metals. Because Planck's law describes temperature dependent spectra for perfect blackbodies, infrared microscopy applies an emissivity scaling factor to compensate for each material's divergence from true blackbody. Early implementations to measure heating in microelectronics scanned fiber probes across the sample surface and collected the signal in an infrared sensitive photodiode [4] (not to be confused with near field optical scanning probes discussed later.) With advances in infrared cameras, commercial imaging systems are now common which capture microscope full field of view thermal images quickly in a relatively

simple measurement procedure. The method is all optical, noncontact, and does not require special sample preparation. Thermal images can be acquired of the top surface of the device or the backside through the chip substrate. Spatial resolution in far-field optical systems is determined by the Rayleigh diffraction limit, d = $\lambda/(2\text{NA})$, where d is the smallest resolvable feature, λ is the radiation wavelength, and NA is the numerical aperture of the lens. Most infrared imaging microscopes operate in the 3µm to 5 µm range, and produce spatial resolution on the same scale. Systems working in near infrared (NIR) wavelengths, 0.8 µm to 3 µm, can achieve spatial resolution of 1 µm. [25] However, near infrared systems are limited to measuring radiation corresponding to temperatures above 500 K, as the signal at these shorter wavelengths becomes too small at lower temperatures. Spatial resolution of 1.4 µm can be achieved by use of a specially fabricated solid immersion lens. [5] Temperature resolution for commercial systems is typically in the range of 50 mK, but 10 µK has been achieved using a lock-in infrared thermal microscope. [6] Transient infrared microscopy imaging has been demonstrated with 20 µs time resolution using internal camera shuttering. [50]

Micro-Raman thermography is a noncontact method based on analysis Raman scattered laser light in semiconductors. [57] Measurement is performed by scanning a focused laser across the device surface and analyzing the location, broadening, and ratio of Stokes and Anti-stokes peaks in the resulting Raman scattered spectrum. The relationship between temperature and phonon frequency information contained in Raman spectra is well documented and has been used extensively to characterize temperature as well as stress in a broad range of semiconductors. Spatial resolution is determined pri-

marily by the size of the focused laser spot and the method of scanning the laser. Spatial resolution of less than one micron has been demonstrated. [19] Temperature resolution is based on experimental calibration of the spectra and accuracy has been reported in the range of 5 K to 10 K [52] for many materials and better for selected semiconductors. Micro-Raman thermography and thermoreflectance imaging provide complementary temperature characterization capabilities. Micro-Raman excels at measuring temperature in semiconductors, including some capacity to measure temperature below the surface, but is unable to measure metals. Thermoreflectance excels at measuring temperature of metals, due to their high reflectance, but can also measure temperature in semiconductors. However, thermoreflectance measures temperature only at reflective interfaces and cannot perform profiling at arbitrary depths in the material. Studies combining micro-Raman thermography and thermoreflectance imaging have been useful in characterizing high speed thermal performance of gallium nitride based high electron mobility power devices. Like thermoreflectance imaging, Micro-Raman thermography can be adapted to measure high speed transient temperature [53] with time resolution of less than 10 ns. [82]

Atomic force microscopy (AFM) has been adapted to measure temperature with state of the art spatial resolution on the scale 1 to 10 nm. Two implementations have proven popular. Scanning thermal microscopy (SThM) measures the temperature induced potential difference (thermovoltage also called Seebeck voltage) between the AFM cantilever tip probe and the sample, [73] or within the tip itself by replacing the single wire tip with a two-wire microfabricated thermocouple tip. [64] The ther-

mocouple tip is brought within 10 nm of the sample surface and scanned laterally to generate both a thermal map and topographical map simultaneously. Improvement in thermocouple tip fabrications has enabled SThM temperature measurement with spatial resolution of 24 nm. [59] A variation of SThM measures electrical resistance rather than thermovoltage. [69, 79]

Scanning Joule expansion microscopy (SJEM) [94] is similar to scanning thermal microscopy, but achieves superior spatial resolution without the need to fabricate an extremely small (1 nm) coaxial thermocouple tip. The technique scans a conventional AFM probe tip across the sample surface and extracts the temperature distribution directly from Joule expansion of the sample in response to a lock-in excitation signal. Spatial resolution is 1nm to 10 nm, similar to AFM. Temperature resolution of 250 mK has been reported. [41] Calibration has been implemented using in-situ resistance-temperature measurement, but the most common calibration method for SJEM uses the known linear thermal expansion coefficient for the material inspected. [10] SJEM is well suited to characterize temperature in nanoscale structures due to its state of the art spatial resolution. Measuring surface displacement is difficult if the sample does not contain a surface layer with high thermal expansion coefficient. [9] Temperature calibration can be challenging for many novel experimental nanomaterials and structures because material thermal expansion coefficients are not always easily obtainable, especially for hybrid nanostructures or nanomaterials with unpredictable thermal expansion dependence on scaling.

Near field scanning optical microscopes (NSOM) [56] replace the force tip or

thermocouple tip with an optical fiber. By bringing the fiber within 1 nm to 10 nm of the sample, spatial resolution is no longer constrained by the far field diffraction limit. Spatial resolution is improved to $\approx \lambda/50$. Spatial resolution is determined by the size of the aperture that can be made on the metal coated fiber tip. Spatial resolution of 12 nm has been reported. [3] NSOM measures temperature using reflectance [39], Raman spectroscopy, or infrared thermometry.

Because of the proximity or direct contact between tip and sample in all scanning probe tip based thermal measurements, it is critical to understand the heat transfer properties between tip and sample. Heat transfer controls spatial and temperature resolution, and measurement artifacts. [63]

Several less frequently used microscale thermal measurement techniques should be mentioned due to their unique approach or capability. Micro-photoluminescence measures the temperature dependence of optically stimulated photon emission in semiconductors. Temperature resolution of 0.2 K for GaAs [42] and several Kelvin for GaN [87] samples are reported with spatial resolution < 5 microns using a scanning far field fiber. For cases where sample preparation is not an issue, temperature sensitive fluorescent thin films applied to sample surfaces can produce thermal images with 10 mK temperature resolution and 1 μm spatial resolution. [51] Nematic liquid crystals applied to the surface of active devices change color or opacity in the presence of temperature change. [16] Temperature resolution of 1 K and submicron spatial resolution has been reported. [2,76] Interferometric temperature mapping measures the real time phase shift in infrared laser illumination as it propagates through the substrate (backside) of device

that experiences self-heating perturbation. [38] This interferometer based method is the only one reviewed that demonstrates the ability to capture images of the self-heating response to a destructive single-shot device excitation. [78] This unique capability was employed to characterize destructive pulses in electrostatic discharge protection devices, and self-heating distribution silicon power transistors and gallium nitride high electron mobility transistors. [54]

1.2 Applications of thermoreflectance imaging microscopy

Thermoreflectance imaging combines several of the advantages of the thermal characterization methods described above. Because it uses source illumination in the visible spectrum, calculated diffraction limited resolution is on the order of 0.2 µm. As will be shown in part 3, practical spatial resolution in thermoreflectance images can be less than 0.1 µm. Excellent temperature resolution of 10 mK [68] is achieved by averaging the measurement over multiple device excitation cycles, which usually requires only a few minutes. The method is optical and noncontact, and requires no special sample preparation. Transient thermoreflectance imaging has been demonstrated with 50 ns [60] and subnanosecond [62] time resolution. Due to its capabilities and relatively simple measurement procedure, thermoreflectance imaging has been used in thermal studies of a broad range of integrated microscale devices in recent years. With commercial thermoreflectance imaging systems now available, adoption of the tool in research and industry is likely to increase. Farzeneh conducted a review of thermoreflectance

imaging applications in 2009. [34] The following section describes seminal thermoreflectance imaging studies and provides examples of application to thermal inspection and analysis across a diverse range of devices.

Ju, Goodson, et al., 1997, first demonstrated thermoreflectance temperature mapping using a scanning implementation to inspect self-heating in LDMOS transistors. [47] Grauby, et al., 1999, demonstrated the first thermoreflectance imaging configuration to combine a microscope and charge coupled device (CCD) camera to record images of temperature change on an integrated structure without scanning a probe sensor. [40] This study used a heterodyne stroboscobe illumination scheme to measure amplitude and phase of self-heating in a transistor being operated at frequencies (MHz) far above the frame rate of the camera (200 Hz). Tessier, et al, 2001, determined optimal illumination for thermoreflectance of three different resistors consisting of metal and semiconductor materials. [93] Luerssen et al., 2005, experimentally demonstrated temperature resolution of 10 mK using a 12-bit CCD camera to image self-heating temperature distribution in polycrystalline solar cells. [58] Burzo, Raad et al, 2005, demonstrated transient thermoreflectance CCD imaging with microsecond time resolution to inspect self-heating in silicon field effect transistors. [7] Parasitic effects influencing calibration of the thermoreflectance coefficient, such as defocusing of the microscope objective, are discussed. Fast self-heating in silicon based electrostatic discharge protection circuits in response to 100 ns pulses were mapped across device surface by Freitas et al., 2005, using a scanning thermoreflectance probe. [23] Thermoreflectance imaging has been effective for heterostructure semiconductor characterization. Chan et al., 2006, imaged

temperature distribution in SiGe bipolar transistors. [14]

Cooling distribution in micro-thermoelectric coolers was imaged by Christofferson et al., 2007, using a custom analog high frequency thermoreflectance PIN array camera. [21] With the appropriate thermoreflectance algorithm, cooling and heating can be measured simultaneously in the same image. Christofferson et al., 2009, measured transient cooling and heating over the first 500 ns to 1 ms for a 50 x 50 micron SiGe superlattice thermoelectric microrefrigerator. [31]

Thermoreflectance imaging of optoelectronic and photonic structures is possible for both electrical and optical device excitation. Thermoreflectance imaging has been used to characterize quantum dot lasers [12], high power semiconductor lasers [13], and vertical cavity surface emitting lasers [33]. Summers et al., 2010, measured temperature in semiconductor optical amplifiers on photonic integrated circuits to calculate the optical power distribution during operation. [91] Kendig, et al., 2010, used a combined simultaneous thermoreflectance and electroluminescence imaging to detect distribution of hotspots indicating location of shunt defects in photovoltaic cells. [48]

Experimentally acquired information from thermoreflectance imaging can extend fast simulation and verification models. Temperature measurement can provide missing simulation parameters. Inverse heat methods can use temperature maps to calculate power distribution. Raad et al., 2008, calculated the thickness of a silicon dioxide passivation layer and other 3D geometric features based on thermoreflectance images. [80] Thermoreflectance temperature maps have been used to estimate critical material parameters such as thermal conductivity. [61, 81]

Chapter 2

Thermoreflectance imaging microscopy - experiment method and apparatus

Key features of thermoreflectance imaging microscopy include submicron spatial resolution, fast time resolution (50 ns and 800 ps,) 10 mK temperature resolution, and an all optical, non-contact measurement procedure. [7, 47, 93] Thermoreflectance imaging is part of an expanding set of experiment characterization methods, including micro-Raman spectroscopy [67, 88] and infrared imaging, that have proven useful in thermal metrology for a broad range of microelectronics and novel materials.

Thermoreflectance measurements are based on the change in light reflected by a material surface or interface for a change in its temperature. For integrated electronic devices and structures, this temperature change can be induced via self-heating in response to an applied external electrical excitation. The concept is illustrated in Figure 2.1. Thermoreflectance imaging microscopy combines an optical microscope and

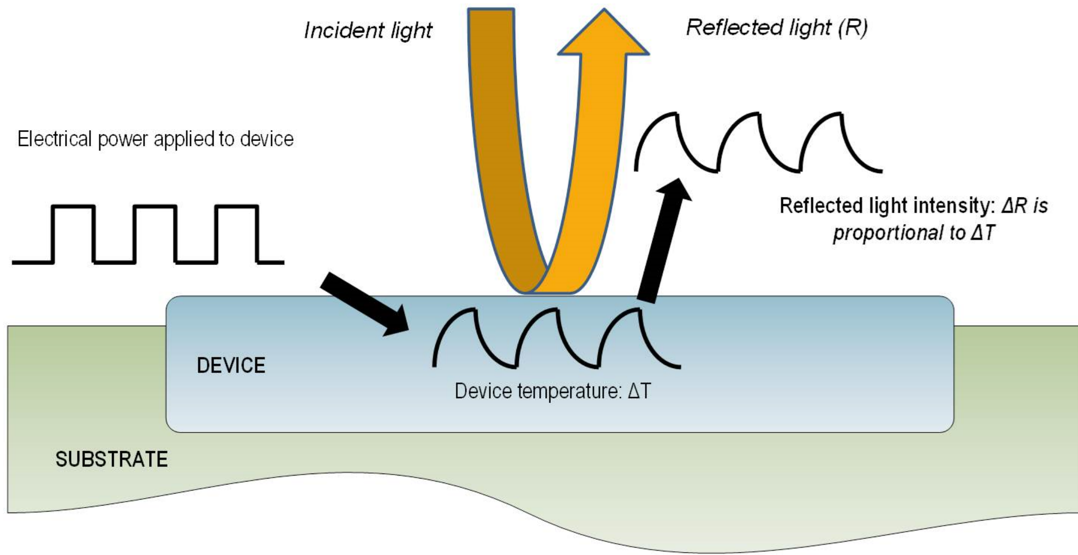

Figure 2.1: Thermoreflectance characterization records the small change in light reflected by a device material surface due to device self-heating. Self-heating is induced by electrical excitation applied to the device.

integrated imaging camera (usually a charge coupled device, CCD) to record the change in light reflected from a device under test as that device is electrically and thermally cycled. The change in reflected light is converted to temperature change using calibration values obtained in a separate experiment process. The measurement produces megapixel thermal images of the device under test as captured in the field of view in the microscope.

Figure 2.2 shows an example experiment configuration for thermoreflectance imaging. The device under test (DUT) is placed under a reflectance microscope with normal incident illumination provided by a narrowband source, typically a light emitting diode or laser. A periodic electrical excitation signal is applied to the device under test, which induces a periodic change in surface temperature, ΔT, and corresponding change

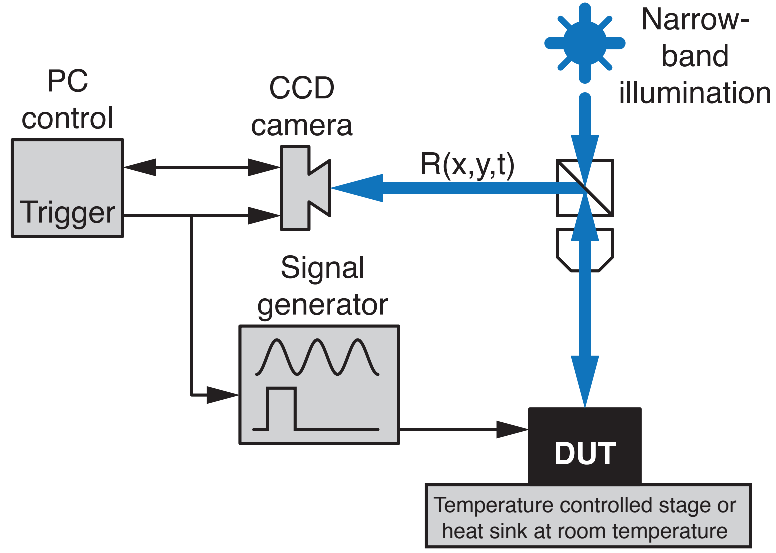

Figure 2.2: Example thermoreflectance imaging experiment configuration.

in reflectivity, ΔR, due to device self-heating. If R_0 is the intensity of light reflected from the sample surface for a given temperature T_0, then the normalized change in surface optical reflectivity can be described by [84]:

$$\frac{\Delta R}{R_0} = \frac{1}{R_0}\frac{dR}{dT}\Delta T. \tag{2.1}$$

The value $\Delta R/R_0$ is the thermoreflectance change or thermoreflectance amplitude. Typical magnitudes of $\Delta R/R_0$ are on the order of $10^{-5}\,\mathrm{K}^{-1}$ to $10^{-4}\,\mathrm{K}^{-1}$. An image of device surface thermoreflectance change is recorded by a CCD camera attached to the microscope. To extract the small magnitude of thermoreflectance change from background noise, the thermoreflectance change image is averaged over many continuous device thermal excitation cycles at a selected frequency. This method of extracting small amplitude signals from background noise by means of exciting the system with an external

frequency is often called “lock-in” amplification. The thermoreflectance image is then converted to a map of device surface temperature by scaling each material region in the image by its corresponding material thermoreflectance response:

$$\Delta T = \frac{1}{C_{TH}} \frac{\Delta R}{R_0} \tag{2.2}$$

$$C_{TH} = \frac{1}{R_0} \frac{dR}{dT}, \tag{2.3}$$

where the scaling factor $C_T H$ is called the thermoreflectance coefficient. In this report, the term “thermoreflectance image” will be used interchangeably to refer to images presented in either units of temperature change (K) or raw thermoreflectance change. Material thermoreflectance has nonlinear temperature dependence, but can be approximated as linear for temperature changes of less than 100 K. Thermoreflectance also varies with the wavelength of incident illumination. Choosing an optimum incident illumination wavelength for a given material can substantially improve thermoreflectance amplitude. For example, gold has significant thermoreflectance peaks for incident illumination centered at 530 nm (green) and 470 nm (blue). [58] Thermoreflectance imaging is particularly well suited to measuring the temperature of gold and other metals commonly used as interconnects and electrodes in integrated structures. Thermoreflectance coefficients for each material on the sample must be determined experimentally. The experiment calibration procedure is described later in this section.

2.1 Calculation of thermoreflectance amplitude

Several methods have been implemented to measure the small amplitude of thermoreflectance change in a device under excitation. This study used two approaches: a fast Fourier transform (FFT) algorithm for measuring self-heating at low frequency or effective thermal steady state, and a pulsed differential algorithm for measuring fast transient self-heating. These two algorithms are discussed next.

2.1.1 Low frequency thermoreflectance imaging - fast Fourier transform algorithm

Figure 2.3 shows a schematic representation of timing signals used in the fast Fourier transform (FFT) thermoreflectance algorithm. Probe illumination is continuous and at constant intensity. Sinusoidal voltage or current at a preselected lock-in frequency, F, is applied to the device under test. Joule heating, for example produced by resistors, induces reflectance oscillation at $2F$. Peltier heating or cooling, produced by devices with thermoelectric properties, induces reflectance oscillation at F, the same frequency as device electrical excitation. The CCD camera records images of the thermoreflectance signal for a preselected acquisition time period, approximately 5 s, and camera frame rate (20 frames per second to 200 frames per second). For the FFT algorithm, the camera frame rate determines the effective sampling rate for a given time series of data. After each acquisition period, the system hardware computes the fast Fourier transform of the image series and calculates the amplitude and phase of ther-

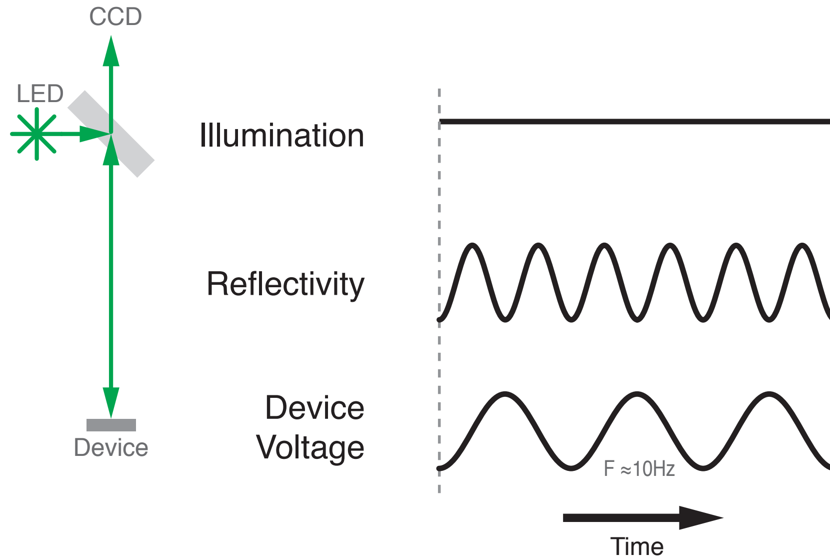

Figure 2.3: Schematic representation of timing signals used in low frequency, fast Fourier transform thermoreflectance algorithm. Probe illumination is constant. Device is excited with a sinusoidal voltage or current at low frequency lock-in frequency, typically 5 Hz to 20 Hz. Corresponding reflectance signal can be at F for Peltier heating or $2F$ for Joule heating.

moreflectance change. The result is a pixel for pixel map of thermoreflectance change across the device surface. Joule heating or Peltier heating (if present) is inspected by specifying the appropriate frequency to be analyzed at the start of image acquisition. Cumulative averaging of the thermoreflectance image over multiple acquisition periods improves signal to noise and corresponding temperature resolution. Clear images with temperature resolution of approximately 50 mK can be obtained for averaging duration of ten minutes or less for most materials.

The maximum lock-in excitation frequency for the FFT algorithm is Nyquist limited by the maximum sampling rate of the CCD camera. For the thermoreflectance imaging measurements discussed in part one of this thesis, the maximum FFT lock-

in frequency was approximately 100 Hz. Though faster scientific grade cameras are available, there is often a trade off between speed and light sensitivity. With this upper bound on the FFT lock-in excitation frequency, the FFT method in our studies was reserved for scenarios when only the device steady state thermal response was of interest. Steady state self-heating distribution in power transistor arrays is the subject of part one of this thesis. Complete details of the experiment FFT thermoreflectance imaging acquisition parameters used in that study are presented along with results.

2.1.2 Fast pulsed transient thermoreflectance imaging - differential algorithm

Measuring fast transient thermal response of microscale devices is useful for analyzing performance and understanding critical time dependent temperature dependent parameters. The transient thermoreflectance imaging method used for measurements discussed in this thesis is capable of subnanosecond time resolution. The technique is well suited for imaging ultra-fast thermal effects in microscale devices. Like the FFT method, pulsed transient imaging extracts the thermoreflectance amplitude by cumulative averaging over a periodic lock-in frequency. However, time resolved thermoreflectance imaging is achieved by switching to a pulsed measurement scheme. The sinusoidal device excitation signal and continuous illumination signal used in the FFT method are both replaced with low duty cycle square pulse signals.

Figure 2.4 shows the relationship between device excitation and illumination timing signals for one period at the transient thermoreflectance lock-in frequency. The

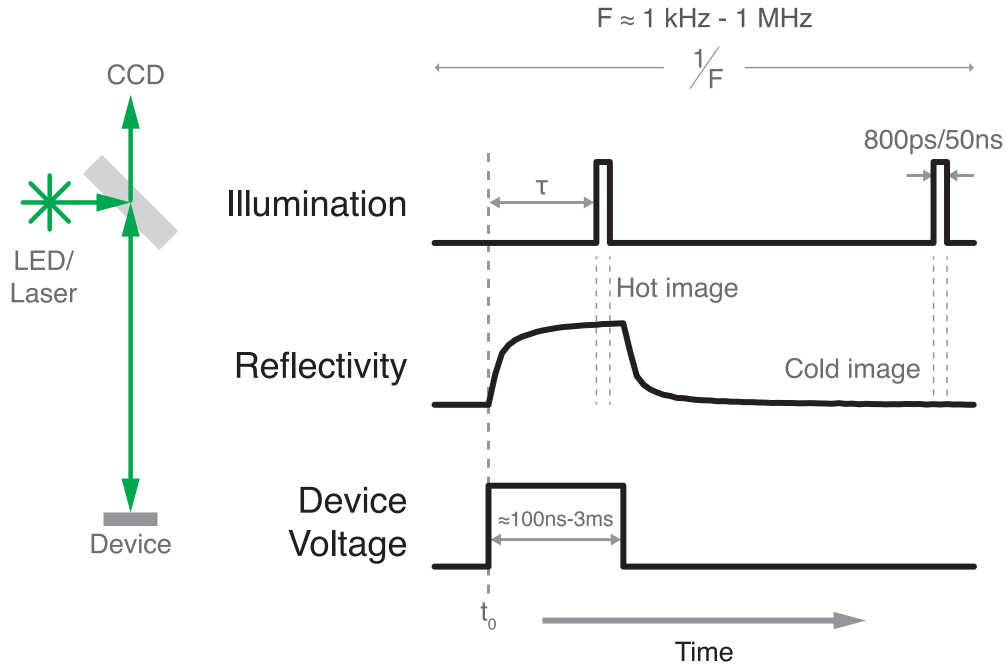

Figure 2.4: Transient thermoreflectance imaging timing signals. There is one low duty cycle electrical and illumination pulse per lock-in excitation cycle. Lock-in frequency selected to allow device fast thermal transients to return to steady state during each cycle. Full device thermal transient acquired by sweeping delay, τ, of illumination pulse relative to device pulse. Thermoreflectance change calculated by difference between "hot" and "cold" images. Hot and cold images are acquired in alternate cycles, but shown in same cycle in the figure for illustrative purposes.

bottom waveform represents the square voltage pulse applied to the HEMT. The middle waveform represents the change in device reflectance in response to the power pulse. The top waveform represents the measurement illumination pulse, provided by either narrowband pulsed light emitting diode (LED) or pulsed laser. In transient thermoreflectance imaging, the light pulse can be viewed as the equivalent of an exposure shutter in a conventional imaging system. The CCD camera records reflectance data only when the LED pulse is on. By choosing a light pulse that is shorter in duration than the device pulse, and adjusting the delay, τ, of the light pulse relative to the rising edge of the

device pulse, the system can measure temperature change for individual time segments and reconstruct the thermal heating and cooling transients. Unlike the FFT method, transient imaging calculates the magnitude of thermoreflectance change directly from the difference of a "hot" and "cold" image. The first light pulse shown in the cycle represents the hot frame. The second light pulse, corresponding to acquisition of the cold frame, is delayed until just prior to the subsequent device excitation pulse, which corresponds to the time at which the device is at its coolest in a given excitation cycle. Data for the hot and cold images are acquired in alternate pulse trains, though both are shown in the same cycle in Figure 2.4 for illustrative purposes. A thermoreflectance change image is calculated from the difference of hot and cold images every five seconds. As with the FFT method, temperature resolution of 50 mK can be obtained in ten minutes for most materials. Minimum transient time resolution is determined by the minimum light pulse width that can be achieved. Until recently minimum time resolution for the configuration used in this study was 50 ns, constrained by the pulse characteristics of commercially available power LEDs. Recently an ultra-fast transient thermoreflectance system based on a Picoquant 800 ps pulsed 440 nm solid state laser demonstrated transient imaging with subnanosecond time resolution. Chapter 4 discusses ultra-fast pulsed self-heating in gallium nitride high electron mobility transistors based on transient thermoreflectance imaging using both 50 ns and 800 ps time resolution systems.

Because the transient lock-in repetition rate is on the order of 1 kHz to 1 MHz, it should be noted that the sample and heat sink do not reach complete thermal equilib-

rium between excitation pulses. Consequently, the choice of transient thermoreflectance lock-in frequency will determine the bandwidth of thermal transients included in the measurement. For lock-in pulse repetition rates of 1 kHz to 100 kHz and duty cycles between 5% to 20%, device thermal transients that are faster than approximately 100 µs will relax completely between excitation cycles and be recorded in the thermoreflectance measurement. Slower background transients such as die, heat sink, and ambient temperature transients will be rejected by the measurement. Consequently, by using square pulse widths significantly longer than the thermal rise time of critical features on the device, transient thermoreflectance imaging can be used to characterize device thermal response from very early in the transient out to "quasi" thermal steady state.

2.2 Experiment calibration of material thermoreflectance coefficients

The output from a thermoreflectance imaging measurement is a matrix of pixels containing the raw amplitude of reflectance change, $\Delta R/R$, for the device during excitation. This image is converted to a map of temperature change, ΔT, across the device by scaling with appropriate material thermoreflectance coefficients, C_{TH}. Because thermoreflectance coefficients vary considerably between materials and also with the wavelength of the source illumination, published thermoreflectance coefficient values are rarely available for novel integrated microelectronics. A separate experiment calibration procedure is generally required. The calibration procedure is very similar to

thermoreflectance imaging.

Figure 2.5 shows the in-situ experiment setup used to extract material thermoreflectance coefficients for arbitrary device samples. Ideally, thermoreflectance imaging and calibration are performed on the same sample, but this is not required as long as the materials in the imaging sample are identical to the materials of the calibration sample. Calibration chips should be 1 mm thick or less. The chip is fixed to a 200 µm thick bismuth telluride thermoelectric (TE) module which serves as a fast heating stage with Peltier (linear) temperature change versus current behavior. The TE stage is typically 5 mm to 10 mm along a linear dimension, so the calibration chip should be of similar dimensions to ensure it fits on the calibration stage. A 25 micron micro-thermocouple is placed in contact with the top surface of the calibration chip. The remaining experiment components–optical microscope, external illumination LED or laser, driving instruments and computer interface–are identical to the standard thermoreflectance imaging experiment configuration. During calibration the TE module current is cycled with a low frequency periodic reference signal, which produces an oscillating temperature signal in the range of 0.1 Hz to 2.0 Hz. The TE module temperature signal induces a corresponding low frequency temperature oscillation distributed uniformly in in plane (the x-y direction) over the calibration chip. No electrical excitation is applied to any device on the chip during thermoreflectance calibration. The amplitude of temperature change on the chip was recorded by the thermocouple. Because the calibration chip is heated uniformly in plane by the TE module, the temperature change at the location where the thermocouple contacts the chip can be assumed to represent the temperature change at

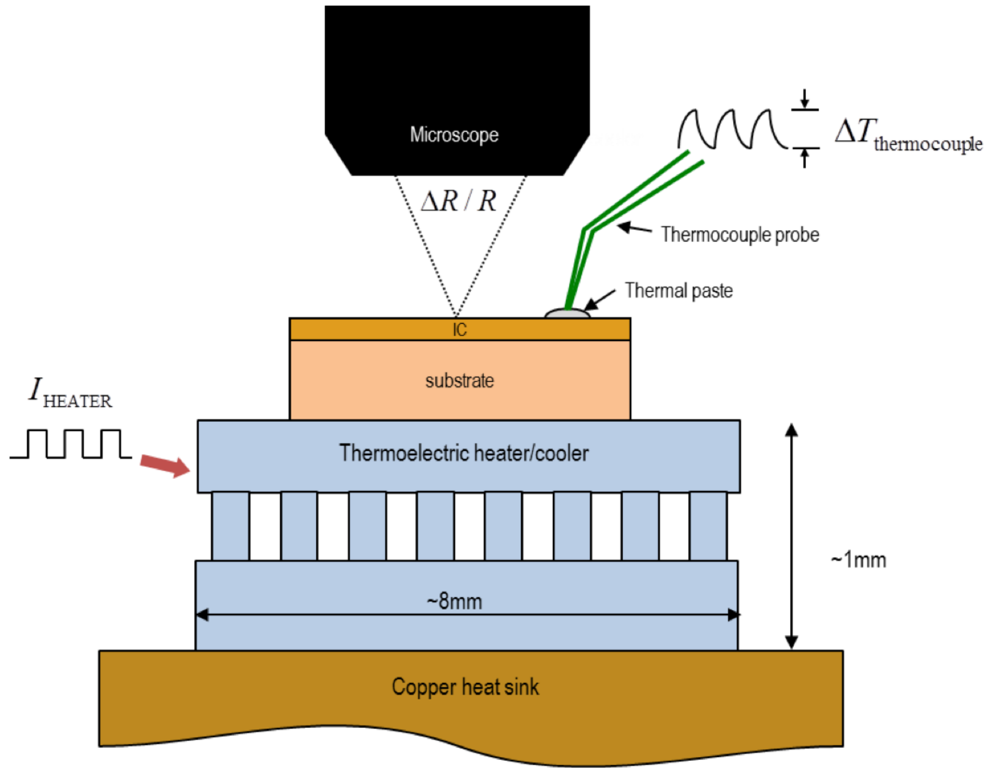

Figure 2.5: In situ experiment configuration for calibration of sample material thermoreflectance coefficients (C_{TH}).

any x-y location across the chip surface within some small variance. Spot thermocouple measurements at the four corners and center of the calibration chips showed a 3% variation in chip temperature change amplitude during calibration procedures. A CCD camera simultaneously records a calibration image of the thermoreflectance amplitude over the full chip. All instruments are controlled by a Sanjview program to synchronize chip heating and CCD acquisition of the calibration image.

Several timing algorithms have been proposed for acquisition of thermoreflectance CCD calibration images. Calibration results in this thesis were obtained using a low frequency differential method that allows the TE stage and sample to reach steady

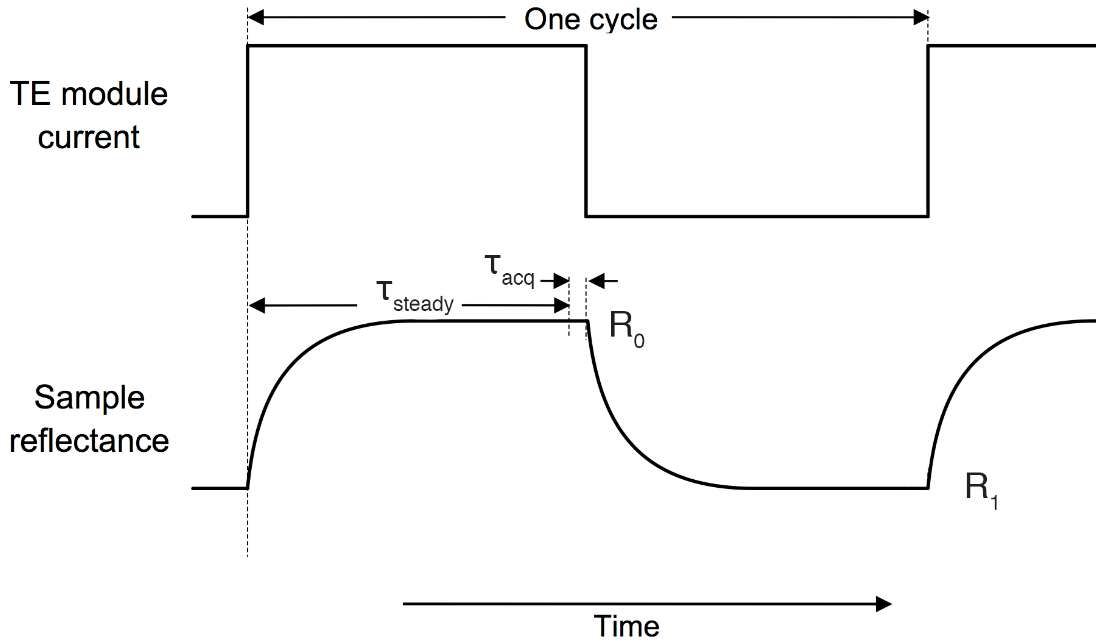

Figure 2.6: Differential thermoreflectance calibration timing diagram showing one cycle of excitation. Camera records steady state hot, R_0, and steady state cold, R_1, calibration reflectance values after time = τ_{steady} into the heating and cooling transients for the calibration sample. Typical values of τ_{steady} and τ_{acq} are 20 s and 2 s. Material thermoreflectance coefficients are calculated from the reflectance change measured by the camera and temperature change measured by the micro-thermocouple.

state "hot" and "cold" temperature for each cycle. Figure 2.6 shows the timing diagram for differential thermoreflectance calibration. Excitation frequency for each the calibration chip was selected from trial and error inspection of the temperature change as read by the thermocouple. First, a half-cycle duration was found that permitted the calibration chip to reach steady state temperature, τ_{steady}. Then a short duration, τ_{acq}, was chosen for camera acquisition of the reflectance values during hot steady state, R_0, and cold state, R_1. Typical durations for τ_{steady} and τ_{acq} were 20 s and 2 s respectively, for a total calibration signal period of 44 s or calibration frequency of approximately 0.02 Hz. Similar to thermoreflectance imaging, a the thermoreflectance amplitude im-

age $(R_0 - R_1)/R_0$ was calculated for each period, and a cumulative or running average of this image was performed until the desired signal to noise was achieved. For all results presented, calibration was performed with the heat sink at ambient room temperature (297 K). Typical magnitudes for the calibration chip temperature change were on the order of 10 K, as measured by the micro-thermocouple. The magnitude of temperature change chosen for the calibration procedure is not significant, provided that it exceeds the minimum resolution of the micro-thermocouple and does not exceed the range over which the thermoreflectance coefficient can be approximated as linear. Unfortunately, published data regarding C_{TH} temperature dependence is very limited. No significant nonlinearity was observed for any thermoreflectance coefficient versus temperature over the range 300 K to 400 K for source illuminations of 530 nm, 470 nm and 455 nm. Detailed analysis of the temperature dependence of thermoreflectance coefficients in the visible spectrum has been proposed for future study.

Thermoreflectance coefficients, C_{TH}, for selected material regions were extracted from the calibration images. This was done by selecting a rectangular region of pixels in the acquired calibration image corresponding to homogeneous material, calculating the median normalized reflectance change amplitude, and dividing by the chip temperature change as measured by the micro-thermocouple during the calibration procedure. Material thermoreflectance coefficients, including standard deviation of pixel values and estimates corresponding temperature resolution is given for each case study discussed.

Part II

Case Studies

Chapter 3

Steady state self-heating in silicon power transistor arrays

3.1 Abstract

Thermoreflectance imaging with high spatial resolution is used to inspect self-heating distribution in active high power (4 A) MOSFET transistor arrays designed for high frequency (MHz) operation. Peak temperature change and self-heating distribution is analyzed for both low and high DC bias cases and for different ambient die temperatures (296 K to 373 K). Thermoreflectance images reveal temperature nonuniformity greater than a factor of two over the full area of the transistor arrays. Thermal nonuniformity is revealed to be strongly dependent on both bias level and ambient die temperature. Verification based on the fine grain power dissipation in the transistor array was performed using the R3D method for electrical simulation and Power Blurring

for thermal simulation. Results demonstrate thermoreflectance imaging as an effective tool for fast, submicron, noncontact thermal characterization of active power devices.

3.2 Introduction

Performance and reliability in fast switching, high power integrated semiconductor transistors are strongly related to the peak temperature in the device. It has been shown that temperature distribution in power devices is generally not spatially uniform. [15, 75, 89, 90] For power transistors with large areas or arrayed layouts current is often distributed nonuniformly throughout the device, giving rise to regions of increased self-heating or local hot spots. These local temperatures strongly influence the rated electrical safe operating area (SOA). Consequently, an analysis of the thermal performance and reliability of large area and arrayed power semiconductor designs should consider not only the average temperature of the structure but also the spatial distribution of hot spots.

This study presents thermoreflectance image measurements of steady state surface temperature distributions for large area (to 0.7 mm^2) silicon power transistor arrays based on the metal-oxide-semiconductor field effect transistor (MOSFET) design. Two-dimension temperature maps of the active power arrays are obtained using a lock-in thermoreflectance camera imaging system capable of submicron spatial resolution and 50 millikelvin temperature resolution. Thermoreflectance imaging results compare self-heating in the power transistor arrays for drain current to four amperes and current

density to 47 milliamperes per millimeter of gate width.

Thermoreflectance image measurements presented here study two factors affecting self-heating in the transistor array: electrical bias and ambient die temperature. Thermoreflectance images at low and high DC electrical bias (current densities of 12 and 47 milliamperes per millimeter gate width respectively) reveal different self-heating magnitude as expected, but also display significant change in spatial temperature distribution across the transistor array. Thermoreflectance images of the active transistor array for ambient die temperatures 296 K, 333 K and 373 K with DC electrical bias held constant reveal an increase in average total device self-heating and also increase in temperature nonuniformity across the array.

3.3 Experiment method

Thermal images and temperature profiles of the power transistor arrays and adjoining chip area surface were acquired using thermoreflectance imaging. [7,47,68,93] This non-contact method measures the change in material surface optical reflectance for a change in temperature. Figure 3.1 illustrates the thermoreflectance imaging experiment setup. The topside of the unpackaged power transistor array chip is illuminated under a reflectance microscope using a narrow-band light emitting diode (LED) source in the visible spectrum. The transistor array is excited by a reference or lock-in square wave voltage signal, V(t), at 10 Hz. This applied bias signal induces a time varying temperature in the transistor array and corresponding time dependent oscillation in reflected

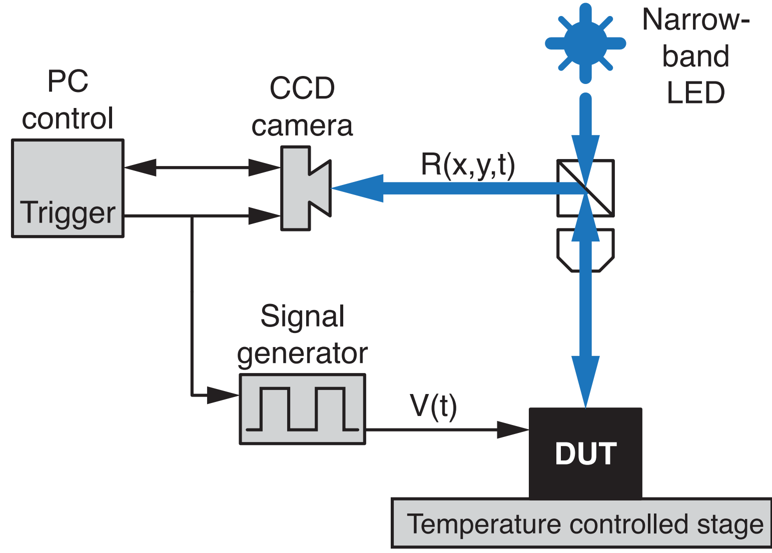

Figure 3.1: Experiment configuration for steady state thermoreflectance imaging of LDMOS transistor arrays.

light intensity across the transistor array surface. This reflectance signal, $R(x, y, t)$, is recorded on a variable frame rate, high dynamic range Andor charge coupled device (CCD) camera with 128×128 pixel resolution. Fourier analysis of the time varying reflectance signal at the lock-in frequency produces a pixel-for-pixel map of the amplitude of thermoreflectance change, $\Delta R/R$, across the transistor array surface. Camera operation and device excitation timing is controlled by a unified SanjVIEW program and custom designed hardware trigger board.

Theoretical minimum temperature resolution of 50 mK precision is achieved by recording the cumulative average thermoreflectance change amplitude on the sample surface over continuous device excitation cycles. [68] The observed temperature resolution of the thermoreflectance system used in this experiment was 70 mK. This value was obtained by measuring the temperature change of the device when no electrical

excitation is supplied. The resulting "noise floor" amplitude represents the system's experimental minimum temperature resolution. Thermoreflectance images in this study were averaged for 10 minutes with device at 10 Hz excitation bias. Choosing measurement illumination in the visible spectrum with high microscope objective numerical aperture yields submicron spatial resolution (compared to 10 µm spatial resolution for IR emissivity thermal imaging.) For this experiment a 20X magnification lens with 0.4 numerical aperture was used to ensure the full length of the transistor array was visible in the camera's field of view. In this configuration, the pixel resolution is 1.4 µm. With 455 nm source illumination, the diffraction limited resolution is about 200 nm to 300 nm.

Raw thermoreflectance change images were converted to image maps of temperature change across the device surface in units Kelvin using experimentally calibrated material thermoreflectance coefficients, C_{TH}, for the transistor array. Experimental calibration of sample material thermoreflectance coefficients was achieved using an external heat modulation technique. In this method the sample chip is thermally fixed to a fast, 3 mm thick thermoelectric heat stage. The heat stage externally cycles chip temperature (relative to ambient room temperature) using a sinusoidal lock-in signal of frequency 1 Hz and amplitude 10 K. Devices on the chip are electrically inactive during calibration. Because there is no device self-heating, the external heat stage produces an oscillating temperature signal that is uniform across the full surface of the sample chip. The amplitude of the chip's surface temperature signal, ΔT, is measured directly by a microthermocouple (with tip diameter 25 µm) placed on the chip surface. A simultaneous calibration image records the amplitude of thermoreflectance change $\Delta R/R$ on the

chip surface. The ratio $C_{TH} = (\Delta R/R)/\Delta T$ gives thermoreflectance coefficient values for all sample materials visible in the calibration image. Values of the experimentally calibrated thermoreflectance coefficients for the transistor array materials are discussed with results.

All measurements were performed on bare, unpackaged dies, excited with electrical probes. Gate voltage was held constant at 10 volts for all measurements. Drain-source voltage was a 10 Hz square wave, assigned positive offset to ensure the peak of the signal was equal to V_D and the trough was equal to 0V. Thermoreflectance images were obtained with V_D amplitude selected between 0.5 V to 5.0 V to observe the thermal response in the transistor array at different current densities. To measure device heating at thermal steady state, a lock-in excitation frequency must be selected that permits the device to reach thermal steady state (both hot and cold) during each excitation pulse. Two separate methods were used to ensure the transistor array was in thermal steady state during thermoreflectance measurement. First, direct microthermocouple point measurements were obtained on the silicon at the source end of the slowest (3175 micron long) transistor array. The microthermocouple time varying temperature waveform (observed on oscilloscope) revealed the transistor array to be in thermal steady state for an excitation frequency of 10 Hz. Second, thermoreflectance images of the 3175 micron array were compared for excitation frequencies of 10 Hz and 5 Hz. The difference in thermoreflectance temperature change for these two frequencies was on the order of the minimum system resolution (70 mK.) This implies device self-heating changed by a maximum of nine percent for a doubling of excitation pulse width. This condition is

consistent with thermal steady-state. For measurements comparing device self-heating at low and high bias, the die backside was fixed to a solid copper heat sink with thermal paste. External chip temperature was maintained at room temperature. For measurements comparing device self-heating as a function of external temperature, samples were thermally bonded to an aluminum temperature controlled hot plate and thermal images were acquired for three external sample temperatures: $T_{EXTERNAL} = 296\,K$, $333\,K$ and $373\,K$. High conduction probe tips were used to minimize joule heating at contact pads.

Numerical simulation of both electrical power spatial distribution and temperature change spatial distribution at steady state were performed and compared to thermoreflectance temperature change measurements for the active transistor arrays. Electrical power simulation was performed using the R3D method. [29] Temperature change simulation based on the simulated power distribution was performed using the Power Blurring method. [97, 98]

3.4 Device description

Modern communication and "smart power" applications have created strong demand for power devices capable of high frequency (MHz-GHz) switching with high current compliance. One design that meets this dual requirement incorporates large arrays containing many small, intrinsically fast transistors connected in parallel. Driving all of the underlying individual transistors in this design often requires complex interconnect metal systems. Dense interconnect routing can result in nonuniform current

and temperature distribution during operation. The power structures in this study (Figure 3.2) consist of arrays of parallel connected transistors fabricated on a silicon process. Total planar active areas range between 0.28 mm^2 to 0.7 mm^2. The arrays are designed for high voltage (50 V) and high current (up to 6 A) operation at 10 MHz frequency. Intrinsic transistor layout is based on the diffused channel metal-oxide-silicon (DMOS) design illustrated in Figure 3.2c. DMOS transistors employ a diffused or "stacked" conducting channel grown parallel to the plane of the wafer to enable relatively high current per unit area while still being capable of fast switching. [92] The lateral diffused version (LDMOS) exhibits low on-resistance due to a combination of short channel length and additional lightly doped region between channel and drain contact. The power array units in this study consist of LDMOS transistors.

Gate width is 100 microns per transistor unit. Sets of 15 parallel FETs are connected in rows or "cells." Cells are connected in parallel to create an array with the desired size, total gate width, and current compliance. Measured along the long axis of the transistor array the shortest array is 1270 microns (50 mil) and has 12 parallel cells for a total effective gate width of 36 millimeters. The longest array is 3175 microns (125 mil) with total gate width of 90 millimeters. The source and drain of each intrinsic transistor in the array is accessed by a planar metal interconnect system of aluminum fingers and vias isolated by oxide insulation layers (Figure 3.2b.) The top aluminum source finger is common to the source contact of each intrinsic FET in the underlying array. Similarly, the top drain finger connects all drains in the transistor array. The top source and drain fingers are each 115 microns wide and the total distance along the

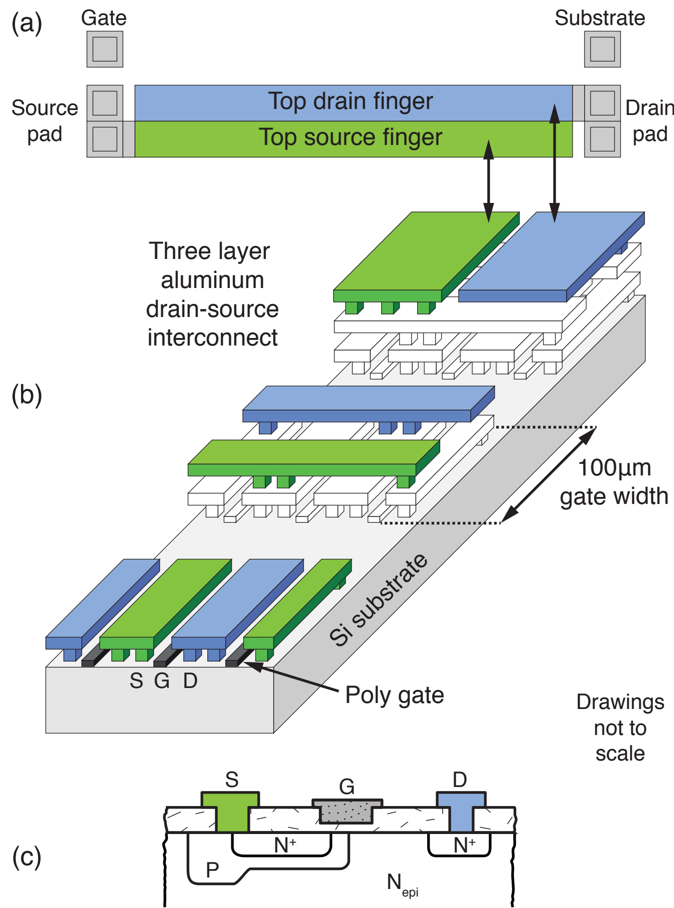

Figure 3.2: (a) Top view of power transistor array with top source and drain fingers indicated. (b) Layout of three rows in the LDMOS array showing intrinsic transistors at the silicon level and the three layer aluminum drain-source interconnect system. Gate width per individual transistor is 100 microns. (c) Cross section of a single lateral diffused channel MOSFET.

short axis of each transistor array is 250 microns. The gates of the intrinsic transistors are connected by patterned poly silicon. Gate, drain, source, and substrate contact pads are located at the ends of the array (Figure 3.2a.) The test sample die size was 8 mm × 22 mm with a 500 micron thick silicon substrate.

Experimentally calibrated thermoreflectance coefficients, C_{TH}, were acquired

for two material regions on the sample die: the top aluminum layer of the LDMOS interconnect, and the silicon substrate adjoining the transistor array. Thermoreflectance coefficient values were calculated from the mean value of a 30×30 rectangular pixel region (70 square microns) in the thermoreflectance calibration image corresponding to the aluminum and silicon regions respectively. Experimental calibration produced $C_{TH,Al} = 5.8 \times 10^{-5}\,K^{-1}$ and $C_{TH,Si} = 9.1 \times 10^{-5}\,K^{-1}$. The standard deviation of thermoreflectance values within the 30×30 pixel sampling region provides an indirect estimate of material roughness. One standard deviation was $2.0 \times 10^{-3}\,K^{-1}$ for the aluminum region and $4.1 \times 10^{-6}\,K^{-1}$ for the silicon region. The large standard deviation in thermoreflectance pixel values for the calibrated aluminum region is due to its optical roughness, the result of coarse sputtering deposition and subsequent etching of the passivation. The smoother silicon provides much better precision in the thermoreflectance measurement, consequently all thermoreflectance CCD images in this report are calibrated for temperature change on the silicon region only and all temperature change values reported are for the silicon region immediately adjoining the metal.

3.5 Results

3.5.1 Self-heating dependence on bias level

Thermoreflectance images of the LDMOS transistor array were obtained at both low and high bias to study the influence of drain-source voltage and current density on self-heating in the power array. Gate voltage was 10 V for both low and high

bias measurements. Chip external temperature was maintained at room temperature. The low bias case ($V_D = 0.5\,V$) corresponds to operation in the quasi-linear region of the power transistor arrays I-V, while the high bias case ($V_D = 5.0\,V$) represents the transistor in saturation operation. Figure 3.3a shows the CCD image of the 3175 micron long LDMOS transistor array. Top layer aluminum metallization drain and source fingers are indicated. The bright colored squares along the left half of the source finger and right half of the drain finger indicate regions where SiN passivation was removed to test electrical performance at different probing locations. For the thermal measurements in this study, electrical probing was applied at the source and drain contacts at the extents of the array.

3.5.1.1 Self-heating at low bias

Figure 3.3b shows the thermoreflectance image for the 3175 micron long LDMOS power transistor array at low bias. Drain voltage was 0.5 V and drain current was 1.0 A, producing channel current density of $12\,mA/mm_{GATE\ WIDTH}$. Total power in the transistor array for this bias was 550 mW with surface area power density of $69\,W\,cm^{-2}$. Current flowing through the source/drain interconnect network and through the intrinsic transistors causes Joule heating, which can be seen to spread laterally into the adjoining substrate. The thermoreflectance image is calibrated for temperature change on the silicon region only. The corresponding plot shows the thermoreflectance temperature change profile (L-L') parallel to the long axis of the array for low bias. The profile was taken on the silicon adjoining the source finger. Temperature distribution in the

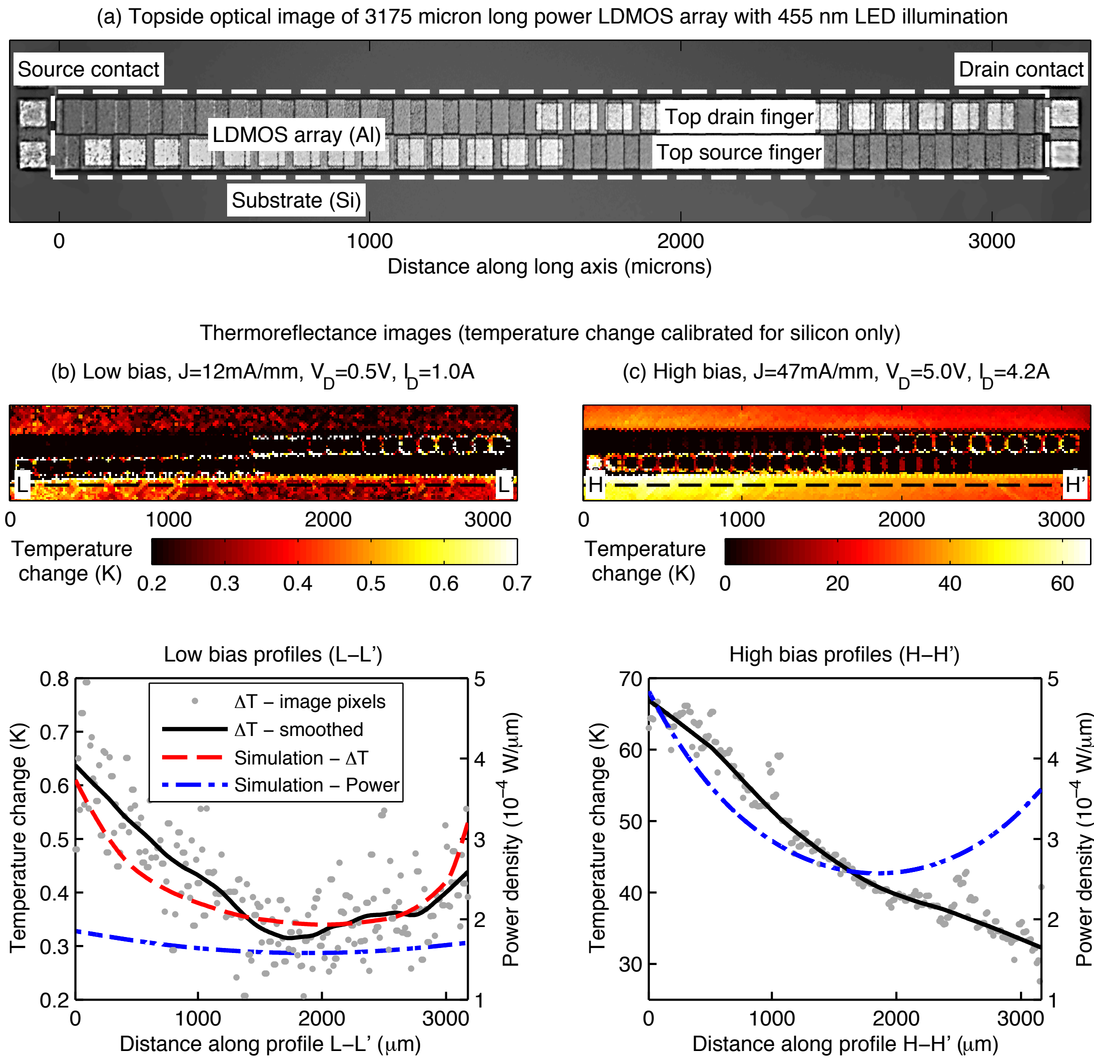

Figure 3.3: Thermoreflectance temperature change images of active 3175 micron LDMOS power transistor array at low and high bias. Thermoreflectance images calibrated for temperature change on silicon region only. (a) Optical image showing boundaries of LDMOS power array. (b) Thermoreflectance temperature change image and profile (L-L') for low bias, J=12 mA/mm. (c) Thermoreflectance temperature change image and profile (H-H') for high bias, J=47 mA/mm.

LDMOS power array at low bias showed greater heating toward the ends of the array and less heating near the middle. Maximum temperature change of 0.6 K is visible at the end of the array near the source contact. Minimum temperature change was 0.3 K,

half of the maximum. There is a noticeable asymmetry in the U-shape of the measured temperature profile at low bias. The source contact side is about 60% hotter than the drain contact side. Minimum temperature is offset from the geometric middle of the array and is closer to the drain contact side.

The nonuniform and asymmetric “U” shape of the measured temperature profile was predicted by both power and temperature simulation. R3D simulation of electrical power distribution in the metal interconnect for the active LDMOS power array revealed a voltage drop (relative to external applied voltage) throughout the three layer interconnect system. The simulated power density profile along the long axis of the array (L-L’) is shown with temperature profiles at low bias in Figure 3.3b This spatially varying voltage drop along the interconnects during operation, sometimes referred to as debiasing [22, 26], is caused by electrical resistance in the metal fingers and vias and is a significant cause of nonuniform self-heating in power devices. There is good qualitative agreement between the nonuniform “U” shape distribution of the measured temperature profile and the R3D simulated power profile, indicating greater power dissipation toward the ends of the array and less near the middle. Simulation also reproduced the asymmetry in the measured “U” shape profile. Both measured temperature change and simulated power is greater on the source contact side than on the drain contact side. There is similar agreement between the location of minimum measured temperature change along the profile and minimum simulated power, both occurring about 13% from the geometric middle of the array, offset toward the drain side. It should be noted that the device layout is symmetric along its long axis. Asymmetry in power and tem-

perature during operation is a consequence of external applied bias only. Simulation of the temperature change using the power blurring technique was performed for the low bias case. Because power dissipation at the contact pads due to probe-contact resistance is unknown, this value was used as a fitting parameter in the simulation. The simulated power distribution was modified slightly by introducing an additional 170×10^{-6} W (on average) of probe contact power dissipation at both ends of the power array. The resulting simulated temparature change profile at low bias (Figure 3.3b) shows good agreement with measurement.

3.5.1.2 Self-heating at high bias

The arrays thermal pattern shifts significantly at higher bias levels. Figure 3.3c shows the thermoreflectance image of the array at 5.0 V and 4.2 A for a channel current density of 47 $\mathrm{mA/mm_{GATE\ WIDTH}}$. Total power was 21 W and power density was 2600 $\mathrm{W\,cm^{-2}}$. At this high bias the hottest part of the array was 63 K above ambient. This value was confirmed with direct micro-thermocouple point measurement. The high bias thermoreflectance image and corresponding temperature profile along the long axis of the array (H-H') show that at high bias heating becomes significantly concentrated at one end of the array, near the source contact pads.

The dramatic change in the self-heating spatial distribution along the LDMOS array, from a "U" shape at low bias (V_D=0.5 V) to one with heating dominant at one end of the array at high bias (V_D=5.0 V,) implies a change in current density distribution throughout the array. This may be related to changes in the temperature dependent

electrical and thermal conductivity of the metal interconnect layers under high bias and high temperature conditions. Temperature dependent current transfer characteristics of the intrinsic LDMOS transistors at the silicon level may also play a part.

Simulation of the electrical power spatial distribution at high bias, however, did not reproduce the substantial shift in magnitude and spatial nonuniformity visible in the high bias thermoreflectance image and profile shown in Figure 3.3c. Instead, the simulated power profile at high bias repeated the same "U" shaped distribution seen at lower bias but with proportionally higher power and slightly increased eccentricity of the profile. Thermal simulation at high bias is not included because no extrapolation based on the "U" shaped high bias electrical power distribution would produce a simulated temperature profile resembling the shape of the measured temperature change profile at high bias. The high bias measurement indicates non-linear effects where temperature dependent device and metallization properties substantially change the three dimensional current distribution in the active structure. The mechanism responsible for this change at high bias is the subject of future investigation involving self consistent analysis. The unexpected result at high bias illustrates the usefulness of thermal imaging with high spatial resolution when characterizing high power devices. Thermoreflectance CCD imaging can instantly correlate changes in device electrical behavior with occurrence and location of hot spots. By comparison, thermal characterization methods that rely exclusively on electrical measurements provide limited or no information about the spatial thermal distribution in the device.

3.5.2 Self-heating dependence on ambient temperature

Self-heating distribution in complex power devices can change as ambient temperature conditions change, even if the applied bias is held constant. Thermoreflectance CCD imaging was used to characterize changes in the LDMOS power transistor array's self-heating distribution at different external chip temperatures. Thermoreflectance images of the active device were obtained for steady state external chip temperatures of $T_{EXTERNAL} = 296\,K$, $333\,K$ and $373\,K$. Excitation bias applied to the LDMOS array was the same for all three external chip temperatures. Gate voltage was constant at $V_{GS} = 10\,V$. Drain excitation was again a 10Hz square wave with $V_D = 0.55\,V$ and $I_D = 1.0\,A$, producing channel current density of $19\,mA/mm_{GATE\ WIDTH}$. The LDMOS array used in the ambient temperature comparison was 1905 microns along its long axis with effective total gate width of 54 millimeters. External chip temperature during thermoreflectance imaging was controlled by fixing the chip substrate to a digital hot plate using a high thermal conductivity paste.

The effect of external chip temperature on the LDMOS arrays self-heating distribution can again be observed by inspecting the temperature change amplitude along the long axis of the array. Figure 3.4 (solid lines) shows the measured thermoreflectance temperature change profiles along the long axis of the LDMOS array for increasing ambient temperature. For all three external chip temperatures the self-heating profiles along the long axis of the LDMOS array showed the same "U" shape characteristic: hotter at the contact ends and cooler in the middle of the device. However, with

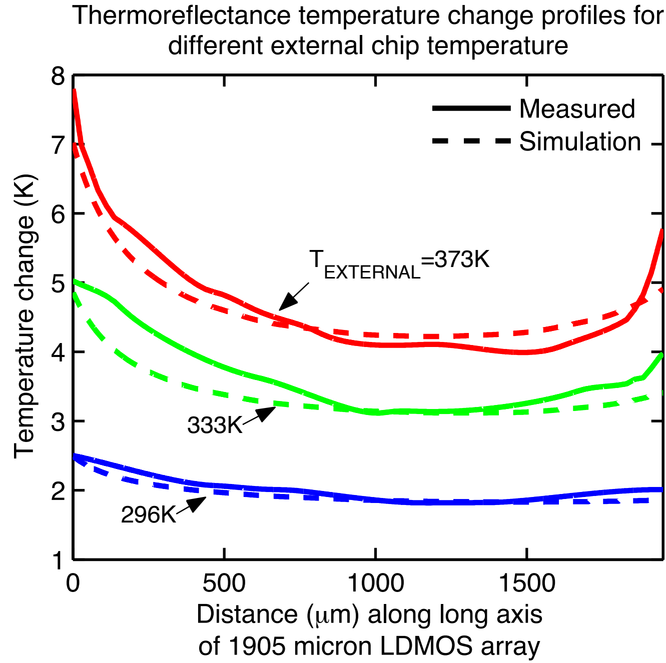

Figure 3.4: Measured thermoreflectance temperature change profiles and simulated temperature change profiles along the long axis of the 1905 micron LDMOS power array at $T_{EXTERNAL}$=296 K, 333 K and 373 K. V_D=0.55 V.

increasing external chip temperature, average device self-heating temperature change increased and the temperature change peaks at the ends of the LDMOS array became more pronounced. Average device self-heating temperature change along the full length of the array increased by a factor of 2.8 as external temperature increased 77 K above room temperature ($T_{EXTERNAL}$ = 373 K). Also, self-heating became less uniform with increasing ambient temperature. For example, peak temperature change at the source end of the array increased by a factor of 3.1 (from 2.5 K to 7.8 K) as external chip temperature increased from 296 K to 373 K. As with the results for increasing device bias current, increasing the ambient temperature also showed a similar, though smaller, shift in overall self-heating toward the source end of the power array.

Simulation was performed for both the electrical power distribution and temperature change distribution in the transistor array at the three different external chip temperatures. Figure 3.4 (dashed lines) shows the simulated temperature change along the long axis of the array for the three different external temperatures. For each simulation, thermal conductivity of the die's silicon substrate was adjusted for external die temperature. As with the simulation comparing low and high bias, heat generated at the probe contacts was used as a fitting parameter in the thermal simulation. The power map was modified slightly by introducing an additional 170×10^{-6} W (on average) of probe contact power dissipation at both ends of the power array. The resulting temperature verification, based on temperature dependence of resistance in the multilayer metal interconnect, temperature dependence of substrate thermal conductivity, and probe contact resistance, provides a good match with experiment. Simulation varies from thermoreflectance measurements by no more than 12% at any point along the long axis of the LDMOS array. In particular, it is worth noting that the nonuniform electrical power distribution predicted by simulation (due to debiasing in the metal interconnect) successfully reproduced the nonuniform shift in device self-heating with increasing external chip temperature.

3.6 Self-heating dependence on geometric layout parameters

To reduce power loss, geometric layout parameters are chosen to minimize the effective on-resistance (RDS-on) of the entire power array. However, a layout that minimizes total RDS-on may not produce the most uniform current and temperature distribution. If reliability and optimum breakdown values are also a priority, it is important to consider the influence of geometric layout parameters on two-dimensional current and temperature uniformity. Thermoreflectance imaging was used to inspect the "quasi" steady state topside temperature distribution in the high power DMOS transistor arrays for several different geometric layout parameters. Thermoreflectance thermal images compared spatial heat distribution in different device aspect ratio and metal interconnect shape. Measurements also compared the thermal effect of conjoining several power arrays in close proximity on chip. Thermal images reveal that geometric layout design strongly influences both the maximum temperature in the power arrays and also the distribution of hot spots. Selected measurements were compared to two-dimension temperature simulation of the LDMOS power arrays using the fast power blurring simulation method.

3.6.1 Self-heating dependence on transistor array length

Heating in the power arrays was compared for different length (aspect ratio) layouts ranging between 1270-3175 microns. Because thermal images revealed arrays

of different length to have similar U-shaped temperature distribution, with maximum heating occurring at the source end of the long axis, heating dependence on array length was inspected by thermocouple spot temperature measurements at identical locations for each array. Temperature change was measured with a 25 micron thermocouple placed in the silicon region of the sample adjoining the source finger near the source contact of the array. Again the silicon region was chosen because of its proximity to the active intrinsic transistors.

Figure 3.5 shows steady-state temperature change at identical locations for LDMOS arrays of four different lengths, 1270 micron, 1905 micron, 2540 micron, and 3175 micron. The temperature change for each layout is plotted versus current density (total current/device area.) Gate voltage was 10 V for all measurements. The measurements clearly show heating increase with array length. For identical applied current density, increasing array length by 25% results in an increase in temperature change of approximately 33%. This ratio is consistent both at low bias (less than 20 A/mm) and high bias.

3.6.2 Self-heating dependence on transistor array interconnect taper

Measurement and simulation suggest that electrical resistance in the transistor arrays metal interconnect layers are the primary cause of nonuniform power distribution and therefore nonuniform temperature distribution throughout the transistor array, especially along its long axis. It is assumed that power uniformity would be improved if the external drain-source connections ran the full length of the array, for example, by

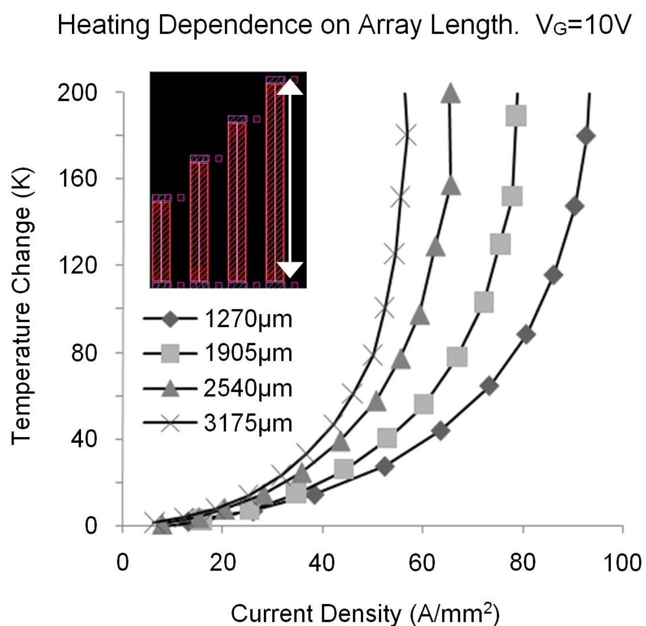

Figure 3.5: LDMOS heating dependence on array length. Temperature change for arrays of length 1270, 1905, 2540, and 3175 microns. Width is 230 microns for all arrays. For a 25% increase in array length, temperature change at identical current density increases by approximately 33%.

wire bonds or transmission lines connected to the entire top drain and source finger. However, such a configuration would reduce space efficiency and packaging options. It is therefore desirable to design the interconnect layers with a goal to minimize variation in the electric potential (debiasing) throughout the array. One way to reduce debiasing is by tapering the top drain and source fingers as shown in Figure 3.6 a,b. R3D electrical simulation of the interconnects array revealed that allocating more conducting metal area in the regions nearest to the contact pads could reduce the total drain-source on-resistance. Electrical measurements of a 2540 micron array confirmed an 11% drop in total array RDS-on from 0.40 ohms for no taper to 0.36 ohms for a maximum taper factor of 0.75.

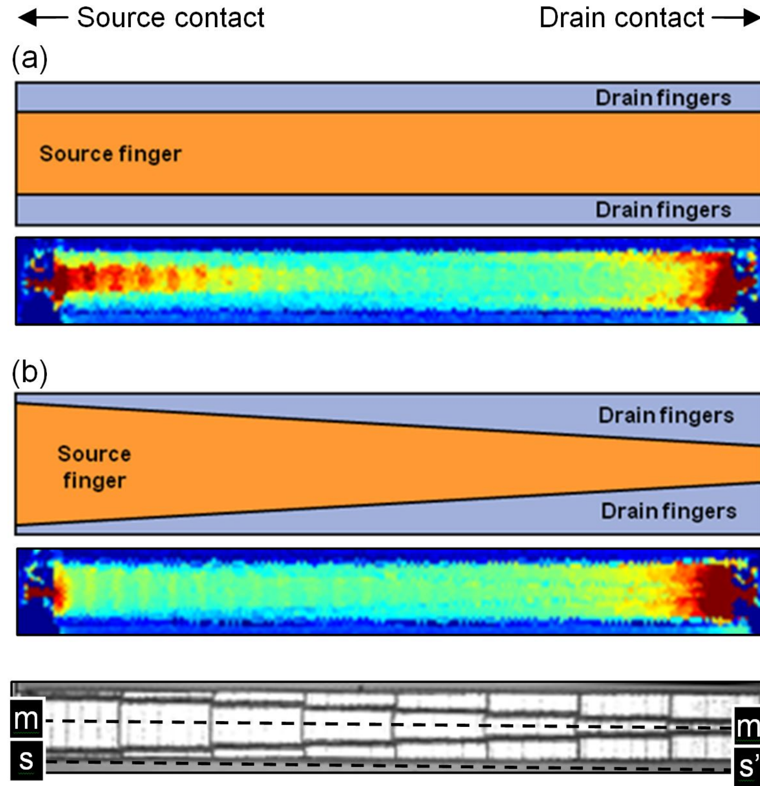

Figure 3.6: Heating dependence on tapering of interconnect top finger. Diagram and corresponding thermoreflectance images of 2540 micron power array with (a) no tapering and (b) a taper factor of 0.75. Current density is 15 A/mm, $V_G = 10$ V.

Figure 3.6a shows a diagram of a 2540 micron LDMOS array with no tapering of the top interconnect finger and the corresponding thermoreflectance thermal image. Figure 3.6b shows the same for top finger taper of 0.75. Current density for both images is 15 A/mm with gate voltage = 10 V. Figure 3.7 plots the thermoreflectance temperature change profiles along the long axis of the power arrays for interconnect taper factors ranging between zero and 0.75. The profiles are measured on the aluminum metal. The source ends of the arrays show a strong correlation between finger taper and self-heating. Peak temperature change for the maximum taper (0.75) is 47% lower than

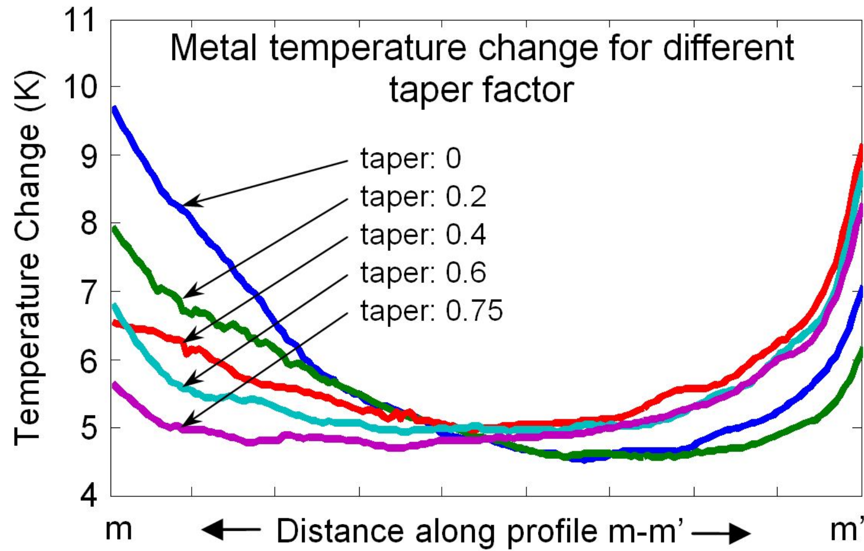

Figure 3.7: Thermoreflectance temperature profiles on the transistor array interconnect aluminum along the arrays long axis for taper factors ranging between 0 and 0.75.

the array with no taper. In addition to reducing the peak temperature, the tapered interconnect created a more uniform (flat) temperature distribution along the long axis of the array. It is worth noting that changing the interconnect layout resulted in a 47% drop in peak local temperature while the corresponding drop in total RDS-on was 11%. In this case thermal imaging provides local spatial information about power array performance that may not be easily extracted from methods that measure average values for the entire device.

Figure 3.8 shows the power blurring simulated temperature change for different taper factors, based on the R3D simulation of power distribution throughout the array. The power simulation included the effect of debiasing throughout the interconnects. The trend visible in the temperature simulation agrees with the one seen in the thermoreflectance measurements. Increasing finger taper reduces peak heating and

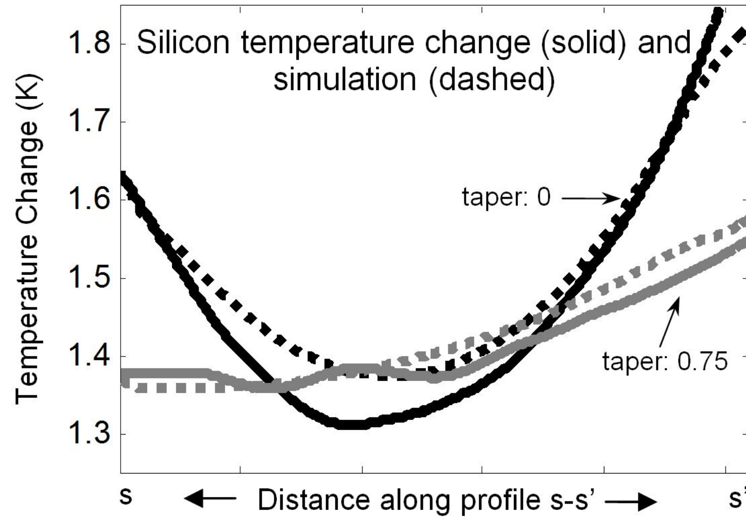

Figure 3.8: Power blurring simulated temperature change along the transistor array long axis, measured at the silicon, for varying top finger taper, based on R3D simulated interconnect power maps.

improves temperature uniformity. The disparity in absolute magnitude between measurement and simulation can be explained by the exclusion of interconnect self-heating from the power map simulation. This implies that thermal models for power devices should include contributions from interconnect self-heating even at low bias levels, when device temperatures are not sufficiently high to induce changes in material thermal properties. At lower bias levels, such as 12 mA/mm as seen in Figure 3.3b, current crowding and heating in the interconnects becomes less significant and we see better agreement between measurement and simulation.

3.6.3 Self-heating dependence on number of parallel array units

The power array cells can be cascaded in parallel to further reduce total on-resistance or increase total current compliance to meet the requirements of a given

power application. The thermal effect of conjoining power transistor array cells with no space buffer can be complex, and it may not be possible to infer the ensemble heating pattern from looking only at the thermal response from a single array. Therefore, the temperature distribution for multiple parallel LDMOS power arrays was studied for the case of one, two, and four conjoined arrays. For this experiment, the smallest structure consisted of a single 1270 micron by 230 micron base unit, including drain and source metal interconnect layers and underlying transistors. Larger power structures were constructed by conjoining multiple 1270 micron arrays in parallel. Figure 3.9 shows the thermoreflectance images of active power structures consisting of (a) one, (b) two, and (c) four conjoined 1270 micron LDMOS arrays. To isolate the thermal effect of introducing additional neighboring arrays, all three structures were imaged at identical area power density of 594 W/cm^2. Drain voltage was held constant at 5.5 volts. Drain current was adjusted between 0.31 and 1.35 A by varying gate voltage between 1.3 and 1.5 V to achieve identical power density for all three structures. Figure 3.9d shows the temperature change profiles measured on the interconnect metal, from source contact to drain contact along a line bisecting the center of the active conjoined power arrays. Results show the maximum temperature change for four conjoined parallel arrays increases by 215% over the maximum temperature change for the baseline single array at identical power density. The steep heat increase for conjoined arrays demonstrates the thermal influence neighboring heat sources in densely packed integrated circuits.

It is worth noting the measurements at low gate voltage (V_G less than 1.5 V) show self-heating concentrated in the center of the arrays. This is in contrast to the

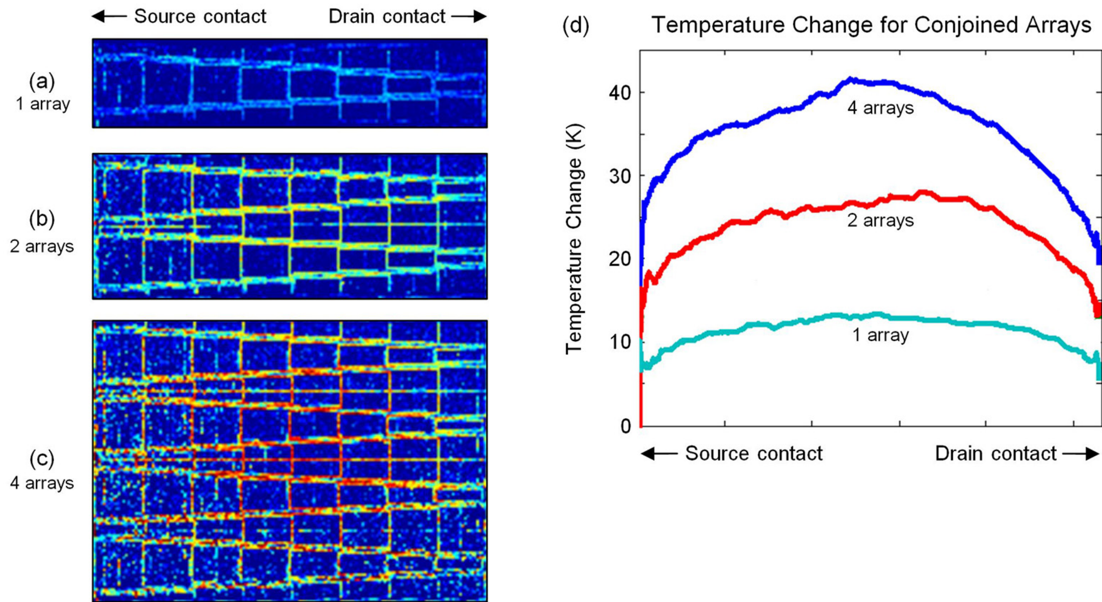

Figure 3.9: Heating dependence on number of conjoined parallel arrays. Thermoreflectance images at identical area power density (594W/cm2) for power structures consisting of (a) one, (b) two, and (c) four conjoined 1270 micron long LDMOS arrays. (d) Temperature change profiles measured along the center of the conjoined arrays (metal) from source contact to drain contact.

U-shaped distribution seen for single arrays at high gate voltage ($V_G = 10$ V) as in Figure 3.3. The result can be explained by changes in the dominant source of heating. At lower gate voltages channel resistance increases and heating at the intrinsic silicon transistor level dominates. At higher gate voltage (lower channel resistance) heating in the metal interconnects becomes dominant due to higher current.

Finally, thermal images did not show variation in self-heating distribution for gate widths of 100 and 200 microns.

3.7 Conclusion

Thermoreflectance CCD imaging was demonstrated as a fast and versatile method for characterizing steady state self-heating in power microelectronics. Thermoreflectance imaging with submicron spatial resolution and 50 mK temperature resolution was used to study self-heating temperature distribution in LDMOS silicon power transistor arrays under DC operation. Thermoreflectance images revealed highly nonuniform spatial self-heating distribution in the active power arrays. Two dimension thermoreflectance temperature change images of power LDMOS arrays were acquired for low device bias (V_D = 0.5 V, I_D = 1.0 A) and high bias (V_D = 5.0 V, I_D = 4.2 A), and as a function of external die temperature (296 K to 373 K). Low bias self-heating was roughly symmetric with respect to the array's long axis, while high bias heating was strongly concentrated at the source end of the transistor array. Thermoreflectance measurements also showed maximum temperature change in the transistor array increase by a factor of 3.1 as external die temperature increased from 296 K to 373 K for same applied bias. Transistor array self-heating showed strong dependence on geometric layout parameters such as array length, tapering of the metal interconnects, and assembling larger arrays through conjoining multiple units in parallel. Results suggest temperature-dependent material properties play a key role in heating for fast switching, high power transistor devices with complex interconnect metalization. Thermoreflectance imaging revealed spatial thermal nonuniformity in the power devices that likely would not have been evident using thermal characterization methods that rely exclusively on electrical

measurement.

Chapter 4

Ultra-fast transient thermoreflectance imaging of gallium nitride high electron mobility transistors

4.1 Abstract

Transient thermoreflectance CCD imaging with submicron spatial resolution and 50 millikelvin temperature resolution is used to study fast pulsed self-heating in two finger AlGaN/GaN high electron mobility transistors (GaN HEMTs) on a silicon carbide substrate. Transient thermoreflectance imaging systems based on both pulsed light emitting diode illumination and 800 ps pulsed laser illumination are demonstrated with minimum time resolution of 50 ns and 5 ns respectively. Time evolution of device self-heating magnitude and spatial distribution is measured between 5 ns and 100 µs in response to square drain voltage pulses of 21 V with fully open channel (V_G = 2

V) and current of 0.28 A for pulsed power of 19 W/mm. Device transient temperature change is analyzed for critical HEMT features at micron length scales. Significant variation is observed between thermal rise times for device gate metal, GaN channel, and contact metal. Quasi-steady state temperature rise of 140 K is reached at time = 100 µs. A case example is presented for fast transient thermoreflectance imaging as a compatible extension of the industry standard electrical test die method for extracting thermal resistance of semiconductor devices. Ultra-fast, high resolution imaging of time-varying thermal gradients in critical thin-film device features can be used to study failure mechanisms and improve thermal performance of modern fast-switching power devices.

4.2 Introduction

Gallium nitride high electron mobility transistors (GaN HEMTs) have attracted considerable interest in the fields of power switching systems for power conversion and radio frequency communications due to their fast switching capabilities, high breakdown voltage, and high temperature tolerance. Despite these promising characteristics, insufficient understanding of thermal behavior and reliability has limited applicability of GaN HEMTs, especially at high power densities. Phenomenon such as current collapse due to electron trapping in the gate dielectric under switching operation [88, 96] and formation of defects in the thin AlGaN layer near the gate due to inverse piezoelectric mechanical stress have been observed. [20, 24] Temperature plays

the most pervasive role in GaN HEMT reliability, affecting the above processes but also affecting industry standard accelerated life testing which requires precise understanding of the temperature of the fail site even for steady-state operation. [43] High power fast switching presents additional challenges, and while it is understood that evaluation of pulsed operation requires understanding transient temperatures [28], the GaN materials system presents new challenges at very short time scales because GaN HEMTs are operated to higher temperatures, thermal gradients, and much higher power density [85] than competing technologies such as GaAs FETs. Comprehensive evaluation and cross-validation of these difficult to measure temperatures with multiple techniques capable of collecting data at the required small length and short time scales, such as micro-Raman thermography [67], coupled electro-thermal modeling, and transient thermoreflectance imaging will be critical. Here we will discuss fast, pulsed transient thermoreflectance imaging measurements of fast, time-varying self-heating in a representative multi-finger GaN HEMT power structure.

The experiment measured fast transient heat distribution on the surface of a two-finger GaN/AlGaN power transistor on a silicon carbide substrate under high power bias. The transient thermal rise was measured for square voltage pulses applied to the drain with 3 ns rise time. Device pulse widths were 1, 10, and 100 µs with duty cycle of 15%. Pulse amplitude was 20.5 V with the channel fully open (V_G = +2 V), producing saturation drain current I_D = 280 mA and total transistor power of 5.7 W (19 W/mm). Thermal characterization was performed with the HEMT in fully open channel bias condition to optimize distribution of the heat load along the entire channel

and Ohmic contacts. [44] Additionally the fully open bias condition afforded maximum heat load with minimal drain bias (to avoid degradation during characterization) and avoids non-uniform power distribution along the gate width that can occur in a mostly pinched off device. Transient thermoreflectance images of the GaN HEMT were obtained using two system configurations capable of different minimum time resolution. The first system used a pulsed light emitting diode illumination source with 50 ns minimum time resolution. The second system used a pulsed, visible wavelength semiconductor laser with 800 ps minimum time resolution. Thermoreflectance images with 50 ns time resolution revealed different thermal transient rise times for adjoining HEMT features. The small gate metal ($\approx$ 1 µm) and GaN channel (L $\approx$ 4 µm, W = 150 µm) were observed to heat up two to three times faster than the drain contact metal. The HEMT GaN channel and gate metal were observed to reach "quasi" steady state temperature rise, 120 K and 100 K above ambient respectively, within the first 5-10 µs following the rising electrical pulse edge. Drain contact metal adjoining the channel required 100 µs to reach "quasi" steady state temperature rise of 68 K. The ultra-fast transient response of the HEMT gate and contact metal over the first 50 ns of the excitation pulse are compared with 5 ns time resolution using data obtained with the laser based measurement. A test case is offered to demonstrate how the high temporal resolution of transient thermoreflectance imaging can be used to extend the JEDEC industry standard electrical test die method for extracting thermal parameters of integrated circuits.

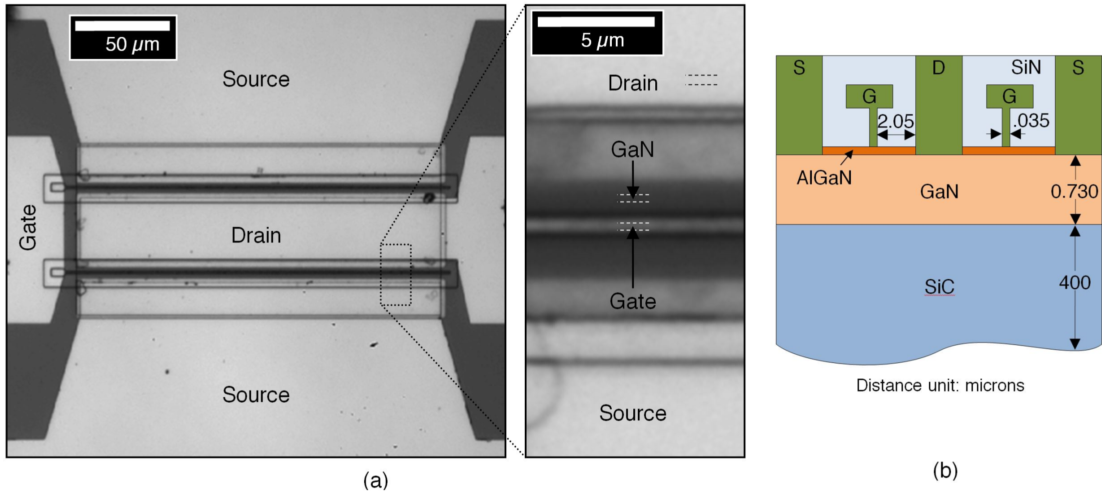

Figure 4.1: Two finger AlGaN/GaN high electron mobility (HEMT) power transistor designed for MHz operation. (a) Optical CCD image. Gate width = 150 μm. Channel length = 5 μm. Enlarged image shows location of thermoreflectance sampling boxes for HEMT drain metal, GaN channel, and gate metal. (b) Schematic cross section of AlGaN/GaN HEMT (not to scale).

4.3 Device description

The device studied is an AlGaN/GaN high electron mobility transistor (HEMT) designed for radio frequency power applications. A magnified optical image of the HEMT is shown in Figure 4.1a. The two-finger field effect transistor consists of two 150 μm wide channels. Channel length of each finger is 5 μm. The unpackaged sample was grown on a 350 μm SiC wafer. Each of the two active channels (SiN passivated AlGaN/GaN stack) are situated between a single drain metal contact in the middle of the structure and source metal ground contacts (top and bottom in Figure 4.1a). This coplanar ground-signal-ground layout reduces Ohmic loss under fast switching radio frequency operation. Devices used in this study are normally-on or depletion-mode. For V_G less than -4 V they were verified to have negligible drain current for drain bias up

to 50 V.

4.4 Experiment method

4.4.1 Transient thermoreflectance imaging

Transient thermal images were obtained using a thermoreflectance CCD system capable of submicron spatial resolution and 50 mK temperature resolution. Minimum time resolution was 50 ns and 800 ps [31] for light emitting diode and laser based systems respectively. A diagram of the experiment configuration for transient thermoreflectance imaging is shown in Figure 4.2. The top surface of the GaN HEMT sample is illuminated using either a narrowband light emitting diode (LED) or laser. Square voltage pulses were applied to the HEMT drain at 15 kHz repetition rate with 15% duty cycle. Each voltage pulse induces joule heating in the HEMT and corresponding perturbation in HEMT temperature and surface reflectance. A sensitive high dynamic range CCD camera synchronized to the HEMT electrical repetition rate records separate reflectance images corresponding to HEMT hot and cold states during the pulse cycle. The difference of hot and cold images produces a pixel-for-pixel map of temperature induced reflectance change amplitude ($\Delta R/R$) for the HEMT surface materials in response to the applied bias pulse. As described previously, the raw thermoreflectance images of the GaN HEMT were converted to maps of device surface temperature change by applying the appropriate thermoreflectance coefficient, C_{TH}, to each material region of interest in the image. Calibrating the GaN HEMT material thermoreflectance coefficients

involved a combination of the experiment external heat stage technique and indirect estimates of C_{TH} based experiment calibration. A 530 nm (green) LED was found to optimize amplitude of the thermoreflectance signal on HEMT metal regions. The experimentally calibrated thermoreflectance coefficient for the HEMT drain/source contact metal was $\mathrm{C_{TH,contact\ metal}}=1.6 \times 10^{-4}\,\mathrm{K}^{-1}$ using 530 nm LED illumination. Thermoreflectance coefficients for the HEMT gate metal and GaN channel were estimated as $\mathrm{C_{TH,gate\ metal}}=5.2 \times 10^{-5}\,\mathrm{K}^{-1}$ and $\mathrm{C_{TH,GaN\ channel}}=-2.0 \times 10^{-5}\,\mathrm{K}^{-1}$ at 530 nm illumination. Because the amplitude of the transient thermoreflectance change for the GaN HEMTs were typically on the order of $10^{-4}\,\mathrm{K}^{-1}$ to $10^{-5}\,\mathrm{K}^{-1}$, acquisition of thermoreflectance images with good signal to noise ratio required averaging over many device excitation cycles. Transient thermoreflectance images of the GaN HEMT were averaged for 10 to 120 minutes of continuous HEMT excitation at lock-in repetition rates ranging between 1.5 to 150 kHz.

As described previously, transient thermoreflectance imaging is achieved by pulsing the illumination source rather than using constant illumination. Transient images of the GaN HEMT were obtained using the pulsed differential algorithm described in Figure 2.4. The CCD camera records reflectance information only for the duration of the illumination pulse. The delay of the illumination pulse (τ) relative to the device excitation pulse is controllable. The full HEMT thermal transient can then be assembled by acquiring a sequence of images as the illumination pulse delay is adjusted in increments relative to the rising edge of the HEMT excitation pulse. Minimum transient time resolution is determined by the minimum pulse width that can be achieved by the

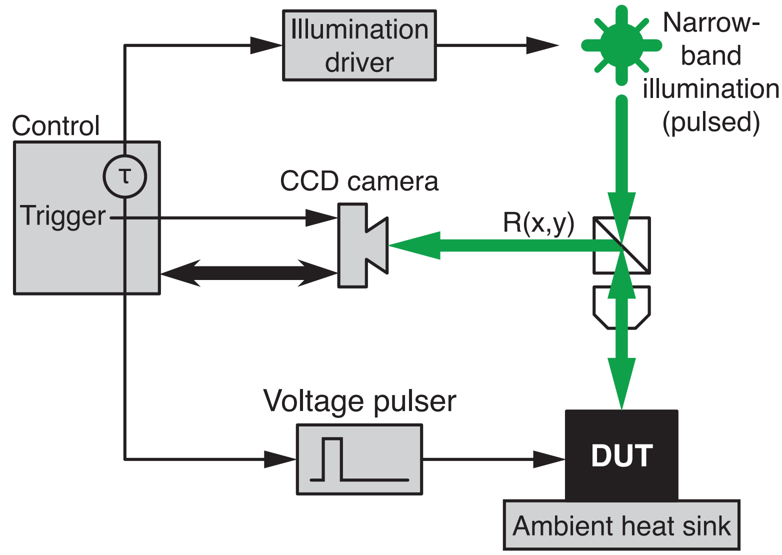

Figure 4.2: Experiment configuration for pulsed transient thermoreflectance imaging of the GaN HEMT.

illumination source, 50 ns for the LED and 800 ps for the laser. System timing and CCD acquisition were controlled by custom Microsanj hardware triggers and SanjView program.

4.4.2 Electrical pulsing parameters for GaN HEMT thermoreflectance imaging

Each thermoreflectance image of the 2 x 150 micron GaN HEMT was acquired for a single bias point combination of drain-source voltage, gate voltage, and resulting drain current. A positive voltage pulse signal, V_D, was applied across the HEMT drain-source terminals. Constant voltage, V_G, was applied to the gate terminal. This would produce a positive drain-source current pulse, I_D. The pulse amplitude of V_D and the value of V_G were maintained at constant levels over the averaging duration of

each thermoreflectance image acquisition. To measure HEMT degradation caused by thermoreflectance pulsing, separate DC measurements of I_D for a given V_D-V_G were obtained before and after each thermal image acquisition. DC I_D was observed to increase or decrease by a maximum of 3% during the time required to acquire each image. Voltage and current levels specific to each thermoreflectance measurement are given for each result presented herein.

Figure 4.3a shows the circuit used during thermoreflectance imaging of the HEMT. V_{PULSER} sends a periodic voltage pulse signal triggered at the predetermined lock-in frequency (pulse repetition rate.) Pulse width typically varied between one microsecond to one millisecond with duty cycle typically 5-20%. V_{PULSER} was supplied using a Berkeley Nucleonics 202H high voltage pulser capable of pulses up to 3 milliseconds in duration with maximum compliance of 300V and 6 amps. The rated pulse rise and fall times for the 202H are 3 ns and 10 ns respectively when matched to a 50 ohm load. Because the GaN HEMT thermoreflectance pulsing circuit shown in Figure 4.3a is not an inherent 50 ohms, additional circuit elements were required to match the output impedance of the pulsing instrument and minimize electrical ringing in the pulse waveform. With tuning, the pulsed power in the GaN HEMT was stable 30 nanoseconds after the pulse rising edge. To compare heating under different HEMT terminal excitation, an alternate bias scheme was tested using gate modulation instead of drain modulation. For gate modulation the gate terminal was supplied -4 to +2V square pulse waveform using an SRS DS345 function generator while the drain voltage was supplied by an Agilent DC supply held at 20 V constant. Following initial thermoreflectance

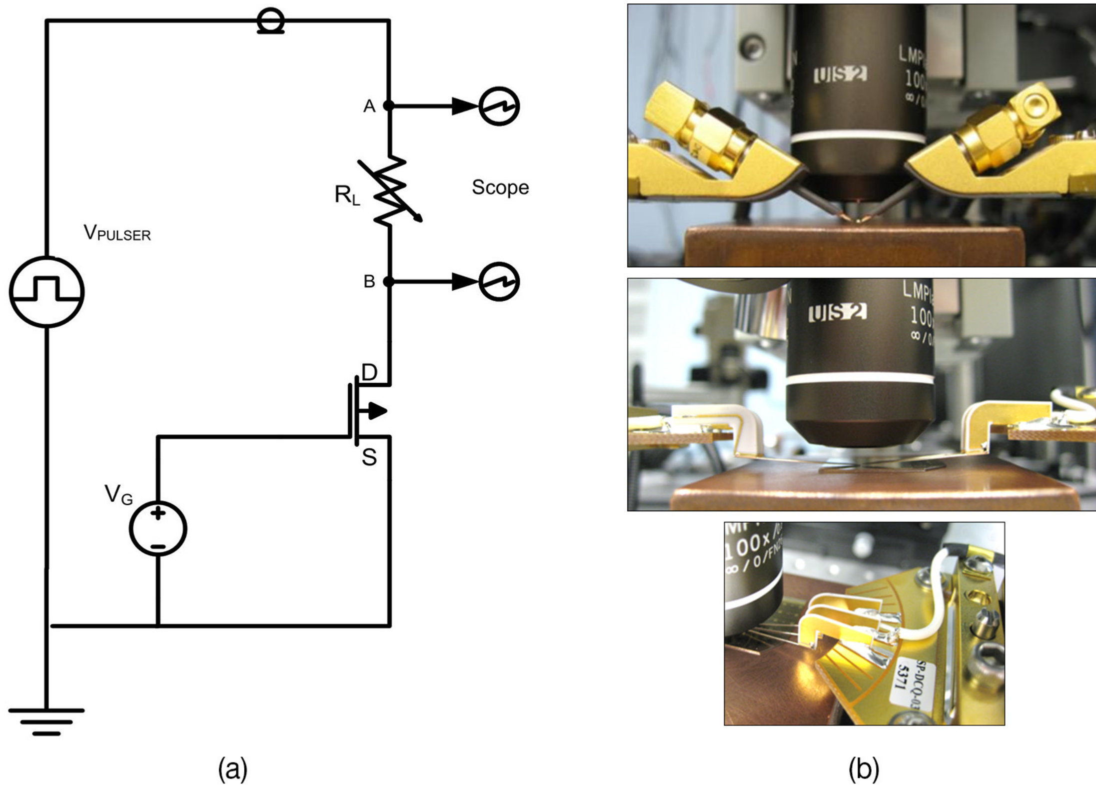

Figure 4.3: Electrical configuration for transient thermoreflectance imaging of GaN HEMT (a) GaN HEMT bias circuit for pulsed HEMT excitation. (b) High speed coplanar electrical probing of GaN HEMT for high magnification thermoreflectance imaging. Conventional coplanar RF probes (top image) do not fit within working distance (4 mm) of high magnification lens (100 X.) Custom low profile Cascade Microtech DC coplanar probes (middle, bottom image) simultaneously permit high speed ground-signal-ground device probing and high magnification imaging.

tests with the HEMT, the gate modulation bias scheme was discarded because the resulting waveform displayed very slow rise time and ringing. This was likely caused by impedance mismatch between the HEMT circuit and the DC drain voltage supply or parasitics in the DC supply, which is not optimized for high speed switching operation. Consequently, all thermoreflectance measurements presented were obtained using the

drain modulation technique only, with the BNC 202H supplying fast rise time pulses to the drain terminal and constant bias applied to the gate terminal. Thermoreflectance characterization of self-heating in HEMTs and other high speed power devices under radio frequency electrical operating conditions is the subject of future studies.

Pulsed voltage and current waveforms in the HEMT during testing and thermoreflectance imaging was measured in real time using a LeCroy high bandwidth 3.5 GHz digital oscilloscope. HEMT drain-source voltage, V_D, was obtained directly from the voltage at node B in the circuit diagram of Figure 4.3a. Pulsed current through the HEMT, I_D, was measured from the voltage drop across a high power measurement resistor, R_L, which was placed in series with the HEMT drain-source contact. The value of the measurement resistor R_L ranged between 50 ohms for HEMT drain currents above 30 mA and 500 ohms for smaller currents.

All thermoreflectance imaging measurements were performed on a bare GaN quarter wafer sample fixed to a large copper heat sink maintained at room temperature. Probing of individual GaN HEMT structures was done with two high frequency ground-signal-ground coplanar probes and micropositioners, one each for gate and drain contacts. Cascade Microtech ACP-40L probe tips were used for thermoreflectance images acquired using objective lenses of 50 X or lower magnification. For imaging at 100 X magnification, special DC coplanar probe tips were fabricated by Cascade Microtech (model DC-Q-3) to accommodate the low objective working distance of 4 mm (See Figure 4.3b.) Pulse rise time using custom ground-signal-ground coplanar DC probes was $\approx$ 15 ns, compared to $\approx$ 300 ns when using standard single pin DC probes. Coaxial cabling

and minimum cable lengths were used to minimize electrical ringing and reflections in the pulsing circuit.

4.5 Results

4.5.1 Rising and falling transient response: Device pulse width = 10 µs, time resolution = 500 ns

Figure 4.4a shows false color thermoreflectance images at selected times in the HEMT rising and falling thermal transient for one cycle in the lock-in excitation signal. The voltage pulse applied to the drain was 20.1 V producing drain current of 123 mA. Gate voltage was +2.0 V and gate current was negligible. The width of the pulse was 10 µs and the duty cycle was 15% for a total pulse period of 66 µs. HEMT electrical waveform for the 10 µs drain pulse is shown inset in Figure 4.4b. HEMT thermal response was measured over the time interval between 0 and 40 µs relative to the rising edge of the drain voltage pulse. Time resolution was one image per 500 ns. A pulsing signal using 15% or shorter duty cycle is sufficient to capture most of the fast thermal transients of integrated circuits with features on the micron scale. Our transient thermoreflectance system measures temperature change normalized to the sample absolute temperature at time = 0 s in each excitation cycle. With good sample thermal interface to heat sink, it is assumed that the small, thermally fast HEMT features inspected (channel, gate, and contacts) reach thermal quasi-steady state at the end of each pulse period. However, it is possible that slower thermal transients, such

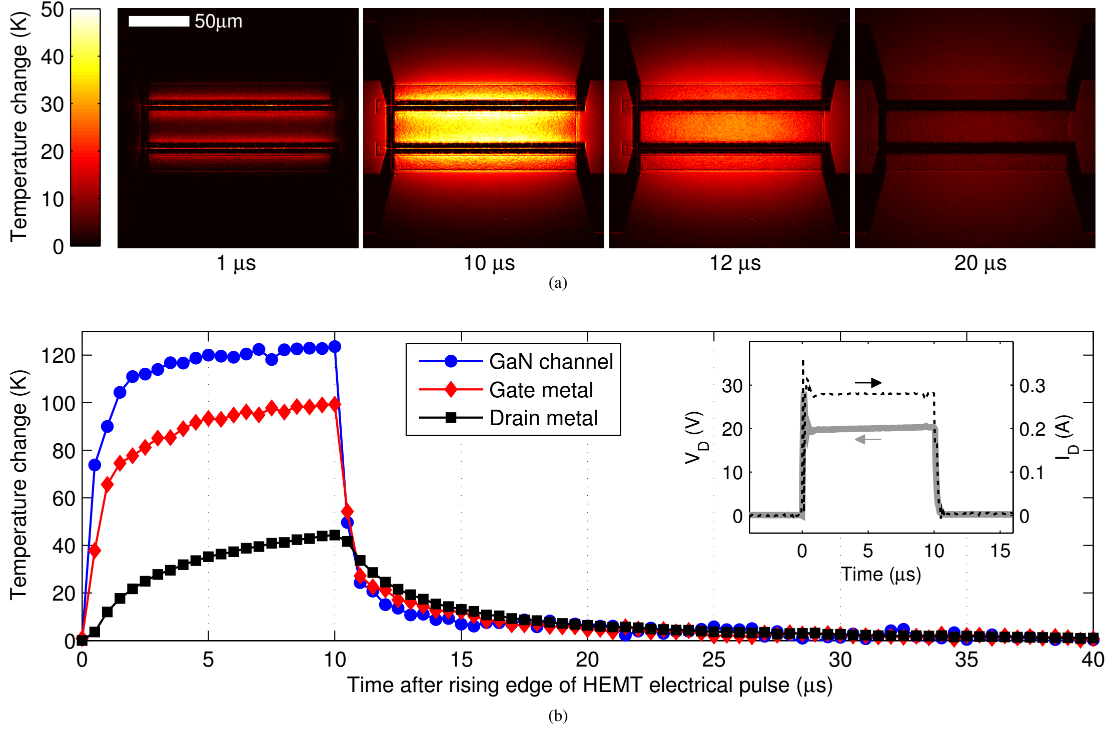

Figure 4.4: AlGaN/GaN HEMT transient thermoreflectance image heating and cooling for a 10 µs excitation pulse. Time resolution is 500 ns. V_D = 20.5 V, I_D = 280 mA, V_G = +2 V. Power is 5.7 W. (a) False color transient thermoreflectance images of the HEMT at 1, 10, 12, and 20 µs after the rising edge of the HEMT excitation pulse. Images calibrated for temperature change on the drain contact metal only. (b) Heating and cooling transient for GaN HEMT channel, gate metal and drain contact metal. Electrical waveform for 10 µs pulse shown inset. Rise times (1-1/e) for the channel and gate metal are 1 µs. Rise time for the drain contact metal is 3 µs.

as those related to the full wafer sample, are not evident in the measurement. The thermoreflectance images in Figure 4.4 are calibrated for temperature change on the HEMT drain metal material only. The GaN channel region, in comparison, appears dark because the sign of the thermoreflectance coefficient for GaN was observed during calibration to be opposite to that of the drain metal. The sequence reveals the time evolution of self-heating distribution across the HEMT surface. Early in the rising

transient (heating) we observe heat distribution conforming to the rectangular geometry of the two channels, which is the source of joule heating in the HEMT. At time = 10 µs, the duration of the drain voltage pulse, temperature on the drain metal has increased 42 K. The falling transient (cooling) shows heat spreading into the contact metal and substrate, and then generally dissipating in a radial pattern until reaching quasi-steady state temperature at approximately time = 40 µs.

The plot in Figure 4.4b shows the rising and falling thermoreflectance transient for three adjoining device features on the HEMT: drain contact metal, GaN channel, and gate metal. These features are indicated in the enlarged optical image of the HEMT channel in Figure 4.1a. Each data point in the transient plot represents the average thermoreflectance change for a rectangular sampling pixel box corresponding to a specific HEMT material feature. The sampling boxes are approximately one micron tall (four pixels at 50 X magnification) and run the full horizontal width of the HEMT active area. The vertical dimension and location of the sampling boxes are also indicated in the enlarged CCD image of the channel, Figure 4.1. The amplitude of temperature change for the drain metal is calculated from the experimentally calibrated thermoreflectance coefficient for this region in the sample. Temperature change on the gate metal and GaN channel is estimated using the calibration.

Because the GaN channel represents the primary source of joule heating in the HEMT, it can be seen that the temperature in the channel differs greatly from adjoining device features under transient switching operation. The gate metal and GaN channel heat up fastest. At time = 1 µs, both the gate and GaN reach 63% (1-1/e) of their

maximum value at time = 10 µs. The drain metal heats more slowly, requiring ≈ 3 µs to reach the same 63% fraction of its maximum temperature change at time = 10 µs.

4.5.2 Transient heating from time = 50 ns to 100 µs

Measurement using a 10 µs device pulse with 500 ns time resolution is useful for comparing the respective rise times of adjoining HEMT device features such as channel, gate, and contact metal regions, but this timing window does not provide information about the HEMT thermal transient over longer or shorter timescales. For example, the 10 µs excitation pulse is not long enough for the HEMT to reach steady-state "on" temperature for the experiment probing configuration. Similarly, thermal events faster than the 500 ns resolution are not visible. To inspect the HEMT transient thermal distribution over a broader range of time scales, measurements were obtained for two additional time windows: a slow window with device pulse = 100 µs and time resolution = 5 µs, and a fast window with device pulse = 1 µs and time resolution = 50 ns.

Combining transient data from the fast and slow time windows with the intermediate time window (device pulse = 10 µs, time resolution = 500 ns) creates a piecewise complete set of HEMT rising transient thermal data for time = 50 ns to 100 µs after the device rising electrical edge. Figure 4.5 shows a logarithmic plot of the full rising thermal transients for the HEMT GaN channel, gate metal, and drain contact metal for time = 50 ns to 100 µs for the same drain voltage pulse of V_D = 21 V. HEMT drain metal temperature change does not rise significantly above 65 K between time = 40-100 µs, indicating the HEMT is in thermal steady state for pulse durations greater

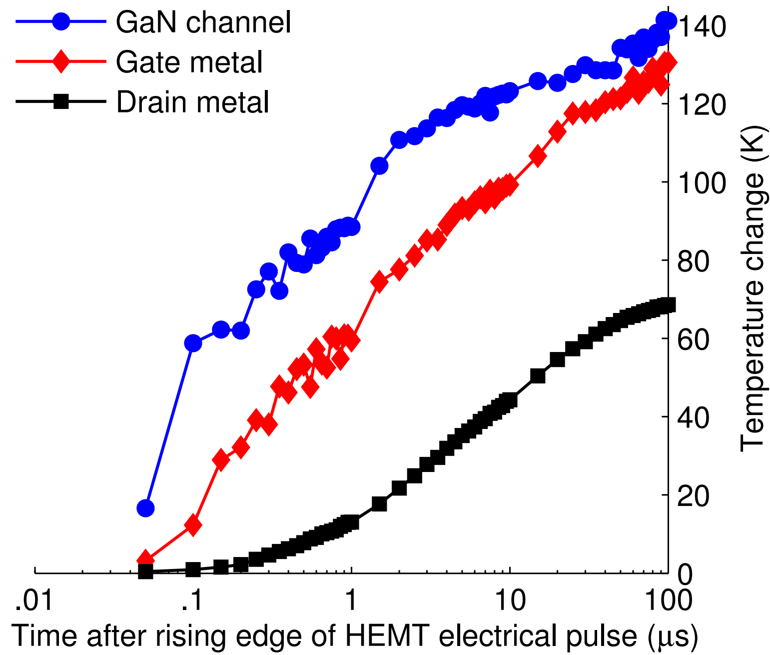

Figure 4.5: GaN HEMT transient thermoreflectance image heating versus logarithmic time for time = 50 nanoseconds to 100 microseconds after rising edge of the excitation pulse. Heating transients are compared for HEMT channel, gate metal, and drain contact metal regions.

than 100 microseconds. Consequently, it is possible to estimate the HEMT thermal rise time (1-1/e) to be in the range of ≈ 10 µs. Ideally, this complete transient would be acquired in a single thermoreflectance measurement sequence using minimum system time resolution. However, optical signal to noise of the transient thermoreflectance system is optimized when using approximately a 20:1 ratio between device pulse width and light pulse width (time resolution). Consequently, measurement of the HEMT from 50 ns to 100 µs necessitated acquisition of three separate data sets at different time resolutions.

4.5.3 Extracting device thermal parameters using transient thermoreflectance imaging and electrical test methods

As an example application, transient thermoreflectance imaging can validate and extend established industry test methods used to extract thermal parameters of integrated circuits. The electrical test method defined by JEDEC industry standards JESD 51-1 [27] and JESD 51-14 [28] experimentally extracts device thermal resistance, $R_{\theta JX}$, for packaged integrated circuits using a test die with embedded thermally calibrated diode. The technique requires measurement of the transient cooling curve from thermal equilibrium hot state (or conversely measuring the heating curve from equilibrium cold state) for a step change in applied power. Extracting $R_{\theta JX}$ requires knowledge of T_0, the device junction temperature at the start of the power transient (time = 0s). A condition of the electrical test method is that for very early times in the transient thermal measurement, typically for time earlier than 1 µs, electrical oscillations due to the coupling between excitation power and diode sensor can prevent precision measurement of electrical properties tied to temperature of the device (while in contrast we only need the power dissipation to normalize well faster than the measurement timescale). For these early portions of the transient the electrical test method uses an extrapolation to estimate T_0. Theory predicts IC transient temperature change in response to a step power change follows a linear relationship with the square root of time for early times in the transient (time earlier than 500 µs) as in JESD 51-14. This effect has been confirmed by measurement for prior technologies, and follows theoretically for 1D

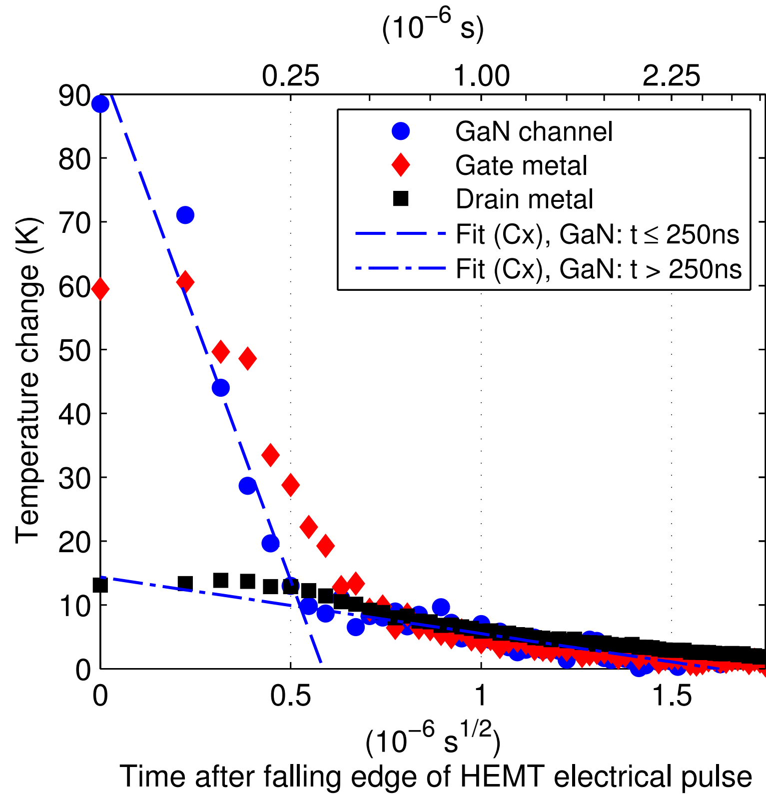

Figure 4.6: HEMT transient thermoreflectance image cooling vs square root time for time = 0 to 3000 ns after the falling edge of a 1 µs, 15% duty cycle excitation pulse. Time resolution is 50 ns per step. V_D = 21 V. Two distinct linear extrapolations of T_0 based on time segments before and after 250 ns are illustrated for the GaN channel.

diffusion of heat from a 2D (planar) source into a 3D (bulk) material of uniform thermal properties. However, GaN devices are almost universally not grown on a GaN substrate (usually instead Si or SiC) with a poor thermal conductivity interlayer, violating the theoretical assumption underlying this technique. [66]

Transient thermoreflectance imaging provides a compatible alternate method for approximating T_0 with temporal resolution significantly superior to the electrical test die method. Figure 4.6 shows the GaN HEMT transient thermoreflectance cooling

curves versus square root time for time = 0 to 3000 ns after the falling edge of a 1 µs drain voltage pulse at 15% duty cycle. (The corresponding heating transient can be seen in Figure 4.5 for time earlier than 1 µs.) Time resolution is 50 ns. HEMT drain voltage was again 21 volts. Preliminary observation reveals possible significant deviation from the linear approximation predicted by theory for early time (earlier than 1 µs) in the cooling transient. Two distinct linear approximations can be inferred from the transient thermoreflectance data over this time interval. Two example approximations are illustrated for the case of the HEMT GaN channel. Between time = 300 ns to 1000 ns, linear extrapolation predicts T_0 approximately 15 K. It is reasonable to assume the electrical test die method applied to the GaN HEMT would extract a similar T_0. However, if we inspect transient thermoreflectance data for the cooling curve at times earlier than 250 ns, a second linear extrapolation of T_0 becomes evident which differs significantly from the result calculated from later times in the transient. Linear extrapolation for time = 50 ns to 250 ns predicts T_0 approximately 90 K. The occurrence of two different linear regimes in the square root time transient is most prominent in the HEMT for the GaN channel and gate metal. Likely, this is due to the thermal conductivity difference between the buffer layer and the substrate. It is also suggested that because thermoreflectance measures die temperature optically and therefore not subject to the transient electrical oscillations of the test die technique, T_0 can be taken directly from the thermoreflectance transient curve without extrapolation.

4.5.4 Ultra-fast transient thermoreflectance imaging of GaN HEMT: 800 ps pulsed illumination

Minimum temporal resolution for pulsed transient thermoreflectance imaging is primarily determined by the shortest duration pulse that can be produced by the illumination source. The GaN HEMT transient thermoreflectance images presented previously were obtained using a narrowband light emitting diode capable of 50 ns square pulses. To inspect transient self-heating events earlier than time = 50 ns after device excitation pulse rising edge, minimum temporal resolution was extended to the subnanosecond range by using a new ultra-fast transient thermoreflectance system based around 800 ps pulsed laser illumination. [9] The ultra-fast system employs the same lock-in scheme already described. Temporal resolution was enhanced by replacing the light emitting diode illumination source with an externally triggered PicoQuant solid state 440nm visible wavelength laser with fixed 800 ps pulse width. The laser pulse produces less light than the LED per sample excitation cycle and consequently weaker overall thermoreflectance signal. This is compensated by using a higher sensitivity camera. An Andor 512x512 pixel electron multiplying charge coupled device camera (EMCCD) was used, which incorporates avalanche multiplication gain directly in the sensor to improve signal to noise. Tests of the 800 ps transient thermoreflectance imaging system on a known Au sample yielded estimated temperature resolution of one Kelvin.

Ultra-fast transient thermoreflectance images of the GaN HEMT were acquired for time resolution steps of 5 ns. Figure 4.7 shows an enlarged EMCCD image of a

single channel in the GaN HEMT with gate metal and drain contact metal indicated. Corresponding 800 ps transient thermoreflectance images show self-heating of HEMT features at 15, 25, and 50, and 100 ns after the rising edge of the excitation pulse. The thermoreflectance images shown in Figure 4.7 are calibrated for temperature change on the drain metal only. HEMT excitation pulse width was 300 ns with 15% duty cycle. Drain voltage was 15 V, drain current was 285 mA. Gate voltage was +2 V. Images were averaged for 10 minutes each. Thermoreflectance coefficients for the gate metal and drain metal at the 440 nm wavelength of the pulsed laser were estimated from the HEMT temperature change observed previously for these regions at 100 ns using the LED based system (Figure 4.5). Although some hot (bright) regions can be observed in the HEMT channel region of the thermoreflectance images in Figure 4.7, this should not be interpreted as channel temperature change, because the 800 ps thermoreflectance images shown are not calibrated for the channel region. The effect may be due to slight defocusing of the microscope during measurement, causing temperature variation along the width of the gate metal to appear as if blurring into the channel region. Transient temperature variation along the width of the gate and channel may be real, however, and will be subject of future studies.

The ultra-fast system revealed the GaN HEMT thermal transient for times earlier than the 50 ns time resolution limit of the LED based system. The images in Figure 4.7 show HEMT self heating initially confined to the gate metal and channel in the first 25 ns. Heating becomes visible in the contact metal at 50 ns. Figure 4.8 compares the transient thermal response for the HEMT gate metal and drain metal for

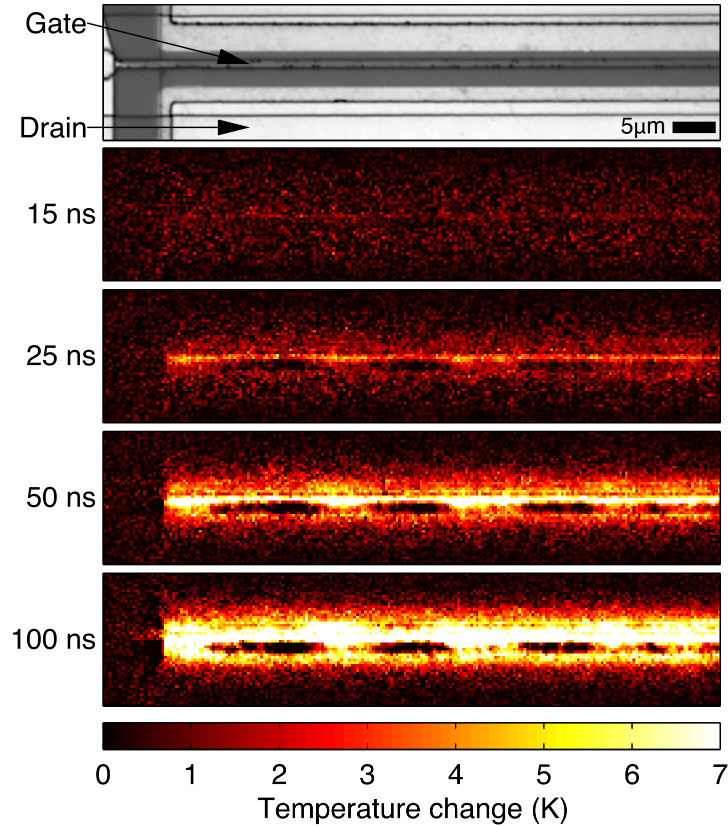

Figure 4.7: 800 ps pulsed laser transient thermoreflectance imaging of the GaN HEMT. Enlarged EMCCD image of one finger in the GaN HEMT with gate metal and drain contact metal indicated. Corresponding thermoreflectance images calibrated for temperature change on the drain metal show self-heating at 15, 25, 50, 100 ns after the rising edge of a 300 ns, 15 V excitation pulse applied to drain.

time = 0-50 ns. Measureable thermoreflectance change is visible as early as ten ns into the device pulse. Similar to the GaN HEMT measurements over longer time windows, the ultra-fast regime reveals the gate metal to have a faster thermal rise time than the drain metal. The (1-1/e) rise times for the 300 ns pulse width are 70 ns for the gate metal and 180 ns for the drain metal.

Results presented of the GaN HEMT fast transient self-heating effects demon-

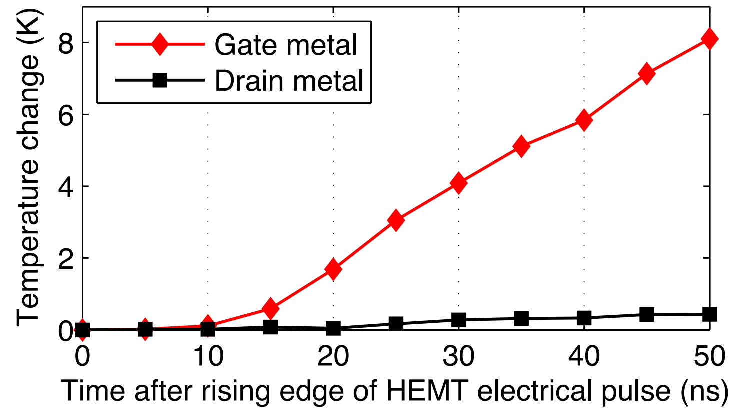

Figure 4.8: HEMT transient self-heating compared for the gate metal and drain metal with 5 ns time resolution. Pulsed laser wavelength is 440 nm.

strate the importance of high temporal resolution to extract accurate device thermal parameters. Fast transient thermoreflectance imaging demonstrates excellent capabilities in exploring critical time varying thermal performance of modern high speed devices.

Chapter 5

Fast transient thermoreflectance imaging of snapback in semiconductor controlled rectifiers

5.1 Abstract

Transient thermoreflectance imaging has been used for the first time to reveal current distribution in electrostatic discharge (ESD) protection devices based on device surface temperature change due to fast pulsed self-heating. Experimentally calibrated temperature images are obtained of a multiple finger, 80 x 80 micron, semiconductor controlled rectifier (SCR) device in the snapback power dissipating state triggered by ESD voltage pulses. Time resolved thermorefelectance images reveal non-simultaneous triggering of individual fingers on the multiple finger SCR. Self-heating is measured for different current levels (1.15-1.47 A) and at different times ranging between 100

nanoseconds to one millisecond after the rising edge of the ESD pulse. The novel applied methodology demonstrates a practical and straightforward way to characterize non-uniform temperature and current distribution in ESD structures.

5.2 Introduction

The on-chip local ESD protection device in this study is typically implemented using ESD clamps engineered to provide ESD current level according to package or system level standards. Typical clamp design includes distributed multifinger device that provides operation in conductivity modulation mode. [95] Many designs attempt to increase current uniformity, robustness, and area efficiency through multiple finger layouts. It is helpful to characterize such multiple finger designs during operation to improve efficiency or identify undesired behavior. For example, one possible problem is that individual fingers can turn on (trigger into snapback) prematurely, resulting in current crowding and thermal failure in a single finger or other local hot spot. [74]

Optimization of ESD protection designs can be assisted with visual characterization tools. Over recent years the method of backside laser transient interferometry (TIM) [38] has been used to inspect current distribution problems in ESD devices during snapback. [8, 36] The purpose of this study is to solve the same problem using the simpler alternative method of topside thermoreflectance thermography, which exploits the change in material reflectivity with temperature. [83, 84] Thermoreflectance methods that use CCD cameras [40] capture megapixel thermal images much faster

than earlier scanned laser thermoreflectance methods and at lower external illumination levels. Temperature resolution of 10mK has been demonstrated. [58] Recent pulsed illumination techniques have improved CCD thermoreflectance temporal resolution to 100 nanoseconds [31] and even sub-nanosecond, allowing for the first time thermoreflectance CCD imaging of fast transient effects such as snapback in ESD devices. Both thermoreflectance and backside interferometry can measure heating through the samples substrate using near infrared illumination. However, thermoreflectance can also obtain thermal images directly from the topside of the device using visible wavelength illumination. Topside thermoreflectance with visible light offers better diffraction limited spatial resolution (250nm) than backside infrared methods (1.5-3 microns.) The thermoreflectance method has a comparatively simple experiment setup, requiring only a standard optical microscope, LED illumination, CCD camera, timing instruments, and sample biasing instruments. No interferometer is required and the sample does not require special preparation such as backside polishing, thinning, or application of infrared antireflection coating. The main drawback is that, since the thermoreflectance coefficient is small, one cannot do single shot measurements, and averaging (from seconds to minutes) is required. One should note that typically the thermoreflectance coefficient is calibrated for small temperature variations. When temperature rise is several hundreds of degrees, the nonlinear dependence of the reflection coefficient as a function of ambient temperature should be taken into account. Thus more accurate calibrations are necessary in order to quantify the exact temperature rise. However the measured transient reflectance map should provide some information about the current non-uniformity in

the device.

This study presents transient thermoreflectance CCD images of the surface temperature on a multiple finger n-type lateral diffused MOS based silicon controlled rectifier (NLDMOS-SCR) implemented for 100V node protection using 0.5m biCMOS-DMOS process technology. Thermal images have been captured to analyze non-destructive current localization over the first 300 ns in response ESD like pulses. Submicron transient thermal images show isolated single finger triggering in the SCR with hot spots that move to different locations on the device in 100s of nanosecond time scale. In addition, dominant heating is shown to alternate between active fingers at different snapback current levels.

5.3 Experiment

5.3.1 Transient thermoreflectance imaging

The topside of the SCR chip is illuminated under a reflectance microscope using a narrow-band LED light source. The light reflected from the SCR surface is recorded on a variable frame rate, 12-bit scientific grade Dalsa CCD camera with 1024x1024 pixel resolution. Camera operation and device excitation timing is controlled by a unified labview program and custom designed hardware trigger board. Repeated square wave voltage pulses are applied to the SCR at 1% duty cycle. For this study, the width of the excitation pulse was varied between 300 nanoseconds to one millisecond to inspect SCR heating under different duration pulses. For each excitation cycle, the

pulse causes a temperature rise in the SCR, which in turn induces a change in the optical reflectance (R) at the SCR surface. Typical averaging time for the images in this study varied between seconds to several minutes. Calibration of the SCR thermoreflectance coefficient for the silicon substrate and aluminum interconnects was performed in a separate experiment step. A blue 470nm LED was used with the SCR sample due to its relatively high CTH for both aluminum and silicon. Transient thermoreflectance imaging time resolution was 50 ns, determined by the minimum pulse width of the light emitting diode source used for reflectance illumination.

5.3.2 Device pulsing method and I-V characteristics

An optical image of the NLDMOS-SCR ESD protection cell is shown in Figure 5.4a. The 80 micron square layout consists of three anode fingers and two cathode fingers. The electrodes are aluminum. The region surrounding the featured SCR is silicon. Electrical probing and thermal imaging were performed in-situ on a wafer sample. Two high speed, high current probes were used to force the ESD-like pulse at anode and cathode contact pads near the device (not shown). The other two probes simultaneously measured the voltage waveform across the SCR, which was recorded on a high bandwidth 3.5GHz LeCroy oscilloscope. Figure 5.1 shows a diagram of the pulsing circuit with voltage measurement probes indicated. Device excitation was supplied by a commercial Berkeley Nucleonics voltage pulser rated to 300V and five amperes into a 50 ohm load. Pulse rise times during excitation were observed to be less than 5 nanoseconds. Pulse current was measured from the transient voltage across the 50

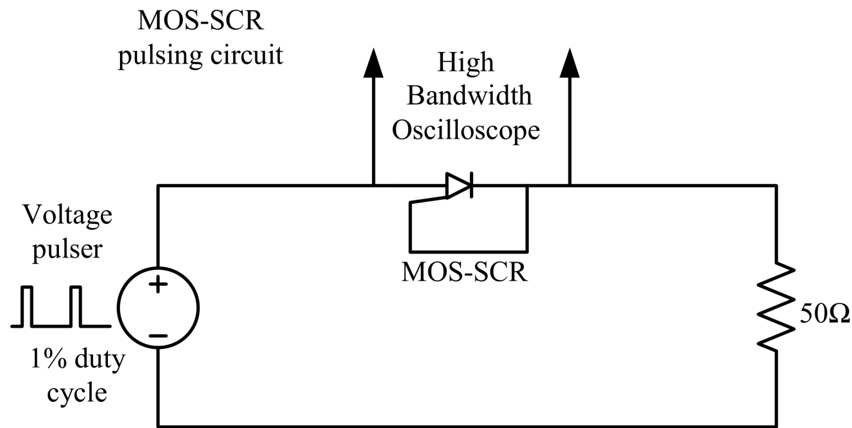

Figure 5.1: Circuit diagram for pulsed transient thermoreflectance imaging of the semiconductor controlled rectifier (SCR) in snapback operating mode.

ohm terminator. These specifications enabled loading of the SCR with pulse waveforms comparable to those produced by transmission line pulsers in the context of human body model and machine model ESD testing [37], or pulses on the order of 3A for 100 nanoseconds with rise time less than 5 nanoseconds.

Figure 5.2 shows a typical SCR electrical waveform for a 300 nanosecond long pulse using the described test setup. When supplied with a voltage pulse of sufficient fast rise time and amplitude in excess of the breakdown voltage (VBR,) drain-gate capacitive coupling triggers the SCR into snapback operating mode. The structure enters breakdown (VBR=106V) approximately 10 nanoseconds into the ESD pulse, undergoes an unstable period (t=10-100 nanoseconds) of changing device internal resistance, then stabilizes at a holding voltage (VH) and current after 100 nanoseconds. All thermal images in this study showing SCR self heating in snapback mode were acquired during this quasi steady-state part of the electrical waveform after 100 nanoseconds.

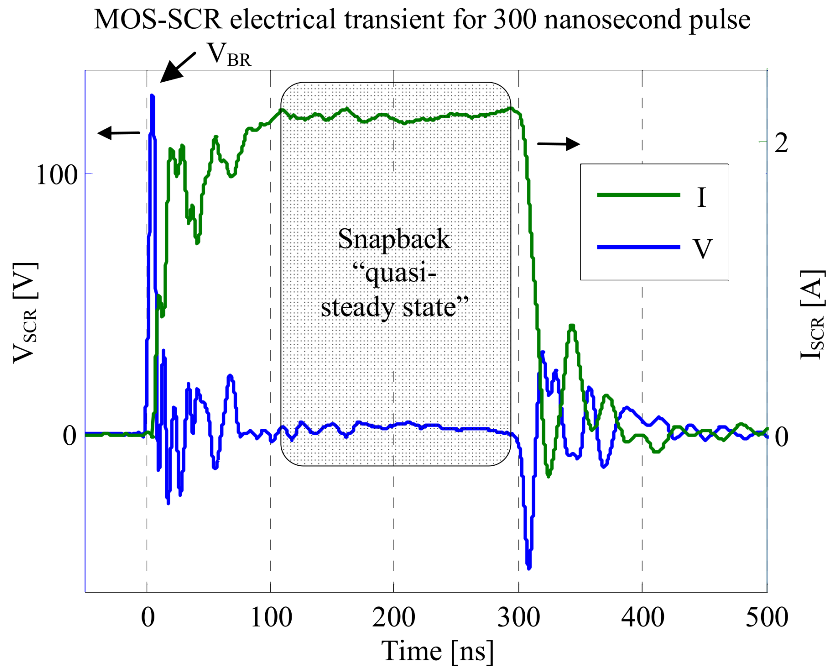

Figure 5.2: Electrical waveform showing SCR device voltage and current for a 300 nanosecond simulated electrostatic discharge (ESD) pulse. Thermoreflectance images as well as snapback holding voltage and current were acquired during the "quasi steady state" time duration of the waveform (approximately between time = 200 ns and 300 ns).

The pulsed I-V curve for the SCR is shown in Figure 5.3. Values are included to show both the open circuit behavior of the SCR for pulses below the breakdown voltage and also the current sourced while in snapback at the holding voltage. The snapback currents were measured from the quasi-steady state portion of the pulse waveform. Also shown in Figure 5.3 is gate leakage current, which was checked using 100V direct current after every pulse to ensure the SCR was not damaged. For thermoreflectance imaging, SCR snapback current levels were chosen between 1.15 and 1.47 amperes and pulse widths were chosen between 100 nanoseconds to one millisecond. The influence of photogenerated carriers on SCR device triggering is assumed negligible due to the

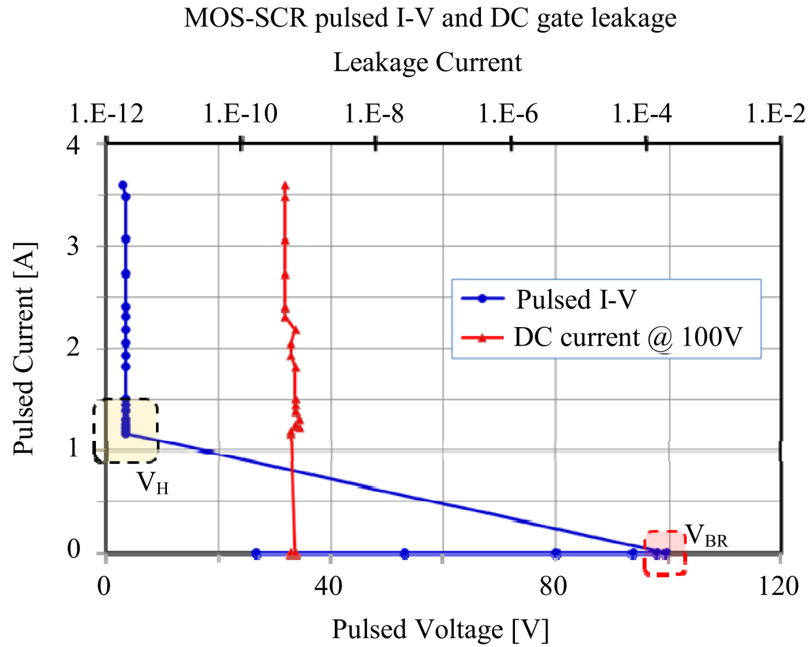

Figure 5.3: SCR device pulsed current and voltage below breakdown voltage and at snapback holding voltage. DC gate leakage current was measured after each pulsed measurement.

low intensity of the external LED illumination. (Unlike scanning imaging methods, which focus the illumination to a high intensity spot, camera based thermoreflectance methods distribute the illumination over the full device.) This assumption is supported by the observation during experiment that neither the SCR breakdown voltage nor the electrical waveform showed any dependence on whether the external LED was enabled or disabled.

An optical image of the ESD NLDMOS-SCR is shown in Figure 5.4. The 80 micron square layout has three aluminum anode fingers and two cathode fingers. In pulsed mode the snapback device is triggered by drain-gate capacitive coupling in response to ESD pulses with sufficient amplitude and rise time. The NLDMOS-SCR

structure enters breakdown (VBR=106V) approximately 10 nanoseconds into the ESD pulse, undergoes an unstable period (t=10-100 nanoseconds) of changing device internal resistance, then stabilizes at holding voltage and current after 100 nanoseconds. All thermal images in this study showing SCR self heating in snapback were acquired during this "quasi steady state" time duration of the electrical waveform after 100 nanoseconds.

Thermal images have been captured to analyze non-destructive current localization over the first 300 ns in response ESD like pulses. Submicron transient thermal images show isolated single finger triggering in the SCR with hot spots that move to different locations on the device in 100s of nanosecond time scale. In addition, dominant heating is shown to alternate between active fingers at different snapback current levels.

5.4 Results

5.4.1 Semiconductor controlled rectifier self-heating in snapback for different current levels

Temperature rise distribution in the SCR was studied for increasing current levels while in snapback mode. In snapback, the SCR maintains a constant reference or holding voltage that is effectively independent of the current through the diode. Figure 5.4 shows transient thermoreflectance CCD images of the MOS-SCR for snapback current levels I=1.22 and 1.33 amperes. The images were acquired at time = 300 nanoseconds after the rising edge of the excitation pulse. Snapback holding voltage is constant (VH=3.4V.) The thermal images at 300 nanoseconds revealed dominant

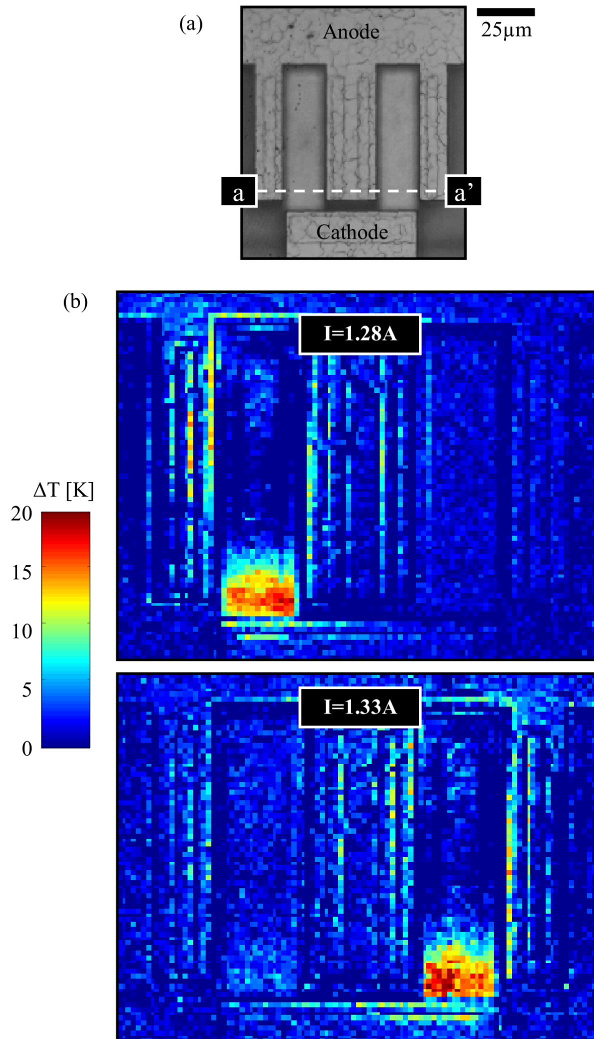

Figure 5.4: SCR self-heating in snapback for different current levels. (a) Optical image of MOS-SCR ESD protection device. (b) Transient thermoreflectance images of SCR for snapback currents of 1.28 A and 1.33 A. Time = 300 ns.

heating confined to a 20 micron region of the cathode finger near the cathode pad metal. Figure 5.5 shows thermoreflectance temperature change profiles perpendicular to the SCR fingers (profile a-a') for snapback current levels I=1.15 through 1.47A. Between I=1.15A (onset of snapback) and I=1.28A, hot spots occur only in the left

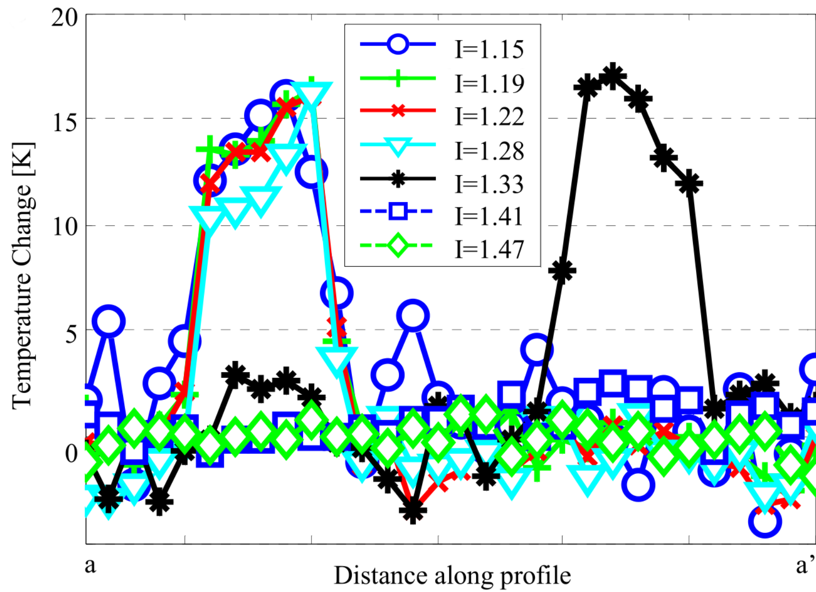

Figure 5.5: SCR self-heating in snapback for different current levels. Thermoreflectance measured temperature change for the indicated profile line a-a' in across the three SCR anode fingers and two cathode fingers for snapback currents between 1.15 A and 1.47 A.

cathode finger and the maximum temperature change is 17K. At I=1.33A, dominant heating switches to the right cathode finger, and temperature increases by two degrees. At the next current level, I=1.41A, no hot spot is seen and measured self heating decreases almost to the level of the background thermoreflectance noise level. One possible explanation for the apparent turn-off of heating at I=1.41A is that the current filamentation threshold has been exceeded. At lower current, power and heating is concentrated in a single cathode finger. If higher currents produce a more uniform power distribution, for example across both cathode fingers, then localized self heating is reduced.

5.4.2 Time dependence of SCR self-heating in snapback

Thermoreflectance images of heating in the SCR during snapback were obtained at several different times in the thermal transient ranging between 300 nanoseconds and one millisecond. A clear time dependence was observed in both magnitude and spatial distribution of the temperature change across the SCR. Bias conditions were constant for all images in the thermal transient, with snapback current = 1.22A, and holding voltage = 3.4V. Three characteristic time regimes became apparent in the SCR self heating transient. During the first 300-1000 nanoseconds (for a 300 nanosecond square pulse) temperature change was less than 20K and heating was confined to a single cathode finger (Figure 5.4.) Figure 5.6 shows the thermoreflectance images and temperature change profiles at 30 and 170 microseconds. In this time regime maximum self heating increases to T=400K and dominant heating appears to switch from left cathode finger to right cathode finger. This phenomenon might be explained by high speed current localization or non-simultaneous triggering of different finger junctions. Figure 5.7 shows SCR heating one millisecond into the transient, when device heating appears to reach thermal steady state. Heating is observed to spread to the anode fingers and become symmetric with respect to the device fingers, favoring neither the left nor right side of the SCR.

Current localization and thermal induced changes in the material and device properties should be the cause of heat switching fingers during the microsecond portion of the thermal transient for the SCR in snapback. One should note that typically

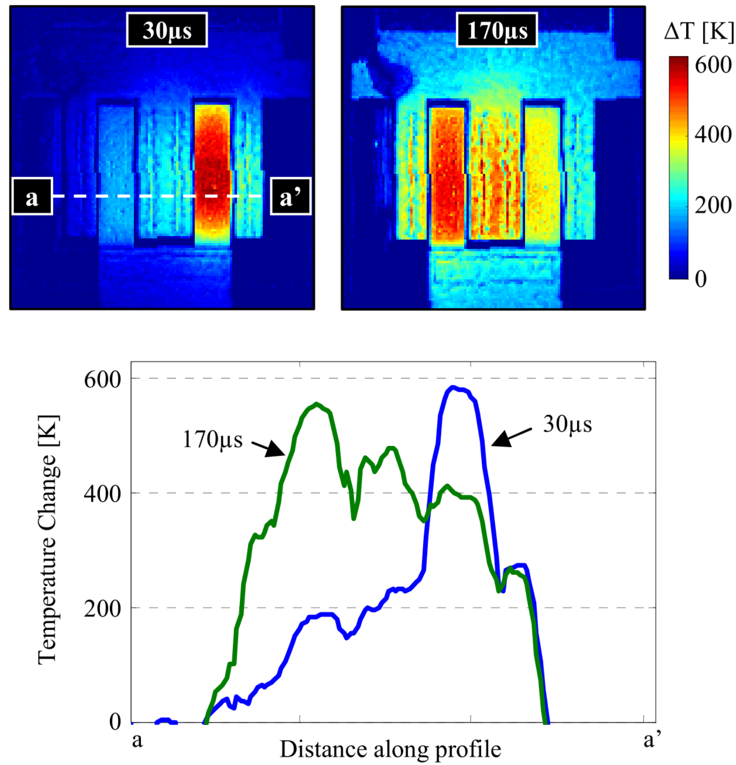

Figure 5.6: SCR transient thermoreflectance images and temperature profiles at 30 microseconds and 170 microseconds after snapback triggering. Snapback current is 1.22 A for both images.

thermoreflectance coefficient is calibrated for small temperature variations. When temperature rise is several hundreds of degrees, the nonlinear dependence of the reflection coefficient as a function of ambient temperature should be taken into account. Thus more accurate calibrations are necessary in order to quantify the exact temperature rise. However the measured transient reflectance map should provide some information about the current non-uniformity in the device.

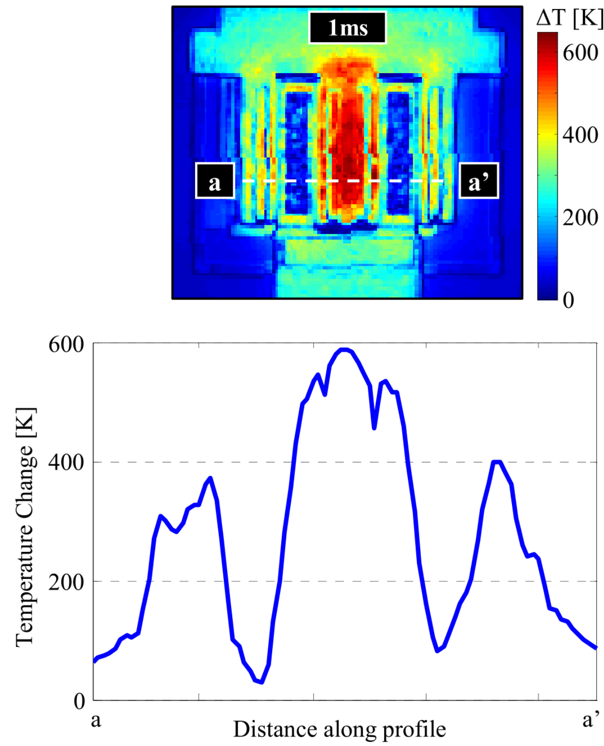

Figure 5.7: SCR transient thermoreflectance image and temperature profile at 1 ms after snapback triggering. Snapback current is 1.22 A, same as in fig.

5.5 Conclusion

Fast pulsed transient thermoreflectance imaging with 50 nanosecond time resolution has been applied toward indirect measurement of current distribution in electrostatic discharge protection devices during high power pulsed operation. Self-heating distribution in the device is inspected during snapback operation, providing information about the transient current distribution during a simulated ESD event. Experimental validation of the new approach is presented for a multiple finger NLDMOS-SCR ESD protection device. Thermoreflectance images of the SCR revealed non-simultaneous, nonuniform triggering of individual device fingers both as a function of snapback cur-

rent level and at different times in the thermal transient. Temperature change of 15 K was observed at hotspots on the SCR within the first 300 nanoseconds of the simulated ESD pulse. Temperature change in excess of 400 K was observed 30 microseconds into the pulse. Results demonstrate fast transient thermoreflectance imaging as an effective tool for characterizing device self-heating distribution in response to electrostatic discharge pulses or similar fast impulse electrical events.

Chapter 6

High spatial resolution thermoreflectance of silver nanowire percolation networks

6.1 Abstract

Transistors, Sensors, and transparent conductors based on nanotube/nanowire networks have found applications in flexible electronics, bio-chemical sensing, and solar cells. Lacking a high-resolution characterization of the network, the percolating transport is presumed linear and spatially homogenous, although, in practice, the devices operate in the nonlinear regime. In this study, we use thermoreflectance imaging with submicron spatial and 50 mK temperature resolution to map self-heating and hotspot formation, and find that transport is dominated by nonlinear thermal and electrical resistances. High resolution thermoreflectance imaging reveals heterogeneity not ob-

servable with macroscopic characterization. The response differs significantly between Ag-NW based vs. hybrid Ag-NW/graphene cooperating networks. The results encourage a fundamental reevaluation of the transport models and characterization results for these network-based percolating conductors.

6.2 Introduction

Randomly assembled networks describe a broad range of physical systems and processes. A simple classification suggests that some networks are static (e.g. CNT or Ag nanotube network, network of highways), while others dynamic (e.g. social networks), yet others parametric (e.g. bias dependent network during metal-insulator transition, or puddle-transport in graphene [1]). Percolation models had been originally developed to describe linear-response transport in static/parametric random networks, although the distinction - as we will see - is often artificial. [11,35,71,72,77] Percolation models have recently been generalized to nonlinear response (including electro-thermal coupling) for CNT nanotube network, however, a fundamental presumption regarding the network persists: the microscopic properties such as local resistivity or thermal conductivity does not evolve with operating conditions. The assumption is clearly unphysical, but the degree to which it is violated in practical networks and the implication thereof in interpreting results, remain unexplored.

From a material perspective, nanoscale networks have recently been the focus of efforts to exploit and tune the unique properties of percolation transport systems,

opening a design path toward artificial composites with applications such as transparent electrodes for photovoltaics, light and flexible electrodes for supercapacitors, and multi-functional polymer nanocomposites. [17, 45, 55] Nanoscale network materials consisting of two or more nanostructures (henceforward called hybrid materials) have emerged to produce device applications such as transistors built from a 1-D network of nanotubes/nanowires (called nanonet-FETs), hybrid transparent conducting electrodes, and electrodes for super capacitors and Li-ion batteries. [32, 49, 86] Recently we have experimentally validated co-percolation transport in hybrid graphene/silver nanowire network devices that circumvent the transport bottlenecks of individual components of the hybrid, thus demonstrating record performance in the electrical conductivity and optical transmittance. [18,46] In each of these applications, the network operates at high-current and/or high voltage regime, and yet, the analysis presumes that the network is defined by bias-independent microscopic parameters. Obviously, engineering high quality network materials will ultimately require understanding the microscopic behavior of these systems. Microscopic characteristics not only influence practical design and reliability, but also provide insight to the underlying physical transport mechanisms.

Measuring temperature with high spatial resolution is one method for probing microscopic properties of nanoscale networks. This study uses thermoreflectance imaging with submicron spatial resolution to probe electrically induced nanoscale self-heating in network devices. Two network materials are considered: a network of silver nanowires only, and a hybrid network of silver nanowires wrapped by single layer graphene.

Scanning thermal metrology techniques such as scanning probe thermocou-

ple microscopy, scanning Joule expansion microscopy, and surface-enhanced Raman spectroscopy have been employed to estimate the temperature in nanoscale dimensions. [41, 65] For thermal characterization of nanoscale network devices, thermal imaging methods have the advantage of simultaneous measurement of large regions of the network device. Choosing the appropriate microscope magnification permits inspection of self-heating over a broad range of spatial resolution. Recently, infrared thermography imaging was used by Estrada et al on carbon nanotube network transistors to find hot regions during operation and extrapolated to conclude that transport, dissipation, and reliability of the network are limited by the tube-tube junctions. [30] Like infrared imaging, thermoreflectance imaging can quickly measure temperature distribution over large regions of a sample, up to about one square centimeter in area. However, thermoreflectance imaging can also measure temperature distribution with submicron spatial resolution. In this study, thermoreflectance imaging recorded hotspots of individual nanowire junctions corresponding to regions approximately 300 nanometers square. To our knowledge this is the first measurement of self-heating over large region of a nanowire network device with submicron spatial resolution.

This method enabled the measurement of self-heating distribution for discrete nanowires and nanowire junctions within the network. As expected, the measurements revealed local, microscopic electrothermal variability and inhomogeneity in the nanoscale networks, a characteristic generally not observed in uniform materials. Remarkably, however, self-heating over a range of current excitations revealed local hotspots at silver nanowire junctions in the network that indicated a temperature de-

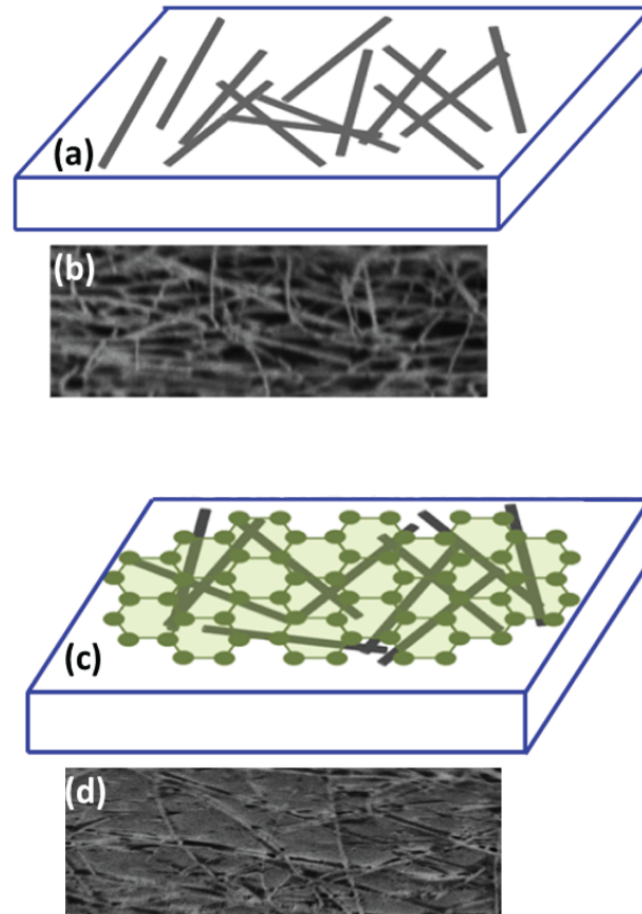

Figure 6.1: Silver nanowire network devices. Schematic representation (a) and scanning electron microscope image (b) of silver nanowire network. Schematic (c) and SEM image (d) of hybrid graphene-silver nanowire network. Individual silver nanowire diameter is 90 nanometers.

pendence on power that exceeded the prediction of joule self-heating in bulk silver, clearly indicating parametric response to the operating conditions. The implication of this spatial and parametric inhomogeneity is significant: thermoreflectance images provide direct evidence that sheet resistance of these networks derived using classical test devices may often be reported incorrectly; in practice, the network resistance could be considerably superior to those calculated from classical theory of homogenous transport.

To illustrate the general principles, we investigated the electro-thermal properties and self-heating of two nanoscale network devices: a silver nanowire network device (Figure 6.1a,b) and a hybrid single layer polycrystalline graphene-wrapped silver nanowire network device (Figure 6.1c,d) with a similar density of nanowires as the first case. Henceforward, these two networks will be distinguished by the description nanowire network device and hybrid network device respectively. Thermoreflectance imaging revealed an order of magnitude lower self-heating at nanowire-nanowire junctions in the hybrid system compared to similar junctions in the nanowire network.

6.3 Experiment

6.3.1 Device description

Fabrication of the nanowire network device (silver nanowire) and hybrid device (single layer polycrystalline CVD graphene deposited on a silver nanowire network with a similar density of wires) was reported earlier in [18] Circular concentric inner and outer electrodes were fabricated to minimize parasitic electric field fringing during electrical characterization of the networks film.

6.3.2 Thermoreflectance imaging method

Thermal images were obtained using a thermoreflectance charge coupled device (CCD) camera system capable of submicron spatial resolution and 50 mK temperature resolution. Full field thermal images were acquired quickly with no scanning of

the instrument required. Low magnification measurement of the network devices were obtained using a 20 X lens, producing thermoreflectance images with a field of view covering approximately 450 square microns of the chip with pixel resolution corresponding to approximately 500 nanometers. Individual low magnification thermoreflectance images show the full network device, consisting of inner and outer electrodes and the network channel between the electrodes. High magnification thermoreflectance images were obtained using a 100 X lens, producing image field of view covering approximately 100 square microns and pixel resolution of approximately 30 nanometers. High magnification images resolved submicron local self-heating hotspots at individual nanowire junctions.

The transient thermoreflectance differential algorithm described in 2.1.2 was used to image self-heating in the network devices. Though the transient algorithm is capable of measuring fast thermal effects, it is equally capable of inspecting steady state self-heating, provided the device excitation pulse width is sufficiently long. A diagram of the thermoreflectance imaging experiment setup is shown in Figure 6.2. The top surface of the network device was illuminated using a narrowband, 530 nm light emitting diode (LED.) The network devices were probed on the wafer. Square current pulses were applied across the sample inner and outer electrodes with a pulse width of 1 millisecond at a 15% duty cycle. Thermoreflectance images in this study were averaged for 20 minutes of continuous sample excitation at a 150 Hz lock-in repetition rate, producing signal to noise ratios equivalent to 0.2 K error in low magnification images and 3.0 K error in high magnification images. The thermoreflectance coefficient

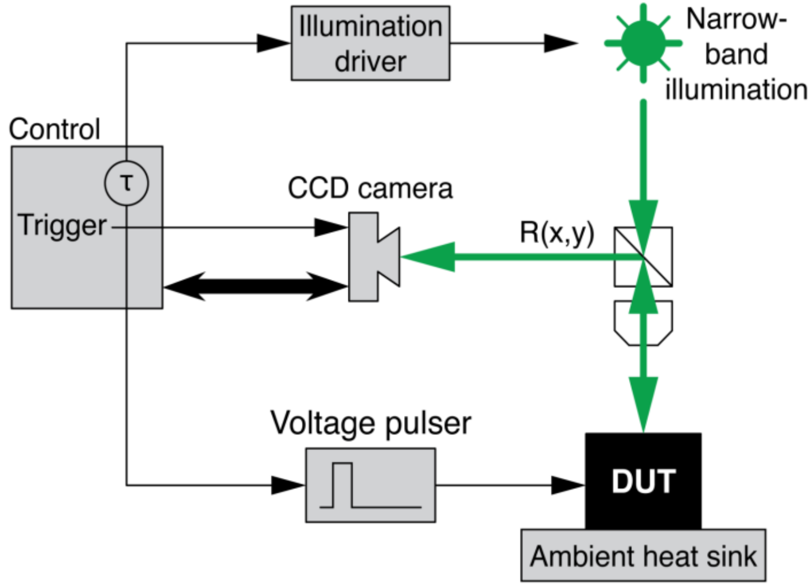

Figure 6.2: Thermoreflectance imaging microscope experiment configuration. Nanowire network device excitation pulse width was 1 millisecond. Duty cycle was 15%. Illumination (LED) wavelength is 530 nanometers.

(C_{TH}) for the silver nanowires in the network was extracted indirectly. Because the thermoreflectance coefficient for the gold electrodes is known, measured temperature change on the gold electrodes can be used to estimate temperature change on, and therefore thermoreflectance coefficient for adjoining silver nanowires that are a very short distance- less than 100 nm–from the electrode. For 530 nm LED illumination at 20 X magnification, the estimated silver nanowire thermoreflectance coefficient was $C_{TH,AgNW} = 1.7 \times 10^{-4}\,K^{-1}$. For comparison, at the same illumination wavelength and magnification the thermoreflectance coefficient for the electrode gold is $C_{TH,Au} = -2.4 \times 10^{-4}\,K^{-1}$. Thermoreflectance imaging has been used in thermal characterization of a broad range of integrated devices and bulk materials, however, this is the first time the technique has been used to probe self-heating in silver nanowire networks.

6.4 Results and discussion

6.4.1 Macroscopic network self-heating (low magnification)

Figure 6.3 shows the low magnification (20 X) optical images and corresponding thermoreflectance images for (a) nanowire and (b) hybrid network devices. Pixel resolution for the low magnification images is 0.8 microns per pixel. Visible in the optical images are the samples concentric inner and outer gold electrodes. The channel is the region between these contacts, with a length of 100 microns. At this magnification, thermoreflectance images measure the ensemble thermal properties of the network or self-heating in nanowire clusters. Thermoreflectance images were obtained for both nanowire network and hybrid network devices as the applied current was swept from I=0 to 37 mA. Figure 6.3 shows the thermoreflectance images at selected bias points of I = 2, 10, 17, 23, and 31 mA for both nanowire and hybrid samples. The thermal images show temperature change in the nanowire network due to self-heating for each applied current bias using the square pulse excitation scheme described in the experiment section. The thermoreflectance images are calibrated for the silver nanowires. Consequently, temperature change data shown is valid only for regions corresponding to silver nanowires in the network. Thermoreflectance response of the substrate, and graphene in the case of hybrid samples, was below measurement threshold for the magnitude of temperature change induced in the devices and duration of image averaging in this experiment. Longer averaging combined with illumination wavelength optimized for graphene may permit measurement of temperature distribution on the graphene.

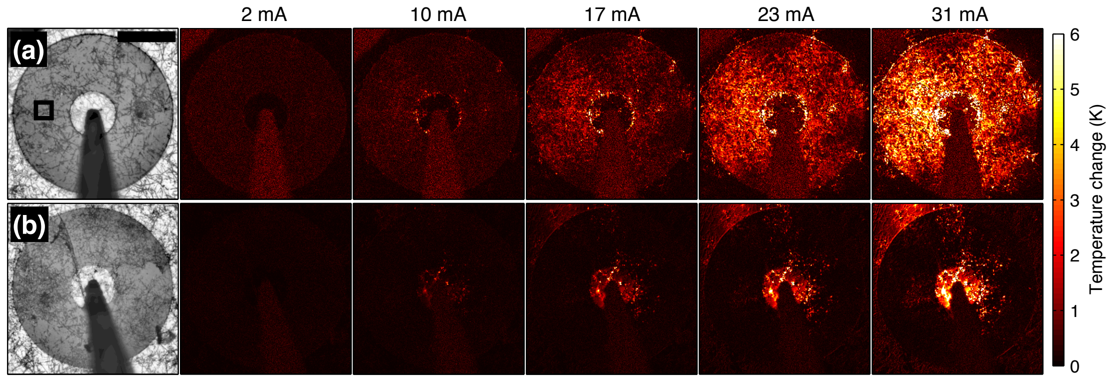

Figure 6.3: Low magnification (20 X) macroscopic self-heating in nanowire and hybrid network devices. (a) Optical image of full nanowire network device (scale bar is 100 microns) and corresponding thermoreflectance temperature change images for selected applied total device current. Active network channel length (distance between inner and outer concentric electrodes) is 100 microns. Spatial heterogeneity of ensemble nanowire self-heating visible in the image for I = 31 mA, with regions of higher and lower temperature change over distances corresponding to clusters of nanowires. (b) Optical and thermoreflectance images for hybrid network device with same contact geometry as nanowire network device. Visual inspection at the same current reveals self-heating magnitude is lower in the hybrid network than in the nanowire network.

Several characteristics are immediately evident. First, self-heating is prominent in the hottest sample (i.e. the nanowire network sample at I = 31 mA), with thousands of hotspots occurring throughout the channel region. Additionally, the spatial distribution of self-heating in the network at this magnification can be qualitatively described as simultaneously uniform (homogeneous) over large areas of the network and nonuniform (heterogeneous) over smaller areas. For the purposes of this analysis, let us define large areas as being equal to a 30 x 30 micron sampling box as illustrated in the optical image of Figure 6.3a. Henceforward we will use this sampling box in discussions of network macroscopic properties, because an area of the network with these dimensions encloses a random cluster of nanowires, junctions, and–for the hybrid case–a

large area of graphene. Quick inspection of the corresponding thermoreflectance image at $I = 31$ mA shows average temperature change of all pixels inside the macroscopic sampling box falls within the range of 3.5 to 5 K for all but a few regions of the active channel. This implies macroscopic self-heating in the network channel is generally homogeneous. However, inspection also suggests self-heating at smaller scales is not uniform. For example, the pixel to pixel temperature distribution inside the 30 x 30 micron sampling box reveals both hot (6 K) and cold (0 K) regions randomly distributed within the network. This nonuniformity, which is discussed later, hints at heterogeneous self-heating at the microscopic scale, as would be expected for a classical percolating network. Another prominent characteristic is the relative magnitude of macroscopic self-heating distribution in the respective nanowire and hybrid samples. At 31 mA, macroscopic self-heating in the nanowire sample (a) shows average temperature change in the range of 4 K over the full channel. In comparison, the hybrid sample (b) at the same current amplitude shows only a few regions of self-heating scattered throughout the channel, and the average macroscopic temperature change for these regions is 1 to 2 K.

6.4.2 Implications: Measure of network thermal inhomogeneity

Inhomogeneity was observed for self-heating in ensemble nanowire clusters in the low magnification thermoreflectance images. Figure 6.4 compares self-heating magnitude in four quadrants of the nanowire network channel. Plotted temperature change was calculated from the mean of all pixels within a sampling region, in this case by

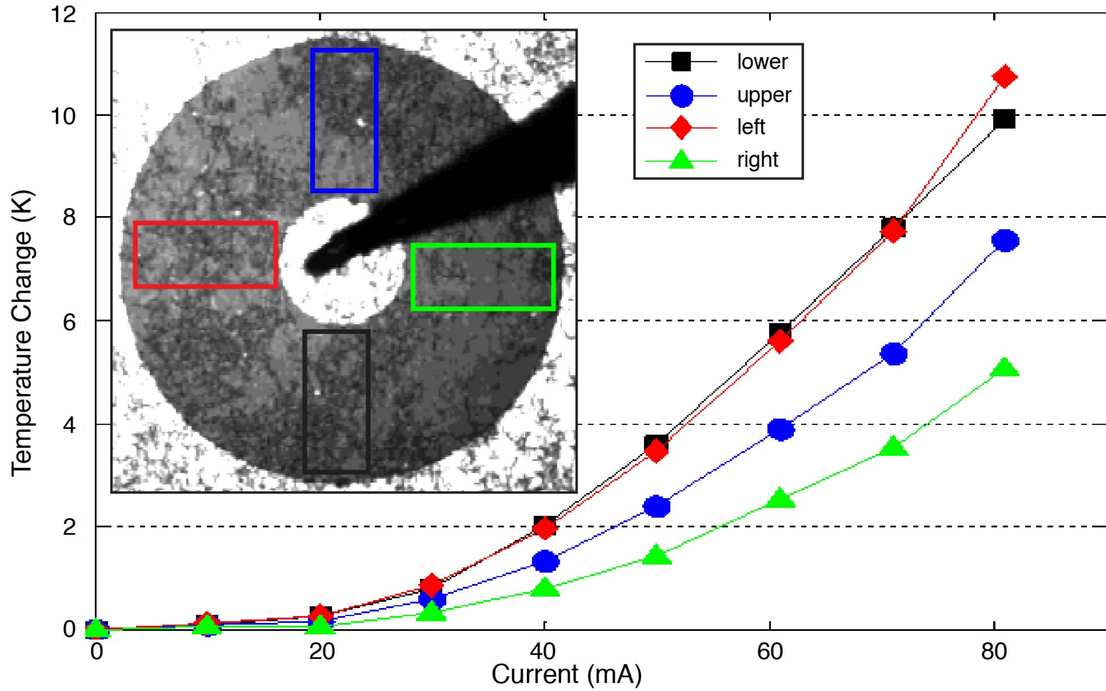

Figure 6.4: Network self-heating heterogeneity at low magnification. Plot shows ensemble self-heating in four quadrants of the nanowire network channel shown. Sampling regions are approximately 100 x 50 microns. Ensemble nanowire heating varies spatially by as much as a factor of 1.7 (between left and right quadrants).

four rectangles in different quadrants of the network channel as indicated in the optical image of the device in Figure 6.4. Each of the four sampling regions encloses an area of approximately 50 x 100 microns. The plotted temperature change versus total device current for the four quadrants reveals that self-heating varies by as much as a factor of 1.7 between the left quadrant (13 K) and right quadrant (7.5 K) at 80 mA current. The observed variation in ensemble self-heating in different quadrants of the network channel provides an estimate of the inhomogeneity of the underlying nanowire distribution in the network. Measured temperature change is a coupled effect depending on both the spatial distribution of nanowire density and the spatially varying thermal resistance in

the network.

6.4.3 Microscopic network self-heating (high magnification)

Microscopic self-heating distribution in the network devices was inspected using thermoreflectance imaging with high magnification. Figure 6.5 shows the high magnification (100 X) optical images and corresponding thermoreflectance images for (a) nanowire and (b) hybrid network devices. The scale bar in Figure 6.5a (also valid for Figure 6.5b) is five microns. Pixel resolution is approximately 50 nanometers per pixel. At this magnification, discrete nanowires in the network are clearly visible in the both the optical and thermoreflectance images. Thermoreflectance images are shown for increasing current bias applied to the network device.

Several interesting characteristics of the network microscopic temperature distribution are evident from visual inspection of the high magnification thermoreflectance images. Foremost is visual confirmation of the spatial variation in self-heating between individual nanowires and nanowire junctions during electrical excitation. Heterogeneous (nonuniform) self-heating at the microscopic scale in the network is first observed in the nanowire network device thermoreflectance image for $I = 10$ mA. In this image, temperature change for individual wires varies between 0 to 6 K, with temperature resolution of 0.8 K. Microscopic network temperature resolution was estimated from the half-width of the Gaussian noise distribution in the thermoreflectance image when no current is applied to the device. Nanowires and junctions with temperature change of 0 K indicate regions of the network with either no electrical excitation (hanging

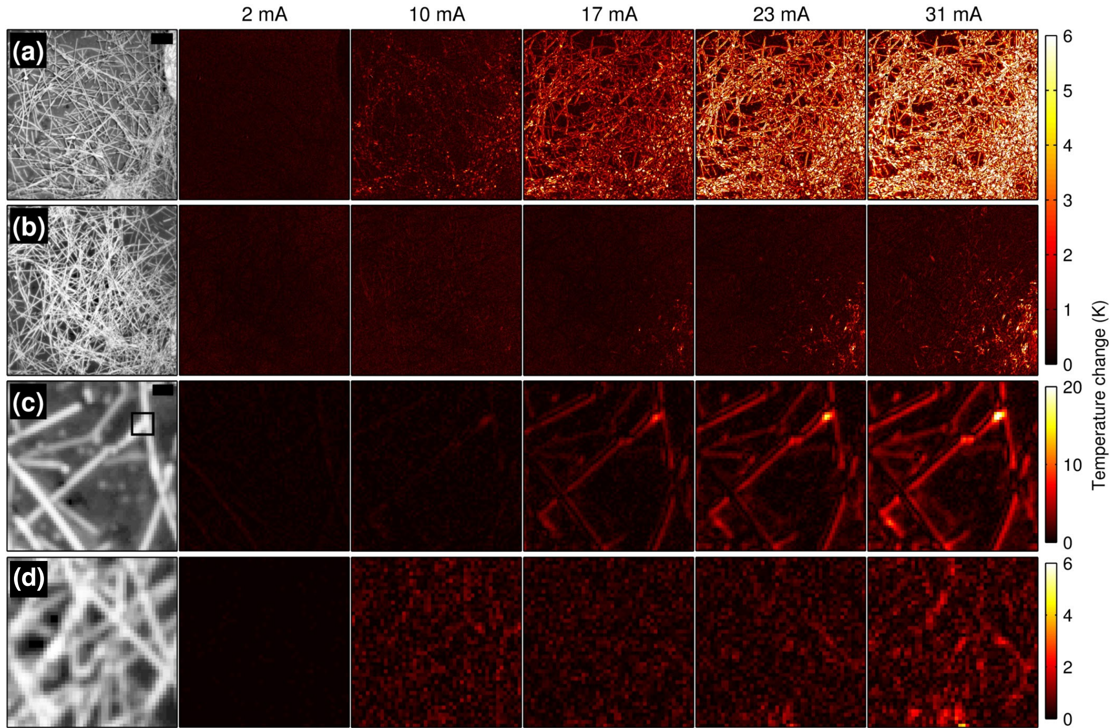

Figure 6.5: High magnification microscopic self-heating in nanowire network and hybrid network devices. (a) 100 X optical image of nanowire distribution in channel of nanowire network device and corresponding thermoreflectance temperature change images for selected applied total device current. Scale bar in (a) is five microns. Microscopic spatial variation in network self-heating is visible in the nanowire network channel for currents above 10 mA. (b) Optical image and corresponding thermoreflectance images for the hybrid network device, with same scale as (a). Magnitude of microscopic self-heating is lower in the hybrid network channel, but similar local hotspots are evident at higher device current. (c) Enlarged region of nanowire network channel showing representative hotspots for discrete nanowires and nanowire junctions. Scale bar is 300 nanometers. Large temperature gradients (up to 20 K) observed between hot and cold regions of individual nanowires and nanowire junctions. (d) Enlarged region of hybrid network channel showing representative hotspots. Representative hotpots in hybrid channel are 5 K, compared to 20 K for nanowire channel.

or isolated branches) or negligible electrical or thermal resistance. Hot nanowires and nanowire junctions (temperature change of 6 K and greater) indicate locations of microscopic hotspots with higher power dissipation due to either electrical bottlenecks in

high conductance pathways in the network or higher local thermal resistance. Similar temperature nonuniformity is observed in the hybrid microscopic temperature distribution at $I = 31$ mA. However, it is notable that even at higher currents, the hybrid network has fewer hotspots with a temperature change of 6 K or greater compared to the nanowire network.

Figure 6.5c shows an enlarged high magnification optical image of the nanowire network device with corresponding thermoreflectance images. The scale bar is 300 nanometers and pixel resolution is approximately 50 nanometers per pixel. The enlarged thermoreflectance images reveal detailed microscopic nonuniformity in network self-heating distribution for individual nanowires and nanowire junctions. Comparing the optical image to the thermoreflectance image at $I = 31$ mA, this sub-region of the network contains examples of both local hotspots (the nanowire junction in the upper right of the image) and passive nanowires with small or zero temperature change. One prominent feature of the microscopic thermal distribution is that local hotspots can be significantly hotter than the average temperature change within the network. Temperature change for the visible hotspot junction at $I = 31$ mA exceeds 20 K, while no nanowire or junction in the vicinity of the hotspot has temperature change greater than 10 K. This result affirms the importance of high resolution mapping - the local temperature rise (and any nonlinear effect associated thereof) would be considerably underestimated in low-magnification imaging. Figure 6.5d shows enlarged optical and thermoreflectance images for regions within the hybrid network channel. The temperature scale for the enlarged hybrid thermoreflectance images is adjusted to allow

comparison of magnitude and distribution of representative hotpots to the nanowire case. Hotpots in the hybrid channel are typically 5 K, compared to 20 K for nanowire channel.

6.4.4 Network linear and nonlinear self-heating at different spatial domains

Figure 6.6a quantitatively compares magnitude of macroscopic self-heating for two nanowire network devices and three hybrid network devices, all with same nominal nanowire density and contact geometry. Temperature change is plotted versus current over the range $I = 0$ to 31 mA. Temperature change for each current bias data point was calculated from the mean temperature change of all pixels within a 30 x 30 micron sampling box enclosing a highly active region of the network channel in the thermoreflectance image. The dimensions of the sampling box are illustrated in the optical image of Figure 6.3a. For each device, the sampling box was positioned over a 30 x 30 micron region of the network channel that displayed the greatest temperature change at $I =$ 31 mA as determined by visual inspection of the thermoreflectance image. At a given current level, the temperature increase in the nanowire network samples is significantly higher than for the hybrid sample, with increase 5-10 times at the higher current levels.

Self-heating in Ohmic materials under electrical excitation is described by Joule's law, which states power is proportional to the square of current,

$$P = I^2 R, \tag{6.1}$$

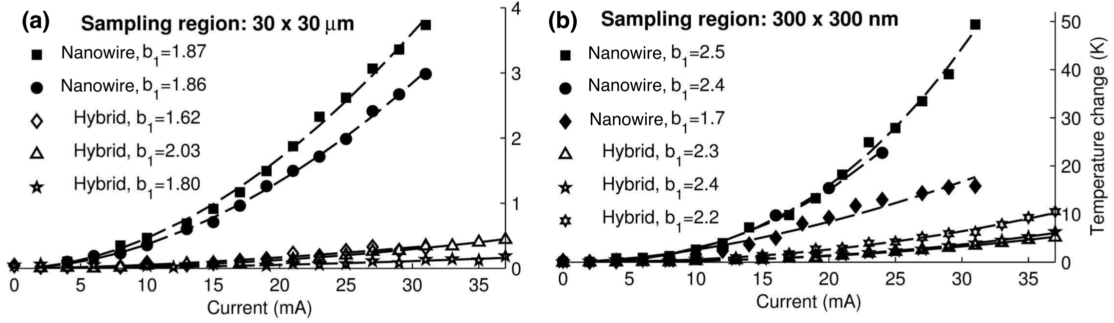

Figure 6.6: Self heating in the network channel compared for macroscopic and microscopic sampling regions. (a) Macroscopic ensemble self-heating temperature change versus total device current for two different nanowire network devices and three different hybrid network devices. Temperature change was calculated from the mean value of all pixels in a 30 x 30 micron sampling box in the active channel regions of the thermoreflectance images (a representative 30 x 30 micron box is shown in Figure 6.3a). Fit to power model $\Delta T = a_1 I^{b_1}$, explained in text, shows $b_1 < 2.0$ for all network devices. Plot reveals magnitude of ensemble self-heating is five to ten times greater in the nanowire network compared to the hybrid network at the same current. (b) Temperature change versus current for microscopic hotspots in the network devices. One hotspot is plotted from each of three different nanowire network devices and three different hybrid network devices. Hotspot temperature change was calculated from the mean temperature change of all pixels within a 300 x 300 nanometer sampling box in the thermoreflectance image. A representative 300 x 300 nanometer sampling box is shown in Figure 6.5c for a nanowire junction corresponding to a hotspot in one of the nanowire network channels. Plotted hotspots are selected from the top 10% hottest spots in the respective network channels. Microscopid hotspot curves fit to same power model reveal temperature dependence of current for microscopic hotspots exceeding prediction for Joule self-heating, with $b_1 = 2.2 to 2.5$.

where P is the power dissipated in the device, I is the total current through the device, and R is the device electrical resistance. Using the steady state heat equation, temperature change within the network channel can be expressed as a function of applied current,

$$\Delta T = a_1 I^{b_1}, \tag{6.2}$$

where the parameter a_1 combines both device electrical resistance and device abso-

lute thermal resistance, which are assumed constant for most bulk materials over a small range of temperature change. The parameter b_1 is the exponent of current. For Ohmic bulk materials Joule's law states that $b_1 = 2$. Network macroscopic self-heating temperature change was fit to this Joule model (6.2). Figure 6.6a shows the fits and corresponding value of b_1 for each device measured. Fitting suggests macroscopic self-heating in the network is at or slightly below the temperature predicted by Joule's law. This relationship will be explored further later in this paper by comparing the macroscopic and microscopic self-heating properties of the network. The much lower magnitude of self-heating observed in the hybrid networks compared to the nanowire networks is strong evidence of the hybrid distribution properties of this material. Electronic co-percolation would have the effect of spreading current over a larger area in the network, resulting in lower power densities and fewer local hotspots.

Figure 6.6b plots temperature change versus current for microscopic hotspots in the network devices. One hotspot is plotted from each of three different nanowire network devices and three different hybrid network devices. Microscopic hotspot temperature change was calculated from the mean temperature change of all pixels within a 300 x 300 nanometer sampling box in the thermoreflectance image. Dimensions of the microscopic sampling box are illustrated by square outline in the optical image of Figure 6.5c. The size of this sampling region is comparable to three times the diameter of the nanowires, or about four times the area of a single nanowire junction. Images of the microscopic electrothermal distribution at these length scales in active network structures have not been reported previously. The hotspots were selected from the

hottest 10% of the full temperature change distribution in the high magnification thermoreflectance images. These microscopic hotspots, typically located at or near nanowire junctions, are self-heating outliers, but represent critical performance bottlenecks in the network. Several features are notable in the plot of network microscopic hotspot temperature change versus current. The magnitude of self-heating for the hottest microscopic hotspots is much larger than the magnitude of self-heating observed in the macroscopic thermoreflectance images measured at low magnification (Fig. 6a) for the same total device current. For example, at $I = 31$ mA, microscopic hotspots in the nanowire network show temperature change in the range of 20 to 50 K, while the macroscopic (low magnification) temperature change for the same nanowire networks was in the range of 3 to 4 K. Comparing microscopic hotspots for nanowire and hybrid networks again showed magnitude of self-heating significantly reduced in the hybrid material for the same total current. The hottest microscopic nodes in the nanowire network devices were five to ten times hotter than the hottest nodes in the hybrid network.

Quantitative analysis revealed the hottest microscopic nodes in the network did not follow the self-heating temperature dependence of current predicted by Joule's law. The dashed lines in Figure 6.6b show the power model fit described by (6.2) for the microscopic hotspot temperature change versus total current applied to each network device. For all but one of the devices, the microscopic hotspot temperature increased at a rate in excess of the square of the applied current. The exponent of current ranged between $b_1 = 2.2$ to 2.5 for hotspots in both the nanowire and hybrid networks. The one outlier hotspot with $b_1 = 1.7$ exhibited similar self-heating over the lower range of

current, where $b_1 = 2.6$ for $I = 0$ to 17 mA. For this outlier hotpost, an inflection in the self-heating curve appears to occur at $I = 20$ mA, possibly due to self-heating induced change in local microscopic electro thermal properties.

The observation of "super-Joule" hotspots suggests that self-heating at the microscopic nanowire junction scale violates one or more conditions of Joule's law. We propose the super-Joule behavior is the result of self-heating dependent (i.e., non-constant) electrical resistance at the nanowire-nanowire junctions. Joule self-heating assumes electrical resistance is constant. We remove this condition and instead express electrical resistance at random microscopic hotspots in the network channel, R_1, as a function of self-heating power:

$$R_L = R_{L0} + b_2 P_L = R_{L0} + b_2 I_L^2 R_L \tag{6.3}$$

$$R_L = R_{L0}/(1 - b_2 I_L^2), \tag{6.4}$$

where R_{L0} is the local electrical resistance in the absence of any self-heating, P_L and I_L are the local power and local current respectively, and b_2 is a self-heating parameter. Power dissipated at the local hotspot expressed as a function of self-heating is

$$P_L = I_L^2 R_L = R_{L0} I_L^2/(1 - b_2 I_L^2). \tag{6.5}$$

We use Joule's law to predict local microscopic hotspot temperature change in terms of local electrical power and local absolute thermal resistance, R_{TH}:

$$\Delta T_L = P_L R_{TH}. \tag{6.6}$$

Substituting (6.5) into (6.6) yields

$$\Delta T_L = a_2 I_L^2/(1 - b_2 I_L^2), \tag{6.7}$$

where a_1 is a scaling factor incorporating local absolute thermal resistance and local electrical resistance in the absence of self-heating. Equation (6.7) presents a model for nonlinear (that is, non-Ohmic) self-heating of microscopic hotspots in the network channel where local microscopic resistance and self-heating are coupled. Local current is unknown at microscopic hotspots in the network. Consequently the relationship between the total network device current, I, and the local microscopic current, I_L, at any local hotspot within the network is undetermined. In view of this experimental unknown, microscopic hotpot self-heating was modeled as a function of total network device current.

Figure 6.7 compares microscopic hotspot temperature change versus total device current for the two self-heating models presented so far. Fit (1) is the power law of equation (6.2) which assumes device electrical resistance and thermal resistance are constant on both the macroscopic and microscopic scale in the network. Fit (2) is described by equation (6.7), which assumes local microscopic electrical resistance in the network is a function of local microscopic self-heating. Figure 6.7 shows a log-log plot of fit (1) and fit (2) based on measured local microscopic hotspot temperature change, ΔT, versus total current applied to the full network device, I. The expressions in Figure 6.7 for fit (1) and (2) omit subscript notation indicating local temperature change. The log-log plot includes fits for five of the six devices plotted in Figure 6.6b, with the outlier

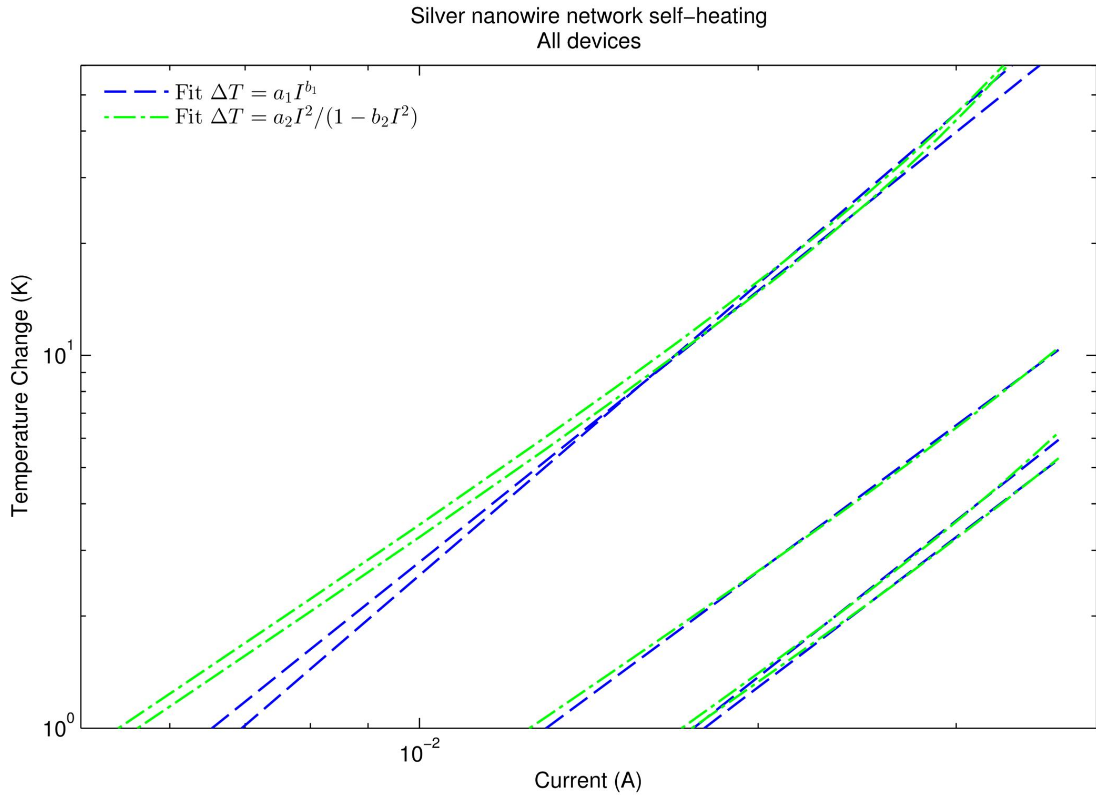

Figure 6.7: Log-log plot of temperature change versus current for fits (1) and (2) for microscopic junction hotspots selected from two different nanowire devices and three different hybrid network devices.

device excluded. Data points used for the fits are not shown to improve plot readability. The horizontal axis is scaled to emphasize the higher range of currents over which the network displays measurable self-heating. The slope of all the lines in Figure 6.7 exceed 2.0, the expected values for Joule heating. The coupled local self-heating model of fit (2) provides a sufficient, though incomplete, hypothesis for nonlinear self-heating at microscopic hotspots in the network. The observed nonlinear microscopic thermal properties of the nanowire networks will be the subject of future study.

6.5 Conclusion

Using high magnification thermoreflectance imaging, we demonstrated submicron heterogeneous self-heating in silver nanowire network devices. Significant spatial thermal variability was revealed both at the microscopic level for individual nanowires and nanowire junctions and for ensemble nanowire clusters. Local, submicron hotspots for discrete nanowires and junctions in the network displayed temperature dependence on current in excess of predicted Joule self-heating for similar bulk material. A hybrid nanowire network film demonstrated more uniform thermal distribution and significant reduction in self-heating compared to the nanowire network film. Thermoreflectance images with high spatial resolution motivated the revision of estimated network material properties, producing more accurate parameters and a better understanding of transport behavior within the network.

Chapter 7

Future work

7.1 Thermoreflectance imaging of self-heating in high frequency integrated devices under typical operating excitation.

Under standard operating conditions many modern high frequency electronics are being driven by sinusoidal or square wave voltage or current signals at megahertz and gigahertz frequencies. To date, characterization of self-heating in these high frequency devices under typical operating conditions has primarily been limited to measurement of temperature sensitive electrical parameters. However, purely electrical methods of thermal characterization do not provide information about the spatial distribution of local hotspots in devices. Many studies, including the work contained in this dissertation, have argued that device performance is limited by the local hotpots. Consequently there is great utility in techniques that provide spatial thermal information of high fre-

quency devices. The FFT thermoreflectance imaging algorithm discussed previously is limited to frequencies below 200 Hz and is therefore not suitable. The pulsed transient thermoreflectance algorithm can measure fast transients in response to individual pulses with subnanosecond time resolution, but this method in its standard configuration uses a low duty cycle pulse excitation waveform, not a continuous sinusoidal or square waveform at 50% duty cycle.

The author proposes a novel method for characterizing self-heating in high frequency devices under standard electrical excitation using a transient superposition thermoreflectance scheme. The method is based on a modified version of the pulsed transient thermoreflectance algorithm already discussed in this dissertation. Figure 7.1 shows the proposed superposition timing signals to capture images of self-heating in a hypothetical high speed field effect transistor power amplifier. A sinusoid or square wave at standard operating frequencies of MHz to GHz is applied to the gate of the transistor. The lock-in transient pulse waveform is applied to the transistor drain as a "trigger" enable signal. The high speed device is on and dissipating power only when the thermoreflectance pulse is high. By choosing suitable thermoreflectance pulse width and repetition rate, the device is allowed to reach thermal steady state hot and cold (ambient) conditions corresponding to the normal time windows for calculating thermoreflectance change.

Grauby et al., [40] used a heterodyne thermoreflectance method based on measuring the "blinking" frequency of mixed source illumination signal and high frequency device heating signal. This technique enabled thermoreflectance imaging of device self-

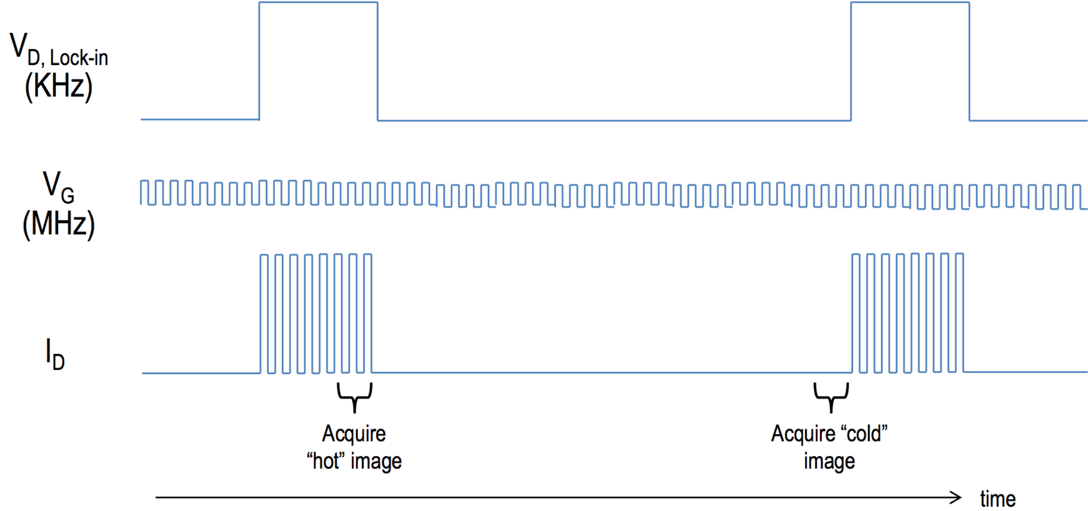

Figure 7.1: Proposed method for thermoreflectance imaging of self-heating in high frequency devices by superposing standard device operating signal (sinusoid MHz-GHz) with pulsed transient thermoreflectance signal at much slower repetition rates (kHz). Thermoreflectance pulse width is selected to enable device to reach effective thermal steady state.

heating at megahertz frequencies well in excess of the camera frame rate. The proposed transient superposition method would provide and alternate technique that would in addition be capable of measuring device transient self-heating distribution under normal high speed operation.

7.2 Optical pumped transient thermoreflectance imaging

Fast optically pumped thermoreflectance imaging promises the ability to quickly inspect two-dimension heat spreading in integrated devices and thin-film materials. Because the method of thermal excitation is optical, the technique can be used to inspect thermal properties of materials and structures when electrical excitation is impossi-

ble or impractical, or when the optical-thermal-response is of interest independent from electrical-thermal response. The method is analogous to time domain thermoreflectance characterization, which uses femtosecond optical pulses to extract fundamental thin material properties, such as thermal conductivity. The experiment optical pumped thermoreflectance imaging microscope currently being developed at Birck Nanotechnology Center will use a 1530 nm pulsed semiconductor laser capable of subnanosecond pulsing and 3 watts average power.

Additional proposed future work areas include thermoreflectance imaging and thermal analysis of surface plasmons in nanowires and plasmonic welding of silver nanowires with submicron spatial resolution. This project may be conducted in unison with implementation of the optically pumped thermoreflectance imaging system. Thermal characterization of gallium nitride high electron mobility transistors can be continued. High resolution imaging can be useful in extended DC stress and at breakdown power thresholds for the GaN HEMT devices.

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