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Demonstration of CMOS-Compatible Multi-Level Graphene Interconnects With Metal Vias

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***Abstract*— Doped-multilayer-graphene (DMLG) interconnects employing the subtractive-etching (SE) process have opened a new pathway for designing interconnects at advanced technology nodes, where conventional metal wires suffer from significant resistance increase, self-heating (SH), electromigration (EM), and various integration challenges. Even though single-level scaled graphene wires have been shown to possess better performance and reliability with respect to dual-damascene (DD) and SE-enabled metal wires, a multi-level graphene interconnect technology (with *vias*) has remained elusive, which is of paramount importance for its integration in future technology nodes. This work, for the first time, addresses that need by engineering a CMOS-compatible solid-phase growth technique to yield large-area multilayer graphene (MLG) on dielectric (SiO_2) and metal (Cu) substrates and subsequently demonstrating multi-level MLG interconnects with metal *vias*. Using rigorous theoretical and experimental analyses, we demonstrate that multi-level MLG interconnects with metal *vias* undergo $<$ 2% change in the *via* resistance under accelerated stress conditions, demonstrating its superior reliability against SH and EM, making them ideal candidates for sub-10 nm nodes.**

***Index Terms*— CMOS-compatible, doped multilayer graphene (DMLG), dual-damascene (DD), electromigration (EM), graphene capping-layer, interconnects, multi-level, reliability, self-heating (SH), solid-phase diffusion, subtractive etching.**

I. Introduction

CONVENTIONAL metal interconnects suffer from significant size effects, as the critical wire dimension scales down to sub-20 nm. The nonlinear increase in resistivity, and subsequent wire and *via* resistance [Fig. 1(a) and (b)] increases self-heating (SH), degrades electromigration (EM) reliability, and thereby limits interconnect current carrying capacity and performance [Fig. 1(c) and (d)] [1]–[5]. Additionally, void formation during metal fill in highly scaled trenches and *via* holes during the dual-damascene (DD) process [Fig. 2(a)] exacerbates the reliability and variability problems [9]–[11].

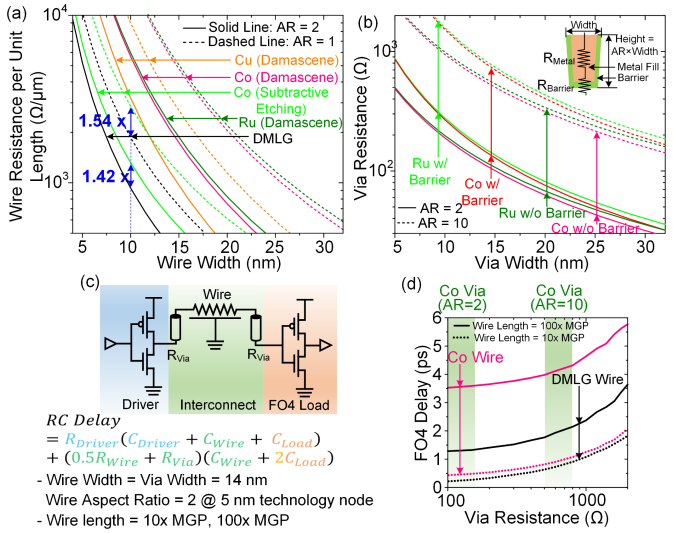

Fig. 1. (a) Resistance per unit length versus wire width for Cu, Co, and Ru wires by single damascene process, and Co and DMLG wires by SE, with AR of 1 and 2. The Cu, Co, and Ru wire resistance by damascene process is estimated from an empirical model [6], Co wire resistance by SE is estimated from the model in [7], and DMLG wire resistance is calculated from an analytical model based on the Landauer approach [8] with consideration of DMLG bandgap opening (for sub-20 nm wire widths) and a doping level of $|E_F| = 0.6$ eV. All the models are calibrated with measured data. (b) *Via* resistance versus *via* width for Ru and Co metals, with and without barrier layers and AR = 2 and 10, estimated from [6]. High AR (=10) contacts are used in dynamic random access memory (DRAM) cells. The side and bottom barrier thicknesses are fixed at 2 and 3 nm, respectively. For *vias* with barrier layers, the *via* resistance is the summation of the resistance of metal fill (R_{Metal}) and barrier ($R_{Barrier}$). (c) Schematic of a driver-interconnect-load circuit in HSPICE simulations, where the driver is a unit-sized inverter and load is 4× (FO4) the size of the driver (at 5 nm technology node). The interconnect is modeled by *via* resistors (R_{Via}) and a distributed *RC* network for wires (using the *RC* delay equation shown). (d) FO4 delay [from (c)] versus *via* resistance for Co wires and DMLG wires of length 100× and 10× minimum gate pitch (MGP). The vertical green regions in (d) indicate the Co *via* resistances corresponding to AR = 2 and AR = 10, respectively. Moreover, in all these calculations, the quantum capacitance and quantum contact resistance corresponding to DMLG wires have already been incorporated in the analytical model developed in [8].

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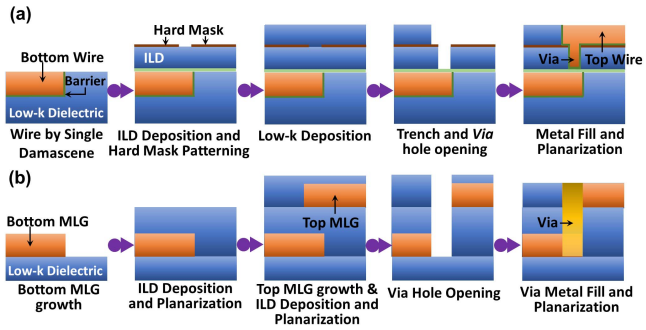


Fig. 2. Schematic of process steps of (a) DD process for conventional metal wires and (b) proposed SE *via* scheme using MLG wires and metal *vias*.

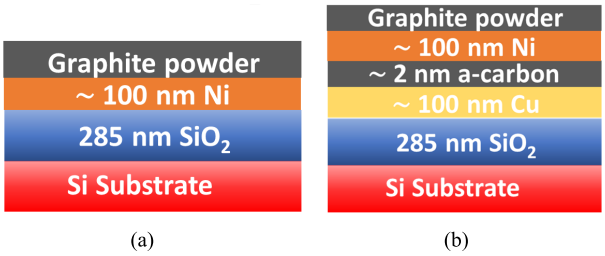


Fig. 3. (a) Schematic of the initial stack used for growing MLG at 350 °C directly onto SiO_2 using the CMOS-compatible solid-phase growth technique [19]. (b) Schematic of the initial stack used for growing MLG directly on Cu substrates, as demonstrated in [25].

Owing to its excellent electrical [12], [13], optical [14], [15], and thermo-electric [16], [17] properties, graphene [or more specifically doped multilayer graphene (DMLG)] was first proposed by Xu *et al.* [18] as a promising solution to various interconnect scaling challenges, and was theoretically shown to beat the resistivity and performance of sub-20 nm Cu by appropriate level of doping (by intercalation) [8]. Thereafter, DMLG interconnects were experimentally demonstrated to overcome the fundamental current-carrying-capacity limit of nanoscale metal interconnects, improving reliability by >100-fold [19], performance by > 4-fold [20], and energy-efficiency by >70% [19]. Furthermore, CMOS-compatible DMLG wires, employing low-temperature solid-phase graphene growth and SE process [20], have been demonstrated to exhibit comparable/higher electrical conductivity with respect to metal interconnects fabricated by DD process [19], negligible EM effect, and long-term doping stability.

It is worth noting that SE of metal wires (e.g., Ru [21]) leads to a marginal improvement (∼30%) in electrical conductivity as compared with those fabricated using the DD process due to larger metal grain sizes resulting from a better and more efficient metal fill process. In addition, it simplifies the back-end-of-line (BEOL) fabrication by eliminating low-*k* dielectric etching, which can potentially increase the dielectric constant because of plasma damage, and thereby affect the circuit performance [21], [22]. Even though reliability/performance of horizontal wires by SE process for both metals [21], [7] and DMLG [19], [20] are well studied, realization and characterization of a multi-tier graphene interconnect system by SE incorporating robust and low resistance *vias*/contacts have remained elusive. *Vias* are crucial elements for signal propagation between various metallization levels, which also suffer from significant EM at advanced technology nodes [23], as also shown in detail in Section II-B. Jiang *et al.* [24] reported carbon nanotube (CNT) *vias* integrated with horizontal multi-tier multilayer graphene (MLG) wires by SE process with extremely high EM resistance in CNT *vias*, MLG wires, and their contacts. However, CNT *vias* require very high growth temperatures (>600 °C), which is not BEOL-compatible. In this work, for the first time, we demonstrate a BEOL-compatible *via*/contact scheme for a two-tier SE-enabled MLG wire system [Fig. 2(b)], and present a comprehensive performance and reliability study, including SH and EM analysis. The major contributions of this work include: 1) demonstration of large-area and uniform CMOS-compatible multi-level MLG growth on arbitrary surface topologies and substrates; 2) demonstration of an SE-enabled multi-level MLG/*via* scheme that is compatible with BEOL process and exhibits < 2% *via*-resistance change under 200 MA/cm^2 current stress; and 3) scalability analysis of the proposed multi-level MLG interconnect scheme to evaluate its benefits at ultimate scaled dimensions. In this article, we present a much more rigorous evaluation of our recent work [25], by providing more evidence and reasoning behind the nature of our results.

This paper is organized as follows: Section II describes the design guidelines necessary for realizing CMOS-compatible multi-level MLG interconnects. Detailed theoretical and experimental evidences are used to arrive at an optimal wire-*via* system for MLG-based BEOL technology. Section III discusses the fabrication process flow necessary for realizing a multi-level MLG wire-metal *via* system. Electrical and reliability characterization results are also shown in Section III. Section IV describes the scalability analysis of the proposed *via* scheme for advanced technology nodes. Finally, conclusions are drawn in Section V.

II. Design Guidelines for CMOS-Compatible Multitier MLG Interconnect

The use of alternative metals such as Co [7], Ru [21] (as compared with conventional Cu) at advanced technology nodes eliminates the need for the metal diffusion barriers resulting in a larger metal wire cross-section. This reduces the severity of the resistivity size effect for these metals at critical dimensions, leading to an improved electrical conductivity and circuit performance as compared with the DD process [Fig. 1(a)]. Moreover, DMLG offers much higher conductivity benefits at smaller aspect ratios (ARs) [Fig. 1(a)] as compared to these barrierless metals due to reduced surface and grain boundary scatterings, in addition to being barrier-free itself. It is instructive to note that even though the elimination of conventional TaN/TiN barrier and capping layer by using a single-layer-graphene (SLG) barrier reduces the effective resistivity of Cu [26], the fundamental reliability problem in nanoscale Cu wires arising from EM and SH remains unsolved [19].

Like other SE metals, for graphene wires to be directly integrated into the CMOS process, it is important to reliably grow large-area, uniform, and good-quality MLG at multiple levels for them to be eventually etched and connected (for multi-level schemes) into practical interconnect

structures. This work first addresses this issue by engineering the solid-phase graphene growth technique [20] to yield wafer size, uniform, and high-quality MLG on dielectric (SiO_2) [Fig. 3(a)] as well as metallic (Cu) substrates [Fig. 3(b)]. In this section, we describe the necessary groundwork needed for realizing the SE-enabled multi-level graphene technology.

A. DD Versus Proposed Subtractive Etching (SE) Based Interconnect Scheme

Our recent work on CMOS-compatible single-level DMLG wires [20] establishes its performance and reliability benefits against the state-of-the-art metal interconnects. Furthermore, for advancing this technology toward practical BEOL process integration, a multi-level interconnect scheme (supported by SE-metal *via*) is proposed in Fig. 2(b). In this scheme, the *via* is fabricated by a single damascene-like metal fill process on the *via* hole through top-MLG, interlayer dielectric (ILD), and bottom-MLG. This might not only reduce the overall processing time (DD versus single damascene-like process), but also result in significant current crowding and EM alleviation, as proved both theoretically (Section II-B) and experimentally (Section III-C), later. The lower resistivity of DMLG wires (as compared to metal wires) [19], [20] coupled with the use of barrierless SE metals (such as Co, Ru, W) for the *vias* promises much better performance (at advanced technology nodes) as compared to the conventional DD process, as also verified in Section IV. An important consequence of using a low-dimensional material like MLG as an interconnect material is the addition of a contact resistance between the MLG and metal. Among the two possible contact geometries to MLG (top contact and edge contact) [27], [28], the former one offers higher contact resistance due to the presence of a van der Waals (vdW) gap. Taking advantage of this fact, the authors uniquely design the proposed *via* scheme in a way that allows edge contacts to MLG, which are obviously preferred over top contacts [28] to achieve lower contact resistance [Fig. 2(b)]. As a matter of fact, this subtractive etching process was first used by the industry for fabricating Al interconnects with W plug, before transitioning to copper-based wires employing the damascene process [29]. The SE process first involves forming a multi-level stack of the wires with some overlap region separated by an ILD. Since the overlap region is used for connecting the two wires, it becomes important to modulate its dimensions to avoid any lithography-induced opens or shorts. The *via* is subsequently formed in a single damascene-like metal fill process by etching through the top wire, the ILD, and the bottom wire. While forming the two-level interconnection, the following issues are the key sources of errors/risks:

1) Wire/Via Misalignment: It is obviously important to make sure that there is minimal misalignment between the wires and *vias* at multiple levels as it can be a significant cause of SH and current crowding, which are the major reliability degradation factors. This effect can be even more pronounced for aggressively scaled (sub-100 nm) wires and high AR *vias* in the proposed SE *via* scheme, where the anisotropic etching and lithography induced opens or shorts can significantly reduce the overall yield of the process.

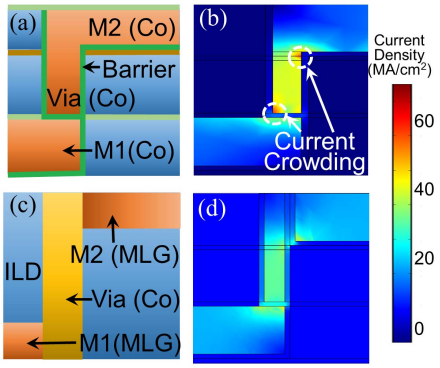


Fig. 4. Layouts and current density profiles for single side M1-*via*-M2 cross section made using: (a) and (b) DD process, and (c) and (d) proposed subtractive etching (SE) (MLG with Co *via*) process. Width of M1/M2/*via* is 12 nm and AR of M1/M2/*via* is 2. A constant current (from ITRS data set) is assumed in these simulations. These finite element electromagnetic simulations have been conducted assuming an empirical conductivity model for MLG (as developed in [8] and validated by experiments in [19]).

2) Lithography Related Challenges: As shown in Section III-A, we have used a photoresist as the mask for performing the vertical etching, which is not the best suited approach as we shrink down the wire dimensions. For sub-100 nm wire/*via* dimensions, a metal mask would serve as a more accurate and robust method due to high alignment accuracy and better tolerance to the etching agents used in this step. These optimizations are crucial to realize high AR *vias* and multi-level interconnections using the proposed *via* scheme.

It is also worth noting that DMLG offers higher electrical conductivity and EM resistance compared with SE Co and Ru [20], especially at smaller ARs [AR = 1, Fig. 1(a)]. Hence, even-though the addition of the edge-contact resistance between MLG and metal *via* increases the overall *via* resistance, the fan-out of four (FO4) delay remains invariant with respect to the total *via* resistance [Fig. 1(c) and (d)]. This is primarily because the FO4 delays show weak dependence on the *via* resistance in the small *via* resistance regime (AR = 2 to 10), where the *via* resistance is much smaller than the transistor (driver) resistance. This highlights the negligible side effects of this technology on the eventual circuit performance.

B. Alleviation of SH and EM in the Proposed Via Scheme

To evaluate the SH and current crowding alleviation of the proposed SE *via* scheme, steady-state solutions were conducted for a M1-*via*-M2 system, as shown in Fig. 4. Our analyses reveal that the MLG-*via*-MLG system suffers from almost no current crowding effects as compared with conventional DD process (using Co). This is mainly due to the current redistribution at the M1/M2-*via* interface due to the edge contact resistance between MLG and metal *via*. Similar behavior is also expected for the proposed *via* scheme (with metal wires and metal *vias*) due to the presence of highly resistive barriers.

To validate the reliability of the proposed *via* scheme against SH and EM, which are major causes of wire and *via* degradation at highly scaled dimensions, a comprehensive finite element method (FEM) model capturing an interplay of the four major complex processes affecting EM and SH is

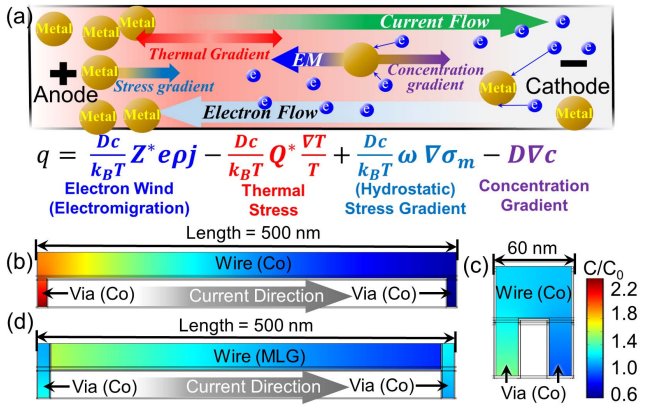


Fig. 5. (a) Illustration of EM and an interplay of various complex processes in a metal wire, where electrons under the presence of high electric stress gain enough momentum to knock out metal atoms out of their lattice sites (EM). Here, q, D, Z^*, ρ, j, Q^*, ω, σ_m, k_B, and T are the total atomic flux, the effective atom diffusivity, effective charge, resistivity, current density, heat of transport, atomic volume, average hydrostatic stress, Boltzmann's constant, and temperature, respectively. (b) DD process with Co wires and Co-*vias*. (c) Normalized metal atomic concentration (C/C_0) in wire and *vias* for (b), and (d) proposed SE MLG + Co-*via* scheme under a constant dc current stress (same current direction for all, as shown in figure). Negligible EM is observed in the *vias* for the proposed scheme (d), as shown by the minor change in atomic concentration. The long wire in (d) shows some EM, primarily due to the inability of the simulator to capture the intrinsic physics of graphene under accelerated stress conditions.

developed [Fig. 5(a)]. This model solves the time-dependent continuity equation mentioned below to obtain the time evolution of the concentration gradient throughout the *via*-wire-*via* system under a constant dc stress, as shown in Fig. 5(b)–(d)

$$\nabla.\vec{q} + \frac{\partial c}{\partial t} = 0.$$

In the above equation, c is the normalized atomic concentration, given by $c = C/C_0$, where C is the actual atomic concentration at time $t(= 10^6$ s in these calculations), C_0 is the initial atomic concentration at $t = 0$, and $\vec{q}$ is the total normalized atomic flux capturing the four major effects mentioned in Fig. 5(a). The constant dc stress used in these simulations is estimated from the International Technology Roadmap for Semiconductors (ITRS) corresponding to the wire/*via* dimensions. As seen in Fig. 5(b), the DD wire-*via* system suffers from significant EM, as evident by the huge change in the concentration gradient throughout the wire and the *vias*. As a sanity check to establish the validity of the simulations, Fig. 5(c) shows the normalized concentration gradient for a DD wire-*via* system with a wire length L less than the blech length (L_B) for Co (~100 nm for the chosen current density). Negligible EM is observed in the wire-*via* system as seen by the minor change in the atomic concentration, validating the well-known experimental claims [30]. Moreover, in the proposed *via* scheme [Fig. 5(d)], even though the *vias* suffer from negligible EM, some minor change in atomic concentration is observed for the MLG wires. This is slightly contradictory to the experimental demonstrations [19], [20], [31] (where MLG wires were shown to exhibit almost zero EM) and mainly arises due to the inability of the electromagnetic simulator to capture the true physics of low-dimensional materials like MLG under these elevated stress conditions. In conclusion, the absence of EM in DMLG wires [19], [20], [31] coupled with the immunity of the metal *vias* fabricated using the proposed scheme to EM [Fig. 5(d)] proves the robust nature of the proposed *via* scheme against major interconnect degradation mechanisms.

C. Large Area/Uniform and High-Quality Multi-Level MLG

The first step toward realizing a multi-level graphene technology is its reliable growth at multiple levels in a CMOS-compatible manner. Thus, a two-tier MLG system with 200 nm SiO_2 as the ILD is fabricated using the initial material stack shown in Fig. 3(a) and by employing the low-temperature (~350 °C) solid-phase MLG growth reported in [20]. Before the growth at each level, the samples are annealed at ~400 °C for 2 h in an H_2/Ar environment. Annealing improves the overall microstructure of the metal catalyst (Ni), by increasing the size of the grains from ~100 nm (before annealing) to ~5 μm (after annealing). Since the diffusion coefficient (and hence, the carbon flux) through the bulk is about 0.5 times than that of through the grain boundaries [20], a larger grain size essentially translates to a more uniform MLG growth. However, this reduces the thickness of the MLG (for the same growth time as reported earlier [20]). To compensate for that, we have doubled the overall growth time (~60 min) and slightly increased the growth temperature (~350 °C) while keeping the same pressure (~65 psi) to result in similar thickness as compared with our previous work [20]. Fig. 6(a) shows the optical image after the fabrication of the bottom MLG on a 285 nm SiO_2/Si substrate. A large-area Raman map in Fig. 6(b) and the sharp G and 2D peaks in the single point Raman spectrum in Fig. 6(c) confirm the uniform high-quality growth. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image in Fig. 6(d) clearly shows the layered structure of graphene, once again confirming the high growth quality. Atomic force microscopy [Fig. 6(e)] confirms a thickness of ~20 nm for the bottom MLG. The main incentive for optimizing the growth for a thickness of ~15–20 nm is because it has been shown (via simulations) to minimize the FO4 delay for DMLG wires for sub-20 nm wire widths (AR ~ 1) [19]. The top MLG [optical image, Fig. 6(f)] is fabricated over the ILD under the same conditions and exhibits almost comparable quality and thickness with respect to the bottom MLG, as evidenced from the single point Raman spectra [Fig. 6(g)] and the uniform large area Raman map [Fig. 6(h)]. Fig. 6(i) shows the HAADF-STEM image of the top MLG, once again validating the layered structure of graphene. The unevenness in the TEM image of the top MLG [Fig. 6(i), yellow box] is mainly due to the uneven SiO_2 ILD surface grown by plasma-enhanced chemical vapor deposition (PECVD) process. This unevenness can be attributed to the relatively low substrate temperature (~300 °C) for the PECVD process [32], which can be eliminated by using chemical mechanical polishing (CMP) to planarize the ILD. The successful growth of high-quality MLG on both levels also confirms the applicability of the growth technique on arbitrary surface morphologies.

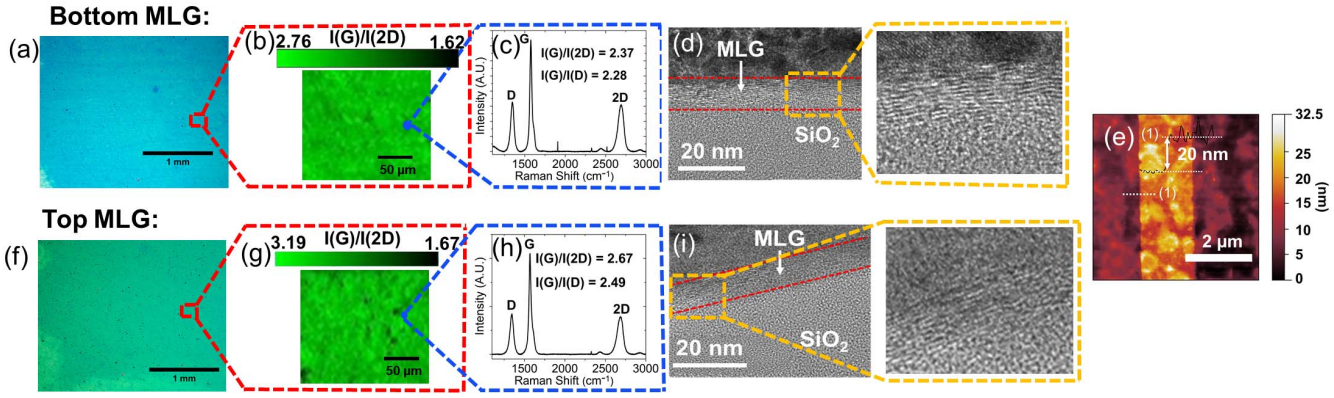
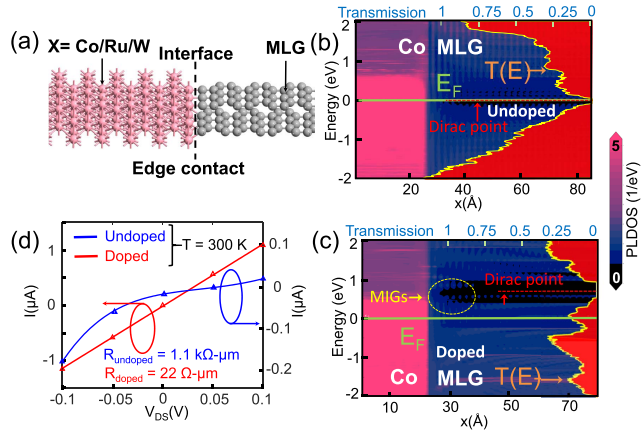


Fig. 6. (a) Optical image of a large-area MLG (bottom level) grown using the solid-phase growth technique. (b) Raman map [corresponding to the highlighted region in (a)] of the *I*(G)/*I*(2D) ratio of the bottom MLG. (c) Shows the single point Raman spectra in (b). A large area *I*(G)/*I*(2D) ratio of ~2.4 indicates the uniform large area coverage of MLG using the optimized growth process. (d) HAADF-STEM of the bottom MLG in (a). The red lines indicate the approximate region of the MLG. The zoomed-in region in the yellow dashed rectangle clearly shows the layered structure of the MLG. (e) AFM profile of the bottom MLG etched into ~1-μm wide wires, indicating 20 nm thickness. Similar thickness is observed for the top MLG as well. (f) Large-area optical image of the top MLG. (g) Raman map of *I*(G)/*I*(2D) ratio and (h) single point Raman spectrum of the top-level MLG in (f) indicates its large-area uniformity. The HAADF-STEM image in (i) shows a zoomed-in view of the top MLG on an uneven SiO_2 surface; the zoomed-in region shows the layered structure of the top-level MLG.

X-ray photoelectron spectroscopy (XPS) analyses of the grown MLG reveal that the exact peak position (1202.3 eV) and atomic composition (~83%) corresponding to the $C = C$ sp2 bond can also be observed in the conventional CVD grown MLG [25], once again validating the high-quality growth of the solid-phase MLG.

D. Identification of Optimal Via Metal

The next step after forming a two-level MLG stack is to identify the optimal *via* metal to be used for forming a two-level interconnection. The total resistance of the *via* consists of two components, the resistance of the *via* metal due to its physical dimensions and the contact resistance between the graphene-*via* metal interface. Since the contact resistance forms a major component of the overall *via* resistance at advanced technology nodes, it becomes critical to identify the MLG edge-metal combination that offers the lowest contact resistance to minimize the overall *via* resistance and, hence, the eventual circuit performance. To this end, we employ an *ab initio* density functional theory (DFT) coupled with Non-equilibrium Green's Function (NEGF) transport framework to assess the electrical properties of MLG-metal edge following the methodology described in [33]. Fig. 7(a) shows the interface geometry of the simulated supercell. DFT calculations were performed utilizing generalized gradient approximation (GGA) functional [34] and Pseudo Dojo Pseudopotentials using $7 \times 5 \times 200$, 150 Rydberg, 0.05 eV/Å of *k*-point sampling, energy mesh cutoff, and maximum force for geometry optimization, respectively. To include the out-of-plane interactions, DFT-D2 corrections [35] have been incorporated. Top three SE based barrierless *via* metals (Co, Ru, W) [6], [36] form the prospective choice for the *via* metal as they minimize the resistance at sub-10 nm nodes. Contact resistance of any interface essentially translates to determining the available states with matching energy and *k*-vectors on both sides of the interface,



(e)

$R_{edge\text{-}contact}$ (kΩ-μm)	Co	Ru	W
Undoped MLG	1.1	2.357	4.137
Doped MLG	0.022	0.013	0.026

(f)

Activation/ Cohesive energies (eV)	Co	Ru	W
	2.4-3.1	1.9	0.69

Fig. 7. (a) Atomic supercell of metal X (X = Co, Ru, W) and MLG interface. (b) Band-alignment (projected local DOS) and transmission spectrum, T(E), of undoped MLG. In undoped MLG (X = Co), Fermi-level lies at the Dirac point and transmission will be intrinsically limited by the low DOS around Dirac point. This will lead to nonlinearity in the *I*–*V* response, and result in an aggravated contact resistance. (c) Band-alignment (projected local DOS) and transmission spectrum of DMLG and Co metal. A practical doping level of −0.6 eV has been assumed in these calculations. Graphene's Fermi-level will move down and away from Dirac point to energies with higher DOS as doping increase; this will result in increase of transmission coefficient for graphene and a perfect linear *I*–*V* response and thus low contact resistance. (d) *I*–*V* response of doped graphene and undoped MLG (X = Co). (e) Table summarizing the edge-contact resistances between various SE metal candidates with doped and undoped MLG. (f) Table showing the experimentally obtained EM activation energies of the *via* metals [6], [36].

followed by their transmission (coupling) probability to each other. In this study, we consider the case of both undoped MLG and $FeCl_3$ doped MLG. For the case of undoped MLG, the Fermi-level lies on the Dirac point where the density of states (DOS) surrounding Fermi-level is negligible [Fig. 7(b)].

This low DOS around Fermi-level suppresses the available transmission modes, increasing the edge contact resistance between the MLG-metal interface [Fig. 7(d) and (e)]. For DMLG (p-type doping of 6.85×10^{13} cm^{-2}), Fermi-level moves down and settles in a high DOS region of the Dirac cone [Fig. 7(c)]. Consequently, upon formation of the metal contact, higher DOS are available for conduction around Fermi-level which significantly reduces the edge-contact resistance, as evident in the increase of the transmission spectrum around the Fermi-level [Fig. 7(d) and (e)]. It is interesting to note that DMLG possess almost identical edge-contact resistance to the prospective metal candidates (Co, Ru, W), as shown in Fig. 7(e). The small variations in the contact resistance can be attributed to the variations in the DOS of the 3-D metal at the Fermi-level energy. While Ru performs best among the simulated metals, however, the higher activation energy and lower resistivity of Co as compared with Ru and W [6], [36] implies its higher tolerance to EM and SH [Fig. 7(f)], making it the better choice as the *via* metal for a multi-level MLG wire system.

E. Extension of CMOS-Compatible Graphene Growth Onto Metallic Substrates

The simplicity of the solid-phase CMOS-compatible graphene growth technique helps in easily extending it onto arbitrary substrates if the growth temperature does not result in thermal degradation of the substrate. Depending upon the relative diffusion coefficients of the substrate material and the metal catalyst (Ni) upon thermal annealing, a sacrificial separation layer might need to be inserted between them. In the previous demonstrations of the growth of MLG on SiO_2 substrates, no sacrificial layer is required as carbon has very little solubility in SiO_2 [20]. Due to the potential use of MLG as a capping layer for conventional Cu interconnects [37], we demonstrate high-quality MLG growth directly on Cu without the need for any transfer process [25]. As both Ni and Cu have finite solubilities at ~350 °C, a ~2 nm amorphous carbon layer [25] is inserted between them [Fig. 3(b)]. The amorphous carbon prevents Cu and Ni layers from interdiffusion and aids the graphene growth process by acting as an additional source of readily available carbon at the Cu interface. Excellent optical and material characterizations of the MLG grown on Cu [25] demonstrate the outstanding reliability of the growth technique on metallic substrates.

III. Fabrication and Characterization of Multi-Level MLG-Interconnect

In this section, we demonstrate a two-level SE-MLG interconnect structure using Co *via* where the *via* hole is etched through the wires and ILD using a single damascene-like process. This is followed by its electrical characterization from where the edge contact resistance is extracted and compared with the numbers obtained theoretically. High current stress tests are performed to establish the reliability of the multi-level MLG wire-*via* system. Similar growth parameters as mentioned in the previous section result in 20 nm thick MLG for both levels. Although unintentional, the use of $FeCl_3$ solution for removing Ni catalyst ends up surface-doping the system, as evidenced from the presence of Fe at both the top and bottom MLG surfaces [25], which can lower the MLG resistivity. Significant performance improvement can be obtained by using intercalated DMLG wires [19], [20], as analyzed later.

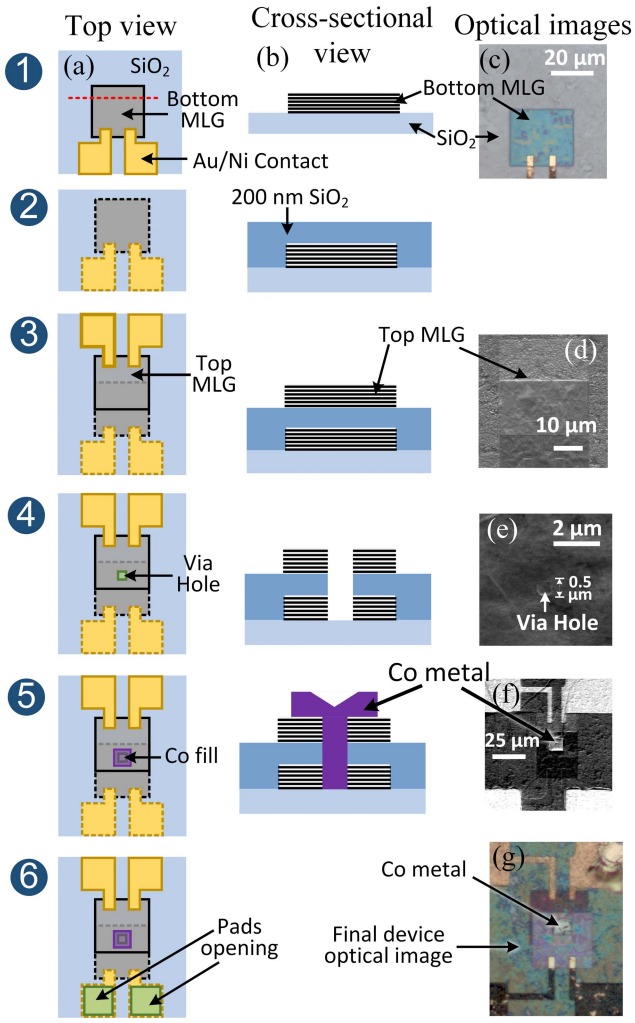


Fig. 8. Process steps showing (a) top view and (b) cross section view [along the red line in (a)]. Steps 1–6 are (1) bottom MLG synthesis by solid phase growth, patterning and contact pads fabrication, (2) SiO_2 ILD deposition by PECVD, (3) top MLG synthesis by solid phase growth, patterning and contact pads fabrication, (4) *via* hole opening by oxygen and CHF_3 ICP etching, (5) 220 nm thick Co deposition by thermal evaporation (rate $<$ 5 Å/s), and (6) bottom pads opening by etching the SiO_2 ILD. (c) and (g) Optical images, and (d)–(f) SEM images are presented to confirm the key process steps.

A. Fabrication Process Flow

The major fabrication steps are summarized in the process flow described in Fig. 8. First, starting from a standard 285 nm SiO_2/Si substrate, 20 nm bottom-MLG is grown and characterized, as shown in Fig. 6(a)–(e). This is followed by patterning the bottom MLG onto 25 μm squares using a 50 nm Ni metal hard mask, followed by oxygen inductively coupled plasma (ICP) etching. The hard mask is removed by $FeCl_3$ wet etching. 15 nm Ni/150 nm Au contacts and pads are patterned

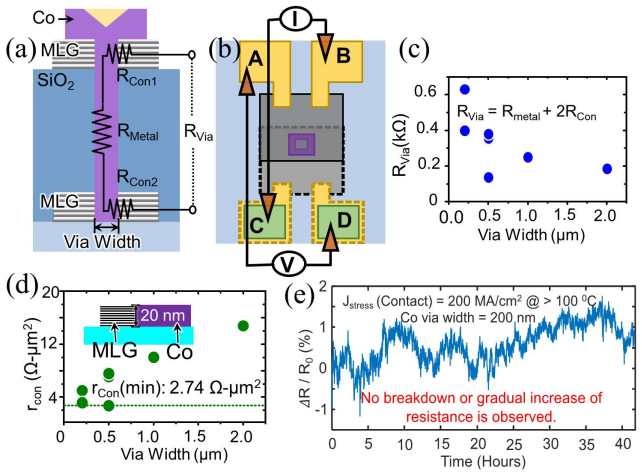


Fig. 9. (a) Cross-sectional view of a Co *via* connecting two tiers of MLG in Fig. 8, and the corresponding resistance network. The Co *via* resistance consists of edge contact resistance to top MLG (R_{Con1}), Co metal resistance (R_{Metal}) and edge contact resistance to bottom MLG (R_{Con2}). R_{Con1} (or R_{Con2}) can be estimated by subtracting R_{Metal} from the measured R_{via}, as shown in (c). (b) Schematic showing four-probe measurement scheme of the *via* resistance (R_{Via}). (c) Measured total *via* resistance (R_{Via}) versus *via* width. (d) Extracted specific contact resistivity (r_{Con}) (Ω-μm^2) versus *via* width, normalized with respect to the *via* width and thickness. (e) Measured *via* resistance change during current stress test, where 200 MA/cm^2 stress current is applied on edge contacts for >40 h. No breakdown or gradual resistance increase is observed, indicating no EM in Co *via* and Co-MLG contacts.

to electrically probe the bottom MLG. This is followed by depositing 200 nm thick SiO_2 ILD using PECVD process. Similar to the bottom MLG, the top MLG is grown and patterned using a Ni metal mask and oxygen ICP etching, while maintaining an overlapping region with the bottom MLG (step 3 in Fig. 8). This is followed by patterning of contacts and pads for the top MLG. In the overlapping region, a square *via* hole (widths ranging from 2 μm to 200 nm) is opened by a three step oxygen-, CHF_3-, and oxygen-ICP process to etch the top-MLG, ILD, and bottom-MLG, respectively, using a bilayer photoresist mask [Fig. 8(e)]. To ensure the *via* fill is successful at sub-1 μm wire widths while simultaneously avoiding any alignment challenges, a 5 μm $\times$ 5 μm window was patterned enclosing the *via* hole (Step 5, Fig. 8). A $\sim$240 nm thick Co is subsequently deposited by thermal evaporation (<100 °C) to fill the *via* hole [Fig. 8(f)] at slow deposition rate to ensure full metal fill. Finally, ILD on top of bottom pads is etched to access the bottom MLG pads. An important consequence of filling the *via* metal in a 5 μm window around the *via* hole is the formation of both edge and top contacts to the top MLG, as shown in Fig. 9(a). This, however, does not deviate significantly from the ideal situation of pure edge contacts to both top and bottom MLG, as explained in the next section.

In these experiments, the wire/*via* width dimensions used are only for demonstration purposes and no way represent the state-of-the-art process technology. The primary bottlenecks in accessing smaller *via*/wire widths are: 1) ensuring complete vertical etch and metal fill at sub-100 nm dimensions and 2) minimizing the misalignment of the top and bottom MLG layers at sub-100 nm wire widths.

B. Electrical Measurement and Contact Resistance Extraction

Since the growth conditions and optical characterizations (Raman maps, STEM) for both the bottom and top MLG are almost identical, it can be safely assumed that they would possess similar I–V characteristics. With that said, the only unique measurable electrical component of this electrical system is the *via* resistance (and, hence, the edge contact resistance between MLG and Co). It is important to note that before taking any electrical measurements, the contact/pads were current annealed, which has shown to significantly enhance the current injection efficiency of the contact pads [24]. The *via* resistance (R_{Via}) can be measured by applying current between top pad B and bottom pad C and measuring the voltage between top pad A and bottom pad D [Fig. 9(b)], like the van der Pauw method. The measured *via* resistance [Fig. 9(c)] consists of only the Co metal resistance (R_{Metal}) and top and bottom Co-MLG contact resistances (R_{Con1} and R_{Con2}). The top and bottom MLG wire resistances can be neglected because of symmetry in the measurement. Assuming a bulk resistivity for Co (the *via* dimensions are large enough for the resistivity to be close to its bulk value), the *via* metal resistance can then be easily estimated using $R_M = \rho L/A$, where ρ is the resistivity of the *via* metal (corresponding to a dimension of 0.2–2 μm, which are the *via* widths fabricated in this experiment). An AR of 1 (corresponding to a square *via* hole) has been used in this analysis. A length L corresponding to $\sim$200 nm (ILD thickness) has been used in these calculations to estimate the metal resistance. This metal resistance is then subtracted from the measured *via* resistance (R_{via}) to estimate the Co-MLG edge contact resistances ($R_{con1} + R_{con2}$). In addition, the "top-contact" resistance is much larger than the "edge-contact" resistance in metal-MLG contacts [25]. Thus, it can be assumed that the top and bottom contact resistances are dominated by the edge contacts (as both top/edge contacts act in parallel). Moreover, both the top and bottom edge contact resistances are almost identical ($R_{Con1} \sim R_{Con2}$) since both top and bottom MLGs are of identical thicknesses ($\sim$20 nm). Thus, the extracted normalized Co-MLG specific contact resistivity (contact resistance normalized by the perimeter (or *via* width) and thickness of the top and bottom edge contact regions) is plotted in Fig. 9(d). The minimum specific contact resistivity is estimated to be 2.74 Ω-μm^2(137 Ω-μm) for the $\sim$0.5 μm wide and 20 nm thick Co-MLG edge contacts. This plot is in exact correspondence to our recent results [25], where the extracted contact resistances were normalized only with the perimeter of the top and bottom contact regions. Moreover, this value also corroborates with the partial surface doping claim of MLG caused by $FeCl_3$, as it lies between the theoretically estimated (by DFT) edge-contact resistance values of doped- and undoped-MLG with Co [Fig. 7(e), column 2] [25]. In addition, it is worthwhile to note that the extracted contact resistance reduces with a reduction in the *via* width. This can be attributed to the enhanced current annealing in narrow *vias* due to a higher local current density [24], [38].

C. EM Reliability Measurement

In order to demonstrate the EM resistance of the proposed Co *via* scheme with two-tier MLG, a constant current stress (current density $J = 200$ MA/cm^2 at > 100 °C at Co-MLG contact) is applied to the device [Fig. 8(g)] (corresponding to a *via* width of 200 nm) from top pad B to bottom pad C [Fig. 9(b)]. The *via* resistance increase is observed to be $<2\%$ over >40 h stress time, indicating negligible EM in the Co *via* and/or at the Co-MLG contacts [Fig. 9(e)]. This also validates our theoretical claims established in Fig. 5(c), regarding the robust reliability claim of the proposed *via* scheme.

IV. Ultimate Scalability of the Proposed *Via* Scheme

The MLG-metal contact resistance forms an integral part of the total *via* resistance in the proposed *via* scheme. Since the scalability aspects of conventional barrierless *via* metals such as Co, Ru, and W have been well studied [6], [7], [21], [36], it becomes customary to look at the scaling trend of the MLG-metal contact resistance to evaluate its prospects for advanced technology nodes. As shown in Section II-D, DFT simulations have been used to estimate the theoretical lower limit of the MLG-metal (edge) contact resistance. We expect these contact resistance values to be nearly the same unless the thickness of the MLG becomes less than its vertical transfer length (<20 nm for both undoped and DMLG). However, in case of DMLG, in addition to reduction of the specific interface resistivity, the cross-plane effective mass of MLG is also predicted to decrease [39], which will lower the vertical transfer length. Further studies are required to experimentally probe the increase of the contact resistance versus the reduced thickness of the MLG to quantify the vertical transfer limit. Since our experiments have a thickness of $\sim$20 nm, we can safely neglect the variation of the edge contact resistance values with the thickness of the undoped/doped MLG.

The DFT simulations in Fig. 7 assume a doping level of -0.6 eV [19], which has been experimentally validated for $\sim$20 nm wire width MLG. To evaluate the benefits of the proposed *via* scheme at sub-10 nm wire widths, these edge contact resistances were manually added to the overall *via* resistance while estimating the FO4 delay. Our simulations show $\sim$ 2-fold improvement in the MLG-wire resistance at $\sim$5 nm wire width. It also indicates that although the edge contact resistance leads to a $\sim$ 2-fold increase in the *via* resistance in the DMLG/Co-*via* scheme [25], the smaller resistance and parasitics of DMLG wires [19] result in an overall improvement of $\sim$ 2-fold in the FO4 delay with respect to that of conventional Co-interconnects by DD process [25]. It is important to note that, in all these performance projections, a constant thickness of around 20 nm has been assumed. Due to the $\sim 50\times$ higher current carrying capacity of MLG interconnects as compared to that of the conventional metals, their thickness can be significantly reduced without compromising the current density requirements. This reduction in MLG thickness would significantly reduce the wire capacitance, which is the key factor determining the performance of aggressively scaled shorter wires whose resistances are significantly smaller than the driver resistances.

V. Conclusion

In this work, the pressure-assisted solid-phase low-temperature/transfer-free graphene growth technique has been engineered to achieve large-area and high-quality MLG films on both standard SiO_2 and Cu substrates. Moreover, a new SE-enabled *via* scheme has been proposed and demonstrated for fabricating multi-level MLG wires. The low-temperature MLG growth technique has been designed to facilitate integration of graphene into the CMOS technology—either as replacement for Cu interconnects or as capping layer for certain Cu wires. The low-temperature growth process is also well-suited for monolithic-3-D integration with 2-D materials involving graphene [16]. In our current experiment, the MLG/Co-*via* interconnect structure offers supreme reliability against SH and EM as compared with conventional DD interconnect technologies. Rigorous scaling analyses indicate that the increase in the total *via* resistance in case of the DMLG/Co-*via* multi-level structure is more than compensated by the reduced wire resistance, resulting in $\sim$ 2-fold improvement in the overall circuit performance as compared with that of the DD process. Owing to the higher current-carrying capacity of graphene with respect to conventional metals, the performance can be further improved by using thinner MLG wires provided the driver resistance is higher than the wire resistance. The higher current-carrying capacity of DMLG wires in conjunction with their lower resistivity also make them an ideal candidate for on-chip inductor applications [40].

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