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Coherent Receivers for O-band, Short Reach Optical Links

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Stephen Misak

Committee in charge:

Professor Clint Schow, Co-chair
Professor Larry Coldren, Co-chair
Professor James Buckwalter
Professor Adel Saleh

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The Dissertation of Stephen Misak is approved.

Professor James Buckwalter

Professor Adel Saleh

Professor Larry Coldren, Committee Co-chair

Professor Clint Schow, Committee Co-chair

December 2024

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Short Reach Optical Links

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Stephen Misak

Dedicated to my Mom and Dad
for their love, patience, and support

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Curriculum Vitæ

Stephen Misak

Education

2024	Ph.D. in Electrical and Computer Engineering, University of California, Santa Barbara.
2019	M.S. in Electrical and Computer Engineering, University of California, Santa Barbara.
2017	B.S. in Engineering Physics, Optical Engineering Minor, Semiconductor Materials and Devices Certificate, Rose-Hulman Institute of Technology

Publications

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Abstract

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Stephen Misak

High bandwidth optical links are required to support the continual increases in the demand for high-resolution video, high-performance computing, machine learning, cloud computing, the Internet of Things (IoT), 5G networks, and other applications. In particular, the bandwidth requirements for short reach inter- and intra-data center optical links are reaching the capability limits of the industry standard intensity modulation, direct detection (IMDD) links. Coherent modulation, while more complex for a single optical link, can operate at higher data rates and spectral efficiency by encoding multiple bits per symbol. The high sensitivity of coherent links also enables data centers to replace electrical switches with optical switches, reducing overall power consumption and hardware cost. O-band coherent receivers (RX) on indium phosphide (InP) and silicon photonics (SiP) platforms will be discussed in this dissertation. These receivers were designed for compatibility with an analog coherent link architecture using an optical phase-locked loop, but they can also be used in a traditional coherent link. Tradeoffs in design, performance, and manufacturability between material platforms will be discussed. The design, fabrication, and measurements from two generations of InP O-band coherent RX PICs will be described. Two generations of O-band coherent RX PICs fabricated using Intel's SiP process (with and without integrated lasers) and a dual-mode coherent RX using Global Foundries 45SPCLO will also be shown. A sampled-grating distributed Bragg reflector (SG-DBR) laser designed for O-band coherent RXs using

Intel's SiP process will be presented. To demonstrate the RX PICs, they are packaged with high-speed electronic integrate circuits (EICs) and measured with multiple coherent modulation formats using digital signal processing (DSP) or analog electronics for data recovery. Architectures using reduced DSP or analog electronics both show promise for energy efficient, short reach coherent links.

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Chapter 1

Introduction

1.1 Brief History of Optical Communications

While light has been used for millennia to transmit signals via fire, smoke, or mirrors, the development of modern optical links began soon after Charles Townes and Arthur Schawlow published the proof of concept paper for the laser, and Theodore Maiman built the first working laser in 1960 [1]. The laser initiated the development of free-space optical links, but commercialization of long distance optical communication through glass fibers was not feasible due to excessive optical loss. Several groups separately raced to reduce the optical loss. The first long distance links in the late 1970s used Corning glass fiber with losses of 3 dB/km and Bell Laboratories GaAs semiconductor lasers at 850 nm to transmit data with repeaters every 10 km [2]. The modern 0.2 dB/km at 1.55 μm was attained in 1979 by a Japanese group through refinement of the fiber preform growth process to reduce imperfections [3]. Another major improvement to the growth process reduced the impact of the SiOH impurities, which lead to the so-called OH or "water peak," bringing the loss down from multiple dB/km to around 0.3 dB/km [2, 4]. There have been some groups who have made slight reductions to fiber loss, but 0.3 to

0.2 dB/km from 1310 to 1550 nm remain the standard values to this day.

Introduction of opto-electronic integrated circuits (OEIC) for communications began with advances in photolithography techonology and the analysis of dielectric waveguides [5]. GaAs lasers at 850 nm with silicon detectors were employed in the first generation of optical communication systems, but systems transitioned to InP at wavelengths centered around 1310 and 1550 nm for lower dispersion and reduced fiber loss in the 1980s. The first coherent receivers on InP with an integrated laser, a 2×2 coupler, and photodiodes were made at NTT and Bell labs in 1989, publishing their work within the same month [6, 7]. Photonic integrated circuits (PIC) became a common term in the 1990s [8] with continued work on InP. Communication systems were struggling to improve the span between signal regeneration in the 1980s. Coherent communication offered benefits in spectral efficiency (SE) and sensitivity to improve the reach, but the invention of the erbium doped fiber amplifier (EDFA) provided a simpler method of increasing reach. Research on coherent communications was largely put on hold from 1990 to 2004 with advances in EDFA technology, fiber dispersion compensation, wavelength division multiplexing (WDM), forward error correction (FEC), and differential quadrature phase shift keying (DQPSK). The broad gain spectrum of the EDFA supported many WDM channels. From 1996 to 2007, research results on overall fiber capacity grew from 1 Tb/s to 25 Tb/s, with 11 Tb/s and 25 Tb/s hero demonstrations including 273 and 160 WDM channels. Commercial systems followed this trend with lag time of several years, introducing 1 Tb/s systems in the early 2000s, right around time that the telecommunications bubble burst [4, 9].

Research into coherent coherent communication systems expanded a few years after the telecommunications bubble as WDM systems filled the EDFA gain spectrum. Coherent systems offered higher SE, better receiver sensitivity, and access to the optical field in digital form for signal processing. CMOS digital-to-analog converters (DACs) for

transmitters and analog-to-digital converters (ADCs) for receivers had improved enough to enable signal processing for correction of chromatic dispersion, polarization-mode dispersion, and other fiber nonlinear effects at 10 Gbaud [9]. Nortel and Alcatel-Lucent brought coherent transceivers to market at 10 and 28 Gbaud in 2008 and 2009. Over the next few years, coherent gained dominance in long-haul networks, and metro networks started using 100 Gb/s coherent systems following the 100 Gb/s Ethernet standard.

Today, coherent has entered the data center interconnect (DCI) market with the 400G modules following the OIF 400ZR standard for point to point links up to 120 km. The deployment of 400G modules has grown since the standards were published in 2020. In October 2024, OIF finalized the 800ZR standard, and Acacia/Cisco already demonstrated 800G modules at OFC2024. As bandwidth continues to scale, especially in data center applications, it is likely that the benefits of coherent will lead to transceivers with a target reach below 2 km for data center campus and intra-data center interconnects, possibly in the 1.6 or 3.2 Tb/s transceiver generations [10]. The next section will discuss some of the driving forces for short reach coherent links and potential packaging form factors.

1.2 Data Center Scaling and INTREPID

As the demands for internet traffic and machine learning continue to drive data center scaling [11, 12, 13], there has been a substantial amount of research and development led by both industry and academia to devise feasible solutions to the future bandwidth and power consumption requirements. Improvements to the intra-data center network will have a significant impact on efficiency and power consumption with >70% of the zetabytes (10^{21}) of data center traffic sent between servers in the same location. In future data centers acting as artificial intelligence (AI) clusters, the server rack bandwidth and power consumption requirements are expected to be 10 times larger than traditional data center

at >100 Tbps and >100 kW [13]. Pluggable 10/25/100G intensity-modulation direct-detection (IMDD) transceiver connections to Ethernet switch ports comprise a large part of the current data center transceiver market, but 400G and 800G solutions are expected to grow over the next few years [13]. Optical links for 400G and 800G transceivers are using 53/56 Gbaud PAM4 modulation with channels on parallel fibers for data center reach (DR) up to 500m. Wavelength division multiplexed channels for fiber reach (FR) up to 2 km and long reach (LR) up to 10 km are also common for hyper-scale data centers. Transceivers using 106 Gbaud PAM4 for 1.6T interconnects been developed by Accelink (with Cisco), Coherent, Innolight, and Eoptolink for DR applications. The switches connecting the data center racks have been operating with 12.8 and 25.6 Tb bandwidth, but 51.2 Tb switches have recently entered the market with NVIDIA, Marvell, Broadcom, and Cisco offering competing chips for leaf/spine switches [14]. Future scaling to 102.4 Tb switches is currently in development.

While 1.6T transceivers have been shown up to 2 km, coherent transceivers are capable of longer reaches or increased link budget while also providing more spectral efficiency. In recent years, coherent communication for short reach, O-band data center links has gained support as a solution to address data center scaling [15, 16, 17]. To demonstrate the capabilities of coherent for improving link budget and reducing power consumption, the INTelligent Reduction of Energy through Photonic Integration for Datacenters (INTREPID) [18] project was started in 2017 as part of the ENergy-efficient Light-wave Integrated Technology Enabling Networks that Enhance Datacenters (ENLITENED) [19, 20] program funded by the Advanced Research Projects Agency - Energy (ARPA-E). The ENLITENED program was created in response to the rising power consumption of data centers in the USA. Estimated at 2.5% of total power in 2017, demand for data center services continues to rise with the fraction currently at >4% and expected to reach 6% by 2026 [21].

The INTREPID project planned to demonstrate transceiver components and new link architectures for improving the bandwidth, cost, latency, and power consumption of data centers. Increasing the energy efficiency of individual links is one method for energy reduction. This can be achieved by low power vertical-cavity surface emitting laser (VCSEL) optical links at moderate bandwidth and short reach links within a server rack or within a row of racks. Coherent optical links with high bandwidth and moderate power can also reduce power consumption and offer >2 km length. Coherent optical links with reduced power were the main focus with some work on VCSEL links [22] during early stages of the INTREPID project. Coherent links at O-band (1260 - 1360 nm) minimize chromatic dispersion, and analog electronics used in place of application specific integrated circuits (ASICs) for digital signal processing (DSP) enable significant power savings. A proof of concept demonstration for low power coherent links with integrated InP photonics using an optical phase-locked loop (OPLL) was made by Mingzhi Lu, Eli Bloch, Hyun-chul Park, and other collaborators in 2012, led by Larry Coldren and Mark Rodwell [23, 24, 25, 26]. Their work builds on a long series of improvements to OPLLs since the first free-space demonstration in 1965 and the first integrated InP photonic demonstration in 2009 [27, 28]. Expanding on their work and the analysis done by Joe Kahn, Anujit Shastri and Jose Perin in [15], a major target of INTREPID was to construct O-band coherent PICs capable of 200 Gbps/λ that can be paired with analog OPLL circuitry to replace the carrier recovery functions of DSP for power savings [29].

1.2.1 Integrated Circuit Efficiency Optimization

A significant fraction of the power (>50%) for IMDD and coherent links come from the DSP, ADC, and DAC circuits [30, 31], so improving these circuits is a clear path to increasing energy efficiency. Replacing DSP circuits with analog electronics for an OPLL

forms the basis of the "analog coherent" link design proposed as part of the INTREPID project, but additional power can be saved by using QPSK modulation with limiting electronics which can achieve efficiency of <1 pJ/bit [32] compared to ADCs which can consume between 4 and 12 pJ/bit [30]. The efficiency of ADCs has also been improving with smaller process nodes edging closer to 1 pJ/bit [33]. Prototype circuits for analog phase recovery have been made on 130 nm BiCMOS SiGe [34] and 130 nm SiGe HBT [35] node with 400 mW (10 pJ/bit at 40 Gb/s) and 200 mW (2 pJ/bit at 100 Gb/s) power consumption, and further improvements are possible with smaller process nodes. A direct comparison to DSP chips optimized for short reach coherent is not possible at this time, but analysis indicates that power consumption for short reach coherent DSP is close to 1.6 times PAM4 DSP [36]. Using advanced process nodes, PAM4 DSP chips consume approximately 5 pJ/bit [37], so the equivalent coherent DSP would be close to 8 pJ/bit. This indicates that analog electronics replacements for DSP using advanced process nodes can potentially save several pJ/bit.

1.2.2 Packaging Considerations

In addition to the power savings from the design of a single optical link, the packaging interface between the optical links and the server is another area for improvement. Pluggable transceivers suffer from channel loss of the high speed electrical signal travelling through the PCB channel from the pluggable to the server ASIC. Due to packaging constraints on electrical interconnect density using ball grid arrays (BGA) or land grid arrays (LGA) with ∼1 mm pitch, the bandwidth density of the interconnects between the PIC and the electronic integrated circuits (EICs) is also limited. Co-packaged optics (CPO) is also part of the INTREPID project's vision for future data centers to overcome these limitations [38]. Using flip chip bonding of the PIC and EIC onto a silicon inter-

poser (2.5D integration), enables the use of finer C4 pitch ($\sim 130\mu m$) which increases the connection density by a factor of ∼60. The short connection length between PIC and EIC through the interposer also reduces the electrical losses which can lead to a 10× improvement in the energy efficiency [38]. The advantages of CPO have lead several companies to develop the technology [39].

Ranovus has been developing their optical engine with PICs from GlobalFoundries (GF) Fotonix process. They have been partnering with multiple companies to develop 3 generations of CPO products using 100Gbps PAM4 [40, 41]. Intel demonstrated a 12.8T switch with LGA and soldered connections [42]. Broadcom have 25.6T CPO switches in production with deployments in Tencent's network, and have shown 51.2T CPO switches with 50% power savings and lower cost compared to pluggable solutions [43, 44, 45]. Marvell showed 2.5D heterogeneous integration of drivers and TIAs that are flip chip bonded to a silicon photonics (SiP) chip that is connected to an multi-layer organic substrate through C4 bumps. This 2.5D light engine was integrated into an LGA package as part of optical module which was tested in a full system demonstration with Marvell's Teralynx 7 switch [46]. Cisco has developed 3.2 Tbps light engines based on SiP FR4 optical modules [47], and demonstrated them at OFC 2023 inside of a 25.6T switch [48]. IBM worked with Finisar (now part of Coherent Corp.) on the Multi-wavelength Optical Transceivers Integrated on Node (MOTION) project (also part of ENLITENED) to develop CPO based on VCSELs for low cost and high radix links [49, 50]. Rain Tree Photonics recently demonstrated a 1.6 Tbps (224 Gbps/λ) optical engine for CPO based on fan-out wafer level packaging [51] at OFC 2024. NVIDIA has published an analysis of CPO discussing its feasibility and benefits [52], and they have also made a SiP light engine using GlobalFoundries Fotonix process [53]. TSMC also announced that it is working with Broadcom and NVIDIA to develop SiP for CPO [54].

While the power savings and density benefits of CPO solutions are clear, there are

a number of technical challenges that must be addressed from the device to module level. Starting at the device level, many pluggable transceivers use SiP Mach-Zehnder modulators (MZM), which consumer a significant amount of area due to their relatively large V_π, limiting the ability to improve the bandwidth density. Shrinking the modulators comes with the trade-off of higher voltage swing requirements to achieve the same optical modulation amplitude. These challenges can be addressed with co-design of the driving electronics and modulator, but the material properties of silicon will always limit the efficiency. Ring modulators offer very compact devices and enable dense wavelength division multiplexed (DWDM) link architectures, but they require wavelength locking feedback loops and more complex signal pre-distortion to compensate for their non-linear response [55]. Careful design is required to enable low DWDM crosstalk, though analysis by NVIDIA has shown that the concept is feasible [52]. Electro-absorption modulators (EAMs) integrated on Si also offer compact solution with good modulation efficiency, but fabrication is challenging. There have been some successful demonstrations of high speed EAMs integrated via micro-transfer printing and wafer bonding [56, 57, 58].

The increased component density also leads to challenges with thermal management where copper heat spreaders and cold plates with liquid cooling will likely be required [55, 52, 59], though Broadcom showed its CPO solution with air cooling [44]. Maintaining acceptable temperatures below 100°C for the high power density from the EICs with enough thermal isolation to keep the PICs below ∼80°C will require more separation between the EIC and the PICs or efficient cooling solutions. Thermal expansion can also lead to issues with mechanical bowing, which will create fiber misalignment. To address thermal and reliability concerns, external lasers are often proposed for CPO to maintain efficiency and enable replacement in case of laser failure.

Broadening out to the module and system level, reliability and serviceability are major concerns since tight integration of the optical modules makes replacement of one

module difficult if not impossible depending on the mounting and cooling design. There has been some progress on creating standards for CPO, with the Optical Internetworking Forum (OIF) publishing an implementation agreement (IA) for 3.2T CPO modules [60]. The IA and past demonstrations have shown integration of optical modules using high speed sockets, making replacement possible, but servicing for one module would likely take the entire switch systems offline, especially if liquid cooling solutions like the one in [59] are used.

The manufacturing cost and complexity are also major challenges with packaging and test are major contributors. The large fiber count of single mode fiber (SMF) and polarization maintaining fiber (PMF) adds cost and the fiber alignment process is also time consuming and expensive. V-groove alignment structures offer some improvement, but there are still issues with epoxy curing time and yield [59]. Issues with assembly have a large impact on yield and cost, since they typically occur at the final stage of assembly. Intel has recently shown a micro-optic glass bridge based using a periscope, which can be added earlier in the assembly process for better yield [61].

The efforts from Cisco, Broadcom, Intel, NVIDIA, and other companies show that the technical challenges can be overcome. Increases in production volume will likely lead to lower costs, but the timeline to more broad adoption and profitability of CPO solutions remains to be seen.

1.2.3 Optical Switching

Expanding out to the view of the data center as a whole, changes in the network architecture can have a much larger impact compared to individual links. Optical switching is a path to significant power savings and cost reduction compared to traditional electrical switching. Optical switches can be implemented with free-space beam steering using

arrays of micro-electro-mechanical system (MEMS) mirrors or liquid crystal pixels, with bulk gratings or planar arrayed waveguide gratings (AWG), with integrated photonics using a network of 2×2 switch cells, or with a combination of multiple methods. There are trade-offs with size, cost, port count scaling, wavelength selectivity, polarization dependency, switching speed, cross-talk, routing flexibility, and insertion loss for different solutions. The cost and power reduction of optical switching was recently demonstrated by Google. They reported a reduction of 30% in capital expenditure and 41% in power by changing from a Clos to a direct-connect topology using custom MEMS based optical circuit switches (OCS) for dynamic topology reconfiguration [62]. Optical switches provide lower latency and enable software defined data center network reconfigurability, which can be used for fast expansion with minimal interruption and optimization of job performance [63]. Reconfigurable optical switch networks can be leveraged to improve data center task execution through optimization of resource allocation in disaggregated data center networks [64]. Since optical switches do not perform any signal conversion, they are also transparent to the modulation format and bit rate. These benefits are valuable in cloud service and machine learning data center networks. Product development has been on the rise with Calient, Accelink, DiCon, and Agiltron offering MEMS optical switches; Polatis offering free-space piezo-electric beam steering optical switches; and Coherent demonstrating switches with liquid crystal technology. A newer start-up, Drut Technologies, has also developed optical switches along with interface cards and management software for a full system solution. High switch radix is key for flattening the data center network to reduce latency, cost, and power consumption [65, 66]. The companies above are offering switches with 128×128 to 576×576 ports. LightCounting forecasts that OCS sales will increase with a 28% CAGR, reaching over $500M by 2029 [67].

The current switch products are useful for slow network topology changes with re-

configuration times on the order of several milliseconds; however, this is not ideal for changing workloads. Low latency and better bandwidth utilization can be achieved with faster switching times, using switches based on integrated photonics. While these switches offer faster switching times on the order of 10 μs for thermo-optic switches to 10 ns for electro-optics switches, there are significant challenges with achieving low loss and high port count with demonstrations typically exhibiting >10 dB of loss and port count below 32 ×32 [66]. Larger port counts with lower loss are possible with low loss materials like thin film lithium niobate [68]. More development is needed before integrated photonics switches are ready to compete with existing free space optical switches.

In all cases, some insertion loss is inevitable, and link budgets are highly constrained for data center applications. Google was forced to implement new DSP and FEC techniques to overcome the additional losses [63]. Coherent links provide an advantage compared to IMDD with higher receiver sensitivity which enables much larger link budgets to incorporate optical switching [38]. The transparency of optical switches to modulation format also aids in reducing the barrier to implementing coherent transceivers. While DSP requirements remain a barrier for coherent to enter into intra-data center markets, there are efforts to simplify the coherent architecture for reduced DSP [69, 70] and improve the efficiency of coherent DSP [71]. In Section 6.2, I will also show a coherent link demonstration using low speed analog optical signal processing with commercial PAM4 DSP, showing that coherent communications can be implemented with minimal changes to existing protocols while unlocking larger link budgets for optical switching.

1.3 Preview of Dissertation

With an understanding of the benefits that coherent links can provide to address data center scaling challenges, this dissertation will discuss the different material platforms and

component design details which comprise the overall PIC design in Chapter 2. My work on a single polarization coherent receiver, designed for analog coherent with an OPLL, using an InP offset quantum well (QW) platform will be discussed in Chapter 3. Building on knowledge from the first InP receiver fabrication, Chapter 4 will provide an overview of a second generation InP receiver and lessons learned from the process. To examine the capabilities of silicon photonics platforms for coherent transceivers, Chapter 5 will review O-band integrated lasers and coherent receivers fabricated by Intel's platform and a coherent receiver made using GlobalFoundries 45SPCLO (Fotonix). The receiver PICs will be tested in short reach links to demonstrate their performance in Chapter 6. The dissertation will conclude with an outlook on coherent for data centers and future work.

Chapter 2

PIC Design for Coherent Communication

As discussed in Section 1.1, InP was used for fabricating the first coherent TX and RX PICs. While InP is still the platform of choice for long-haul coherent communication, silicon on insulator (SOI) and thin film lithium niobate (TFLN) on silicon platforms also offer good performance and manufacturability at high volume. This chapter provides an overview of coherent optical communications in Section 2.1, provides a comparison of material platforms to understand their benefits and limitations for coherent transmitter and receiver PICs in Section 2.2, and discusses the design details for the main photonic components in Section 2.3.

2.1 Basics of Coherent Optical Communications

Electromagnetic fields have multiple properties - amplitude, phase, frequency, and polarization. For optical communications, data is encoded onto the amplitude and phase of the electric field. To maintain a constant frequency, a continuous wave (CW) laser is

used as the source of the field. IMDD only uses the amplitude of the field while coherent modulation uses amplitude and phase. The electric field can be expressed as shown in Eqn. 2.1.

$$E_{sig} = E_0(t)e^{(i\omega_{sig}t+\theta_{sig})} \tag{2.1}$$

To modulate the amplitude and phase of E_{sig}, a nested MZM structure is typically used with a static 90°phase shift between the two MZMs, leading to in-phase and quadrature channels which form the overall IQ modulator (IQM). For PIC based IQMs, TE polarization is maintained on chip, but dual polarization (DP) data output can be achieved by integrating a polarization beam rotator and combiner (PBC) right before the output of the TX with a corresponding polarization beam splitter (PBS) at the RX input. When the signal fields pass through the optical fiber, imperfections in the fiber geometry and material properties lead to rotation of the the polarization state. To correctly recover the transmitted data, corrections must be applied either to the optical signal, using a polarization controller (PC), or to the electrical signal from the photodetectors, using PC digital signal processing (DSP) algorithms. At the receiver, E_{sig} must interfere with another electric field to demodulate the data encoded in the phase. This is required because the photodetectors which are used to convert the optical signal back to an electrical signal are only sensitive, with a responsivity R_{PD} in A/W, to the power of the field, given by $|E^2|$. The interfering field is provided by a second laser (often called a local oscillator) or by a parallel reference path from the original TX laser. To transform the phase modulation into amplitude modulation, a 90°optical hybrid structure is used for each polarization. The structure has inputs for the signal and reference, and it has 4 outputs (2 differential pairs) for the I and Q data [72]. Each output port has a sinusoidal transmission which depends on the relative phase between the signal and reference fields. The sinusoidal output port transmission curves are each shifted by a multiple of

90°, giving the hybrid its name. The balance in power between the differential pairs and the accuracy of the phase dependent transmission are key to recovering the transmitted data. More details on the 90°hybrid will be discussed in Section 2.3.3. In the ideal case, the output fields are expressed as shown in Eqn. 2.2 - 2.5, where the differential I and Q output pairs are E_{out1}, E_{out2} and E_{out3}, E_{out4}.

$$E_{out1} = \frac{1}{2}(E_{sig} + E_{ref}) \tag{2.2}$$

$$E_{out2} = \frac{1}{2}(E_{sig} - E_{ref}) \tag{2.3}$$

$$E_{out3} = \frac{1}{2}(E_{sig} + iE_{ref}) \tag{2.4}$$

$$E_{out4} = \frac{1}{2}(E_{sig} - iE_{ref}) \tag{2.5}$$

The photocurrent which is digitally processed to recover the data depends on the power of the fields. For a more sensitive receiver, the power of the reference field can be increased, boosting the photocurrent after the signal and reference interfere in the 90°hybrid. The photocurrent from the I and Q pairs are given by Eqn. 2.6 - 2.8, which show that the current scales with the square root of reference power P_{ref} times the signal power P_{sig}. This is another advantage of coherent modulation over IMDD.

$$I_I(t) = I_{out1}(t) - I_{out2}(t) = R_{PD}\sqrt{P_{sig}P_{ref}}cos(\theta_{sig}(t) - \theta_{ref}(t)) \tag{2.6}$$

$$I_Q(t) = I_{out3}(t) - I_{out4}(t) = R_{PD}\sqrt{P_{sig}P_{ref}}sin(\theta_{sig}(t) - \theta_{ref}(t)) \tag{2.7}$$

$$I_{tot}(t) = I_I(t) + iI_Q(t) = R_{PD}\sqrt{P_{sig}P_{ref}}e^{i[\theta_{sig}(t) - \theta_{ref}(t)]} \tag{2.8}$$

With the ability to modulate the phase and amplitude, a 2D constellation of points can be constructed which decodes the position in IQ space into a sequence of bits. Each position is referred to as a symbol where $log_2(n)$ of the number of positions determines the number

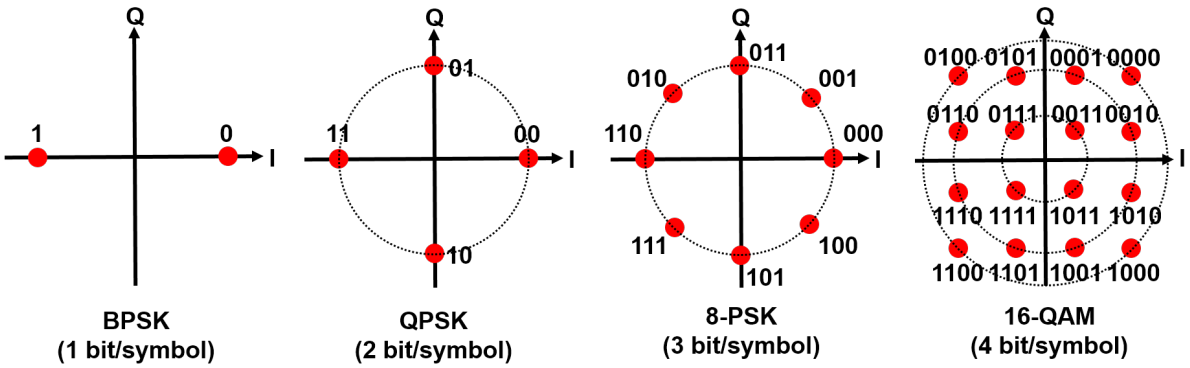


Figure 2.1: Example constellations are shown for coherent modulation formats with increasing bits/symbol.

of bits which is encoded in each symbol. Figure 2.1 shows four example constellations – binary, quadrature, 8 phase shift keying (PSK), and 16 quadrature amplitude modulation (QAM). To minimize the probability of bit errors, the encoding typically follows a rule where there is only one bit difference adjacent symbols. All coherent transceivers require a CW laser, IQM, and receiver, but there are multiple different potential architectures. Figure 2.2 shows block diagrams for 6 different architectures with equal total bit rates. Traditionally, a coherent transceiver includes separate TX and RX lasers, as shown in Fig. 2.2(a) which are kept at the same wavelength within a few GHz. To adjust for the frequency offset, compensate for polarization rotation, and recover the phase, a complex set of DSP algorithms are implemented on a custom circuit. This works well for long haul coherent transmission, but it is costly and uses a large amount of power. For shorter reaches, self-homodyne and analog controlled homodyne techniques do not rely on the complex coherent DSP. All self-homodyne approaches use a single source laser for the signal output and the carrier reference output. This removes the need for frequency offset compensation, but polarization and phase recovery are still required. For the approaches where the signal and carrier are on parallel fibers for spatial division multiplexing, as shown in Fig. 2.2(b) - (d), the fiber path lengths must be closely matched to avoid issues

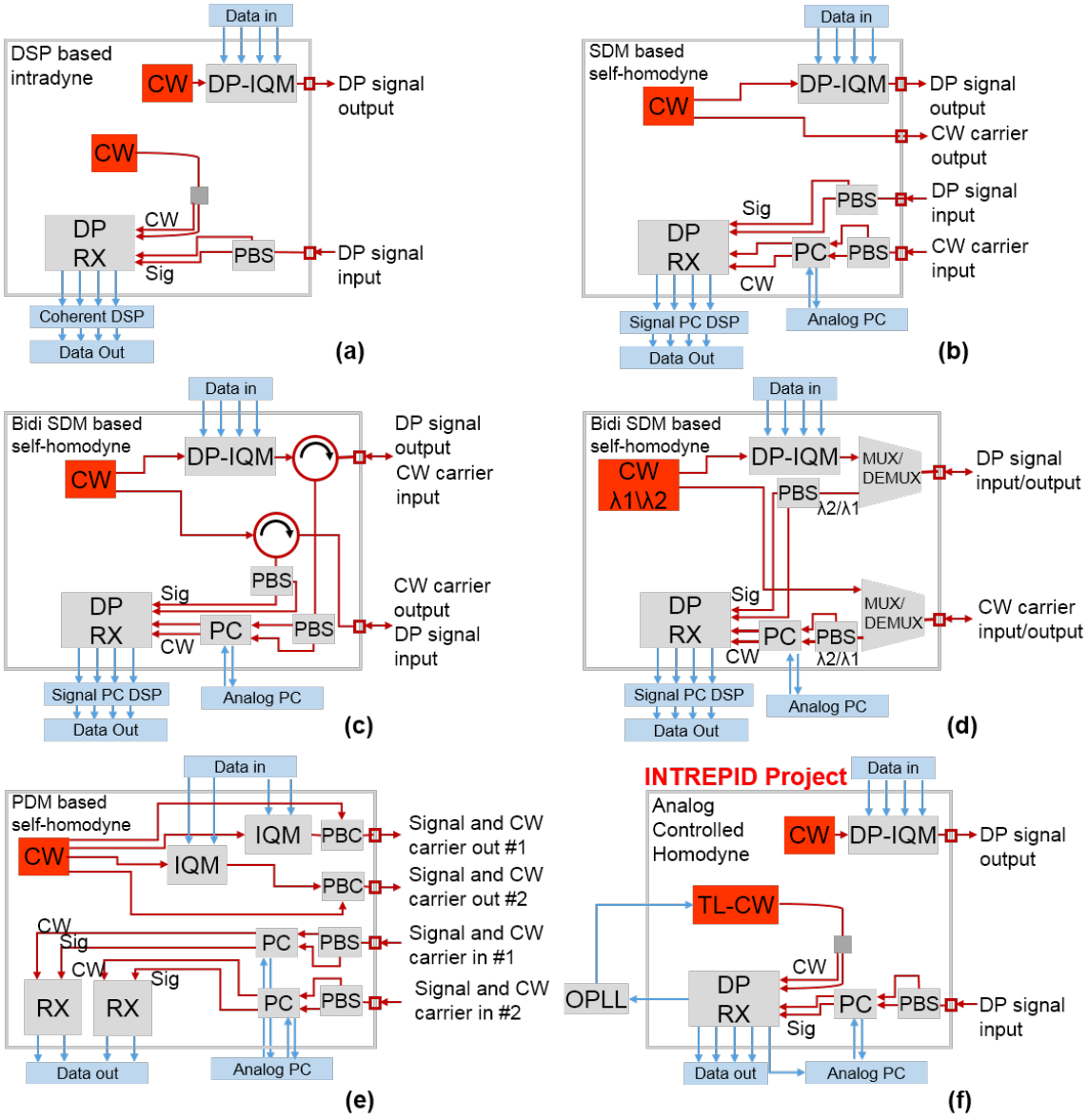


Figure 2.2: Block diagram examples of coherent transceivers using (a) traditional intradyne with DSP, (b) self-homodyne with parallel fiber SDM, (c) circulator based bidirectional SDM self-homodyne, (d) wavelength filter based bidirectional SDM self--homodyne, (e) analog PC based PDM self-homodyne, and (f) OPLL based homodyne architectures show several approaches for achieving data transmission on 4 lanes.

with phase recovery. Reducing the fiber count helps with packaging cost and reliability, so bidirectional (Bidi) architectures have been proposed using wavelength MUX/DEMUX filters with different transmit and receive wavelengths or using optical circulators. These optical elements add complexity and cost to the transceiver, since they are frequently implemented as micro-optic elements, between the PIC and the fiber output from the module. To avoid fiber induced power fading of the carrier between the two received polarizations, a PC is introduced to maintain a constant power split. The polarization recovery for the signal is still handled via DSP algorithms.

A polarization division multiplexing (PDM) approach enables ideal path length matching for simplified phase recovery, but four fibers are required to acheive the same total bit rate as the other architectures. With PDM, the signal and CW carrier are sent on orthogonal polarizations. An analog PC can be made on the PIC for polarization recovery with low cost and moderate complexity. With this architecture, the use of specialized DSP is eliminated, so it is compatible with systems using standard IMDD transceivers. While the physical implementation of the analog PC is relatively simple, tracking the input polarization when there are disturbances to the fiber and avoiding resets of the PC tuning elements are major design challenges. A prototype version of this architecture will be discussed in Section 6.2.

Using an OPLL, mentioned in Section 1.2, the frequency and phase recovery DSP is replaced by an analog feedback circuit. An analog PC is used for polarization recover of the signal. This has the potential to reduce power consumption, and it also compatible with systems using standard IMDD transceivers. This architecture was the focus of the INTREPID project. It sought to develop novel O-band PICs with tunable lasers (TL) and integrated PC and to make novel EICs for the OPLL. While this architecture provides excellent performance in terms of spectral efficiency, power consumption, and compatibility with IMDD systems, it also presents the largest challenge for integration

and analog control. Section 3.1, 4.1, and 5.3 discuss multiple RX PIC designs intended for integration with an OPLL.

These six examples provide an overview of the different design choices and major building blocks for coherent transceivers, but there are numerous other design decisions which determine the performance of the individual building blocks and the overall system. The material platform used for each building block is one of the first major decisions when designing a transceiver module. This will be discussed in more detail in Section 2.2. The overall performance of the transceiver depends on multiple performance metrics from each of the building blocks. High laser power and low linewidth are optimal. Modulators are designed for high extinction ratio (ER), low π phase shift voltage (V_π), high optical and electro-optical bandwidth, low insertion loss (IL), and compact size. Coherent receivers must also have high bandwidth, low noise floor, low IL, low phase error, and compact size. The combined performance of all the elements determines the maximum bit rate and the bit error rate (BER) sensitivity to receiver input power and signal to noise ratio (SNR). More details on the laser, modulator, 90°-hybrid, and photodetectors will be discussed in Sections 2.3.1, 2.3.2, 2.3.3, and 2.3.4, respectively. More comprehensive details on the building blocks and different system considerations for coherent optical links can be found in [4, 10, 73, 74, 75, 76], among other books.

2.2 Material and Integration Platforms

The first coherent PICs were made using InP, and it remains the primary material platform for long haul coherent PICs. While III-V materials on InP substrates have excellent material properties for both modulation and photodetection, silicon on insulator and thin film lithium niobate (TFLN) offer advantages in scalability and integration. While Coherent Inc. recently expanded to 6 inch InP wafers [77], silicon and TFLN

are able to utilize larger 8 to 12 inch Si wafers. With advanced integration techniques, it is possible to combine the advantages of each platform together. Integration of III-V material on silicon has been a major area of research and development for the last decade with continual improvements in different integration techniques. More integration of SiP with InP may happen with Infinera entering the data center market and gaining access to more SiP technology since they were acquired by Nokia [78, 79]. The following sections will provide a comparison of the capabilities and performance of the main material platforms.

2.2.1 Indium Phosphide (InP)

InP is the most mature of the optical communications material platforms with decades of research and development from universities and companies, including AOI, Coherent, Infinera, Lumentum, Neophotonics, NTT, Sumitomo, and many others. InP, and related III-V compounds, have a direct bandgap and strong electro-optical effects, making them ideal for lasers, modulators, and detectors. With advancements in metal-organic chemical vapor deposition (MOCVD) and other fabrication processes, there is large amount of flexibility when optimizing the epitaxial layers and PIC process flow. There are several PIC integration platforms with varying design and processing complexity. Offset QW, dual QW, asymmetric twin waveguide, QW intermixing, butt joint growth, and selective area growth are several popular platforms [80, 81]. While this complexity can make designs more challenging, the changes to the epitaxy and process enable integration of active and passive devices with minimal performance penalties.

For data- and telecommunications wavelengths, InP based lasers are a necessity. Monolithic InP has been the dominant platform for O-band and C-band lasers for decades. In the last 10 years, there has been significant development of heterogeneous

and hybrid lasers [82, 83, 84, 85, 86]. These still use InP based epitaxial layers for the gain material, but the laser cavity is formed by integrating the epitaxy with an SOI platform. There are multiple methods for achieving this integration which will be discussed in Section 2.3.1.

InP based modulators benefit from the Franz-Keldysh, quantum-confined Stark, and free-carrier absorption effects for the amplitude and phase of input laser light. These effects enable efficient and high speed modulation, but they do not have a linear relationship with driving voltage. These effects lead to chirp and distortions in the transmitted data, with more pronounced effects at higher drive swing [87]. At OFC 2024, NTT presented a >100 GHz InP-based modulator with $V_pi = 1.5V$ for beyond 200 Gbaud modulation using a specialized n-i-p-n structure and carefully designed capacitively-loaded traveling-wave electrodes (CL-TWE) that are 3.6 mm long [88]. This is one of best modulators in any platform in terms of BW and modulation efficiency, with only some novel plasmonic or Si-organic-hybrid modulators having higher bandwidth. While laser and modulator performance on InP is excellent, passives often have higher losses and lower fabrication yield. The material properties of InP typically lead to higher insertion losses compared to Si, and the process control for InP etching is more challenging, leading to more dimensional variation. These challenges have made it difficult to realize fabrication tolerant polarization rotators and splitters on InP with recent research showing some progress [89, 90, 91]. Another major argument against InP is the difficulty with scaling to high volume. While wafer sizes and yield have increased over the years, InP fabrication is still more expensive than Si and not as well equipped to meet the large demand for transceivers to connect AI clusters and data centers. For high volume, integration of InP on Si is the popular solution, but there are several integration methods (hybrid, heterogeneous, monolithic) with trade-offs in fabrication complexity, cost, and integration density [92].

2.2.2 Silicon on Insulator (SOI)

Silicon photonics (siP) has matured and expanded rapidly over the past 15 years with manufacturing dominated by foundries (e.g. AIM Photoncis, AMF, CEA-Leti, Cornerstone, Global Foundries, IHP, Imec, SkyWater, Tower, TSMC, etc.) offering silicon photonics processes while a only few other private companies (e.g. Intel, Skorpios) operate their own fabrication facilities. With high development and operating costs, most companies design SiP products while using a foundry for fabrication. The development of SiP modulators began in the late 1980s with the analysis by Soref and Bennett [93] which found that the refractive index could be modulated via the free carrier plasma effect. Initial work to produce low loss passive components and high speed modulators was aided by the existing silicon CMOS ecosystem and the years of Si fabrication development. With continual development in the SiP ecosystem, typical SiP foundry offerings include a variety of passive components, high speed pn modulators, thermal phase tuners, and Ge PDs on 300 mm wafers [94, 95]. Silicon has advantages in wafer size, waveguide loss, component density, production cost, and integration with CMOS electronics. Si nitride (SiN) waveguides are also offered by several foundries, providing even lower losses compared to standard SOI [96, 97]. As mentioned previously, the primary gap in silicon photonics is the lack of integrated gain. This is an active area of development with heterogeneous integration demonstrated by Intel, Tower, and Nexus Photonics, and Skorpios [98, 99, 100, 101]. Other laser integration methods are also in development and will be discussed more in Section 2.3.1. Relative to InP, modulation efficiency and bandwidth are also lower for pn junction based Si modulators, but this deficiency can also be resolved with heterogeneous integration [102, 103]. Advanced modulators using III-V EAMs [104, 57], Si-organic hybrid (SOH) [105], barium titanate (BTO) [106], lithium tantalate (LTO) [107], plasmonic-organic-hybrid (POH) [108], and

thin film lithium niobate (TFLN) [109] have all been demonstrated. Table 2.2.4 provides a performance comparison between the different modulator materials. Of the multiple modulator materials, TFLN on SOI is the most mature.

2.2.3 Thin Film Lithium Niobate (TFLN)

Bulk lithium niobate has been a high performance modulation material for decades, but TFLN modulators using a lithium niobate on insulator (LNOI) platform have only been developing over the last decade. Several companies - including Hyperlight, Fujitsu, Liobate, and Eoptolink - have been refining the fabrication and design of TFLN modulators. Lithium niobate is an advantageous modulator material because it has low loss, high bandwidth, and linear modulation via the Pockel's effect. Using Si 6" to 8" substrates, TFLN also benefits from large volume manufacturing. Modulators with >100 GHz BW have been demonstrated by multiple groups and companies [31, 110]. For integration density, TFLN not the best material because it has a lower modulation efficiency compared to InP, leading to longer modulator lengths. New designs have been proposed to improve the modulation efficiency using thick co-planar waveguide electrodes [111]. Continued development has been reducing fabrication difficulties, but there are material quality and etching challenges where more reliability and yield data is still needed. The TFLN platform also lacks lasers and photodiodes, but there have been successful research demonstrations of heterogeneous III-V wafer bonding to add these elements [112, 113].

2.2.4 Modulator and Photodetector Comparison

Competition between platforms for share of the booming data center and AI market will continue to drive innovation in modulator and photodetector designs. Unless pure InP modulator costs can match the next generation of SiP, it is likely that Si MZMs

will continue to grow in popularity. In the next 5 to 10 years, foundries and transceiver vendors may introduce products using novel modulator materials on SOI to keep up with the BW scaling. Table 2.2.4 provides a comparison between pure InP, pure SOI, and heterogeneous modulators. The table covers several designs and materials, but there are many other designs not included. For photodetectors, InGaAs on InP and Ge on Si have both demonstrated excellent performance. Since Ge on Si PDs have gained maturity on SiP, there is not a major incentive for foundries that already use Ge to develop integration processes for high speed InGaAs PDs on Si, but micro-transfer printing them to a low loss passive platform is being explored by Ligentec [114, 115]. In addition to Table 2.2.4, BW vs responsivity comparisons of III-V PDs can be found in [116, 117]. A tabular comparison of several metrics for WG PDs can be found in [118, 119, 120].

2.3 Photonic Component Design

As discussed in Section 2.1, the laser, modulator, 90°-hybrid, and photodiodes are the main components that are critical to the overall design of PICs for coherent communications. This section will cover the design considerations for each of these components.

2.3.1 Integrated Laser

The advantages of miniaturization, improved optical coupling, higher manufacturing volume, and electronic control provide the foundation for the development of integrated lasers, and the diverse set of applications powered by these lasers (e.g. transceivers, LIDAR, quantum computing, chemical sensing, optical coherence tomography, etc.) has driven their continued growth and advancement.

The first integrated lasers were made with a monolithic integration platform where the laser and PIC were fabricated on the same wafer. Initially, the wafer material platforms

Table 2.1: Modulator performance comparison

Material/ Platform	Design	λ (nm)	3,6 dB EO BW (GHz)	V_{pi} (V)	$V_{pi}L$ (V-cm)	ER (dB)	Length (mm)	Ref.
InP	CL-TWMZM	C-band	>67, -	1.5	0.54	>10	3.6	[121]
InP	CL-TWMZM	C-band	>100, 110	1.5	0.54	>25	3.6	[88]
InP	TWMZM	C-band	54, >65	2	0.55	25	4	[122]
InP	TWMZM	C-band	110, -	3.4	0.7±0.4	15.3	1	[123]
InP	EAM	O-band	85, 90	–	–	3	0.075	[124]
InP	TWEAM	C-band	>100, -	–	–	>20	0.18	[125]
SOI	TWMZM	C-band	44, 62	8	1.6	>25	2	[126]
SOI	CL-TWMZM	C-band	61, 78	8	3.2	–	4	[127]
SOI	MRM	O-band	77, 81	<1.5	0.5	3.8	0.012	[128]
SOI	slow-light	1550±4	110, >120	78[1]	0.96	3	0.124	[129]
InP/SOI	EAM	O-band	60,67	–	–	–	–	[57]
Ge/SOI	EAM	L-band	100, >110	–	–	2.3	0.02	[130]
SOH/SOI	MZM	O-band	100, -	0.92	0.046	20	0.5	[105]
BTO/SiN	MZM	C-band	110, -	6.4	0.0096	13.3	0.015	[106]
LTO/SOI	TWMZM	C-band	110, -	4.8	2.88	–	6	[107]
POH/SOI	MRTM	C-band	176 , -	1.67	0.015	12	0.028	[108]
TFLN/SOI	TWMZM	O-band	70, >100	1.7	3.06	20	18	[109]
TFLN/SOI	TWMZM	C-band	110, >125	1	2.3	35	23	[131]
TFLN/SOI	TWMZM	O-band	110, >125	4.37	2.36		5.4	[110]
TFLN/SOI	TWMZM	C-band	110, >125	5.78	3.12		5.4	[110]

[1] slow-light phase efficiency is very nonlinear

EAM: electro-absorption mod., CL-TW: capacitively-loaded traveling-wave
MRM: micro-ring mod., SOH: Si-organic hybrid, BTO: barium titanate
LTO: lithium tantalate, POH: plasmonic-organic-hybrid, RTM: racetrack mod.

Table 2.2: Photodetector performance comparison

Material/ Platform	Design	R_{ext} (A/W)	λ (nm)	OE BW (GHz)	I_{dark} (nA)	RF P_{sat} (dBm)	Ref.
InGaAs/InP	PIN	0.5	C-band	120	–	–	[132]
InGaAs/InP	PIN	0.4	C-band	145	<40	-10	[133]
InGaAs/InP	MUTC	0.5	C-band	119	1.5	-1.2	[118]
InGaAs/InP	MUTC	0.31	C-band	165	<0.1	-1.7	[116]
InGaAs/InP	MUTC	0.24	C-band	220	<0.1	-1.8	[116]
Ge/Si	PIN	0.78-1.05*	C-band	67	<6.4	–	[134]
Ge/Si	PIN	0.74*	1550	67	<4	–	[135]
Ge/Si	PIN	0.89*	C-band	80	<10	–	[136]
Ge/Si	PIN	0.95*	1550	103	<7	–	[137]
Ge/Si	PIN	0.2	C-band	240	<100	–	[119]

*R_{int} vs R_{ext} not made clear

were limited to the direct bandgap semiconductors (e.g. GaAs, InP, InGaAsP, InAlGaAs, InP) which are required for laser gain. Innovations in fabrication and packaging have led to new integration techniques which can be grouped into hybrid, heterogeneous, and monolithic methods.

Hybrid integration involves packaging a complete laser gain chip with an separate PIC through flip-chip bonding, butt-joint edge coupling, or photonic wire bonding [138, 139, 85]. With flip chip-bonding, devices can be screened before integration to increase yield. The bonding process uses solder bumps to connect a completed III-V device, such as a InP based laser or photodetector, to a separate substrate with metalized pads. While this is a mature process, it is still challenging to achieve low (<2 dB) coupling loss, and it is less flexible with the size and arrange of the chips compared to other integration methods. While the self-alignment of the solder bumps via surface tension, aids in optical alignment, mechanical stops are required for required for reliable low coupling loss, adding complexity to the packaging. The optical coupling with flip-chip bonding may use butt coupling, grating coupling, or a 45° etched mirror [85]. While the position accuracy requirements for grating and mirror coupling are lower due to the

larger beam diameter, the best case coupling losses are also higher, and grating couplers limit the spectral bandwidth. Other designs may use butt coupling without flip chip bonding by precisely aligning the waveguides at the edges of the chips. In all cases, it is important to design the mode size and shape to closely match between the two chips for optimal coupling, which often requires the use of spot size converters. Photonic wire bonding may be used to act as a spot size converter and to remove the precise alignment requirements for optical coupling. A 3D polymer waveguide is aligned to both chips and written lithographically, resulting in low coupling loss. This method is advantageous for relaxing chip placement tolerances, but the relatively long write times for the polymer waveguides make it less suitable for high volume applications.

Heterogeneous integration involves bonding two separate wafers (or smaller dies to wafers) together and completing the fabrication process to define the active and passive devices together on the bonded wafers. With this method, only moderate precision is required for placement before bonding, and precise waveguide alignment is achieved using lithographic pattern alignment and etching on the bonded wafers. With evanescent coupling tapers, low losses can be achieved; passive devices can be more flexibly routed in the bonding area; and a large number of active devices can be defined simultaneously during the post-bond fabrication steps. To maintain a strong bond, the surface preparation and interface material properties are critical. Heterogeneous integration began by using thin polymer layers for their tolerance imperfections in surface preparation, temperature stability, chemical resistance, and low cost [139]. The low thermal conductivity of polymers hinders active device performance, which motivated the development of direct bonding. Though more stringent surface preparation and flatness are required for a reliable bond, direct bonding utilizes the intermolecular forces between two pristine surfaces for integration without an interfacial adhesion layer. This process–which involves plasma surface treatment followed by compression bonding, and high temperature

annealing–was pioneered by the Bower's group at UCSB [82]. While mechanical strain and thermal expansion are concerns, a variety of III-V materials have been successfully bonded, and the process has been commercialized by Intel, resulting in highly reliable lasers which can be manufactured at high volume [83, 140, 98].

Micro-transfer printing (MTP) shares characteristics with hybrid and heterogeneous integration. In many demonstrations, completed devices from one substrate are bonded to another with precise alignment required, similar to hybrid integration. It is possible to transfer partial devices and to continue processing after transfer printing, similar to heterogeneous integration. The transfer printing process uses a elastomeric stamp, typically PolyDiMethylSiloxane (PDMS), to adhere to a membrane device on a donor substrate and break thin tethers to lift it away. The stamp is positioned precisely over the receiving substrate and the device is carefully pressed into place. More details regarding the design of the donor membrane device and the transfer printing process can be found in [138, 85, 141, 142]. This technique provides flexibility in PIC design since small devices can be placed individually, and multiple donor substrates with different materials can be integrated together on one receiving substrate. Less material is wasted in the transfer process since, unlike heterogeneous wafer bonding, a substrate removal is not required, which leads to material cost savings. While the process has been commercialized successfully by X-Celeprint for micro-LEDs, photovoltaic cells, and other semiconductor devices, more process development is needed to enable high volume production of integrated lasers using micro-transfer printed III-V material. Recent laser demonstrations have shown good progress, but achieving low loss coupling for high laser power remains a challenge [143, 144, 145]. For companies already utilizing heterogeneous wafer bonding, switching to MTP for bonding blank membrane coupons rather than larger wafer chips may enable material cost savings with only small changes to existing processes.

Monolithic integration (or direct epitaxial growth) on silicon offers excellent scalabil-

ity, low cost, and dense integration by directly growing the laser gain material on large silicon wafers. This approach faces several technical challenges to achieve high quality III-V material due to the mismatch between the lattice constant, thermal expansion coefficient, and polarity of III-V materials compared to silicon. These differences can create threading and misfit dislocations, antiphase boundaries, and thermal cracking [146]. Techniques using offset cut Si substrates, buffer layers [147, 148], defect trapping and filter layers, v-groove patterned substrates [149], GaP-on-Si templates [150, 151], and lateral aspect ratio trapping growth have all been investigated as methods of reducing defect generation and propagation [138, 139, 146]. Much of the work on direct epitaxial growth has focused on quantum dot (QD) active material because its increased tolerance to defects, and its improved performance compared to quantum well material from its delta function density of states. While the methods above have been successfully employed, with many research demonstrations of high power QD lasers grown on Si, low loss coupling to Si or SiN waveguides remains a challenge. Most solutions are incompatible with the evanescent coupling currently used in heterogeneous wafer bonded lasers, and butt coupling losses need to be improved [148, 150, 152]. For high volume production of cleaved or etched facet lasers on large Si wafers, direct epitaxial growth has clear advantages and commercialization seems feasible in the near future. Integration of directly grown III-V elements into more complex PICs will require more development, but current research work shows promise.

Shifting back to the basics of laser design, regardless of the integration technology, all diode laser designs follow the same principles for calculating device performance. The primary equations governing the laser design are as follows [153]–

$$R = r_1 r_2 \tag{2.9}$$

Lasers need mirrors to form a cavity where in Eqn. 2.9, R is the mean mirror reflection coefficient and r_1 & r_2 are the field reflection coefficients of mirrors 1 & 2.

$$\alpha_m = \frac{1}{L} ln \left(\frac{1}{R} \right) \tag{2.10}$$

In Eqn. 2.10, α_{m} is the mirror loss which is defined per unit length based on the total cavity length, L.

$$\Gamma g = \langle \alpha_i \rangle + \alpha_m = \frac{1}{v_g \tau_p} \tag{2.11}$$

In steady state, Eqn. 2.11 shows the laser gain is equal to the loss where Γ is the confinement factor, g is the modal gain, $\langle \alpha_i \rangle$ is the average internal loss, v_g is photon group velocity, and τ_p is the photon lifetime.

$$\eta_d = \frac{\eta_i \alpha_m}{\langle \alpha_i \rangle + \alpha_m} \tag{2.12}$$

The laser differential efficiency η_d is calculated using Eqn. 2.12 where the carrier injection efficiency η_i is multiplied by the mirror loss divided by the total loss.

$$N_{th} = N_{tr} e^{(\langle \alpha_i \rangle + \alpha_m)/\Gamma g_{0N}} \tag{2.13}$$

As shown in Eqn. 2.13, there is an exponential relationship between $\mathrm{N_{th}}$ and N_{tr}, the threshold and transparency carrier densities, where g_{0N} is the gain coefficient.

$$P_0 = \eta_d \frac{h\nu}{q} (I - I_{th}) \tag{2.14}$$

Above the threshold current I_{th}, neglecting nonlinear effects, the laser optical output power P_0, is linearly related to the electrical current I by the differential efficiency and the photon energy $h\nu$ generated per electron charge q that recombines, where h is Planck's constant and ν is the laser frequency in Eqn. 2.14.

$$MSR = \frac{F_1(\lambda_0)\alpha_m(\lambda_0)[\alpha_i + \alpha_m(\lambda_1) - \Gamma g(\lambda_1)]}{F_1(\lambda_1)\alpha_m(\lambda_1)[\alpha_i + \alpha_m(\lambda_0) - \Gamma g(\lambda_0)]} \tag{2.15}$$

For single mode lasers, the mode suppression ratio (MSR) is defined by 2.15 where λ_1 and λ_0 are the wavelengths of the two competing modes and F_1 is the fraction power emitted from one side of the laser. Competing modes are often adjacent cavity modes spaced apart by $\Delta\lambda_{mode}$ based on the cavity length L and the optical group index $\overline{n_g}$ using Eqn. 2.16.

$$\Delta\lambda_{mode} = \frac{\lambda^2}{2\overline{n_g}L} \tag{2.16}$$

The equations above form the basis for the steady state analysis of diode lasers, but there are a diverse set of laser designs with more detailed analysis of the gain material, the mirror designs, and the dynamic laser behavior which are beyond the scope of this dissertation. Due to their good performance, distributed feedback (DFB) lasers are widely used in communications systems where a single wavelength is desired. For systems with channel reconfiguration, tunable lasers are often used. There have been many tunable laser designs including single distributed Bragg reflection (DBR), sampled grating (SG) DBR, ring resonator lasers, and interferometric cavity lasers. Multi-wavelength comb lasers for WDM are also growing in popularity, but they are not yet implemented in commercial transceivers. More details on integrated lasers for data centers can be found in [10], and Larry Coldren's laser textbook [153] is an excellent resources for the

fine details of diode laser design.

2.3.2 Coherent Transmitter Modulators

While not the main focus of my work, modulators are the second critical component for a coherent link. As mentioned in Section 2.1, the standard design of coherent modulators uses two nested MZM with high speed phase shifters and a 90° phase shift between them for I and Q channels, though there have been demonstrations of coherent modulators based on 3-arm modulators using EAMs [56, 154, 155]. For the high speed phase shifters, pure phase modulation is desired, especially for higher order modulation formats because amplitude modulation will add non-linear distortion to the modulated signal. Lithium niobate phase shifters exhibit the best linearity because they operate based on the Pockel's effect (also known as the linear electro-optic effect). InP phase shifters can be based on the Franz-Keldysh or quantum-confined Stark effects depending on whether quantum wells are used. The plasma dispersion effect is dominant in Si. While the effects on Si and InP often lead to a more efficient modulator (lower $V_\pi L$), they introduce some signal distortion due to their absorption modulation. More discussion of different modulator materials and designs can be found in [4, 10, 156].

Regardless of the material, the most common IQM designs use traveling-wave electrodes (TWE). With TWE, a single driver can be used for each MZM to send the GHz frequency signals through the electrodes which run parallel to the optical waveguides. The electrode design is a challenging aspect of achieving high performance modulators. The electrode transmission lines must be carefully designed to (1) match the electrical and optical velocities, (2) minimize the RC to maintain high BW, (3) minimize the RF transmission losses, and (4) reduction reflections from impedance mismatch. More details on the modeling and analysis of TWE can be found in [157, 158, 159].

With baud rates increasing to 100 Gbaud, the optimization of modulator design is increasing in sensitivity and importance. At current baud rates, modulator designs must take the full system into account during the design phase. Electro-optic simulation and co-design of the driver with the modulator is critical to optimizing performance [160, 161, 162].

2.3.3 Coherent Receiver 90°-Hybrids

As discussed in Section 2.1, the coherent receivers require a 90°-hybrid to demodulate the the optical signal from the transmitter. There are multiple structures capable of creating the required 90°phase relationship between the input and output ports to demodulate the phase encoded onto the optical signal. Several structures are shown in 2.3. Multimode interference (MMI) couplers are the primary method used for integrated

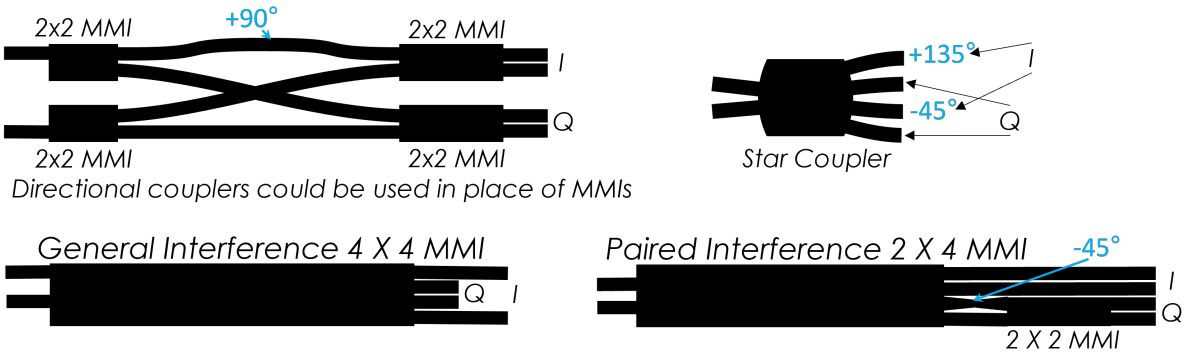


Figure 2.3: Different options for 90°-hybrid structures

photonic devices. All MMI couplers utilize the principle of self-imaging with coherent light in multimode waveguides. The principle of periodic self-imaging was first discovered by Talbot in 1836 when examining periodic bands produced by light guided between two closely spaced glass prisms [163]. This discovery was analyzed further and expanded by Rayleigh [164], Cowley[165], Tolansky[166], and others, leading to advances in fourier optics and interferometry. For integrated photonics, Ulrich described the principles of self

imaging in uniform slab waveguides and proposed the self-imaging optical strip guides which have become the modern MMI couplers [167, 168]. The operating principle of MMI couplers is based on the periodic interference patterns formed by multiple optical modes each traveling with different propagation constants β_v. The periodicity of the self-imaging can be derived, starting with the dispersion equation (2.17) in the multimode waveguide.

$$k_{yv}^2 + \beta_v^2 = k_0^2 n_r^2 \tag{2.17}$$

where k_0 is the free space wavenumber, n_r is the multimode ridge effective index, and k_{yv} is the lateral wavenumber for mode number "v" such that,

$$k_0 = \frac{2\pi}{\lambda_0} \tag{2.18}$$

$$k_{yv} = \frac{(v+1)\pi}{W_{ev}} \tag{2.19}$$

where λ_0 is the free space wavelength and W_{ev} is the effective width of the mode. This width takes the penetration depth of the Goos-Hahnchen phase shift into account [169]. To simplify the calculation, the effective mode width for higher order modes can be approximated as equal to the width of the fundamental mode (W_e), shown in eqn 2.20, assuming the penetration depths are nearly constant for all modes with a physical MMI width of W_M.

$$W_{ev} \simeq W_e = W_M + \frac{\lambda_0}{\pi}(n_r^2 - n_c^2)^{-1/2} \tag{2.20}$$

The propagation constants for all modes can also be approximated using Eqn. 2.18 through 2.19 with the binomial expansion, resulting in Eqn. 2.21.

$$\beta_v \simeq k_0 n_r - \frac{(v+1)^2 \pi \lambda_0}{4 n_r W_e} \tag{2.21}$$

The main parameter for determining the appropriate length for self-imaging is the beat length (L_π) of the two lowest-order modes given by

$$L_\pi = \frac{\pi}{\beta_0 - \beta_1} \simeq \frac{4 n_r W_e^2}{3 \lambda_0} \tag{2.22}$$

When examining the field distribution of an MMI coupler to identify the self-imaging locations, the input field $\Psi(y, z)$ can be expressed as a sum of the contributions from each of the guided modal fields $\psi_v(y)$ as shown in Eqn. 2.23 where c_v is the modal field excitation coefficient which can be estimated using overlap integrals between the input and modal fields [169].

$$\Psi(y, z) = \sum_{v=0}^{m-1} c_v \psi_v(y) e^{j(\omega t - \beta_v z)} \tag{2.23}$$

By assuming time invariance and removing phase of the fundamental mode ($v = 0$) as a reference factor, Eqn. 2.23 can be rewritten as Eqn. 2.24

$$\Psi(y, z) = \sum_{v=0}^{m-1} c_v \psi_v(y) e^{j(\beta_0 - \beta_v) z} \tag{2.24}$$

By expressing the field in terms of the propagation constants, the connection between L_π and the self-imaging property can be deduced. Using Eqn. 2.21 & 2.22 for $\beta_0 - \beta_v$, the field at some propagation distance $z = L$ can be expressed as

$$\Psi(y, L) = \sum_{v=0}^{m-1} c_v \psi_v(y) e^{j\frac{v(v+2)\pi}{3L_\pi}L} \tag{2.25}$$

Examining Eqn. 2.25, while keeping the symmetry of even and odd modes in mind, reveals that the input field is directly or mirror imaged when L is an even or odd integer multiple of $3L_\pi$.

$$\psi_v(-y) = \begin{cases} \psi_v(y) & \text{for v even} \\ -\psi_v(y) & \text{for v odd} \end{cases} \tag{2.26}$$

The symmetry of the modal fields in 2.26(c) comes from the symmetric rectangular MMI region and the boundary conditions for even and odd modes. For single images, the conditions in 2.27 and 2.28 must be true.

$$L = p(3L_\pi) \quad \text{with} \quad p = 0, 1, 2, ... \tag{2.27}$$

$$e^{j\frac{v(v+2)\pi}{3L_\pi}L} = 1 \quad \text{or} \quad (-1)^v \tag{2.28}$$

With even multiples p of $3L_\pi$, the even and odd modes will be in phase, directly replicating the input field. With odd multiples, the odd modes will be π out of phase, resulting in a mirrored image of the input field from the symmetry stated in Eqn.2.26.

When examining multiple self-images, it has been shown [170] that the lengths for multiple images of an N x N port MMI coupler is given by Eqn. 2.29, where the shortest length $p = 1$ is often used.

$$L = \frac{p}{N}(3L_\pi) = \frac{p}{N}\frac{3\pi}{\beta_0 - \beta_v} \tag{2.29}$$

The lengths for double images which would result from a 2 x 2 port coupler can be seen

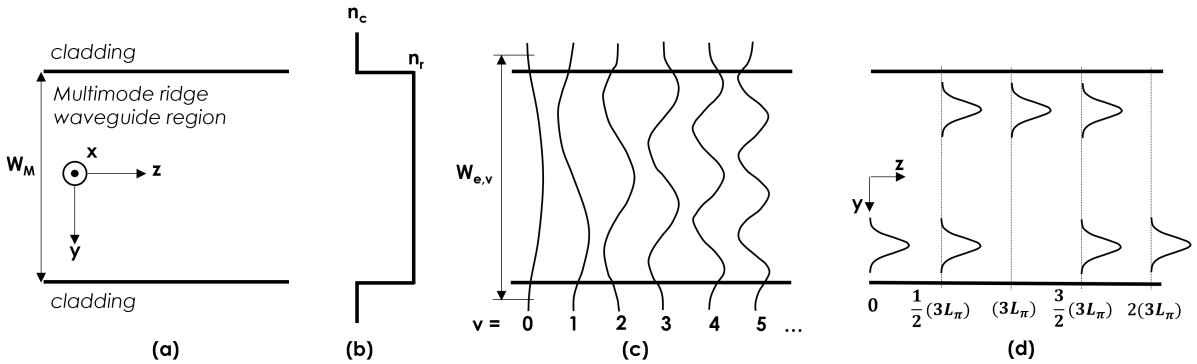


Figure 2.4: Illustration of self-imaging using multimode interference. A rectangular region (a) with ridge (n_r) and cladding (n_c) indices (b) is able to guide higher order modes (c) with different propagation consants (β_v). Inference between these modes enables periodic single- and multi-imaging of the input field illustrated in (d).

in 2.4(d). The phases of the input port "r" to the output port "s" (neglecting a constant phase) are given by Eqn. 2.30.

$$\phi_{rs} = \begin{cases} \phi_0 + \frac{\pi}{4N}(s-r)(2N+r-s) + \pi & \text{for r+s even} \\ \phi_0 + \frac{\pi}{4N}(r+s-1)(2N-r-s+1) & \text{for r+s odd} \end{cases} \tag{2.30}$$

where ϕ_0 is given by Eqn. 2.31.

$$\phi_0 = -\beta_0 \frac{3L_\pi}{N} - \frac{\pi}{N} - \frac{\pi}{4}(N-1) \tag{2.31}$$

By applying algebraic manipulations to the above equations, they can be combined into Eqn. 2.32, as shown in [171, 172].

$$\phi_{rs} = \phi_1 - \frac{\pi}{2}(-1)^{r+s+N} + \frac{\pi}{4N}[r + s - r^2 - s^2 + (-1)^{r+s+N}(2rs - r - s + \frac{1}{2})] \quad (2.32)$$

where the constant phase ϕ_1 is given by Eqn. 2.33.

$$\phi_1 = -\beta_0 \frac{3L_\pi}{N} - \frac{9\pi}{8N} + \frac{3\pi}{4} \quad (2.33)$$

Examining these equations for a 4x4 MMI coupler reveals that the phase relationship between the output ports allow the coupler to act as a 90°-hybrid for coherent receivers. When connecting to input 1&2, 1&3, 2&4, or 3&4, the difference in phase between the two inputs causes the net phase at each output port to be spaced apart by 90°. This is the basis for the general interference 4x4 MMI coupler shown in Fig. 2.3. For an ideal 4x4 MMI coupler, Eqn. 2.34 can be used to calculate the output fields at each of the four ports ($\kappa_{44} = \frac{1}{4}$)[173]. Figure 2.6 shows the transmittance of each of the output ports while varying the phase difference between the signal and LO input fields (with a constant $\frac{\pi}{4}$ shift on the LO). The 90°-hybrid relationship is clearly visible, with the peak of each port spaced 90°apart. The I and Q channel pairs, output 1&4 and 2&3, are also apparent.

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ E_4 \end{bmatrix} = \sqrt{\kappa_{44}} \begin{bmatrix} 1 & 0 & e^{-i\pi/4} & 0 \\ e^{3i\pi/4} & 0 & 1 & 0 \\ e^{-i\pi/4} & 0 & 1 & 0 \\ 1 & 0 & e^{3i\pi/4} & 0 \end{bmatrix} \begin{bmatrix} E_{LO} \\ 0 \\ E_{Sig} \\ 0 \end{bmatrix} \quad (2.34)$$

For the 90°-hybrid using 2x2 MMI couplers, there is a 90°phase difference between the through and cross paths. Using Eqn. 2.32, the through (ϕ_{11}, ϕ_{22}) phase is -45°and

the cross phase(ϕ_{12}, ϕ_{21}) is +45°. When connected together as shown in Fig. 2.3, the accumulated phase from the multiple though and cross paths, with an added 90°phase shift, creates the appropriate output phase relationship for a 90°-hybrid. For an ideal 2x2 MMI, Eqn. 2.35 and 2.36 below can be used to calculate the transmittance for the 90°-hybrid, where $\kappa_{22} = \frac{1}{2}$ for the MMI power splitting. To account for the waveguide cross, E_{arm2} and E_{arm3} swap positions in the input vector before the final matrix in Eqn. 2.36. Using these equations, Fig. 2.5 shows the 90°-hybrid relationship with the I and Q channel pairs from output 1&2 and 3&4. The plots demonstrate that the phase shift can be applied to any of the 4 middle arms of the hybrid while maintaining the 90°-hybrid relationship, but the phase to I/Q intensity demodulation scheme is altered. The code used for Fig. 2.5 can be found in Appendix A.

$$\begin{bmatrix} E_{arm1} \\ E_{arm2} \\ E_{arm3} \\ E_{arm4} \end{bmatrix} = \begin{bmatrix} e^{i\theta_1} & 0 & 0 & 0 \\ 0 & e^{i\theta_2} & 0 & 0 \\ 0 & 0 & e^{i\theta_3} & 0 \\ 0 & 0 & 0 & e^{i\theta_4} \end{bmatrix} \begin{bmatrix} \sqrt{\kappa_{22}} & \sqrt{\kappa_{22}}e^{\frac{-i\pi}{2}} & 0 & 0 \\ \sqrt{\kappa_{22}}e^{\frac{-i\pi}{2}} & \sqrt{\kappa_{22}} & 0 & 0 \\ 0 & 0 & \sqrt{\kappa_{22}} & \sqrt{\kappa_{22}}e^{\frac{-i\pi}{2}} \\ 0 & 0 & \sqrt{\kappa_{22}}e^{\frac{-i\pi}{2}} & \sqrt{\kappa_{22}} \end{bmatrix} \begin{bmatrix} E_{LO} \\ 0 \\ 0 \\ E_{Sig} \end{bmatrix} \tag{2.35}$$

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ E_4 \end{bmatrix} = \begin{bmatrix} \sqrt{\kappa_{22}} & \sqrt{\kappa_{22}}e^{\frac{-i\pi}{2}} & 0 & 0 \\ \sqrt{\kappa_{22}}e^{\frac{-i\pi}{2}} & \sqrt{\kappa_{22}} & 0 & 0 \\ 0 & 0 & \sqrt{\kappa_{22}} & \sqrt{\kappa_{22}}e^{\frac{-i\pi}{2}} \\ 0 & 0 & \sqrt{\kappa_{22}}e^{\frac{-i\pi}{2}} & \sqrt{\kappa_{22}} \end{bmatrix} \begin{bmatrix} E_{arm1} \\ E_{arm3} \\ E_{arm2} \\ E_{arm4} \end{bmatrix} \tag{2.36}$$

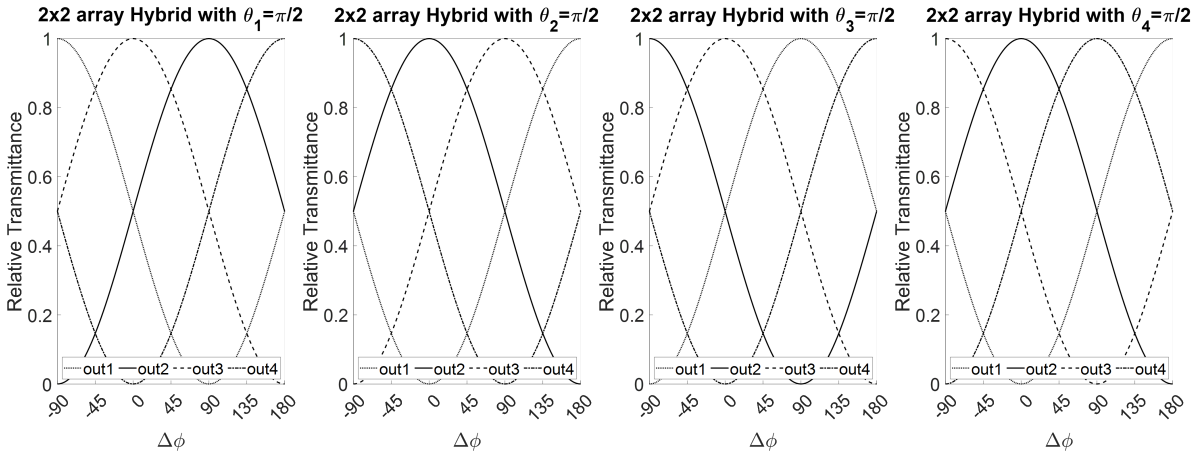


Figure 2.5: Relative Transmittance for the 90°-hybrid using 2x2 MMI couplers. The I/Q output pairs and 90°relation is maintained for a $\frac{\pi}{2}$ shift on any of the 4 middle arms.

The 2x4 Paired Interference MMI coupler operates using the same imaging principle as the general 4x4 MMI, but the input port positions are such that the input field does not excite mode $v = 2, 5, 8, ...$ in the because the peaks of the inputs are aligned with the position of the nulls for these modes. For this structure, the phases from input port 1&2 to the output ports are given by Eqn. 2.37 and 2.38 from [173]

$$\phi_{1y} = \frac{\pi}{16} y(10 + 2\rho - 3y) - \frac{9\pi}{16}\rho \tag{2.37}$$

$$\phi_{2y} = \frac{\pi}{16}[2(1+\rho)y - 3y^2 - \rho] + (\rho - \frac{1}{2})\pi \tag{2.38}$$

where $\rho = 0$ for an odd output port y and $\rho = 1$ for an even output port. These phase equations lead to 180°-hybrid behavior, so a phase shifter and a 2x2 MMI are added after the bottom or top pair of output ports to rotate the phase relation by 90°, creating the 90°-hybrid behavior [173]. Although a 2x2 MMI alone is sufficient to adjust the phase relationship, the phase shifter is added between the 2x4 and 2x2 MMI to improve the SNR by adjusting the transmission. By examining the transfer matrix as a function of the added phase shift before the 2x2 MMI for the Q-channel output, a shift ϕ_{Q12} can be calculated.

$$\phi_{Q12} = -\frac{\pi}{4} \tag{2.39}$$

When ϕ_{Q12} is set to $-\frac{\pi}{4}$, the difference in transmission between the Q-channel ports is maximized. The transfer matrices for the full hybrid structure (2x4 MMI, phase shifters, and the 2x2 MMI are shown in Eqn. 2.40 where $\kappa_{24} = \frac{1}{4}$ and $\kappa_{22} = \frac{1}{2}$ for the power splitting of each MMI. The variables θ_1 and θ_2 represent phase shifters on output 3 and 4 of the 2x4 MMI. To maximize the transmission, $\theta_1 - \theta_2 = \phi_{Q12} = -\frac{\pi}{4}$. Using Eqn. 2.40 (with a constant $\frac{-\pi}{4}$ shift on the LO), Fig. 2.6 shows the improvement in transmittance with $\phi_{Q12} = -\frac{\pi}{4}$. The code used for Fig. 2.6 can be found in Appendix A.

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ E_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & \sqrt{\kappa_{22}} & \sqrt{\kappa_{22}}e^{\frac{-i\pi}{2}} \\ 0 & 0 & \sqrt{\kappa_{22}}e^{\frac{-i\pi}{2}} & \sqrt{\kappa_{22}} \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & e^{i\theta_1} & 0 \\ 0 & 0 & 0 & e^{i\theta_2} \end{bmatrix} \sqrt{\kappa_{24}} \begin{bmatrix} 1 & e^{\frac{-3i\pi}{4}} & 0 & 0 \\ e^{\frac{-i\pi}{4}} & 1 & 0 & 0 \\ e^{\frac{-i\pi}{4}} & 1 & 0 & 0 \\ e^{-i\pi} & e^{\frac{i\pi}{4}} & 0 & 0 \end{bmatrix} \begin{bmatrix} E_{Sig} \\ E_{LO} \\ 0 \\ 0 \end{bmatrix} \tag{2.40}$$

Most coherent receivers use different variations of the MMI-based 90°-hybrids discussed above, but there are some unique variations that have been proposed which have smaller footprints, or other performance benefits. The most noteworthy variation is the tapered or wedge-shaped 2x4 + 2x2 MMI-based 90°-hybrids. It is a direct improvement to the hybrid design using a 2x4 paired interference coupler. With careful design of the taper length and ratio of the input to output widths, the length can be reduced and the

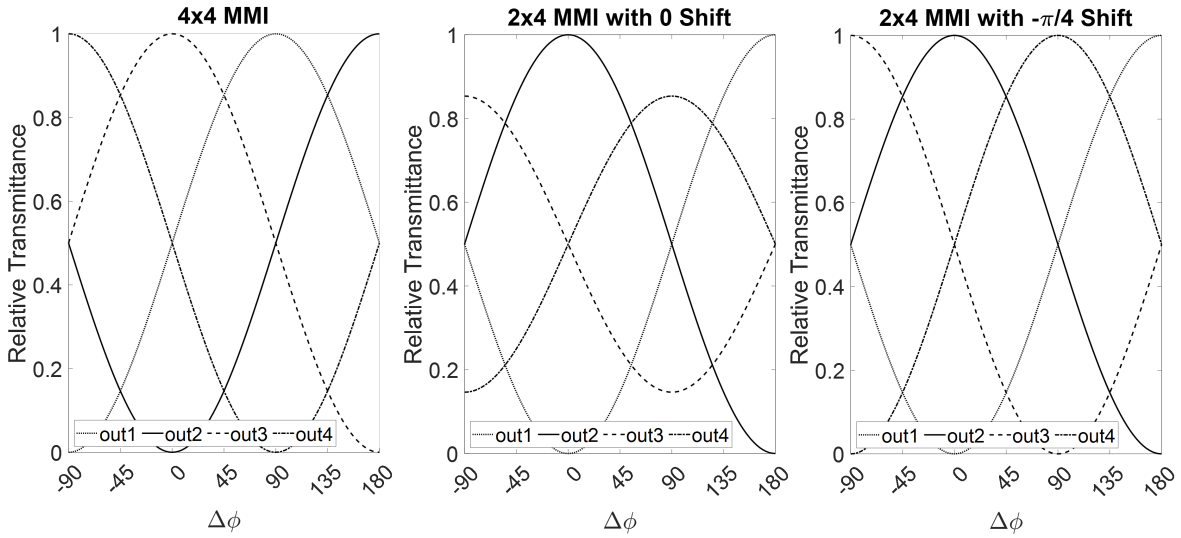


Figure 2.6: Relative transmittance of each output port for 4x4 and 2x4 variants of the 90°-hybrid

$\phi_{Q12} = -\frac{\pi}{4}$ shift can be embedded as part of the tapered section. This design has been successfully demonstrated on both InP [174] and SOI [175] platforms. Another method to reduce the footprint and improve spectral bandwidth involves sub-wavelength gratings (SWG) [176]. The gratings can be designed to both reduce the L_π for a shorter length and reduce L_π wavelength dependency for increased spectral bandwidth. Another interesting 4x4 MMI-based hybrid proposal removes the need for a separate polarization splitter (which typically has a large footprint) in dual-polarization systems by incorporating a photonic crystal in the MMI coupler that filters TE or TM modes.[177] While MMI couplers utilize the interference between several propagating modes, it is also possible to create a 90°-hybrid using the properties of free-space diffraction and interference with a star coupler [178, 24] or an arrayed waveguide grating (AWG) [179]. Driven by the need for more efficient passive network routing, star couplers fabricated with Si technology were proposed in the late 1980s [180]. While it has been demonstrated to work on silicon [178, 181] and InP platforms [24], it is not a popular option as a 90°-hybrid. The star coupler offers a compact footprint, higher fabrication tolerances, and a good spectral

bandwidth; however, it has a higher excess loss compared to other hybrid designs due to the size mismatch between the beam at the output ports and the width of the waveguide ports. The input and output waveguide size and spacing are restricted by the conditions required for the star coupler to act as a 90°-hybrid [24]. AWGs, while they have a large footprint and complex design, can be beneficial compared to an array of MMI-based 90°-hybrids. Utilizing an array of waveguides with specific phase delays in addition to free-space interference, AWGs can simultaneously act as a wavelength demultiplexer, polarization splitter, and 90°-hybrid[179]. The main drawback, similar to star couplers, is the excess loss, though there have been efforts to reduce loss in SOI and silicon nitride platforms[182]. When choosing a design for fabrication, there are several performance metrics that must be considered. For the signal to be correctly demodulated while maintaining a good signal to noise ratio (SNR), the phase error and the imbalance of the MMI outputs must both be minimized. The imbalance, which is sometimes called the peak power variation (PPV), is often characterized by the common mode rejection ratio (CMRR). Equations 2.41 - 2.44 are used to calculate the imbalance and CMRR, and Eqn. 2.46 & 2.45 can be used to convert between CMRR and imbalance. While power is used for physical measurements, the scattering parameters of the hybrid may also be used to calculate the imbalance and CMRR for the I and Q channels when running simulations. Degradation of the CMRR and imbalance may not be identical when using the input for the LO vs. the signal, so it is useful to check both cases. It has been shown that opposite imbalances and phase errors between the LO and signal ports can cancel out some of the degradation in the system performance [183]. The hybrid optical output is converted from a variation in optical power to a voltage variation when implemented in a coherent receiver assembly, so the CMRR is calculated using electrical decibels where the factor of 20 comes from the $P \propto V^2$ relationship. CMRR <-20 dBe is targeted to minimize the degradation in SNR if the hybrid was implemented in a coherent receiver module. The

Optical Interconnecting Forum (OIF) sets the signal input port $CMRR_{DC}$ < -20dBe in their implementation agreements for intradyne coherent receivers, with a LO input port $CMRR_{DC}$ < -16 dBe [184, 185].

$$Imb_I = 10\log_{10}\left(\frac{P_{Ip}}{P_{In}}\right) = 10\log_{10}\left(\frac{|S_{Ip,sig}|^2 + |S_{Ip,LO}|^2}{|S_{In,sig}|^2 + |S_{In,LO}|^2}\right) \tag{2.41}$$

$$Imb_Q = 10\log_{10}\left(\frac{P_{Qp}}{P_{Qn}}\right) = 10\log_{10}\left(\frac{|S_{Qp,sig}|^2 + |S_{Qp,LO}|^2}{|S_{Qn,sig}|^2 + |S_{Qn,LO}|^2}\right) \tag{2.42}$$

$$CMRR_I[dBe] = 20\log_{10}\left(\frac{P_{Ip}-P_{In}}{P_{Ip}+P_{In}}\right) = 20\log_{10}\left(\frac{|S_{Ip,sig}|^2+|S_{Ip,LO}|^2-|S_{In,sig}|^2-|S_{In,LO}|^2}{|S_{Ip,sig}|^2+|S_{Ip,LO}|^2+|S_{In,sig}|^2+|S_{In,LO}|^2}\right) \tag{2.43}$$

$$CMRR_Q[dBe] = 20\log_{10}\left(\frac{P_{Qp}-P_{Qn}}{P_{Qp}+P_{Qn}}\right) = 20\log_{10}\left(\frac{|S_{Qp,sig}|^2+|S_{Qp,LO}|^2-|S_{Qn,sig}|^2-|S_{Qn,LO}|^2}{|S_{Qp,sig}|^2+|S_{Qp,LO}|^2+|S_{Qn,sig}|^2+|S_{Qn,LO}|^2}\right) \tag{2.44}$$

$$CMRR_{I,Q} = 20\log_{10}\left(\frac{10^{Imb_{I,Q}/10}-1}{10^{Imb_{I,Q}/10}+1}\right) \tag{2.45}$$

$$Imb_{I,Q} = 10\log_{10}\left(\frac{1+10^{CMRR_{I,Q}/20}}{1-10^{CMRR_{I,Q}/20}}\right) \tag{2.46}$$

The insertion loss (IL) of the 90°-hybrid is less critical, but it is important to reduce optical loss to improve the power budget in optical links. Equation 2.47 can be used to calculate the insertion loss using power measurements or the scattering parameters in simulation.

$$IL = 10\log_{10}\left(\frac{P_{sig}+P_{LO}}{\sum_{n=1}^{4} P_{n,out}}\right) = 10\log_{10}\left(\frac{|S_{sig}|^2 + |S_{LO}|^2}{\sum_{n=1}^{4} |S_{n,sig}|^2 + |S_{n,LO}|^2}\right) \tag{2.47}$$

For the phase error ϕ_{err}, the phase of the hybrid outputs can be determined in simulation and used to directly calculate the error. There are a few methods which can be used to examine the phase error. Equation 2.48 - 2.50 can be used to check the the phase by examining the I and Q output port pairs are out of phase and there is a 90 °shift between

I and Q.

$$\phi_{err,I} = \phi_{Ip} - \phi_{In} - \pi \tag{2.48}$$

$$\phi_{err,Q} = \phi_{Qp} - \phi_{Qn} - \pi \tag{2.49}$$

$$\phi_{err,IQ} = \phi_{In} - \phi_{Qn} - \pi/2 \tag{2.50}$$

Another method is to use one input port as a reference and check that the other 3 ports follow the 90°-hybrid phase relation with respect to the first port using eqn 2.51

$$\phi_{err,n} = \phi_1 - \phi_n - \theta_{0,n} \tag{2.51}$$

where $\theta_{0,n} = \pi, \frac{\pi}{2}, \frac{3\pi}{2}$ with the order depending on the hybrid design. When running simulations, the output phases can be examined using both the LO and signal input ports to optimize the hybrid design. With physical devices, the phase must be estimated by examining the power from the 4 output ports while light is coupled into both input ports with a phase and/or frequency shift between the two inputs. Two primary methods for estimating the phase involve (1) an asymmetric Mach-Zehnder interferometer (AMZI) structure before the MMI inputs or (2) two coherent light sources with a small frequency offset between them to create a beat tone. For new hybrid designs, the AMZI structure is often used since it can be tested as a passive optical structure or use low speed photodiodes. For compatibility with wafer-level testing (WLT), vertical I/O optical couplers (often grating couplers as show schemtically in Fig. 2.7) are used to examine the transmission spectrum for each output across a multiple of the free-spectral range (FSR) for the AMZI, given by Eqn. 2.52 [175]. It is important to consider the sensitivity and the resolution of the instruments that will be used to enable a precise measurement of the transmission spectrum. The phase error is extracted from the transmission spectrum based on the position of the nulls using Eqn. 2.53, so a better sensitivity allows the null position to be determined with more precision. The transmission data can also be fitted

to adjust for issues related to coupling loss, reflections, wavelength dependence of the coupler, etc. to more accurately extract the transmission of the hybrid structure.

$$FSR_{1,m} = \frac{\lambda_m^2}{n_g \Delta L} \tag{2.52}$$

$$\phi_{err,n} = \frac{2\pi \Delta\lambda_{n,m}}{FSR_{1,m}} - \theta_{0,n} \quad \text{for output n=2,3,4 and measured FSR m=1,2,3, ...} \tag{2.53}$$

While AMZI structures are useful in verifying the performance of a hybrid design, they

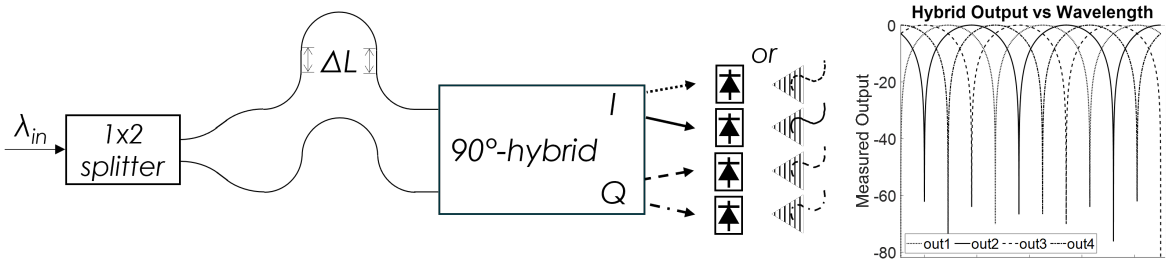


Figure 2.7: Method of phase estimation using wavelength sweep with AMZI structure to examine phase offset between 90°-hybrid output ports

cannot be used to validate the performance of full RX PICs. Calculating the phase offset between the outputs of a real device can be achieved using the beat tone between two laser inputs. A single laser can also be split into two paths with one path shifting the frequency using an acousto-optic modulator (AOM)[186]. The phase offset between the beat tone at each hybrid output is a combination of the 90°-hybrid phases and the delay mismatch in the RF path. Using phase matched cables will reduce the mismatch between paths. To calibrate out the residual RF mismatch, amplitude modulation at a specific frequency is applied on only one input, and the phases of the 4 outputs are recorded as reference points[24]. Using the two lasers to create a beat tone at the same frequency as the calibration amplitude modulation, the phase offset of the hybrid can be calculated by subtracting the calibration from the measured beat tone offsets. When verifying the performance of a coherent receiver assembly, a similar method defined by the OIF can be used[184, 185, 187]. Two optical inputs may be used simultaneously to create a beat

note at the output of the balanced and amplified I and Q channels as shown in Fig. 2.8. The phase error can be measured using the offset between the I and Q beat tones. This method requires a more complex setup with high speed photodiodes, trans-impedance amplifiers (TIA), and two optical input sources tuned with a 10s of MHz to 10 GHz offset. The phase error is the y-intercept of the fit line for I/Q offset vs. beat tone frequency[188], using the fit to account for phase mismatch due to the RF signal paths after the hybrid. To measure the phase error vs. wavelength, the input wavelengths can be adjusted, and the I/Q offset vs. beat tone frequency procedure is repeated[187]. Simulation capabilities

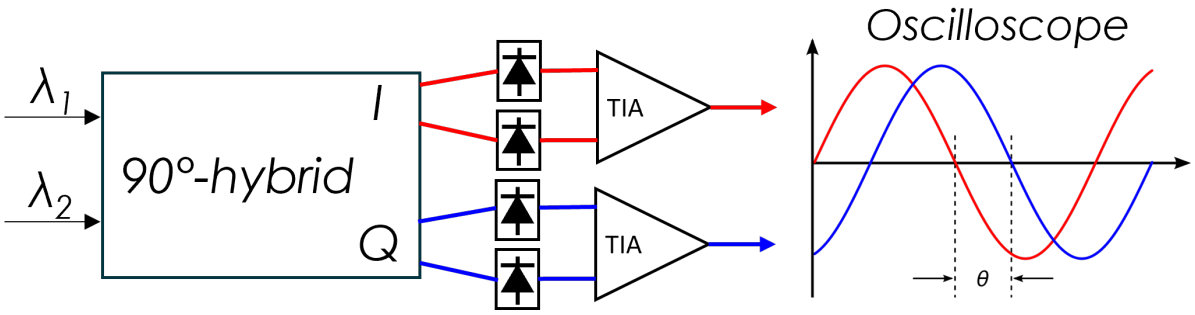


Figure 2.8: Method of phase estimation using beat tone generated from two input wavelengths to examine phase offset between I & Q outputs. Phase error is the y-intercept of θ vs beat tone frequency.

and fabrication precision have improved over the past 30 years, leading to MMI designs with low phase error and minimal imbalance over a large spectral bandwidth, with lower excess loss, and a reduced footprint. Notably, 2x2 MMI cascade style 90°-hybrids on SOI with a ring arrangement have been demonstrated with a <30x30 μm footprint [188] or a fabrication tolerant design without any active phase control [189]. Other compact 2x2 MMI-based designs have also been proposed [190] using simulation to optimize the design. While improvements in simulation provides the foundation for optimized MMI designs, the ability to accurately fabricate the design often prevents good designs from being demonstrated with their full performance [191, 192]. The MMI width is a critical parameter with low tolerance. Variations in the width on the order of 100 to 200 nm are

enough to reduce the CMRR by ≈ 10dB and increase the phase error by 3°. There have been several papers examining the optimization and fabrication tolerance analysis for MMI couplers using simulation and physical devices - see [183, 193, 194, 195, 196, 197] for a few examples.

A summary of the benefits and disadvantages of the various hybrid designs is presented below. Table 2.3 provides a useful performance comparison for the different hybrid designs, but is not an exhaustive list of all published devices.

2x2 MMI Cascade - larger spectral bandwidth, active phase tuning often required (although some devices have been shown good performance without active phase tuning) [188, 189], more components can lead to less reliability in fabrication

4x4 MMI - completely passive design, more limited in spectral bandwidth due to mode dispersion, footprint can be larger than 2x2 cascade depending on the design

2x4+2x2 MMI - larger spectral bandwidth, similar footprint to 4x4 MMI, more complex design, fabrication tolerances are low for phase shift between 2x4 and 4x4 MMIs, tapered variants [174, 175] have been demonstrated with smaller footprint and no phase shift waveguides

Star Coupler - small footprint, larger spectral bandwidth than 4x4 MMI, large excess loss, larger fabrication tolerance

AWG - large footprint (but saves space compared to an array of MMI-based dual-polarization receivers), complex design, large spectral bandwidth, small to moderate fabrication tolerance, relatively high excess loss

Table 2.3: Performance Comparison of Fabricated MMI Designs

90°-hybrid type	Footprint (μm)	$\phi_{err} < \pm 5°$ Range (nm)	CMRR (dBe)	Excess Loss (dB)	Ref.
InP 4x4 MMI	935 x 21.2	NA	≤-20	0.95	[198]
SOI 4x4 MMI	185 x 10	50+	≤-26	0.46	[199]
SOI 4x4 MMI	115.5 x 7.7	55+	≤-23	NA	[200]
InP 4x4 MMI	20 x 842	35($< \pm 7°$)	≤-25	NA	[192]
InP 4x4 MMI	20 x 845	15($< \pm 12°$)	≤-12	>1	[191]
InP 4x4 MMI	NA(? x≈1000)	50+	≤-20	NA	[201]
InP 4x4 MMI	NA(? x≈1000)	≈70	≤-20	NA(≈1)	[202]
TFLN 4x4 MMI	15.2 x 308	35+	≤-20	0.37	[203]
InP 2x4 + 2x2 MMI	18 x 379	94	≤-20	0.5(min)	[173]
InP 2x4 + 2x2 MMI	NA (? x ≈1000)	NA (50+?)	≤-20	0.6	[204]
SOI 2x2 Cascade	21.6 x 27.9	35+	≤-30	≤0.5	[188]
SOI 2x2 Cascade	185 x 185	45+	≤-28	≤0.4	[189]
SOI 2x2 Cascasde	NA(? x≈1000)	≈90	≤-20	3	[205]
InP 2x4 tapered + 2x2 MMI	18.6 x 227	35	≤-20	1.3	[174]
SOI 2x4 tapered + 2x2 MMI	12 x 107	40	≤-20	≈0.5	[175]
Silica Star Coupler	NA	NA	NA	NA	[178]
InP Star Coupler	180 x 107	NA	NA	4.4	[24]
Silica Star Coupler	400 x 780	35+	NA	6	[181]

2.3.4 Photodetectors

Optical to electrical conversion of transmitted data and other monitoring is accomplished via photodetectors in the form of photodiodes (PDs). Direct bandgap semiconductor materials can be used as the absorption layer in PDs for light with an energy above the bandgap of the material. When the light is absorbed, it generates an electron-hole pair which can be accelerated away using the electric field from a reverse biased diode, leading to photocurrent that is proportional to the power of the absorbed light. To utilize this effect, the absorption layer is placed in the depletion region of a p-n or p-i-n junction diode [73]. Responsivity (R_{PD}), the ratio of electrical current (I_{PD}) produced to incident optical power (P_{in}), is an important parameter for all PD applications. The absorption coefficient (α) and the PD length (L) determine R_d for PDs using Eqn. 2.54 to 2.56, where α depends on the material, wavelength (λ), and device design [75]. The external and internal quantum efficiencies (EQE and IQE, also labeled as η_{ext} and η_{int}) are used when examining the causes of reduced responsivity. The EQE encompasses all sources of optical and electrical inefficiencies while the IQE only covers the inefficiencies between the absorption of photons and the collection of photocurrent. The IQE is primarily related to material defects (e.g. trap, surface, or interface states) causing carrier recombination which reduces photocurrent [4]. EQE is related to several mechanisms which reduce the amount of carriers generated from light in the absorption region (P_{abs}). The coupling efficiency (η_{couple}) and reflectivity (r) control the amount of light that is able to reach the PD. To maximize the coupling into the absorption region, the incident mode size must match the PD mode and the overlap with other layers or interfaces which cause optical

loss must be minimized.

$$R_{PD} = \frac{I_{PD}}{P_{in}} = \frac{\eta_{ext} q}{h\nu} \tag{2.54}$$

$$\eta_{ext} = \frac{I_{PD}}{q}\frac{h\nu}{P_{in}} = \eta_{int}(1 - e^{-\alpha L})\eta_{couple}(1 - r) \tag{2.55}$$

$$\eta_{int} = \frac{I_{PD}}{q}\frac{h\nu}{P_{abs}} \tag{2.56}$$

For telecommunications, InGaAsP, Ge, and InGaAs are frequently used for their high absorption in the O-band and C-band wavelengths [73]. For surface-illuminated (or vertical) photodiodes (VPDs), the incident optical mode is typically a Gaussian beam, so PDs have a circular shape with a diameter that is close to the beam waist to maximize η_{couple}. Anti-reflection coatings are also applied to increase the light transmitted and improve R_d. For waveguide PDs where the light is parallel to the plane of the the absorption layer, the epitaxial layer design and the geometry of the coupling region between the input waveguide and the PD can both be optimized to improve η_{couple} by increasing the overlap between the optical mode and the absorption layer. As internet traffic has increased, higher capacity receivers with larger bandwidth PDs have been built. While VPDs are beneficial for free-space and directly fiber coupled applications, since they have relatively large alignment tolerances, there is trade-off between η_{ext} and carrier transit time limited bandwidth (f_{tr}) due to the structure of the device. Waveguide PDs (WGPDs) can overcome this trade-off by separating the light absorption and carrier transit paths [206]. When using PICs, WGPDs are the standard choice for integrating detectors with other waveguides. For applications where cost and simplicity are critical, VPDs are still advantageous due to their optical coupling tolerance and low fabrication complexity. Their is ongoing work to improve the bandwidth of VPDs for 100G data communications [207, 208, 209]. Photodiode bandwidth is limited by carrier transit time across the depletion region, the diffusion time of the carriers generated outside of the depletion region, and the RC time constant of the photodiode circuit [75]. Diffusion time

limitations are avoided by designing p-i-n PDs such that almost all of the carriers are generated in the intrinsic region. The transit time is determined by the carrier velocities and the thickness of the intrinsic region as described by Eqn. 2.57 to 2.59.

$$\tau_{tr} = \frac{d_{abs}}{\overline{v}} \tag{2.57}$$

$$\frac{1}{\overline{v}^4} = \frac{1}{2}\left(\frac{1}{v_e^4} + \frac{1}{v_h^4}\right) \tag{2.58}$$

$$f_{tr} \approx \frac{3.5\overline{v}}{2\pi d_{abs}} = \frac{3.5}{2\pi\tau_{tr}} \tag{2.59}$$

The RC time constant is determined by the effective resistance (R_{eff}) and capacitance (C_{eff}) of the photodiode circuit, which typically includes the series and parallel resistance of the diode, the load resistance of the external receiver circuits, the diode capacitance, and other RLC elements added by device packaging. Equations 2.60 & 2.61 will provide a close approximation of the device $f_{RC,3dB}$, neglecting the impact of packaging inductance.

$$\tau_{RC} = R_{eff}C_{eff} \tag{2.60}$$

$$f_{RC} = \frac{1}{2\pi\tau_{RC}} \tag{2.61}$$

Both the transit time and the RC time constant contribute to overall bandwidth (f_{3dB}) which can be approximated via Eqn. 2.62.

$$f_{3dB} = \frac{f_{tr}}{\sqrt{1 + (\frac{f_{tr}}{f_{RC}})^2}} = \frac{f_{RC}}{\sqrt{1 + (\frac{f_{RC}}{f_{tr}})^2}} \tag{2.62}$$

For high speed and low power signals, the sensitivity of PDs is also an important factor. The shot noise and thermal noise currents (i_{sh}, i_{th}) are the dominant noise sources for PDs. Eqn. 2.63 & 2.64 are used to calculate the mean squared noise currents where k_B is Boltzmann's constant.

$$< i_{sh}^2 > = 2q(I_{PD} + I_d)f_{3dB} \tag{2.63}$$

$$< i_{th}^2 > = \frac{4k_BTf_{3dB}}{R_{eff}} \tag{2.64}$$

For high bandwidth devices, reducing the dark current is key to shot noise reduction, especially for avalanche PDs (APDs) where the carrier multiplication process increases the shot noise [210, 211]. The continually increasing demand for higher speed data transmission has driven the development of more advanced PDs with improved speed and noise performance. WGPDs, APDs, uni-travelling carrier (UTC) PDs, travelling-wave (TW) PDs, metal-semiconductor-metal (MSM), and other variations on those designs have been built for improved performance in data communications systems. An overview of various designs and their improvements can be found in [4, 210, 10].

Chapter 3

Generation 1 InP O-band Coherent Receiver

As mentioned in Section 1.2, PICs made with InP have been successfully incorporated into a low power coherent link using an OPLL. The work done by Mingzhi and others showed 40 Gbaud binary phase shift keying (BPSK) operation with C-band tunable lasers [24]. For the INTREPID project, the goal is to expand on that work by demonstrating O-band QPSK operation at up to 50 Gbaud using a Costas loop based OPLL. The initial target demonstration was a single polarization 50 Gbaud QPSK receiver utilizing commerical-off-the-shelf (COTS) components to construct the OPLL. With this target, InP receiver PICs were designed, fabricated, and measured as described in the following sections. This chapter will conclude by describing some of the problems encountered when testing the PICs and the final receiver assembly which prevented the target demonstration from being achieved. These issues were addressed with modifications to the design in a second generation of PICs, which will be discussed in Chapter 4.

Parameter	Target Value
LO Optical Power	> 10 mW
Mode Suppression Ratio	> 40 dB
Phase Efficiency	$\approx$5 GHz/mA
Mode-hop free range	>25 GHz
Hybrid Phase Error	$< 10^{\circ}$
Baud Rate	50 Gbaud

Table 3.1: Performance Targets for First Generation InP Receiver

3.1 Gen. 1 PIC Design

The design for the first generation of InP coherent receivers was kept simple to reduce the number of challenges with fabrication. A sampled-grating distributed Bragg reflector (SG-DBR) laser is chosen as the local oscillator (LO) based on previous work done at UCSB by Larry Coldren and his students [212, 213, 153]. For the 90°-hybrid, there are several options, as described in Section 2.3.3, but a general interference 4×4 MMI design was chosen to avoid waveguide crossings and active tuning required for the 3-dB coupler based hybrid. The star coupler design was also avoided due to potential back reflection issues. Prior work in C-band InP PICs encountered some of these issues [24], so the 4×4 MMI was selected as the safe option. The performance targets for the receiver are shown in Table 3.1, and the full schematic with the PIC and feedback electronics for the OPLL is shown in Fig. 3.1.

3.1.1 Gen. 1 InP RX Epitaxy and Optical Modes

After the system level component types were chosen, the PIC was designed, starting with the epitaxial layers. Shamsul Arafin (now a professor at The Ohio State) and Hongwei Zhao (now at OpenLight) conducted the calculations and simulations for the layer design. Compressively strained quantum wells were designed to be used as the gain medium for the lasers due to their advantages with carrier confinement, reduction of the

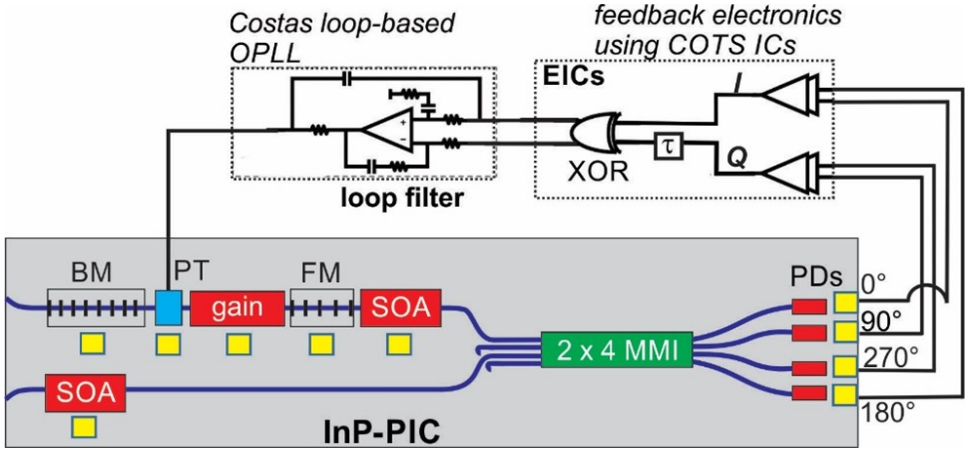


Figure 3.1: Schematic of the first generation InP coherent receiver and feedback electronics for the initial implementation of the OPLL using COTS components (data path from TIAs not shown)

valence band effective density of state through the separation of the heavy-hole/light hole degeneracy, and the decrease in the effective mass of holes. [153, 214, 215]. This improves transparency current density (N_{tr}) and differential gain ($\frac{\delta g}{\delta N}$) by improving the symmetry between the density of states in the valence and conduction bands. Figure 3.2 shows the calculated QW band structure with the photon energy and the ground state electron wavefunction for a single 4 nm well. To increase the modal gain, multiple QWs were

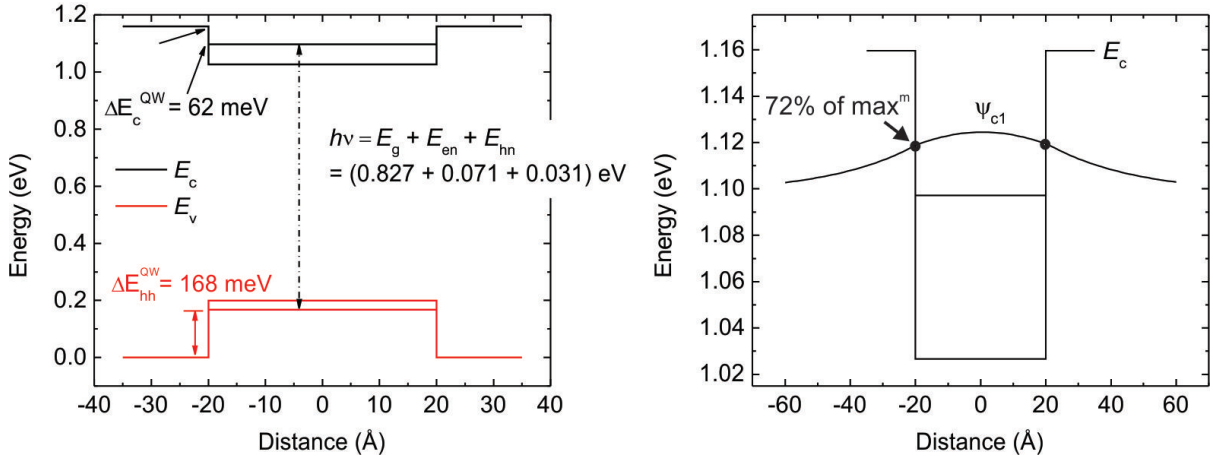


Figure 3.2: (left) Band diagram showing the photon energy and (right) electron ground state wavefunction overlaid on the QW

used. The spacing between the wells was kept to 8 nm to ensure strong wavefunction overlap, as shown in Fig. 3.3, leading to tunneling between the wells for a more even carrier distribution. For the integration of both active and passive components on the receiver, an offset quantum well platform was used. This allows the quantum wells to be selectively etched away in the passive regions of the PIC for low loss waveguides. For the optical mode, transverse and lateral confinement were achieved via a 350 nm

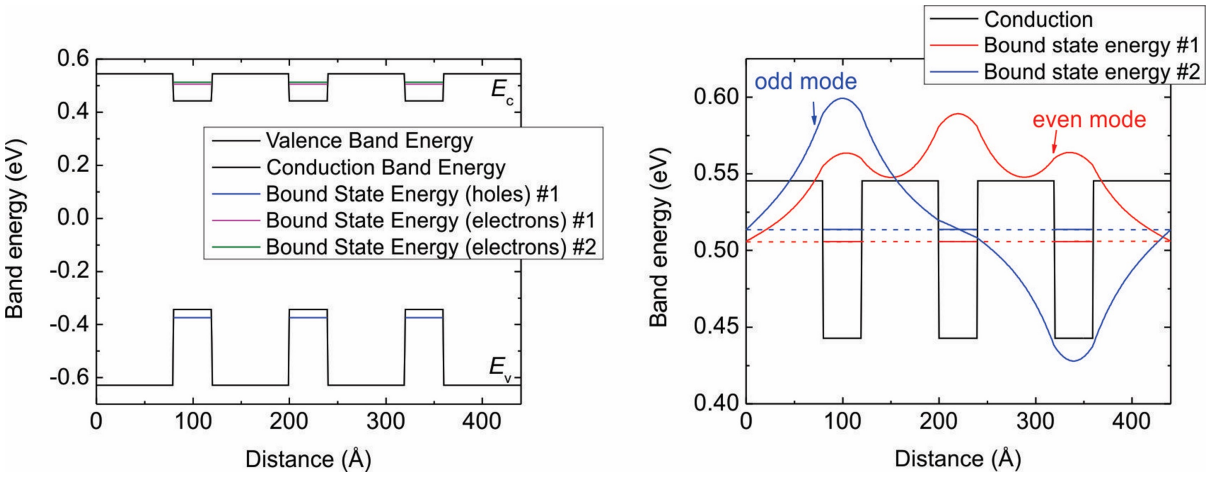


Figure 3.3: (left) Band Diagram for MQWs with carrier bound state energies and (right) electron wavefunctions overlaid on the QWs

$In_{0.78}Ga_{0.22}As_{0.44}P_{0.56}$ waveguide core and a 2.5 μm wide by 2 μm tall surface ridge. Lumerical Mode was used for all optical simulations. Figures 3.4 and 3.5 show the mode profiles for the active and passive sections. With this waveguide structure, nearly 50% of the optical mode is contained in the waveguide core, and the MQW structure has a 5% confinement factor. The heights of the p-doped ridge cladding and the n-doped cladding layers are sufficient to minimize the overlap of the optical mode with the highly doped InGaAs p-contact and the highly doped n-substrate while the doping concentration for the cladding layers is graded to reduce the optical loss caused by the dopants. In the active regions, a 25 nm $In_{0.78}Ga_{0.22}As_{0.44}P_{0.56}$ layer is also included as separate confinement heterostructure (SCH) to enhance the overlap of the optical mode

with the QWs. Unfortunately the impact of this layer on the overall band structure was not closely examined. When simulating the full band structure, this SCH layer creates a parasitic well, impeding hole injection into the QWs. See Section 4.1 for more details.

The base epitaxy was ordered from Landmark Optoelectronics Corporation based on

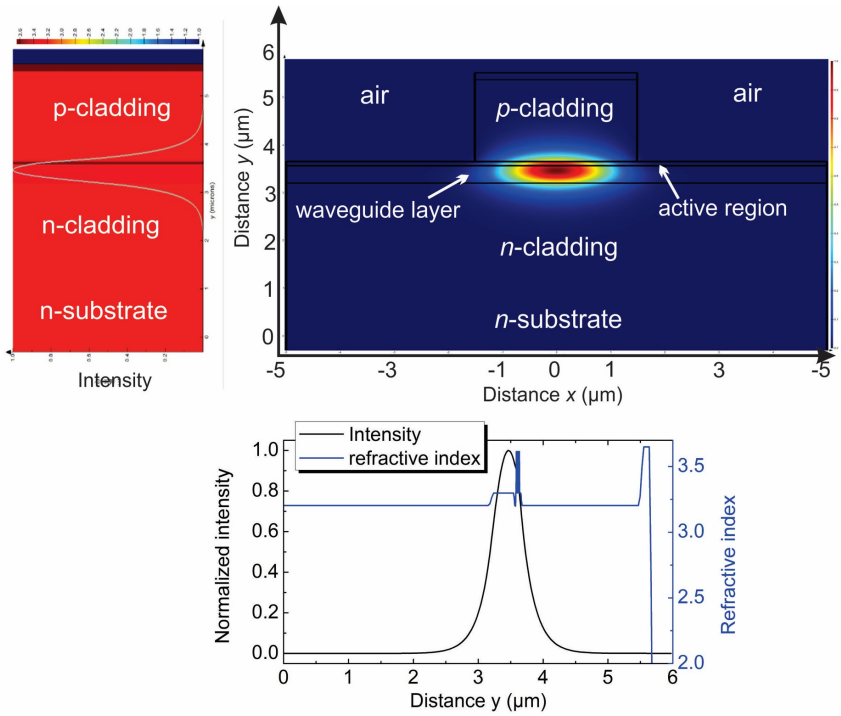


Figure 3.4: Simulation results for the optical mode in the active region

pricing and lead time. Regrowth was performed by Simone Suran Brunelli (now at Aeluma) and Lei Wang (now at Meta) using metal-organic chemical vapor deposition (MOCVD) at UCSB. The full epitaxy design is shown in Table 3.1.1.

3.1.2 Gen. 1 InP RX SG-DBR Mirrors

With the epitaxy design complete, the SG-DBR mirrors and the 90°-hybrid were designed by Thomas Meissner and myself. The SG-DBR mirrors were designed for operation centered at 1310 nm. Considerations in the design included: maximizing mode

Table 3.2: Epitaxy Design for Gen. 1 InP Receiver

#	Purpose	Material	Doping (cm^{-3})	Thickness (μm)	Tolerance ($\pm\mu$m)
0	substrate	n-InP (S)	2 to 8x10^{18}	350	25
1	n-cladding	n-InP (Si)	1x10^{18}	0.8	0.08
2	n-cladding	n-InP (Si)	8x10^{17}	0.1	0.01
3	n-cladding	n-InP (Si)	6x10^{17}	0.1	0.01
4	WG core	n-1.18μm quaternary $In_{0.78}Ga_{0.22}As_{0.44}P_{0.56}$	1x10^{17}	0.2	0.02
5	WG core	n-1.18μm quaternary $In_{0.78}Ga_{0.22}As_{0.44}P_{0.56}$	5x10^{16}	0.15	0.015
6	wet etch stop	n-InP (Si)	5x10^{16}	0.02	0.002
7	gain	quaternary QW & barrier 8x$In_{0.83}Ga_{0.17}As_{0.65}P_{0.35}$ 9x$In_{0.83}Ga_{0.17}As_{0.27}P_{0.73}$	UID	8x4nm 9x8nm 0.104	0.01
8	SCH	1.18-μm quaternary $In_{0.78}Ga_{0.22}As_{0.44}P_{0.56}$	UID	0.025	0.003
9	doping buffer	InP layer	UID	0.03	0.003
10	p-cladding buffer	P-InP (Zn) layer	5x10^{17}	0.17	0.017
↑ base epitaxy — regrown epitaxy ↓					
11	doping buffer	InP	UID	0.04	0.004
12	p-cladding	p-InP (Zn)	6x10^{17}	0.475	0.048
13	p-cladding	p-InP (Zn)	4x10^{17}	0.505	0.051
14	p-cladding	p-InP (Zn)	1x10^{18}	1.01	0.10
15	p-contact	p-$In_{0.53}Ga_{0.47}As$ (Zn)	1x10^{19}	0.1	0.01
16	protective cap	p-InP (Zn)	UID	0.5	0.05

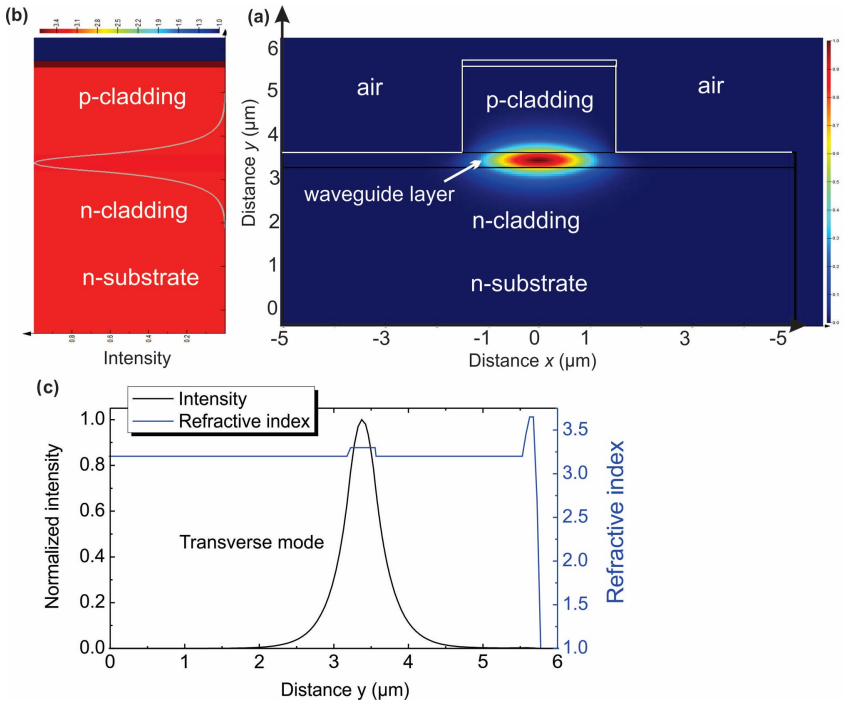


Figure 3.5: Simulation results for the optical mode in the passive region

suppression ratio (MSR) and differential efficiency (η_d) while keeping threshold carrier density (N_{th}) low by maintaining a moderate overall length (<1mm) and mean mirror reflection coefficient (R). Equations 2.9 through 2.14 were used for the basic laser design [153]. Examination of the equations shows that increasing R will increase the mirror loss (α_m) which decreases η_d and N_{th}, so a trade-off must be made between low threshold and high efficiency. For stable single mode operation, a large (typically >40 dB) mode suppression ratio (MSR) is important. Equations 2.9 through 2.15 apply to all semiconductor laser designs, but equations 3.1 through 3.8 are used specifically for SG-DBR mirrors. When designing SG-DBR gratings, there are multiple factors that must be considered to achieve (1) target reflectivity, (2) continuous tuning, and (3) high MSR.

$$\overline{\kappa} = N_{burst} L_{burst} \kappa / L_{mirror} \tag{3.1}$$

where $\overline{\kappa}$ is the average coupling constant for a SG-DBR mirror, N_{burst} is the number of grating bursts, L_{burst} is burst length, κ is the grating burst coupling coefficient, and L_{mirror} is the total mirror length which is calculated as

$$L_{mirror} = (N_{burst} - 1)Z_0 + L_{burst} \tag{3.2}$$

where Z_0 is the sampling period. Assuming a small grating perturbation and low levels of uniform loss, the distributed grating can be modeled as a discrete mirror at an effective distance (L_{eff}) for small deviations of the propagation constant (δ) from the Bragg peak.

$$L_{eff} = \frac{1}{2\overline{\kappa}} tanh(\overline{\kappa} L_{mirror}), (|\delta L_g| \ll \pi) \tag{3.3}$$

The mirror reflection coefficient (R) can be calculated using the lossless reflection coefficient (R') and L_{eff}.

$$R' = tanh^2(\kappa N_{burst} L_{burst}) \tag{3.4}$$

$$R = R'(e^{-2\alpha_i L_{eff}}) \tag{3.5}$$

The FWHM of the reflectivity peaks can be estimated using the average group index ($\overline{n_g}$), λ, and L_{eff} for low reflection magnitudes where the shape is approximately a sinc function.

$$\Delta\lambda_{FWHM} = \frac{\lambda^2}{2\overline{n_g} \cdot 2L_{eff}} \cdot \frac{3.8}{\pi} \tag{3.6}$$

The spacing between peaks is determined by the resonant length between bursts using Z_0, and the bandwidth of the vernier envelope is determined by the resonant length L_{burst} of a single burst.

$$\Delta\lambda_{peak} = \frac{\lambda^2}{2\overline{n_g} Z_0} \tag{3.7}$$

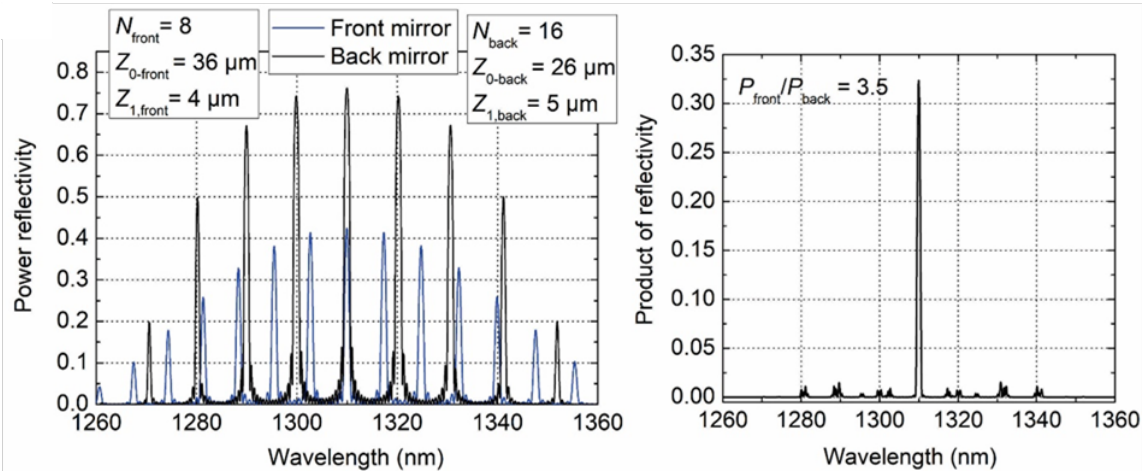
$$\Delta\lambda_{env} = \frac{\lambda^2}{2\overline{n_g} L_{burst}} \tag{3.8}$$

More details on calculations of DBR and SG-DBR gratings are discussed in [153], particularly in chapter 3, chapter 8, and Appendix 7. The equations above were used for

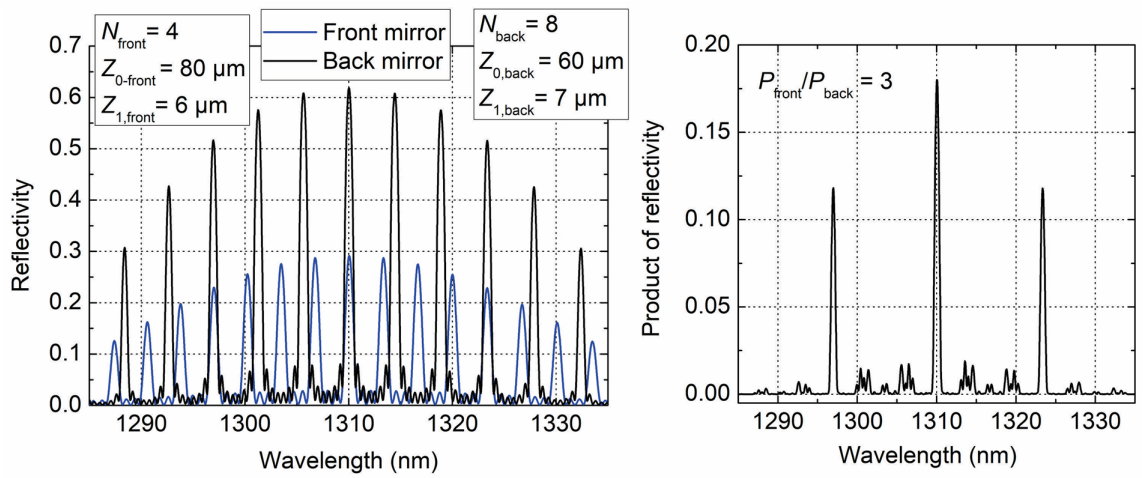
initial calculations of the SG-DBR grating reflection, but more precise calculations with scattering matrices in a custom MATLAB script were used for the final mirror design. Lumerical mode simulations were used to determine the change in the effective index (n_{eff}) with increasing etch depth. Keeping a moderate an etch depth with an aspect ratio <=1 for regrowth and for small perturbations to the optical mode, an etch depth of 80 nm into the waveguide layer (100 nm total after the 20 nm InP buffer layer) was chosen with average effective index of $n_{eff} = 3.27$ for the mode in the grating bursts. This results in $\kappa = 320$ cm^{-1} for the grating bursts. To target a higher η_d, lower mean mirror reflection values were chosen for the two designs. The primary design used R = 0.32 with $\overline{\kappa_{front}} = 40$ cm^{-1} and $\overline{\kappa_{back}} = 65$ cm^{-1} to achieve a balance between I_{th} and η_d to optimize the current needed for the target >10 mW of power. The secondary design was used on test lasers with R = 0.18, $\overline{\kappa_{front}} = 31$ cm^{-1}, and $\overline{\kappa_{back}} = 42$ cm^{-1} to examine the impact of lower R. Both designs maintained MSR >40 dB for single mode operation. The mirror reflection spectra results from MATLAB calculations for both laser designs are shown in Fig. 3.6.

3.1.3 Gen. 1 InP RX Optical Hybrid

The 90°-hybrid is the second critical component in the coherent receiver. A 4×4 general interference MMI was chosen for the hybrid. The geometry was optimized using Lumerical EME and FDTD simulations. Using Eqn. 2.22 & 2.29, a few candidate widths were chosen and the length was swept around the theoretical value. A 19.5 μm width was chosen based on providing a reasonable window of tolerance where the simulated phase error was <10° and the imbalance between the two ports for I & Q was < 1 dB as shown in Fig. 3.8. The width was also in the same range as previous work with InP 4×4 MMI couplers in Table 2.3, showing the design was aligned with past demonstrations.



(a) Primary Laser Mirror Design



(b) Secondary Test Laser Mirror Design

Figure 3.6: Calculated Reflectivity for the gen 1 InP SG-DBR front and back mirrors for (a) the primary laser design and (b) the secondary test design

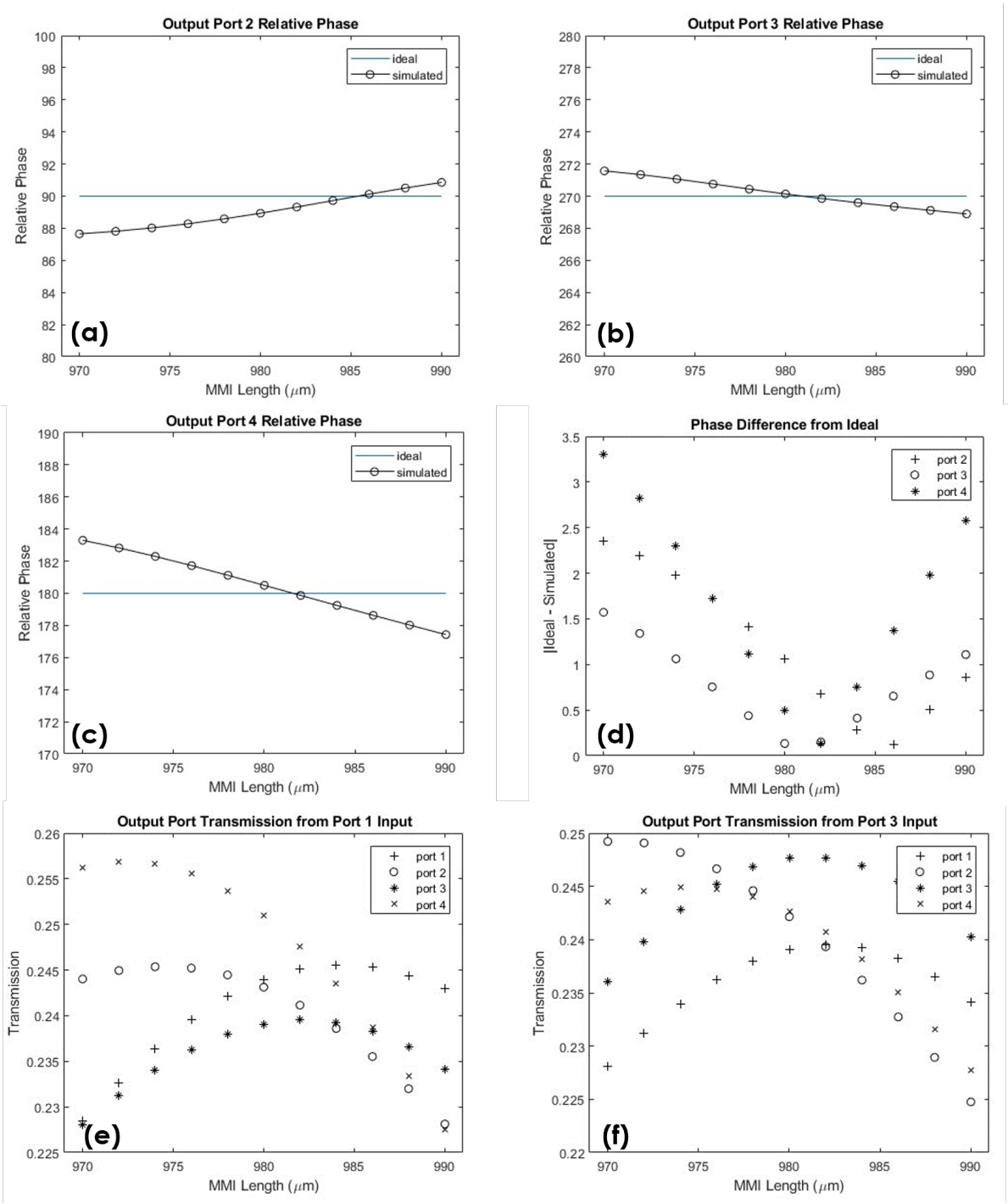


Figure 3.7: Simulation results for 19.5 μm wide 4×4 MMI with a length sweep. The (a) - (c) output port phases, (d) difference from the ideal phase, and output transmission from (e) port 1 & (f) port 2 inputs are shown.

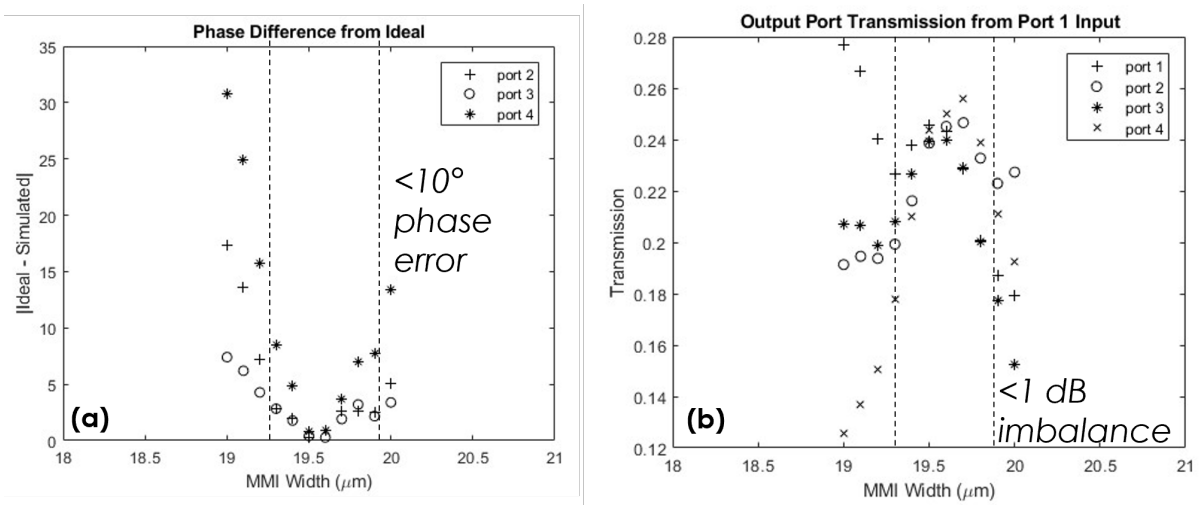


Figure 3.8: Simulation results for 984 μm long MMI width sweep to show the variation in (a) phase and (b) transmission to the output ports

Figure 3.7 shows the sweep that was used to select the 984 μm length to minimize the phase error and equalize the output port transmission. The performance variation over wavelength was also simulated as shown in Fig. 3.9. The phase error remains under 10° from 1280 to 1240 nm, with the phase error from port 4 showing the worst deviation of ±8°. The final design is shown in Fig. 3.10 which achieves equal power splitting within a 2% range over a 20 nm wavelength span and 90° phase shifts between the four output ports for demodulating the coherent signal with <5° phase error between 1290 and 1330 nm.

3.1.4 Gen. 1 InP RX High-speed Photodiodes

The high-speed p-i-n photodiodes used the same QW material as the lasers for the photon absorption. With an expected depletion width of ≈310 to 360 nm and an average dielectric constant (ϵ_r) of ≈13 [216], the parallel plate diode capacitance ($C_{\|}$) using Eqn. 3.9 is 35 to 40 fF, depending on the depletion width increase from reverse bias. A range of values are presented in Table 3.3 for the capacitance of the metal line and the bond

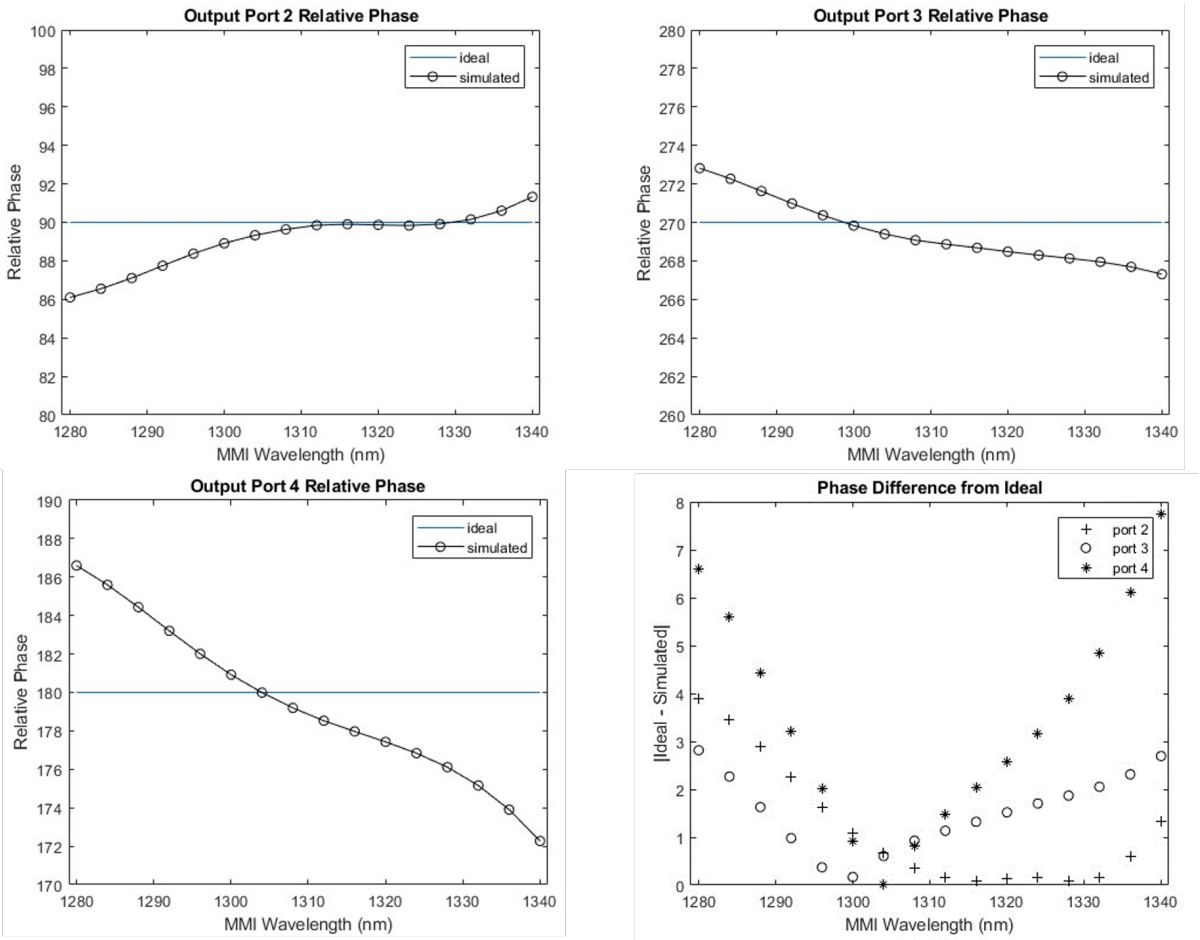


Figure 3.9: Simulation results for 19.5 × 984 μm MMI wavelength sweep, showing (a) - (c) the output port phases and (d) difference from the ideal phase

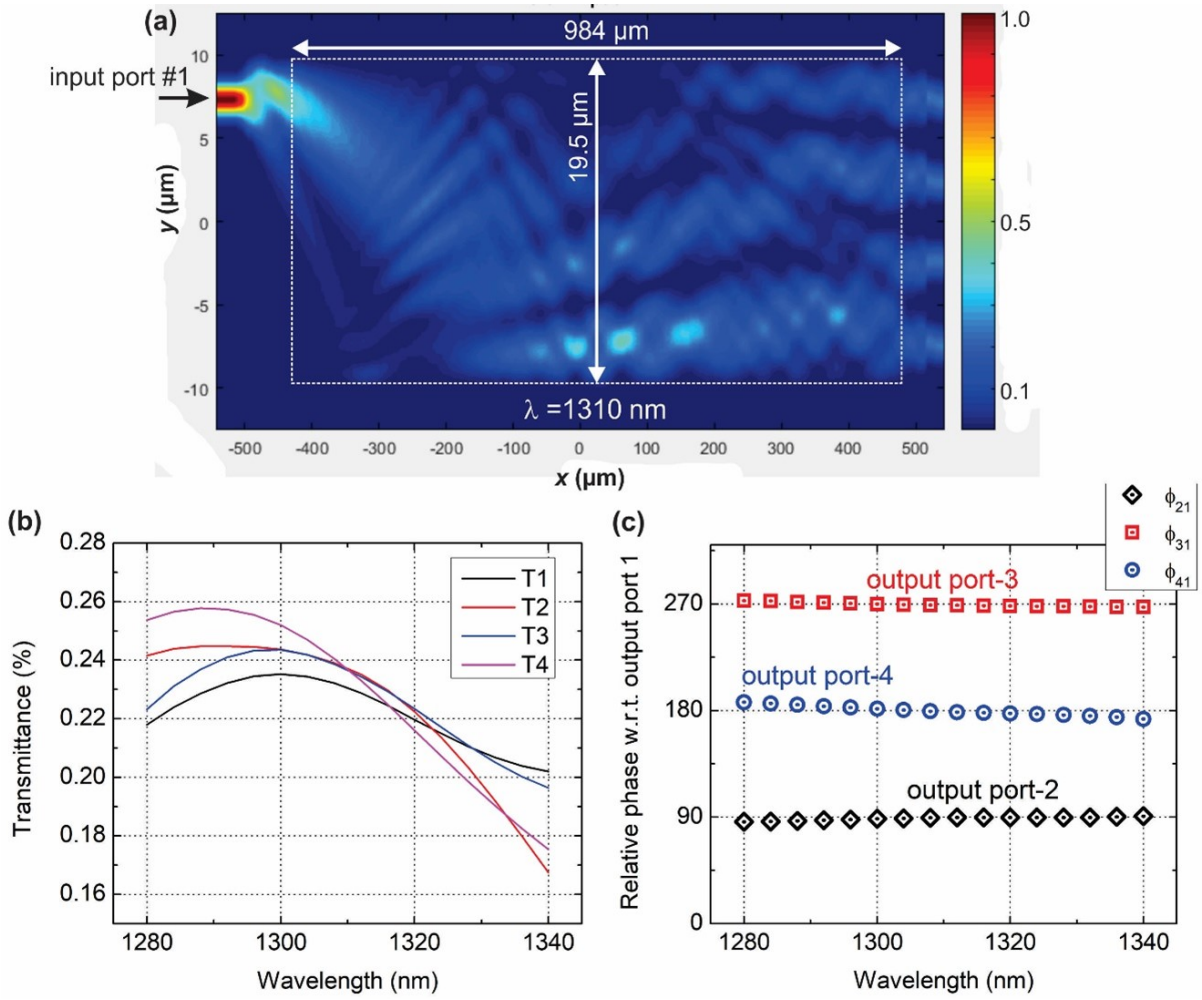


Figure 3.10: (a) Simulated power intensity profile for the 2×4 MMI, (b) transmission spectra at the four output ports, and (c) relative phase spectra for TE polarized light injected into input port #1 only.

pad to show the minimum value from only parallel plate capacitance and a larger value from added fringing capacitance using Eqn. 3.10 from [217].

$$C_{\parallel} = \epsilon_0 \epsilon_r LW/t_{cap} \tag{3.9}$$

$$C_{tot} = \epsilon_0 \epsilon_r L[(W/t_{cap}) - 1.06 + 3.31(t_{met}/t_{cap})^{0.23} + 0.73(W/t_{met})^{0.23}] \tag{3.10}$$

In Eqn. 3.9 & 3.10, L, W, t_{cap} and are the length, width, and thickness of the capacitor. The fringing capacitance also takes the metal thickness (t_{met}) into account. Eqn. 3.10 is an empirical formula that was fitted to simulation data for $0.1 < t_{met}/t_{cap} < 10$ and $0.1 <$

W/t_{cap}, and it was verified with experimental measurements [217]. Benzocyclobutene (BCB) is used as the dielectric spacer for the metal line and pad to reduce the capacitance. The f_{3dB} of the photodiode will likely be closer to 27 GHz, assuming some fringing capacitance that is lower than Eqn. 3.10 estimate. Figure 3.11 shows the top and side views for the photodiodes, and the design values are summarized in Table 3.3.

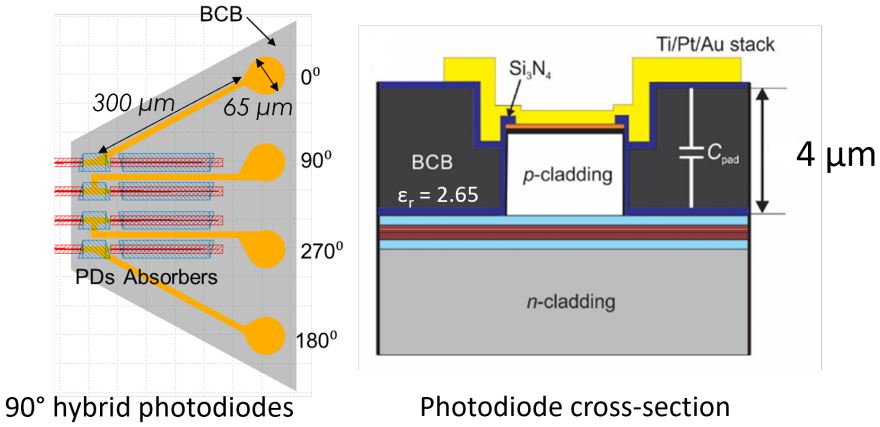


Figure 3.11: (left) Top view of the four PDs with metal lines and bond pads on top of the BCB for high speed operation. (right) Cross section view of the PD

Table 3.3: Photodiode Design Values

Description	Symbol	Value
Reverse biased diode resistance	R_D	GΩ
Biased depletion width	t_{PD}	310 nm
Photodiode size	L_{PD}, W_{PD}	45, 2.5 μm
III-V dieletric constant	ϵ_{III-V}	13
Photodiode capacitance	C_{PD}	35 - 40 fF
BCB thickness	t_{BCB}	4 μm
BCB dielectric constant	ϵ_{BCB}	2.65
Metal Thickness	t_{met}	1.5 μm
RF bond pad diameter	D_{pad}	65 μm
Parasitic capacitance from RF pads	C_{pad}	20 - 24 fF
RF trace size	L_{line}, W_{line}	300, 10 μm
Parasitic capacitance from trace	C_{line}	18 - 36 fF
Series resistance	R_s	15 Ω
RC bandwidth with R_s + 50Ω load	f_{3dB}	35 - 24 GHz

3.1.5 Gen. 1 InP RX Layout

The layout for the gen. 1 RX tile is shown in Fig. 3.12. It was created using the LibMask Photonic IC library with C++ code, and it includes 10 mask layers for the different process steps that will be explained in Section 3.2. Full receiver PICs with varying MMI widths between 19.5 and 19.75 μm were included to account for variability in the lithography and etching process. A range of widths larger than the ideal 19.5 is useful for the cases of over-development or over-etching which reduce the pattern size. To examine the 90° phase relationship between the hybrid outputs, several test structures where included with 2×1 MMIs connecting pairs of hybrid outputs to a photodiode. Standalone hybrid and 1x2 MMI structures with photodiodes at each output were added to examine the power splitting between the outputs. Three test structures using the primary and secondary SG-DBR mirror design were included with increasing gain section length from 400 to 600 μm to examine the laser performance. Characterization of the active material was planned using broad area lasers. Photodiode characterization with increasing active length and different metal trace lengths were included to examine the diode capacitance and parasitic capacitance of the metal. Lastly, circular TLM structures were added for contact resistance measurements.

3.2 Gen. 1 PIC Fabrication

The process flow for the first generation of InP coherent receivers was created using past work from UCSB students as a reference. Past dissertations by Jonathan Barton [218], Anna Pedretti [80], Jonathan Klamkin [81], Kimchau Nguyen [219], Uppiliappan Krishnamachari [220], Mingzhi Liu [24], and others provided valuable knowledge from their previous processing work. Referencing their work and following guidance from current Klamkin group students and UCSB Nanofab staff, the InP receivers were fabricated

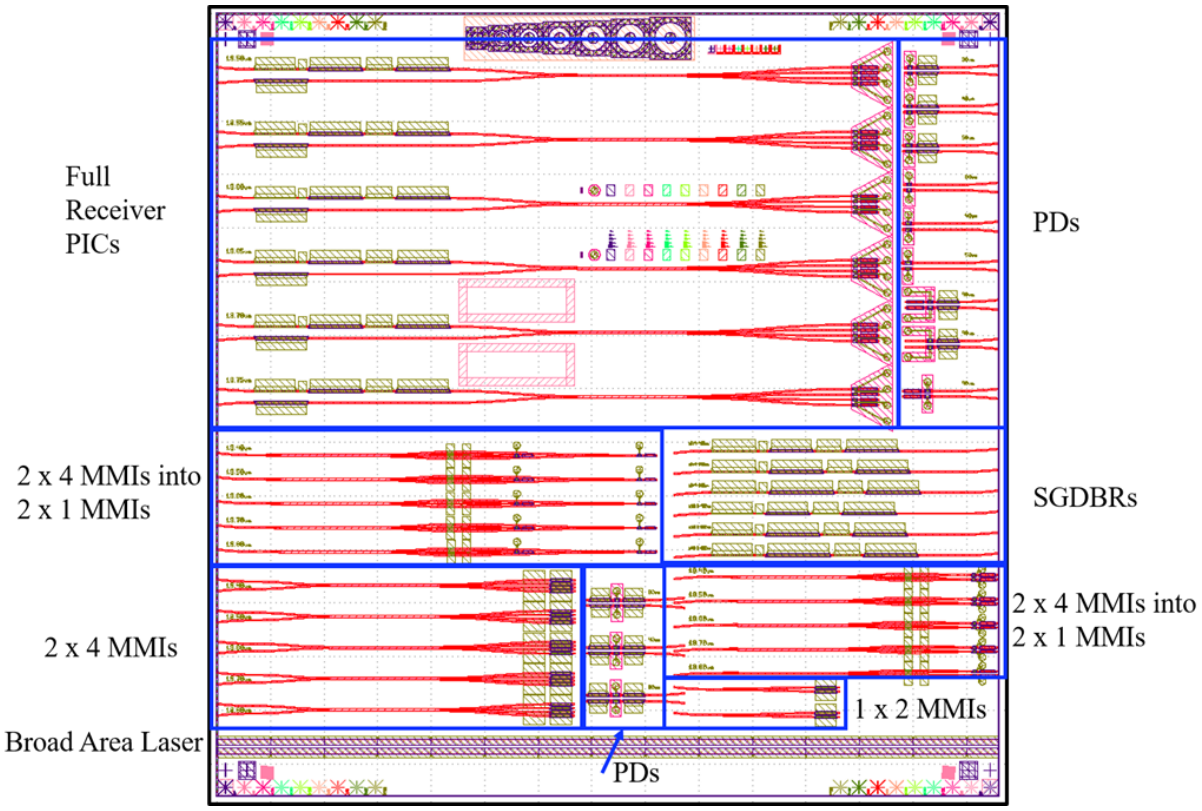


Figure 3.12: Mask Layout (7.3 x 7.3 mm) for gen. 1 InP Receiver with RX PICs and test structures

in the UCSB Nanofabrication Facility. Since the Schow group did not have any senior students with fabrication experience, hands-on processing assistance was provided by Biljana Stamenic, and detailed processing conversations were held with Demis John and Brian Thibeault in addition to meetings with Prof. Coldren. Shamsul Arafin was also involved with the fabrication for the first couple of processing steps before he left for his professor position at The Ohio State. Yujie Xia was my partner throughout the fabrication, sharing the workload and providing valuable feedback. There were a few InP quarter wafers that were processed in parallel, so Biljana, Yujie, and myself were able to work together to accelerate the process. The following subsections briefly discuss the details for each of the fabrication steps. The full process flow is included in Appendix B. Before processing began, the first step was to roughly cleave the epiwafers into quarters.

All processing was conducted using 1/4 of 2 inch InP epiwafers to provide backup pieces in case of sample damage or other processing issues.

3.2.1 Gen. 1 InP RX - Active-Passive

Since the epiwafer is using an offset QW structure, the first step is to remove the QW material in all the regions except the structures for laser gain, SOAs, or PD. This process defines the separate active and passive areas on the wafer. A silicon nitride (SiN) hard mask is deposited using plasma-enhanced chemical vapor deposition (PECVD) and patterned using lithography and dry etching to provide a "hard mask" that is impervious to the wet etching chemicals used for removing the top 200 nm of InP followed by the QWs. A well known InP etchant (HCL mixed with H_3PO_4) [221] was used to remove the top InP with a 1:3 ratio for a moderate etch rate and high selectivity of InP over InGaAsP. The high selectivity enables the InGaAsP layer to act as a strong etch stop, allowing for longer over etching times that are sometimes needed to due etching non-uniformity. The QW and barrier material are subsequently removed with a $1H_2SO_4 : 1H_2O_2 : 10H_2O$ solution for a slow etch through the quantum wells with a good selectivity of InGaAsP over InP. The 20 nm InP layer acts as an etch stop for the active material wet etching. The post-etch active areas are shown in Fig. 3.13, with the trapezoidal shapes of the SiN hard mask. This shape is chosen to provide an angled interface between the active and passive sections to prevent direct back reflection into the waveguide.

3.2.2 Gen. 1 InP RX - Grating

The gratings were defined using eletron beam lithography (EBL) with help from Bill Mitchell. The grating pattern was dry etched into a 50 nm thick SiO_2 hard mask. Dose and line width tests showed that a 300 $\mu C/cm^2$ dose with a width of 88 nm yielded

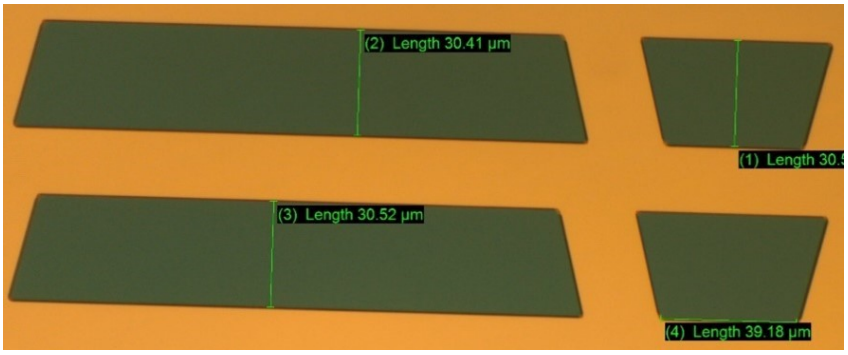


Figure 3.13: Example image of the active regions covered by the SiN hard mask

close to the desired 50% duty cycle. Based on the designs for the SG-DBR mirrors, a 100 nm target etch depth was set (80 nm into the InGaAsP waveguide layer). Initial experiments on InP test samples were run to examine the dry etching recipe for the III-V etch. A Cl_2/N_2 dry etch using the Unaxis ICP was considered, but a couple of etching tests showed roughness at the bottom of the etched gratings. Etching on a test sample using a $CH_4/H_2/Ar$ gas mixture in RIE #2 showed better results, depicted in Fig. 3.14. Imaging with a scanning electron microscope (SEM) and an atomic force microscope (AFM) are both critical methods for calibrating the grating process. While this recipe

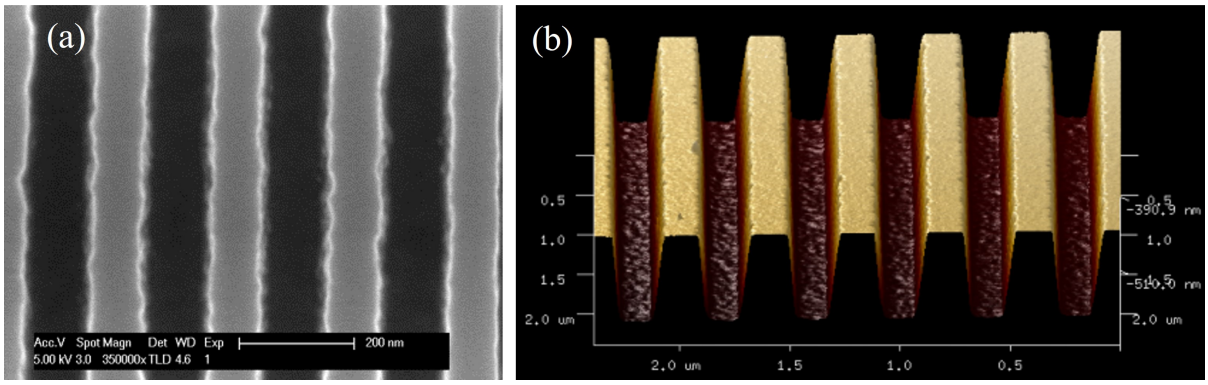


Figure 3.14: Results from RIE #2 etching showing clean gratings in (a) SEM top view and (b) 3D AFM profile

showed good results on the InP test sample, there was some roughness after etching the InP on InGaAsP for the real samples that can be seen in Fig. 3.15. This could add

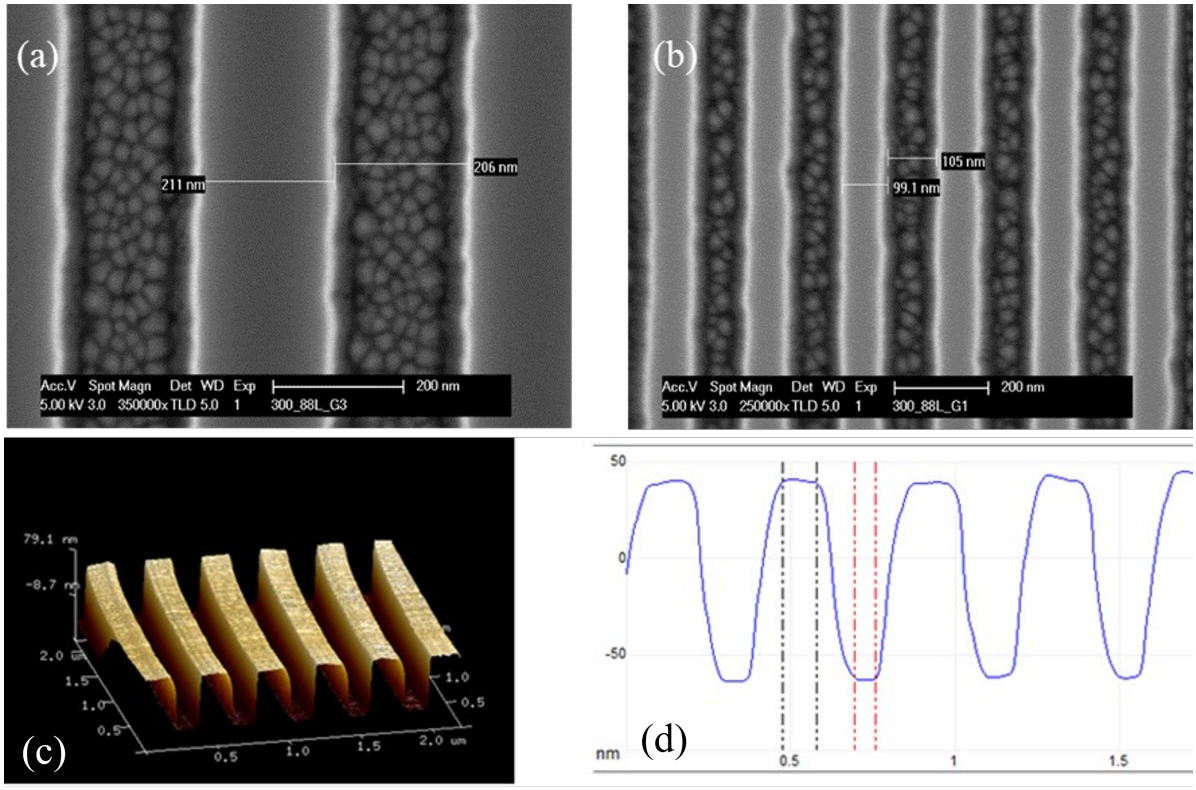


Figure 3.15: SEM images show the (a) 2nd order and (b) first order etched gratings. AFM data shows the (c) smooth 3D grating profile and the (d) ≈100 nm etch depth

some scattering loss to the lasers, but it should not impact the spectral response of the grating. The bumps are laterally smaller than the grating, and they were not easily observed on the AFM scans, indicating that they have a very shallow height. Other than the roughness, the grating etch went according to plan, with Fig. 3.16 showing a microscope image of the sampled gratings next to an active area.

3.2.3 Gen. 1 InP RX Regrowth

UCSB is fortunate to have MOCVD reactors which can be used for regrowth of various III-V materials. Due to the complexity of operating the MOCVD, there are rigorous training requirements that must be met before students are allowed to operate the MOCVD, so only a few students are able to operate the tool. Taking this into account,

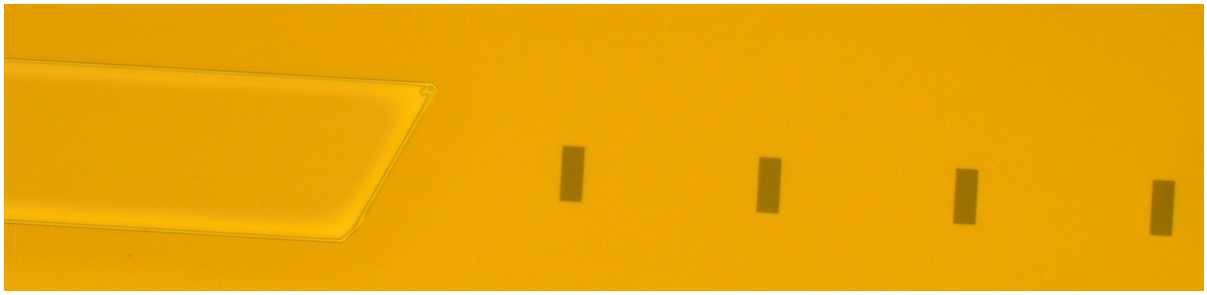


Figure 3.16: Microscope image of the etched sampled gratings

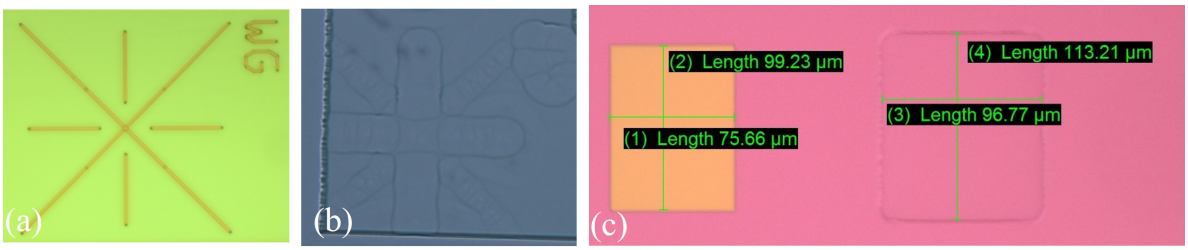


Figure 3.17: Microscope images after regrowth showing (a) the normal dimensions for an alignment mark, (b) the blooming after regrowth of an alignment mark, and (c) the blooming after regrowth of a test rectangle.

regrowth was coordinated with Simone Brunelli and Lei Wang. The regrowth added the p-InP cladding with a top p-InGaAs contact and p-InP protective cap to wafers. These layers fill the etched gratings, help define the pn junction, and provide the optical mode confinement. Sample cleaning right before regrowth is also an critical part of achieving uniform nucleation and growth. UV ozone and BHF cleaning are important to remove oxides and silicon contamination from the growth interface. Ideally, the sample has a smooth surface with vertical growth of the cladding layers, but there are often defects or abnormalities that can occur. Figure 3.17 shows a "blooming" effect that can occur when the conditions on the surface and in the chamber enhance the lateral growth. This occurred around the edges of the active passive patterns where there was a change in the surface condition. Dot defects and rough polycrystalline growth areas, seen in Fig. 3.18 are another common defect that can occur.

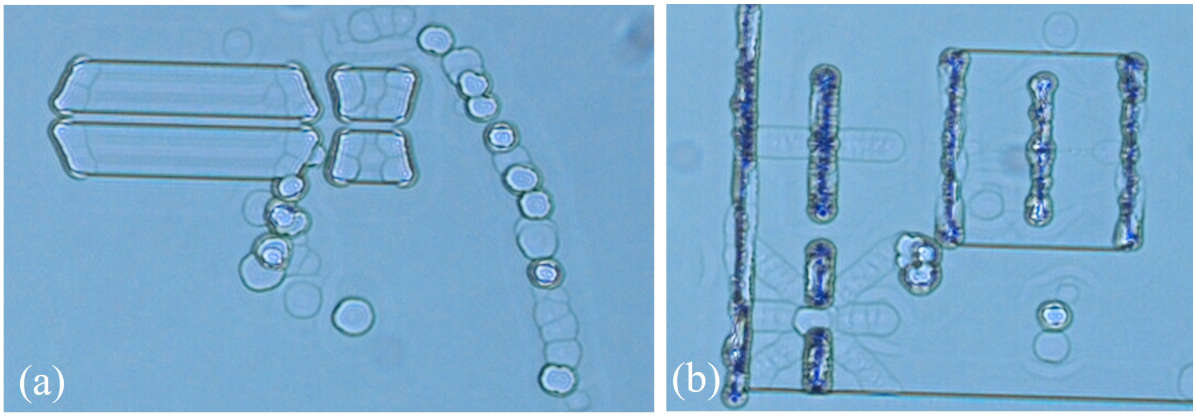


Figure 3.18: Microscope images showing (a) dot defects and (b) polycrystalline growth

3.2.4 Gen. 1 InP RX - Ridge Waveguide

For lateral optical confinement, ridges were etched through the p-InP cladding layers down to the InGaAsP waveguide core layer (for passive sections) or the InGaAsP SCH layer (for active sections). This is accomplished via a dry etch using a $Cl_2/H_2/Ar$ gas mixture at low pressure and 200°C for nearly vertical sidewalls followed an selective, anisotropic wet etch. The $1HCL : 3H_3PO_4$ wet etch helps to smooth the sidewalls and stop selectively on InGaAsP, assuming the ridges are defined parallel to the [011] crystal direction where the anisotropy of the wet etch results in vertical sidewalls. Slight deviations from the [011] crystal direction will lead to undercutting and a dovetail shaped ridge [221]. For this reason, the ridge width was increased when tilting the direction, and the angle to the [011] direction was kept below 7°. Before the wet etch, InP ridge dry etching used the Unaxis ICP with a recipe based on previous work by Parker et al at UCSB [222]. The dry etch has strong temperature dependence, so Dow Corning high vacuum grease was used to provide good thermal contact between the InP sample and the silicon carrier wafer. Care must be take to apply grease uniformly beneath InP sample. The grease cannot be easily removed with standard cleaning procedures, and it will lead to contamination if exposed to the ICP etching. Figure 3.19 shows an overview of several

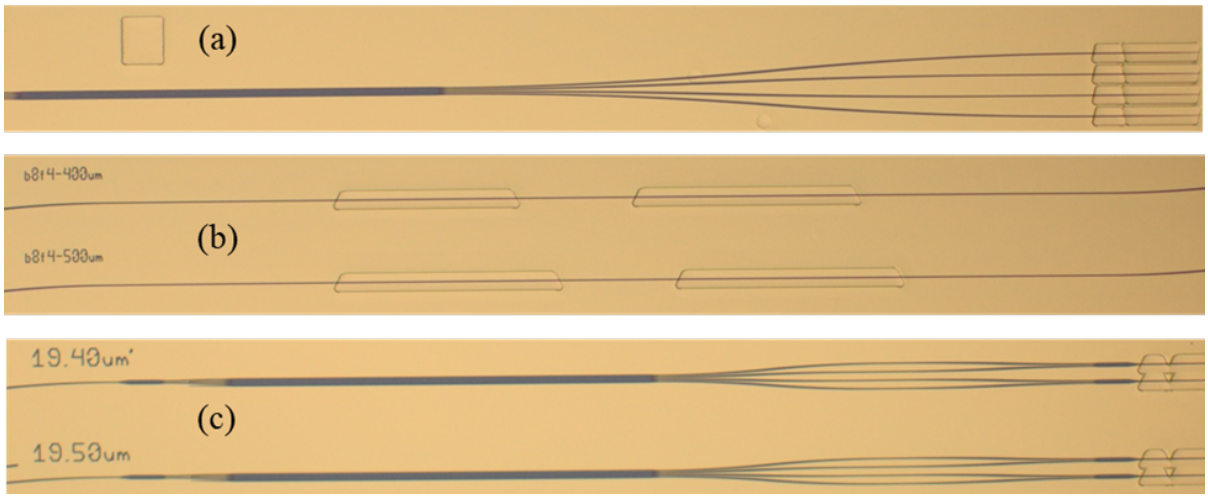


Figure 3.19: Microscope images of etched InP ridges with hard mask on ridge top for (a) the optical hybrid and PDs, (b) the test SG-DBR lasers, and (c) MMI test structures.

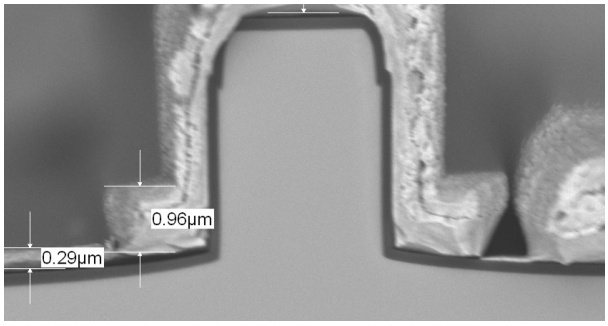


Figure 3.20: SEM image of the cross section of an etched ridge with after metal deposition on a test sample. Nearly vertical sidewalls are achieved from the dry etch.

structures after the ridge etching, and Fig. 3.20 shows the vertical sidewall from the dry etching. One important note is that the etched dimensions will deviate from the design on the mask due to the photolithography resolution limitations, sloped sidewalls of the PR, and lateral etching during the hard mask dry etch. The etched waveguide dimensions were measured to be 0.1 to 0.2 μm smaller than the design. After the ridge etching is complete, BHF is used to remove the hard mask from the ridge top, and a new hard mask is deposited via PECVD which covers the surface and sidwalls, passivating all of the exposed surfaces.

3.2.5 Gen. 1 InP RX - p-InGaAs Removal

The p-InGaAs removal step for p-isolation was conducted after waveguide patterns were defined. By removing the InP cap layer and InGaAs contact layer in waveguide areas without metal contacts, this step reduces the capacitance and current spreading of the photodiodes, and it provides isolation between metal contacts. The unique approach in this step is to do a partial exposure and develop, so a thin layer of resist still remains on the ridge top. Only the ridge top is exposed after dry etching the remaining resist, so the height of the waveguide ridge allows the lithography to be "semi-self-aligned" (SSA). The ending of the photoresist (PR) etching is marked by the appearance of rainbow patterns as the PR thickness gradient produces a color gradient from thin film interference, as seen in Fig. 3.21. When this color gradient is gone over all ridge tops, the etching

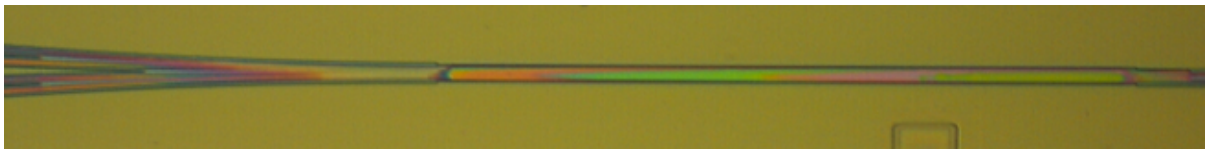


Figure 3.21: Microscope images showing rainbow patterns that appear from thin photoresist on ridge tops when SSA process in almost complete.

is complete. The subsequent dielectric etch can be done accurately on the ridge top without the need of precise alignment in lithography. This exposes the InP cap layer and the InGaAs contact layer which are removed by the same wet etch solutions used in the active passive process. When the wet etch is not complete, roughness can be seen on the tops of the MMI and ridges as shown in Fig. 3.22. Differential index contrast (DIC) microscope images can be used to view this nm-scale roughness.

3.2.6 Gen. 1 InP RX - Vias to P-contact and P-Metal

The p-via step incorporates the same SSA resist etch back technique as the isolation SSA step, but only the dielectric passivation and InP cap layer are removed. After

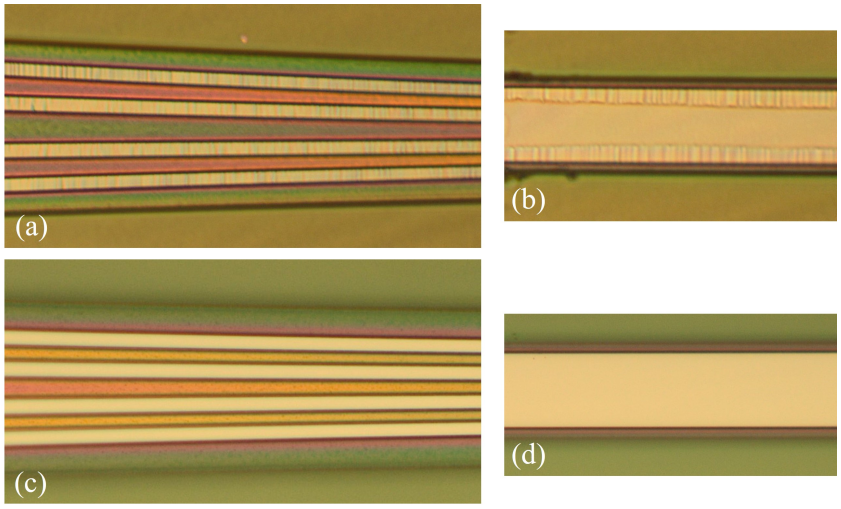
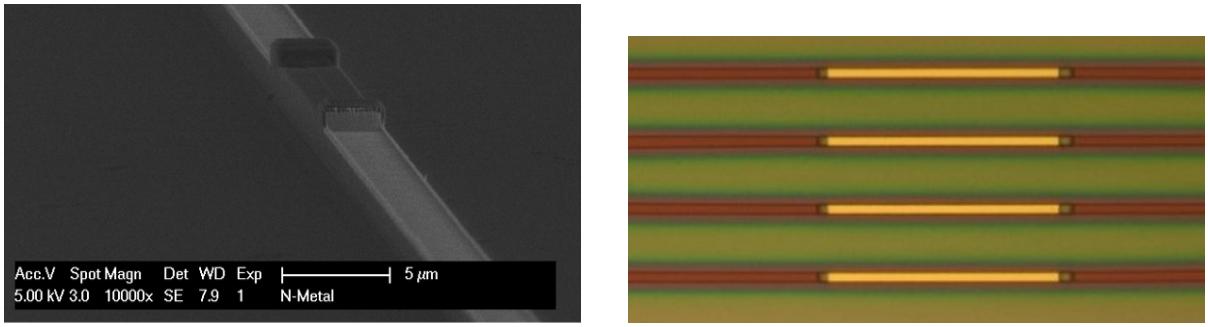


Figure 3.22: Images of the (a) ridges and (b) MMI when wet etching is incomplete, and the smooth (c) ridges and (d) MMI after the wet etch is done.

etching back the resist, the dielectric on top of the contact region was removed by dry etch, and the InP cap layer was removed by wet etch. The InGaAs contact layer was then exposed and ready for metal deposition. It is also important to leave enough space between the SSA via and SSA isolation openings. Since both of these steps use an InP wet etch, the previously etched passive region would over etch into the p-cladding if the p-via and p-InGaAs removal regions overlapped. A 3 μm buffer region is added to avoid this problem, which can be seen in Fig. 3.23. The SEM image shows a dark passive region protected by hard mask between two active sections where the bright p-metal has been deposited on top of the ridge. The taller bumps are the buffer region where the InP cap has not been etched.

An important aspect of the SSA process is the uniformity of the photoresist thickness. Since the PR is etched back in a window around the ridge, the etch time required to exposed the ridges in all structures across the wafer must be relatively uniform. There is some tolerance to over etching as the ridge sidewalls are over 2 μm tall, and the hard mask dry etching will have a small impact on laterally etching the dielectric coating the ridge



(a) (b)

Figure 3.23: Images of the ridges using (a) SEM and (b) visible microscopes, showing the metal on top of the ridges after the p-contact metal liftoff.

sidewalls. Unfortunately, this tolerance is not sufficient in cases where the PR becomes thicker over wide ridges or from the thick edge bead near the edges of the sample. The mask design did not account for this properly, so the broad area laser and the TLM structures were not able to be processed.

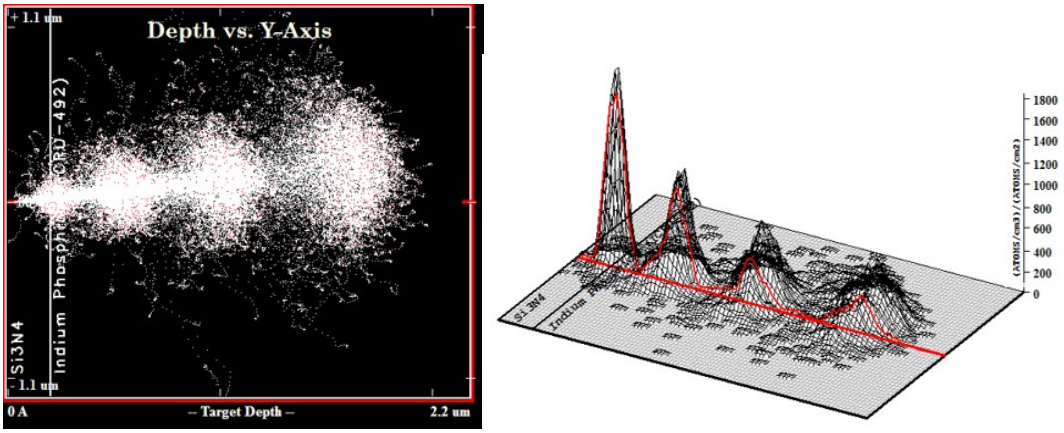
The choice to deposit the p-metal using the remaining PR after the SSA process also posed some problems with achieving a clean liftoff. Since the SSA openings are wider than the ridge, metal was deposited on the PR next to the ridge tops. There is only a small height difference between the ridge top and the adjacent PR, so a metal bridge can form between the two during deposition, making liftoff more difficult. Luckily, the (Ti/Pt/Au, 10/20/100 nm) p-metal was thin enough that a moderately aggressive spraying with solvent and gentle swabbing of the sample broke the bridges to leave a clean layer of metal on only the ridge tops. To form an ohmic contact, the sample was annealed using a rapid thermal annealer (RTA) while flowing forming gas at 415°C for 30 seconds.

3.2.7 Gen. 1 InP RX - Proton Implantation

While the removal of the p-InGaAs increases the isolation between adjacent devices, a proton (H+) implantation significantly improves the resistance, where $> 10M\Omega/\square$ can be achieved [223]. Another benefit of the implantation is the loss reduction that occurs from the positively charged hydrogen ions neutralizing the negatively charge Zn dopant ions. While high levels of Zn dopants improve the conductivity of the p-InP by increasing the hole carrier concentration, the free holes significantly increase the optical loss from inter-valence band absorption [224]. Decreasing the losses could also be achieved by reducing the doping concentration of the p-cladding itself, but there is a tradeoff between optical loss and conductivity of the p-InP material. Using a proton implant, a p-InP cladding with a higher Zn concentration can be grown for low resistance in the active regions, but the losses can be reduced in the passive sections.

To maximize loss reduction and electrical isolation, the implant was designed with several steps to cover the majority of the p-InP cladding. A 2D simulation was made using Stopping and Range of Ions in Matter (SRIM) software, and prior proton implant profiles for InP ridges were used as references [80, 81]. The results shown in Fig. 3.24 were made by running the SRIM simulation using ≈10000 ions for each energy step. The 4 step implant covers a majority of the p-cladding. A 7° implantation angle was used to avoid ion channeling effects that can increase the implant depth. Figure 3.24 also showns the lateral spread of the ions increases at higher implant depths from scattering. The implant recipe, shown in Table 3.4, has increasing doses to account for the lateral spread of the ions with increasing depth.

Simulations were also conducted to ensure that the thick photoresist mask was sufficient to block the implant from reaching the active ridges. One minor issue with the implant process was the difficulty of completely removing the protective PR. The implant



(a) (b)

Figure 3.24: SRIM simulation results showing (a) a 2D scatter plot of the implanted ions and (b) a 3D plot of the normalized ion density.

causes heating and can break the some of the chemical bonds of the photoresist material, leading to hardened PR that is challenging to remove with standard solvent cleaning and O_2 plasma treatment. More than 10 minutes of cleaning was needed using a Gasonics down stream O_2 plasma ashing tool at 200 to 250°C to remove all of the hardened residue.

Table 3.4: Implant Energies and Dose for Proton Implantation

Step ⇒	1	2	3	4
Energy (keV)	35	85	145	215
Dose (cm^{-2})	4.5×10^{13}	6.0×10^{13}	8.0×10^{13}	10.0×10^{13}

3.2.8 Gen. 1 InP RX - BCB Area

As mentioned in Section 3.1.4, BCB is used for reducing the capacitance of the metal line and pads because of its low dielectric constant. While BCB is useful for capacitance reduction, it must be processed carefully to avoid issues with adhesion, deformation, and cracking. The process used for the BCB was originally developed by Brian Thibeault. Photo-BCB 4024-40 was patterned, acting as a negative resist, on top of a SiN adhesion layer. After development, the BCB undergoes a curing process at 250°C to remove re-

maining solvents and strengthen the BCB. During the curing, the BCB shrinks, reducing the thickness by a few hundred nm and adding stress to the edges of the pattern. It is important to have good adhesion to the BCB to avoid peeling and rough interfaces after curing. Figure 3.25 shows a few examples of these problems on a test sample where BCB was patterned directly on the InP. With a SiN layer underneath, the BCB adhesion is better, as shown in Fig. 3.26. When the curing is complete, a 100 nm layer of SiN is deposited with PECVD to provide good adhesion between the BCB and the pad metal.

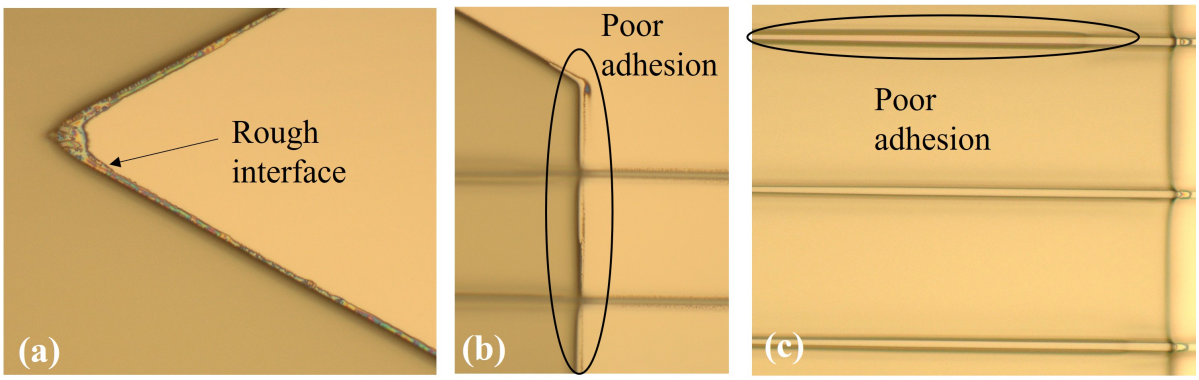


Figure 3.25: Microscope images of on a test sample where BCB was patterned directly on the InP surface. Poor adhesion between BCB and InP leads to (a) rough interfaces and poor adhesion to the (b) wafer surface and (c) ridge sidewalls

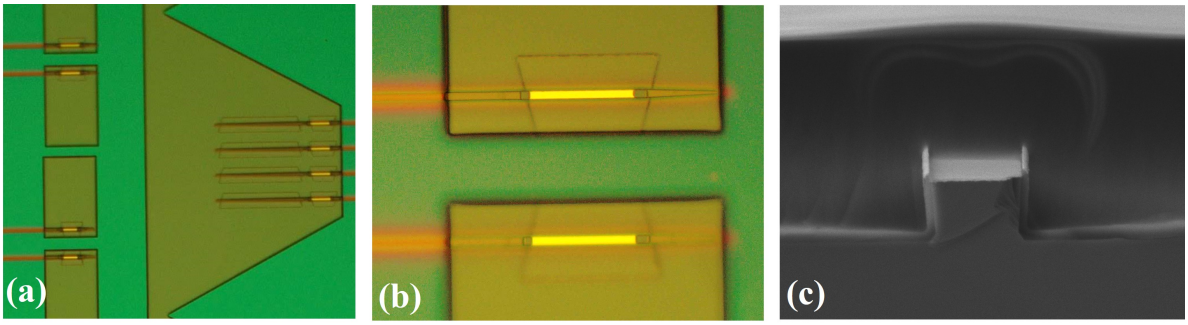


Figure 3.26: Microscope images of an epiwafer sample with the BCB areas over (a) the I/Q PDs and test PDs and (b) a close view of the PDs under the BCB. An SEM image of (c) a cleaved test sample with good adhesion of the BCB to the SiN.

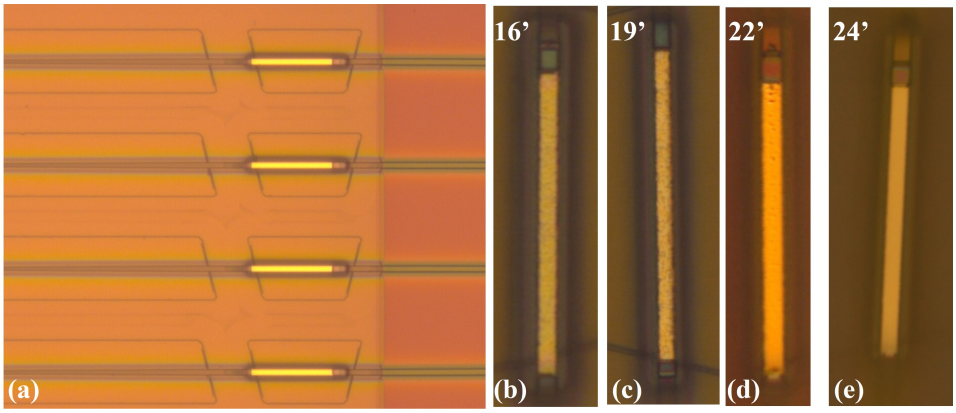


Figure 3.27: Microscope images of (a) the developed BCB via pattern over the I/Q PDs and (b) - (e) the surface of the PD ridge after 16 to 24 minutes of BCB etching.

3.2.9 Gen. 1 InP RX - Vias through BCB

To expose the ridge tops of the photodiodes, vias are etched first through the 100 nm of SiN on top of the BCB then through the 2.5 to 3.0 μm of BCB above the ridge. This etch also uses the ridge height to self-align the etch. The BCB etch is roughly timed using a measured etch rate of ≈100 nm/min from a test sample with larger BCB areas that were scanned with a Dektak profilometer; however, this etch rate will not be exact due to etch rate dependency on exposed area and via aspect ratio. Careful visual inspection of the samples was used to determine the stopping point for the etch. Figure 3.27 shows the progression of the surface texture when the etching is close to done. For the first half of the etching, the BCB is still too thick above the ridge for to see any obvious visual changes, but the etching creates some surface roughness in the BCB that becomes visible when the BCB is thin above the ridge.

Over etching on the sides of the ridge was a concern due to the capacitance it would add and the potential for the BCB to peel away from the ridges. Increased BCB etching near the sidewall due to enhanced ion bombardment effects can worsen this problem [225]. The BCB profile was not completely planarized over the ridge top, so the BCB adjacent

to the ridge must be etched at least a few 100 nm below the ridge top, assuming a uniform vertical etch across the entire opening. Figure 3.28(a) shows a confocal microscope scan where there is an obvious trench from enhanced BCB etching next to the ridge, and the bumps in the BCB from imperfect planarization are visible in Fig. 3.28(b).

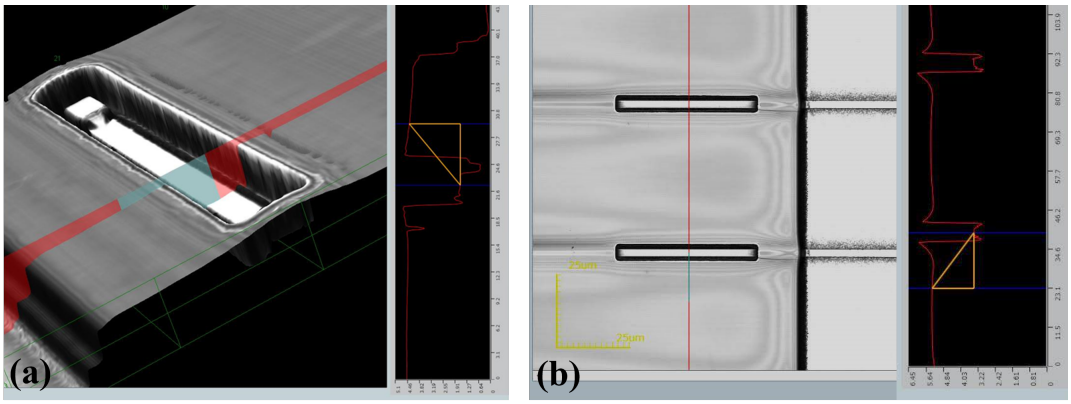


Figure 3.28: Laser confocal microscope images and height profiles of (a) a BCB via after etching and (b) the area around two BCB vias.

To further investigate the etching profile, test samples where cleaved after the etch and inspected with an SEM. The concave shape of the etch next to the ridge, seen in Fig. 3.29, indicates that the etching is enhanced near the ridge, since the original shape of the BCB over the ridge was convex. While delamination of the BCB from the ridge is a potential issue for samples with poor adhesion (from no sidewall SiN) based on Fig. 3.29 (b), the test sample with SiN does not exhibit peeling issues. The sloped/bowed sidewalls of the etched BCB do present a problem for the future pad metal deposition. Rotating metal deposition at a high tilt angle was required to create a connection up the sidewalls to the top of the BCB.

3.2.10 Gen. 1 InP RX - SiN Etch to P-contact Metal

After the via through the BCB, 100 nm of SiN was deposited to cover any small gaps where the BCB adhesion was poor, to protect the exposed BCB, and to aid with metal

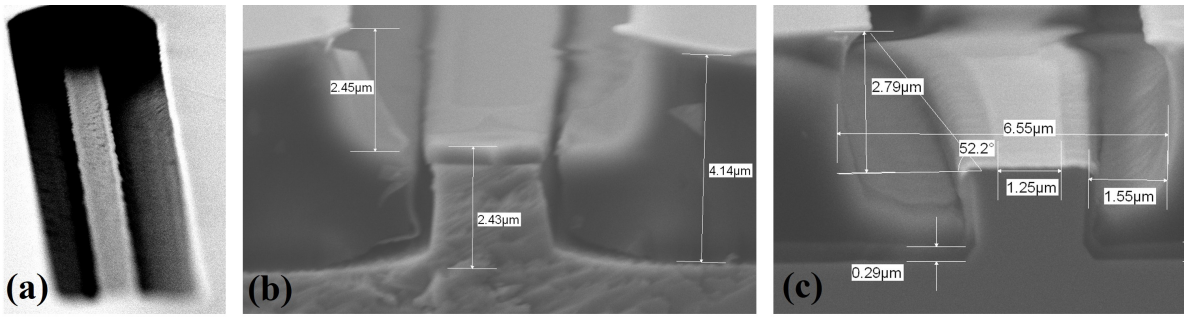


Figure 3.29: SEM images of test samples showing (a) an angled view of an etched BCB via, (b) a cross section where BCB adhesion was poor, and (c) a cross section with good BCB adhesion.

adhesion inside the via. This SiN must be removed from the ridge tops to allow the pad metal to contact the previously deposited p-contact metal. The nitride over the laser ridge tops and inside the BCB via were etched together, but a large SSA window was used for the laser ridges compared while a narrow 1.5 to 2.0 μm direct via was used for the PDs. Figure 3.30 shows images of the ridges before and after the etch.

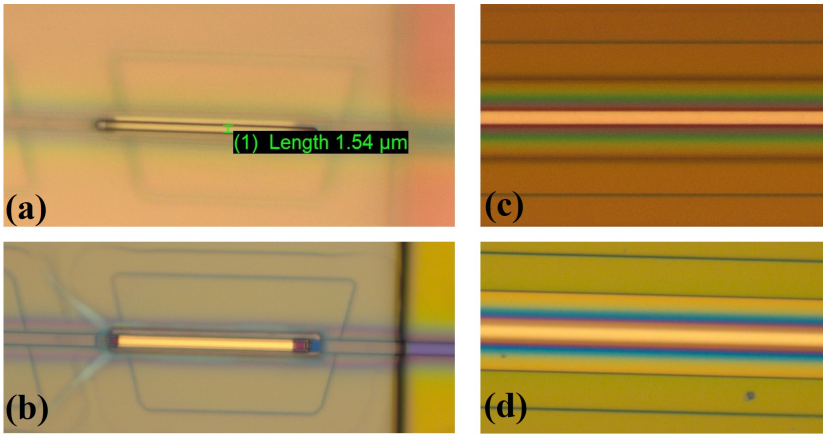


Figure 3.30: Microscope images with patterned PR before the SiN etch and without PR after the etch is completed, depicting the (a)-(b) direct PD via and the (c)-(d) laser ridge SSA windows

The laser ridges have 200 nm of SiN compared to the 100 nm over the PDs, but the etch rate is slower for the PDs due to the aspect ratio of the narrow via. In both cases, the color contrast is not visibly apparent, so the film thickness of a larger test structure

was monitored until all the SiN was removed. An additional 1 to 2 minutes of etching was added at the end to ensure all the SiN was removed. The SSA windows around the laser ridges did not protect the SiN at the base of the ridge through the whole etching process, leading to a partial SiN etch around the ridge that can be seen in Fig. 3.30 (d). Since there is still SiN remaining and the increased capacitance is not a concern for low speed devices, this did not have an negative impact. A minor issue that did cause some issues with the following pad metal step were cracks, seen in Fig. 3.30 (b), that appeared next to the vias through the BCB after cleaning the samples. This issue is likely caused by thermal stress and oxidation of the BCB from high temperature downstream O_2 plasma cleaning.

3.2.11 Gen. 1 InP RX - Pad Metal

A bilayer liftoff process using photoresist on top of polydimethylglutarimide (PMGI) was utilized for the pad metal. There were issues with bubbles and cracking of the PMGI that needed to be mitigated to avoid shorting adjacent devices together. Most of the bubbles, shown in Fig. 3.31, occurred in the regions around the BCB after spinning and baking the PMGI. These bubbles often expanded and occasionally resulted in cracks after spinning and baking the top photoresist. These bubbles can result from trapped gas or from the PMGI peeling away from the resist as the solvents evaporate between spinning and baking [226].

A few different versions of the PMGI spinning and backing recipe were tested with varying degrees of improvement. The recipe shown in Appendix B was used on the real samples with acceptable but not ideal results. The bubbles over the BCB via openings were eliminated, but they were not able to be completely eliminated in the corners between BCB trapezoids and at the edge where the waveguides enter the BCB. Careful

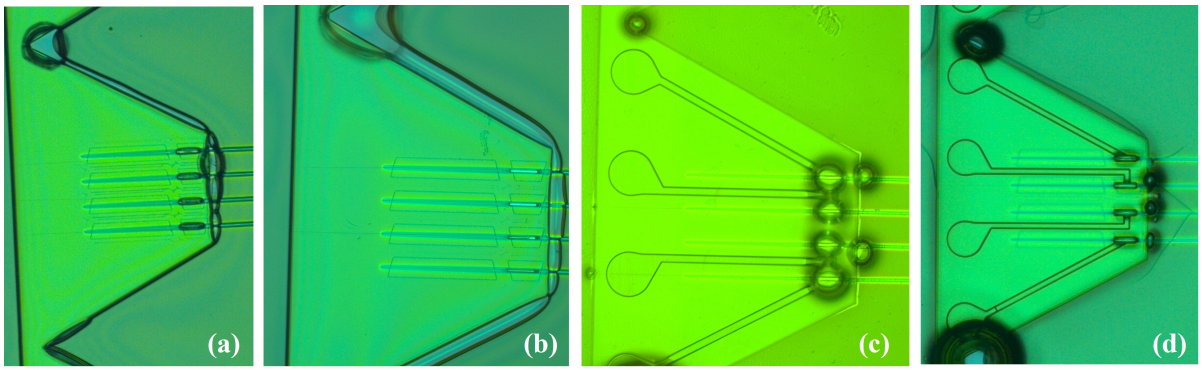


Figure 3.31: Bubbles appeared in the PMGI after (a) - (b) initial baking which can interfere with the (c) - (d) pad metal patterns after development

examination of the sample after development was used to determine whether the impact to the yield was minimal enough to proceed.

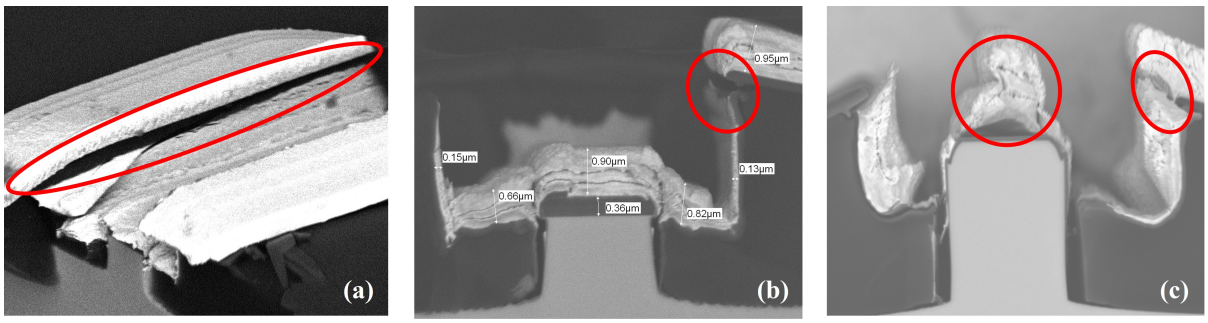


Figure 3.32: SEM images from two different metal deposition tests. (a) - (b) A low angle deposition test with ≈1/0.15μm of surface/sidewall metal leaves a gap. (c) A high angle deposition without continuous rotation leads to shadowing from surface metal.

Multiple pad metal deposition tests were also conducted on test samples which were subsequently cleaved and inspected with SEM. Initial tests used a low (30° to 45° deposition angle. The sidewall coverage was inadequate, as shown in Fig. 3.32 (a),(b). The deposition angle was increased to 60°and periodically rotated between two orientations where the BCB sidewalls on the left/right were facing the deposition source, attempting to increase the sidewall thickness. This resulted in shadowing from the metal accumulation on the ridge between the sidewalls which can be seen in Fig. 3.32(c). The final pad

metal deposition recipe used a (50° to 60° angle with continuous rotation of the sample to avoid shadowing. A thicker metal layer was also deposited to ensure the the surface metal made contact with the BCB sidewall metal.

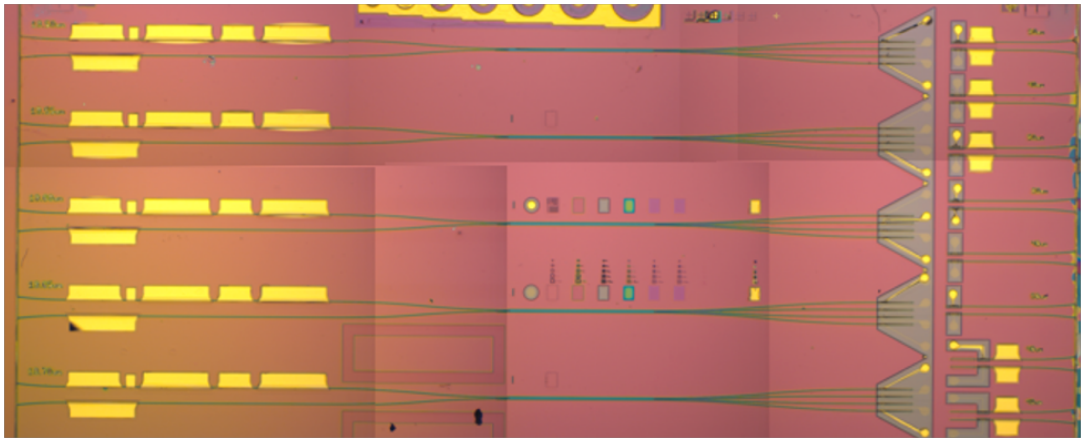


Figure 3.33: The first real sample showed poor adhesion of the PD pads after metal liftoff.

The deposition on the first real sample unfortunately had poor adhesion between the metal and the SiN on the BCB, leading a large fraction of the PD pads lifting off, shown in Fig. 3.33. For the second sample, depicted in Fig. 3.34, the yield was much better. The adhesion metal was changed from Ti to Cr and a 5" dilute BHF dip was added immeadiately before deposition to remove surface oxidation that can weaken the adhesion.

3.2.12 Gen. 1 InP RX - Thinning, Backside Metal, and Cleaving

Wafer thinning is required to achieve a smooth facet for low scattering and reflection when coupling light to/from the devices. For mechanical support, the InP sample is bonded to a silicon carrier piece top side down with Crystalbond mounting wax. Fine grit aluminum oxide lapping paper is used to abrasively remove the InP substrate until

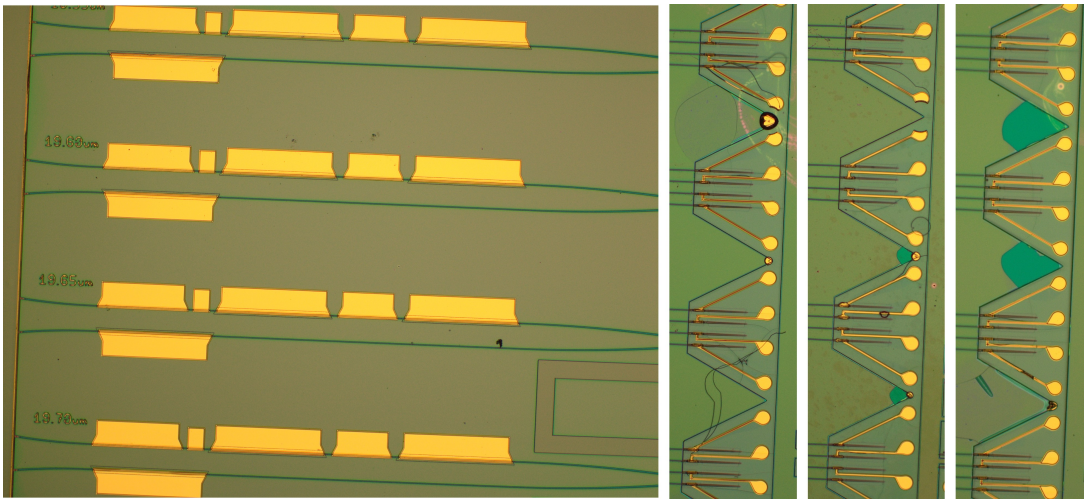


Figure 3.34: The chrome adhesion metal was much better on the second sample.

the thickness is between 125 and 150 μm. The details of this process are shown in Appendix B, Fig. B.16. Backside metal is a simple top down deposition of 20/40/500 nm Ti/Pt/Au. To prepare the devices from testing the sample was manually cleaved into bars and soldered to aluminum nitride (AlN) subcarriers coated with Au.

3.3 Gen. 1 PIC Characterization

Initial testing was conducted using DC needle probes to examine the current-voltage (I-V) characteristics of the devices. The active regions were measured for multiple PICs lasers, test lasers, and high speed photodiodes. The I-V characteristics for each of the 500-μm long PIC gain and SOAs sections, labeled as 19.50 to 19.75 μm based on the width of the MMI, were measured as shown in Fig. 3.35. The turn-on voltage is $\approx$1.05 V with a series resistance of $\approx$8.5 Ω. All the PIC lasers share the same design, so the variance in the data is caused by fabrication. I-V measurements for the stand-alone SG-DBR lasers yielded similar results. The SG-DBR laser variations have two mirror designs, labeled b8f4 and b16f8, with 3 different gain section lengths. The 400-μm and 500-μm variations

showed similar I-V measurements between the two mirror designs. Gain section length, not the mirror design, should impact the I-V curve. The disagreement between the two 600-μm lasers is due to a fabrication defect on the b16f8 600-μm laser. Measurements for the photodiodes on each of the PICs showed that the photodiodes exhibit a higher turn-on voltage and a series resistance of $\approx$15.5 Ω. Due to the smaller size of the PDs, the resistance from the contact and the p-cladding are expected increase.

Another DC probe was added for injecting current into the gain section while monitoring the photocurrent using the front booster SOA as a photodiode. If all the light is absorbed in the SOA, the laser power is approximately 0.9 A/W multiplied by the SOA current. The measurements show that the laser threshold is $\approx$55 mA for testing the lasers without temperature regulation or mirror tuning. This threshold is higher than expected, and the increase is attributed to an error in the epitaxial design, mentioned in Section 3.1.1. Thermal roll-off is evident in Fig. 3.36. Kinks in the graph indicate mode transition due to the lack of tuning and thermal control. From the test structure measurements, the b16f8 500-μm design shows the best performance. This design is the one that was implemented in all of the PIC lasers. Three of the PIC lasers show good uniformity while the lasers on the 19.55 μm and 19.50 μm PICs show more roll-off from heating. Variance in the contact resistance, the low uniformity of the contact across length of the gain section, or increased non-radiative recombination from material defects could lead to more heating. The increase in the output power is also examined while sweeping the booster SOA bias, using the photocurrent from one of the high speed PDs after the 90° hybrid. When the SOA is at a low current, it is absorbing the light from the SG-DBR before it can reach the photodiode. As the SOA current is increased from 7 mA to 22 mA, the response of the PD increases by a more than a factor of 10, showing that the SOA has transitioned from absorbing to amplifying the light from the SG-DBR.

Later testing used a DC probe card after the devices had been wirebonded to the

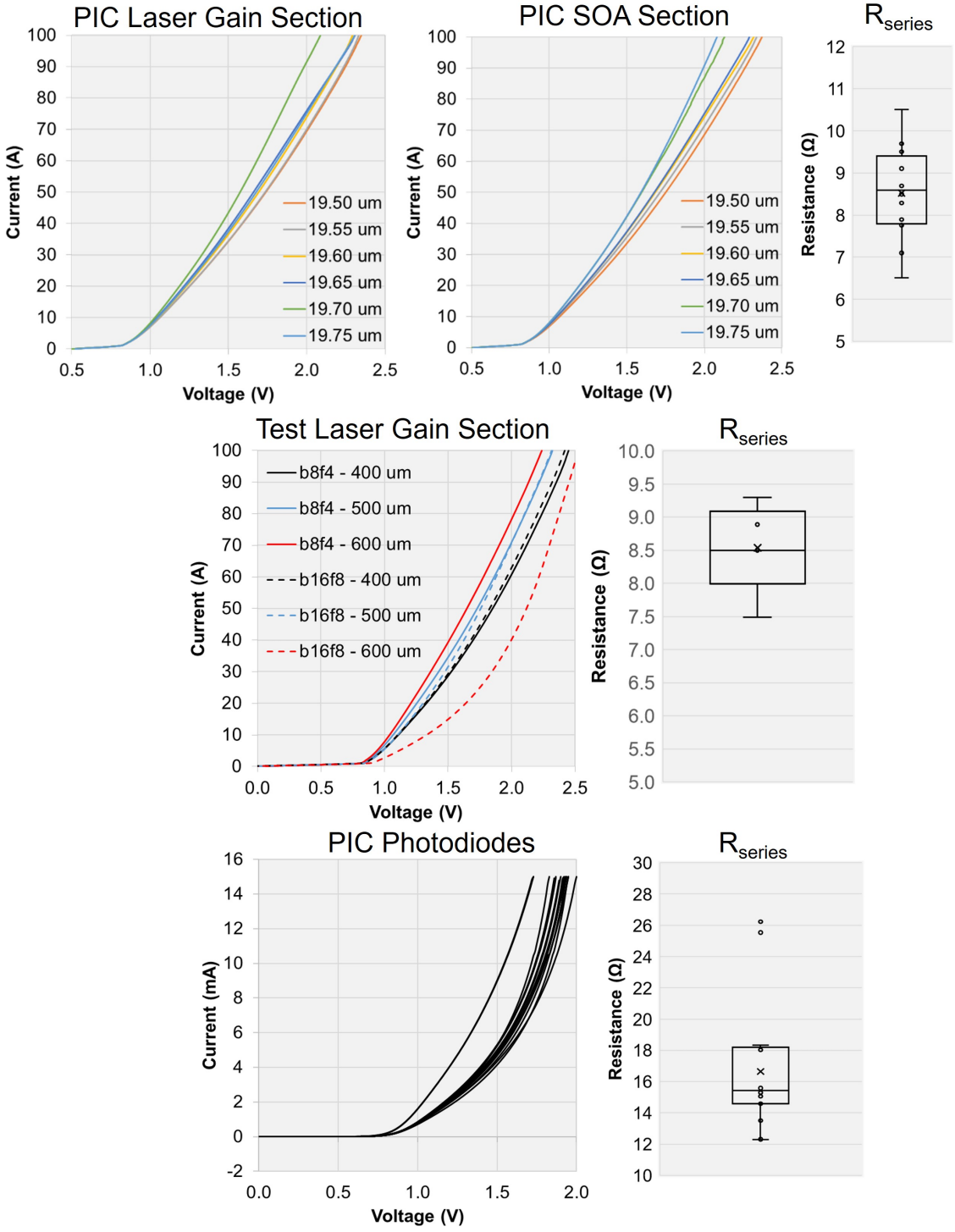


Figure 3.35: I-V measurements for the active regions are shown with the calculated series resistances (R_{series})

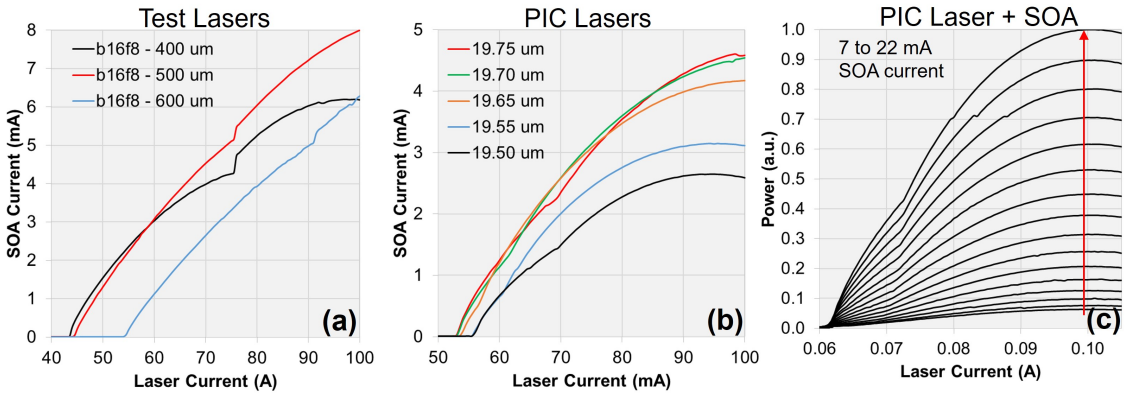


Figure 3.36: Output power resulting in SOA photocurrent is shown for (a) 3 test lasers and (b) several PIC lasers. (c) Relative output power is measured with increasing booster SOA current with a PIC high speed PD.

pads on an AlN subcarrier. A tapered optical fiber is used for coupling light to/from the waveguides. Example images of the wirebonded subcarriers are shown in Fig. 3.37. Using this setup, the laser spectrum was monitored while adjusting the current through the grating mirror sections to tune the wavelength. Figure 3.38 shows the laser can be tuned to 5 different supermodes. Due to changes in the mirror reflectance and gain spectrum, the laser threshold and output power will change as a function of the lasing wavelength. The output power curves in Fig. 3.38 show that the laser has a higher efficiency between 1320 nm and 1330 nm. This is likely due to higher material gain at these wavelengths which can be seen from the peak in the amplified spontaneous emission (ASE) spectra close to 1330 nm. The decrease in the gain and the SG-DBR reflectance both contribute to the higher threshold current when operating at 1297 nm. While the thresholds are higher than desired, the single-mode performance of the laser meets expectations, with MSRs above 40 dB, as shown in Fig. 3.39.

The wavelength tuning efficiency of the SGDBR phase section is important to examine because it is used as the feedback mechanism for frequency and phase locking the LO to the transmitter laser. Figure 3.40 shows that the phase section can tune the laser by 0.2 nm (35 GHz) with an efficiency of 20 to 50 pm/mA (3.6 to 9.0 GHz/mA), meeting the

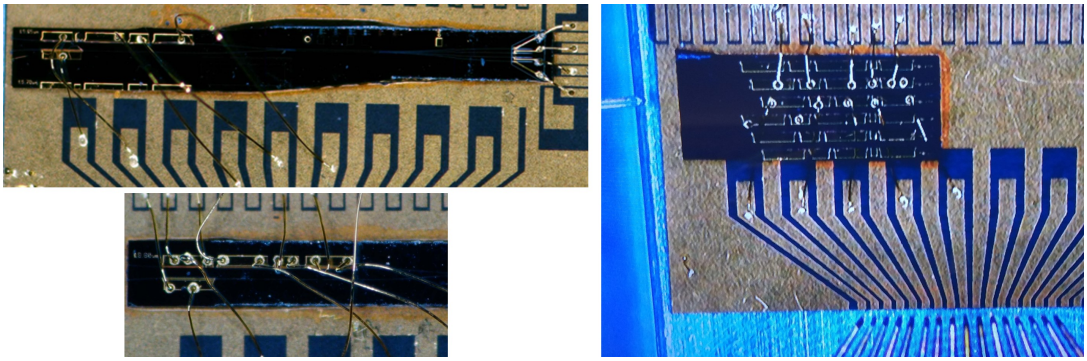


Figure 3.37: Example images of wirebonded PICs and test lasers on AlN subcarriers

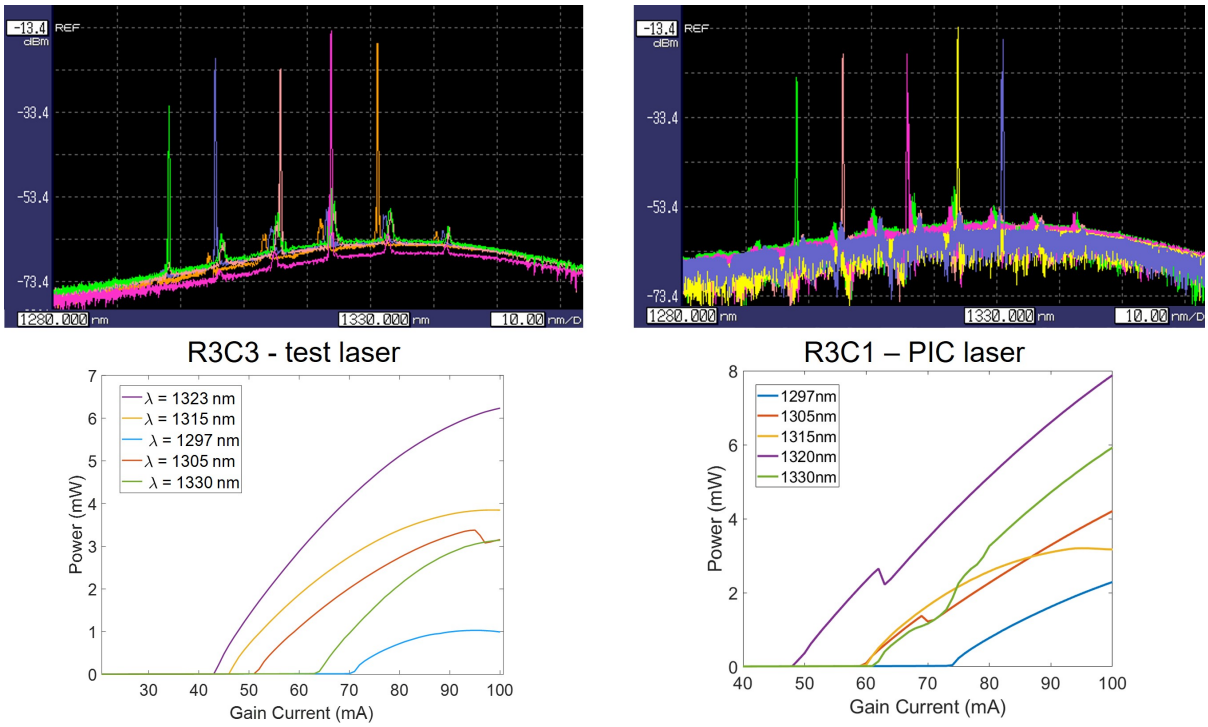


Figure 3.38: On-chip power output and output coupled spectra are show for a test laser and PIC laser.

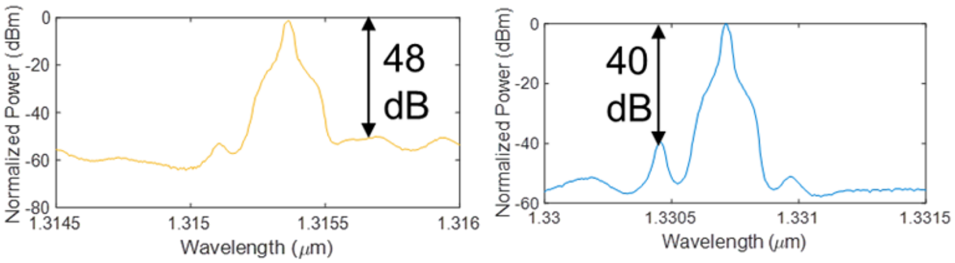


Figure 3.39: High resolution spectral sweeps at two wavelengths show 40 dB or higher MSR.

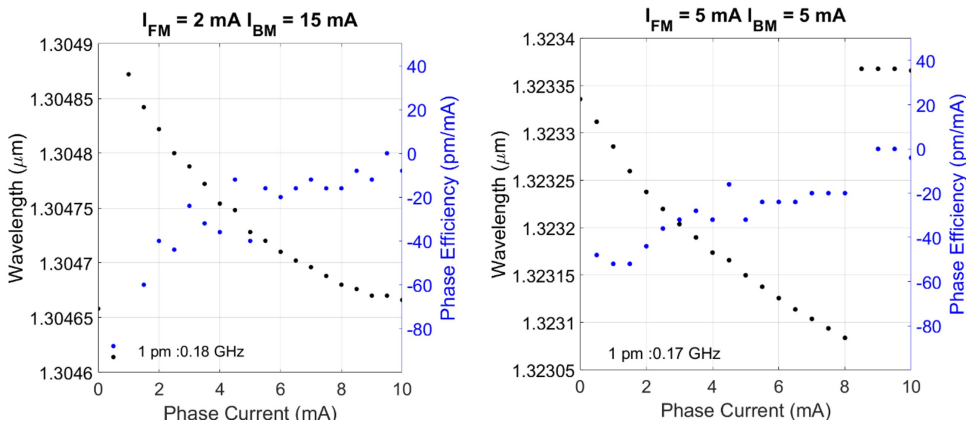


Figure 3.40: Phase efficiency is measured at two wavelengths by tuning the SG-DBR mirrors and phase section current.

desired target from Table 3.1. By setting the phase section to 5 mA as a DC operating point, the current swing from the OPLL feedback loop can tune the phase section and lock to a reference within ±0.1 nm of the LO. This assumes that the cavity length of the laser is tuned such that cavity mode hop will not occur within the ±0.1 nm range. Setting the phase section operating point to maximize the output power will help to align the cavity mode with the mirror reflectivity peak and reduce mode hopping, but this is challenging due to the low variation in power across the phase section tuning range.

The integrated/apparent linewidth, presented in Fig. 3.41, was measured with a standard keithley current source and a low noise source supplying current to the gain section. Noise in the current source contributes greatly to the integrated linewidth. This is expected from previous work [24]. Measurements with increasing power don't show a significant linewidth reduction as expected by the theory on Lorenztion linewidth. This likely indicates that the integrated linewidth is dominated by lower frequency noise. Even when using the battery box to reduce the noise from carrier injection, the linewidth is still relatively large which could be related to variations in carrier concentration from the parasitic well or from other scattering loss mechanisms.

Measurements of the power splitting on the MMI test structures, shown in Fig. 3.42,

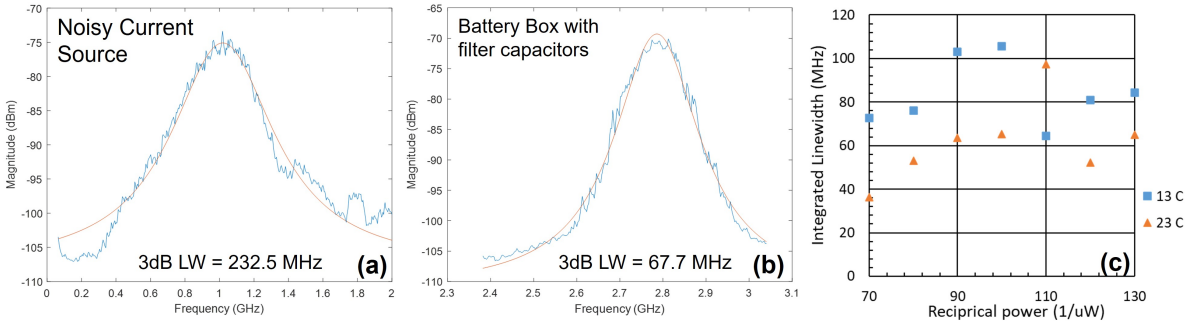


Figure 3.41: Heterodyne linewidth measurements between the SG-DBR and a low noise external laser when biasing the gain with (a) a standard/noisy current source or a (b) low noise supply. Measurements are included (c) at two temperatures and multiple SG-DBR output powers.

indicate that the 19.7 um nominal width shows the best power splitting. This aligns with the 0.1 to 0.2 um decrease in the pattern width observed during fabrication. The large variations in the response show how sensitive the hybrid transmission is to the width, although the testing conditions add confounding factors which can lead to larger variations in the response. The coupling loss was frequently adjusted to maintain optimal coupling, but changes in coupling between measurements will add more imbalance between the photodiodes. Changes in the input polarization can impact the coupling loss, and measurements also showed a strong sensitivity of the spectral response on the input polarizaton. Figure 3.43 depicts the change in the spectral response from one of the 90° hybrid output PDs with two different input polarizations. This polarization sensitivity is likely contributing to some of the oscillations in the measured data shown in Fig. 3.42.

The responsivity over wavelength was measured with the photodiode test structures, and it showed only 0.5 dB of variation across the tuning range of the laser with a steep roll-off after 1330 nm as the photon energy falls below the bandgap. Using a lightwave component analyzer, the photodiode frequency response was measured and is shown in Fig. 3.44. The OE bandwidth is only 21 GHz based on the frequency response, worse than the expected 24 to 27 GHz from the design calculations in Section 3.1.4. The lower

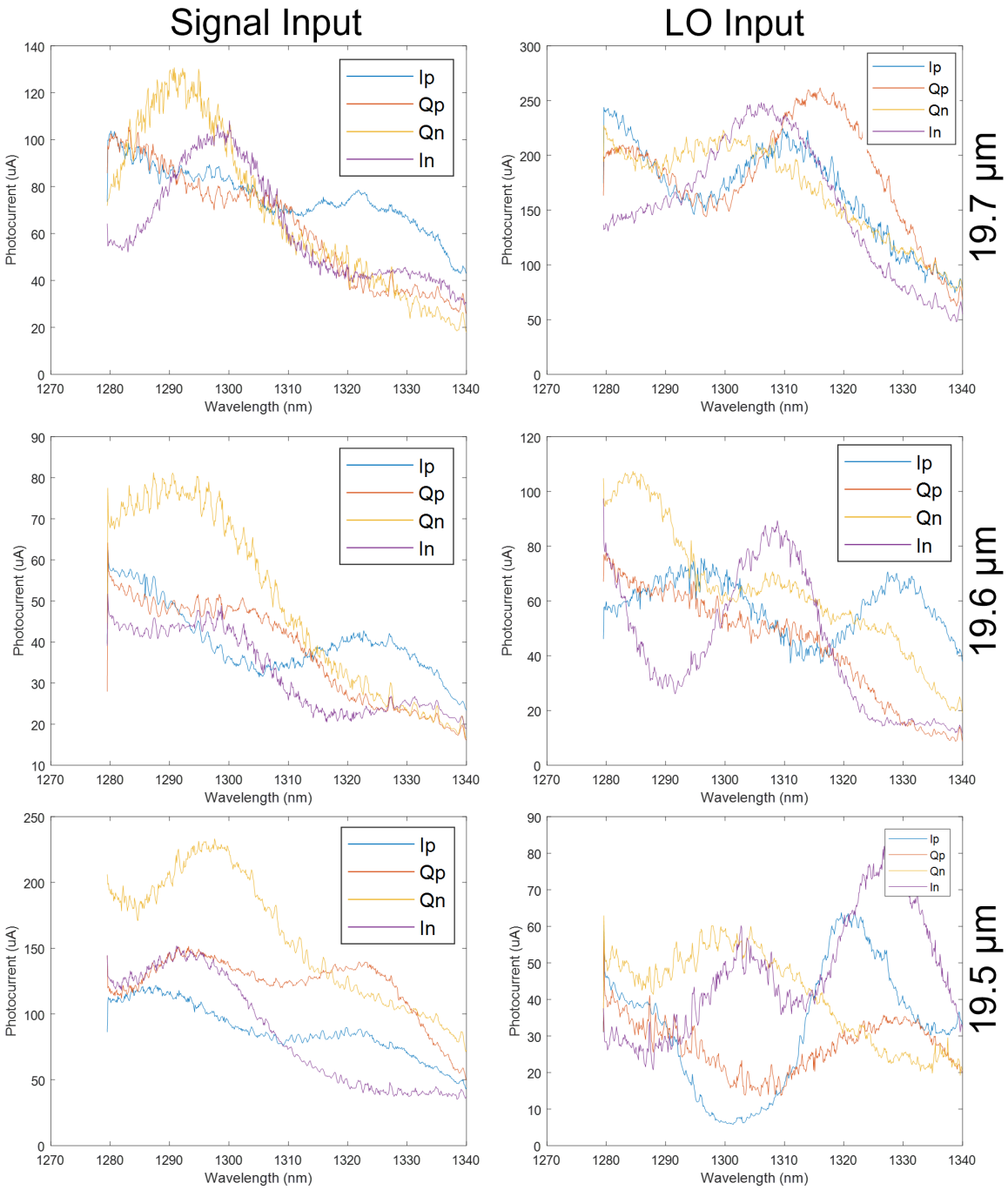


Figure 3.42: Measured output photocurrent from 3 different MMI power splitting test structures using the signal or LO input ports.

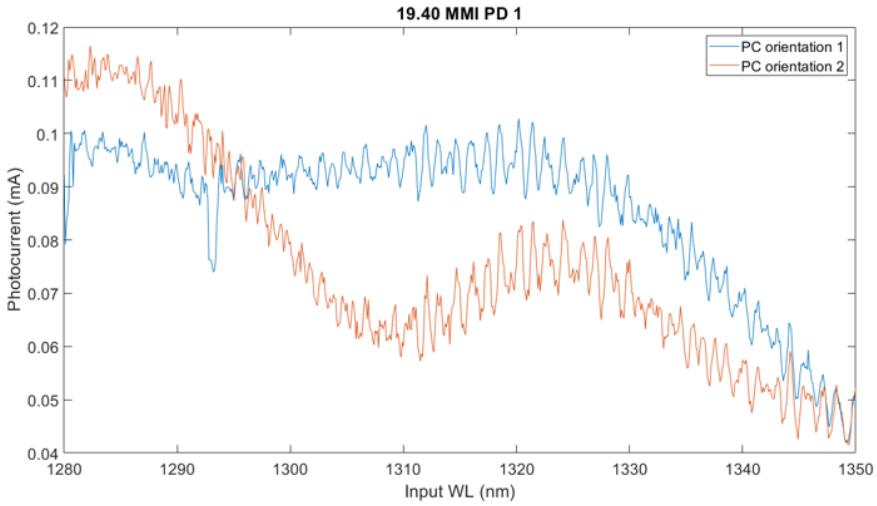


Figure 3.43: MMI spectral response with two different input polarizations.

bandwidth could be caused by a combination of p-dopants diffusing inward from the regrowth and larger than expected capacitance from the PD metal traces & pads.

3.4 Gen. 1 Receiver Assemblies

After characterizing a few of the PICs to check that the laser, SOAs, and photodidoes were all fully functional, they were integrated into a large assembly for demonstrating the coherent receiver with an optical phase-locked loop (OPLL) as discussed in Section 3.1. The first design of the AlN subcarrier for the electronics and PCB were led by Aaron Maharry. A completed assembly is shown in Fig. 3.45. It includes the InP RX PIC connected to two Adsantec 6122-BD transimpedance amplifiers each with a one channel, single-ended input and differential outputs as shown in the Fig. 3.46 schematic. The differential outputs are split, with one end going to the miniSMP connectors on the PCB for monitoring the received signal and the other end going to the Adsantec 5140-BD XOR, acting as the phase-frequency detector (PFD) which helps create the feedback signal for locking the phase and frequency of the InP LO to the transmitted signal. Both

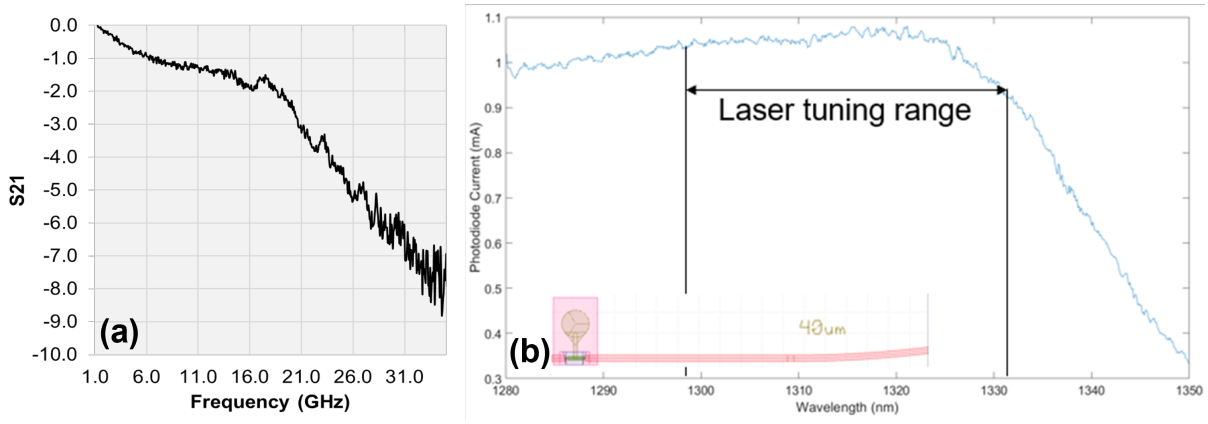


Figure 3.44: Photodiode characterization showing the (a) Electro-optical (S21) response and the (b) spectral response.

of these components have high bandwidth (>30 GHz) in order to detect the phase error of the received high-speed data. A loop filter is needed to adjust the frequency response of the gain and phase of the error signal with a Texas Instruments LMH6609 Op Amp providing high gain a low frequencies. The RC components in the loop filter are chosen to adjust the response of the feedback loop to achieve frequency locking with large offsets and to maintain phase-locked stability despite fluctuations in laser phase and power. More details regarding OPLL design are discussed in [24, 25].

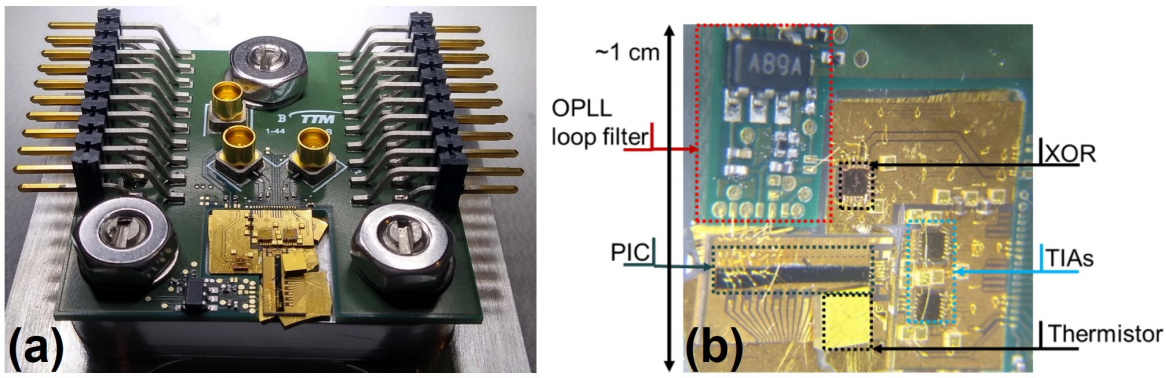


Figure 3.45: (a) The full PCB assembly for the OPLL testing is shown, and (b) the main components are labeled in a close view of the circuit.

Initial tests using the setup in Fig. 3.45 produced a beat tone when the external

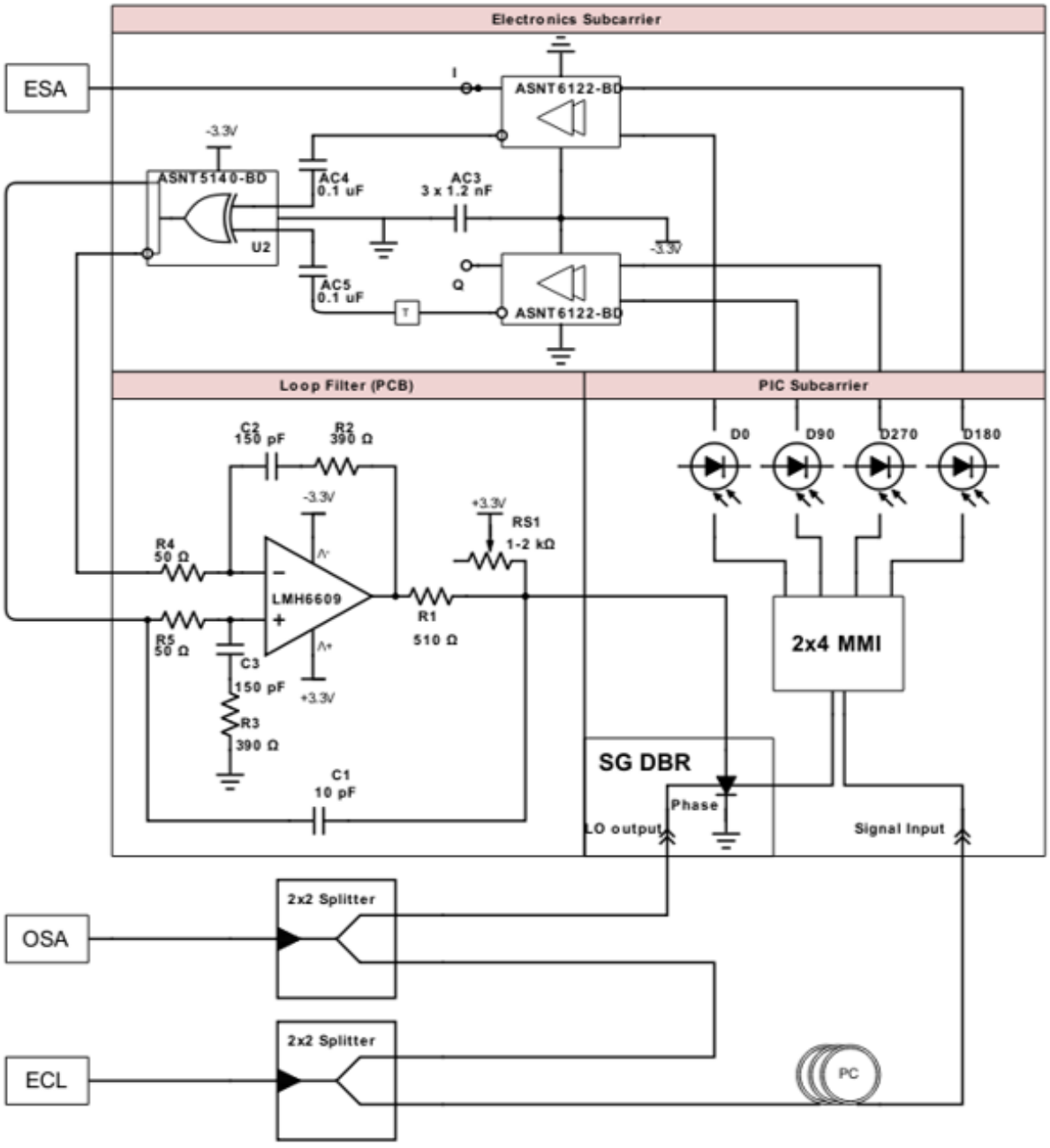


Figure 3.46: Schematic of the test setup for the initial version of the OPLL with the InP RX and COTS electronics.

cavity laser (ECL) was coupled into the signal port of the PIC. Frequency locking is achieved by coarse alignment of the ECL and the LO wavelengths to within 10 GHz using the spectrum observed on the OSA followed by fine alignment by observing the beat tone on the electrical spectrum analyzer (ESA). Once the wavelengths are aligned within a few GHz, the LO laser appears to lock to the ECL. Figure 3.47(a) & (b) depict the beat tone before locking and the spectrum on the ESA after locking. While these results show that the coherent mixing of the lasers and the amplification of the output through the TIAs is working, the width of the beat tone is far too broad compared to the previous linewidth measurements and the frequency spectrum observed after locking does not match the expectation of a sharp homodyne peak near 0 GHz. The broad roll off and persistence of the 8 Ghz peak could be caused by the improper impedance of the terminations or discontinuities in the transmission lines between the TIA and the XOR, causing back reflections. The requirements for the PIC, XOR, and TIA bias also necessitated two different bias planes at 0V and -3.3V on the AlN subcarrier with AC coupling of the high speed signals which could also be contributing to the nonideal frequency spectrum. Since the PIC uses a common n-doped substrate, the PD p-side voltage must be negative to keep the n-side at ground, or substrate voltage and laser p-side voltage must be raised above ground. Despite this issue, the phase section voltage was measured while the LO and ECL showed frequency locking behavior. The phase section voltage decreased while increasing the ECL wavelength as shown in Fig. 3.47 (c). The matches the expected frequency tracking behavior where the phase section voltage and current decrease to increase the LO wavelength.

Further investigation of the broad 8 GHz beat tone showed that it was present with the electronics turned on, even without an optical signal. It was determined that a redesign of the OPLL circuit and PCB was needed to avoid issues with the feedback loop. Fig. 3.48 shows a schematic of the single-ended and differential variants for the

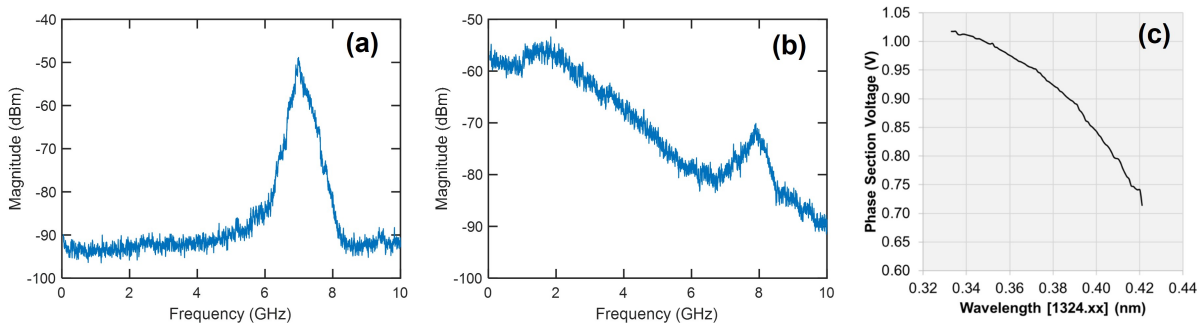


Figure 3.47: (a) The beat tone between the ECL and LO without locking. (b) Frequency spectrum during frequency tracking. (c) OPLL voltage output to the LO phase section as the ECL wavelength is swept.

new OPLL circuit, designed by Junqian Liu. A new two channel Inphi 6552TA TIA replaced the two Adsantec TIAs. The differential variant also included Adsantec 5121E data signal distributors for splitting the signal to enable a fully differential input to the XOR while also monitoring the TIA output. Images of the new assemblies are shown in Fig. 3.49.

With the improved signal integrity and DC bias compatibility from the new OPLL circuit design, a narrow beat tone was measured between the LO and ECL without the OPLL enabled, as shown in Fig. 3.50. When the LO and ECL were locked, the frequency response in Fig. 3.50(b) showed only a single, narrow peak from the locked lasers, and the OPLL was able to reduce the linewidth from 38 to 6 MHz. However, for homodyne frequency locking, a locked peak at 0 GHz is expected, while the peak was measured at 4.37 GHz.

Further testing and simulation by Junqian led to modifications of the loop filter RC values, alterations in the biasing of the XOR, changes to AC coupling between the TIAs and XOR, and the additional of decoupling capacitors in an effort to remove the offset in the beat tone. Figure 3.51 shows an updated loop filter circuit for improved loop stability and the measured frequency response from the TIA. The beat tone offset was shifted to 800 MHz, but it was not eliminated. Continued work on the OPLL was put on hold while

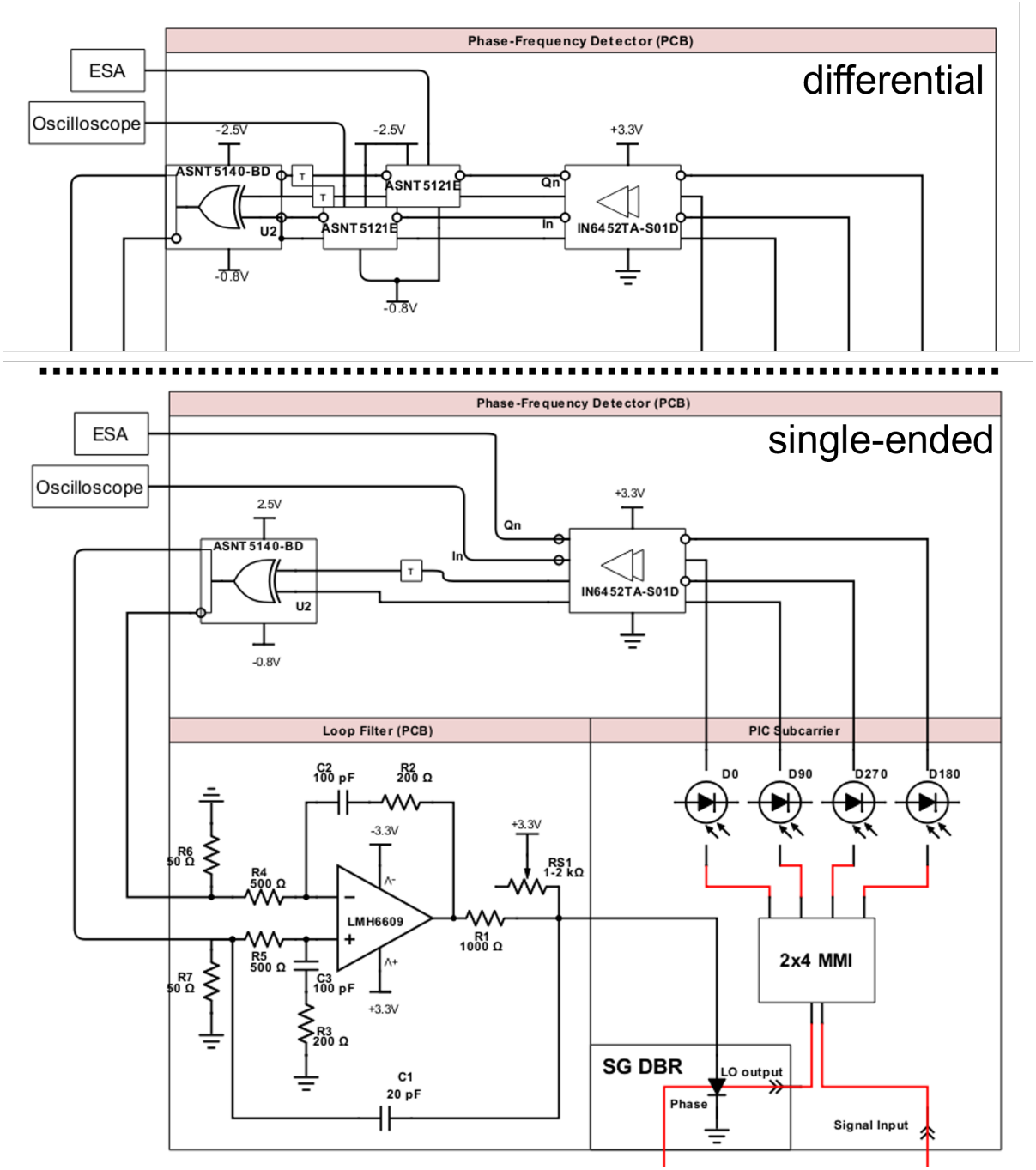


Figure 3.48: Schematic for the new single-ended and differential OPLL assemblies with modified COTS components and loop filter design.

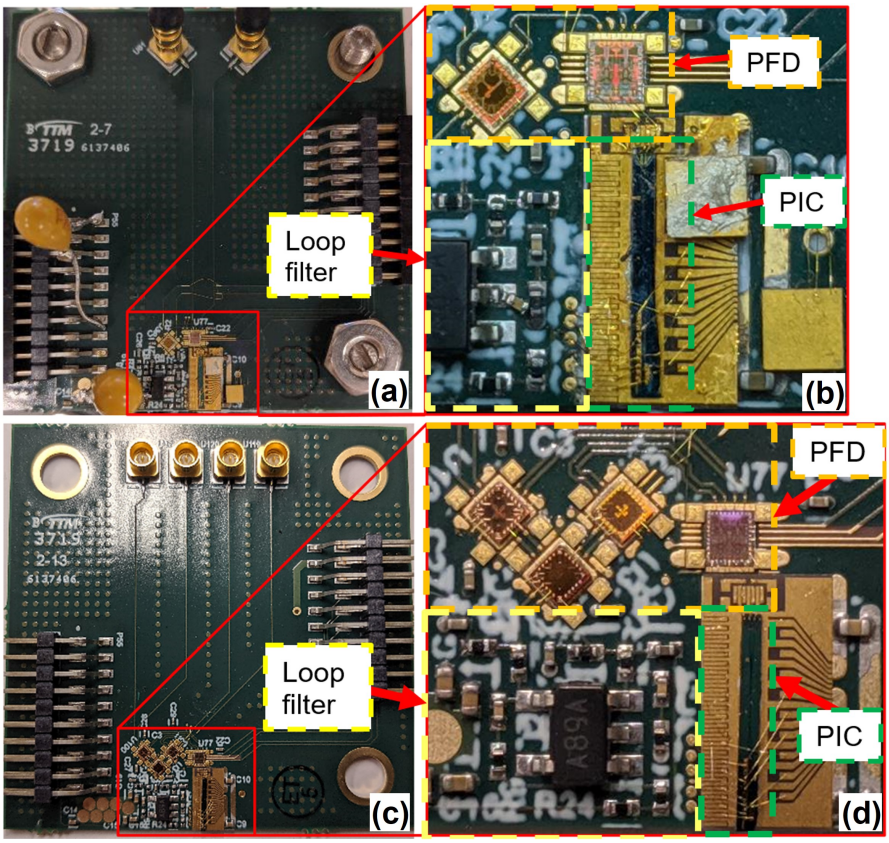


Figure 3.49: (a) An overview of the single-ended assembly with (b) a close view of the major components. (c) An overview of the differential assembly with (d) a close view of the major components.

custom electronic chips where the TIA and XOR were integrated together were designed and fabricated. Integration will mitigate issues with transmission lines between the chips and result in better loop performance from a shorter loop delay.

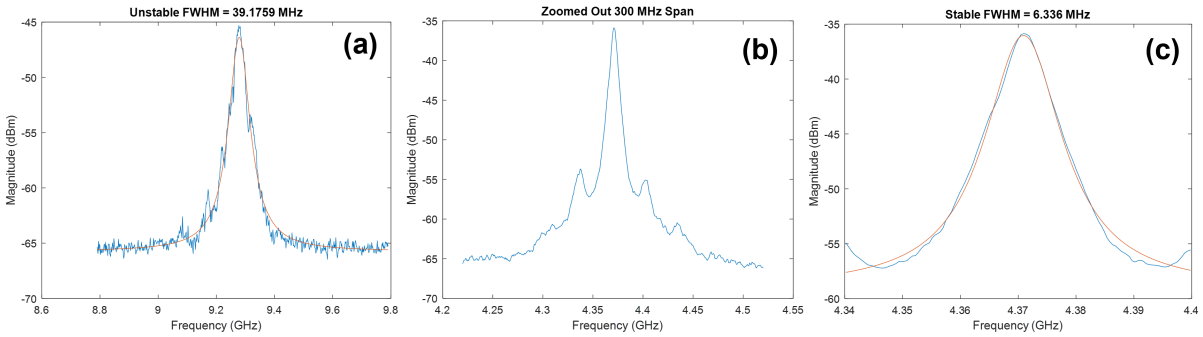


Figure 3.50: The beat tone (a) before and (b) after frequency locking with a 4.37 GHz offset. (c) Higher resolution frequency sweep showing linewidth narrowing.

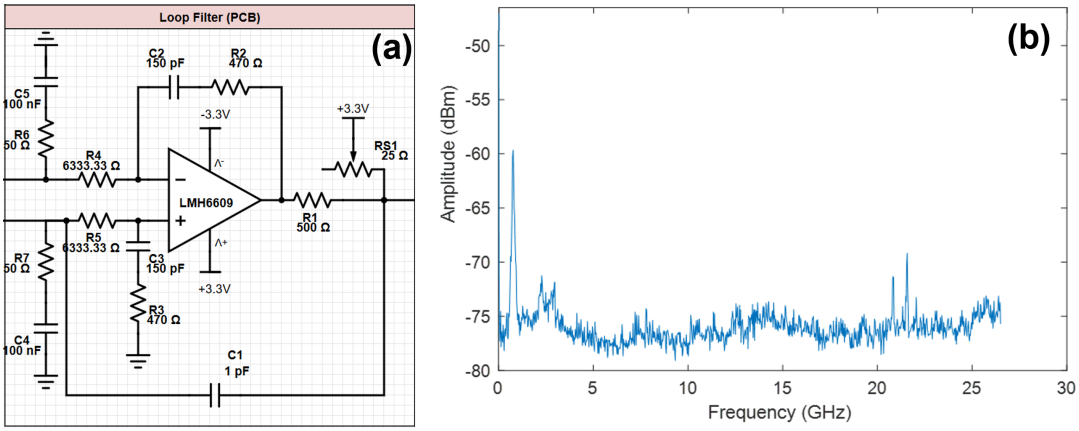


Figure 3.51: (a) Modified loop filter schematic for improved frequency locking and (b) the measured electrical spectrum after locking with an 800 MHz offset.

Chapter 4

Generation 2 InP O-band Coherent Receiver

Based on the insights from testing the first generation InP coherent RX, a second generation was created with several modifications to the design and fabrication. The major design changes will be covered in Section 4.1. An overview of the fabrication will be provided in Section 4.2 with electrical test results discussed in Section 4.3, and lessons learned from issues with the fabrication will be described in Section 4.4.

4.1 Gen. 2 InP PIC Design

After measurements showed higher than expected threshold currents, the band structure of the epitaxial layers was more closely examined. Calculations made by Thomas Meissner showed that the SCH layer was creating a shallow well which will impede the injection of holes into the QWs, leading to an increase in the threshold current. Figure 4.1 shows a side-by-side comparison of the gen. 1 and gen. 2 band structures. The layer was corrected by changing from $In_{0.78}Ga_{0.22}As_{0.44}P_{0.56}$ to $In_{0.88}Ga_{0.12}As_{0.26}P_{0.74}$ which changes

the bandgap wavelength from 1.18 μm to 1.066 μm.

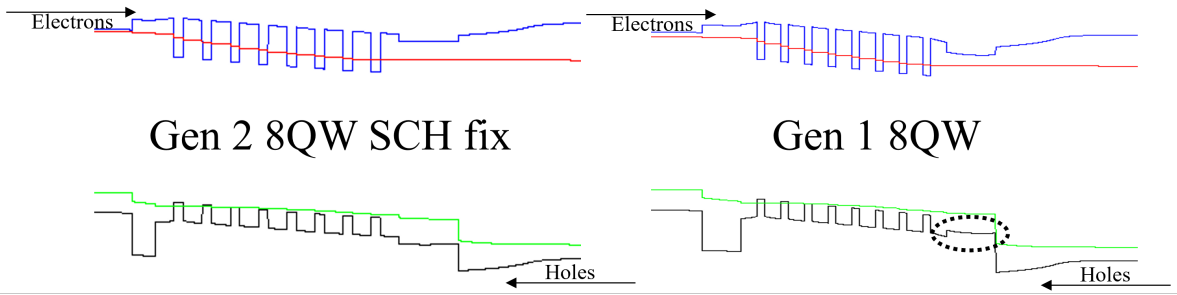


Figure 4.1: Calculated band structure for the gen. 1 active region with the parasitic SCH well and the corrected structure for gen. 2

The switch from an sulfur doped n-type InP substrate to a Fe-doped semi-insulating (SI) substrate was another major design change. A semi-insulating substrate enables PD contact pads to be placed in etched vias rather than on top of BCB. This will reduce the risk of poor pad adhesion that was enconutered in the first generation. For n-contact, an embedded Si-doped InGaAs layer is included in the epitaxy with Si-doped InP acting as the n-cladding layers. To reduce absorption loss, the dopants are graded to lower values close to the optical mode. With thin (2.4 μm) embedded n-doped layers, it is possible to etch and/or implant those layers for electrical isolation between different areas of the PIC. This will avoid conflicts between the biasing requirements for the laser and the TIA connected to the PDs. To examine the impact of QW filling and optical mode confinement, two variants of the epitaxy, with 4 or 8 QWs, were ordered. The full details are presented in Table 4.1.

The junction capacitance of the 4 QW photodiode, shown in Fig. 4.2, is expected to be slightly higher than the 8 QW variant at 45 to 50 fF between 2 and 3 V reverse bias. The overall capacitance from RC parasitics is expected to be similar to the first generation. While the traces are shorter, and the semi-insulating substrate will remove the parallel plate capacitance between the pad and the n-doped layers, the transition into the etch via and the various n-metal structures will add capacitance. BCB is still

Table 4.1: Epitaxy Design for Gen. 2 InP Receiver

#	Purpose	Material	Doping (cm^{-3})	Thickness (μm)	Tolerance ($\pm\mu$m)
0	substrate	Fe-doped S.I.-InP	—	355	15
1	n-buffer	n-InP (Si)	$1x10^{18}$	0.5	0.05
2	n-contact	n-$In_{0.53}Ga_{0.47}As$ (Si)	$3x10^{18}$	0.1	0.01
3	n-cladding	n-InP (Si)	$1x10^{18}$	1.6	0.16
4	n-cladding	n-InP (Si)	$8x10^{17}$	0.1	0.01
5	n-cladding	n-InP (Si)	$6x10^{17}$	0.1	0.01
6	WG core	n-1.18μm quaternary $In_{0.80}Ga_{0.20}As_{0.44}P_{0.56}$	$1x10^{17}$	0.15	0.015
7	WG core	n-1.18μm quaternary $In_{0.80}Ga_{0.20}As_{0.44}P_{0.56}$	$5x10^{16}$	0.15	0.015
8	wet etch stop	n-InP (Si)	$5x10^{16}$	0.01	0.001
9	gain	quaternary QW & barrier 4,8×$In_{0.83}Ga_{0.17}As_{0.65}P_{0.35}$ 5,9×$In_{0.83}Ga_{0.17}As_{0.27}P_{0.73}$	UID	4,8×4nm 5,9×8nm 0.056,0.104	0.006, 0.01
10	SCH	1.066-μm quaternary $In_{0.88}Ga_{0.12}As_{0.26}P_{0.74}$	UID	0.025	0.003
11	doping buffer	InP layer	UID	0.02	0.002
12	p-cladding buffer	P-InP (Zn) layer	$5x10^{17}$	0.18	0.018
↑ base epitaxy — regrown epitaxy ↓					
13	doping buffer	InP	UID	0.055	0.006
14	p-cladding	p-InP (Zn)	$5x10^{17}$	0.010	0.001
15	p-cladding	p-InP (Zn)	$2x10^{18}$	0.030	0.003
16	p-cladding	p-InP (Zn)	$5x10^{17}$	0.430	0.043
17	p-cladding	p-InP (Zn)	$7x10^{17}$	0.500	0.050
18	p-cladding	p-InP (Zn)	$1x10^{18}$	0.805	0.081
19	p-contact	p-$In_{0.53}Ga_{0.47}As$ (Zn)	$1.5x10^{19}$	0.1	0.01
20	protective cap	p-InP (Zn)	$1x10^{18}$	0.490	0.05

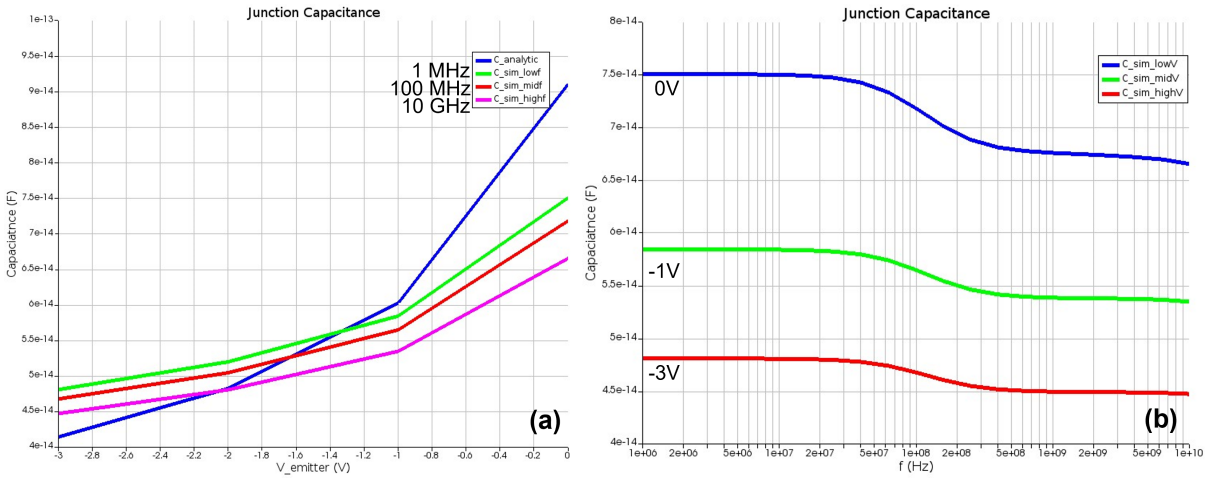


Figure 4.2: (a) Simulated capacitance over PD voltage at different frequencies. (b) Simulated Capacitance over frequency at 3 PD voltages.

used to decrease the capacitance of the metal contact to the PD ridge and of the trace as it slopes down into the etched via to the SI-substrate. Fringing capacitance between the PD anode/signal pads and the other n-metal and capacitance from the pads through the substate to the PCB ground plane can both contribute on the order of 10 fF.

A few changes were made to the RX PIC design for performance improvement and risk mitigation. An SOA was added next to the SG-DBR back mirror to provide a stronger signal for monitoring the wavelength and to allow the full on-chip output power of the laser to be measured, using the front and back SOAs as PDs. The PIC was shortened to help fit more designs and structures on the mask and to reduce the loop delay for the OPLL. The length was reduced by moving the front SOA into the angled waveguide between the laser and MMI and by reducing the waveguide length from the MMI output to the PDs. For risk mitigation, tuning sections were added to the MMI that would enable adjustments to the effective optical length and width of the structure. Deviation from the simulated performance can be corrected with these tuning structures. Attenuators were also added at the output of the MMI to allow for corrections to the power splitting. The full PIC layout is presented in Fig. 4.3. To reduce the risk of

multimode inputs to the hybrid, the waveguide widths were reduced to 1.5 μm at the MMI input and the taper length was increased to 50 μm.

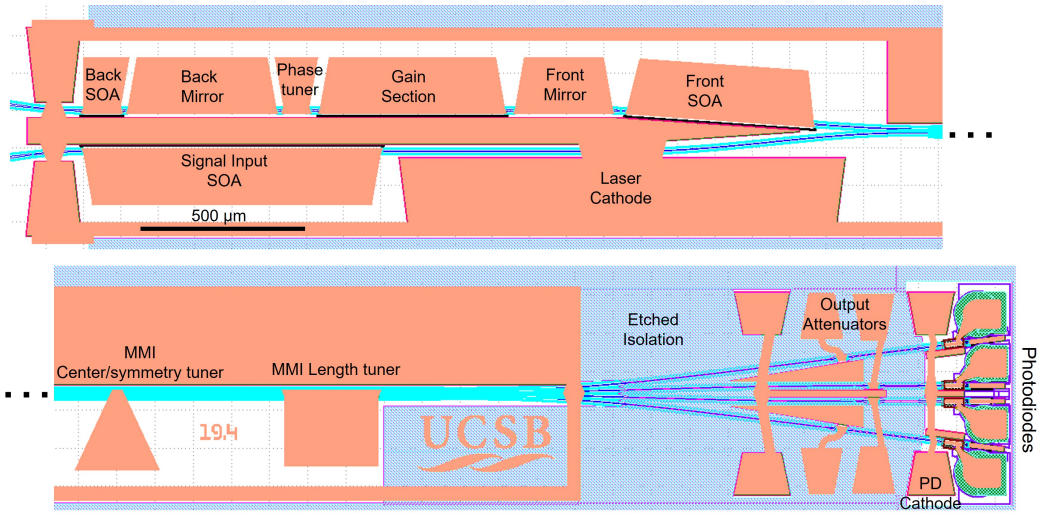


Figure 4.3: Layout of RX PIC with labeled device sections.

Similar to the first generation, several PIC variants were included with changes to the MMI width. Variants with and without MMI tuners were also included to examine the excess loss added by the tuning elements. The 90°hybrid MMI test structures were redesigned to include a tunable Mach-Zehnder interferometer at the input of the hybrid to examine the output with a varying input port phase difference. Broad area lasers were replaced with narrow ridge Fabry-Perot lasers and waveguide test structures for material characterization. Standalone SG-DBR lasers and PDs were included for characterizing the lasers and PD performance separate from the PICs. Electrical TLM structures were kept the same as the first generation. The mask layout is shown in Fig. 4.4 with each of the sections labeled for reference.

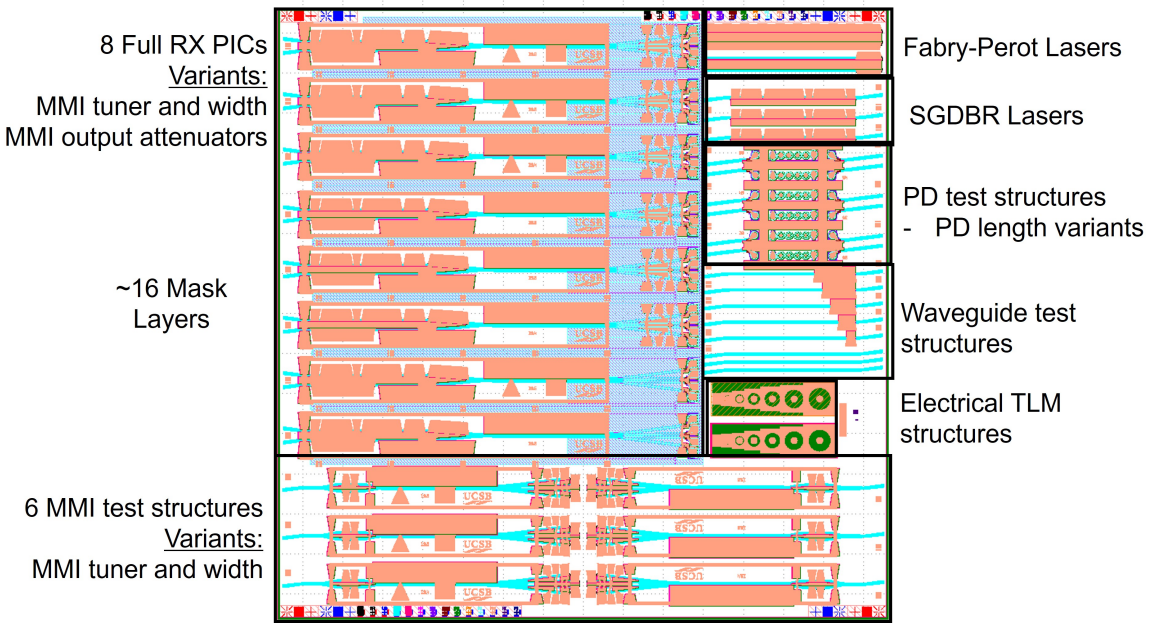


Figure 4.4: Mask Layout with labeled structures for the second generation InP Coherent RX

4.2 Gen. 2 InP PIC Fabrication

The following sections briefly describe the method and reasoning for each of the fabrication steps of the second generation InP RX. Due to unforeseen issues, which will be explained later, process steps were added and others were modified midway through fabrication. As such, this process is not optimized. While many of the fabrication steps went according to plan, there were a few steps later in the process which encountered issues that were challenging to resolve.

4.2.1 Gen. 2 InP RX - Alignment marks

An initial step to dry etch alignment marks for the stepper and e-beam lithography was added in comparison to the first generation InP RX. This allows for more higher contrast marks from a deeper (500 nm) etch. The dry etch also avoids the distortions caused by the anisotropic wet etching of the the QWs. Figure 4.5 shows the photoresist

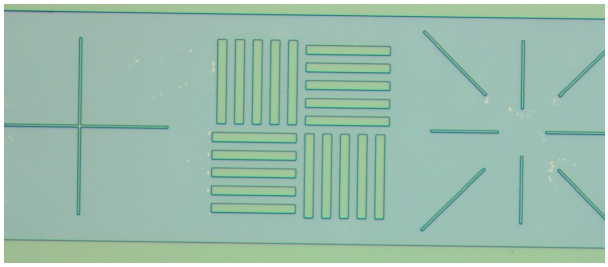


Figure 4.5: Step 1 alignment marks

pattern where a window is patterned around the alignment marks. The SiN hard masks and the III-V epilayers will both be dry etched to form mesas for the alignment marks.

4.2.2 Gen. 2 InP RX - Active Passive

The active passive etching is conducted in exactly the same way as previously described in Section 3.2.1, resulting in trapezoidal etched mesas where the laser gain, SOA, and PD sections will be defined. The QW wet etching needed to be more timed and measured more carefully due to a reduction in the InP etch stop layer from 20 to 10 nm.

4.2.3 Gen. 2 InP RX - Gratings

The grating etching was also processed using the same method as the first generation, discussed in Section 3.2.2. The grating recipe was modified compared to the first generation. A thinner SiO_2 hard mask (20 compared to 50 nm) was used to reduce the size reduction that occurs from the lateral etching of the hard mask. The hard mask dry etch creates a slightly angled sidewall which will reduce the opening size by $2t_{SiO2}/tan(\theta)$. At an 80 degree angle, the opening will decrease by only 7 nm for a 20 nm thick hard mask, compared to 18 nm for a 50 nm thick layer. Figure 4.6 shows an image of the patterned gratings for the back mirror.

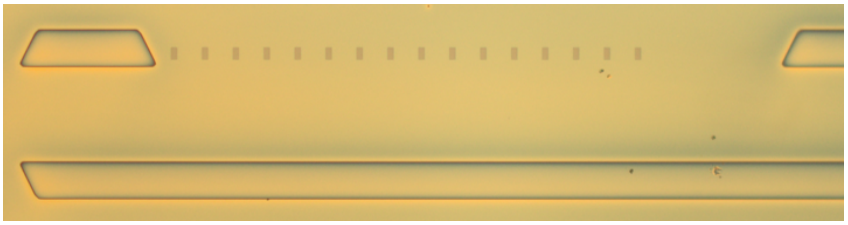


Figure 4.6: SG-DBR back mirror gratings after EBL

4.2.4 Gen. 2 InP RX - Regrowth

Regrowth was performed using the MOCVD reactors at UCSB with help from Simone. The same regrowth preparation steps compared to gen. 1 were used - H_2SO_4 dip, 1 hour UV ozone, and 1 minute BHF dip. The regrown layers for the second generation, shown in Table 4.1 were slightly different than the gen. 1 layers in Table 3.1.1. The height of the ridge was reduced by 200 nm, shrinking the 1×10^{18} doped layer from 1.0 to 0.8 μm. This can help reduce the resistance of the p-cladding layer. Doping was also added to the top p-InP cap layer which can reduce the diffusion of dopants out of the p-InGaAs contact layer. Maximizing the dopant concentration in the contact layer is important for achieving a low contact resistance.

4.2.5 Gen. 2 InP RX - Ridge Waveguide

Using a similar dry etch with a wet etch clean-up as described in Section 3.2.4, the ridges were etched using the Unaxis ICP for the first few real samples. Later test samples were prepared using the (new at the time) Oxford Cobra tool. This tool has a lower temperature recipe that does not require any grease for thermal conductivity. It uses a $Cl_2/CH_4/H_2$ gas mixture at 3 mT and 60°C. A couple new techniques were also added on later samples to improve the etching uniformity and repeatability. A $1:3HCl:H_2O$ clean was added immediately before the dry etching to help remove surface oxidation that can decrease the etch rate and lead to surface roughness. When etching the samples, blank

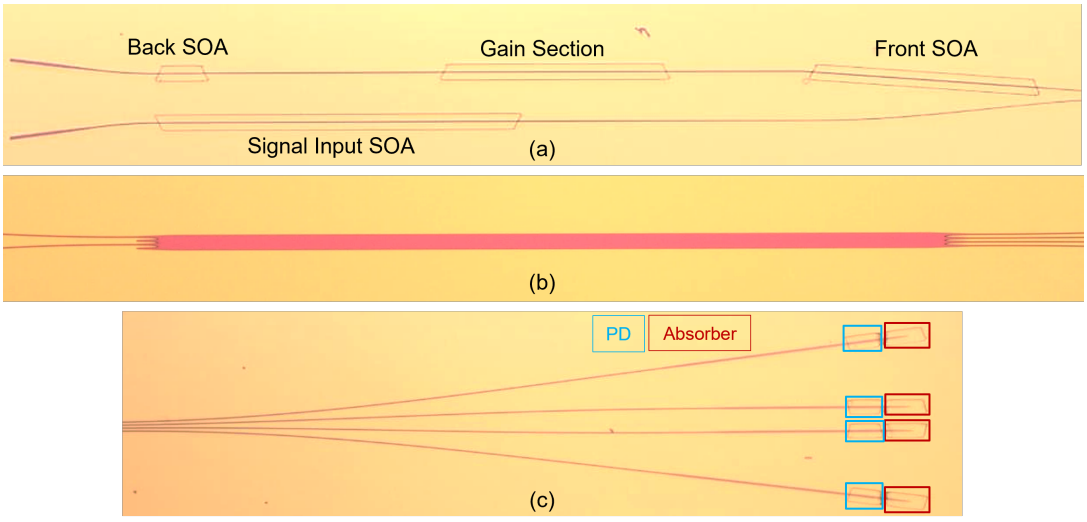


Figure 4.7: Overview images after the waveguide ridge etch show the (a) laser and signal input ridges to the (b) 90°hybrid with (c) the output waveguides to the PDs

InP pieces were also included to create a chamber loading effect which helps stabilize the etch avoid to sidewall roughness and achieve a more consistent etch rate [222].

4.2.6 Gen. 2 InP RX - PD Dopant Removal

To reduce the added capacitance from p-dopants that may have diffused into the SCH layer during regrowth, this layer and part of the QWs are removed from the area extending 8 μm away from either side of the PD ridge. A 50 nm SiN hard mask is deposited with PECVD, patterned with photolithography, and dry etched. The III-V material is then etched down by 50 nm, using a $CH_4/H_2/Ar$ gas mixture in RIE #2, similar to the grating etch.

4.2.7 Gen. 2 InP RX - P-InGaAs Removal

Just as in the gen. 1 InP RX, an SSA process is used to expose the ridge tops and remove the p-InGaAs layer for better electrical isolation between adjacent devices. See Section 3.2.5 and Fig. B.5 for more details on the process. Unlike gen. 1, a thinner 200

nm SiN hard mask was used, and it was removed after the InGaAs etching was complete. For the gen. 2 RX process, there are multiple future steps that deposit new hard masks for etching vias, so the hard mask for the SSA etching can be removed.

4.2.8 Gen. 2 InP RX - N-Via

Etching the n-vias down to the n-InGaAs contact layer is the first completely new step in the gen. 2 process. This step is required due to the Fe-doped SI-InP substrate, so backside contacts are not possible. Having n-contacts on the front of the sample is beneficial as it enables wafer level electrical testing. For the n-via etch, the process is similar to the ridge etch. A hard mask with 200nm SiN on 200 nm SiO_2 is deposited with PECVD. Photolithography is used to define the pattern that is dry etched into the hard mask. Figure 4.8 shows the patterned photoresist. Then the hard mask is used for dry etching III-V material, targeting an etch depth around 400 nm above the InGaAs layer to avoid etching it. The sidewall angle and roughness are not critical for the vias, so the Unaxis, RIE #2, or Oxford Cobra etching tools could be used for etching the vias. Initial samples were etched with RIE #2, but future test samples used the Oxford Cobra once it was installed. To finish the etch and stop on the InGaAs layer, a $1HCL : 3H_3PO_4$ wet etch was used.

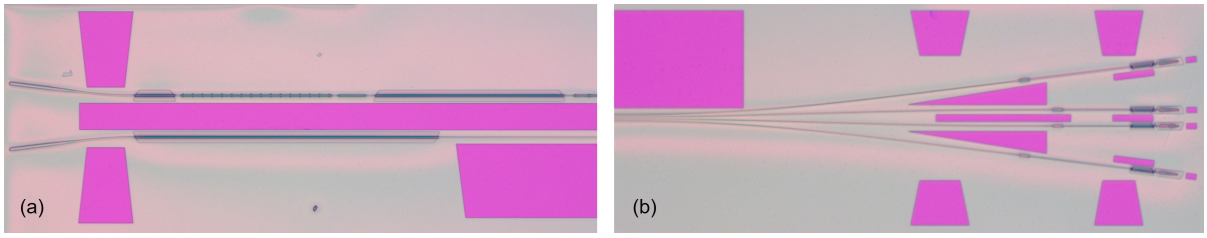


Figure 4.8: Developed N-via PR patterns are shown near (a) the laser and (b) PDs

An important aspect of the n-vias is their placement relative to the ridges. While the n-InP and n-InGaAs layers have relatively low resistivity, metal still provides a lower

resistance path. The high speed performance of the photodiodes can be improved by minimizing the resistance through the n-doped material to the metal which will be deposited in the n-vias. For this reason, small n-vias were placed 10 μm away from the PD ridges.

4.2.9 Gen. 2 InP RX - N-contact Metal

For the metal patterns, a bi-layer liftoff process was used with PMGI SF-15 and SPR220-3.0 photoresist. Prior to deposition, the sample was cleaned with 10 mins of UV ozone followed by a 15 second BHF clean. Based on work from previous students [80, 24], a metal stack with Nickel and Gold-Germanium was deposited for a thin n-contact metal. The metal stack was Ni/AuGe/Ni/Au with 5/100/20/300 nm thicknesses. This was deposited using e-beam #1 with top down deposition at approximately the same distance as the crystal monitor from the metal source. For the AuGe, a single pellet was loaded into a narrow "bazooka" style crucible and the entire pellet was manually evaporated at 2 to 3% of the e-beam power. The Ni and Au were evaporated using the standard e-beam sources and deposition recipes.

After removing the photoresist, the sample was annealed at approximately 420°C for 30 seconds in forming gas to improve the ohmic contact. Using the circular TLM structure on top of the InGaAs contact layer, resistances between 10 and 16Ω were measured for gaps between 40 and 100 μm, roughly corresponding to the expected 65 to 75 Ω/□ sheet resistance for the InGaAs when using the equations for circular TLM structures from [227].

4.2.10 Gen. 2 InP RX - Via to Substrate

For low capacitance, vias were etched down through the n-cladding and slightly into the SI-substrate, about 3 μm deep relative to the top of the WG layer. This step uses the same procedure as the dry etch for the waveguide ridges, but a thicker 300 nm SiO_2 on 200 nm SiN hard mask was used for more protection. When using the Unaxis, this thickness is more than enough with a roughly 20:1 (InP:SiO_2) selectivity, but it is barely enough when using the Oxford Cobra with a 10:1 selectivity. An initial test sample using the Unaxis showed poor etching quality with a faster than expected etch rate and pitting, shown in Fig. 4.9. These can be caused by non-uniform distribution of reactants during the etch and by residual reactants on the surface of the sample after the etch. To mitigate issues from both of these, chamber loading pieces of InP (2 to 3 cm^2 total area) were added during the etch, and the sample was rinsed with water immediately after the etching. After these improvements, the etched surface in Fig. 4.9 was smooth, and the etch rate was close to the ridge etch. For removing the hard mask after etching, a blanket CF_4/O_2 dry etch was used instead of BHF, to avoid photo-electro-chemical reactions that can occur [228].

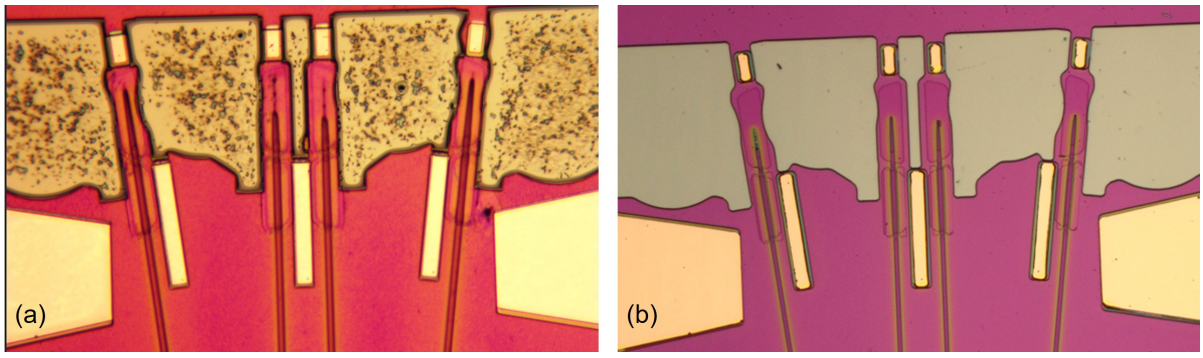


Figure 4.9: The substrate etch (a) before and (b) after adding improvements to the recipe

4.2.11 Gen. 2 InP RX - BCB Area

To create a permanent passivisation around the etched ridges and on the surface, a stack of 100/200/100 nm SiN/SiO_2/SiN was deposited with PECVD. Alternating layers are applied in order to have a more balanced mechanical stress profile. With the standard PECVD #1 recipes, SiN and SiO_2 have similar film stress magnitudes but opposite directions, so the overall film stress is minimized by alternating between them. BCB is patterned on top of the SiN for good adhesion. Unlike gen. 1, the BCB is only patterned in a small area around the PD ridge and into the etched substrate via. The BCB is designed to provide a smooth transition to reduce the capacitance between the metal and the n-doped sidewall and to avoid issues with discontinuities in the metal trace. Since there is only a small area between the PD ridge top and the substrate via, a 4 μm thick layer of BCB is not required. A thinner layer of BCB will help to reduce the aspect ratio of the via to the photodiode and avoid the BCB undercutting issue discussed in Section 3.2.9. A BCB recipe with thickness close to the height of the ridge is desirable to simplify the process of etching through the BCB. To customize the thickness of the BCB, several experiments were conducted with the help of Xinhong Du. Mesitylene or 1,3,5-trimethylbenzene is the solvent used for BCB. By adding more solvent to the BCB, the viscosity is reduced which will lead to thinner BCB after spin coating. Results from the experiments are shown in Table 4.2.

The recipe using 20% diluted BCB with 3.5 krpm spin speed was selected as it provided a thickness close to the ridge height in the area next to the ridge with only about 1.2 μm covering the top of the ridge, as shown by the scan in Fig. 4.10. The thickness and appearance of the BCB both looked good on the test sample, so the same recipe was used for the real sample. The full process steps for the passivation dielectric, BCB lithography, curing, and BCB encapsulation dielectric are presented in Appendix B in

Table 4.2: BCB dilution and spin speed recipes

BCB Recipe ↓	Spin Speed	Post Soft Bake Thickness (μm)	Post Develop Thickness (μm)	Post Curing Thickness (μm)
BCB 4024-40 (datasheet)	2 krpm	8.4	—	5.9
	4 krpm	4.1	—	4.1
10% diluted BCB	2k rpm	5.3 - 5.6	5.0 – 5.2	4.6 – 4.7 (?)
	4 krpm	4.4 - 5.1	2.4 – 2.7	2.4 - 2.5
20% diluted BCB	2 krpm	4.3 - 4.7	2.9 – 3.1	2.7 – 2.8
	3 krpm	—	2.0 – 2.5	2.0 – 2.2
			1.9 – 2.3	—
	3.5 krpm	—	1.8 – 2.0	1.5 – 1.7
			1.7 – 1.9	1.5 – 1.7**
	4 krpm	3.6 - 4.2	1.8 – 2.0	1.8 – 1.9
			1.5 – 1.6*	1.3 – 1.4*
30% diluted BCB	2 krpm	3.1 - 3.4	2.1 – 2.4	2.0 – 2.1
	4 krpm	2.1 - 2.4	1.3 – 1.6	1.3 – 1.4

*small test pieces & baking temperatures led to more variability
**measured on $\frac{1}{4}$ of 2" InP test samples with ridges and substrate vias

Fig. B.17 & B.18. To account for the thinner BCB, a reduced 60°C soft bake temperature was used. The exposure time and focus were also adjusted accordingly.

Unfortunately, despite the success with the test sample, the real sample ran into an issue during the development process. The sample came loose during the spin development. After discovering it miraculously did not break, the sample was rushed over to the post-development bake. Inspection showed that the development did not completely remove all of unexposed BCB. A BCB rinse solvent (T1100) was able to remove the remaining BCB residue, but some of the BCB patterns were distorted as shown in Fig. 4.11. After examining the sample with visible microscopy and SEM, it was determined that the distortions in the BCB BCB may lead to an increased capacitance for some devices, but it was acceptable for the sample to continue with processing.

While the sample looked acceptable after development, there was significant cracking in the BCB post-curing, as shown in Fig. 4.12. Since this was the only sample with

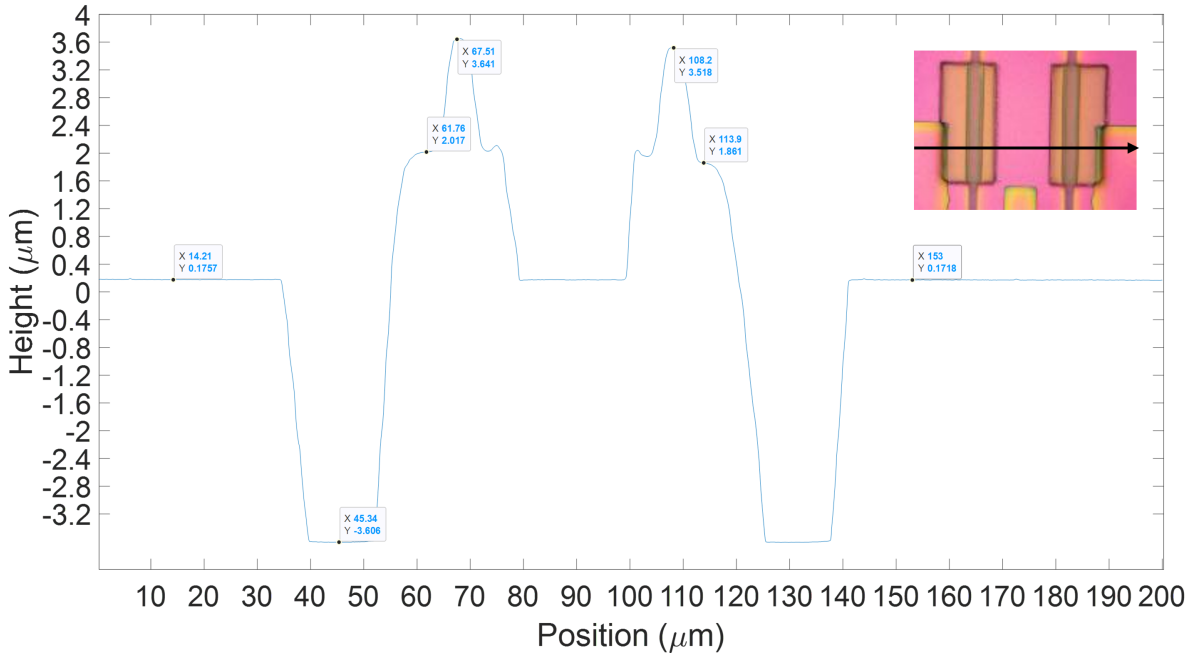


Figure 4.10: Test sample profilometer scan of BCB areas next to substrate vias

regrowth completed, a plan was devised to remove the cracked BCB and repeat the BCB patterning steps. The mask used for patterning the BCB area was repurposed to pattern windows in thick PR for etching the BCB. With the appropriate exposure time, the PR is developed in areas above the BCB, and there is still some filling the cracked areas, as seen in Fig. 4.13 (a). This will help reduce the over etching of the hard mask on the surface. The etch was successful in removing the BCB with only a few small issues. An outline of BCB was still present due to the way the distortions in the BCB expanded the shape. The etch also left some thin ribbons of dielectric and surface roughness which can be seen in Fig. 4.13(c). These minor flaws did not lead to any issues with repeating the BCB area steps on the real sample. Before applying new BCB, 75 nm of SiO_2 then 50 nm of SiN were deposited to replace the over etched hard mask. Figure 4.14 shows that BCB was successfully patterned and cured on the real sample. After curing, the BCB was encapsulated with 50 nm of SiN then 75 nm of SiO_2.

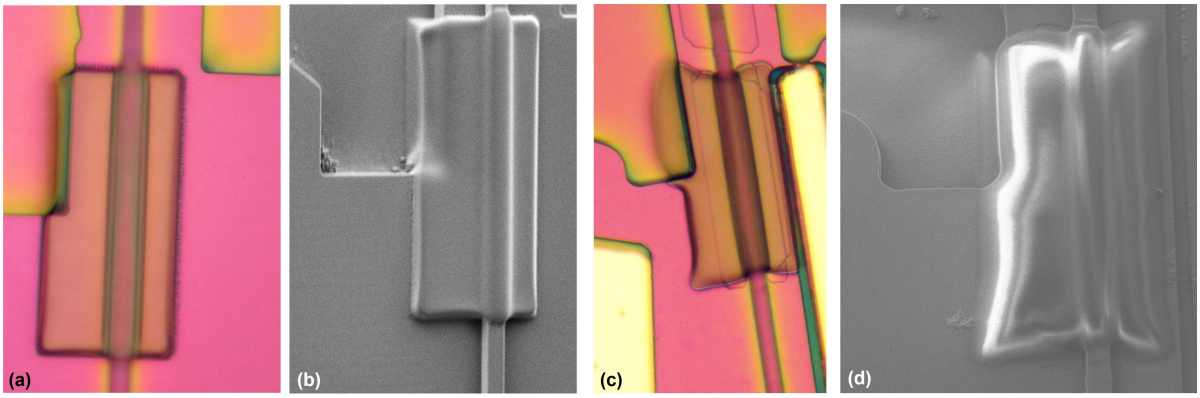


Figure 4.11: A test sample with good BCB is shown with (a) visible light and (b) SEM images. The real, epitaxial sample is shown in (c) - (d) with distorted BCB.

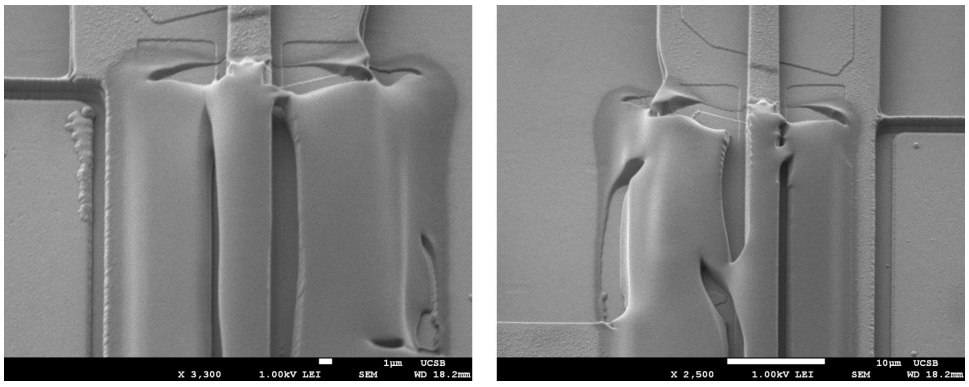


Figure 4.12: Real sample with cracked BCB after curing

4.2.12 Gen. 2 InP RX - BCB Vias

To expose the photodiode ridge top below the BCB for future p-contact metallization, vias must be etched. Similar to the gen. 1 RX, a larger BCB via was etched first, with a more narrow via through the dielectric being etched in a later step. The thinner BCB (only about 1 μm thick above the ridge) will avoid undercutting issues, and the via is only 1 μm wider than the ridge to reduce trenches forming from the etching effects described in Section 3.2.9. Using test samples, the recipe for etching the BCB was also improved. The recipe from gen. 1 used a 4:16 sccm CF_4:O_2 ratio which has undesirable roughness from micromasking that occurs during the etch. The "grass" formation during

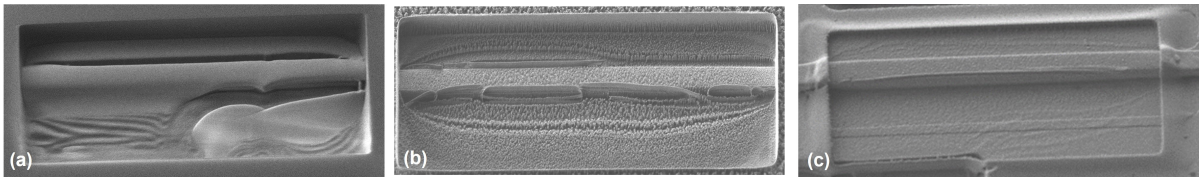


Figure 4.13: SEM images of real sample with (a) patterned PR for BCB removal, (b) partially etched BCB, and (c) completed BCB etch

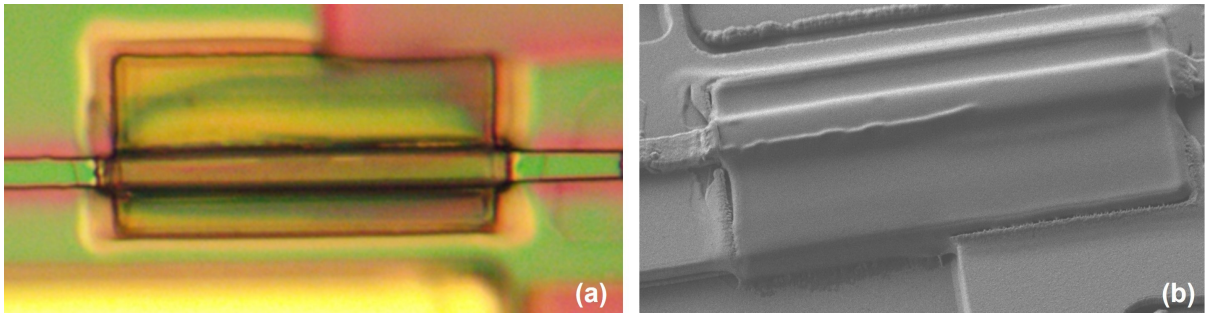


Figure 4.14: (a) Visible microscope and (b) SEM image of the new BCB on the real sample

the etch is apparent in Fig. 4.15 (c) as some reactants are redeposited on the surface or fluoropolymers form. The localized inward and outward flux of reactants and products is dependent on the geometry of the via and the fraction of masked area. Even in Fig. 4.15 (a) there is some roughness without any PR masking. Increasing the flow of CF_4 with a 6:14 ratio improved the etch chemistry, and reduced the roughness.

The mask for the narrow PD vias was also used for the BCB vias, but the defocus and exposure were calibrated to slightly enlarge the pattern to around 3 to 3.5 μm width. After optimizing the lithography, the improved etch recipe was followed for the real sample with good results, shown in Fig. 4.16. The roughness on the ridge tops was present from the BCB removal etch described in the previous section. This will be removed during the later p-via etching steps.

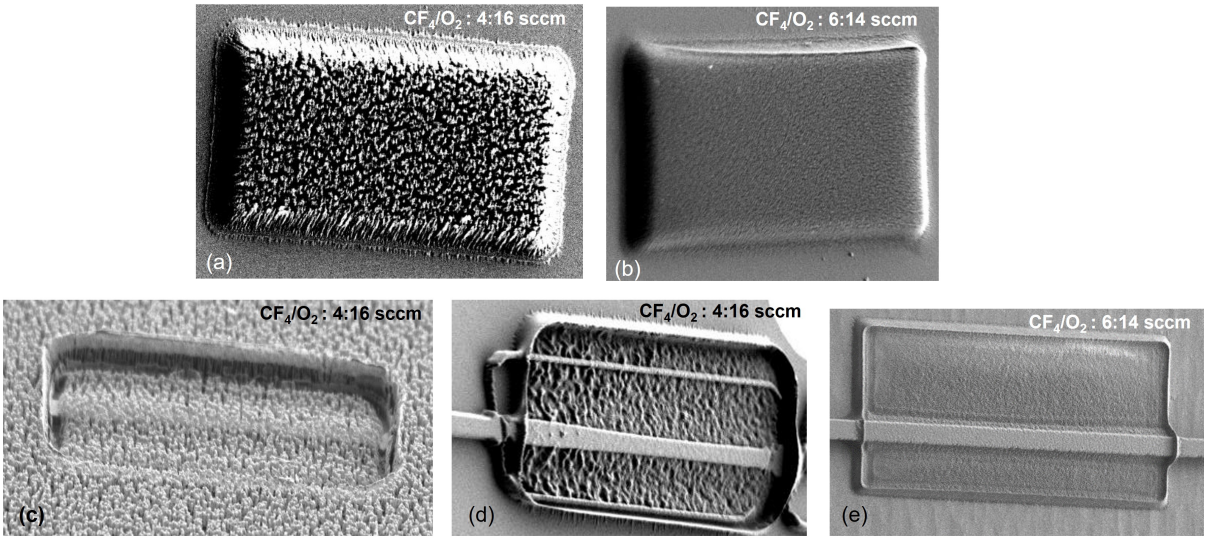


Figure 4.15: Unmasked BCB test sample etches using (a) 4:16 gas flow ratio show more roughness compared to (b) 6:14 ratio. When masked with PR, (c) the 4:16 ratio leads to grassy residue and a (d) rough surface after etching. (e) Roughness is reduced with the 6:14 ratio.

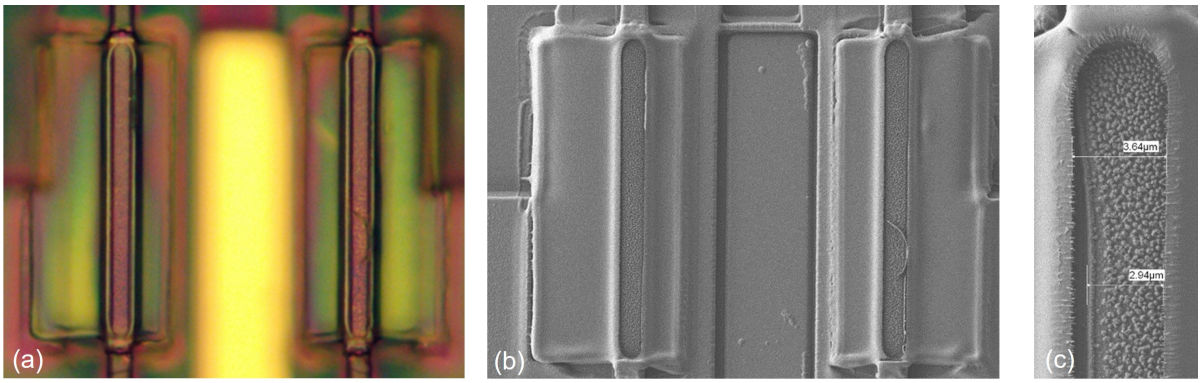


Figure 4.16: Wide view (a) visible microscope and (b) SEM images of etched BCB vias. (c) A close view shows via dimensions are good with some roughness

4.2.13 Gen. 2 InP RX - N-side Isolation Etch

The n-isolation etch was added midway through the processing as an alternative to a high energy helium implant for providing electrical isolation between the PDs and the laser cathodes. The plan for the helium implant was not examined carefully at the start of the process, so a simple 10 μm width outline was draw around the PD cathode area for isolation. Looking at literature on He implantation of n-type InP [229, 230], a strong helium ion implant can provide approximately 500 $\Omega - cm$ resistivity which will lead to about 2.2 M$\Omega/\square$ sheet resistance for the 2.3 μm thick n-InP cladding. The n+ InGaAs contact layer is more resistant to isolation, with literature showing only about 0.1 M$\Omega/\square$ for a 100 nm [231, 232]. With these layers in parallel, the resistor geometry must be at least 0.1 square to achieve a reasonable isolation resistance of 10 kΩ, though more would be preferred. The initial design with a thin outline in Fig. 4.17 is not sufficient. By implanting in the entire area around the n-vias, the resistor geometry is closer to an acceptable value of 0.35 square; however, implanting through the waveguides will induce optical loss. Based on previous work and discussion with Jonathan Klamkin, the optical loss from strong He implantation is on the order of 0.05 dB/μm [233, 81]. This would lead to an unacceptable loss of several dB in each of the arms using the large area implant.

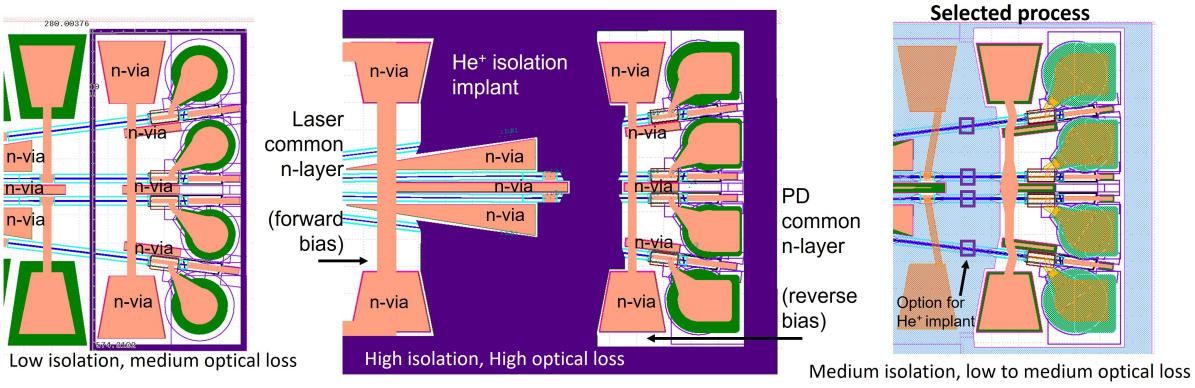


Figure 4.17: Three variations of the process for n-isolation with tradeoffs in isolation resistance, optical loss, and fabrication difficulty.

Using an etch to remove the n-cladding layers away from the optical waveguide will provide good isolation resistance without impacting the optical loss; however, there will still be a conductive path through the waveguides. Assuming the width of the MMI arms are between 3 and 4 μm and using estimated values of 290, 27, and 8.3 $\times 10^{-4}$ Ω-cm, for the resistivity of the InGaAsP WG core, InP n-cladding, and InGaAs contact, the arms will act as parallel resistors to yield approximately 500 Ω of total resistance. Material resistivity (ρ) is estimated using Eqn. 4.1 assuming the carrier concentration (n) is 90% of the doping concentration and using mobility μ estimates from [80, 234].

$$\rho = \frac{1}{q\mu n} \tag{4.1}$$

To achieve good isolation, implants are still required, but the optical loss can be minimized by only implanting around 10 μm of length. Assuming the resistance of the regions that have been etched to the substrate have MΩ level resistance due to the SI-substrate, the implants will add 100 kΩ resistors in series with each of the MMI arms, increasing the overall resistance to 25 kΩ.

With this plan, the mask and process steps for the n-isolation etch were designed. Test samples were used to calibrate the lithography defocus and exposure time and the time required for the InP dry etch. To keep the PD ridge and BCB protected during the 3 μm deep dry etch, another 200 nm SiN then 300 nm SiO_2 was added via PECVD. During the hard mask etching process, a issue with incomplete etching in small corners was discovered after removing the photoresist, seen in 4.18. This was difficult to see with the thick photoresist still on the sample. To fix the issue, the lithography was repeated, and a short etch was run. Unfortunately, the repeated etch with about 200 to 400 nm of misalignment from the first lead to some etched of the dielectric on the sidewalls, causing some of the layers to peel off in multiple places.

The ribbons of dielectric that peeled off the sidewall could not be removed without

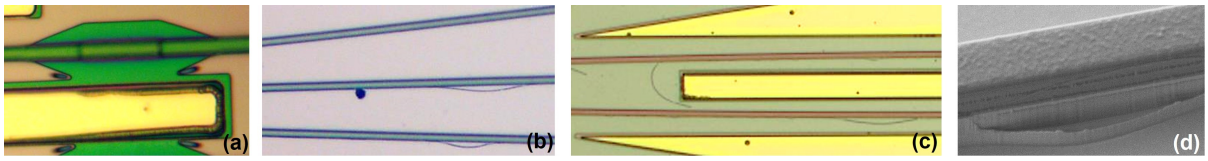


Figure 4.18: Issues were encountered with (a) incomplete hard mask etching in tight corners and (b) - (c) hard mask peeling after repeating the etch. (d) Thin InP structures were etched from the peeled sidewall masking.

damaging the other structures, but they did not pose a major risk to the processing. They created thin etched structures during the InP dry etch as shown in Fig. 4.18(d), but these are far enough away from the optical mode that there will be very minor impact on scattering loss. Otherwise the dry etch was successful using the Oxford cobra standard InP etch recipe. The deep etched areas can be seen in Fig. 4.19. After the InP etch, a blanket dielectric etch was used to remove most of the remaining hard mask used for the etch in an effort to manage the overall thickness of the dielectric. The etched sidewalls were then passivated with 75 nm of SiO_2 then 50 nm of SiN.

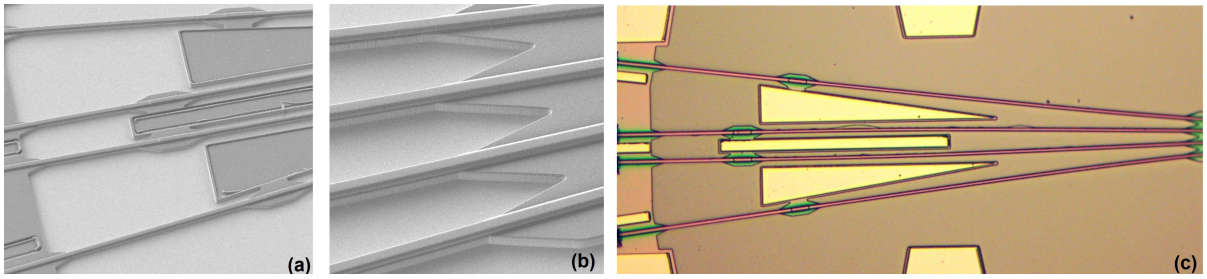


Figure 4.19: Images of the completed etch using (a) - (b) SEM and (c) visible microscopy

4.2.14 Gen. 2 InP RX - Vias to N-contact Metal

After the n-side isolation etch, the resistance was examined by etching vias through the dielectric layers to expose the previously deposited pad metal. This was a simple dry etch process with ICP #2. The resistance between different n-metal locations was measured using needle probes and a multimeter, with the results shown in Fig. 4.20.

Measurements were not aligned with the expectation for the isolation between the PDs and the laser cathode, with only 120 to 130 Ω resistance. After measuring only around 600 Ω between the laser cathode and isolated n-metal mesa, it was clear that there was some issue with the isolation provided by the substrate or that the etch was not deep enough. The isolation etch depth and the depth of the n-InGaAs layer were double checked, but they did not show discrepancies.

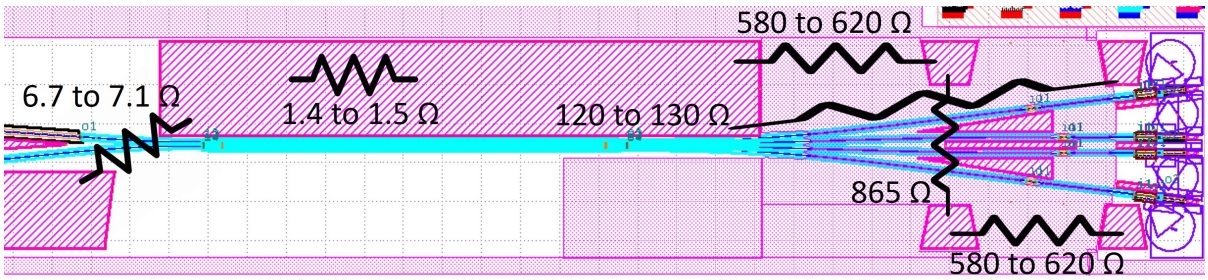


Figure 4.20: Isolation resistance measurements on real sample.

The next section describes the steps taken to examine this issue further which ultimately led to the decision for a second, deeper isolation etch. The dielectric etch step was repeated with a modified lithography recipe to account for the increased surface topography and a shorter etch time to again remove the hard mask used for the deeper etch. As shown in Fig. 4.21, the isolation resistance between the PD and the laser cathode was aligned with the expected 500 Ω after the deeper etch, though the 11 kΩ resistance between the n-metal mesas was still much lower than expected for a SI-InP substrate.

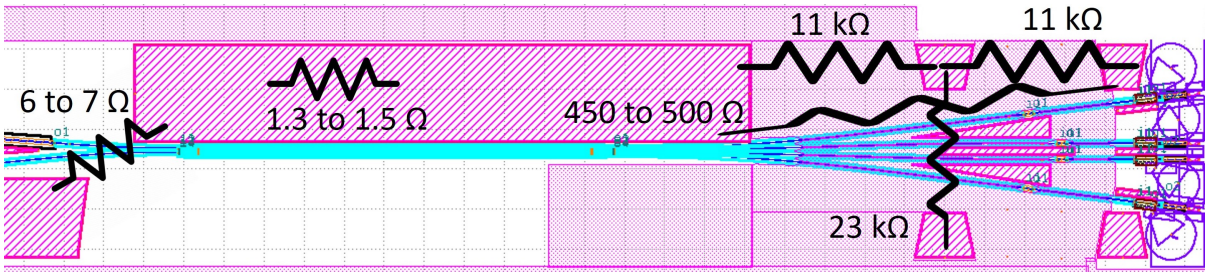


Figure 4.21: Isolation resistance measurements on real sample after deeper etch.

4.2.15 Gen. 2 InP RX - Isolation Testing

To examine the low isolation resistance further, a large piece of a broken epiwafer was used to conduct a study on the isolation resistance with increasing etch depth. The n-side isolation etch of the hard mask was completed, and then the sample was cleaved into several smaller pieces to test the resistance with progressively deeper etches. The tests showed similar results to the main sample with a 4 to 5 μm etch depth, but the pieces with etch depths >6 μm showed close to the expected resistance. The reason for this is not certain, but it could be related to defects or vacancies in the substrate that increase the native donor concentration or to poor electrical activation of the Fe dopants that create the deep acceptor traps levels which help neutralize the native n-type conductivity of undoped InP [235, 236, 237, 238].

SIMS analysis on the InGaAsP composition, Si doping, and Fe doping concentrations was conducted on pieces from a broken sample with the 4 QW epitaxy shown in Table 4.1 and an 8 QW piece from the same wafer order with a slightly different InGaAsP WG layer composition and Si doping. Analysis for the Si dopant concentration was used to verify that Si was not present in the SI-substrate, leading to low resistance. Figure 4.22 shows that the Si concentration drops to the noise level at 3 μm below the InP cap layer from the base epitaxy which matches the designed stopping point of the n-cladding. Checking the Fe concentration shows that it ramps up to 1 to 2 $\times 10^{16}$ cm^{-3} at the expected 3 μm depth. This concentration is reasonable for producing SI-InP with resistivity in the range of 1 MΩ-cm, but it might not be sufficient if there the concentration of donor defects is higher than average. Without more detailed materials analysis, it is difficult to definitively confirm the cause of the low isolation. Since the increased etch depth on the test epiwafer pieces led to the expected resistance values, a deeper etch was planned for the main epiwafer sample.

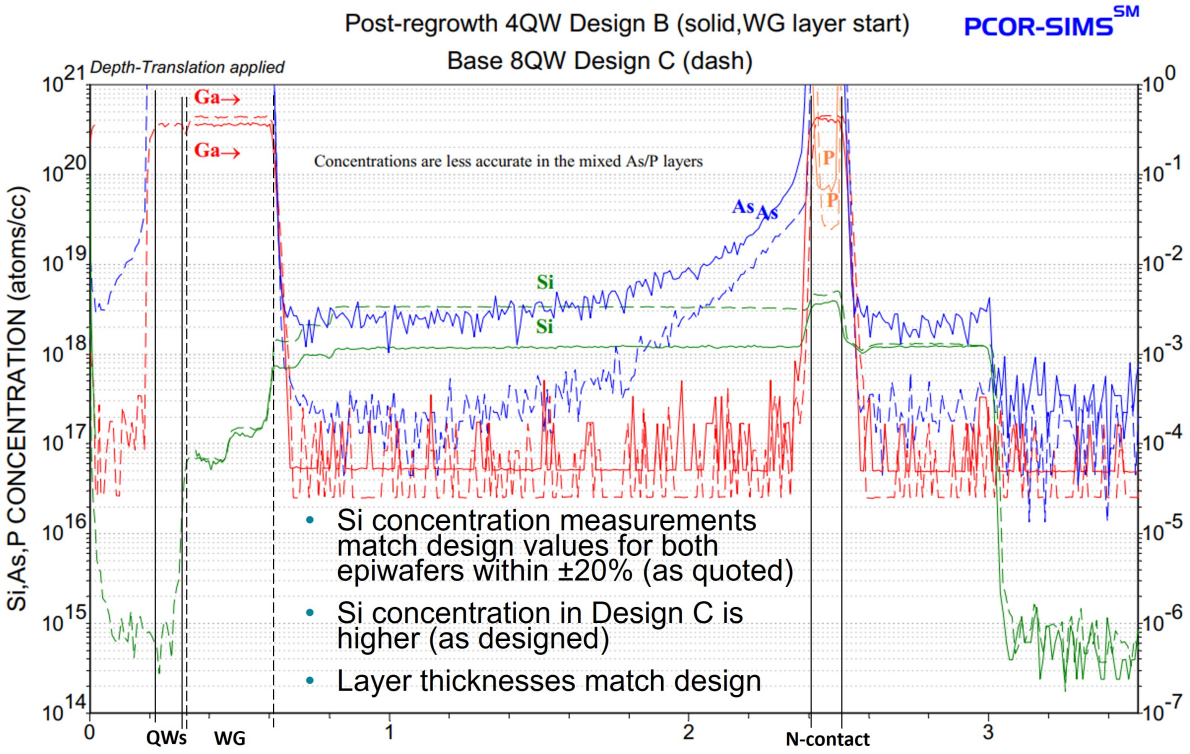


Figure 4.22: SIMS data to examine Si doping profile in epitaxial layers and top part of SI-substrate for the two epiwafer pieces.

4.2.16 Gen. 2 InP RX - N-side Isolation Deep Etch

The layout for the deep isolation etch is a slight modification of the first isolation etch. To avoid additional etching of the dielectric on the sidewalls, a buffer of 1.25 μm is used to move the edges of the deep isolation etch away from the first etch. This buffer is sufficient to account for slight misalignment of the pattern and PR patterns that are more narrow than designed after development. For the deeper etch, 200 nm SiN then 400 nm SiO_2 was added via PECVD as hard mask. To avoid issues with capacitance from the top part of the substrate, the PD substrate vias were also etched deeper. The etch was completed successfully, and it increased the laser to photodiode resistance to the expected level as shown in Fig. 4.21. However, the increased surface topography that is shown in Fig. 4.24 made the later lithography steps much more difficult to calibrate.

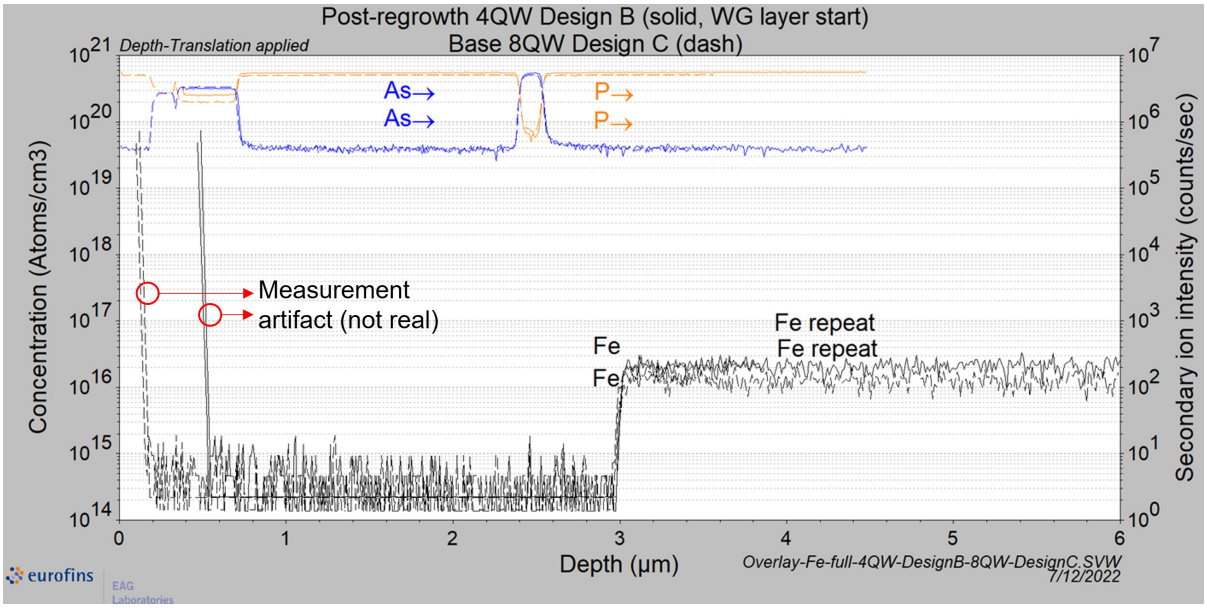


Figure 4.23: SIMS data to examine Fe doping profile in epitaxial layers and top part of SI-substrate for the two epiwafer pieces.

4.2.17 Gen. 2 InP RX - Vias to P-InGaAs

To contact the p-InGaAs, the protective dielectric layers and the InP cap need to be removed in a p-via process. A narrow direct via pattern was used for the photodiodes while an SSA process was used for the rest of the ridges. Calibrating the exposure time for this step was a challenging and time consuming procedure. Due to the localized changes surface topography, the photoresist thickness varied significantly in different areas. This made it necessary to split the patterns for this step into multiple exposures. Figure 4.25 shows how the areas with deep etched trenches create more variation in the thickness of the photoresist above the ridge. The small bumps in Fig. 4.25 (a) correspond to the four ridges. The difference in the height of small bumps shows that the PR thickness is varying by >1 μm. Most of the non-uniformity was compensated by splitting the SSA layout into 5 different exposures. Using the SSA isolation mask, test exposures were run to examine how much exposure time was needed for different parts of the layout, identifying 5 main subsections. During the process of testing the local alignment procedure, the stepper

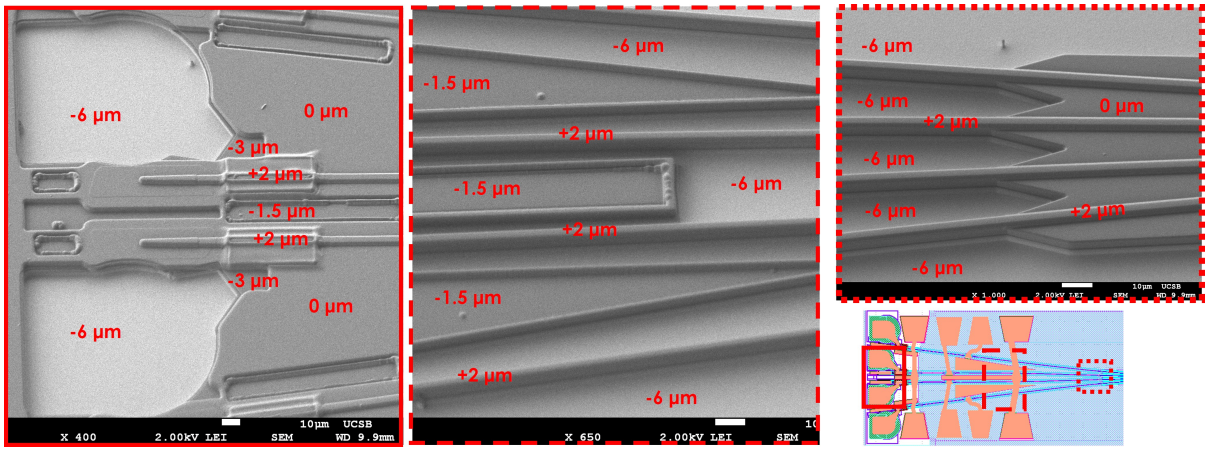


Figure 4.24: SEM images of the main sample after the deep isolation etch with depth labels showing the high variability in surface topography.

was not able to correctly map the local alignment marks and apply the corrections. The thickness of the total dielectric layers had increased the width of the marks by >50% and rounded the corners which would make the mark identification more difficult and less accurate for the stepper. The thick photoresist could also be making the mark more difficult to identify. Both of these issues were fixed using the maskless aligner MLA150 to pattern windows over the alignment marks for a BHF wet etch to remove the dielectric. In the next set of lithography testing, the MLA was used to create windows through the thick photoresist for the stepper to more clearly see the local alignment marks. These were developed first, and the stepper was used to expose the rest of the p-via patterns which were subsequently developed. This procedure with two developments presented issues with incomplete and inconsistent pattern development for the p-vias. After some process debugging and discussion with Brian Thibeault, it was determined that the first development step was changing the surface chemistry which led to poor wetting of the surface during the second development. A test without the first development showed that the stepper was able to perform the local alignment through the thick photoresist now that the alignment marks were sharper.

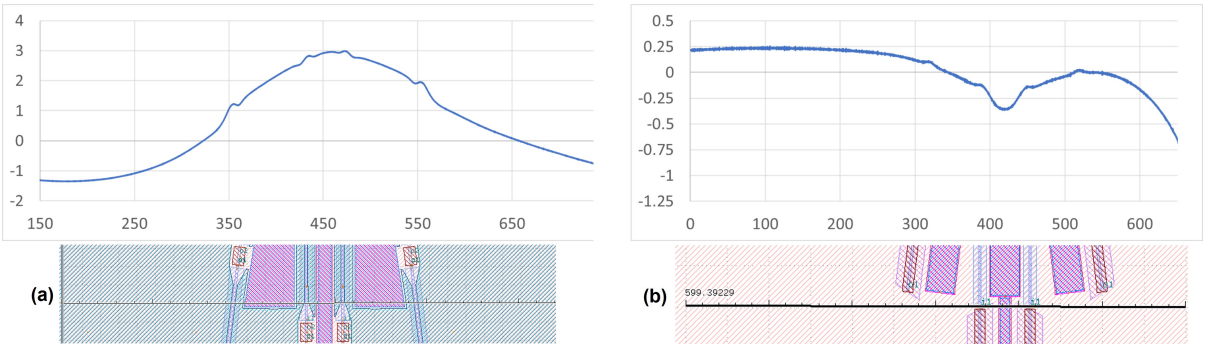


Figure 4.25: Surface profile scans are shown with a corresponding layout image to show the large non-uniformity of the photoresist in (a) areas with the deep etching compared to (b) areas without it.

The final procedure used Stepper 2 with 5 exposures for the p-via and 1 exposure with precise local alignment for the PD-vias, then all of the patterns were post-exposure baked and developed. For thick photoresist, it is important to wait close to 1 hour for the photoresist to rehydrate and complete the photochemical reaction. Nitrogen bubbles can form and distort the exposed patterns if the waiting time is too short. Another issue with thick photoresist is the large edge bead that forms, especially with small and non-circular pieces, like the 1/4 of 2" wafer pieces being used. One technique for reducing the edge bead is to use blank InP 2" wafer pieces to create a full wafer during photoresist spinning, as shown in Fig. 4.26. For the best effect, the edges of the pieces must be touching or very close together, so it requires a steady hand and some practice to be proficient with the technique.

The dielectric etching was performed with the Fluorine ICP using a combination of pure CHF_3 and CF_4/CHF_3 plasma etching with periodic O_2 plamsa polymer cleaning. The color of the ridge tops was examined after each etch step to monitor the progress of the etch. Due to the additional steps to redo the BCB and etch the n-cladding deeper, the top hard mask thickness was close to 1.2 μm. Even after splitting the SSA lithography into 5 exposures, there was still some non-uniformity which lead to etching

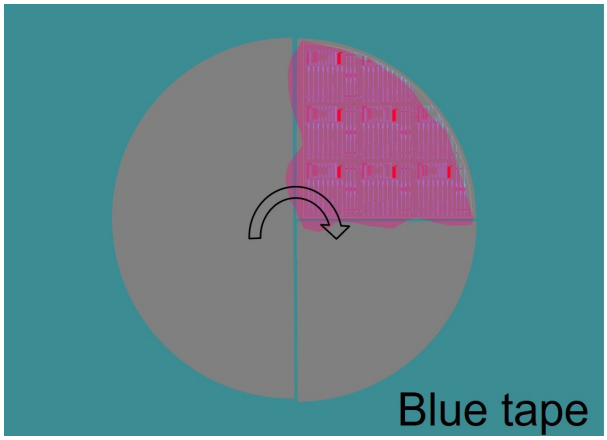


Figure 4.26: Diagram showing wafer spinning technique for edge bead reduction.

of the dielectric next to the ridges. The over etching mainly occurred for the MMI output attenuators, some test structures, and the deep etched ridge tops, as shown in Fig. 4.27. Partway through the etching, the PR was removed to inspect the over etching and the lithography was repeated. The etch was complete when the ridge tops showed a uniform white color, as seen in Fig. 4.28, indicating the the InP cap layer was completely exposed. Due to the anisotropic dry etches used for thinning the hard mask in previous steps, the sidewall dielectric was able to accumulate with a thickness closer to 1.7 μm, as shown in Fig. 4.28 (c). The InP cap was removed with a $1HCL : 3H_3PO_4$ wet etch, monitoring the surface roughness until it was smooth.

4.2.18 Gen. 2 InP RX - P-Metal Deposition

The patterned p-via photoresist was used for the thin p-contact metal liftoff, similar to the gen. 1 RX process in Section 3.2.6. A test sample was used to practice the liftoff which showed that the rough surface of the plasma etched PR made liftoff more difficult and could potentially trap some PR residue underneath the metal. To avoid this issue, the PR on the real sample was etched back until it was removed in the SSA openings. The test sample also showed that there would be some metal deposited on the sloped

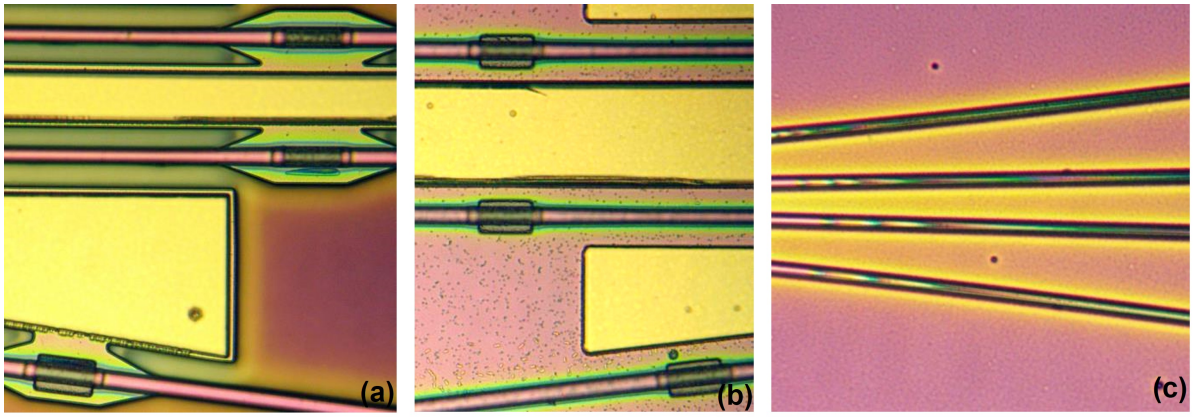


Figure 4.27: Photoresist non-uniformity led to over etching in multiple areas including the (a) RX PIC hybrid output attenuators, (b) MMI test structure attenuators, and (c) the tops of the deep etched ridges

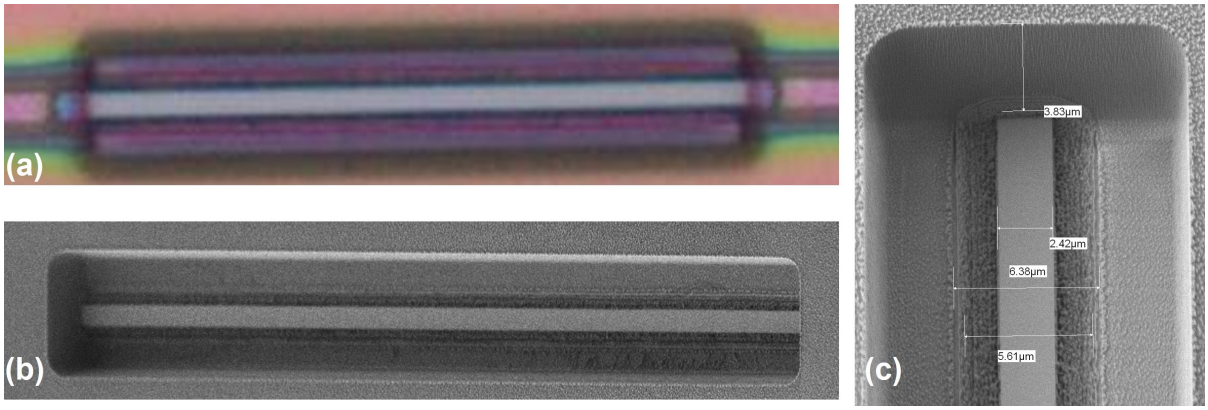


Figure 4.28: The uniform white color of the InP ridge can be seen with (a) visible microscope and (b) SEM images. (c) SEM measurements show the large width of the etched sidewall dielectric layers.

sidewalls of the PR. This was able to be removed by gently wiping the surface with a loose cotton swab soaked in isopropyl alcohol. On the main sample, UV ozone and diluted BHF cleaning were performed, and the sample was immediately loaded into e-beam #3 for top down deposition of 20/40/120 nm of Ti/Pt/Au. After after soaking in acetone for liftoff, residual metal that was deposited on the PR sidewalls, seen in Fig. 4.29, needed to be removed.

After carefully wiping the surface to remove the excess metal, the sample was rapid

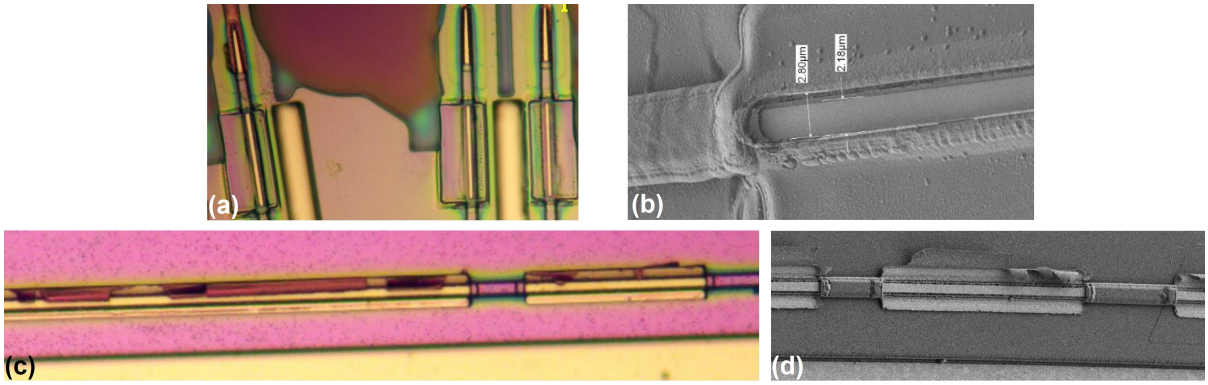


Figure 4.29: The PDs showed a clean liftoff in (a) visible microscope and (b) SEM images while the laser sections showed sidewall metal still attached in (c) visible and (d) SEM images.

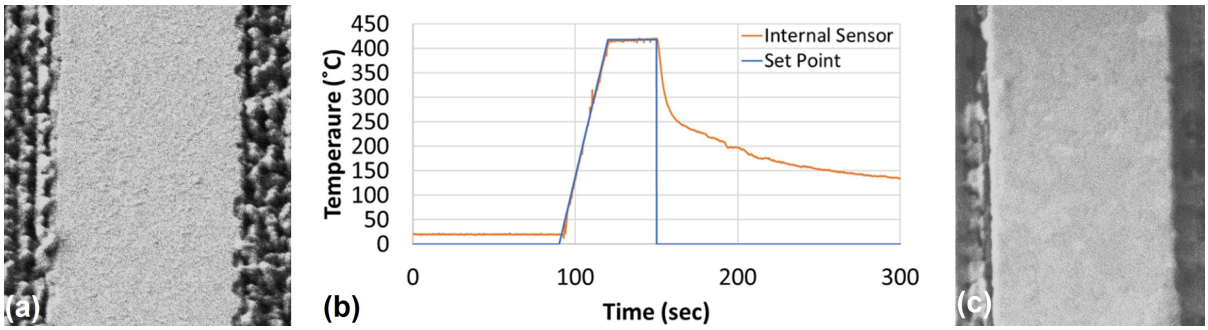


Figure 4.30: (a) The surface texture is rough after deposition. (b) The RTA temperature profile peaks at 420°C. (c) A smooth surface and grain growth are seen after annealing.

thermal annealed at approximately 420°C for 30 seconds with forming gas flowing at 1 slm (1000 sccm). Figure 4.30 shows the change in surface texture from grain grown during the anneal and the temperature profile of the annealing process.

4.2.19 Gen. 2 InP RX - Pad Metal Deposition

The pad metal deposition used a bi-layer liftoff process with LOR 30C and SPR220-3. Several lithography experiments were conducted using test samples with similar topography to the real sample in order to optimize the process steps without accumulating residue or risking damage to the main epitaxial sample. A thick layer of PMGI or LOR

was required to cover the ridges inside the deep etched area. Initial tests used multiple layers of PMGI SF-15, but there were issues with bubbles forming around the edges of the deep etched area, as shown in Fig. 4.31. After some discussion and literature review, an experiment was run where the sample was immediately baked after spinning the PMGI layer. The interference patterns in Fig. 4.31 (a) are from PMGI peeling away from sharp corners as the solvent slowly evaporates, and they will expand into bubbles after baking [226]. By minimizing the time between spin and bake, this issue can be avoided.

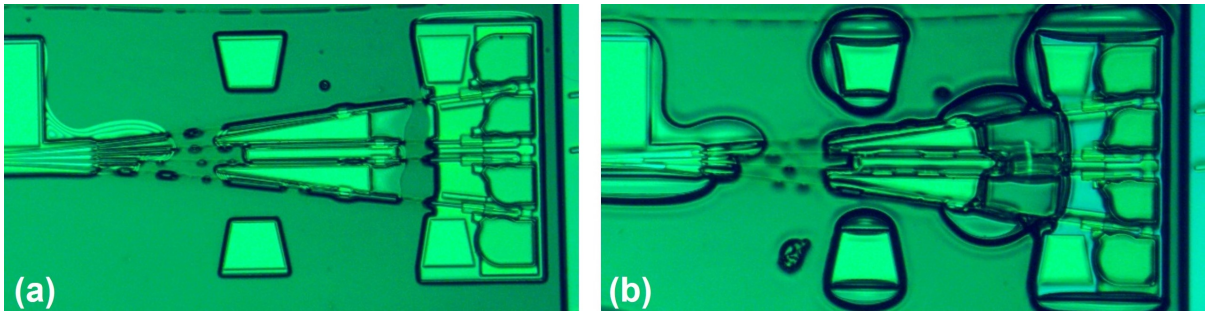


Figure 4.31: SF15 spun on a test sample (a) before and (b) after a 170°C soft bake

After solving the problem with the bubbles, deposition experiments were completed to examine the thickness and angle required for good surface and ridge sidewall coverage. To avoid high current density, a sidewall metal thickness of >300 nm was desired. An initial test used a 45° tilt relative to the source with the sample positioned 24 cm away, resulting in sidewall deposition rate roughly 0.80 times the value from the crystal monitor ($2.25 \times 0.71 \times 0.5$). This rate is the result of the inverse square relation for deposition flux, the angle to the source, and the roughly 50% time facing the source. The crystal monitor, at $\approx$ 36 cm from the source, was set to deposit 30/700 nm of Ti/Au which resulted in metal coating the sidewalls of PMGI, seen in Fig. 4.32, despite the 1 to 1.5 μm undercut. While the thin residual metal was able to be cleaned up after the p-contact, the metal on the PMGI sidewalls is >5 times the thickness, making it difficult to remove. It was evident that a larger undercut was needed for a clean liftoff.

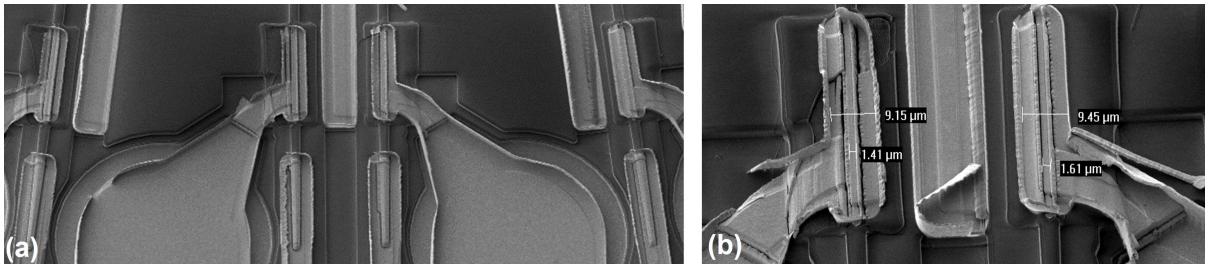


Figure 4.32: SEM images of (a) metal in PD vias and (b) on top of BCB after a test pad metal deposition.

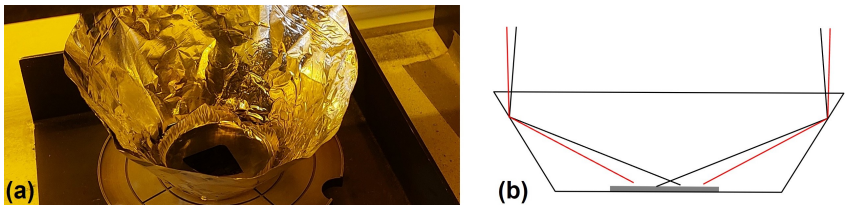


Figure 4.33: (a) A reflector cone is used for increased undercut. (b) The diagram shows reflected light rays with incident angles that can be absorbed for a deep undercut.

To increase the undercut, LOR 30C was used instead of PMGI SF15 for its higher undercut rate, based on the data sheet. While this improved the undercutting, it was not sufficient to achieve the desired ≈5 μm undercut. This deep undercut is needed to shield the sidewalls of the ≈5 μm thick LOR during metal depositions at a 45° angle. The limiting factor for achieving deeper undercut is the absorption of the deep UV light. With top down illumination in the deep UV flood exposure tool, the LOR in deep undercuts is shielded from the light by the top photoresist. Using a reflector, as shown in Fig. 4.33, the LOR in the undercut will receive more light, enabling a deeper development of the undercut.

With a recipe capable of deeper undercutting, the pad metal layout was altered to shrink some patterns and increase the spacing in several areas. Increased spacing is required to avoid undercutting between p- and n-side pads which could lead to shorted devices. It also ensures that the top PR is supported, so that it doesn't collapse and lead to poor lift off. The final process for spinning and baking is shown in Appendix

B in Fig. B.19. With the recipe finalized, the calibration for the dose and defocus was completed using a test sample with the Heidelberg Maskless Aligner (MLA). Although the thick LOR helps to planarize the surface, there is still enough non-uniformity to require multiple exposures. Figure 4.34 shows undeveloped photoresist where the deep PD vias lead to a thicker layer. The patterns were split up into 3 groups: main pads, PD top metal, and deep pads to optimize the dose and exposure. The final developed patterns on the main sample are shown in Fig. 4.35 with completely developed PR and deep undercuts.

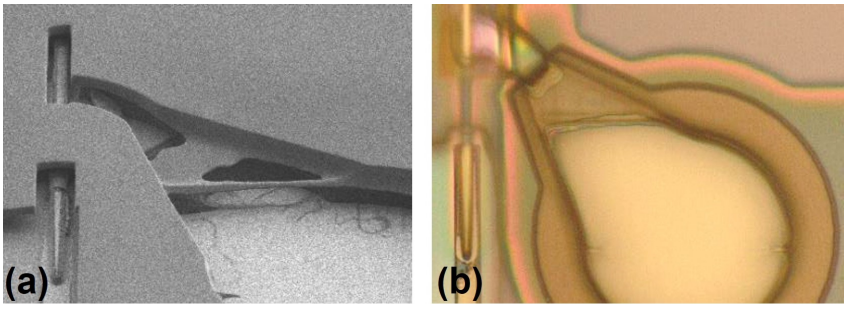


Figure 4.34: Undeveloped PR from thickness non-uniformity is evident in (a) SEM and (b) visible microscope images.

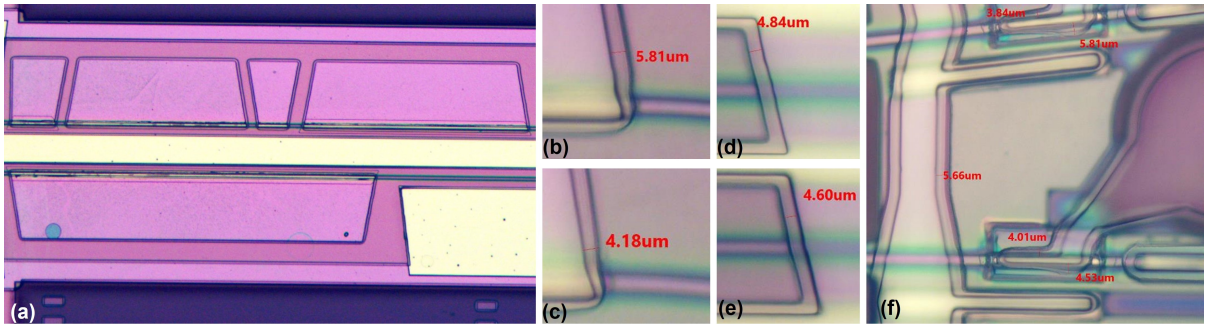


Figure 4.35: (a) An overview of the pad metal patterns for the laser with large undercuts is shown with close views of (b)-(e) measured undercuts for the laser area and (f) the photodiode area.

The details of the pad metal deposition are also included in Appendix B, Fig. B.19. During initial tests there were issues with poor metal adhesion, so a final test was conducted where the metal source was heated a couple of times to burn off surface residue.



Figure 4.36: Stitched image of the main sample after completing the pad metal deposition

Wirebonds were then made on the test sample to ensure a strong metal adhesion. This process showed good results, so it was repeated on the main test sample. Figure 4.36 shows one of the RX PICs from the main sample after a successful deposition and liftoff.

4.3 Gen. 2 InP RX - Device Testing

After liftoff, the I-V characteristics were measured to examine the turn-on voltage and the series resistance (R_{series}), expecting similar behavior to the gen. 1 InP results from Fig. 3.35. Unfortunately this was not the case, with few devices exhibiting I-V behavior close to the expectation. Many devices exhibited one of two types of erroneous behavior: low turn-on voltage or high R_{series}. Example measurements of devices with low turn-on as shown in Fig. 4.37 (a), and high R_{series} devices are shown in Fig. 4.37 (b). The R2C1 labeling corresponds to the row and column of the die on the sample while the d# corresponds to one of the 8 PICs on each die.

After testing devices from multiple dies and finding only a few diodes with reasonable performance, another thermal anneal was conducted at 420°C for 30 seconds to help reduce the series resistance. As shown in Fig. 4.38, measurements on high R_{series} devices showed some small improvement after the anneal while devices with lower R_{series} showed a negligible change.

After measurements showed a slight post-anneal improvement, the anneal at 420°C was repeated with a 60 second duration to see if the resistance continued to decrease. Devices with peak currents on the order of 0.1 mA showed an order of magnitude im-

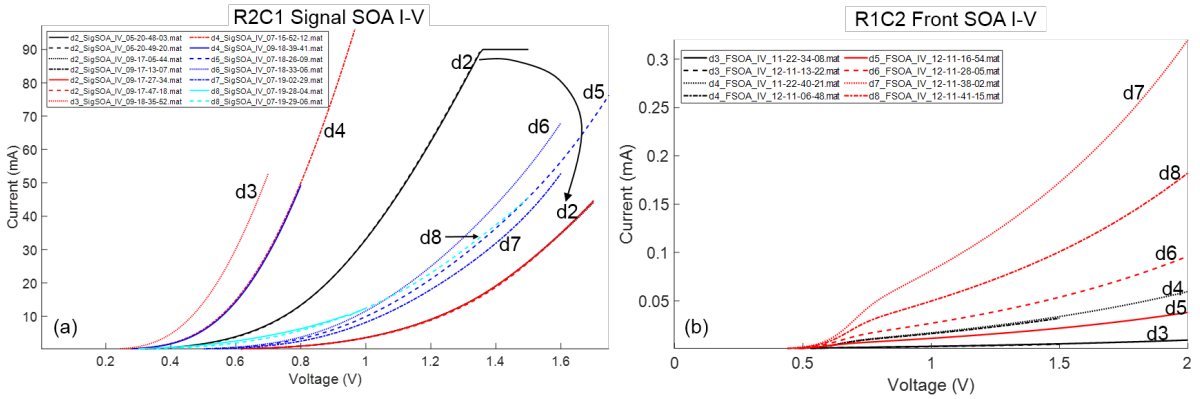


Figure 4.37: Initial I-V measurements for (a) R2C1 signal input SOAs and (b) R1C2 front SOAs, showing poor electrical behavior for InP diodes

provement, as shown in Fig. 4.39 with peak currents now in the 1 mA range at 2V, but this is still much higher than the desired <10 Ω R_{series}. Many other devices did not exhibit significant improvements with peak currents <0.1 mA at 2V. The devices with a high peak current and a low turn-on voltage showed a slight increase in the turn-on voltage after the longer anneal, seen in Fig. 4.40. A potential explanation for the behavior of these devices is a high resistance InP diode in parallel with a low resistance diode which has a lower built-in voltage. These devices are likely the result of a Schottky diode forming where the surface dielectric was over etched during the p-via process step, as was shown in Fig. 4.27.

Another method for improving resistance on individual devices is to use low duty cycle, high current electrical pulses. Electropulsing has been used to improve the performance by altering the microstructure of the material through a combination of Joule heating and the electron wind force. The forces exerted on the lattice structure during the pulse can help to recrystallize the material, repairing vacancy and dislocation defects [239, 240]. This process has been shown to repair degradation in Schottky [241], Zener [242], and laser diodes [243]. While this process showed modest reduction in resistance (1.5 to 2×) for some devices, it damaged other diodes, creating resistors. After limited

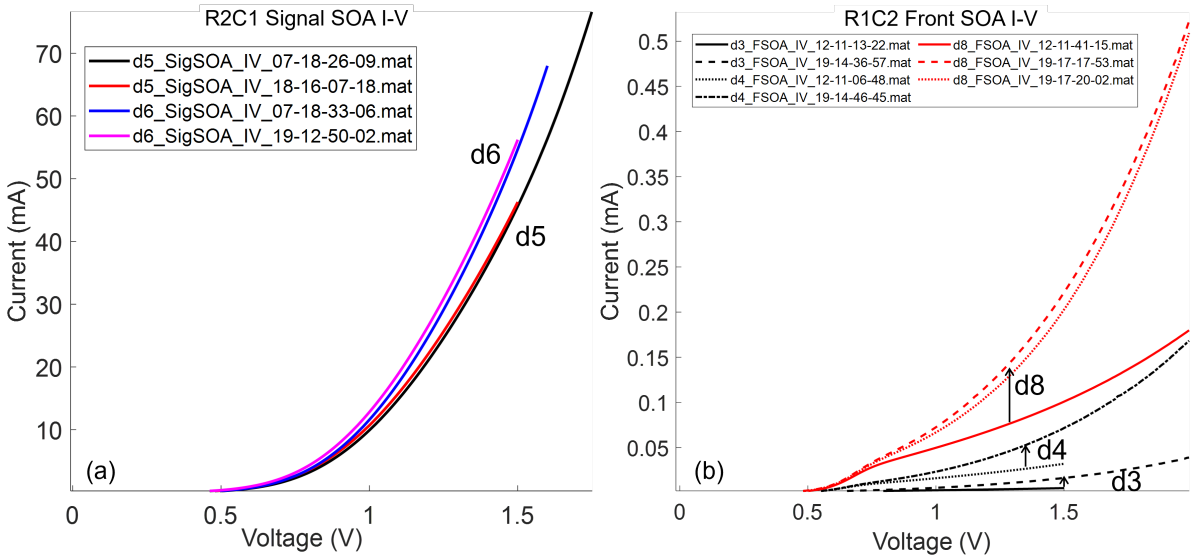


Figure 4.38: I-V measurements before and after 420°C RTA for (a) R2C1 signal input SOAs and (b) R1C2 front SOAs, with arrows showing slight improvement in R_{series}

success from the electropulsing, a final anneal at 430°C was run for 15 seconds as a last attempt to improve the devices, but this did not yield a major improvement.

It was evident that there was a significant issue with the material properties of the contact and possibly the cladding material. Resistance measurements were taken between the diodes which showed much higher than the expected values. Example results can be seen in Fig. 4.41. Based on the doping and mobility model from [80], a resistivity of 0.0087, 0.097, and 0.16 Ω-cm were estimated for the 10^{19} doped p-InGaAs, 10^{18} doped p-InP, and 5×10^{17} doped InP. Treating the layers are parallel resistors, the net resistance of was calculated to be about 140 Ω/μm and 240 Ω/μm for the ridges with and without the p-InGaAs layer. With 15 to 25 μm long isolated sections between devices, the expected isolation resistance is <10 kΩ compared to the >50 kΩ that was measured. There were several devices like the example shown in Fig. 4.41 (c) where the back mirror and front SOA had relatively low contact resistance after annealing, but the gain section and front mirror showed R_{series} >1 MΩ. This enabled a measurement through a longer length of the ridge, and supported the theory that the material resistance was higher than expected.

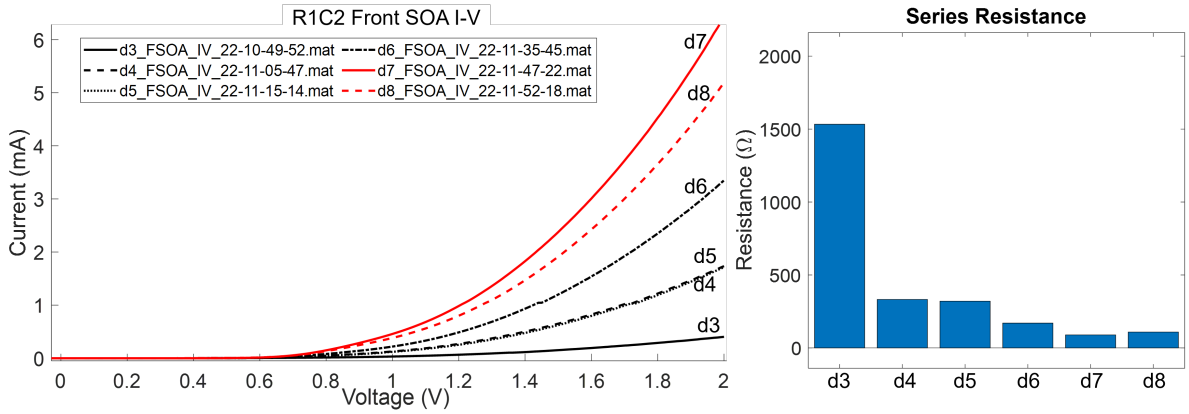


Figure 4.39: (Post 420°C +60s) I-V measurements for R1C2 front SOAs with calculated series resistances.

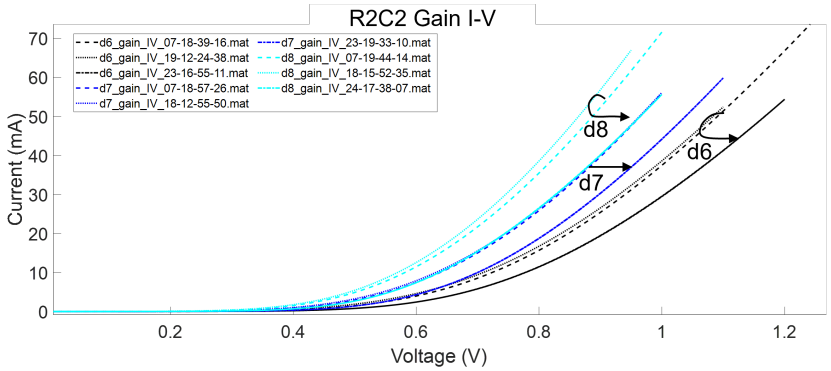


Figure 4.40: I-V measurements showing a slight increase in the turn-on voltage after the second anneal.

For the devices with R_{series} low enough for a few mA of current below 2V, the spontaneous emission was examined to understand the distribution of the current. Figure 4.42 shows that all of the SOA devices exhibited poor emission uniformity. This suggests that the annealing created a localized region of lower resistance where the current is channeled, reinforcing the low resistance path. It is curious that all the SOA devices tested showed emission only near the edge of one side. There were a few other active regions in the Fabry-Perot lasers and 90°hybrid test structures which showed emission with better uniformity. Since part of the material was able to emit light, it suggests that the QWs were operating as expected, but there carriers were not able to reach the QWs

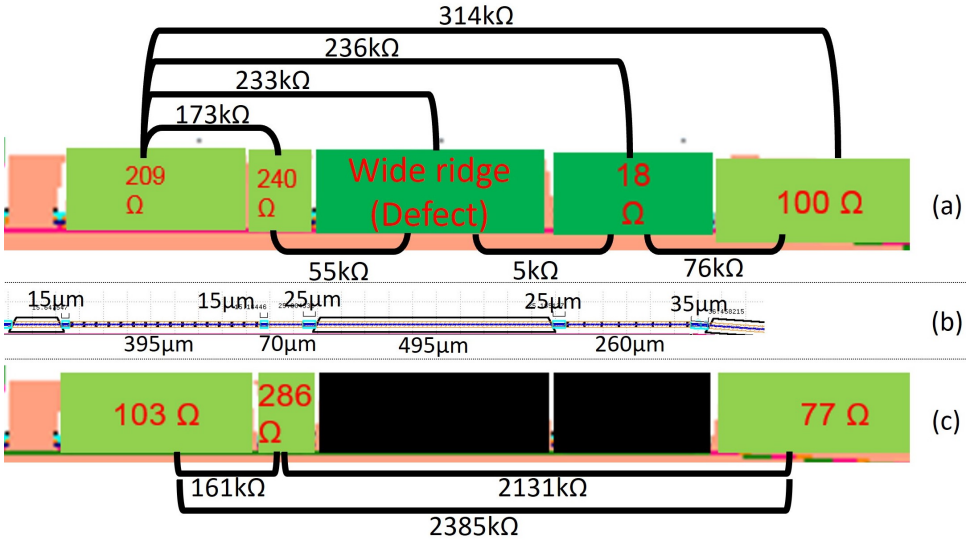


Figure 4.41: Resistance measurements are shown (a) between lasers sections which all had low R_{series} with (b) measurements for the length of each section. (c) Resistance measurements are shown through ridges with R_{series} >1 MΩ.

across most of the SOA length. A thermal imaging microscope (QFI Infrascope) was also used to examine the heating from the current with examples shown in Fig. 4.43. This revealed the same non-uniform distribution as the IR emission in the devices with low turn-on voltage.

It is not clear whether there is a primary cause for the high resistance and poor current uniformity issue. Assuming the regrown material was doped as expected, the cladding layers must have been damaged in some way during the fabrication to induce the high resistance through the ridge. Ion bombardment from long exposures to plasma etching during the SSA steps, mechanical stress from the thick dielectric layers, thermal stress, or diffusion of carbon or silicon contamination are possible ways that the ridges could be damaged. For the contact layer, it is possible that a thin oxide layer could be preventing current flow. Surface cleaning steps prior to p-contact deposition for the InP were used to remove oxides, but it is possible they were not effective enough. The oxidization of Ti during deposition is another possible way a insulating layer could be

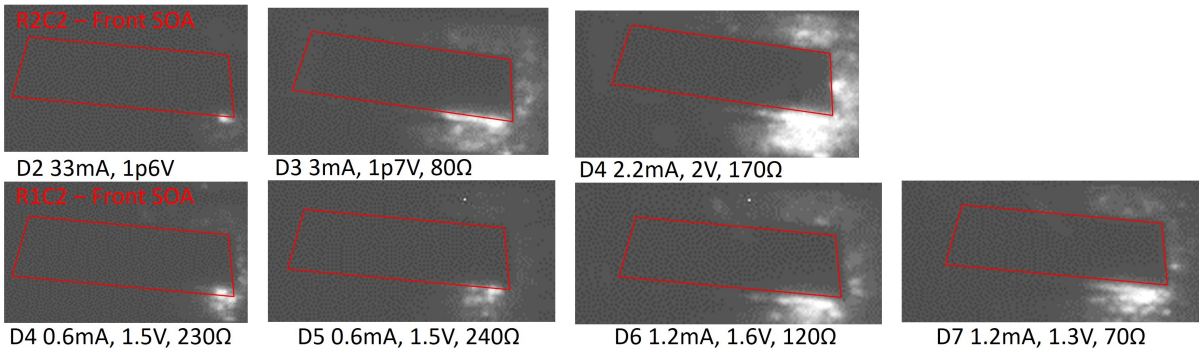


Figure 4.42: IR camera images of SOA regions showing spontaneous non-uniform spontaneous emission.

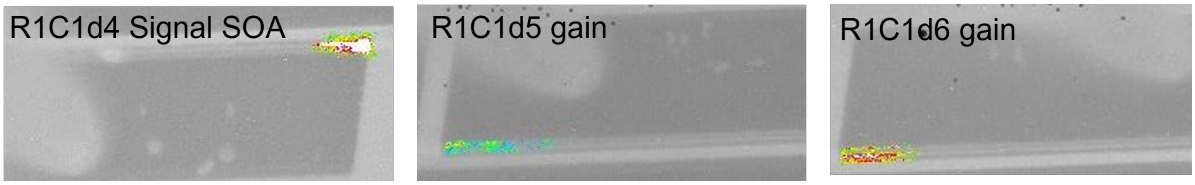


Figure 4.43: Thermal camera images of hot spots in diodes with low turn-on voltage showing the current is concentrated non-uniformly.

blocking current flow. This seems unlikely for e-beam #3 since the metal sources as kept under a constant vacuum, but it is possible for e-beam #1 where the entire chamber is vented.

4.4 InP PIC Processing Challenges, Lessons, and Recommendations

While the second generation InP receiver was originally intended as a incremental improvement from the first generation, the complexity of the fabrication, the amount of new process development, and the incomplete design analysis added significant challenges and risks. In this section, I will summarize some of the major challenges, mistakes, and lessons for future fabrication.

In a complex project, continuity is critical to avoid overlooking details and ensuring

that information is not lost. The root of some issues with the gen. 2 InP was the back and forth transition of the InP work between myself and Junqian. Some issues with mask layout and processing details could have been avoided if continuity had been maintained. A complete understanding of the key device and system level requirements is also important to ensure that the design does not have unexpected flaws. While the need for n-side isolation was recognized in the design, the helium implant process, discussed in Section 4.2.13 and the level of attainable isolation with low optical loss penalty was not properly calculated. More detailed calculations of the system level requirements and the device level design to achieve the required isolation should have been conducted before starting fabrication.

Adding additional steps and modifying the process in the middle of fabrication added risk and uncertainty. With new process steps, it is important to validate the process using test samples, ideally with the same material and structure as the main samples. This was another issue with the gen. 2 fabrication, where the difficulty and lack of availability for regrowth prevented processing on new epitaxial (epi.) quarters. This was a major risk as there was only one epi. quarter that survived the entire process. For long process flows, maintaining a leading epi. quarter along with 2 backups helps to mitigate risks. A test InP quarter can be used for initial process verification, followed by the leading epi. quarter and the 2 backups. Test quarters are useful for optimizing lithography recipes where the material layers are not important. They are also useful for validating dielectric or InP dry etching recipes. Processing with a leading and two following epi. quarters allows for the leading quarter to be replaced in case of unexpected damage while still maintaining a following quarter. With only one leading and one following quarter there is a cost and benefit analysis of bringing another epi quarter up to the current process step. The risks in the rest of the process flow and the expected device yield need to be weighed against the time and money required to process another epi quarter. Sample

damage from mishandling is a constant, unavoidable risk due to the fragility of InP. Unexpected tool issues, especially with etching or metal deposition also present risks where the damage is often irreversible.

Short runs are an excellent way to validate segments of the process with critical process steps (e.g. metal deposition, waveguide etching, implantation) where device measurements can quantify the outcome. The gen. 2 RX would have benefited from a short run to ensure the quality of the contact metal process. While additional epi. quarters are needed for short runs, they can improve device performance through fabrication process optimization with feedback from device measurement. They also allow for problems to be found quickly, reducing the risk of unexpected issues for the full process run. Checking the quality of the epi. wafers is another benefit of short runs. A short run to validate the n-isolation resistance could have identified the issue with the lower than expected resistance discussed in Section 4.2.15. The difficulties with lithography from the surface topography of the deep isolation etch may also have been identified in an n-isolation short run.

Epiwafer vendors typically provide photoluminescence data to verify the peak emission wavelength and x-ray diffraction data to check the QW thickness, but it is also valuable to verify material composition with secondary ion mass spectroscopy (SIMS), refractive index with spectroscopic ellipsometry, and electrical properties with hall effect measurements. With appropriate ellipsometer measurements and modeling software, the refractive index of the epi. quarters used for processing can be approximated. Sacrificial pieces are needed for SIMS or hall effect measurements.

Successful device fabrication is a multi-disciplinary endeavour where the learning curve is sharp initially and never has a large plateau. From experience, fabrication always reveals new problems to solve and lessons to learn. Completing a fabrication run on-time with good yield requires drawing from the expertise of many people due to the complexity

of the process. Having a group with experience and open communication is major benefit. The UCSB nanofab staff, Prof. Coldren, and the dissertations from previous students were crucial to the learning process. While the experienced people at UCSB are helpful for answering questions, the benefits of a senior student or a partner in the fabrication process should not be understated. A fellow group member with processing experience can provide quick and low stress communication, lessons from hands-on experience, a more detailed understanding of how the overall process fits together, and moral support when needed.

For future PIC fabrication projects, a hierarchy of requirements for system properties to material characteristics should be constructed during the design phase and reviewed by people with materials, photonics, and circuits backgrounds to identify any missing aspects. Designs and simulations should consider how the variation in material properties, fabricated geometry, and device performance impact the overall system. Verification of material properties will reduce risks with design and processing. Splitting the fabrication into sections which can be used as short runs will also reduce risk with the full process. While detailed analysis and calculations in the design phase and short runs will help find problems early, there is a balance between risk mitigation and progress. It is important to draw from people's experience to find the right balance and to have knowledgeable feedback which can clarify the impact and importance of uncertainties and design and fabrication.

Chapter 5

Silicon Based PICs for O-band Coherent Links

While III-V based materials are required for lasers and SOAs, it is a challenging material to process, especially with an small team and limited experience, which is evident from the previous chapters. While there are InP foundries, the fabrication process and associated process development kits (PDK) for designing devices are less mature than silicon photonics foundries. SMART Photonics and Fraunhofer HHI offer PDKs, but their MPW runs are based in C-band. HHI and other InP foundries have developed O-band capabilities, but they are only offered for a dedicated fabrication run, which is cost-prohibitive for university projects. There are several silicon photonics foundries with multi-project wafer (MPW) runs and PDK models for design, notably GlobalFoundries (GF), AIM Photonics, Tower Semiconductor, Advance Micro Foundry, and IMEC. Intel is also a major manufacturer of silicon photonics with the advantage of heterogeneous integration of III-V material for lasers and SOAs. Through the INTREPID project, a collaboration with Intel enabled the design and fabrication of SG-DBR lasers and two generations of TX and RX PICs. This chapter will cover my work on the SG-DBR lasers,

a brief summary of the second generation TX PIC, and the two RX PIC generations. A coherent receiver using GF 45SPCLO process will also be introduced.

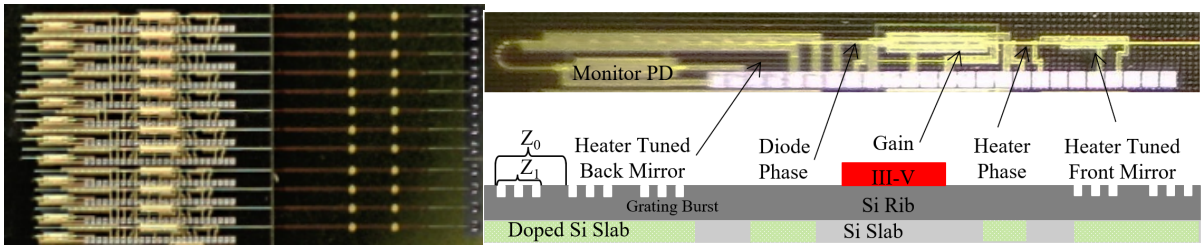
5.1 Heterogeneous III-V on Si based tunable lasers

Tunable lasers have applications in multiple areas, but the lasers in this section (originally published in [244]) are focused on short reach communications. The lasers below are designed to act as the local oscillator (LO) for analog coherent links, previously mentioned in Section 1.2. An optical phase-locked loop (OPLL) is used in these links to frequency- and phase-lock the LO to the transmitter laser. This is accomplished by modulating a diode in the laser cavity with an error signal generated by feeding part of the received data signal through a Costas loop phase/frequency detector and loop filter. A diode phase section with sufficient bandwidth and tuning efficiency is required to maintain phase locking [30, 15]. For fabricating the laser, the silicon photonics platform is advantageous for its large-scale manufacturability, reduced cost, and integration capabilities [245, 246]. While silicon does not have a native light source, wafer bonding of III-V on silicon has matured, enabling high performance lasers on silicon and a large variety of photonic integrated circuits (PICs) to be manufactured at scale [82, 84].

5.1.1 Laser Design and Fabrication

Using Intel's silicon photonics platform, several SG-DBR laser variants were designed. Fig. 5.1 shows the fabricated lasers and a design schematic. The gratings were designed to maximize output power with a low threshold and high mode suppression ratio (MSR). For high front output power, the front gratings were designed with low reflectivity by reducing the number of periods (Λ) per grating burst ($Z_1 = n\Lambda$) and the number of bursts. A long, high reflectivity back mirror was used for high MSR and low threshold.

The cavity length needs to be optimized such that the phase section provides several GHz of tuning for frequency locking using the OPLL. To examine the impact on MSR, threshold, tuning efficiency, and output power, multiple grating designs and phase section lengths were fabricated [244].



(a) (b)

Figure 5.1: (a) The full array of laser variants is shown. (b) A schematic view of the laser shows the details for the SG-DBR devices.

5.1.2 Laser Characterization

For all measurements, a thermo-electric cooler is used for temperature stability, and a probe card is used for biasing. For one variant, labeled Design A, a tuning range of 48 nm (1273 to 1321 nm) and MSR of 50 dB, as shown in Fig. 5.2, were measured by sweeping the voltage for the front and back mirror heaters while measuring a fraction of the output power with an optical spectrum analyzer (OSA). The low MSR band in Fig. 5.2(b) is likely due to reduced gain, supported by the lower spontaneous emission at longer wavelengths in Fig. 5.2(c). Output power shown in Fig. 5.2(d) is measured using an integrating sphere with a power meter. The output power and threshold worsen as the wavelength increases, but 20 mW of power is achieved from 1280 to 1315 nm. To the author's best knowledge, this is a record for O-band SG-DBR lasers on silicon, and it is comparable to other O-band widely tunable lasers [83, 140]. Although the laser has a large tuning range, Fig. 5.2 shows that continuous tuning is only achieved in a 1 to

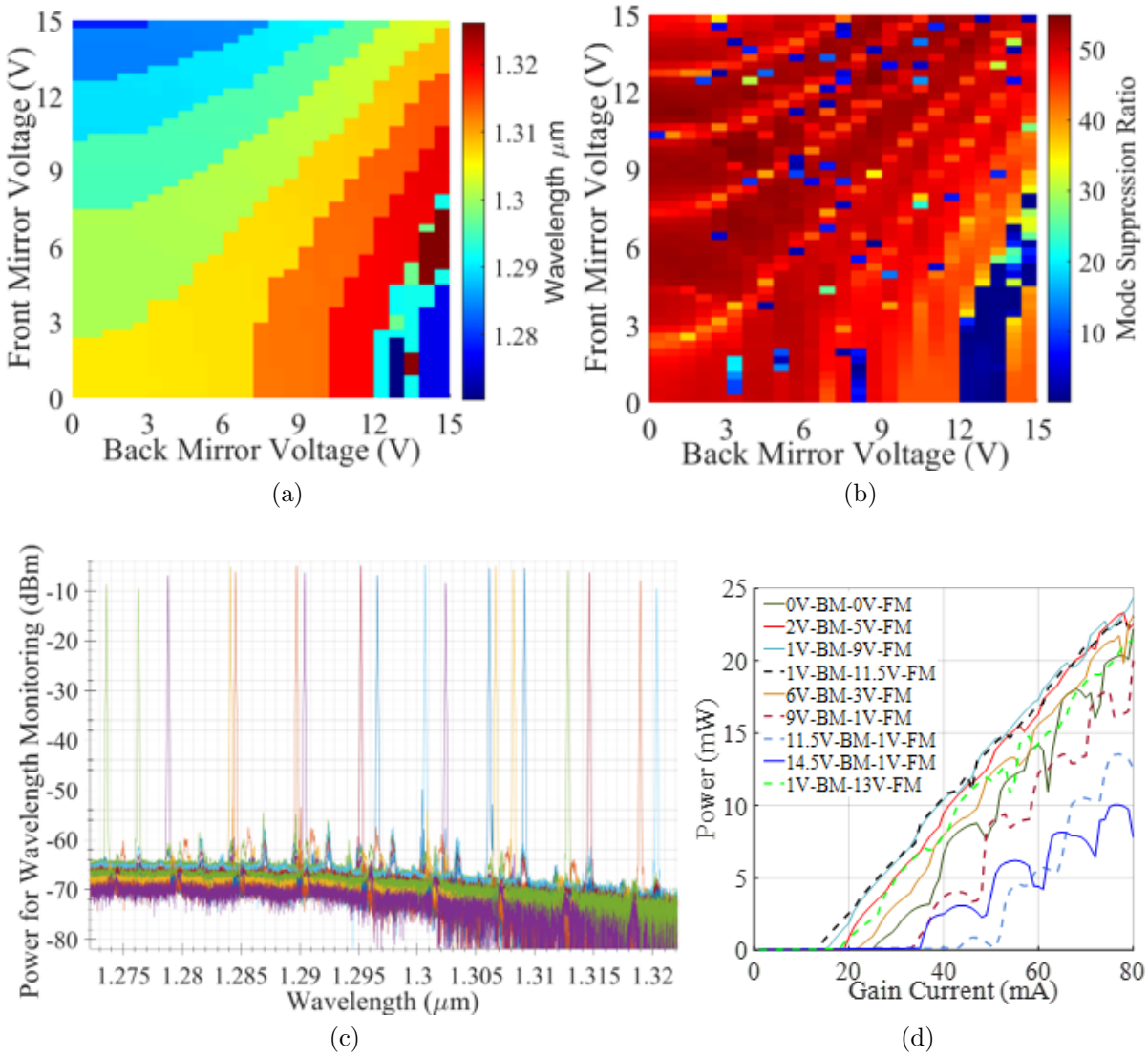


Figure 5.2: For Design A, (a) wavelength map and (b) MSR, (c) spectra, and (d) output power are measured at 20°C

3 nm range around each SG-DBR supermode, not across the entire tuning range. By sweeping the diode phase section current, tuning efficiency was measured using an OSA as shown in Fig. 5.3(a)-(b). The 400 µm length for Design A provides up to 0.75 GHz/mA tuning compared to 0.32 GHz/mA for the 200 µm length in Design B. The decrease in tuning efficiency at higher currents is likely caused by Joule heating which shifts the index in the opposite direction compared to carrier injection. The impact of heating was confirmed using low duty cycle pulsed current and monitoring the OSA spectrum in max hold mode, which saves the maximum power at each wavelength over repeated sweeps. The pulsed current will minimize thermal effects to examine the improvement in phase shift efficiency from carrier injection. Fig. 5.4 compares the spectrum with the same peak current in DC and pulse modes, resulting in close to double the phase efficiency in pulsed mode. When using 10% cycle pulses with 10 kHz frequency, the OSA detects the average power over many pulses, which is the reason the shifted wavelength has a 10 dB lower peak in the pulsed measurement.

Using a standard delayed self-heterodyne (DSH) setup with a 25 km fiber delay and a 200 MHz acousto-optic modulator, a linewidth (LW) of 0.60 MHz (broadened by flicker and other technical noise) was fitted for Design A, as seen in Fig. 5.3 (c) . The frequency response of the diode phase tuner was measured by converting the optical frequency modulation to amplitude modulation (AM) using the edge of a bandpass optical filter with the setup in Fig. 5.5. A photoreceiver connected to an electrical spectrum analyzer (ESA) was used to measure the frequency response of the AM signal, yielding a 100 MHz 3-dB BW in Fig. 5.3(d), sufficient for operation in the analog coherent OPLL.

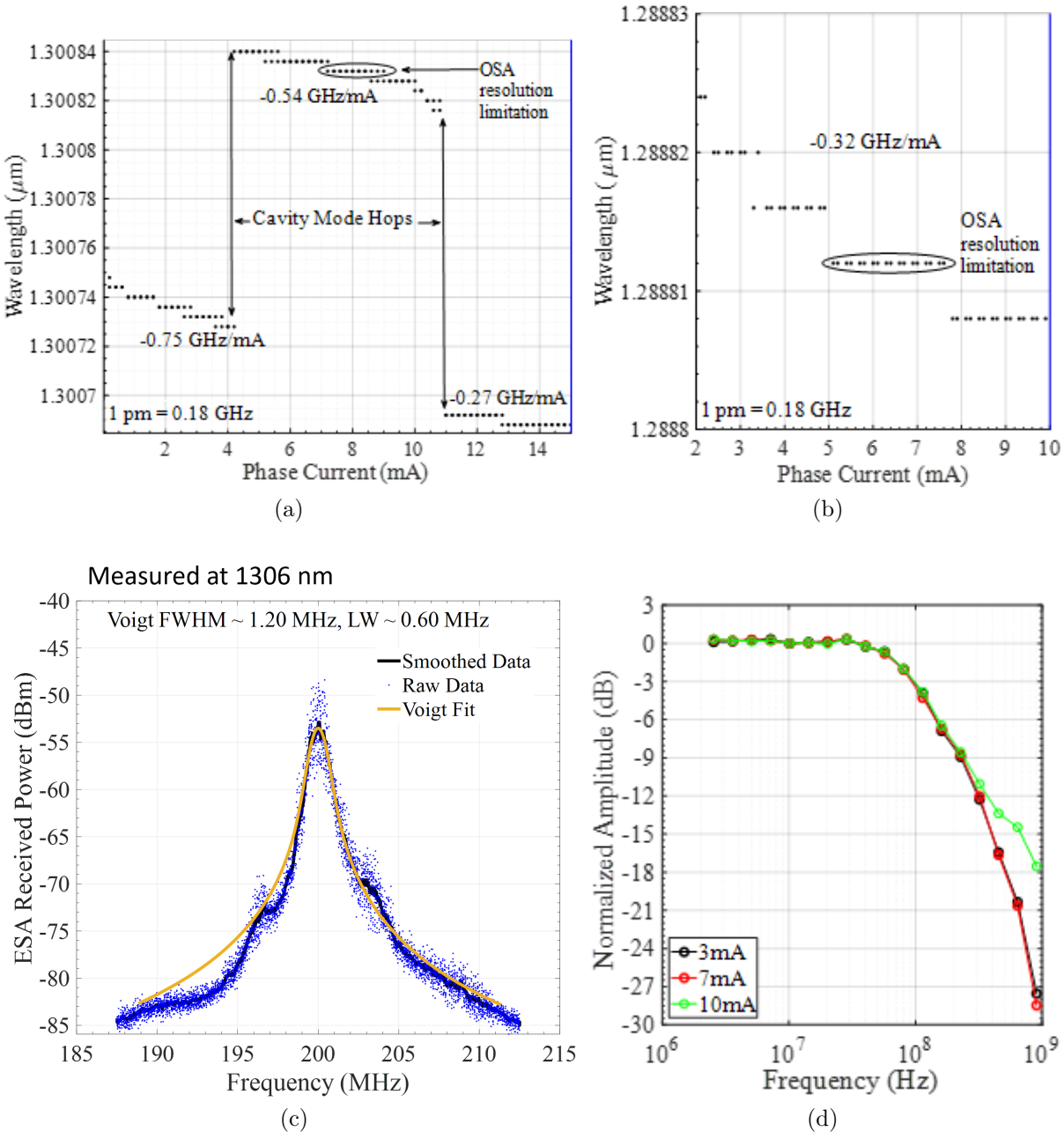


Figure 5.3: Tuning efficiency is larger for (a) Design A compared to (b) Design B. Apparent LW (c) of Design A is 0.60 MHz. (d) Diode phase tuner frequency response shows 100 MHz 3-dB BW.

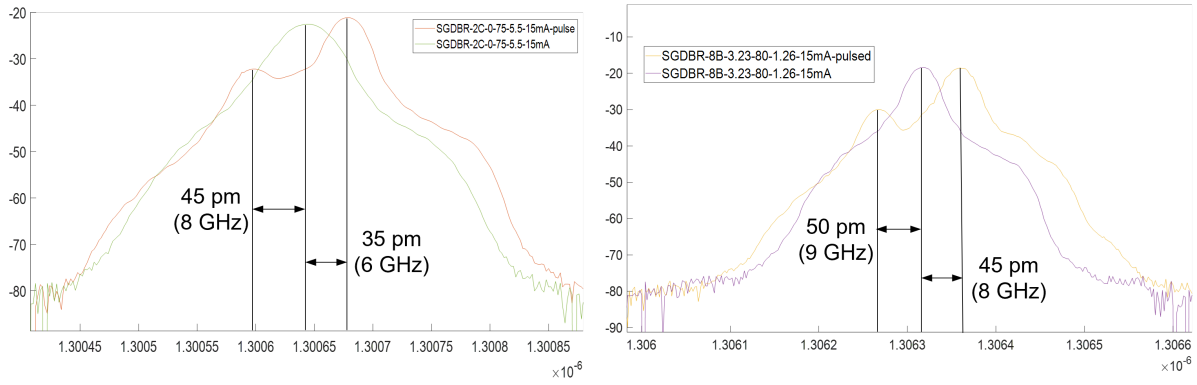


Figure 5.4: OSA spectrum in max hold mode showing increased phase shift efficiency with pulse current compared to DC.

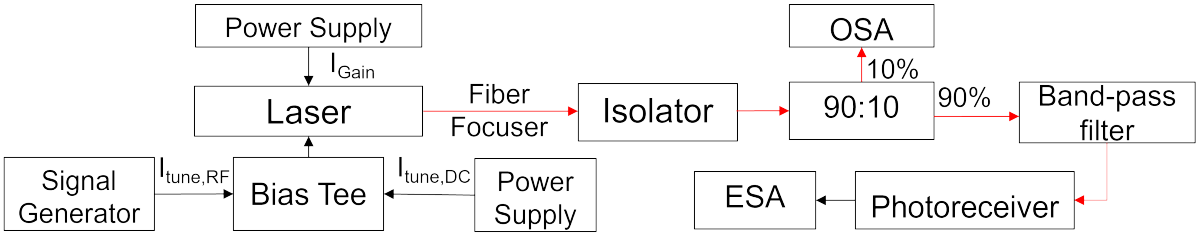


Figure 5.5: Schematic of the diode phase section bandwidth setup

5.2 IQ Traveling Wave Modulator

For future measurements in Chapter 6, the Intel Alpha Transmitter was used for generating the coherent optical signal, so the details of the TX PIC will be briefly discussed here. The TX PIC, shown schematically in Fig. 5.6 and as part of a wire-bonded assembly in Fig. 5.7, includes 3.2 mm travelling wave Mach-Zehnder modulators (TWMZM) designed for push-pull operation with a differential drive that are nested for dual-polarization IQ modulation. Integrated termination resistors and capacitors are included to extend the electro-optic bandwidth by peaking the modulator frequency response. Thermo-optic phase shifters (TOPS) are used with monitor photodiodes (PDs) to set the DC bias point for each of the MZMs, and diodes are used as free-carrier phase shifters (FCPS) for bias point and attenuation adjustment. A 3-arm interferometric tunable laser [247] is used to provide >10 dBm input optical power to the TWMZMs.

This laser design provides continuous wavelength tuning across a roughly 15 nm range for aligning the wavelength to the receiver laser with the same design while maintaining >40 dB mode suppression ratio and <700kHz integrated linewidth [248]. After each of the IQMs, an integrated SOA boosts the power to mitigate the impact of the inherent modulation loss for coherent. Details on the design and performance of the SOAs are provided in [249]. The data from each IQM passes through the polarization beam combiner-rotator (PBC) which rotates one set of data to the TM polarization. The output coupling is achieved using a broadband spot-size converter to increase the mode diameter for edge coupling to a lensed fiber. Two test lasers (A & B) are included for optional laser characterization measurements.

This PIC which was previously used to demonstrate 64 Gbaud self-homodyne QPSK transmission [248]. The Pre-Alpha version of this PIC was also used for 56 Gbaud self-homodyne DP-QPSK with an external laser. More details regarding the design of the modulator, co-designed electrical driver circuits, and past coherent link measurements are found in [248, 250, 251].

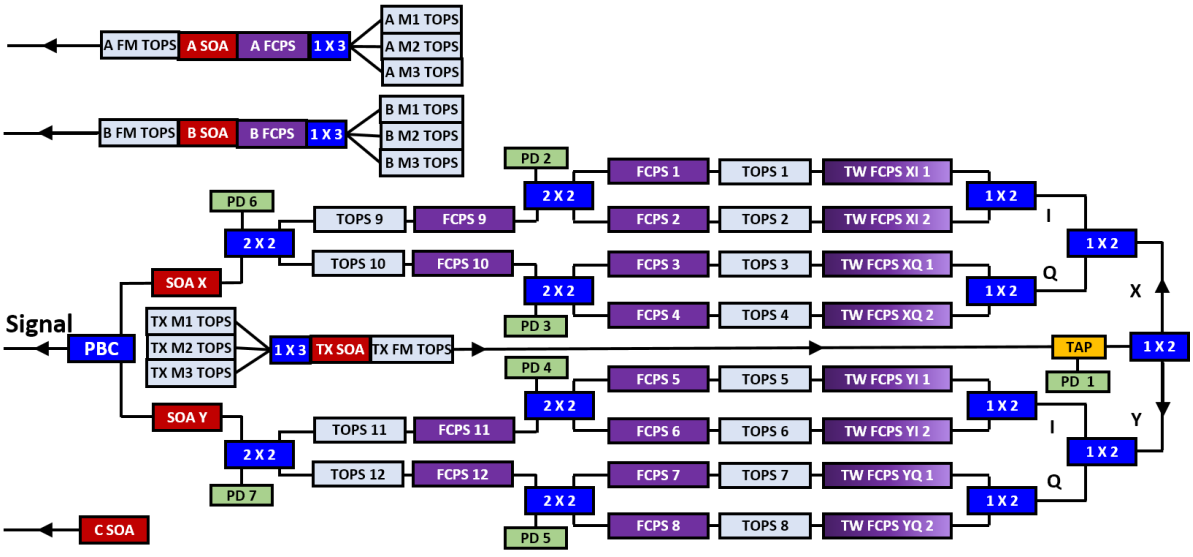


Figure 5.6: Block Diagram of the Intel Alpha Transmitter PIC

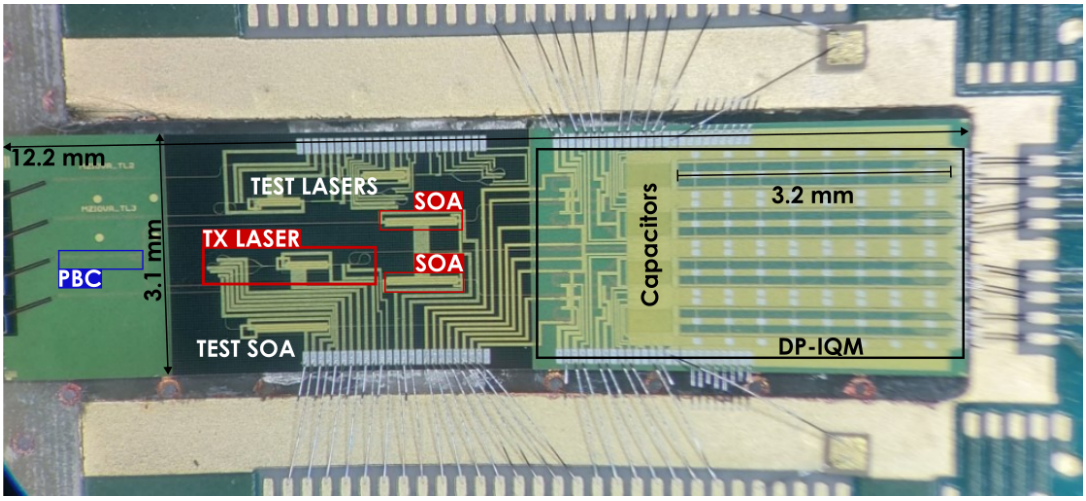


Figure 5.7: Top view of the wirebonded transmitter assembly with the key elements labeled on the PIC

5.3 Coherent Receivers

As part of the INTREPID program's goal to demonstrate >50 Gbaud, I was involved with the design and/or testing of two generations of receiver PICs from Intel's silicon photonic process and one receiver from GlobalFoundries 45SPCLO process. This section will provide an overview of the PIC features.

5.3.1 Intel Pre-Alpha Receiver

The design of the receiver began with an assessment of the available components and simulation for new components that were required. The O-band waveguide crossing was identified as a missing component, and Lumerical was used to simulate new designs. A crossing was designed based on MMI self-imaging, similar to [252]. The other major components were all identified and the design performance met the requirements for low insertion loss and broad, dual polarization, O-band performance. Using the chosen components, the system level design was examined to ensure that the transmitted polarization state was recoverable with minimal power imbalance and the LO phase offset was

matched for each polarization. For active alignment of an edge-coupled fiber array, MPD A1 and A2 are included on the outer edges of the chip. A polarization splitter-rotator (PSR) separates the incoming polarizations, and an on-chip polarization controller (PC) can be used to recover the transmitted polarization state before coherent demodulation in the two 90° hybrids. Using cascaded TOPS and 2×2 MMI couplers, the input state of the light is transformed to recover the original TE and TM states, following a Jones matrix transformation [253]. Monitor PDs and variable optical attenuators (VOA) are used to detect and equalize the polarization dependent loss. The 90° hybrids utilize a 2×4 paired interference multimode interference (MMI) coupler with a cascaded TOPS and 2×2 MMI for the quadrature demodulation, as described in [173]. Ge-on-Si photodiodes with ≈40 GHz bandwidth and 0.9 A/W responsivity [42] detect the signals. An image of the Pre-Alpha RX PIC is shown in Fig. 5.9. This PIC was used in a successful 56 Gbaud DP-QPSK link demonstration with the Pre-Alpha TX PIC [250].

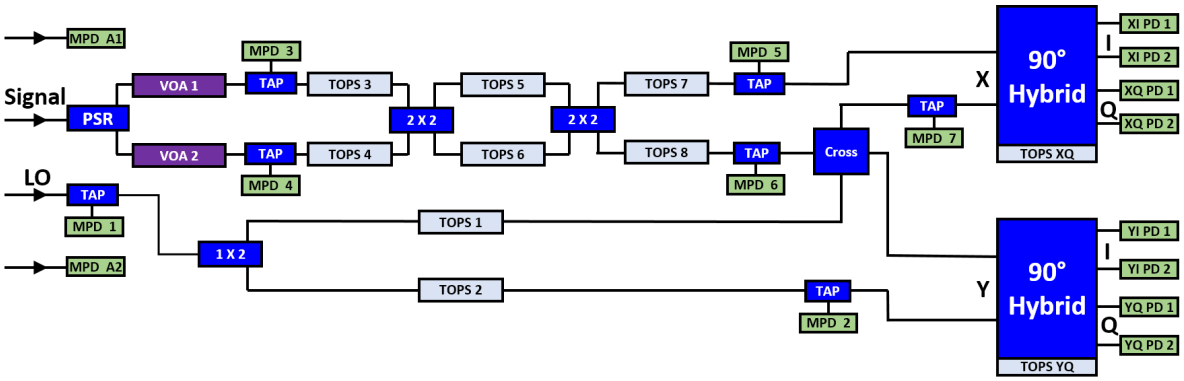


Figure 5.8: Block Diagram of the Intel Pre-Alpha Receiver PIC

5.3.2 Intel Alpha Receiver

The Intel Alpha RX PIC is depicted in Fig. 5.11. It uses a similar design as the Pre-Alpha RX except a tunable laser is integrated as the local oscillator (LO), using

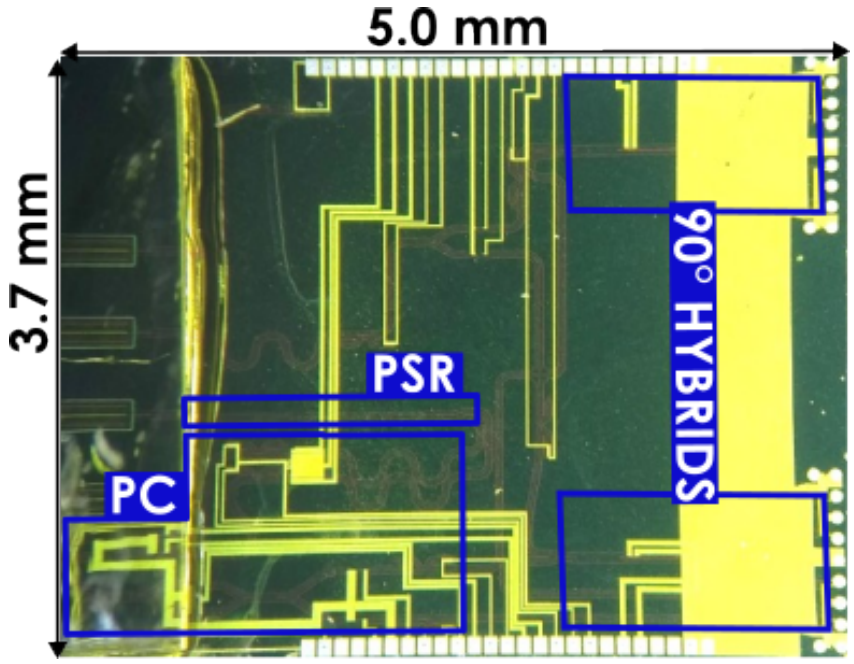


Figure 5.9: Image of the Intel Pre-Alpha Receiver PIC

the same 3-arm design as the TX Alpha PIC. Broadband edge couplers with spot-size converters are used for input coupling the transmitted signal and for output coupling a 5% monitor tap of the local oscillator (LO) laser. The included output SOA is used to amplify the power from the LO tap for monitoring the spectrum. In the Fig. 5.11 assembly, the PIC is packaged with Marvell 6452TA transimpedance amplifiers (TIAs) for linear amplification of the photocurrent. This assembly was used for a DP-16QAM demonstration which will be discussed in Section 6.1.

5.3.3 45SPCLO Dual Mode Receiver

To demonstrate reconfigurable functionality for direct detection and coherent demodulation, a receiver was designed and taped out in GlobalFoundries Fotonix (45SPCLO) process. The design and layout work were conducted by Aaron Maharry and Viviana Arrunategui-Norvick. The PIC includes broadband edge couplers with silicon v-grooves

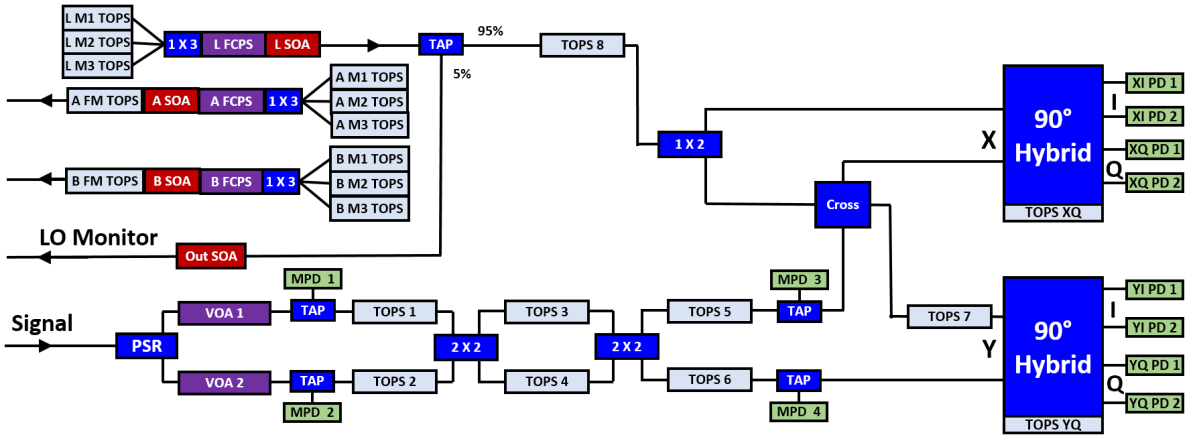


Figure 5.10: Block Diagram of the Intel Alpha Receiver PIC

for optical coupling. A PSR and cascaded TOPS with 2×2 MMIs are used for polarization control, similar to the Intel RX PIC. Additional TOPS and MMIs act as tunable couplers (TC), routing the light through or around the 90°hybrid. The assembly shown in Fig. 5.12 was used in a 53 Gbaud PAM4 and 16QAM demonstration. More details regarding the PIC functionality and the link experiment are explained in Section 6.2.1.

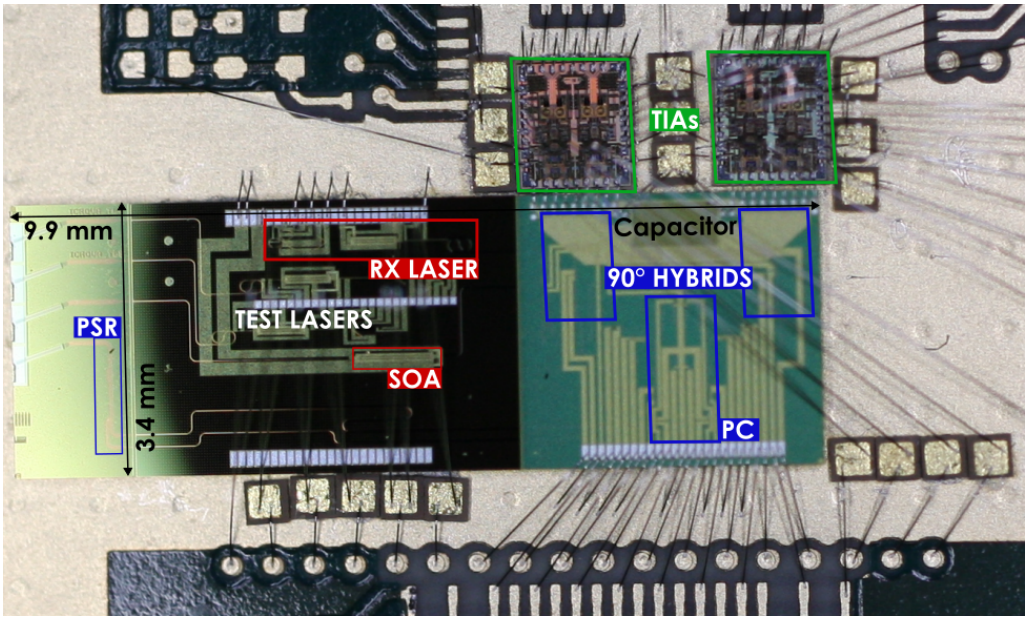


Figure 5.11: Top view of the wirebonded Alpha RX assembly showing the TIAs and the major components on the PIC

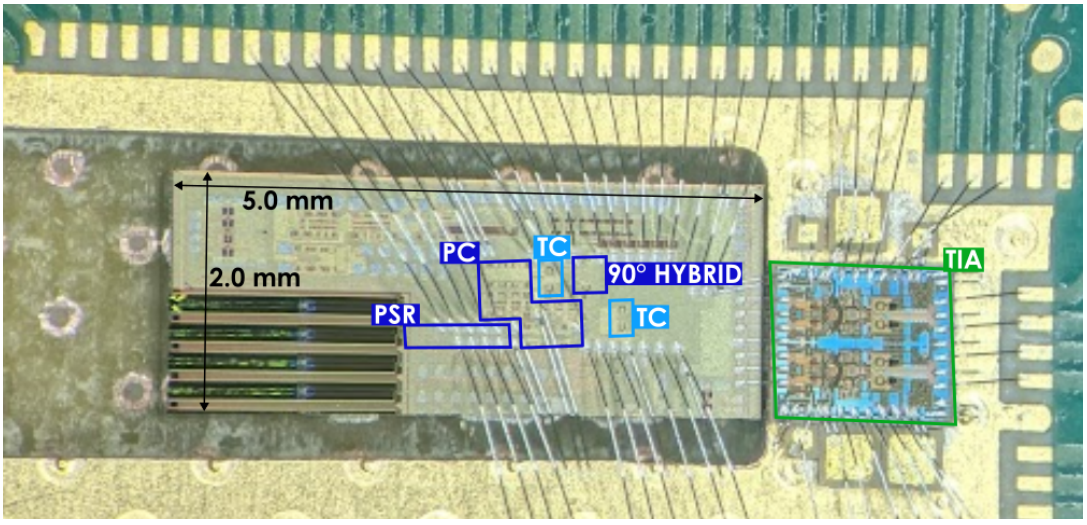


Figure 5.12: Top view of the wirebonded dual mode RX assembly with the PIC and TIA

Chapter 6

Short Reach O-band Coherent Link Demonstrations

Exponential growth in intra-data center (IDC) interconnect traffic necessitates higher capacity links for short reach applications up to 10 km. Current data centers employ intensity-modulation direct-detection (IMDD) with multiple wavelengths in the O-band. Scaling intra-data center optical links beyond 1.6 Tbps presents significant challenges for intensity-modulation direct-detection (IMDD) due to bandwidth limitations in optical and electrical components beyond 200 Gbps per lane [254], and scaling with additional wavelength division-multiplexed (WDM) channels is constrained by chromatic dispersion (CD) and four-wave mixing (FWM) [255, 256, 257]. Therefore, maximizing spectral efficiency is critical for increasing net data rates both for single-λ links or WDM links with a fixed number of wavelengths. To demonstrate the capability of coherent links for improved spectral efficiency and bit rate scaling, link experiments using the Intel RX Alpha PIC and the 45SPCLO dual mode RX PIC are covered in this chapter, using the Intel TX Alpha PIC as the transmitter.

6.1 Integrated Laser Intradyne Coherent Link

Coherent detection provides a promising approach towards 400 Gbps/λ links that can be scaled to 1.6 Tbps or 3.2 Tbps with WDM or multiple fibers. Recently, 64QAM net 1.6 Tbps transmission over 10 km has been demonstrated in the O-band using the thin-film lithium niobate (TFLN) platform and dual-polarization (DP) emulation [31]. However, silicon photonics (SiP) remains an attractive platform for its high-yield, cost-effectiveness, and PDK passive elements - including MMI couplers, ring resonators, polarization splitters, rotators, and combiners. Prior experimental work in coherent O-band SiP links often used external optical amplifiers such as praseodymium-doped fiber amplifiers (PDFAs) or was limited to QPSK [250, 248, 258]. Higher order coherent transmission experiments have been reported in O-band using single-polarization SiP IQ modulators (IQMs), but not as a link between packaged DP transmitter (TX) and receiver (RX) photonic integrated circuits (PIC) [259].

This section covers a coherent link where O-band lasers and semiconductor optical amplifiers (SOAs) are heterogeneously integrated on both the TX and RX SiP PICs, using the Intel Alpha TX and RX described in Section 5.2 & 5.3.2. The use of integrated gain sections circumvents the need for external optical amplifiers as used in previous O-band work. Integrated polarization beam combiners (PBCs) and polarization splitter rotators (PSRs) allow true DP-16QAM to be demonstrated in an O-band SiP coherent link at 400 Gbps/λ without external optical amplifiers over 2 km. This first-of-a-kind demonstration was published at OFC 2024 [260] and will be discussed in greater detail in the following subsections.

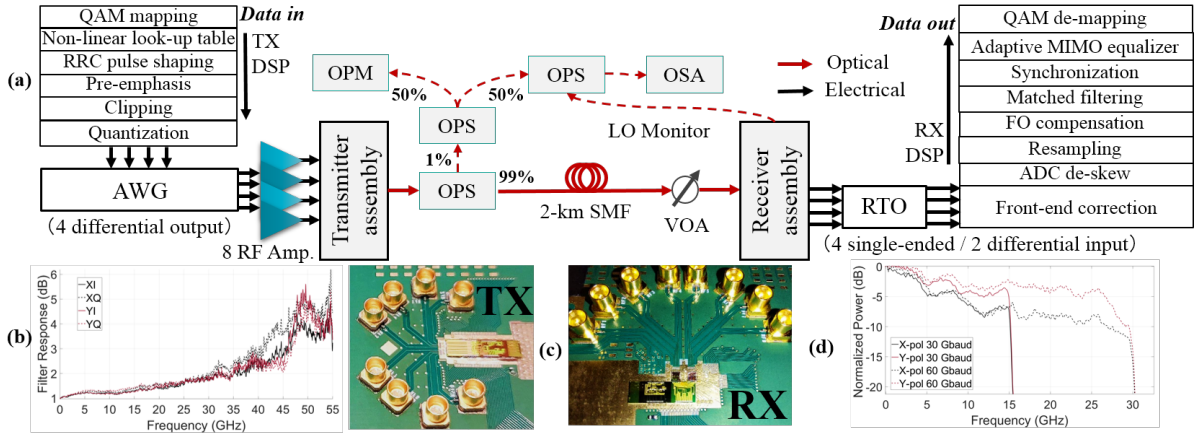


Figure 6.1: (a) Schematic of coherent link with TX & RX DSP routines with (b) the pre-emphasis filter response, (c) images of the assemblies, and (d) the RX normalized power spectra for DP-16QAM at 30 and 60 Gbaud.

6.1.1 Experimental Setup

The coherent link was constructed as shown in Fig. 6.1. On the TX DSP side, raised root cosine (RRC) pulse shaping with 0.02 roll-off is used for improved signal to noise ratio (SNR) along with pre-emphasis that is calibrated to equalize the response of the signal at the output of the RF amps.

We apply a 1-symbol nonlinear look-up table as a pre-distortion algorithm to compensate for the nonlinearity of the modulator and the SOAs [261, 262, 263, 264]. The signals are clipped to maintain a 7 dB peak to average power ratio (PAPR) and loaded onto a Keysight M8199A (70 GHz) arbitrary waveform generator (AWG). Four differential signals from the AWG were amplified with a combination of 4 SHF S804B (66 GHz) and 4 S807C (55 GHz) amps to drive the transmitter. AWG differential output swing ranged from 230 to 380 mV, with increased swing required at higher baud rates. The high-speed drive signals are delivered via coax cables through mini-SMP connectors to 50-Ohm traces ending with double-wirebonds to the PIC. Lensed fibers were used for optical edge coupling on both assemblies with an estimated 7 dB of coupling loss for each

PIC.

The independent TX and RX tunable lasers are aligned within ±3 GHz in an intradyne detection scheme, where frequency offset (FO) compensation is used in the RX DSP. The wavelength and power of the TX are monitored with a tap from a 99/1% optical power splitter (OPS) which is then split between an optical power meter (OPM) and optical spectrum analyzer (OSA). A monitor tap from the RX PIC is used for the LO spectrum. Both lasers are set to 1310.9 nm for all measurements. The received signal on the RX PIC is amplified with a wirebonded Marvell IN6452TA transimpedance amplifier (TIA) and connected through miniSMP to DC blocks to a Keysight DSOZ634A real-time oscilloscope (RTO). For dual-polarization measurements, the RTO has 4 inputs with 33 GHz and 80 GSa/s. Single-polarization data was measured using the two 63 GHz, 160 GSa/s inputs. Output swing from each of the 4 TIA channels was approximately 500 mV for all measurements.

Table 6.1: Optimized DSP for TX and RX Components

Parameter	Value	Parameter	Value
RRC roll-off	0.02	clipping PAPR	7 dB
sampling	2 SPS	sampling length	2×10^{19}
Eq. 1 taps	17	Eq. 2 taps	181
Eq. 1 learning rate, μ	4×10^{-4}	Eq. 2 learning rate, μ	9×10^{-6}
DPLL 1 gain	8×10^{-4}	DPLL 2 gain	3×10^{-5}

Data captures from the RTO were processed offline with the steps in Fig. 6.1. Front-end correction centers the constellation and corrects for IQ imbalance before the data is de-skewed and resampled to 2 samples per symbol. Filtering is matched to the TX RRC roll-off. Two layers of adaptive 4x4 real-valued multiple-input-multiple-output (MIMO) equalizers are used to compensate for impairments in the link, with 17 taps used in the first equalizer, and 181 taps used for the second equalizer. Because the link is operated in the O-band at the single-mode fiber (SMF) zero dispersion wavelength, a CD

compensation block is not used. The large number of taps is partially attributed to the packaging, which adds additional losses due to wirebonds and PCB traces. RF cabling, connectors, and DC blocks may create additional back-reflections, causing ripples in the frequency response before equalization. The current packaging is designed to interface with the test equipment, but could be optimized in a fully packaged transceiver. The set of optimized DSP parameters is shown in Table 6.1.

6.1.2 Link Optimization

Achieving the minimum BER for different ROP and baud rates requires tuning multiple bias parameters. To examine the sensitivity of the BER to several bias parameters, a set of sequential optimization sweeps were performed with the link operating at 60 Gbaud 16QAM, starting with the TOPS on the 90°-hybrid and finishing with the TIA automatic amplitude gain control. The optimal value in each sweep was kept for the next sweep. Figure 6.2 depicts the BER trends for each optimization sweep. Relative values are used for common plotting with Table 6.2 listing the actual values. It is clear that the BER is most sensitive to the TIA automatic amplitude gain control with the hybrid TOPS and input swing showing moderate sensitivity, and the PD reverse bias causing only a small change. This indicates that the system is primarily limited by the increased noise with high TIA amplification. The green markers indicate the relative bias values that were used for the sweeps in Fig. 6.3 and 6.4. Since the bias values differ from optimum points in Fig. 6.2, it may be possible to improve the full-link BER by a factor of 2, using more careful optimization.

Table 6.2: BER Bias Sensitivity Sweep Values

Parameter	Min	Max	Optimum
Hybrid TOPS bias (V)	0	1.6	1.2
PD Bias (V)	2	4	3
Input Swing (mV)	290	440	320
SOA Bias (mA)	35	55	45
TIA Gain Bias (V)	0.75	2.25	1.25

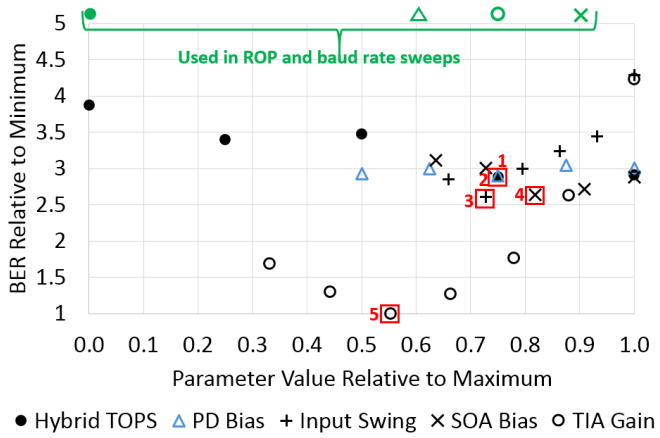
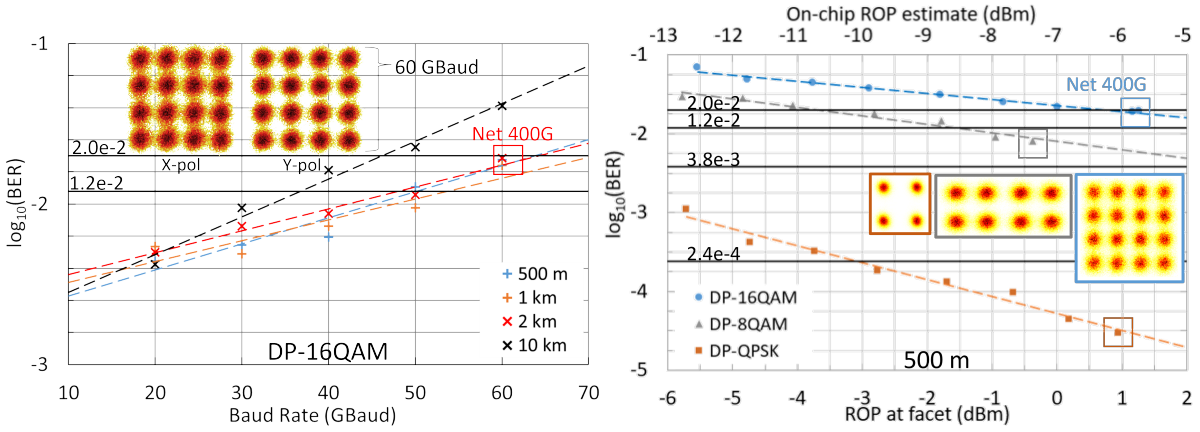


Figure 6.2: Relative change in BER when varying different bias parameters while operating with 60 Gbaud 16QAM. The numbers 1 - 5 in red indicate the order for optimizing each parameter.

6.1.3 Link Characterization Results

To characterize the system, the bit error rate (BER) was measured across baud rate and received optical power (ROP) for both polarizations (pols). Measurements with DP-16QAM in Fig. 6.3 show that the link is capable of operating under the O-FEC threshold up to 60 Gbaud, for net 400G transmission. The small variation in BER between the 0.5 to 2 km measurements indicate that the system does not suffer from any significant dispersion penalties, as expected for O-band. SNR penalties caused by loss have a noticeable impact on BER with the 10 km results. The impact of SNR on BER is clearly seen in Fig. 6.3(b) where there is a 4.5 dB sensitivity penalty between 8QAM and 16QAM, and the BER for QPSK is significantly lower. BERs in Fig. 6.3 are the average

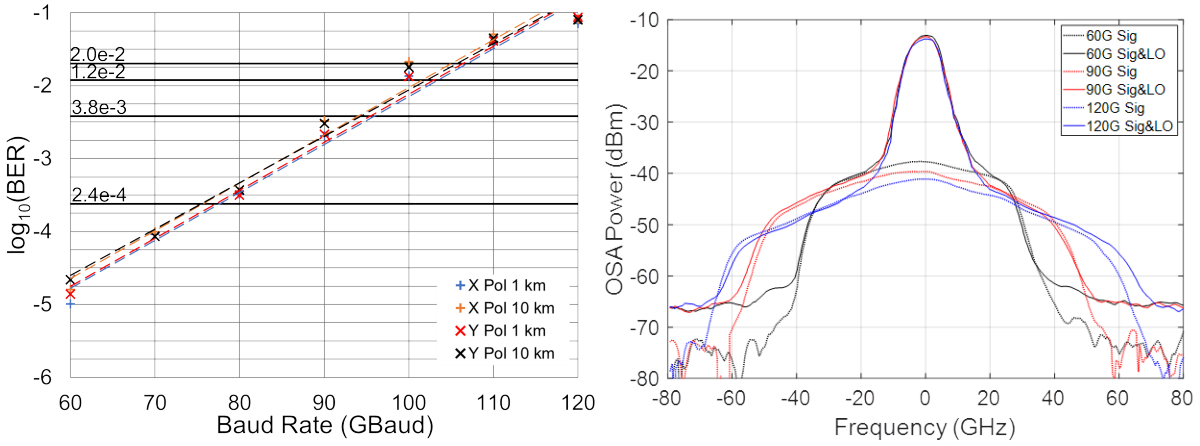
of the X&Y pols. As seen in the Fig. 6.3(a) inset, the X-pol. constellation has more noise. At 2.0×10^{-2}, DP-16QAM and DP-8QAM have sensitivities of -6.25 and -10.75 dBm for on-chip ROP. The sensitivity for DP-8QAM is -8.5 dBm at 1.2×10^{-2} BER, and for DP-QPSK it is -10 dBm at 2.4×10^{-4} BER.



(a) (b)

Figure 6.3: Measured BER for DP-16QAM link with 0.9, 1.4, 0.6, and -2.6 dBm ROP at the RX facet for 0.5, 1, 2, 10 km (variation due to connector losses) and (b) 60 Gbaud dual-pol. link at 500 m.

Dual polarization measurements are limited to 60 Gbaud by the 4-ch bandwidth (BW) of the RTO, but the 2-ch RTO BW is capable of 120 Gbaud. In Fig. 6.4(a), the higher SNR with single polarization QPSK (using the TX X-pol or Y-pol to the RX Y-pol) enables the link to operate at 90 Gbaud below the HD-FEC 3.8×10^{-3} limit and at 100 Gbaud below the O-FEC 2×10^{-2} limit. Closer agreement between BER of the TX X-pol & Y-pol transmitted to RX Y-pol suggests that the added noise in the DP X-polarization constellations comes from the RX side. With small variations between the single-polarization 1 and 10 km results, the system BW is the limiting factor for high baud rate QPSK. The BER data and OSA spectral roll-off in Fig. 6.4(b) suggest the system BW is close to 50 GHz. This supports the capability of SiP for 100 Gbaud links with improved packaging.



(a) (b)

Figure 6.4: (a) Measured BER for single-pol. QPSK link with -3 to -5 and -7 to -10 dBm ROP for 1 and 10 km. High baud rate reduces TX swing and RX ROP. (b) Optical spectra for increasing baud rates.

To my knowledge, this was the first demonstration of a net 400G/λ O-band SiP coherent optical link using heterogeneously integrated lasers and SOAs. Net 400G transmission over 2 km was accomplished using 60 Gbaud dual-polarization 16QAM, operating below the 15% overhead O-FEC threshold of 2×10^{-2}. Furthermore, it was shown the link can transmit 100 Gbaud QPSK below the O-FEC threshold of 2×10^{-2} and 90 Gbaud QPSK below the HD-FEC threshold of 3.8×10^{-3}, all over a span of 10 km. Notably, the link was closed without the use of external optical amplifiers, such as PDFAs, demonstrating the efficacy of using integrated gain in SiP coherent links. Flip-chip integration of high-bandwidth integrated drivers with peaking and shorter, high-bandwidth PCB traces would enable higher baud rates. Similar integration improvements can be made to the receiver, which can enable a future 100 Gbaud 16QAM silicon photonic link. Nevertheless, the coherent transmitter and receiver designs demonstrated in this work could be integrated into a full WDM transceiver to support reaches up to 10 km with QPSK, and data rates of 1.6 Tbps with DP-16QAM using only 4 wavelengths in the O-band.

6.2 Reconfigurable Mixed Domain Coherent Link

As mentioned in Section 1.2.3, deployment of optical circuit switches (OCS) in data center networks can drastically improve overall network cost and power consumption while providing scaling and performance advantages for both AI clusters and cloud applications [62, 63, 265], but optical switches will add insertion loss (IL), further constraining link budgets. Coherent detection is an attractive alternative to IMDD due to its potential to scale per-λ data rates and most importantly to improve receiver sensitivity which enables significant expansions of optical link budgets. The discussion in this section borrows from my article on the Mixed-Domain Coherent (MDC) link demonstration [266].

Coherent link deployment in short-reach, intra-data center networks has been prevented by their relatively high cost, power consumption, and lack of interoperability with current IMDD links. Conventional coherent link architectures rely on costly, power-hungry, cooled tunable lasers and advanced digital signal processing (DSP) application specific integrated circuits (ASICs) to enable key functions, including CD compensation, polarization recovery, and carrier recovery (CR). Despite ongoing efforts to optimize coherent DSP for shorter reaches, this technology will struggle to reach power and cost parity with IMDD and will also break compatibility with IMDD-based data center links.

The MDC architecture [267], shown in Fig. 6.5, uses polarization-multiplexed self-homodyne detection (PM-SHD) [69, 268, 269]. Light is split with a tunable coupler (TC) from a single, uncooled laser to transmit 16QAM data on one polarization, and an unmodulated carrier on the orthogonal polarization. This method avoids the optical circulators or wavelength filters used in other bidirectional SHC links [270, 70, 258]. The MDC receiver performs analog polarization control and carrier recovery optically, which enables use of cost-efficient PAM4 DSP ASICs. Crucially, an analog polarization controller (PC) and on-chip optical switching enable the coherent receiver to be reconfigured for IMDD

operation using the I-channel DSP lane and halving the per-wavelength bit rate. This link thus achieves power- and cost-parity with IMDD alternatives, while doubling the per-wavelength data rate, expanding the link budget, and maintaining interoperability with IMDD transceivers.

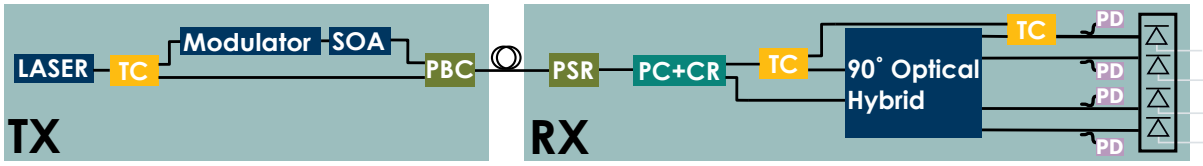


Figure 6.5: Block Diagram of the PIC components for the MDC Architecture.

6.2.1 Photonic Integrated Circuits for MDC

Detailed schematics of the transmitter (TX) and receiver (RX) photonic integrated circuits (PICs) used in this work are shown in Fig. 6.6 with images of the bare PICs shown in Fig. 6.7. The TX Alpha PIC used for this experiment was fabricated using Intel's silicon photonics process [98]. It includes four TWMZMs which are nested inside two IQ modulators, for dual polarization modulation. Ge-on-Si monitor PDs, III-V SOAs, and a tunable laser are also integrated [248, 247]. See Section 5.2 for more details. Although this TX is capable of performing the functions required for mixed domain coherent, it was not designed specifically for the MDC architecture. A tunable coupler is not included after the laser for adjusting the power splitting between the signal and carrier, and the bottom IQM for the unmodulated carrier has IL that would not be present in a design specifically for MDC.

The RX PIC was designed in GlobalFoundries (GF) 45SPCLO monolithically integrated electronics and photonics platform as part of a multi-project wafer (MPW) [94, 271]. The schematic in Fig. 6.6 shows the phase tuners and monitor PDs used for the analog polarization and carrier recovery. The tunable couplers are implemented us-

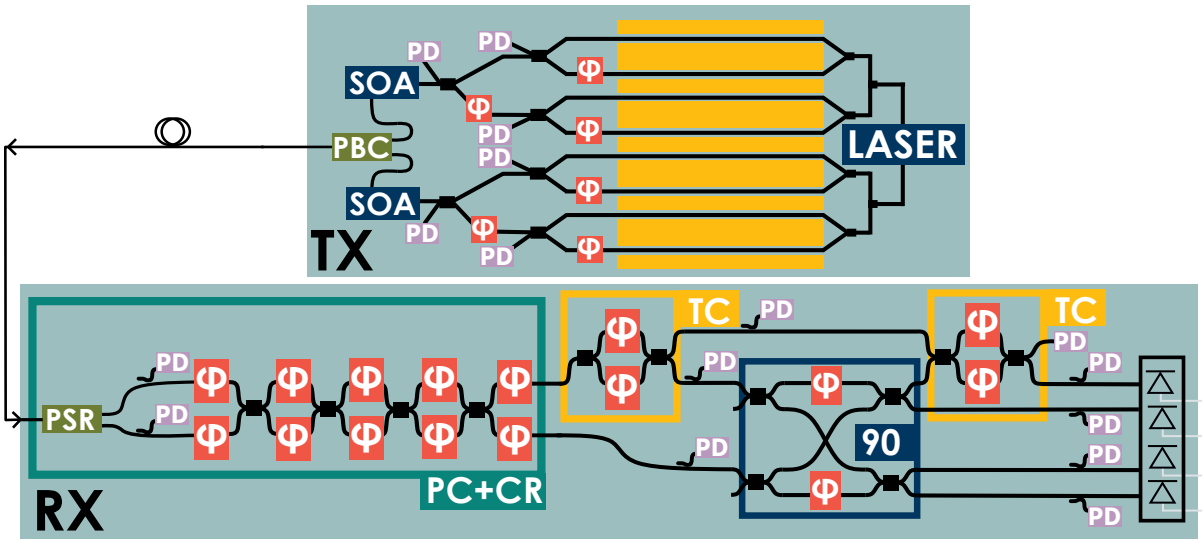


Figure 6.6: TX and RX PIC schematics showing the DP-IQM with an integrated laser and two SOAs above the reconfigurable RX with integrated PC+CR and tunable couplers.

ing TOPS to control the output from a Mach-Zehnder interferometer. To enable future control via low voltage CMOS, the TCs use the GF 45SPCLO sealed undercut design with a low P_π [272]. The analog polarization controller is implemented using cascaded 2x2 MMI couplers and the GF standard TOPS. This configuration enables reset-free recovery of the original linear polarization state by transforming the state of polarization (SOP) with the same effect as a quarter-wave plate (QWP) followed by a half-wave plate (HWP)[253]. A QWP-HWP system is capable of restoring the transmitted linear SOP from an arbitrary input SOP to the RX [273]. PCs using cascaded phase shifters and couplers have been previously demonstrated by multiple groups on silicon photonic platforms [274, 275, 276, 270, 277, 278, 279, 280] using various control algorithms. The standard GF 45SPCLO heater design was chosen for the polarization controller because of its faster switching time [281]. Carrier recovery is performed by adjusting the phase offset between signal and carrier with the final TOPS pair in the PC+CR section shown in Fig. 6.6. The optical transmission when tuning one TOPS in the polarization con-

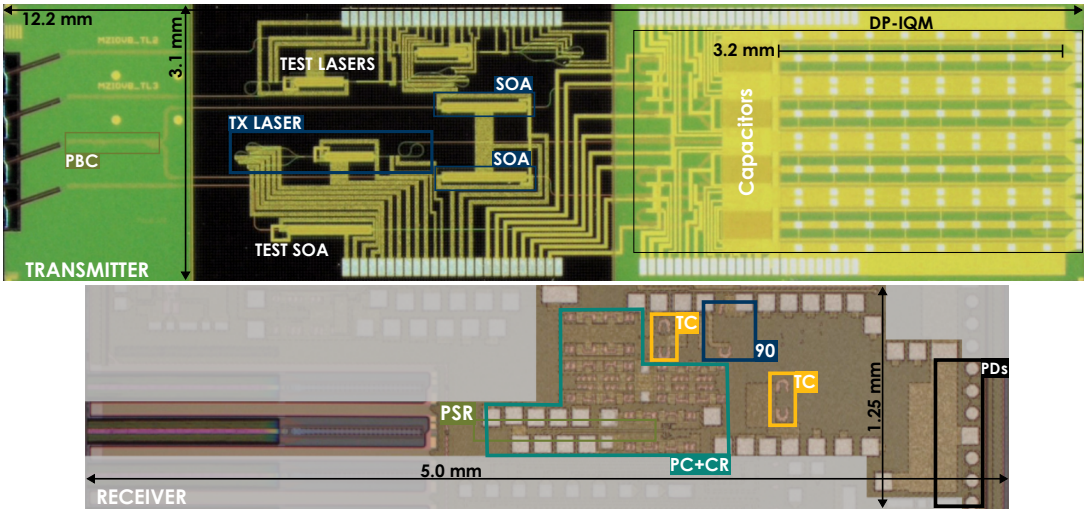


Figure 6.7: The bare TX and RX PICs are shown with labels to highlight the important components in each PIC.The shaded parts of the RX PIC cover other devices on a shared multi-project die.

troller and the tunable coupler are shown in Fig. 6.8 with $P_\pi = 31$ mW and 10 mW, respectively, which are close to the expected values [272].

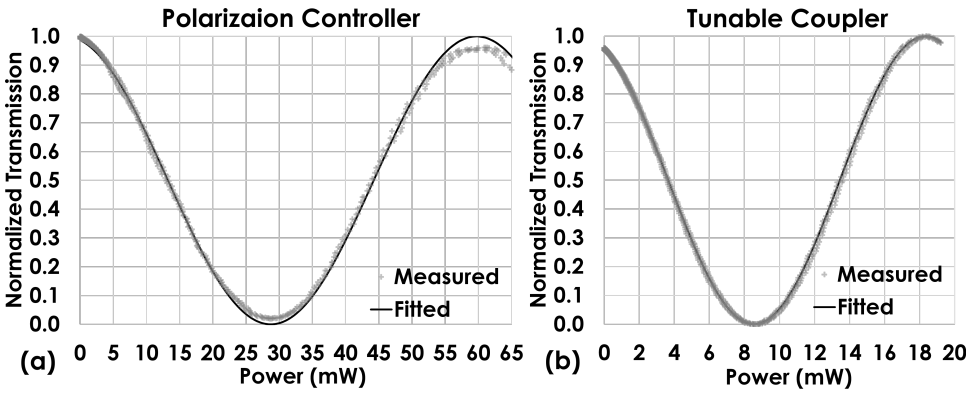


Figure 6.8: Normalized transmission data and $cos^2(P)$ fit for the thermal phase tuner in (a) the polarization controller and (b) the tunable coupler.

6.2.2 Reconfigurable Link Setup

The reconfigurable link was constructed as shown in Fig. 6.9 with back-to-back standard single-mode fiber (SMF-28). A commercially-available MaxLinear Keystone

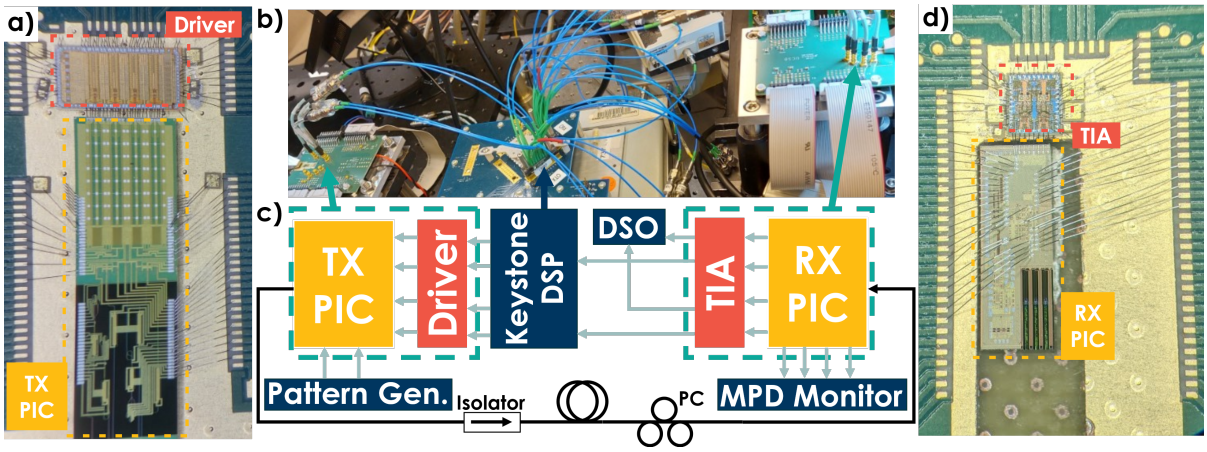


Figure 6.9: The physical (a) TX assembly and (b) full link setup are shown with the (c) setup block diagram and (d) physical RX assembly.

100G PAM4 DSP (MxL93683) was used to generate, transmit, receive, and analyze 53.125 Gbaud PAM4 pseudo-random bit sequence (PRBS) signals [282]. The Keystone DSP performed digital predistortion (DPD) on the transmit side to compensate for the frequency roll-off of the transmitter packaging, the nonlinear response of the modulator, and nonlinear pattern effects from the SOA [283]. The DPD was used to adjust the input voltage levels to improve the linearity of the optical output and provide 6 dB of pre-emphasis to counteract packaging losses. Feedforward equalization (FFE) was performed after the receiver to correct for additional RX packaging and lineup impairments. An on-chip clock-and-data recovery circuit was used to retime the PRBS signal at the receiver, and real-time bit error ratio (BER) was measured using the on-chip BER tester (BERT). Differential signals from the Keystone DSP were sent to the transmitter assembly via coax cables connected through mini-SMP connectors to 50-Ohm traces on a custom Isola MT-40 PCB with approximately 25 GHz bandwidth. Connections from the PCB to the Marvell IN6426DZ driver were made through wirebonds.

For polarization multiplexed coherent transmission, one IQ-MZM is biased for coherent modulation, while the other is set for minimum insertion loss to maximize un-

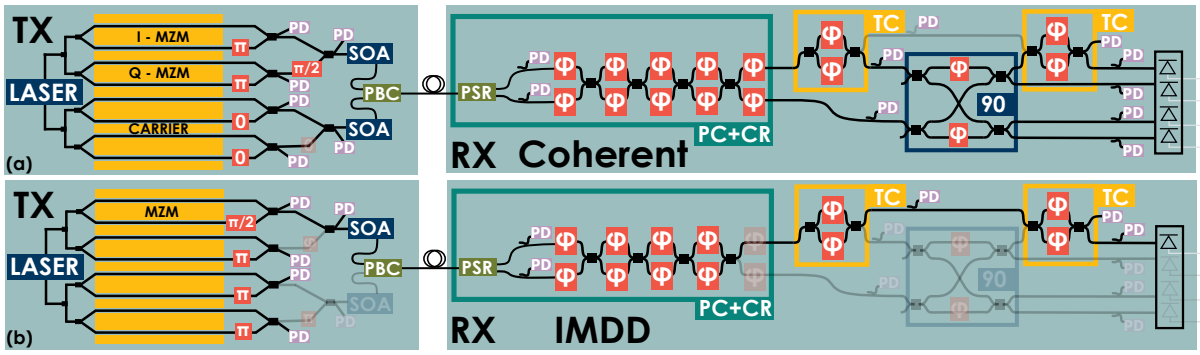


Figure 6.10: Configurations for the TX and RX PICs in (a) coherent and (b) IMDD modes are shown. The DC phase between the MZM arms is labeled and the waveguides without transmitted optical power are greyed out for each case.

modulated carrier power in the forwared LO path. Fig. 6.10(a) depicts the PM-SHD configuration where the signal and carrier are superimposed on orthogonal polarizations through the PBC edge-coupled to a lensed fiber. For IMDD transmission, one child MZM is biased at quadrature, while unused child MZMs are null-biased as shown in Fig. 6.10(b). For bias optimization and carrier recovery during coherent transmission, a low-speed pattern generator is used to drive the TOPS which set the bias points for the I and Q MZMs. PRBS waveforms at 10 kbps with 10 to 20 mV swing were used as a marker pattern to generate a low-speed constellation for manual optimization using the receiver monitor photodiodes (MPD).

The optical input to the RX is provided by a single cleaved fiber positioned in a V-groove edge-coupler. For convenience of testing, an off-chip isolator and polarization controller were used, which would not be required for a full transceiver. Light is coupled into a polarization splitter-rotator (PSR) followed by the on-chip polarization controller (PC) that recovers the transmitted polarization state by separating the modulated signal from the unmodulated carrier.

While automated polarization control and carrier recovery have not been implemented yet, the monitor photodiodes on the RX were connected to a prototype monitoring circuit

to manually optimize the biasing by visualizing the low-speed marker patterns applied to the thermal phase tuners on the TX. Figure 6.11 depicts the circuit and oscilloscope that were used to monitor the low-speed constellation which was optimized by adjusting the biasing of the phase shifters for the transmitter, the receiver 90° hybrid, and the carrier recovery. The recovered high-speed signals are mixed in the 90° hybrid and detected by differential PDs, as shown in Fig. 6.10(a). The PDs are >50 GHz Ge-on-Si waveguide photodetectors with ∼1 A/W responsivity. In the IMDD mode depicted in Fig. 6.10(b), there is no forwarded carrier so the signal bypasses the hybrid I/Os using switches set by TOPS. The received photocurrent is fed to a wirebonded Marvell IN6452TA transimpedance amplfier (TIA), which outputs to 50-Ohm traces and miniSMP cables with one single-ended output connected to the Keystone DSP and the other to a Tektronix DSA8300 digital sampling oscilloscope (DSO) to monitor the eye diagrams. All experiments were performed at room temperature without active temperature control.

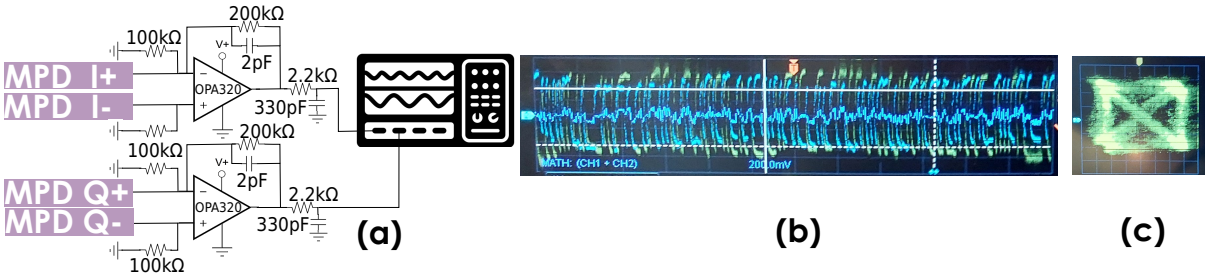


Figure 6.11: The diagram of (a) the setup for the low-speed constellation monitoring, (b) the captured PRBS patterns, and (c) an example constellation are shown.

6.2.3 Link Characterization Results

For all the experiments, the laser was set to ∼1306 nm with ∼10 dBm output into the DP-IQ-MZM. IMDD operation using single lane 53.125 Gbaud PAM4 achieved a BER of 2.80×10^{-5} when the TX fiber-coupled output modulation amplitude is ∼4 dBm and -5 dBm of signal power reaches the PD. Figure 6.12 shows the PAM4 eye captured from

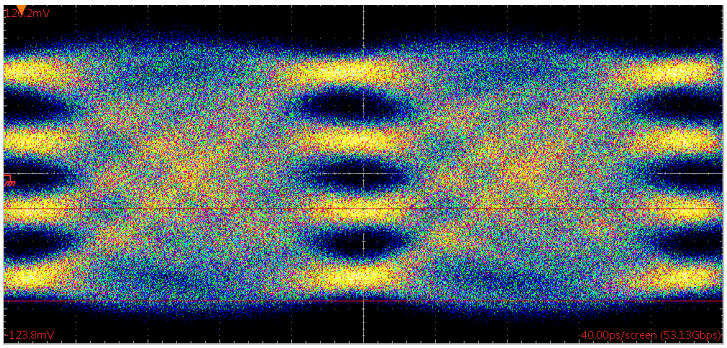


Figure 6.12: Receiver eye diagram captured by DSO during PAM4 measurements

the single-ended TIA output connected to the DSO. In comparison, coherent mode using two 53.125 Gbaud PAM4 DSP lanes to drive I and Q channels simultaneously achieved an average BER of 1.02×10^{-4} where, after an additional 6 dB of 90° hybrid splitting loss, each PD received approximately -18 dBm signal and -10 dBm carrier power.

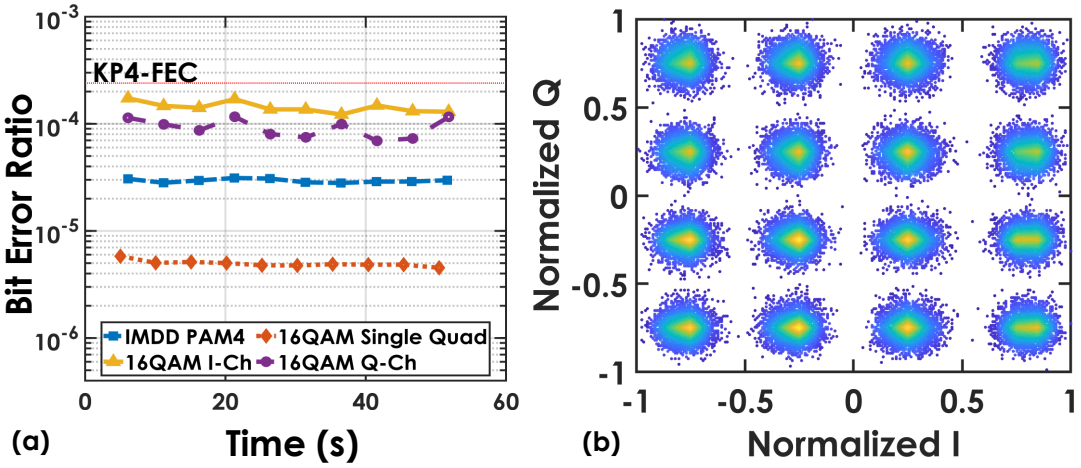


Figure 6.13: (a) BER vs. Time plotted for three link configurations. (b) 16QAM constellation using post-FFE sampled data.

These results were achieved with a facet-to-facet link loss budget of ∼12 dB. With improvements in optical packaging and PIC architecture, we expect significant improvements in the available link budget. As demonstrated in Fig. 6.13(a), $> 10^{12}$ total bits were transmitted with stable BERs for the three link configurations. Assuming 5.8% overhead KP4-FEC, the net bit-rate achieved is 200 Gbps for 16QAM and 100 Gbps

for PAM4. Setting the state of the on-chip polarization controller manually resulted in stable operation over periods sufficient to enable the measurements of low BER results. Further measurements are needed to examine the polarization stability over longer time scales, but slow variations in polarization state will be continuously compensated once the on-chip TOPSs and monitor PDs are connected to a feedback circuit for automatic control. Fig. 6.13(b) shows the constellation that was constructed from the post-FFE 16QAM histogram data in Fig. 6.14. For clear visualization, the histograms with 256 bins were smoothed with a 4 bin moving average. In the IMDD PAM4 configuration, a BER penalty is incurred due to equal TX laser splitting to all four MZM paths and from using a single-ended photodiode connection to the TIA. Overall results of the histogram and BER analysis are shown in Table 6.3, including linearity analysis based on level mismatch separation ratio (R_{LM}) [284], where normalized separations of 0.33 for all levels results in $R_{LM} = 1$. Measurements with a single 16QAM quadrature channel were included to assess the impact of IQ crosstalk on BER and level histograms. With more than an order of magnitude increase in the BER for full IQ modulation compared to single quadrature, there is a clear penalty from crosstalk and reduced level separation, but the BER is still below the KP4-FEC threshold. Imperfect biasing of the phase tuners for the transmitter IQ quadrature and the receiver 90° hybrid can both contribute to IQ crosstalk. With higher signal input power, there will also be more nonlinear phase and amplitude noise [264, 261] caused by self-gain and self-phase modulation [263, 262] that will impact the BER. Power consumption in IMDD / coherent modes, not including DSP, was 0.87 W / 1.62 W for the TX (driver+PIC) and 0.33 W / 0.62 W for the RX (PIC+TIA). For the PAM4 power consumption, only the power of the active channel is included for the driver and the TIA to provide a fair comparison between the modes.

An O-band coherent link capable of programmed interoperability with IMDD using tunable couplers has been presented with BERs below the KP4-FEC threshold and

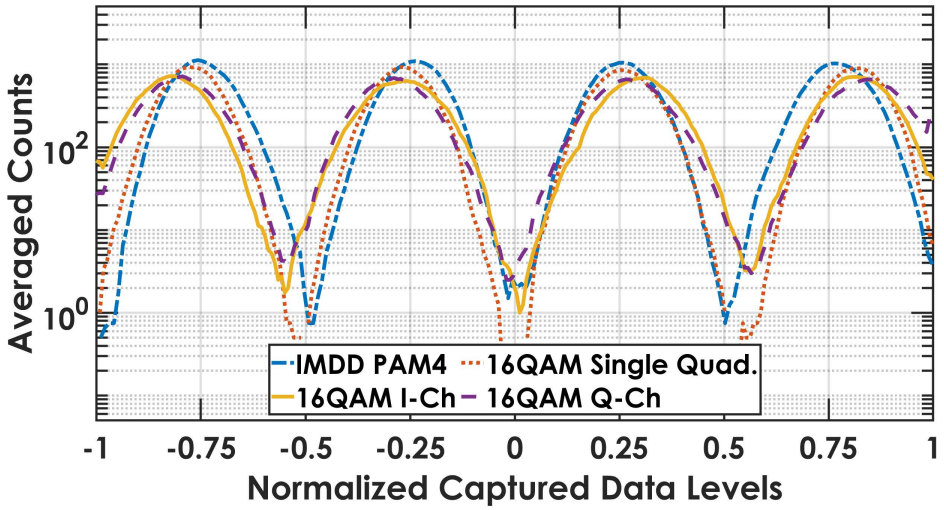


Figure 6.14: Smoothed post-FFE memory capture histograms.

Table 6.3: Full Link Performance Extracted from DSP Memory Capture Analysis

Modulation format	IMDD PAM4	16QAM Single Quadrature	16QAM I-Ch	16QAM Q-Ch
R_{LM}[284]	0.96	0.89	0.85	0.84
Normalized Minimum Level Separation	0.33	0.32	0.31	0.31
Normalized Maximum Level Separation	0.34	0.35	0.35	0.35
Minimum BER	2.80×10^{-5}	3.05e-6	1.22e-4	6.93×10^{-5}
Energy Consumption (pJ/bit)	12.0	-	11.2	

minimum energy consumption of 11.2 pJ/bit. Both 53.125 Gbaud 16QAM and PAM4 transmission are shown using custom TX and RX PICs with commercial drivers, TIAs, and a 100G PAM4 DSP, for single-λ data rates of 200 Gbps and 100 Gbps, respectively. Future work will focus on implementing automatic polarization tracking in the RX subsystem that will enable transmission experiments through various fiber lengths to quantify reach limits and power penalties. The MDC link architecture demonstrated here is promising for data center and AI/ML applications that require large link budgets and compatibility with established IMDD technology.

Chapter 7

Conclusion

7.1 Outlook on Data Centers and Coherent Links

It is evident from recent trends that AI/ML workloads will be a major driving force for the design of the next generation of data centers. The advent of large language model AI from OpenAI, Google, Microsoft, Meta, and other companies has accelerated the demand for data centers running AI training and inference. NVIDIA continues to push the boundaries of GPU hardware for AI with the announcement of their Grace Blackwell 200 Superchip which powers their DGX GB200 systems which can be connected together in their DGX SuperPOD [285]. Google, Microsoft, Amazon, and Oracle have already announced plans to incorporate the new Blackwell systems into their data centers [286]. Discussions at OFC 2024 further solidify the prominent role of AI for the data center transceiver market [287, 288]. Market analysis from LightCounting shows that Microsoft and Google have increased their spending by 66% and 91% year-over-year for AI infrastructure, contributing to the 85.5% and 164% year-over-year growth in revenue at Eoptolink and Innolight [289]. Overall data center spending forecasts expect a 24.1% increase in 2024, reaching $293.09 billion [290]. Silicon PICs are expected to gain market

share from AI applications with sales increasing from $0.8 to $3 billion by 2029 [291].

The demand is clear, but there is some uncertainty regarding the data center architecture and hardware requirements that will enable optimal performance for AI applications. The very large, distributed computation requirements of AI demand a significant increase in bandwidth which leads to higher density connections that can consume >100 kW per rack. The power requirements are scaling beyond what current data centers are able to handle and thermal management via liquid cooling is often necessary. NVIDIA's DGX GB200 systems are liquid-cooled. To reduce the runtime of AI programs, minimizing packet loss and low probability "tail" latency events is critical, with Meta showing that AI/ML workloads spend 30% of the time waiting for the network [13, 292]. While traditional data centers can handle some penalty from latency and packet loss, the massive parallelism and batch processing in AI applications greatly increases the sensitivity to low probability delays which slow down the set of dependent computations. There are several solutions to address the challenges with power consumption, latency, and bandwidth requirements for future AI clusters.

7.1.1 Solutions for Reduced Power Consumption

As discussed in Section 1.2, power consumption can be reduced in several areas from individual links to the data center network. Energy efficiency of EICs will continue to improve with more advanced process nodes (i.e. 5 to 3 nm) and improvements in DSP design [71, 293], but more significant improvements can be achieved at the module and system level. One the module level, linear-drive optics removes the DSP between the switch ASIC and the transmitter to save power. This solution has been studied by Arista and other companies [294] who have partnered together to create a multi-source agreement [295]. Eoptolink has already demonstrated linear-drive pluggable optics

(LPO) modules at OFC [296]. The excitement around LPO may have a short lifespan as analysis by Meta showed that it will be challenging for 200G/lane LPO to meet the requirements for receiver sensitivity [297]. Also on the module level, as discussed in Section 1.2.2, co-packaged optics (CPO) provides power savings compared to pluggable optics. Broadcom has been leading the way with their 51.2T Tomahawk5-Bailly CPO Switch, partnering with Bytedance, H3C, Juniper Networks, and Micas Networks to incorporate their CPO solution into switch platforms [298]. Cisco's demonstration of a 25.6T switch with 22% power reduction compared to a switch with pluggable transceivers helps bolster the market adoption of CPO. With multiple CPO suppliers, data center operators, such as Meta and Amazon, will be more willing to deploy CPO switches, but Google remains skeptical of their reliability. Market forecasts expect the demand for CPO to ramp up from a few thousand per year in the next 2-3 years to over 100 thousand by 2029, capturing 10 to 15% of the Ethernet switch market [298, 67]. On the system level, migrating from electrical switches to optical circuit switches (OCS), discussed in Section 1.2.3, led to reduction of 30% in capital expenditure and 41% in power for Google. In 2024, Google remains the only major data center that incorporates optical switching, but the market is expected to expand with other data centers adopting OCS in the coming 3 to 5 years, reaching close to the same production level as Google's internal OCS manufacturing [67].

7.1.2 Solutions for Reduced Latency

Addressing latency for AI clusters is a system level problem that can be addressed both in software and hardware. As mentioned earlier, the latency of the overall network or the tail latency is the primary concern for AI programs. While OCS can reduce the latency of connections by removing the data conversion that happens in electric switches, it

does not necessarily improve the overall speed of the network to complete a job. Network latency can be improved by optimized load balancing of the computation and bandwidth requirements, workload scheduling from end-to-end, incorporating seamless switching to new connections for zero impact failover from bad connections, and minimizing the number of hops between ends with a high-radix fabric design [292]. With traditional electrical packet switches, traffic can be dynamically rerouted, but they are delayed by saving the packet in the switch memory buffer and waiting in a queue before transmission to the next node. Packets will often traverse different paths through a network which can increase the tail latency. With OCS, data is sent continuously from end-to-end, which can reduce latency, but there must be a software defined topology and traffic engineering control loops to optimize the throughput and adjust to changing traffic [62]. Google has demonstrated better performance in ML workloads, compared to NVIDIA A100, using their TPU v4 ASIC with OSC connected in a 3D torus [265]. They also showed that the OCS dynamic topology reconfiguration enables 1.5 to 3.3× speed improvement compared to a static topology [63]. For data centers without OCS, software defined networks and different network topologies can reduce network congestion, improve load balancing, and provide more fault tolerance for better network latency [299, 300, 301, 302].

7.1.3 Solutions for Increased Bandwidth

Increasing link bandwidth in data center networks can be achieved by:

- electrical modulation baud rate (50 to 200 Gbaud)
- modulation format (PAM4, PAM8, 16QAM)
- wavelength multiplexing (CWDM, DWDM)
- polarization multiplexing
- spatial division multiplexing (SDM)

where there are trade-offs in link sensitivity, energy efficiency, cost, and implementation challenges for the different methods.

Bandwidth scaling in short-reach links has typically been increased by raising the electrical modulation rate. This method keeps the overall transceiver complexity low by maintaining the component count, only replacing existing hardware with higher bandwidth parts. The current generation of transceivers is using approximately 50 Gbaud modulation, with a few 100 Gbaud transceivers entering the market. Transmitters using standard SiP processes have been demonstrated at >100 Gbaud using: TWMZMs [126], slow-light TWMZMs[129], ring modulators [303], and SiGe EAMs [130], with >200 Gbaud PAM2 achieved after applying equalization to the received signal [303]. A 200 Gbaud PAM4 link has not been achieved with standard SiP processes to my best knowledge. Adding new materials to SiP processes has enabled higher bandwidth and better modulation efficiency. Thin film lithium niobate (TFLN) [31, 109, 131] and plasmonic[108, 304] MZMs have been able to achieve net 400 Gbps IMDD modulation. Silicon-organic hybrid [105], barium titanate [106], and heterogeneously integrated III-V EAM [58] devices are also close to achieving net 400G. On the receiver side, there have been several demonstrations of Ge-based PDs with >60 GHz bandwidth [120] with IHP holding an unrivaled record of 265 GHz bandwidth while maintaining a 0.3 A/W responsivity [119]. InP-based devices are also approaching a 200 Gbaud PAM4 demonstration with 160 Gbaud PAM4 shown recently using the SMART Photonics process [123] and NTT presenting a 100 GHz bandwidth TWMZM [88]. For receivers using III-V materials, waveguide integrated PDs with >100 GHz BW have existed for more than 10 years [117], and recent work has demonstrated modified uni-traveling-carrier PDs with 153 GHz, 0.38 A/W [118] and 220 GHz,0.24 A/W [116]. Many III-V modulator and receiver components, including the references above, are targeting longer reach applications using 1550 nm, but they could be adapted to O-band applications with modifications to the

epitaxial design.

Additional link bandwidth can also be achieved by increasing complexity of the modulation format. PAM4 is the standard for intra-data center communications, and it is built into the Serializer/Deserializer (SerDes) electronics which send/receive data from the transceivers, so there is a high barrier to change the modulation format; however, by switching the optical modulation to 16QAM, it is possible to treat the IQ channels as two separate PAM4 data lanes. This was one of the motivating factors for the link presented in Section 6.2. Coherent has already been adopted for >10 km data center interconnect (DCI) with the OIF 400ZR agreement [305], and the benefits of coherent for short reach links have been a topic of discussion for several years [16, 17, 30, 254, 257]. There is an increasing probability that coherent modulation will be implemented in < 2 km links in the 3.2 Tb/s generation of transceiver links.

Some data center transceivers (e.g. 400G-FR4) utilize multiple wavelength channels with CWDM. While 4 or 8 wavelengths is typical today, the number of wavelength channels is expected to rise to 16 or 32 in the coming years, with the CW-WDM MSA helping to define the wavelength grid and laser output specifications. With increasing power and tighter wavelength spacing, the TX launch power must be limited for IMDD links to avoid BER penalties from four-wave mixing (FWM). With coherent modulation, the null bias point leads to lower TX launch power, so it is able to be scaled with less impact from FWM.

Polarization multiplexing has not been traditionally used in IMDD transceivers, and it is demodulated using DSP for traditional coherent transceivers. There have been efforts to manage polarization control in the optical domain with analog feedback loops as mentioned in Section 6.2.1. For IMDD links, it is easier to scale the number of wavelength channels until FWM becomes a problem, since implementing polarization control adds more complexity to the link. To address bandwidth scaling needs, DP-PAM4 has recently

been developed by Aloe Semiconductor using optical polarization control. A 106 Gbaud DP-PAM4 system was demonstrated at ECOC 2024 in collaboration with Broadcom and Eoptolink [306]. For coherent, polarization multiplexing can enable a self-homodyne link (mentioned in Section 6.2) where the transmitter launches the modulated data and a CW carrier on orthogonal polarizations and utilizes existing IMDD DSP.

Spatial division multiplexing is another method that has gained support for increasing the capacity of data center interconnects [307, 308, 309, 310, 311]. The simplest form of SDM is a standard fiber bundle, but more compact solutions involve multi-core fiber (MCF). Replacing a single core with several ideally uncoupled cores is one MCF solution. For data centers, MCF is able to improve the density of connections from PIC to fiber, increase the front panel bandwidth density, and reduce the overall fiber count. Other MCF solutions involve multiple larger cores for few-mode fibers (FMF). These fibers utilize mode division multiplexing (MDM) in addition to multi-core SDM, but they require carefully designed passive elements for mode MUX and DEMUX. To undo the effects of differential mode delay and spatial mode crosstalk, MIMO DSP is also required with complexity that scales with the number of modes [312, 313]. While their are many challenges to solve - compatibility with existing fiber, attachment to PICs, manufacturing maturity, cost, inter-core skew, DSP requirements, crosstalk, and others - MCF has the potential to improve bandwidth density and reduce packaging complexity for short reach applications when the technology is more mature. MCF is entering the market with Furukawa OFS and Sumitomo leading the development of MCF products [314]. Google recently partnered with NEC to use Sumitomo's 2 core fiber in the Taiwan-Philippines-U.S. submarine cable deployment which is currently under construction [315]. With more deployments, the manufacturing will mature, prices will reduce, and other challenges with packaging, maintenance, and impairments will also improve. If MCF adoption continues to increase, it may become a viable option for the data center within

the next decade as demands on bandwidth density increase.

While increasing the baud rate with higher electrical bandwidth has been the prevailing focus for many years, the explosion of AI and its bandwidth requirements has prompted data center operators and transceiver vendors to invest more in WDM. Since adding more parallel wavelengths does not require any significant change from the current data center designs, higher channel count WDM will likely be adopted in the near future. WDM nonlinear impairments will lead to higher link penalties as the number of wavelengths grows, and larger networks with optical switching may require increase link budgets. In these cases, coherent modulation with light DSP and polarization multiplexing become more attractive. With SDM, unless advancements are made very quickly which develop into a mature solution, it will likely be the last method implemented by data centers. While data center operators typically support the solutions with the lowest cost, best reliability, and smallest barrier to adoption, there are diverse requirements for different data centers and for different reaches within a data center campus. All of these solutions may find their niche in the coming years with varying levels of adoption.

7.2 Summary of Work

This work has covered PIC design, fabrication, and testing for multiple short-reach, O-band coherent links. To pursue the power savings of analog coherent with an OPLL, two generations of InP receivers were designed and fabricated. The first generation PICs exhibited slightly less than the desired performance, but showed promise for future improvements as described in Section 3.3 & 3.4. Using the results from the InP gen. 1 RX, several changes were made to the design for performance improvements as discussed in Section 4.1. Issues with fabrication, explained in Section 4.2 prevented detailed testing of the gen. 2 RX, but important lessons, covered in Section 4.4 were learned which will

help mitigate risks with future InP transmitter processing by Xinhong Du.

SG-DBR lasers and two generations of TX and RX PICs (with/without) integrated lasers, depicted in Chapter 5, were successfully designed, fabricated with Intel's heterogeneous III-V on Si photonics process, and tested. High speed capabilities of the PICs up to 100 Gbaud DP-QPSK and 60 Gbaud 16 QAM were demonstrated using an intradyne coherent link in Section 6.1. In Junqian Liu's upcoming publications, he will also show DP-QPSK demonstrations of these PICs packaged with OPLL electronics. A 53 Gbaud 16QAM demonstration of a mixed domain coherent link was presented in Section 6.2 with transmission below the 2.4×10^{-4} KP4 FEC threshold. This link architecture provides a promising path for intra-data center architectures utilizing optical switching.

7.3 Future Work

Due to the difficulty of InP fabrication and the limited benefits of single polarization InP coherent RX PICs, future work that builds on the gen. 2 InP RX may not be a worthwhile pursuit. The Intel alpha receiver has more functionality and better performance. Junqian Liu will show more work using that PIC for analog coherent links with an OPLL, and future work is planned to improve the feedback loop electronics. Improvements to the RX PIC for the OPLL are possible using the Tower Semiconductor PH18 process which includes integrated lasers and detectors. While further work on the InP RX may not be productive, the material properties of InP lead to high modulation efficiency and the potential for high bandwidth, which are good incentives to warrant further work on TX PICs. Integrated lasers, SOA signal amplification, and power efficient modulation are all advantageous for data center applications. This work is currently being led by Xinhong Du.

For mixed domain coherent, as mentioned in Section 6.2.3, a functional polarization

recovery feedback loop is needed to demonstrate the full capabilities of the coherent link. Lucidean is leading the development of the algorithms and circuits for the transmitter and receiver biasing and detection which enable the analog polarization and phase recovery. I have joined the company and am assisting with these efforts while also pursuing the next generation of the mixed domain coherent link, targeting 106 Gbaud modulation. After the circuits and algorithms for a stable feedback loop are established, more detailed link sensitivity, robustness to polarization disturbances, and polarization dependent loss are important aspects of the link that warrant further characterization.

Appendix A

MATLAB Code

A.1 MMI Transmittance

The code below was used to generate Fig 2.5 and 2.6.

```
close all;
clear variables;

points = 100;
dphi = linspace(-pi/2,pi,points);
Elo = exp(-1i*pi/4)*ones(1,points);
t1 = 0;
t2 = [-pi/4,0,pi/4];
Es = exp(1i.*dphi);
E_in = [Es; Elo; zeros(1,points); zeros(1,points)];

K_T1 = sqrt(1/4);
K_T2 = sqrt(1/2);


%% 2x4 hybrid (2x4MMI, phase shift, 2x2MMI) output calculation
for q=1:length(t2)
T1 = [1, exp(-1i*3*pi/4), 0, 0;
    exp(-1i*pi/4), 1, 0, 0;
    exp(-1i*pi/4), 1, 0, 0;
    exp(-1i*pi), exp(1i*pi/4), 0, 0];
```

```
TPS = [1,0,0,0;
    0,1,0,0;
    0,0,exp(-1i*t1),0;
    0,0,0,exp(-1i*t2(q))];
T2 = [1,0,0,0;
    0,1,0,0;
    0,0,K_T2,K_T2*exp(1i*pi/2);
    0,0,K_T2*exp(1i*pi/2),K_T2];

T_2x4(:,:,q) = K_T1*T2*TPS*T1;

for m = 1:points
    E_out_2x4(:,m) = T_2x4(:,:,q)*E_in(:,m);
end

figure(q);
axis tight
styles = {'k:','k-','k--','k-.'};
for r=1:4
 plot(dphi*180/pi,abs(E_out_2x4(r,:)).^2,styles{r},'LineWidth',2)
 hold on
end
legend('out1','out2','out3','out4',...
'Orientation','horizontal',Location='southwest')
ylabel('Relative Transmittance')
xlabel('\Delta\phi')
xlim([-90 180])
ylim([0 1])
xticks([-90 -45 0 45 90 135 180])
title(['2x4 MMI with \pi/',num2str(pi/t2(q)),' Shift'])
fontsize(gcf,scale=3)
figurePosition = [0, 0, 600*1.3, 800*1.3];
set(gcf, 'Position', figurePosition);
hold off;
end


%% 4x4 MMI output calculation
q=q+1;
Elo = exp(1i*pi/4)*ones(1,points);
E_in = [Elo;zeros(1,points); Es; zeros(1,points)];
```

```
T_4x4 = [1, 0, exp(-1i*pi/4), 0;
    exp(3i*pi/4), 0, 1, 0;
    exp(-1i*pi/4), 0, 1, 0;
    1, 0, exp(3i*pi/4), 0];
for m = 1:points
    E_out_4x4(:,m) = K_T1*T_4x4*E_in(:,m);
end

figure(q);
hold on;
for r=1:4
 plot(dphi*180/pi,abs(E_out_4x4(r,:)).^2,styles{r},'LineWidth',2)
end
legend('out1','out2','out3','out4',...
'Orientation','horizontal',Location='southwest')
ylabel('Relative Transmittance')
xlabel('\Delta\phi')
xlim([-90 180])
xticks([-90 -45 0 45 90 135 180])
ylim([0 1])
title('4x4 MMI')
fontsize(gcf,scale=3)
figurePosition = [800, 0, 600*1.3, 800*1.3];
set(gcf, 'Position', figurePosition);
hold off;

qtemp=q;

%%2x2 MMI style hybrid

%check output using 90 shift on each arm
t = [pi/2,0,0,0;
    0,pi/2,0,0;
    0,0,pi/2,0;
    0,0,0,pi/2];
arm ={'\theta_1','\theta_2','\theta_3','\theta_4'};

for q=1:length(t)
Elo = exp(1i*0)*ones(1,points);
E_in = [Elo;zeros(1,points);zeros(1,points);Es];
```

```
TPS = [exp(1i*t(1,q)),0,0,0;
    0,exp(1i*t(2,q)),0,0;
    0,0,exp(1i*t(3,q)),0;
    0,0,0,exp(1i*t(4,q))];

T2x2 = [K_T2,K_T2*exp(1i*pi/2),0,0;
    K_T2*exp(1i*pi/2),K_T2,0,0;
    0,0,K_T2,K_T2*exp(1i*pi/2);
    0,0,K_T2*exp(1i*pi/2),K_T2];

for m = 1:points
 E_temp = TPS*T2x2*E_in(:,m);
 E_temp2 = E_temp; E_temp2(2) = E_temp(3); E_temp2(3)=E_temp(2);
 E_out_2x2hybrid(:,m) = T2x2*E_temp2;
end

figure(q+qtemp);
hold on;
for r=1:4
 plot(dphi*180/pi, abs(E_out_2x2hybrid(r,:)).^2,styles{r},'LineWidth',2)
end
legend('out1','out2','out3','out4',...
'Orientation','horizontal',Location='southwest')
ylabel('Relative Transmittance')
xlabel('\Delta\phi')
xlim([-90 180])
xticks([-90 -45 0 45 90 135 180])
ylim([0 1])
title(['2x2 array Hybrid with ',arm{q},'=\pi/',num2str(pi/t(q,q))])
fontsize(gcf,scale=3)
figurePosition = [1600, 0, 700, 800*1.3];
set(gcf, 'Position', figurePosition);
hold off;
end
```

Appendix B

InP Process Flows

B.1 Generation 1 InP RX Process

The process flow used for the first generation InP receiver processing is presented in detail with Fig. B.1 through B.16. This process was completed in January 2019, so the available tools and the configuration of some tools (e.g. PECVD #1, RIE #3, E-beam #1) have changed since that time. New tools have also become available (e.g. MLA and Oxford Cobra) which offer alternative methods for certain process steps. Nevertheless, this process is a useful reference for future InP processing.

B.2 Generation 2 InP RX Process

Some of the steps for the second generation InP receiver processing are presented in detail in this section. The full details of the process are not included for brevity, since many of the steps follow a similar flow to the gen 1. RX process. This process was completed in May 2023, so the available tools and configuration of some tools have likely changed since that time.

Equipment	Description	Key Parameters
Active Passive Area Definition		
SiN Deposition: 1000Å		
Solvent Bench	ACE/IPA/N2 Dry	2'
UV Ozone	UVO3, 10min warm up + 10 min bake	10'
HF Bench	BHF Clean/DI/N2 Dry	2'
PECVD	Chamber clean : CLNSIN30, SiN deposition: SiN10 (100nm) Si3N4 is better than SiO2 because SiO2 might delaminate	100nm
Ellipsometer	Measure SiN thickness	
Microscope	Check for surface roughness or pinholes	
AP lithography, GCA 6300 Stepper#1		
Solvent Bench	ACE/IPA/N2 Dry ~2' total	2'
Spinner	Prebake @135C/2min	1'
	HMDS, soak first for 20-30sec then spin 3krpm/30"	3krpm/30"
	Use Blue tape, SPR955-0.9,soak first for 20-30sec then spin 3krpm/30"	3krpm/30"
	Bake 95C, 90" , cool for 60"	90"
Stepper 1	Load mask: new mask for AP/Schow	
	Chuck 1/4 of 2" (620-820)um; Shim=260um	
	Exposure: 1.4", FOC=2, EX TEST1, pass:1	**1.4", focus=2**
	PEB 110C , 90" , cool for 60"	90"
Developer Bench	AZ300 MIF develop for 55"	55"
	DI Rinse, N2 blow dry	
Microscope	Inspect features, if necessary, wet for +20" in DI, +10" MIF300, and rinse in DI	Save 2-3 images
Dry Etch SiN		
PE 2	O2 Plasma 300mT/100W for 10" to clean surface	10"
ICP-2	Coat Recipe 104 (CHF3/CF4/O2) 500 W for 5' (35/5/10), 500W/50W, 0.5Pa-for stright sidewalls	5'
	Run Recipe 104 for 1' to etch	1'
	O2 Clean Chamber for 10'	10'
	Rinse sample soon after done to stop etching reactions	
Filmetrics	Check the etched area to make sure the SiN is gone	
Strip Photoresist		
Solvent Bench	Soak in NMP with change over	10'+
	IPA/DI/N2 Dry	2'
Gasonics	Recipe 2 (200C)	180"
Microscope	Inspect for PR "ribbons", repeat cleaning if needed	Save 2-3 images
Dektak	check that etched step height is 100 nm	
Wet Etch QWs		
Acid Bench	NH4OH:DI=1:10 (Not required but helps remove surface oxidation for more uniform wet etch)	20"
	Etch InP: HCl:H3PO4=1:3 ~200ml	~30sec
	(add HCl to H3PO4 when making solution)	
	DI Soak/N2 Dry (rinse thoroughly since H3PO4 is viscous)	2'
	Etch InGaAsP: H2SO4:H2O2:DI=:1:1:10 , do it slowly	~4 min total
	Mix H2SO4 and H2O (1:10), let cool 30min	
	Measure 100ml of H2O and add 10ml of H2SO4 to water	
	Add H2O2(1part) which is 10ml of fresh H2O2, wait 5-10min before doing etch	
	Etch slowly (1' 30" +1' 30" + 30"+15"+15"+10"…)	
	DI Soak/N2 Dry	1'
Strip SIN		
Acid Bench	BHF dip 5'	**5'**
	DI rinse 1-2', N2 blow dry	**1-2'**
	Dektak (optional to double check etched thicknes)	

Figure B.1: Process flow Steps for active-passive area definition

Equipment	Description	Key Parameters
Gratings		
SiO2 Deposition: 500Å		
Solvent Bench	ACE/IPA/N2 Dry	2'
UV Ozone	UVO3 10min warm up	10'
HF Bench	BHF Clean/DI/N2 Dry	2'
PECVD	_CLNSIO30/_SiO05 (chamber clean and SiO dep)	**50nm**
Ellipsometer	measure SiO2 thickness	
E-beam Grating Lithography (Bill Mitchell)		
Solvent Bench	ACE/IPA/N2 Dry	2'
Spinner	Prebake 100C+	1'
	Spin 2:1 CSAR:Aniso	5000rpm/30"
	Bake 180C	5'
E-Beam Litho	Chuck 5, 5th Lens, 500 pA, 220 J/cm2, 88nm line, 300 uC/cm^2 dose	
Developer Bench	1:1::MIBK:IPA	60"
	50:1::MIBK:IPA + N2 Dry	30"
Microscope	Inspect Grating Regions	Save 2-3 images
Dry Etch SiO2		
ICP-2	Coat Recipe 108 (CHF3/CF4/O2)=40/0/10 500W/50W, 0.5Pa	5'
	Run Recipe 108 - Goal 50 nm etch	~45"
	O2 Clean	10'
	Rinse sample soon after done to stop etching reactions	
Strip E-beam Resist		
Solvent Bench	Soak in NMP/80C	30'+
	IPA/DI/N2 Dry	2'
Gasonics	Recipe 2 (200C)	180"
Microscope	inspect etched gratings profile in SiO2	Save 2-3 images
AFM	Check SiO2 etch depth	50nm
RIE#2: Dry Etch		
RIE 2	Clean - O2 20 sccm 500V 125 mT	30'
	Coat - MHA::4:20:10 sccm 500V 75 mT	20'
	Etch - MHA::4:20:10 sccm 170V 75 mT InP Rate: ~80 nm/min, InGaAsP Rate: ~30 nm/min	Goal: 100 nm
	Post Clean - O2 20 sccm 300V 125 mT	10'
	DI Soak/N2 Dry	1'
Microscope	examine grating etch for any obvious defects	Save 2-3 images
AFM	Check etched depth and roughness	
SEM	Check duty cycle and roughness	
Strip SiO2		
HF Bench	BHF 5'	5'
	DI rinse 1-2', N2 blow dry	2'
Wet Etch Clean up -- run the following steps right before regrowth		
Acid Bench	Grating Cleanup H2SO4	20"
	DI Soak/N2 Dry	1'
Regrowth Prep		
UV Ozone	Heat up	**10'**
	Ozone clean	**60'**
HF Bench	BHF Dip	1'
	DI Soak/N2 Dry	1'
	Picking up sample in gowning room	
MOCVD Lab	InP (p-cladding)	1850
	InGaAs (p-contact)	100
	InP (protective cap)	500
	Dropping off sample in gowning room when done	
Microscope	Check surface for roughness, defects, growth abnormalities	

Figure B.2: Process flow Steps for grating definition

Equipment	Description	Key Parameters
Waveguide lithography		
Dielectric Deposition: SiN 2000Å / SiO2 2000Å		
Solvent Bench	ACE/IPA/N2 Dry	2'
UV Ozone	UVO3, 10min warm up + 10 min bake	10'
HF Bench	BHF Clean/DI/N2 Dry	2'
PECVD#1	_CLNSIN30/_SiN20, dep. time=17'14.5"	200nm
PECVD#1	_CLNSIO30/_SiO20, dep. time=4'52.4"	200nm
Ellipsometer	check dielectric thickness for test piece	200 nm SiO2 on 200 nm SiN
Filmmetrics	check dielectric thickness for on real sample	200 nm SiO2 on 200 nm SiN
WG Lithography, Autostep 200, LOG IN [10,71]		
Solvent Bench	ACE/IPA/N2 Dry	2'
Spinner	Prebake 135C/5min, cool for 1 min	5' , 1'
	PE-II O2 plasma (use left asher), 20sec	20"
	Use BLUE tape for spinning, important for uniformity of resist across a quarter and keeping back side clean	
	Use small chuck for spinning resist, important for uniformity	
	HMDS, apply and let it soak for 20sec	3krpm/30"
	bake HMDS@100C/1min, cool down for 1 min	1' , 1'
	Use BLUE tape for next layer	
	SPR955-0.9 (poured fresh resist), apply and soak for 20sec	3krpm/30"
	Bake 95C/1min, cool for 1 min	1' , 1'
Stepper 2	LOG IN [10,71] , WG mask , Chuck 1/4 2"/500um/ Shim180um	
	EX RECV1/pass [EXP=0.38", FOC=+3] (pass=1 is for BR orientation, pass=2 is for BL orientation)	0.38/+3
	PEB 110C /1min, cool for 1 min	1',1'
Developer Bench	AZ300 MIF	55"
	DI Rinse, N2 blow dry	
Microscope	Inspect features, +10" MIF300 if necessary	Save 2-3 images
PE 2	O2 Plasma 300mT/100W to descum residual PR	~10"
Dry Etch SiNx		
ICP-2	**Selectivity of ICP-2 etch (1.25 to 1.5:1)= resist to dielectric**	
	Coat Recipe 104 (CHF3/CF4/O2) 500 W for 5' (35/5/10), 500W/50W, 0.5Pa-for stright sidewalls	5'
	Run Recipe 104 for 5'20" to etch (some overetch)	5'20"
	O2 Clean Chamber for 10'	10'
	Rinse sample soon after done to stop etching reactions	

Figure B.3: First part of process flow steps for InP waveguide ridge etch.

Strip Photoresist		
DUV	5' flood exposure for removing resist	5'
Developer Bench	AZ 300 MIF develop	2'
Solvent Bench	Soak in NMP with change over	30'+
	IPA/DI/N2 Dry	2'
Gasonics	Recipe 2 (200C)	180"
Microscope	Inspect for PR "ribbons"	Save 2-3 images
Solvent Bench	More cleaning if needed. MAke sure sample is clean!	
Gasonics	Recipe 2 (200C)	180"
Dektak	mesure SiN+SiO2 thickness on a few dies	410 to 440 nm
Filmetrics	200 nm SiO2 on 200 nm SiN (optional recheck)	200 nm SiO2 on 200 nm SiN
Dry Etch with Unaxis		
Unaxis ICP	**Clean** - O2 clean @200C, use double side polished Si wafer	30'
	Coat - Cl2:H2:Ar::6:13:2 sccm 125/800W 1.4 mT, load dummy InP sample approximatelly in the center of 1mm thick double side polished Si wafer	15'
	Surface Prep - NH4OH:DI=1:1 Dip for 1min	1'
	Apply grease by using wooden q-tip. Use wooden side, and gently spread grease on the wafer. Apply in thin layer and area shuld be a little bit smaller then sample size. Place sample on Si wafer. Use 2 Q-tips (cotton side), and genlty push diagonal sides of the quarter, and twist left/right and up and down. Make sure sample is sitting FLAT. Make sure that grease is not coming on sides. If it does, it would get on your sample, and there is NO WAY to remove the grease. Use tweezers and gently push sample on the carrier. If there is any grease beside the sample CLEAN it. Use Q-tip and ISO to remove any grease. Use N2 gun and genly blow dry the surface.	
	Etch - Cl2 : H2 : Ar :: 6.3 : 12.7 : 2 sccm 125/800W 1.4 mT ~1 um/min InP rate , InP : SiO2 :: ~1:11.5 etch selectivity	2'
	DI Soak/N2 Dry	
Microscope	Inspect features and measure dimensions of WG structures	
Dektak	measure thickness of etched ridge + remaining dielectric	
Filmmetrics	measure thickness of remaining SiO2+SiN on top of ridges	
Wet Cleanup Etch InP		
Acid Bench	Etch InP: HCl:H3PO4::1:3 ~200ml	30" + 15" + ...
	DI Soak/N2 Dry	1'
Dektak	InGaAsP is pretty resistant to this wet etchant. So longer etch time will not be a problem. Measure thickness until etching stops.	2.8 to 2.9 um
Strip SIN and SIOx		
HF Bench	BHF dip 5'	5'
	DI rinse 1-2', N2 blow dry	2'
Dektak	measure thickness of ridge after removing dielectric	2.5 to 2.6 um
Microscope	Take some pictures of ridge structures	

Figure B.4: Continued process flow steps for InP waveguide ridge etch.

Equipment	Description	Key Parameters
Isolation _SSA		
Dielectric Deposition: 5000Å		
Solvent Bench	ACE/IPA/N2 Dry	2'
PE 2	O2 Plasma 300mT/100W	30"
HF Bench	BHF Clean/DI/N2 Dry	2'
PECVD	_CLNSIN30/_SiN20, 200nm of SiN	200 nm
	_CLNSIO10/_SiO20, 200nm of SiO2	200 nm
	_CLNSIN10/_SiN10, 100nm of SiN	100 nm
Ellipsometer	check 100 SiN on 200 nm SiO2 on 200 nm SiN on test piece	100 / 200/ 200 nm
Filmmetrics	check 100 SiN on 200 nm SiO2 on 200 nm SiN on real sample	100 / 200/ 200 nm
ISO SSA Lithography, Autostep 200, LOG IN [10,71]		
Solvent Bench	ACE/IPA/N2 Dry	2' each
Spinner	Prebake 135C/5min, cool for 1 min	5' , 1'
	PE-II O2 plasma (use left asher), 20sec	20"
	Use BLUE tape for spinning, important for uniformity of resist across a quarter and keeping back side clean	
	Use small chuck for spinning resist, important for uniformity	
	HMDS, apply and let it soak for 20sec	3krpm/30"
	bake HMDS@100C/1min, cool down for 1 min	1' , 1'
	Use BLUE tape for next layer	
	SPR220-7 -- step 1: 3500rpm/150rpm/45s; step2: 0/1000/0	45" for 3.5krpm
	Bake 95C	3'
Stepper 2	SSA ISO mask , Chuck 1/4 2"/500um/ Shim180um	
	Exposure: RECALL\pass [EXP=0.45", FOC=0] (pass=1 is for BR orientation, pass=2 is for BL orientation)	0.45"\0
	let sample sit for 20min to avoid bubble formation	20'
Developer Bench	AZ300 MIF Develop	70"
	DI Rinse, N2 blow dry	60"
Microscope	Inspect features	save some images
Etch Back Photoresist to expose ridge top		
RIE 3	Clean O2 20sccm/50mT/500V	30'
	O2 Etch 20sccm/10mT/200V	5' steps
	Clean O2 20sccm/50mT/500V - reclean chamber after ~20'	30'
	O2 Etch 20sccm/10mT/200V	2' steps near end
	O2 Clean , clean the tool, sample taken out	10'
Microscope	inspect when rainbows appear from thin photoresist and when they are gone from complete removal of photoresist	
SEM	Check in SEM to see the ridge above the photoresist	
Dry Etch SiNx		
ICP-2	**Coat - Recipe 104** (CHF3/CF4/O2)=35/5/10, 500W/50W, Presure=0.5Pa	5'
	Etch - Recipe 104 (CHF3/CF4/O2)=35/5/10, 500W/50W, Presure=0.5Pa, time = 5'30"	Goal: etch ~>500 nm
	SiO2 etch 70 to 85 nm/min, SiN etch 160 to 180 nm/min for rough approximation of etch rate. Exact values will vary based on tool, total area exposed, and aspect ratio of openings	5'30" estimate
Microscope	microscope inspect to see if color is gone on ridge tops	
ICP-2	Run Recipe 104 again if more time needed for etch	15" more if needed
	O2 Clean Chamber for 10'	10'
	Rinse sample soon after done to stop etching reactions	
SEM	Check in SEM to see clean ridge tops (optional)	

Figure B.5: First part of process flow steps for p-InGaAs isolation etch.

Wet Etch InP and InGaAs		
LEXT, Confocal microscope	Inspect the SSA openings before wet etch steps	
Acid Bench	NH4OH:DI=1:10	20"
	DI Soak/N2 Dry	
PE-II	help with hydrophilic surface properties	
Acid Bench	Etch InP H3PO4: HCl=3:1 ~200ml (120ml:40ml)	30"+30"
	In this InP etch we should etch ~500nm of InP, which will take~1min. We cannot see bubbles, because etching areas are small.	
	DI Soak/N2 Dry	1'
microscope	Use bright field and DIC images to examine surface roughness etched surface will be smooth when etch is complete	
LEXT, Confocal microscope	Use Dektak or LEXT to confirm InP etch(~500nm)	
PE-II	help with hydrophilic surface properties	
Acid Bench	Etch InGaAs: H2SO4:H2O2:DI=1:1:10	1' 30" + 30"
	Add H2SO4(10ml) to DI(100ml), and then 10ml of fresh H2O2. Stir with the basket a little bit to make sure all is mixed then etch	
	DI Soak/N2 Dry	
LEXT, Confocal microscope	Use Dektak or LEXT to confirm InGaAs+InP etch(~600nm total)	
Microscope	inspect the ridge tops for smooth surface	Save 2-3 images
Strip Photoresist		
Solvent Bench	Soak in NMP	30'+
	IPA/DI/N2 Dry	2'
Gasonics	Recipe 2 (200C)	180"
PE-II asher	O2 ashing 0.300T/100W, (alternative to Gasonics)	180"
Microscope	Inspect for PR "ribbons"	Save 2-3 images
Dektak	After stripping resist, check the step height in places with/without the isolation etch. Examine the dielectric "ears" formed around the etched ridge tops.	
Dielectric Deposition: 2000Å		
Solvent Bench	ACE/IPA/N2 Dry	2'
PE 2	O2 Plasma 300mT/100W	30"
HF Bench	BHF Clean (thin the dielectric and remove dielectric "ears" formed by the InP+InGaAs etching)	2'
	DI Soak/N2 Dry	
Microscope	Inspect sample	
Dektak	check the step height with some dielectric removed from BHF	
Filmetrics	Measure SiN on the surface, and top of the WG MMI	
PECVD	_CLNSIN30/_SiN20, t=17'14.5" add SiN for passivation of exposed ridge tops from SSA ISO	200 nm
Filmmetrics	Measure SiN on the surface, and top of the MMI after deposition	

Figure B.6: Continued process flow steps for p-InGaAs isolation etch.

Equipment	Description	Key Parameters
P-via		
P-via Lithography, Autostep 200, LOG IN [10,71]		
Solvent Bench	ACE/IPA/N2 Dry	2' each
Spinner	Prebake 135C/5min, cool for 1 min	5' , 1'
	PE-II O2 plasma (use left asher), 20sec	20"
	Use BLUE tape for spinning, important for uniformity of resist across a quarter and keeping back side clean	
	Use small chuck for spinning, important for uniformity	
	HMDS, apply and let it soak for 20sec	3krpm/30"
	bake HMDS@100C/1min, cool down for 1 min	1' , 1'
	Use BLUE tape for next layer	
	SPR220-7 -- step 1: 3500rpm/150rpm/45s; step2: 0/1000/0	45" for 3.5krpm
	Bake 95C	3'
Stepper 2	SSA p-contact mask , Chuck 1/4 2"/500um/ Shim180um	
	Exposure: RECALL\pass [EXP=0.45", FOC=0] (pass=1 is for BR orientation, pass=2 is for BL orientation)	0.45"\0
	let sample sit for 20min to avoid bubble formation	20'
Developer Bench	AZ300 MIF Develop	70"
	DI Rinse, N2 blow dry	60"
Microscope	Inspect features	save some images
Etch Back Photoresist to expose ridge top		
RIE 3	Clean O2 20sccm/50mT/500V	30'
	O2 Etch 20sccm/10mT/200V	20' + 3' steps
	Clean O2 20sccm/50mT/500V - reclean chamber after ~20'	30'
	O2 Etch 20sccm/10mT/200V	2' steps near end
	O2 Clean , clean the tool, sample taken out	10'
Microscope	inspect when rainbows appear from thin photoresist and when they are gone from complete removal of photoresist	
	*noticed that Broad area lasers and TLM cannot be exposed due to much thicker photoresist covering them compared to ridge tops	
SEM	Check in SEM to see the ridge above the photoresist	
Dry Etch SiNx		
ICP-2	**Coat - Recipe 104** (CHF3/CF4/O2)=35/5/10, 500W/50W, Presure=0.5Pa	5'
	Etch - Recipe 104 (CHF3/CF4/O2)=35/5/10, 500W/50W, Presure=0.5Pa, time = 5'30"	400 nm SiN etch
	SiN etch 160 to 180 nm/min for rough approximation of etch rate. Exact values will vary based on tool, total area exposed, and aspect ratio of openings	3' (some over etch)
Microscope	microscope inspect to see if color is gone on ridge tops	
ICP-2	Run Recipe 104 again if more time needed for etch	15" more if needed
	O2 Clean Chamber for 10'	10'
	Rinse sample soon after done to stop etching reactions	
SEM	Check in SEM to see clean ridge tops (optional)	
LEXT	inspect the profile of the etched SiN in narrow SSA openings	
Wet Etch InP		
LEXT, Confocal microscope	Inspect the SSA openings before wet etch steps	
PE-II	PE-II, 5-10"	
Acid Bench	NH4OH:DI=1:10	20"
	DI Soak/N2 Dry	
PE-II	help with hydrophilic surface properties	
Acid Bench	Etch InP H3PO4: HCl=3:1 ~200ml (120ml:40ml)	30"+30"
	In this InP etch we should etch ~500nm of InP, which will take~1min. We cannot see bubbles, because etching areas are small.	
	DI Soak/N2 Dry	1'
microscope	Use bright field and DIC images to examine surface roughness etched surface will be smooth when etch is complete	
LEXT, Confocal microscope	Use Dektak or LEXT to confirm InP etch(~500nm)	

Figure B.7: Process flow steps for SSA via to p-contact layer.

Equipment	Description	Key Parameters
P-contact Metal		
Pre-clean		
UV Ozone	Heat up	10'
	load sample and Ozone clean	10'
HF Bench	BHF Dip	15"
	DI/N2 Dry	1'
P-metal Deposition		
E-Beam 1	Load Sample: Ti/Pt/Au	10/20/100nm
	Pump Down, Deposit 100 nm Ti with shutter closed to pump down quicker	1.00E-06
	Deposit:Ti/Pt/Au	10/20/100 nm
Lift-Off		
Solvent Bench	Soak in AZ NMP 80C	24 hrs
	spray with ACE/IPA and gently swab surface to remove residual metal. Thin photoresist next to ridges and no undercut profile from SSA leads to imperfect liftoff	
Microscope	Inspect features	Save 2-3 images
Anneal		
RTA	415C, forming gas	30"

Figure B.8: Process flow steps for p-contact metallization.

Equipment	Description	Key Parameters
Proton Implantation		
Proton Implant Lithography, Autostep 200, LOG IN [10,71]		
Solvent Bench	ACE/IPA/N2 Dry	2'
Spinner Bench	Prebake 135C/5min	5min
PE-II	PE-II 20sec	20"
Spinner Bench	Use blue tape during spinning resist	
	HMDS @recipe "7"	4000rpm/30s
	SPR 220-7@recipe"6"	3500rpm/45"
	bake@115/2min	2'
Stepper 2	SSA ISO mask , Chuck 1/4 2"/500um/ Shim180um	
	Exposure: RECALL\pass [EXP=1.35", FOC=0] (pass=1 is for BR orientation, pass=2 is for BL orientation)	1.35"\0
	let sample sit for 20min to avoid bubble formation	20'
Spinner Bench	PEB: Start 50C/1min, ramp up to 115C slowly, bake@115C/90sec	
Developer Bench	AZ300MIF	120"
	DI Rinse, N2 blow dry	
Microscope	Inspect features	Save 2-3 images
PE 2	O2 Plasma 300mT/100W	30"
Sample Mounting and Shipment		
Bench	Mount samples on Si Wafer (1/4 of 4" Si wafer). Use kapton tape (single side), and use it to attach InP quarter on Si piece. Put the tape at the coners (all three).	
UCSB Gateway	Notify them of expected shipment date, request **1 day turnaround & FedEx overnight**. Can provide **UCSB FedEx acct. #** Also **Print out** implant params, UCSB contact info, shipping address and ensure overnight delivery/other instructions, and include in shipment box	
SRIM/TRIM Software	Simulated to cover most of the p-type InP ridge with H+ ions, at 7° incident angle 35keV 4.5x10^13(cm-2) 85keV 6x10^13(cm-2) 145keV 8x10^13(cm-2) 215keV 10x10^13(cm-2)	
Strip Photoresist		
Solvent Bench	Strip resist using AZ NMP at 80C	overnight
	IPA rinse	
	Strip resist using AZ NMP at 80C	2hrs
	IPA/DI rinse	
Microscope	Nomaski/DIC inspect, look for PR residues at edges etc.	
Gasonics	Use recipe "2" (200C to 250C, O2 clean) repeat until clean (10 to 15' total was needed)	2 to 3' steps
PE-II	final clean for photoresist	30"

Figure B.9: Process flow steps for proton implant preparation.

Equipment	Description	Key Parameters
BCB Definition		
Microscope	Inspect samples, make sure samples are clean after proton implant	
Filmetrics	Measure SiN thickness (field~400nm and WG~200nm)	400 nm
Preparation	Spinner#3, bay 6, edit recipe: "5"	
	Spinner #3, bay6, edit recipe : "0" (step1: 500 rpm/400 rpm/10sec; step2: 3000 rpm/1000 rpm/30sec)	
	Set one of the hotplates@80C	
	Solvent bench, spinner#1 or# 2, edit program "7", run recipe using test sample to make sure vacuum is working (we had the issue with sample flying off the chuck)	
BCB-1 Lithography, Autostep 200, LOG IN [10,71]		
Solvent Bench	ACE/IPA/N2 Dry	2'
Spinner Bench	Prebake 135C/5min	5'
PE-II	PE-II O2 plasma (use left asher), 30sec	30"
Acid Bench	Dip HCl:Di=1:10 for 20sec (HCl conc. =36-38%, so when diluted it is 3-4 HCl %) -- turn off bench lights to avoid photochemical etching from Au	20"
Microscope	Di rinse , followed my microscope inspection	
Spinner Bench	Immediately go to next step to preserve surface cleaning	
	Use BLUE tape for spinning	
	Use small chuck (be consistent , always use same chuck, same spinner, bay 6- spinner#3(left one))	
	Appply AP3000 on your sample, let it soak for 30sec	30"
	Spin AP3000 @ recipe "5"	3krpm/30"
	NO BAKING	
	OPEN the small bottle with BCB	
	Spin BCB using recipe "0" with program in preparation step	500rpm/10" to 3krpm/30"
	Bake 80C/90sec	90sec
Stepper 2	BCB-1 mask , Chuck 1/4 2"/500um/ Shim180um	
	Exposure: RECALL\pass [EXP=2.2", FOC=0] (pass=1 is for BR orientation, pass=2 is for BL orientation)	2.2"/0
Spinner Bench	PEB 55C /30sec	30"
Solvent Bench	Immediately do the following puddle development	
	POLOS development(solvent bench) - use flat chuck	
	Edit program "7" to be (step1: 500 rpm/400 rpm/s /10sec; step2:4000 rpm/400 rpm/s /60sec)	
	Apply DS2100 on your sample	
	Let it sit on sample for 60sec	60"
	Run program "7", make sur vacuum is ON	
	While the recipe is running (step1, first 10sec) gently apply DS2100 drop by drop in the center of your samples	
	Spin dry @4000rpm/60sec (step#2) in program "7"	4krpm/60"
	Repeat developing step (cycle) until development is complete (usually 3 times)	
Microscope	Inspect sample, make sure all BCB is developed	
Solvent Bench	bake@90C/60sec to further dry out DS2100	90C/60"

Figure B.10: First part of process flow steps for BCB area definition.

Curing BCB		
Dektak	Dektak BCB (our test sample from 6/20/18 was ~4-4.2um)	
BLUE M Oven	Curing BCB Program #5	
	Purge oven with N2(for 1/2hr)before loading sample for curing	
	Edit the program	
	ramp up to 50C-5min(time in program is 0.05 for 5min)	5min ramp
	soak@50C-5min	50C/5min
	ramp up to 100C-15min(time in program is 0.15 for 15min)	15min ramp
	soak@100C-15min	100C/15min
	ramp up to 150C-15min	15min ramp
	soak@150C-15min	150C/15min
	ramp up to 250C-1hour(time in program is 1.00 for 1hour)	1 hour ramp
	soak@250C-1hour	250C/1hr
	Load sample in Al boat, DO NOT cover it, upper tray	
	Close the door, leave a note that BCB is curring	
	Make sure N2 in ON(60-70)	
	Run the program(P5, run)	
	Wait few minutes to check if it is running and if T is going UP!	
	CURRING takes 4hours	
	COOLING DOWN takes 8hours(overnight)	
	DO NOT OPEN door while cooling down! OK to open at <100C.	
Dektak	Dektak BCB after curing (will shrink ~0.4-0.5um)	
SEM	inspect the BCB surface, sidewall, and interface with SiN	

Figure B.11: Continued process flow steps for BCB area definition

Equipment	Description	Key Parameters
BCB-2		
Dielectric Deposition: 1000Å		
PECVD#1	_CLNSIN30/ precoat for 1'40" (200Ang SiN)/_SiN10 (dep for 8'20") Nitride needs to be at least 100nm for metal pads later	100nm, 8' 20"
Filmmetrics	Measure SiN [in the field(~470nm, on top of the WG~300nm]	470, 300 nm
BCB-2 Lithography, Autostep 200, LOG IN [10,71]		
Solvent Bench	ACE/IPA/N2 Dry	2'
Spinner Bench	Prebake 135C/5min	5min
PE-II	PE-II 20sec	20"
Spinner Bench	Use blue tape during spinning resist	
	HMDS @recipe "7" after 30" soak	4000rpm/30s
	SPR 220-7@recipe"6"	3500rpm/45"
	bake@115/2min	2'
Stepper 2	SSA ISO mask , Chuck 1/4 2"/500um/ Shim180um	
	Exposure: RECALL\pass [EXP=1.35", FOC=0] (pass=1 is for BR orientation, pass=2 is for BL orientation)	1.35"\0
	let sample sit for 20min to avoid bubble formation	20'
Spinner Bench	PEB: Start 50C/1min, ramp up to 115C slowly, bake@115C/90sec	
Developer Bench	AZ300MIF	120"
	DI Rinse, N2 blow dry	
Microscope	Inspect features, note all microscope parameters used so that they can be replicated for a color comparison during the etching	save several images
PE 2	O2 Plasma 300mT/100W	30"
SiN 100nm and BCB 2um Deep Window Etching		
RIE 3	O2, 20 sccm, 50mT, 500V, 30min chamber clean	30'
Filmmetrics	Check SiN thickness on a test structure for etch rate monitoring	
RIE 3	Load real sample and test sample	
	CF4/O2, 20sccm/1.8sccm, 10mT, 250V, 7min (overetch) expecting close 17 nm/min etch from test sample	7'
Filmetrics	Check on a test structure if SiN is all etched	100 nm
RIE 3	CF4/O2, 4sccm/16sccm, 20mT, 350V expecting ~100 nm/min etch rate for BCB SiN etches at ~13 nm/min with this recipe	350V 21 to 24 min
	Load sample in RIE#3, O2, 20sccm,10mT, 200V, 5min O2 descum to clean chamber and sample of polymer buildup	5 min
Strip Photoresist		
DUV	use DUV or contact aligner flood expose for ~3-5 minutes	3-5 minutes
Developer Bench	develop for ~5 min in AZ300MIF	5 min
Solvent Bench	ACE/IPA clean, N2 dry	~2 min
Gasonics	PE-II is bad because it can create thin oxide on nitride and can sputter the gold. Gasonics at 200C is safer	4 to 6 min
SEM	inspect tilted view of etched trench	

Figure B.12: Process flow steps for etched windows through BCB.

Equipment	Description	Key Parameters
BCB3 - Direct Vias		
Dielectric Deposition: 1000Å		
Solvent Bench	ACE/IPA/N2 Dry	2'
	110/2min	2'
Gasonics	PE-II is bad because it can sputter the gold Gasonics at 200C is safer	30"
PECVD#1	_CLNSIN30/ precoat for 1'40" (200Ang SiN)/_SiN10 (dep for 8'20") protective SiN to cover etched BCB	100nm, 8' 20"
Ellipsometer	check thickness on a test piece	100 nm
BCB-3 Lithography, Autostep 200, LOG IN [10,71]		
Solvent Bench	ACE/IPA/N2 Dry	2'
Spinner	Prebake 135C 5min	5'
PE-II	O2,300mT, 100W, 20"	20"
Spinner Bench	HMDS Resist adhesion promoter, wait 20" before spinning, use recipe 7. use blue tape	4krpm/30"
	bake sample at 100C for 1 min for good wetting of HMDS	100C, 1'
	put sample on metal bench to cool for 1'	1'
	Use new blue tape. Check for bubbles in pipet before applying SPR220-3. Apply, then Wait 5 minute for resist to settle in trenches	5'
	Spin SPR-220-3 resist 2500rpm/30"	resist 2500rpm/30"
Microscope	use filters to prevent exposing, look for air bubbles in resist	
	Make sure to wait at least 5 min before baking	
Spinner Bench	Bake 50C for 1 min, ramp to 70C slowly (wait until T ~70C), then ramp up to 90C (wait until T~90C), then ramp up to 100C (wait until T is ~110C), ramp up to 115C, and bake @115C for 90sec	~5 min total time
	put sample on metal bench to cool for 1'	1'
Microscope	use filters to prevent exposing, look for air bubbles in resist	
Stepper 2	BCB-3 mask , Chuck 1/4 2"/500um/ Shim180um	
	Use Local alignment program with distance from center Bottom left and right x=3182.175, y=3432.176 Top left and right x=3182.175, y=3417.825	
	MAP RECALL\LOCAL, pass [Exp: 0.75", Foc: 10] (pass=1 is for BR orientation, pass=2 is for BL orientation)	0.75"/10
	Align as usual, using global alignment mark then stepper will use local al. mark) and cheack/correct alignment. This way aligning BCB-3 latyer to WG layer should be <200nm.	
	wait for 45min before developing or more	>45min
Microscope	use filters to prevent exposing, look for air bubbles in resist	
Developer Bench	AZ300 MIF 60"	60"
Microscope	Inspect features, +10" MIF300 if necessary	Save 2-3 images
PE-II	O2 Plasma 300mT/100W, 30sec and more if needed!	30"
RIE3 Dry Etch SiN		
PE-II	O2 Plasma 300mT/100W	30"
RIE 3	Preclean chamber O2, 20 sccm, 50mT, 500V, 30min	O_2, 20 sccm, 50mT, 500V, 30min
	SiN etch CF4/O2, 20sccm/1.8sccm, 10mT, 250V, t = 9 to 11 min need to overetch in open areas; etch rate in small vias is lower	etch in 4 min, then 1 min steps
Filmetrics	check nitride thickness after each etch step in test rectangle	
Microscope	also look at color change of nitride in BCB vias and test structures -etch rate in large areas is faster than etch rate in small vias	
RIE 3	Load sample in RIE#3, O2, 20sccm,10mT, 200V, 5min	5'
Strip Photoresist		
DUV	use DUV or contact aligner flood expose for ~3-5 minutes	~3-5 minutes
Developer Bench	5' in AZ300MIF -- repeat DUV + develop until >90% clean	5 min
Solvent Bench	long ACE soak or short NMP soaks if ACE is not working	~1 hour
	ACE/IPA clean, N2 dry	2'
Gasonics	300 mT, 100W 30"	30"

Figure B.13: Process flow steps for direct vias to photodiodes.

Equipment	Description	Key Parameters
Pad Metal Lithography		
Pad Metal Lithography, Autostep 200, LOG IN [10,71]		
Solvent Bench	ACE/IPA/N2 Dry	2'
Hot plate	Prebake 115C to dehydrate, cool on bench for 1'	2' +1'
Spinner Bench	HMDS Resist adhesion promoter, wait 20" before spinning, use recipe 7. use blue tape	4krpm/30"
	bake sample at 100C for 1 min for good wetting of HMDS	100C, 1'
	put sample on metal bench to cool for 1'	1'
	Put sample on blue tape; Use cut pipets to apply PMGI SF-15, wait 2' for resist to settle in small openings	2'
	PMGI SF15 spin resist	400rpm/30" , 4krpm/30"
	-carefully remove whiskers using tweezers or razor blade -can also use EBR on a swab (risky-need to be careful that only the very edge is removed)	1'
Microscope	Use filters and inspect the sample for bubbles while waiting 5' before baking	5'
Spinner Bench	Bake 110C for 60"	110C/60"
	Transfer to IKA RET Hot plate for Bake at 175C for 2min	175C/2'
	Remove sample from hotplate and cool for 2' crushing the PMGI after baking can cause cracks	2'
Microscope	Inspect sample for bubbles	
Spinner Bench	Put sample on blue tape; Use cut pipets to apply PMGI SF-15, wait 2' for resist to settle in small openings	2'
	PMGI SF15 spin resist	400rpm/30" , 4krpm/30"
	-carefully remove whiskers using tweezers or razor blade -can also use EBR on a swab (risky-need to be careful that only the very edge is removed)	1'
Microscope	Use filters and inspect the sample for bubbles while waiting 5' before baking	5'
Spinner Bench	Bake 110C for 60"	110C/60"
	Transfer to IKA RET Hot plate for Bake at 175C for 2min	175C/2'
	Remove sample from hotplate and cool for 2' crushing the PMGI after baking can cause cracks	2'
Microscope	Inspect sample for bubbles	
PE-II	O2 Plasma 300mT/100W to help prevent solvent intermixing which causes cracks in the PMGI	60"
Spinner Bench	Put sample on blue tape; Use pipets to apply SPR 220-3.0, wait 2' for resist to settle in small openings	
	SPR 220-3.0 2.5krpm/30"	2.5krpm/30"
Microscope	Use filters and inspect the sample for bubbles while waiting 5' before baking	5'
Spinner Bench	Bake 50C for 1 min, ramp to 70C slowly (wait until T ~70C), then ramp up to 90C (wait until T~90C), then ramp up to 100C (wait until T is ~110C), ramp up to 115C, and bake @115C for 90sec	~4 - 5 min
	Cool Sample for 2'	2'
Microscope	Inspect to check for bubbles before exposing	5'

Figure B.14: First part of process flow steps for pad metal.

Stepper 2	Pad_Metal Mask with Chuck 500um/180nm shim	
	Exposure: RECALL/pass [Expose 0.85 sec FO 5] (pass=1 is for BR orientation, pass=2 is for BL orientation)	exp:0.85" , Foc:5
	Wait 10min before developing	10'
Developer Bench	AZMIF300 develop for 40~50 sec	45"
Microscope	Inspect pad metal pattern, take pictures	
DUV	flood exposure for PMGI SF15 undercut	4'
Developer Bench	develop for PMGI SF15 undercut	60"
	DI Rinse, N2 blow dry	
Microscope	Inspect in microscope and Dektak	
DUV	flood exposure for PMGI SF15 undercut	3'
Developer Bench	develop for PMGI SF15 undercut	60"
	DI Rinse, N2 blow dry	
Microscope	Inspect in microscope and Dektak	
DUV	flood exposure for PMGI SF15 undercut	2'
Developer Bench	develop for PMGI SF15 undercut	60"
	DI Rinse, N2 blow dry	
Microscope	Inspect in microscope and Dektak	
DUV	flood exposure for PMGI SF15 undercut	1'
	develop for PMGI SF15 undercut	30"
Developer Bench	DI Rinse, N2 blow dry	
Microscope	Inspect features, +30" SAL101 if necessary	Save 2-3 images
Developer Bench	develop for PMGI SF15 undercut	30"
	Repeat until satisfied that all PMGI is developed	
PE 2	O2 Plasma 300mT/100W	30 - 60"
UV Ozone	Heat up	10'
	Ozone clean	10'
HF Bench	BHF:DI :: 1:5 Dip for 10"	5"
	DI/N2 Dry	1'
Pad metal Deposition		
E -beam 1	Load Sample on rotating chuck using screw tightened clips 50 to 60 deg angle with sample 23 to 25 cm from hearth	
	Pump Down, Deposit Ti with shutter closed to pump down quicker	1.00E-06
	Deposit:Ti/Au or Cr/Au (Ti/Au had poor adhesion on 1st sample) real deposition is ~2 to 2.5X the XTAL monitor reading	XTAL - 10/750 nm Real - 20/1500 nm
Lift-Off		
Solvent Bench	Soak in ACE	~24 hr
Developer Bench	Short soak in MIF300	~10min
Microscope	Inspect features	Save 2-3 images

Figure B.15: Continued process flow steps for pad metal.

Equipment	Description	Key Parameters
Wafer Thinning and Backside Metallization		
Manual Lapping Station		
Diamond Scribe	Cleave a ~1.2" by 1.2" Silicon piece to use as carrier for the InP quarter; the piece should be slightly larger than the InP piece	1.2" x 1.2" Si piece
Klamkin Lab Lapping Station	Attach Si to chuck with crystalbond @ 120 - 150C	120 - 150C
	Attach sample to Silicon with crystalbond @ 120 - 150C Topside down to thin the backside of wafer	120 - 150C
	Cover w/ vaccum with cleanroom wipe or filter paper Suction the InP+Si stack to make it more level	
	Let cool to room temperature and clean off excess crystalbond w/ acetone. Don't want any wax on top of the sample	
	Use water surface tension to adhere 12um grit Aluminum Oxide lapping paper to the reference flat surface	
	Use thickness gauge to measure thickness of InP+crystal bond from the top of Si carrier as a reference height. Check in each corner to confirm sample is level.	
	Redo Vacuum press procedure if sample is not level. If stil not level, carefully remove sample (see steps below) and redo mounting. Want sample to be level within +/-10um	
	screw chuck into manual lapping weighted hand tool	
	apply DI for lubrication and remove 200 to 225 um by lapping with figure 8 pattern (sample is ~350 um to start)	200 - 225nm lapped 150 - 125 left
	periodically check the thickness after rinsing back with DI/ISO and gently using a wipe on the backside	
	when done, remove the silicon carrier from lapping chuck by heating @ 120 - 150C and gently sliding off, then cool down	120 - 150C
Backside Metallization		
Solvent Bench	Quick clean with ACE/IPA on InP backside	
E-beam 3	Put the clips on the Si carrier to mount on chuck	
	Ti/Pt/Au 20/40/500 nm (distance about same as XTAL monitor)	20/40/500 nm
Hotplate	Hotplate bake @ 120 up to 150C until sample slides when gently pushing on the curved edge. Place stack of wipes near hotplate for sample to gently land on when falling off Si carrier	120 - 150C
Solvent Bench	ACE/ISO clean gently until all crystalbond is gone; can gently place sample on cleanroom wipe and spray with ACE/IPA then let soak. repeat ACE/IPA gently soaking until sample is clean	
Microscope	Inpsect sample surface to check that crystal bond is gone	

Figure B.16: Process flow steps for wafer thinning and backside metallization.

BCB Definition

Hard Mask Deposition

Tool	*Description*	*Comments*
Solvent Bench	ACE/IPA clean	Dry thouroughly
***ideally measure 1 test sample for each step & 1 more sample with all steps (3 test pieces for this film stack)		
PE II	10s O2	300mT 100W
Wet Bench	NH4OH 30s (turn off lights in fume hood to be safer)	clean surface for dep - removes InP surface oxides
PECVD-1	run clean if last user did not	can always run another clean to be safe
PECVD-1	Run SiN coat process	
PECVD-1	Deposit 100 SiN (~500 sec)	*use a blank piece to check thickness
PECVD-1	vent, unload sample with metal tweezers	
PECVD-1	wet clean chamber walls and O-ring with DI then IPA, pump down	
PECVD-1	SiN Clean 1 min for every 7 min dep	run for 3 min to be safe
Ellipsometer	check SiN thickness with blank test piece **#1**	
PECVD-1	Run SiO2 coat process	
PECVD-1	Deposit 200 nm SiO2 (~283 sec)	
PECVD-1	vent, unload sample with metal tweezers	
PECVD-1	wet clean chamber walls and O-ring with DI then IPA, pump down	
PECVD-1	SiO2 Clean 1 min for every 1 min dep	run for 6 min to be safe
Ellipsometer	check SiN+SiO2 thickness with blank test piece **#1** check SiN thickness with black test piece **#2**	
PECVD-1	Run SiN coat process	
PECVD-1	Deposit 100 nm SiN (~500 sec)	
PECVD-1	vent, unload sample with metal tweezers	
PECVD-1	wet clean chamber walls and O-ring with DI then IPA, pump down	
PECVD-1	SiN Clean 1 min for every 7 min dep	run for 3 min to be safe
Ellipsometer	check SiN+SiO2+SiN thickness with blank test piece **#1** check SiN thickness with black test piece **#3**	
Filmetrics	check SiN+SIO2+SiN thickness with blank test piece and real sample measure the samples in a few locations to check uniformity	
uScope	Check for pinholes and roughness **take images of hard mask color at PDs for color comparison during BCB via etch**	

BCB 4024 spin and pattern

bottles in freezer in chase	Take out small BCB bottle from freezer and warm up overnight	use the bottle within ~7 days
solvent bench sonicator	Use small pipet to measure ~2.5 mL of BCB 4024 Use small pipet to measure ~0.5 mL of mesitylene Inject mesitylene first then BCB into large pipet for mixing put pipet in beaker with liquid, put in sonicator and mix for 30 min	
PE-II	Place sample in PEII at 100W, 300mT for 30s	
acid bench	Dip HCl:DI 1:10 for 60s, Rinse in DI 60s, Blow Dry	
resist spinner	Apply AP3000 BCB Adhesion promoter, wait 30sec, and then spin 3krpm for 30sec	
resist spinner	Spin BCB -- step1: 500rpm-400rpm/s-10sec step2: 3.5krpm-1000rpm/s-30sec	
custom hotplate	bake @ 60C/90sec because BCB is thinner	sheet <4.5um 60 C , 4.6 to 6.6um 65C 6.7 to 8.7 um 70C, 8.8 to 10.0 um 75C
Autostep200	1/4 of 2" chuck with 180 um (no sticker) shim use manual alignment for better focus uniformity across wafer G2TLMAN -pass- MEAS then MANUAL -- for TL samples G2BLMAN -pass- MEAS then MANUAL -- for BL samples diluted BCB --- **expose 1.3 sec , FO (-)27** **mask error --- change pass shift to x = (-)4.2961, y = 4.3084**	6um FO -1 per 0.1 um reduced thickness below 6um ~0.37 sec exp. per um of post soft bake BCB thickness 2um,0.75",FO=-40 // 3um,1.1",FO=-30 //
custom hotplate	PEB @55C/30sec	
POLOS spinner	put blue tape on polished Si wafer (sticky side up) put sample on blue tape and press to ensure it is stuck in place put Si wafer in POLOS chuck puddle develop + rinse + dry (1'30" puddle develop) after puddle develop - spin **@ 500 rpm for 10" while dripping developer** then 4kprm 60" while blownig with N2 to dry sample	**wafer! If puddle leaks off the wafer, the wafer will not stick to the blue tape and it will fly away when spinning!** POLOS spinner should have program for BCB developing, if not -- can create new POLOS program
bench hotplate	**immeadiately** Bake@90C/60sec to further dry out DS2100	BCB sidewall could be bad if waiting to bake for more than 1 minute
Dektak or KLA-tencor	Measure with dektak before curing	
microscope	inspect BCB pattern for uniform size and color across sample	

Figure B.17: First part of process flow steps for BCB areas.

BCB Cure		
Blue-M Oven	Load sample in oven (put in Al boat/container to prevent sample from sliding around the oven) and purge oven with N2 at 60 to 70 for 30 min to remove O2 from oven before baking	
Blue-M Oven	Final Cure in BLUE M Oven (Program 5): Program#5 -- Edit the program to match the steps shown below ramp up to 50C-5min(time in program is 0.05 for 5min) soak@50C-5min ramp up to 100C-15min(time in program is 0.15 for 15min) soak@100C-15min ramp up to 150C-15min soak@150C-15min ramp up to 250C-1hour(time in program is 1.00 for 1hour) soak@250C-1hour	
Blue-M Oven	DO NOT cover sample. Close the door, Make sure N2 in ON (60-70) Run the program (P5, run) Wait few minutes to check if it is running and if T is going UP! CURING takes ~3hours	
Blue-M Oven	COOL DOWN to <150C (takes ~2 hours to cool below 150) DO NOT OPEN door while it is cooling down! OK to open at 150C.	

Examine the BCB profile		
Dektak or KLA-tencor	Measure with dektak after curing	****need to determine BCB thickness for p-via etch**
Confocal Laser Scope	Examine BCB profile (height, ridge coverage, shape)	
SEM 1 or 2	check BCB profile in SEM examine sidewall angle, adhesion, roughness, etc	

Protective SiN/SiO2 Deposition		
PE II	10s O2	300mT 100W - clean organics
Wet Bench	NH4OH 30s then DI rinse for 1 min	clean surface oxides
PECVD-1	run clean if last user did not	can always run another clean to be safe
PECVD-1	Run SiN coat process	
PECVD-1	Deposit **50nm SiN (~250 sec)**	*use a blank piece to check thickness
PECVD-1	vent, unload sample with metal tweezers	
PECVD-1	wet clean chamber walls and O-ring with DI then IPA, pump down	
PECVD-1	SiN Clean 1 min for every 7 min dep	run for 3 min to be safe
Ellipsometer	check SiN thickness with blank test piece	
PECVD-1	Run SiO2 coat process	
PECVD-1	vent, load sample with metal tweezers, pump down	
PECVD-1	Deposit **75 nm SiO2 (~105 sec dep time)**	check dep rate data on wiki
PECVD-1	vent, unload sample with metal tweezers	
PECVD-1	wet clean chamber walls and O-ring with DI then IPA, pump down	
PECVD-1	CF4/O2 clean 1 min clean for every 1 min dep	run for 3+ min to be safe
Ellipsometer	check SiN+SIO2 thickness with blank test piece	
Filmetrics	check SiN+SiO2+SiN+SiO2 thickness with blank test piece and real sample. measure the samples in a few locations to check uniformity	100/200/150/80 nm SiN/SiO2/SiN/SiO2 in total
Confocal Laser Scope	Examine BCB profile (height, ridge coverage, shape)	**need to determine BCB thickness
KLA/dektak	Examine BCB and ridge profile to check against confocal	
uScope	check for roughness or pinholes in dielectric	

Figure B.18: Continued process flow steps for BCB areas.

Pad Metal

Lithography

Tool	*Description*	*Comments*
Wet Bench	Acetone, IPA rinse	1' each
Hot Plate	200C 10 min	
spinner	HMDS at 4krpm	sample on blue tape
Hot Plate	110C 1 min	
Spinner	LOR 30C 1.3 krpm (250 rpm/s) 45s	Make 2 in. wafer with blank pieces on blue tape. Use small pipette with cut tip to slowly apply LOR 30C, holding the pipette close to the sample for a continuous flow and moving in a zig-zag pattern.
Hot Plate	110C 1 min, +15C steps until 170C, hold for 5 min	Immediately remove from blue tap by gently rolling the tape from the curved edge to the center of the sample until it slides away from the blank pieces (some finesse is required). Wear double gloves and remove the outer pair with LOR residue.
bench	cool down slowly	place on cleanroom wipes or Al foil container to cool slowly and avoid cracking from thermal shock.
Spinner	SPR 220-3 at 2krpm for 40 seconds	Make 2 in. wafer with blank pieces on blue tape. Use small pipette to dispense SPR 220-3 carefully to avoid introducing bubbles in the resist
Hot Plate	50C for 1min, +15C steps until 115C, hold for 2min	Gently roll blue tape using same technique as with LOR.
bench	cool down slowly	place on cleanroom wipes or Al foil container to cool slowly and avoid cracking from thermal shock.
MLA	main metal - 250 dose, -10 defoc deep metal - 375 dose, -10 defoc PD metal - 200 dose, -15 defoc	use 405nm laser **wait for 1 hour before development**
Solvent Bench	MIF 300 for 75s	should see patterns and small undercut
DUV	5 minutes with reflector cone	
developer bench	60 second development with SAL101A	undercut ~1.5 um
DUV	5 minutes with reflector cone	
developer bench	60 second development with SAL101A	PD undercut ~2 to 3 um, laser undercut ~3 um
DUV	5 minutes with reflector cone	
developer bench	60 second development with SAL101A	PD undercut 2.5 to 4 um, laser undercut ~ 3.5 to 4.5 um
DUV	3 minutes with reflector cone	
developer bench	30 second development with SAL101A	PD undercut 3.5 to 5 um, laser undercut ~ 4.5 to 5.5 um
PE-II	2 min	residue cleanup

e-beam deposition

e-beam 1	Load sample on small chuck	use screw climps on small chuck and connect to adjustable mounting arm with rotation motor. Measure position to be ~24 cm from the crucible with ~40 deg angle between sample surface normal and the crucible. Turn on rotation motor.
e-beam 1	pump down and check program	40 nm Ti at 0.1 nm/s , 800 nm Au at 0.2 nm/s
e-beam 1	Ti deposition (40 nm Ti at 0.1 nm/s)	to help ensure clean metal, run soak multiple times to burn off oxides and other contiminants with closed shutter
e-beam 1	wait for metal to cool	follow SOP for waiting time before changing metal
e-beam 1	Au deposition (800 nm Au at 0.2 nm/s)	use same cleaning procedure as above. Au should be molten.
e-beam 1	wait for metal to cool	follow SOP for waiting time before opening chamber

Pad metal Liftoff

solvent bench	overnight acetone soak	**BCB will expand in NMP - do not use for long soak**
solvent bench	clean with IPA/DI water	spray with pipette to encourage metal to lift off
developer bench	soak in MIF300 1 to 2 hours	*liftoff time extended by largest area without pads. Longer time needed to dissolve LOR in area between dies

Figure B.19: Process flow steps for pad metal lithography and deposition.

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