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Graphene as tunable contact for high performance thin film transistor

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Material Science and Engineering

by

Yuan Liu

2015

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ABSTRACT OF THE DISSERTATION

Graphene as tunable contact for high performance vertical thin film transistor

by

Yuan Liu

Doctor of Philosophy in Material Science and Engineering

University of California, Los Angeles, 2015

Professor Yu Huang, Chair

Graphene has been one of the most extensively studied materials due to its unique band structure, the linear dispersion at the K point. It gives rise to novel phenomena, such as the anomalous quantum Hall effect, and has opened up a new category of “Fermi-Dirac” physics. Graphene has also attracted enormous attention for future electronics because of its exceptional high carrier mobility, high carrier saturation velocity, and large critical current density. However, graphene has zero intrinsic band gap, thus can not be used as the active channel material for logic transistors with sufficient on/off current ratio. Previous approaches to address this challenge include the induction of a transport gap in graphene nanostructures or bilayer graphene. However, these approaches have proved successful in improving the on– off ratio of the resulting devices, but often at a severe sacrifice of the deliverable current density. Alternatively, with a finite

density of states, tunable work-function and optical transparency, graphene can function as a unique tunable contact material to create a new structure of electronic devices.

In this thesis, I will present my effort toward on-off ratio of graphene based vertical thin film transistor. I will include the work form four of my first author publication. I will first present my research studies on the a dramatic enhancement of the overall quantum efficiency and spectral selectivity of graphene photodetector, by coupling with plasmonic nanostructures. It is observed that metallic plasmonic nanostructures can be integrated with graphene photodetectors to greatly enhance the photocurrent and external quantum efficiency by up to 1,500%. Plasmonic nanostructures of variable resonance frequencies selectively amplify the photoresponse of graphene to light of different wavelengths, enabling highly specific detection of multicolours. Then I will show a new design of highly flexible vertical TFTs (VTFTs) with superior electrical performance and mechanical robustness. By using the graphene as a work-function tunable contact for amorphous indium gallium zinc oxide (IGZO) thin film, the vertical current flow across the graphene-IGZO junction can be effectively modulated by an external gate potential to enable VTFTs with a highest on-off ratio exceeding 10^5. The unique vertical transistor architecture can readily enable ultrashort channel devices with very high delivering current and exceptional mechanical flexibility. Furthermore, I will, demonstrate a new design strategy for vertical OTFT with ultra-short channel length without using conventional high-resolution lithography process. They can deliver a high current density over 1.8 A/ cm^2 and thus enable a high cutoff frequency devices (~ 0.4 MHz) comparable with the ultra-short channel organic transistors. Importantly, with unique vertical architecture, the entire organic channel material is sandwiched between the source and drain electrodes and is thus naturally protected to ensure excellent air-stability. Finally I will present a new strategy by using graphene as the back electrodes to achieve Ohmic contact to MoS_2.

With a finite density of states, the Fermi level of graphene can be readily tuned by a gate potential to enable a nearly perfect band alignment with MoS_2. For the first time, a transparent contact to MoS_2 is demonstrated with zero contact barrier and linear output behaviour at cryogenic temperatures (down to 1.9 K) for both monolayer and multilayer MoS_2. Benefiting from the barrier-free transparent contacts, we show that a metal-insulator-transition (MIT) can be observed in a two-terminal MoS_2 device, a phenomenon that could be easily masked by Schottky barriers found in conventional metal-contacted MoS_2 devices. With further passivation by boron nitride (BN) encapsulation, we demonstrate a record-high extrinsic (two-terminal) field effect mobility up to 1300 $cm^2/V\ s$ in MoS_2 at low temperature. These findings can open up exciting new opportunities for atomically thin 2D semiconductors as well as other conventional semiconductors in general.

The dissertation of Yuan Liu is approved.

Dwight C.Streit

Yang Yang

Xiangfeng Duan

Yu Huang, Committee Chair

University of California, Los Angeles

2015

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Biography

Yuan Liu received his B.S. degree in Electrical Engineering from Zhejiang University, Hangzhou, China in 2010. He joined Dr. Yu Huang's group in 2010 and conducted the research of graphene for novel electronic and photonics. He was awarded Chinese Scholarship Council (CSC) scholarship from 2010 to 2014 and UCLA Dissertation Year Fellowship (DYF) in 2015. He has 5 first-author and 17 co-author papers published in peer-review journals. He gave oral presentations in American Conference on Crystal Growth and Epitaxy (ACCGE) 2013 in Keystone, CO, Material Research Society (MRS) Meeting 2014 in Boston and MRS Meeting 2015 Spring in San Francisco, respectively. His research interests include electrical and optical properties of two-dimensional layered materials or other semiconducting nanomaterial.

INTRODUCTION

Graphene is two-dimensional carbon atoms assembled in hexagonal structure, like a honeycomb. This 2D structure comes from triangular planar arrangement of carbon-carbon σ bonds due to sp^2 hybridization, which is further enforced by half-filled π band[1]. This strong carbon-carbon bonding enables the lattice stability even up to 1500 °C upon annealing[2-3]. Although graphene may be easily produced with pencil writing, it is difficult to locate such atomic layer thin material by conventional imaging techniques such as atomic force microscopy (AFM), transmission electron microscopy (TEM) and scanning electron microscopy (SEM), due to the low through-put and uncertainty of sample preparation[4-5]. This came to an end in 2004 when Geim and co-workers successfully isolated atomic thin carbon layer by micro-mechanical cleavage method[4]. The discovery of graphene owed to its unique optical property: this atomic thin material can be visualized using optical microscope due to its notable opacity when prepared on Si substrate with certain thickness of SiO_2. Later on, it was discovered that graphene displayed distinctive Raman spectral characteristics, which was very powerful in distinguishing between single, double and multi-layer graphene[9-12]. The simple technique of optical microscopy in conjunction with Raman spectroscopy greatly facilitated the scientific research on graphene based novel materials.

Ever since it was first experimentally discovered, graphene is quickly rising to be one of the most attractive material systems for fundamental studies as well as potential applications due to its unique electronic properties, such as high saturation velocity, large tunable work function, as well as the ultra-high carrier mobility[13-17]. At low temperature (4 K), the mobility of graphene is measured to be 1,000,000 cm^2 /V s, making it one of promising candidate for future electronics. The band structure of single layer graphene is determined to have 2D character and a linear dispersion relation of electronic wave functions with perfect electron-hole symmetry, in which

Fermi surface consists of two cones touching at one singular, so-called Dirac point (Fig. 1-1a). The typical graphene transistor showed ambipolar field effect (Fig. 1-1b)- the conductance showed a valley as a function of gate voltage where the charge carrier changed the sign at the conductance minimum, beside which the conductance increased linearly with gate voltage on both sides of the valley.

Due to the touching of two Dirac cone, graphene have zero intrinsic bandgap, with an on/off ratio less than 10 at room temperature. Since the discovery of graphene, lots of effort have been put into area of bandgap opening inside graphene, and one of the most successful approach is using graphene nanoribbon. Graphene ribbons were first introduced as a theoretical model by Mitsutaka Fujita and coauthors to examine the edge and nanoscale size effect in graphene[18-20]. They found that by reducing the width of graphene into nanosize, the edges provide the edge localized state with non-bonding molecular near the Fermi energy, which is expected to have large changes in electronic properties, thus can open up a measureable bandgap inside graphene. Based on this motivation, various methods are developed to fabricate graphene nanoribbon transistor between 2008 and 2011[21-30]. The maximum bandgap is demonstrated to be ~0.5 eV[17], resulting in an improved on/off to be around 1000. However, the method of using graphene nanoribbon greatly sacrifice the deliverable current density and the corresponding mobility of graphene nanoribbon, making it unsuitable as an active channel material. Alternatively, without bandgap, graphene can also be viewed as a semi-metal. Compared with conventional metal with a fixed work function, the work function of graphene can be tuned up to 3 eV. With a finite density of states, tunable work-function and optical transparency, graphene can function as a unique tunable contact material to create a new generation of electronic devices[31-38].

In this thesis, I will present my study about graphene as a unique platform for photodetection in planar vertical thin film transistor, as well as unique contact material for vertical thin film transistor. I included four of my first author publications and assemble them in sequence[39-42]. I will first present my research studies on the a dramatic enhancement of the overall quantum efficiency and spectral selectivity of graphene photodetector, by coupling with plasmonic nanostructures. It is observed that metallic plasmonic nanostructures can be integrated with graphene photodetectors to greatly enhance the photocurrent and external quantum efficiency by up to 1,500%. Plasmonic nanostructures of variable resonance frequencies selectively amplify the photoresponse of graphene to light of different wavelengths, enabling highly specific detection of multicolours. Then I will show a new design of highly flexible vertical TFTs (VTFTs) with superior electrical performance and mechanical robustness. By using the graphene as a work-function tunable contact for amorphous indium gallium zinc oxide (IGZO) thin film, the vertical current flow across the graphene-IGZO junction can be effectively modulated by an external gate potential to enable VTFTs with a highest on-off ratio exceeding 10^5. The unique vertical transistor architecture can readily enable ultrashort channel devices with very high delivering current and exceptional mechanical flexibility. Furthermore, I will, demonstrate a new design strategy for vertical OTFT with ultra-short channel length without using conventional high-resolution lithography process. They can deliver a high current density over 1.8 A/ cm^2 and thus enable a high cutoff frequency devices (~ 0.4 MHz) comparable with the ultra-short channel organic transistors. Importantly, with unique vertical architecture, the entire organic channel material is sandwiched between the source and drain electrodes and is thus naturally protected to ensure excellent air-stability. Finally I will present a new strategy by using graphene as the back electrodes to achieve Ohmic contact to MoS_2. With a finite density of states, the Fermi level of graphene can be readily tuned by a gate potential

to enable a nearly perfect band alignment with MoS_2. For the first time, a transparent contact to MoS_2 is demonstrated with zero contact barrier and linear output behaviour at cryogenic temperatures (down to 1.9 K) for both monolayer and multilayer MoS_2. Benefiting from the barrier-free transparent contacts, we show that a metal-insulator-transition (MIT) can be observed in a two-terminal MoS_2 device, a phenomenon that could be easily masked by Schottky barriers found in conventional metal-contacted MoS_2 devices. With further passivation by boron nitride (BN) encapsulation, we demonstrate a record-high extrinsic (two-terminal) field effect mobility up to 1300 cm^2/V s in MoS_2 at low temperature. These findings can open up exciting new opportunities for atomically thin 2D semiconductors as well as other conventional semiconductors in general.

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Figures and Legends

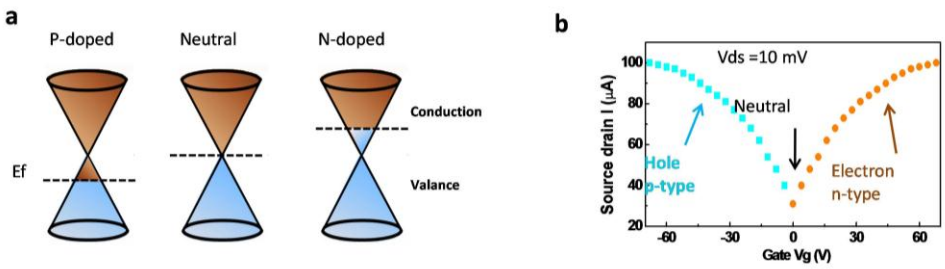

Figure 1-1. a, Band structure of graphene, where the top cone is conduction band and bottom cone is valance band. The blue color is electron filled and the yellow color is electron empty (hole filled). **b**, The typical transfer behavior of graphene transistor. Neutral point is corresponding to the minimal conducting point, where the Fermi level is on the Dirac point.

Chapter I: PLASMON RESONANCE ENHANCED MULTICOLOUR PHOTODETECTION BY GRAPHENE

A. Introduction to graphene based photodetection

Graphene is emerging as an attractive material candidate for future electronics[1-3] and optoelectronics[4,5] due to its unique combination of several important characteristics, including high carrier mobility[6], high optical transparency[7], exceptional mechanical flexibility and strength[8]. Ultra-high speed electronic and photonic devices with the operation frequency up to terahertz regime have been demonstrated or suggested[9-14]. Recent studies have demonstrated the exciting potential of exploiting graphene for diverse optoelectronic devices including solar cells, touch panels, photodetectors, ultrafast lasers, polarizer and optical modulators[15-21]. The wideband absorption[7], high carrier mobility[6] and short carrier lifetime make graphene an ideal material for wideband, high speed photodetectors. Ultra-fast metal-graphene-metal (MGM) photodetectors have been demonstrated, with operation frequency (40 GHz achieved and 500 GHz suggested) comparable to or exceeding traditional group III-V materials based photodetector.[9,22] Importantly, with a zero band gap, graphene photodetectors can be used for ultra-wide band (300nm to 6μm) operation, far exceeding the capability of the current photodetectors[23,24]. Additionally, with the fast development in chemical vapour deposition (CVD) growth of large area graphene[25-27]and its exceptional mechanical flexibility[8], graphene based photodetectors may be implemented over large area and in a flexible form at a low cost that is not possible with traditional group III-V semiconductor based technologies.

However, the performance of graphene based photodetectors reported to date is limited at least by two factors arising from its intrinsic characteristics. The first limitation is associated with the low photoresponsivity and very low external quantum efficiency (0.1-0.2%)[16,22] largely due to its intrinsically poor light absorption properties (~2.3% for single layer graphene). Another limitation is the lack of spectral selectivity in intrinsic graphene, which is originated from the

wavelength-independent absorption characteristics of graphene due to the constant universal conductivity G for Dirac fermions[7]. Although the graphene absorption characteristics can be modified in the infrared regime by tuning the Fermi level away from Dirac point[28,29], the spectral selectivity achieved with this approach is however relatively weak with a shallow cut-off edge. To overcome these limitations and achieve overall practical advantages in graphene based photodetectors, here we report a new strategy to fabricate highly sensitive multi-color photodetectors by integrating graphene with a thin layer of plasmonic nanostructures. Plasmonic nanostructures have been explored for surface enhanced Raman spectroscopy of graphene[30]. In this study, we show that the plasmonic nanostructures can be prepared on a first substrate and transferred onto CVD grown graphene without degrade its electronic performance. Here the plasmonic nanostructures can act as subwavelength scattering source and nano-antennas to enhance the optical detection and photoresponse at selected plasmon resonance frequency, and therefore enabling graphene photodetectors that respond sensitively to selected colors. Photoresponse studies show that the integration with plasmonic nanostructures can greatly enhance the photocurrent by up to 1,500%, with the external quantum efficiency reaching up to ~1.5% at zero source drain bias and zero gate voltage, about one order of magnitude better than previously reported graphene devices (~0.1-0.2% at zero bias)[16,22].

B. Device fabrication and characterization.

Figure 2-1 shows the schematic illustration of the process flow to couple plasmonic nanostructures with graphene devices. In general, back-gated graphene transistors are first fabricated on silicon/silicon oxide substrate using CVD grown graphene. The coupling between the plasmonic nanostructures with graphene is accomplished through a transfer process. Specifically, a 4-nm thick gold thin film is first sputtered on a Si/SiO_2 substrate, followed by a thermal annealing process at 350 ^{o}C for 15 minutes under forming gas atmosphere, to result in a high density monolayer of gold nanoparticles (Fig. 2-1a). A poly(methyl methacrylate) (PMMA) layer is then

spin coated onto the gold nanoparticle array to fully wrap the nanoparticles inside, followed by a lifting-off process using buffered oxide etch (BOE) to obtained a free-standing PMMA/nanoparticle thin film (Fig. 2-1b). After repeated rinsing with de-ionized water to remove the BOE residues, the PMMA/nanoparticle thin film is fished by pre-fabricated back-gate graphene transistors (Fig. 2-1c). Finally, PMMA is dissolved away to leave gold nanoparticles on the surface of the graphene devices (Fig. 2-1d).

Scanning electron microscopy (SEM) was used to characterize the gold nanoparticle array before and after the transferring process on Si/SiO_2 surface and graphene surface, respectively (Fig. 2-2a, b). The SEM image of the thermally annealed gold nanoparticles on Si/SiO_2 surface (Fig. 2-2a) shows a high density array of Au nanoparticles with an average diameter ~18 nm and density of 1,320 particle/μm^2 (Figure 2-7). After transferring onto the graphene devices, the gold nanoparticle array structure is well kept with nearly the same morphology (Fig. 2-2b). To investigate the plasmon resonance characteristics of these Au nanoparticle array on graphene, we transferred Au nanopartilces onto a continuous CVD graphene layer on glass substrate using the same process, with which UV-vis spectral analysis is used to study the absorption/scattering characteristics in the gold-plasmonic-nanostructure — graphene heterostructure. The extinction spectrum of the CVD graphene layer shows a nearly flat absorption of ~2.3% (black line in Fig. 2-2c), consistent with the expected absorption by a single layer graphene. Importantly, the nanoparticle-graphene conjugate exhibits a strong plasmon resonance enhanced absorption/extinction of nearly 21% with a pronounced resonance peak around 515 nm (red line in Fig. 2-2c).

Before we developed the transfer process to couple Au nanoparticles with graphene, we have attempted to obtain Au nanoparticle array on graphene by directly evaporating Au thin film on graphene followed by thermal annealing, which can result in similar nanoparticles. However, Raman spectrum of the graphene after this process indicates that the graphene lattice structure is

severely degraded as evidenced by the diminishing 2D peak at 2690 nm (red line in Fig. 2-2d). Further electrical measurement confirms that the device is completely damaged with an open circuit (black line in Fig. 2-2f). In contrast, the coupling of Au nanoparcticles with graphene through the transfer process described above retains the structure integrity of the graphene as shown by the well-kept G peak (1590 nm) and 2D peak (2690 nm) in Raman spectrum (red line in Fig. 2-2e). Electrical measurements show that the graphene device with transferred Au nanoparticles exhibit typical gate transfer and source-drain output performance of a graphene transistors (Fig. 2-2f red line and inset). The carrier mobility of the graphene devices with transferred Au nanoparticles is typically in the range of 1000-2000 $cm^2/V\cdot s$, comparable to those without Au nanoparticles (Figure 2-10).

C. Plasmon resonance enhanced photodetection.

To characterize the photoresponse characteristics of these devices, scanning photocurrent measurement was performed at zero source-drain bias and zero gate voltage, with a well-focused laser beam scanned from source to drain. The short circuit photocurrent is measured as a function of the laser position, with a resolution of ~1 μm (Fig. 2-3a). The location dependent photocurrent measurements of the graphene devices with (red line, Fig. 2-3b) and without (black line, Fig. 2-3b) Au nanoparticles show several important features. First, the maximal photocurrent response is observed when light is focused in the graphene channel near the graphene-metal junction. Second, the position dependent photocurrent plot shows an anti-symmetric characteristic, in which the photocurrent generated at each electrode is opposite and the photocurrent is nearly zero at the center of the channel. These observations suggest that the photocurrent generation is originated from the band offset near the metal—graphene contact. The anti-symmetrical photocurrent in metal-graphene-metal device was also observed in previous reports[16,31], and can be attributed to the nearly symmetric band structure at both contact electrodes along the device. Fig. 2-3c shows the schematic potential profile of the device, with the solid line representing graphene Dirac point and

the dashed line denoting the Fermi level. Due to the smaller work function of contact metal (Ti in our case) than graphene, the graphene under the contact electrodes is a little electron-doped compared to graphene in the channel, leading to a built-in potential barrier across the graphene under metal contact and the graphene in the channel. This is analogous to the traditional p-n junction photodiode, where the photo-generated electron-hole pairs can be separated by the built-in potential, contributing to the total measurable photocurrent. The built-in potential is strongest at the junction area, resulting in a maximal photocurrent detected at this position. Additionally, the same Ti contact of both electrodes can create an opposite symmetric potential profile to result in an anti-symmetrical photocurrent characteristic.

Comparing the photocurrent amplitude, it is obvious to notice that the graphene device with Au nanoparcticles shows an overall 4-5 times higher photocurrent than those without Au nanoparcicles. Power dependence studies show that the photocurrent scales linearly with the excitation power even at zero source-drain bias (Fig. 2-3d). The average peak photo-responsivity is about 0.42 mA/W for the graphene device without Au nanoparticles, comparable to previous studies at zero bias[16,22]. Significantly, a much larger value up to 2.2 mA/W is achieved for the device with the plasmonic gold nanostructures, with an average enhancement of the photoresponsivity by more than 400%.

To confirm that the enhanced photoresponsivity is indeed originated from the enhanced light trapping effect when coupled with plasmonic nanostructures, wavelength dependent photocurrent measurement is conducted with laser focused on one of the graphene-metal junction area. After comparing with the control devices without Au nanoparticles to obtain the enhancement factors at variable wavelength, the spectral dependent response is obtained (Fig. 2-3e). Importantly, the spectral dependent photocurrent enhancement shows an obvious peak around 530 nm, which is close to the extinction peak of graphene—nanoparticle conjugate and strongly

suggests that the enhancement is indeed originated from the plasmon resonance enhanced absorption in graphene devices.

In general, the photocurrent enhancement in graphene devices with Au nanoparticle array can be attributed to both the enhanced near field oscillation and scattering effect of Au nanoparticles. Due to localized surface plasmon of gold nanoparticles, there is an oscillation of conduction electrons that arises in the metal nanoparticles when excited by a specific frequency of electromagnetic radiation. With this oscillation, light is trapped around the surface of the nanoparticles, lead to an enhanced local electrical (optical) field that can effectively enhance the total absorption of graphene. In addition, the scattering effect can also contribute to the enhanced photocurrent, similar to plasmonic enhancement effect observed in 2D nanostructure array[32]. The optical energy scattered by one nanoparticle can be collected by neighbouring nanoparticles as plasmons instead of decaying as free-space light. In this way, the plasmon oscillation of individual Au nanoparticles and the interacting scattering between neighbouring Au nanoparticles can result in a strong coupling between the nanoparticles, trapping light in the plane of the nanoparticle array and localizing optical fields on each nanoparticle, and therefore lead to a greatly enhanced optical field near graphene to dramatically enhance the overall absorption by graphene and the photocurrent.

The photoresponsivity of the plasmonic enhanced devices can be further increased by using Au nanoparticle array obtained by annealing gold thin film of increasing thickness, which can result in larger Au nanoparcticle array with increased scattering cross-section and lead to a further enhancement of local electrical field. Figure 2-3f shows the photocurrent enhancement of graphene devices with nanoparticles obtained from variable starting gold film thickness. Importantly, annealing 8-nm thick gold film can result in the formation of 60 nm diameter nanoparticles with a density of 76 particles/μm^2 (Fig. 2-8), with which on graphene an average photocurrent enhancement >800% can be achieved near graphene-metal junction; with the 110 nm-diameter

nanoparticle array obtained by annealing 12-nm gold film (Fig. 2-9), the photocurrent can be enhanced by about 1,000% (up to 1,500% with a photoresponsivity of 6.1 mA/W). These experiment results agree well with the extinction spectra of various Au nanoparticle array on graphene, in which the absorption/extinction increases significantly with increasing particle size (or the initial gold film thickness) (Fig. 2-11).

To further understand the plasmon resonance enhanced photodetection, we have employed finite-difference time-domain (FDTD) technique[33,34] to calculate the electric field distribution near the gold nanoparticle (nanoplate) array under 514-nm incident light. The simulated electrical field distribution strongly indicates that light is enhanced and trapped in the close proximity of the nanoparticle array (Fig. 2-4a-c). We have further integrated field intensity to achieve average light intensity enhancement versus distance to the plane of nanoparticle array with different nanoparticle sizes (18-nm, 60-nm 110-nm diameter) (Fig. 2-4d). The results show that the average light intensity decays rather rapidly with increasing distance from the nanoparticle plane, which is particularly evident in the smaller sized particle array. These results clearly demonstrate the importance to have a thin active layer (e.g. monolayer of graphene) and to place the active layer in the close proximity of the plasmonic nanostructures to ensure maximum enhancement effect. Considering the PMMA residue between graphene and the nanoparticle array, an average enhancement factor of ~4.5, ~7.5 and ~9.5 is achieved at a ~2 nm distance from the nanoparticle plane by 18 nm, 60 nm and 110 nm diameter nanoparticle array, which agrees well with the photocurrent measurement.

D. Plasmon enhanced photodetector to enable multi-color photodetection.

The highly spectral selective enhancement of the photocurrent in graphene devices can readily allow us to construct multi-color photodetectors by coupling graphene with plasmonic nanostructures of designed plasmon resonance frequency. Importantly, a wide range of plasmonic nanostructures can now be readily created to exhibit distinct resonance frequencies by controlling

the nanostructure size, shape and periodicity. To this end, in addition the Au nanoparticles obtained by simple thermal anneal of Au thin films, we have created well-defined Au nanostructure array on SiO_2/Si substrate using standard E-beam lithography approach. These plasmonic nanostructures were then transferred onto the graphene using a similar process described above. In general, for the 18-nm diameter Au nanoparticles obtained by thermally annealing 4-nm thick gold film, the dark-field optical microscope image of a 50 μm × 50 μm area of such nanoparticles exhibits a distinct green colour, particularly on the peripheral due to strong scattering effect and out-of-plane free space decaying without neighbouring particles (Fig. 2-5a). This green colour in dark field image is consistent with the UV-vis extinction spectrum obtained from such nanoparticle thin films (Fig. 2-2c). The graphene devices coupled with such nanoparticle array (Fig. 2-5b) exhibit photoresponse peak around 530 nm with a consistent maximum sensitivity to green light (Fig. 2-5c). Importantly, a well defined array of 50-nm wide 30-nm high Au nanodisks shows yellow-green colour in the dark field image (Fig. 2-5d), and the devices coupled with such nanodisk array (Fig. 2-5e) show an enhancement peak around 550 nm with a consistent maximum photocurrent response to a yellow-green color (Fig. 2-5f). Further increasing the nanodisk size to 100 nm diameter in a regular array (Fig. 2-5h) leads to a more red-shift in the dark field image color (Fig. 2-5g) with a photocurrent enhancement peak corresponding to a yellow color detection (~ 575 nm) (Fig. 2-5i). Creating rod-like Au nanostructure array (Fig. 2-5k) with orange-red dark field image (Fig. 2-5j) can lead to even more red-shift of photocurrent response to beyond 633 nm (which is our experimental limit due to the limited number lasers available in our confocal microscope) (Fig 2-5l), resulting in a selective detection of the red-end color. The agreement between dark field image color with photocurrent enhancement peak further confirms that enhanced photocurrent is a result of plasmon resonance effect of nanoparticle array.

These studies clearly demonstrate that spectral selective multi-color photodetection can be readily achieved by coupling graphene photodetector with different plasmonic nanostructures.

With this approach, it is possible to integrate multicolour photosensor pixels in a small footprint as little as a few square micrometers or less, and therefore enable a new generation of high performance, high speed, high resolution, low cost and zero operation voltage (zero dark current) photosensor arrays for a wide range of applications ranging from imaging cameras to optical communication devices.

E. Plasmon resonance enhanced photodetection in asymmetric devices.

With the same metal contact on both electrodes in the metal-graphene-metal (MGM) device, the potential profile is symmetric within the channel and the photocurrent is anti-symmetric and opposite near both metal-graphene contacts, leading to a zero total current if device is illuminated globally. To this end, asymmetric metal electrodes can be employed to break the mirror symmetry in band profile to allow the observation of an overall photocurrent in the device, as demonstrated in a recent study[22]. For example, metal of different work functions (e.g. Ti and Pd[22]) can be used as the different contact material (Fig. 2-6a). In this case, the photocurrent generated near the Ti electrode side is identical with Ti-contacted symmetric device (Fig. 2-3). The difference exists at the Pd electrode side, where the high work function of Pd cause nearly no additional doping to the underneath graphene and a nearly flat band structure is formed around this electrode with the expectation of little photocurrent (inset, Fig. 2-6b). Indeed, scanning photocurrent measurement conducted under zero bias and zero gate voltage shows that photocurrent can only be observed near the Ti contact side, but not Pd side (Fig. 2-6b). Similarly, compared to the control device without Au nanoparticles (black line), our plasmonic enhanced device (with 18-nm particle array) exhibits a >400% enhancement, consistent with the symmetric devices discussed above (Fig. 2-3). The global illumination measurement is conducted using a de-focused 532 nm green laser to cover the whole device. Figure 2-6c shows the overall photocurrent

of the asymmetrical device obtained under global illumination with a 5.2K Hz mechanical chopper in front of laser. The periodic photoresponse characteristics exhibit the same frequency as that of the mechanical chopper, clearly demonstrating the generation of overall photocurrent in the asymmetric device in response to global illumination.

F. Discussion and summary

To further probe the plasmon resonance enhancement effect and overall device performance, it is important to determine the overall external quantum efficiency (QE) of the device at zero bias. For the control graphene device without the Au nanoparticles, the photo-responsivity is about 0.4 mA/W at 514 nm, which translates to an external QE of 0.1%, and is comparable to the external QE observed in previously reported graphene photodetectors (~0.1-0.2% at zero bias)[16,22]. Importantly, for the graphene device with Au nanoparticles, the maximum photoresponsivity can reach up to 6.1 mA/W at 514 nm with an external QE of ~1.5%, which is more than one order of magnitude increase over the device without the plasmonic nanostructures under similar bias conditions. Such a high plasmonic enhancement effect is rarely observed in traditional planar semiconductor devices[35] because the local enhancement nature of plasmonic resonance can only affect semiconductor material in the very proximity of the plasmonic nanostructures (e.g. decay length within ~10 nm, see Fig. 2-4)[36], while the active depth of the traditional semiconductor device is usually much bigger. With the nature of a single atomic thickness, the entire graphene can be placed within the close proximity of the plasmonic nanostructures and therefore it can fully exploit the local plasmonic enhancement effect to achieve an unprecedented enhancement. It is also important to note that all our results discussed above were obtained at zero gate voltage and zero source drain bias to pursue zero power consumption

photodetectors. The quantum efficiency can be further improved by tuning the gate voltage (Fig. 2-12), contact metals and/or source-drain bias to optimize the graphene-metal potential barrier[22].

In addition to the built-in electrical potential near the graphene-metal contact, photothermoelectric (PTE) effect has also been reported to contribute a lot in photocurrent generation [37]. In this mechanism, incident light will introduce a different temperature gradient at different part of graphene, resulting a net photo-thermal current at graphene-graphene junction or graphene-metal junction. With our nanoparticle-graphene heterostructure, the part of photocurrent generated by this mechanism can also be greatly enhanced. The nanoparticle array can act as a light absorber, concentrated light on the graphene surface and induced larger temperature gradient, resulting a plasmonic enhanced photo-thermal current.

In summary, we have demonstrated a new concept of highly specific multi-color graphene photodetectors by coupling graphene devices with plasmonic nanostructures. Coupling plasmonic thin film with the atomic thin graphene creates a greatly enhanced local optical field near the graphene plane, and result in an overall plasmonic enhancement by more than a factor of 10. With this substantial enhancement and further optimization of the device structures to improve built-in potential and the active area[22], a further enhancement of the overall photoresponsivity can be expected. Together with demonstrated abilities including zero operation voltage, high speed, flexibility and ultra-wide band absorption, the scalable fabrication of plasmon resonance enhanced graphene photodetectors can open up exciting opportunities for future graphene based optoelectronics. Lastly, coupling the atomically thin graphene with plasmonic nanostructures can most effectively convert local plasmonic enhancement effect into electrical signal to enable fast

direct electrical read-out of plasmonic resonance, and thus has the potential to enable the design of a new generation of plasmon resonance based multiplexed bio-sensor array[38,39].

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H. Figures & Legends

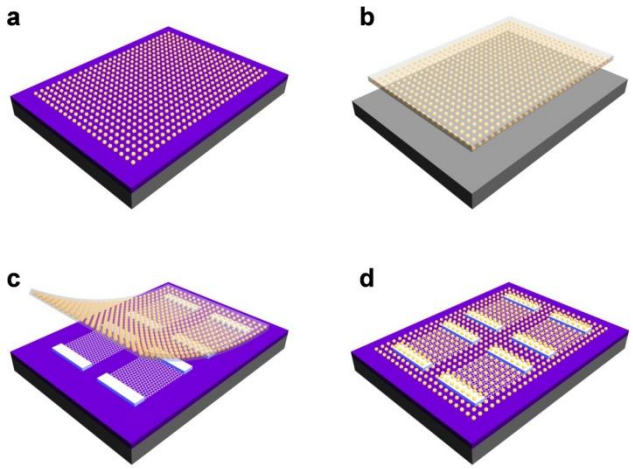

Figure 2-1. Schematic illustration of the fabrication process to integrate plasmonic nanoparticles with graphene transistors to obtain plasmon resonance enhanced photodetectors. a, Gold nanoparticles are obtained by thermally annealing 4-nm thick gold film on the SiO_2 substrate. **b**, PMMA is spin-coated on substrate, followed by a lifting-off process using buffered oxide etch to obtain free-standing PMMA/Au-nanoparticle thin film. **c**, PMMA/Au-nanoparticle thin film is fished by pre-made back-gate CVD graphene transistors. **d**, PMMA is dissolved away to leave gold nanoparticles on the surface of the graphene devices. Gray, blue, yellow and white represent silicon, silicon dioxide, gold nanoparticles, and gold electrode, respectively.

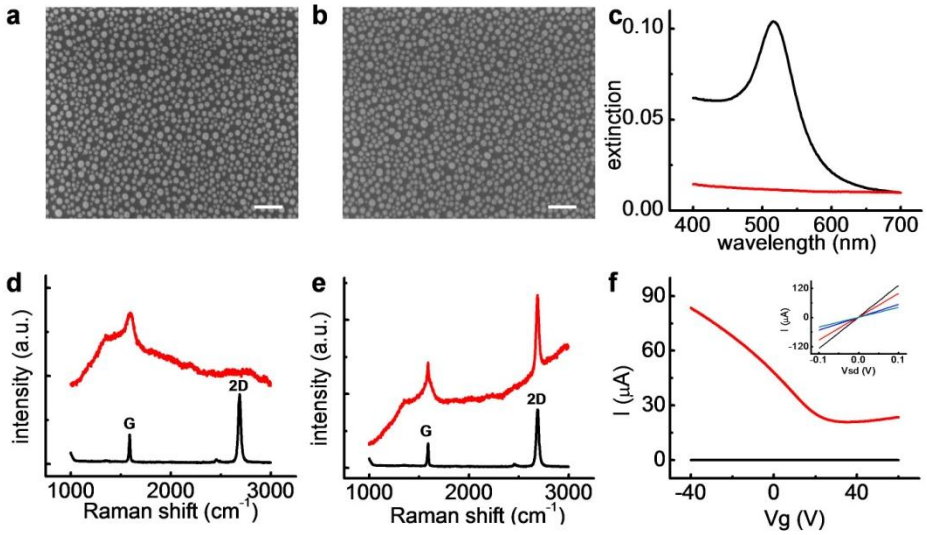

Figure 2-2. Characterization of the graphene and graphene transistors with transferred gold nanoparticles. **a,** SEM image of the gold nanoparticles obtained by annealing Au thin film on SiO_2 surface at 350 ^{O}C before transferring process. Scale bar 100 nm. **b,** SEM image of gold nanoparticles transferred onto graphene surface. Scale bar 100 nm. **c,** UV-vis spectrum of graphene on glass (black line) shows nearly flat spectrum with an absorption of ~2.3%, and that of nanoparticle/graphene (red line) on glass shows a plasmonic resonance peak around 515 nm with a peak absorption of ~21%. **d,** Raman spectroscopy of the graphene (black line), and graphene with Au nanoparticles obtained by direct annealing 4-nm gold thin film on graphene (red line). The diminishing 2D peak (2690 nm) indicates the nearly complete destruction of graphene structure by the Au deposition and annealing processes. **e,** Raman spectroscopy of graphene (black line), and graphene with transferred Au nanoparticles (red line). The G peak (1590 nm) and 2D peak (2690 nm) is well kept in this case, demonstrating that the integrity of the graphene is preserved. **f,** Transfer characteristics (I-V_g) at V_d = 50 mV for a back-gated graphene transistor with transferred Au nanoparticles (red line), and a graphene transistor with directly annealed Au nanoparticles (black line). The inset shows the source drain current I versus source-drain voltage V_{sd} of the graphene transistor with transferred Au nanoparticles at gate -20, 0, 20, and 40 V (black, red, blue, and green lines) respectively. The device has a length of 8 μm and width of 8 μm. These studies demonstrate the electrical performance of the graphene transistors is retained in the device with transferred Au nanoparticles, but not in the device with directly annealed Au nanoparticles, consistent with Raman studies.

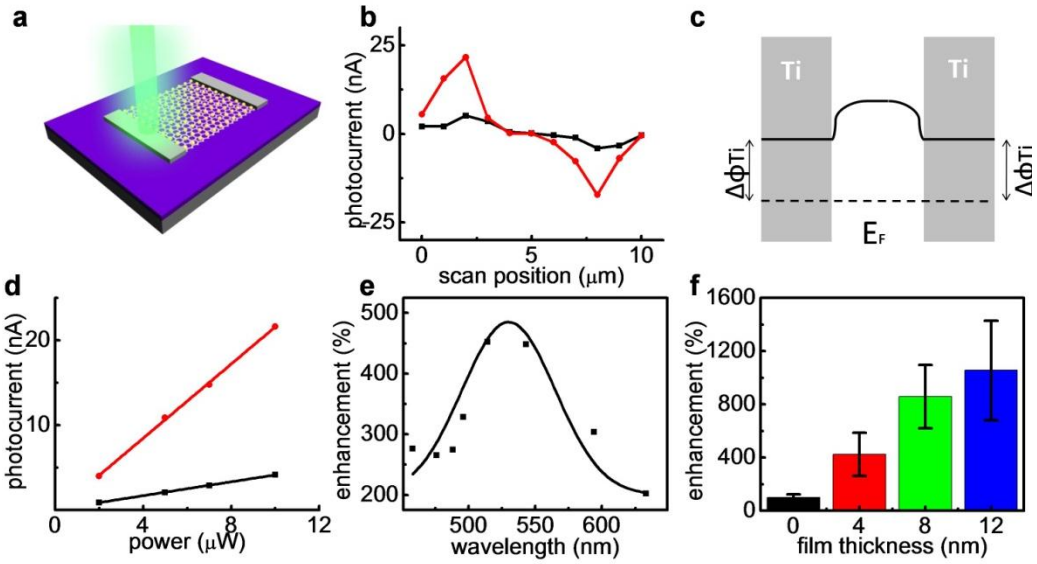

Figure 2-3. Photocurrent measurement of the plasmon resonance enhanced graphene photodetectors with a localized laser excitation under a confocal microscope. a, Schematics of graphene photodetector, with a laser scanning across the graphene-metal (Ti) junction. All devices studied have a channel length of ~8 μm and channel width of ~8 μm. **b**, Photocurrent measurement with laser scanning from the outside of source electrode to the outside of drain electrode shows anti-symmetric photocurrent response. The red and black lines indicate the response of the device with and without Au nanoparticles, respectively. The electrode width is 1 μm, and the laser wavelength is 514 nm with a total power of 10 μW. **c**, Band profile of the graphene photodetector. $\Delta\varphi_{Ti}$ represents the difference between Dirac point energy and Fermi level in Ti doped graphene. The Ti electrode contact slightly dopes the graphene with electrons to shift its Fermi level up towards Dirac point, and creates a potential barrier between the graphene under the electrodes and the graphene in the channel. **d**, Photocurrent generated as a function of laser power. The red and black lines indicate the response of a typical device with and without Au nanoparticles, respectively. Laser wavelength is 514nm. **e**, Photocurrent enhancement as a function of laser wavelength, indicating an enhancement >400% can be observed in the devices with plasmonic Au nanoparticles, and the spectral response of the enhancement is consistent with the plasmonic resonance spectrum of the Au nanoparticles. The black squares represent the experimental data points and the solid line is the guide to the eye. **f**, The photocurrent enhancement with Au nanoparticles obtained by annealing Au film of variable initial thickness (0, 4, 8, and 12 nm). With increasing Au film thickness, there is increasing plasmon resonance intensity, leading to an

increased enhancement effect, with a maximum enhancement of ~1500% observed in the device obtained from 12-nm film. The error bars show the variation of device performance from 5 devices.

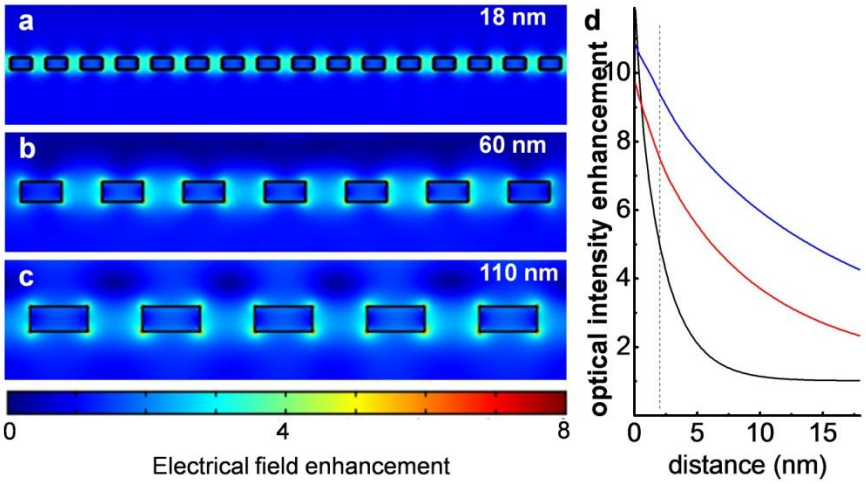

Figure 2-4. Finite-difference time-domain (FDTD) simulation of plasmon resonance enhancement of local optical field near the nanoparticle array. a, **b**, **c**, Electrical field distribution near the gold nanoparticle (nanoplate) array with an average particle diameter of 18, 60 and 110 nm, respectively. The field images are cross-section of the nanoparticle array and are achieved by two dimensional FDTD calculations. **d**, Average enhanced light intensity versus distance to the plane of nanoparticle array with different nanoparticle sizes (18-nm, 60-nm 110-nm diameter). The results show that the average light intensity decays rather rapidly with increasing distance from the nanoparticle plane.

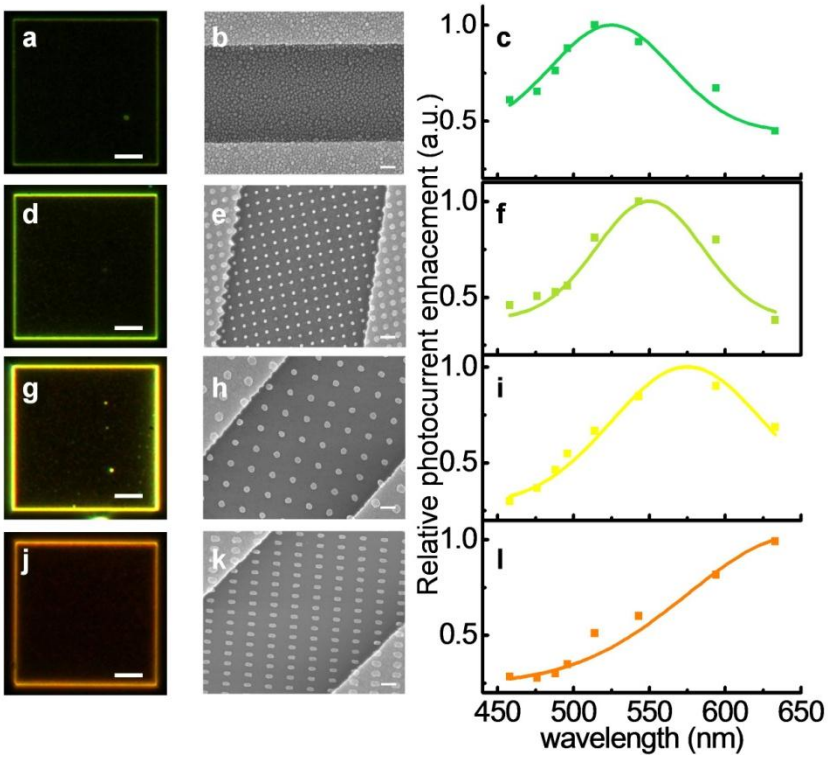

Figure 2-5. Multi-color photodetection using graphene devices coupled with different plasmonic nanostructures. a, Dark field image of a 50 μm×50 μm area of 18-nm diameter nanoparticle array obtained by thermally annealing of 4-nm Au thin film. **b,** SEM image of a representative device with the nanoparticle array, and **c,** the corresponding spectral response of the photocurrent enhancement. **d,** Dark field image of a 50 μm×50 μm area of 50-nm diameter 30-nm height nanodisk array. **e,** SEM image of a representative device with the 50-nm diameter nanodisk array, and **f,** the corresponding spectral response of the photocurrent enhancement. **g,** Dark field image of a 50 μm×50 μm area of 100-nm diameter 30-nm height nanodisk array. **h,** SEM image of a representative device with the 100-nm diameter nanodisk array, and **i,** the corresponding spectral response of the photocurrent enhancement. **j,** Dark field image of a 50 μm×50 μm area of 100-nm length, 50-nm width, and 30-nm height nanorod array. **k,** SEM image of a representative device with the nanorod array, and **l,** the corresponding spectral response of the photocurrent enhancement. Scale bars are 200 nm in (**b**, **e**, **h**, and **k**). The plasmonic nanostructures in (**d**, **g**, and **j**) are obtained by e-beam lithography to defined Au patterns. The square symbols and the lines in (**c**, **f**, **i**, and **l**) represent the experimental data points and the line guide to the eye. The photocurrent measurement is obtained by focused laser illumination the grahene-metal contact of graphene

device with ~8μm channel length and 8 μm channel width. The spectral response of graphene devices is consistent with the dark field image color of the corresponding plasmonic nanostructures, further confirming the plasmonic enhancement effect and demonstrating that he multi-color photodetection can be achieved by coupling the graphene devices with plasmonic nanostructures of different resonance features.

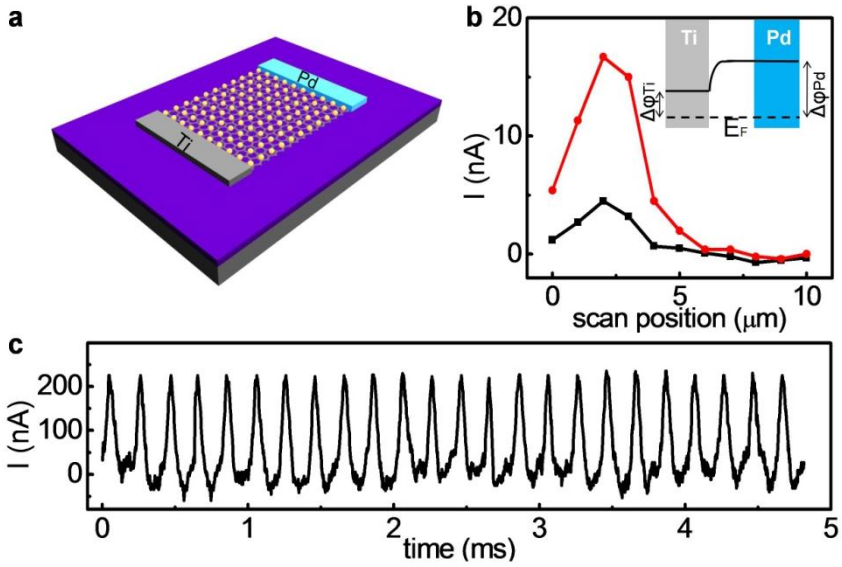

Figure 2-6. Plasmon resonance enhanced graphene photodetectors with asymmetric metal contacts under global illumination. a, Schematic illustration of a graphene photodetector with asymmetric metal contacts (Ti and Pd respectively) that can enable photocurrent generation under global illumination. **b,** Photocurrent profile with laser scanning from outside of Ti electrode (black line: normal graphene device; red line: plasmon resonance enhanced graphene device). The inset shows the band profile of asymmetric metal contacted graphene photodetector. $\Delta\varphi_{Ti}$ and $\Delta\varphi_{Pd}$ represent the difference between Dirac point energy and Fermi level in Ti-doped graphene and Pd-doped graphene, in which Ti raises the Fermi-level energy position, while Pd maintains nearly the original Fermi level position of the intrinsically p-doped graphene. The photocurrent can only be seen near the Ti electrodes because bend bending only occurs there. **c,** Time dependent photocurrent measurement with a global laser (532 nm) illumination and a 5.2 KHz chopper.

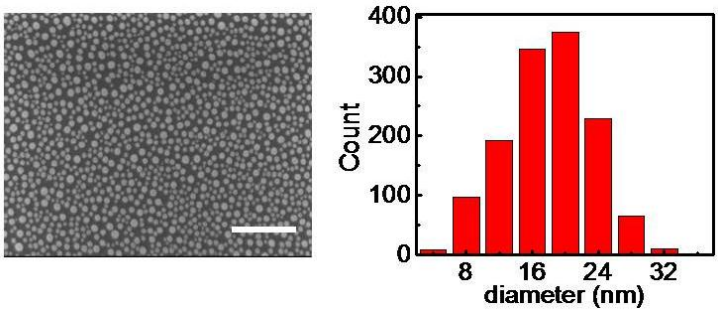

Figure 2-7. (left) SEM image and of the Au nanoparticles obtained by annealing 4-nm thick gold thin film. The scale bar in SEM image is 200 nm. (right) Size distribution histogram with an average diameter of 18 nm and a particle density of 1320/μm^2.

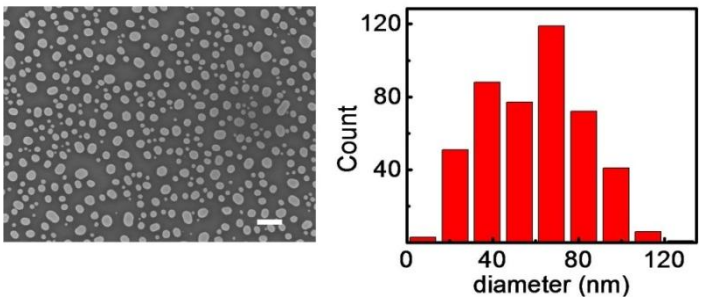

Figure 2-8. (left) SEM image and of the Au nanoparticles obtained by annealing 8-nm thick gold thin film. The scale bar in SEM image is 200 nm. (right) Size distribution histogram shows an average diameter of 60 nm and a particle density 76/μm^2.

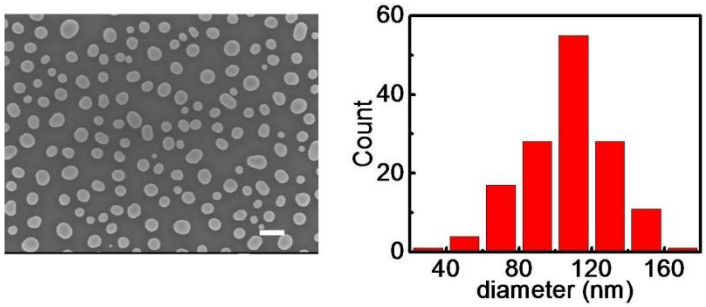

Figure 2-9. (left) SEM image and of Au nanoparticles obtained by annealing 12-nm thick gold thin film. The scale bar in SEM image is 200 nm. (right) Size distribution histogram shows an average diameter of 110 nm and a particle density 28/μm^2.

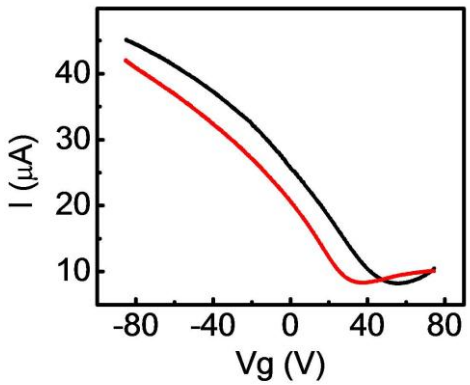

Figure 2-10. Transfer characteristics of graphene before ((black line) and after (red line) transferring gold nanoparticle thin film. Electrical property of graphene is well kept after transferring process with a little n-doping (Dirac point shifts to negative direction). The mobility of the back-gated device can be determined by the equation: $\mu=[dI_{ds}/dV_g]\times[L/WC_iV_{ds}]$, where L is the channel length, W is the channel width, C_i is the capacitance between the channel and back gate per unit area. The carrier mobility was determined to be 1140 cm^2/Vs before transferring and 1280 cm^2/Vs after transferring gold nanoparticles, highlighting the transferring process and gold nanoparticles don't produce any obvious impact on the charge transport in graphene.

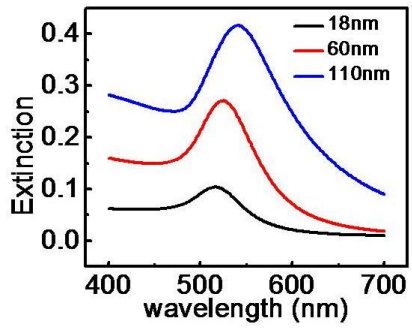

Figure 2-11. Extinction spectra of nanoparticle-graphene conjugates on glass. Compared with 18-nm particles (~21% extinction at 530 nm), the 60-nm nanoparticle array shows a little red-shift peak and an overall peak extinction of ~45%, and 110-nm nanoparticle array show a more red shift and ~61% peak extinction.

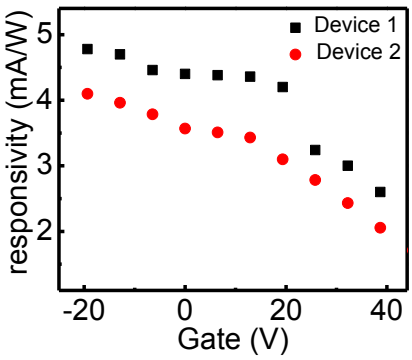

Figure 2-12. Photo-responsivity as a function of back gate voltage for two plasmon resonance enhanced photodetectors. The responsivity can be greatly reduced by applying a positive gate voltage. On other hand, the responsivity can also be increased by applying a negative gate voltage, however, to much a smaller degree. We believe this is because that our graphene device is relatively highly p-type doped intrinsically, and applying of additional negative gate voltage would only have limited ability to increase the potential barrier.

Chapter II: HIGHLY FLEXIBLE MACROELECTRONICS FROM SCALABLE VERTICAL THIN FILM TRANSISTORS

A. Introduction to vertical thin film transistor

Thin film transistors (TFTs) represent the fundamental device building blocks for macroelectronics that requires the distribution of functional electronic components over large area. Flexible plastic is becoming the preferred substrate for macroelectronic applications because of their light weight, flexibility, short resistance and low cost. To this end, flexible thin-film transistors (TFTs) are of central importance for a wide range of macroelectronic applications including flexible displays and electronic paper, electronic paper and radio frequency identification[1-7]. To ensure the compatibility with flexible plastics and to mitigate the cost in large area fabrication, current TFT technologies normally adopt lower performance materials (typically amorphous or polycrystalline materials processed at low temperature) and lower resolution lithography (typically with 10s micrometer transistor channel length) with the resulting devices typically having relatively poor electrical performance or insufficient mechanical robustness. For example, amorphous indium gallium zinc oxide (α-IGZO) can be readily prepared through a RF sputtering process, and IGZO based TFTs have attracted considerable interest for applications in large area electronics (or macroelectronics)[8,9]. However, the performance of the IGZO based TFTs is often limited by two intrinsic factors of the α-IGZO material. First, the intrinsically lower carrier mobility of the α-IGZO material (~5-20 $cm^2/V\cdot s$) poses a limit in the overall current density of the IGZO TFTs and consequently the switching speed. Second, the brittle nature of the ceramic IGZO film make it ill-suitable for highly flexible electronics on plastic substrate because the in-plane cracks in the IGZO thin film can severely degrade the lateral charge transport in the conventional planar IGZO TFTs.

Graphene has emerged as an exciting material for flexible electronics due to its superior electrical and mechanical properties[10-19]. However, the lack of an intrinsic band gap in graphene makes it unsuitable for logic transistors. New concepts of vertical transistors and barristers have recently been reported by exploring the heterostructures of graphene with flakes of layered materials[20-23]or silicon wafer[24], which is however difficult to scale, too costly or too rigid for flexible macroeletronics. Here we report a new design of highly scalable and flexible vertical thin-film transistors (VTFTs) based on the heterostructure of graphene and amorphous indium gallium zinc oxide (α-IGZO) thin film. By using graphene as a unique work function tunable contact for the IGZO semiconducting channel, we show that the vertical current flow across the graphene-IGZO junction can be effectively modulated to achieve VTFTs with a highest ON-OFF ratio exceeding 10^5. Importantly, the VTFT architecture can readily enable transistors with ultra-short channel length (typically <100 nm as determined by the thickness of the IGZO thin film rather than by lithography) to afford a delivering current greatly exceeding that of the conventional planar TFTs. With the availability of large area graphene and IGZO thin film, our strategy is intrinsically scalable for large scale integration of VTFT arrays and logic circuits (inverters, NOR/NAND logic gates) on the wafer scale. Furthermore, unlike conventional planar IGZO TFTs, in which any cracks in the IGZO channel can severely degrade the lateral charge transport[25], the vertical (out-of-plane) current flow in the VTFTs is largely unaffected by the in-plane cracks, and thus can enable a new generation of highly flexible macroelectronics with exceptional electrical and mechanical performance.

B. Fabrication of graphene based vertical thin film transistor

Our design of vertical thin-film transistors (VTFTs) are based on the vertical heterostructures

of graphene-IGZO-metal stack (Figure 3-1a,b). Here graphene functions as a unique work function tunable (by an external gate) contact to IGZO thin film to enable effective modulation of the vertical current flow across the graphene-IGZO junction and achieve a large ON-OFF switching ratio. The concept of VTFTs can offer several combined advantages not readily possible in conventional planar TFTs. First, with the design of graphene-IGZO heterostructure based VTFTs, the ultra-short channel transistors (typically <100 nm as determined by the thickness of the IGZO thin film rather than by lithography) can be readily created by *using low resolution lithography* to afford a delivering current greatly exceeding that of the conventional planar TFTs. Second, the vertical (out-of-plane) charge transport across the large area vertical junction makes the source-drain current much less affected by the in-plane cracks in the IGZO thin films to afford unprecedented tolerance to in-plane crack (Figure 3-1c,d). It can therefore simultaneously address two most critical challenges (low delivering current and insufficient mechanical flexibility) of conventional planar inorganic (e.g. IGZO) TFTs to enable a new generation highly flexible electronics with exceptional electrical performance and mechanical robustness.

To fabricate the vertical heterostructure devices (Figure 3-2), a thin film of 60-nm thick Ti is first sputtered as the adhesion layer and drain electrode on a pre-patterned metal (Au) finger on a selected substrate, followed by RF sputtering of α-IGZO as the channel material. The use of the Ti layer with low work function (4.33 eV) is important for making Ohmic contact with IGZO to ensure the delivery of high current density by the VTFTs. Next, a monolayer of graphene grown by chemical vapor deposition (CVD) approach is transferred onto the IGZO thin film, as the source electrode. After photolithography and oxygen plasma etching, graphene is patterned into 10×50 μm stripes. The channel area is defined by the overlapping area between graphene layer and the

IGZO/Ti thin film, which is around 10×10 μm^2 and highlighted by dash line in Figure 3-2a. Finally, a thin film of 40-nm thick Al_2O_3 is deposited on top of the channel as the gate dielectric, followed by the e-beam deposition of Ti-Au gate electrode. The optical microscope image (Figure 3-2a) and the cross-sectional scanning electron microscope (SEM) image (Figure 3-2b) of a typical VTFT clearly show eight distinct layers, including the entire vertical stack of Au-Ti-Al_2O_3-Graphene-IGZO-Ti on the silicon/silicon nitride substrate.

C. Electrical transport of vertical thin film transistor

Electrical transport studies of the as-fabricated VTFTs were carried out at room temperature under ambient conditions. The output characteristic of a VTFT with a 100-nm thick IGZO film clearly shows that the source-drain current increases with increasing positive gate voltage (Figure 3-3d), indicating that electrons are the majority charge carrier in this vertical transistor, consistent with the typical n-type semiconducting behaviour observed in α-IGZO thin film[9]. Overall, the VTFT showed an exceptionally high current exceeding 600 μA for a 10×10 μm device, which is at least two orders of magnitude larger than that of a planar IGZO TFT with a similar sized footprint (Figure 3-6). The device can also be completely switched off in the negative bias direction with a negative gate voltage to achieve the highest ON-OFF current ratio exceeding 10^5, sufficient for high performance logic operations.

In general, the gate voltage applied across the vertical stack can modulate the doping level or work function of the graphene (Figure 3-3a-c), as well as the charge concentration in the IGZO layer and the relative Schottky barrier height/width across the graphene and IGZO interface. A negative gate voltage increases the work function of graphene and the Schottky barrier height with

n-type IGZO. At V_g = -4 V, the Schottky barrier height is increased to ~640 mV (Figure 3-3b and Figure 3-7). At this point, the graphene-IGZO junction behaves as a Schottky diode with an ideal factor as small as 1.27 (Figure 3-8), where a full current rectification is observed with the current in the negative direction completely switched off. With increasing gate voltage towards the positive direction, the work function of graphene is reduced and so does the Schottky barrier height with IGZO, thus greatly enhance the current at the negative bias. At V_g = 4 V, the barrier height between graphene and IGZO is reduced to ~40 mV (Figure 3-7), the VTFT is switched to the ON-state (Figure 3-3c), and its output characteristic shows nearly linear Ohmic behaviour.

Because the gate modulation is achieved by tuning the electron barrier height at the graphene-IGZO interface, our VTFT typically shows asymmetric transfer characteristics. In the reverse biased region with a negative bias to the top-graphene electrode (Figure 3-3e), the electrons are injected from graphene into IGZO (inset, Figure 3-3e), where the current is strongly dependent on the barrier height φ_b according to the equation[26]:

$$I_{sat} = AA^{*} T^{2} \exp\left(\frac{-q\varphi_b}{kT}\right)$$

where A is the Schottky junction area, A^* is the effective Richardson constant, q is the element charge, k is the Boltzmann constant and T is the temperature. In this case, the current increases exponentially with the decreasing barrier height. This leads to a very large ON-OFF current ratio over 10^5 at a source drain bias -0.1 V. Increasing the bias in the negative direction increases the current density but will lead to a small drop in the ON-OFF current ratio, which could be attributed to the large bias induced barrier lowering effect[26]. Overall, the device can function as an effective

transistor with a large enough ON-OFF ratio for logic applications in the reverse bias regime. The subthreshold swing of VTFT is further analysed in Supporting information S4.

In the forward biased region with a positive voltage applied to the graphene electrode, the transfer characteristics can be separated into two parts. In the small forward bias region where $V_{sd} < \varphi_b$ (e.g. $V_{sd} = 0.1V$) (Figure 3-3f, right inset), the current is still limited by the electron diffusion across the graphene-IGZO barrier, result in a small current at OFF-state and a large current modulation with the ON-OFF ratio > 10^3. While in the large forward bias region (e.g., $V_{sd} = 1V > \varphi_b$) (Figure 3-3f, left inset), source drain bias overcomes the graphene-IGZO barrier, at which point the electrons can be directly injected into graphene without significant influence from graphene-IGZO barrier and gate voltage, leading to a large current density and small ON-OFF current ratio. According to band diagram, the only current limitation in this region comes from the small barrier formed between Ti and IGZO.

We have further investigated the channel length (the thickness of the IGZO thin film) scaling relation of our VTFTs. Figure 3-3g shows the room-temperature ON-OFF current ratios of the VTFT as function of different IGZO thickness at a source drain bias of -0.1 V. The ON-OFF current ratios are strongly dependent on the IGZO film thickness. In general, it is found that a large ON-OFF ratios over 10^5 can be achieved with thick IGZO (100 nm thickness), which gradually decreases to 2 when the IGZO thickness is reduced to 20 nm. This trend can be explained by a short-channel effect. With the decreasing IGZO thickness, the potential of the entire channel becomes more and more dominated by the electric field of the Ti metal electrodes, which can reduce the OFF-state graphene-IGZO Schottky barrier height, resulting in a smaller ON-OFF current ratio (Figure 3-3g, insets). This observation is also consistent with our recent studies of

graphene-MoS_2 heterostructure based vertical transistors[22].

D. Scalable fabrication of graphene based vertical thin film transistor

The above studies clearly demonstrate that high performance VTFTs can be readily achieved with high ON-OFF ratio using the graphene-IGZO heterostructures. With the recent availability of large area CVD graphene[27-31] and the scalability of the RF sputtering process, our integration strategy is intrinsically compatible with conventional photolithography-based microfabrication process, and can be readily implemented on the wafer scale in high yield, allowing us to demonstrate the fabrication of a large array of VTFTs and functional logic circuits on the wafer scale, which is not yet possible for similar vertical transistors based on exfoliated flakes of layered materials such as MoS_2 or WS_2 flake[20-23]. To evaluate the scalability and reproducibility of our integration strategies, we have fabricated an array of VTFTs with over 1600 devices on a 2-inch wafer (Figure 3-4a,b). Importantly, our process exhibits a high yield over 85% across the entire wafer. The failure mostly comes from the broken graphene due to the un-optimized transfer process, which can be improved in future upon optimizing the transfer techniques or using multiple layers of graphene.

The high yield fabrication of VTFTs with large ON-OFF ratio on the wafer scale can readily allow us to integrate multiple VTFTs into functional circuits. For example, a NMOS logic inverter can be achieved with two VTFTs connected in series, where gate and drain of the top VTFT is connected to make a depletion load (Figure 3-4c). At 1 V source-drain bias, the inverter displays sharp switching behaviour with a gain 1.26 (Figure 3-4d). Taking a step further, more complicate logic function can be created by connecting more VTFTs together. For example, a logic NOR or

NAND function can be created using 3 VTFTs, respectively (Figure 3-4e,g). The measured input and output voltages clearly demonstrate the correct logic function for the NOR and NAND gate (Figure 3-4f,h). Overall, these results clearly demonstrate our VTFTs can provide a scalable pathway to high performance logic applications.

E. High flexibility of vertical thin film transistor

For macroelectronic applications, there is increasing interest in applying functional electronic circuits on large area plastic substrate for flexible electronics. The function of active transistors on plastic substrate is however often limited by the intrinsic material performance (e.g. very low carrier mobility of conventional inorganic or organic thin film semiconductors) or insufficient mechanical robustness (e.g. extreme brittleness of ceramic IGZO film). Although the IGZO thin film have been explored for the fabrication of flexible transistors on plastics[8,32], but only with limited success to date. In particular, the brittle nature of IGZO film makes it non-ideal for highly flexible electronics because any small in-plane crack of the IGZO thin film can severely degrade the lateral charge transport in conventional planar IGZO TFTs (Figure 3-1c). In contrast, with our design of graphene-IGZO heterostructure based VTFTs, the current transport across the vertical direction is largely unaffected by the in-plane crack in the IGZO film (Figure 3-1d). It can therefore enable a new pathway to high performance flexible electronics using conventional brittle material.

Additionally, since our entire fabrication process is conducted essentially at room temperature, our VTFTs can be readily fabricated on plastic substrate using the same processing steps. The only fabrication difference is that thicker dielectric (300nm Al_2O_3) are used to avoid

gate leakage since flexible substrate have large surface roughness than silicon wafer (Figure 3-5a). Indeed, devices made on the polyethylene terephthalate (PET) substrate exhibit similar output characteristic to those on silicon wafer (Figure 3-5b). In general, when applying negative gate voltage, large Schottky barrier is formed and device shows nearly ideal diode behaviour. With positive gate bias, the VTFT is turned on with linear IV Ohmic characteristics. The transfer characteristics show that a large ON-OFF current ratio exceeding 10^4 can be achieved for flexible logic applications (inset of Figure 3-5b).

We have further compared the mechanical robustness of our VTFTs with conventional planar TFTs under increase bending stress (decreasing bending radius) or repeated bending cycles. The mechanical failure of inorganic TFTs under bending is generally associated with the strain-induced cracking or bucking in the films[8,9,25]. These cracking or slip could severely limit the lateral current flow across the channel in conventional planar TFTs (Figure 3-1c), resulting in a smaller current, larger resistance and the mechanical failure of the devices. However, within our VTFT architecture, the current flow vertically (out-of-plane) from the bottom-Ti to top-graphene electrode and those in-plane lateral cracks no longer pose obstacles for the current flow (Figure 3-1d). This can be clearly demonstrated in the bending test at various bending radius (Figure 3-5c). As expected, the conventional TFTs with planar device structure suffer large conductance drop with reducing bending radius (< 10 mm), result from the strain induced in-plane crack of the IGZO channel; In contrast, the VTFTs are not influenced much with stable current delivery until a bending radius as small as 1-2 mm.

We have further compared the planar TFTs and VTFTs under repeated bending cycle test at a fixed bending radius of 5 mm (Figure 3-5d). For the planar TFTs, the current drops by about 5

orders of magnitude from their initial state within 50 bending cycles due to the formation of small cracks or dislocations inside the channel under repeated bending cycles. Further increasing the bending cycles leads to the complete device failure, suggesting the formation of a continuous crack cross the channel area. On the contrary, the VTFTs are much more robust under repeated bending cycles. The current level show little change up to 1000 bending cycles. These bending test studies clearly demonstrate the overall robustness of VTFTs under large bending curvature or repeated bending cycles and its unique advantages for flexible electronics.

F. Summary

In summary, we have demonstrated a new design of high performance VTFTs based on graphene-IGZO junction. The unique vertical device architecture takes the full advantage of high mechanical strength of graphene and the out-of-plane current flow to ensure high delivering current and overcome the critical bending limitation of conventional planar inorganic TFTs to promise a transistor technology that is highly tolerant to repeated mechanical bending. Our approach is intrinsically scalable and can be readily extended to a wide range of semiconductor thin films including the solution processable ones[4,5] to enable a low-temperature, low cost process to high performance VTFTs on plastic substrate, and threrefore defines an new pathway to high performance macroelectronics. With a combination of high current density, high ON-OFF current ratio, exceptional flexibility and wafer scale process, our VTFTs satisfy the practical requirements for high performance logic applications for a wide range of flexible, wearable and disposable electronics.

G. Reference

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H. Figures and Legends

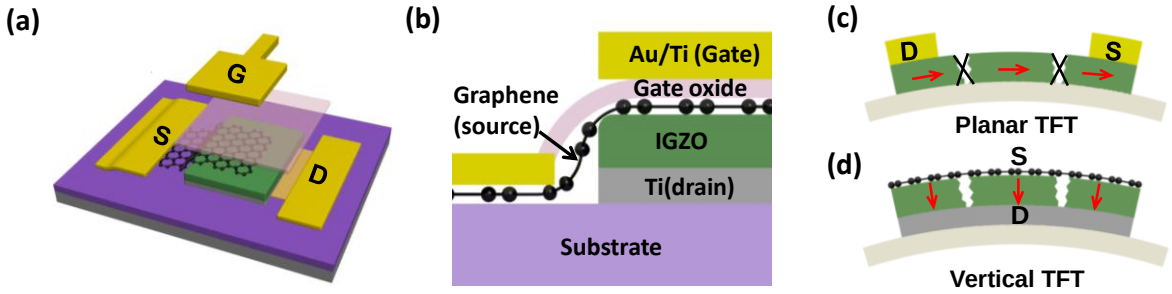

Figure 3-1. Schematic illustration of the graphene-IGZO VTFT. a, A schematic of the three-dimensional perspective view of the device layout. **b**, A schematic of the cross-sectional view of the device, with the graphene and bottom Ti thin film functioning as the source and drain electrodes, the IGZO layer as the vertically stacked semiconducting channel with its thickness defining the channel length. A 40-nm thick thin film of Al_2O_3 is used as the gate dielectric and Ti/Au thin film as gate electrodes. **c**,**d**, Schematics of device operation of the planar TFT and VTFT on flexible plastic substrate. Red arrows indicate current flow across channel, which can be severely limited by cracks in the planar TFT, but not affected in the VTFT.

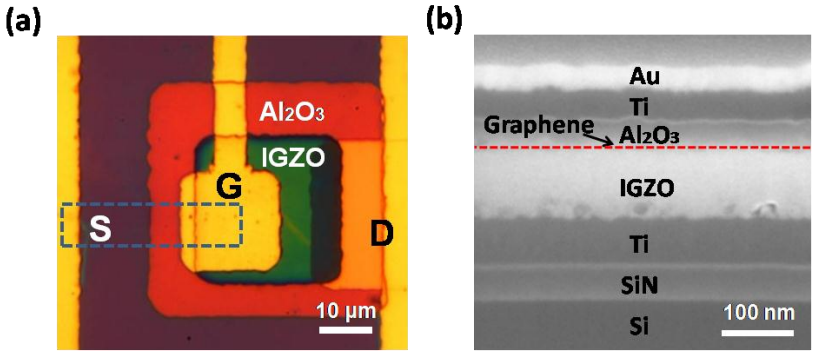

Figure 3-2. Structural characterization of the graphene-IGZO VTFT. a, Optical top view image of a VTFT. Ti/IGZO stack is the dark green area, Al_2O_3 is the orange area, Ti/Gold is yellow area and graphene is highlighted by the dashed lines. The active channel area is defined by the overlap between the graphene and IGZO. **b**, A cross-sectional SEM image of a VTFT, clearly illustrating 8 layers of the vertical stack. Graphene is highlighted by dash line.

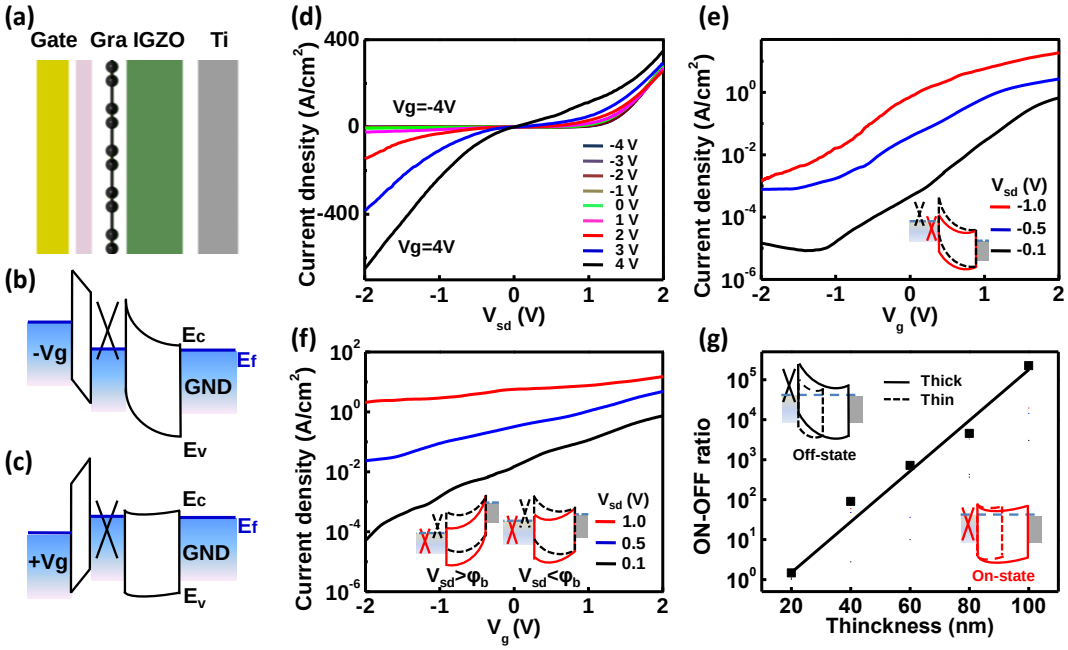

Figure 3-3. Room temperature electrical properties of the VTFTs. a, A schematic layout of the critical layers of the vertical transistor. Gate electric field is applied from left gate electrode on top of graphene and grounded Ti electrode. **b**, **c**, The band structure under negative gate voltage **b** and positive gate voltage **c** at zero source-drain bias. **d**, I_{sd}-V_{sd} output characteristics of a VTFT at various gate from -4 V to +4 V (1 V step). The current is normalized by the area. **e**, I_{sd}-V_g transfer

characteristics of the device shown in **d** in reverse region where V_{sd} = −0.1, −0.5 and -1 V. The band diagram of the corresponding ON- (red) and OFF-(black) state at negative bias is shown in the inset. **f,** I_{sd}-V_g transfer characteristics of the device shown in **d** in positive bias region where V_{sd} = 0.1, 0.5 and 1 V. The band diagrams of the corresponding ON- (red) and OFF- (black) state at small positive bias ($V_{sd}<\varphi_b$) (right inset) and at large positive bias ($V_{sd}>\varphi_b$) (left inset). **g**. The ON-OFF current ratio of the VTFTs with various channel length (IGZO thickness) at a source-drain bias of -0.1 V. The inset shows the band diagrams for thick (solid) and thin (dashed) IGZO film at ON- (red) and OFF- (black) state, respectively.

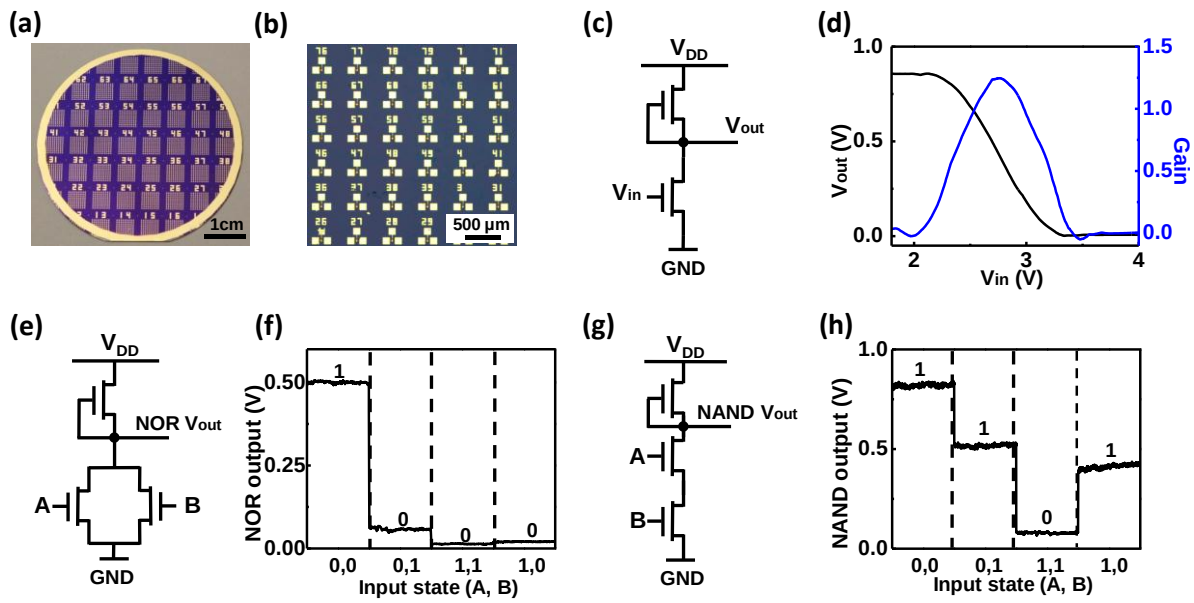

Figure 3-4. Scalability and logic applications of graphene-IGZO VTFTs. a, A photograph of a 2-inch wafer with an array of 1620 VTFTs. **b**, An optical image of a large array of VTFTs fabricated on Si/SiN_x substrate. **c**, Schematic of a inverter obtained by integrating 2 VTFTs in series, with the top one as a depletion load. **d**, Output behaviour of the inverter as a function of input voltage. Power supply (V_{DD}) is at 1 V and the peak gain is ~1.26. **e**, Schematic of a logic NOR gate obtained by integrating 3 VTFTs. **f**, Output voltage levels of the logic NOR gate at four typical input states and 1 V power supply (V_{DD}). **g**, Schematic of a logic NAND gate obtained by integrating 3 VTFTs. **h**, Output voltage levels of NAND logic gate at four typical input states at 1 V power supply (V_{DD}).

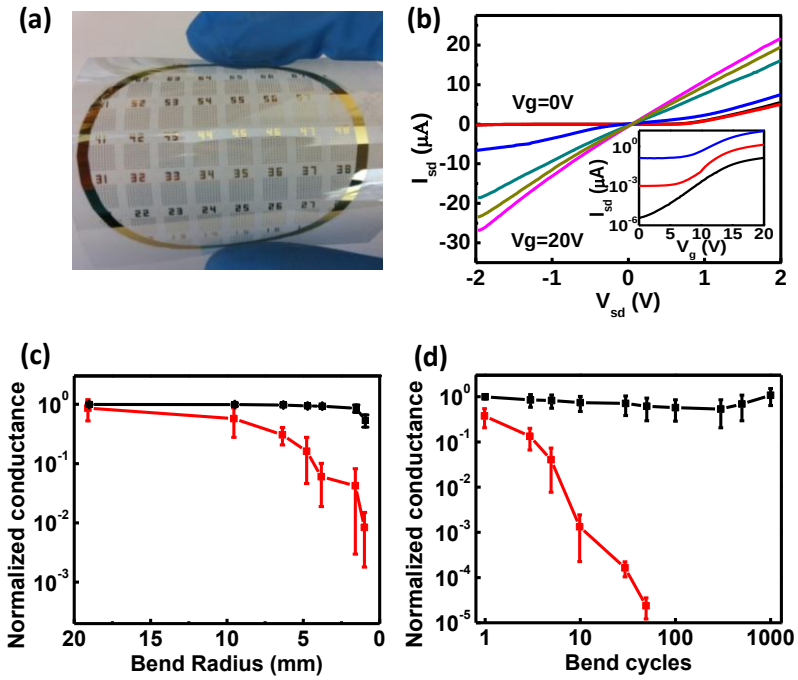

Figure 3-5. VTFT as a unique architecture for highly robust flexible electronics. a, Photograph of a large array of VTFTs integrated on PET substrate. **b**, I_{sd}-V_{sd} output characteristics of a VTFT on PET substrate at various gate from 0 to 20 V (4 V step). Inset: I_{sd}-V_g transfer characteristics of the device in reverse region where $V_{sd} = -0.1$ (black), -0.5 (red) and -2 V (blue). **c**, Normalized conductance at various bending radius for planar TFT (red) and VTFT (black). **d**, Normalized conductance at various bending cycles for the planar structure (red) and vertical structure (black), highlighting significant greater robustness of the VTFT architecture. All the data are obtained from the average of 8 typical tested devices.

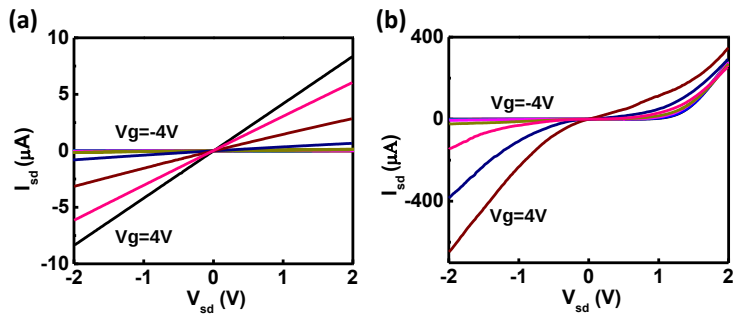

Figure 3-6. a, I_{sd}-V_{sd} (output characteristic) curve of a conventional planar IGZO TFT at various gate voltage. The device channel area is 10×10 μm^2. **b**, I_{sd}-V_{sd} (output characteristic) curve of a IGZO VTFT at various gate voltage. The device channel area is 10×10 μm^2, which is the same as our VFETs. The gate voltage step is 1V.

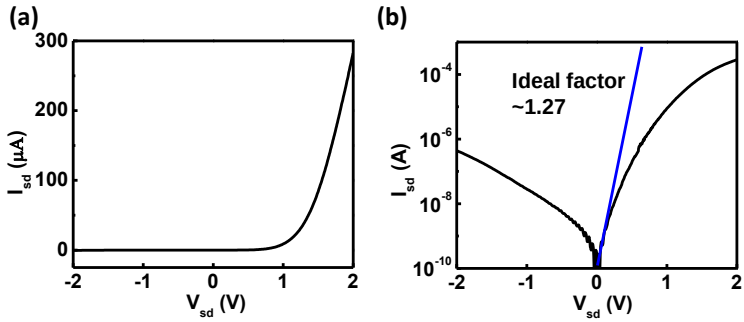

Figure 3-7. a, I_{sd}-V_{sd} curve of graphene-IGZO VFETs at OFF state (V_g=4 V), showing a typical current rectification behaviour. **b**, Semilog plot of **a** showing the ideal factor around 1.27.

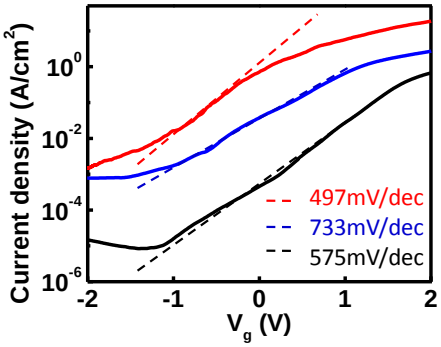

Figure 3-8. Subthreshold swing (SS) of VTFTs derived from Figure 2. The red, blue black dash lines indicate a SS with bias of -1 V, -0.5 V and -0.1 V, respectively.

Chapter III: HIGH PERFORMANCE ORGANIC VERTICAL THIN FILM TRANSISTOR USING GRAPHENE AS A TUNABLE CONTACT

A. Introduction of organic vertical thin film transistor

Organic thin film transistors (OTFTs) have received significant attention over the past decade for their potential in low-end, large-area electronic and optical applications.[1-6] Obvious advantages over their silicon counterparts include flexibility, large area manufacture, and low processing costs. Despite considerable efforts and progresses to date, two major challenges remain for current OTFTs. First, with rather low carrier mobilities, organic transistors typically deliver relatively low driving current compared to their inorganic counterparts, resulting in low operating speeds. Secondly, compared to p-type OTFTs, the development of n-type organic semiconductors has lagged behind due to their high sensitivity to ambient conditions,[7] which causes poor stability and reliablity. In order to overcome these limitations, considerable efforts have been devoted to preparing higher mobility materials[8] and/or developing surface passivation strategies.[9-11] These approaches have successfully improved the delivering current and air-stability, but often at a sacrifice of additional costs and complexities of fabrication processes. Here we report a new strategy to fabricate high-performance organic vertical thin film transistors (OVTFTs)[12,13] based on the heterostructures formed between monolayer graphene and organic semiconducting thin films. By using graphene as a unique, work function-tunable contact for the organic semiconductor channel, we show that the vertical current flow across the graphene–semiconductor junction can be effectively modulated to achieve an ON/OFF ratio over 10^3. Furthermore, our vertical design readily allows transistors with ultra-short channel lengths (typically ~100 to 200 nm as determined by the thickness of the spin-coated thin film) without typical lithography processes, delivering a maximum current density over 3.4 A/cm^2 and transconductance over 0.66 S/cm^2, greatly exceeding

those of conventional planar OTFTs. With our unique vertical architecture, the entire organic channel is sandwiched between the source and drain electrodes, which function as both a self-passivation layer to ensure air-stable operation of both p- and n-channel devices. Furthermore, we studied the frequency response of graphene based vertical transistors. Without high-resolution lithography processing, our vertical transistor enable a maximum cutoff frequency up to ~0.4 MHz, comparable with previous ultra-short channel planar OTFTs using the same channel material.[14,15] This high delivering current and air-stable operation of our vertical organic transistors opens up new opportunities in organic electronics, macroelectronics, and graphene based flexible circuits.

B. Device fabrication

Figure 4-1a and 4-1b shows a schematic illustration of the graphene–organic semiconductor–metal sandwich structure. To fabricate the device, graphene grown using the chemical vapor deposition (CVD) approach[16-19] is first transferred onto a silicon substrate with 68 nm thick SiN_x, followed by photolithography and oxygen plasma etching to form graphene stripes (100 × 200 μm) as the bottom source electrode. Thin film organic layers are then spin-coated on the surface of graphene as the channel material (see methods). Several different organic semiconducting materials, including p-type poly(3-hexylthiophene-2,5-diyl) (P3HT); p-type poly({4,8-bis[(2-ethylhexyl)oxy]benzo[1,2-b:4,5-b′]dithiophene-2,6-diyl}{3-fluoro-2-[(2 ethylhexyl)carbonyl]thieno[3,4-*b*]thiophenediyl}) (PTB7)[20]; and n-type phenyl-C61-butyric acid methyl ester (PCBM), are used to demonstrate the versatility of our fabrication strategy and the ability to integrate complimentary OTFTs together. Within our device structure, the channel length is controlled by the thickness of the organic thin films and is typically around 100 to 200 nm.

Finally, a metal thin film (Au for p-type and Ti/Au for n-type) is deposited through a shadow mask and used as the drain electrode. The channel area is defined by the overlapping junction area between the top metal and bottom graphene electrodes, as shown in the optical image in Figure 4-1c. Figure 4-1d shows a cross-section scanning electron microscopy (SEM) image of a typical graphene–P3HT–Au structure, where the sandwich of different layers is clearly seen.

C. Electrical transport of organic vertical thin film transistor

Electrical transport studies of the vertical devices were carried out at room temperature under ambient conditions. For the measurements of all devices made from different materials (P3HT, PTB7, PCBM), the bottom-layer graphene is always grounded as the source electrode, while the top-metal is used as the drain electrode. Figure 4-2c shows the output characteristics of the graphene–P3HT–Au vertical structure device. As shown by the band diagram schematic in Figure 4-2a, there is little barrier between Au and P3HT due to the work function match.[21] The carrier transport is dominated by the junction between graphene and semiconducting P3HT, which is similar to graphene–inorganic[22-27] and graphene–organic[28-31] vertical heterostructures studied previously. In general, a gate voltage applied from the back gate can modulate the doping level or work function of the graphene. A positive gate voltage (red dashed line) accumulates electrons in graphene and decreases its work function, leading to a larger barrier with p-type P3HT. At this point, the graphene–P3HT junction behaves as a Schottky diode, where current rectification is observed and the current in the negative bias regime is completely switched off (cyan line). With decreasing gate voltage towards the negative direction, the work function of graphene is increased and the height of the Schottky barrier with P3HT is reduced, thus greatly enhancing the current at the negative bias and switching the device into the ON state. Under this ON state (purple and gray curve), current under positive bias is smaller than that under negative bias, indicating the relatively

smaller graphene–P3HT barrier compared to the Au–P3HT barrier. The current decreases with gate voltage, which mimics p-type transistor behavior (Figure 4-2c). The transfer characteristics are semi-log plotted in the inset of Figure 4-2c, where an ON/OFF ratio over 10^3 is observed, demonstrating the potential of OVTFT for digital electronics and logic based applications.

Our fabrication strategy is versatile and can be applied to other solution-processable semiconductors beyond P3HT. To this end, we have fabricated similar vertical heterojunction transistors using PTB7 (p-type) and PCBM (n-type) as the channel materials and studied their transistor characteristics. Graphene–PTB7–Au heterostructures show similar electrical transport behavior as the P3HT system (Figure 4-2d), where a larger (smaller) barrier is formed at positive (negative) gate voltages, mimicking p-type FET behavior. Compared with Figure 4-2c, the current level drops by about one order of magnitude, indicting either poor vertical charge transport inside PTB7 or the formation of a large barrier between the PTB7–graphene and PTB7–Au interfaces. Furthermore, we have fabricated graphene–PCBM–Ti vertical heterostructures using the n-type PCBM thin film as the channel material. Ti is used here as the top metal to match the work function and minimize the contact barrier with PCBM.[32] The electrical measurements of the graphene–PCBM–Ti vertical heterostructure show expected opposite behavior (Figure 4-2e) to those observed in P3HT and PTB7 based heterostructures. A negative gate voltage increases the work function of graphene and the barrier height with n-type PCBM (Figure 4-2b), rendering the device in its OFF state with obvious rectifier behavior. By increasing the gate voltage toward the positive direction, both the graphene work function and barrier height will be decreased, resulting in a large delivery current under positive bias, mimicking typical n-type FET characteristics. With the demonstration of three different channel materials above, our generalized fabrication strategy has the potential to be extended to any solution-processable thin film semiconductors that utilize

simple spin coating.

D. Air-stability of organic vertical thin film transistor

Besides the ultra-short channels, the unique sandwich structure creates a self-encapsulation of the semiconductor layer by the source and drain electrodes that protect the delicate organic materials. This is particularly important for n-type organic semiconductors that are usually highly sensitive to ambient environments. The instability is largely attributed to the oxygen and/or water that diffuses into the semiconducting channel and degrades its performance.[6] In traditional planar device structures, the channel material is exposed to air without any protection and will degrade rather quickly under ambient conditions.[9] To evaluate the enhanced stability in our vertical transistors, we fabricated n-type PCBM devices with a conventional planar structure as a control device. The channel length and width are 50 μm and 100 μm, respectively. Figure 4-5 shows that when measured in air, the planar device becomes an open circuit without any current flow. This is consistent with previous reports, where oxygen is shown to easily diffused into the channel, destabilizing and trapping negative charge in the PCBM.[33] We also note this does not mean that the PCBM is destroyed by oxygen exposure: the planar devices recover upon returning to a vacuum environment (Figure 4-5). However, in our vertical structure, the entire channel area is sandwiched between the graphene and metal electrodes, which works as passivating layers that protect the channel material from the environment. Figure 4-3a shows the transfer characteristics of a typical n-type PCBM vertical device measured in air after exposure for one week, clearly showing that good switching behavior is retained. It is noted that the drain current level is reduced to around half of its original value, which is significantly more stable than the planar device structure that is completely in-operational in air. The output characteristics after being exposed to air for one week is plotted in the inset (Figure 4-3a), where the barrier based $I-V$ curve is retained

and can be readily modulated by the gate voltage, again indicating good air stability of our vertical transistors. This is further demonstrated by the time dependent ON current measurement (Figure 4-3b), which remains relatively stable when the device is exposed and measured in air.

Besides working as a self-passivation layer, the top-drain electrode can also act as an etching mask to pattern the organic material underneath. As shown in Figure 4-3c, the left image is our as-fabricated device where PCBM is spin-coated as a continuous film over the substrate, and the right image is after we immerse our device into chloroform for 10 seconds. It is clearly shown that the excess PCBM film is etched away, while the channel area protected by the top metal electrode remains untouched. From this point of view, the OVTFT is not only stable in air as demonstrated previously, but also stable in its chemical solvent. Furthermore, this self-aligned patterning technique utilizes the electrode as the mask to define the channel area and etch away any unnecessary polymer without introducing additional lithography or etching steps that tend to degrade the performance of OTFTs. In general, this is an effective method for isolating individual OTFT devices, reducing leakage currents, and scaling up towards integrated circuits.

More importantly, this self-aligned patterning approach allows for flexible integration of multiple organic semiconductors on the same substrate to create functional circuits. For example, after the graphene–PCBM–metal devices are fabricated and patterned to create isolated n-channel OVTFTs using the approach described above, another layer of p-type P3HT is spin-coated and used to fabricate p-channel OVTFTs for creating complementary circuits directly on one chip. With this strategy, a complementary inverter is fabricated on a 30 nm Al_2O_3/p^{++}-silicon substrate. The output characteristics of the inverter show a sharp switching behavior with voltage gain over unity (Figure 4-3d), indicating the possibility for future integration of complementary OVTFTs.

E. Frequency response of organic vertical thin film transistor

With the ultra-short channels determined by the thickness of the spin-coated films, our unique design of vertical organic transistors can deliver very large current densities to enable moderate frequency operation with low-performance organic semiconductors and low-resolution lithography. To evaluate the frequency performance, we fabricated OVTFTs on glass substrates with isolated gate electrodes to reduce the source–gate and drain–gate coupling capacitance. First, a patterned thin film Ti/Au (5/25 nm) is deposited as the back gate electrode, followed by atomic layer deposition (ALD) of 30 nm thick Al_2O_3 as the gate dielectric. All other fabrication processes follow the same steps as the graphene–P3HT–Au devices on silicon/silicon nitride substrates. Figures 4-4a-c show the schematic illustration and optical microscope images of the device structure. Figure 4-4d shows the transfer characteristics under different bias voltages in ambient environment. Importantly, a large delivery current up to 170 μA can be achieved at a source-drain bias of −9 V, corresponding a current density 3.4 A/ cm^2. The transconductance derived from the slope of the transfer characteristic show a maximum transconductance (G_m) of 33 μS at a gate voltage of 3 V and source drain bias of –9V (Figure 4-4e).

We further evaluated the operation frequency limit of the devices using standard measurement techniques. For the unity-gain bandwidth, the upper frequency limit (cutoff frequency, f_T) is reached when output and input AC levels exhibit the same amplitude. Beyond this cutoff frequency limit, the output of a first transistor is not able to drive a second transistor of the same kind and it is thus not possible to have an effective signal cascade in circuit applications. To experimentally measure the f_T, a sinusoidal wave [3 V + 0.5 V × sin(ωt)] is applied to the gate while a constant DC voltage (−9 V) is applied to the drain. The AC components of the input and output current are measured by an Agilent DSO3202A oscilloscope connected with a constant

resistor. Figure 4-4f shows a set of gate (input) and drain (output) currents as a function of frequency. First, the gate current is plotted as black squares. It can be observed that I_{gate} increases linearly with frequency ($I \propto \omega C$), where a measured capacitance of 18.6 pF (1 MHz) can be derived from the slope of this curve. This measured capacitance is comparable with our calculated value of 20.93 pF using the expression $C = \varepsilon_r \varepsilon_0 S/d$, where d is 30 nm, S is 100×100 μm^2 and $\varepsilon_r = 7.1$. On the other hand, the output drain current (red dot) remains relatively stable below the cutoff frequency f_T. Beyond that point, I_{drain} is dominated by the coupled gate capacitance. Within our device geometry, an f_T value ~ 0.2 MHz was measured, as shown in Figure 4-4f. It should be noted that effective channel area of our vertical device is determined by the overlapping area of the vertical source–drain–gate electrodes, while there is considerable source–gate overlap (around half of the area shown in Figure 4-4c) that does not contribute to drain current but contributes to the parasitic gate capacitance. To exclude these parasitic capacitances, we manually de-embed the OVTFT by calculating the effective gate capacitance to be 10.45 nF and then calibrate the resulting effective gate current ($I_{gate\text{-}c}$) as the blue triangles using this value (Figure 4-4f). The calibrated intrinsic cutoff frequency of the vertical transistor is determined to be ~0.4 MHz (Figure 4-4f), which is comparable to that of ultra-short channel P3HT planar transistors with sub-micron channel length.[14,15] Considering our OVTFTs usually have a footprint on the scale of 100 × 100 μm^2 without any high-resolution lithography, such a high cutoff frequency could not be achieved using conventional planar OTFT structures.

F. Summary

In summary, we have fabricated high-performance OVTFTs based on graphene–organic semiconducting thin film heterostructures. By utilizing monolayer graphene as a work function-

tunable contact electrode, we demonstrate a general strategy of OVTFT fabrication with ultra-short channel length without using conventional high-resolution lithography processes. Electrical studies show that our vertical transistors exhibit excellent switching behavior with an ON/OFF ratio over 10^3. Additionally, they deliver a high current density over 3.4 A/cm^2 and thus enable high cutoff frequency devices comparable with other ultra-short channel organic transistors. Within our unique vertical architecture, the entire organic channel material is sandwiched between the source and drain electrodes and is thus naturally protected to ensure excellent air-stability. Furthermore, the top metal works as a self-aligned etching mask for the organic polymer underneath, allowing us to easily integrate both p- and n-type materials on the same substrate to enable complementary circuits with voltage gain. This high delivery current, self-passivated air stability, and simplistic fabrication of our vertical organic transistors open up new opportunities in organic macroelectronics.

G. Reference

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H. Figures and Legends

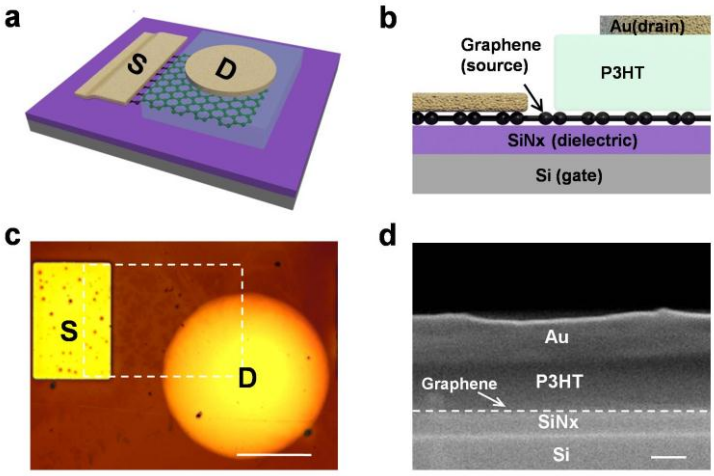

Figure 4-1. Schematic illustration and structural characterization of a graphene–P3HT–Au OVTFT. a, A schematic of the three dimensional perspective view of the device layout. **b,** A sc hematic of the cross sectional view of the device, with the graphene and top gold thin film function ing as the source and drain electrodes. The P3HT layer is the vertically stacked semiconducting ch annel with its thickness defining the channel length. **c,** Optical top view image of an OVTFT. Grap hene is highlighted by the dashed lines and the effective channel area is defined by the overlapping area between graphene and the top gold (drain) electrode. The scale bar is 100 μm. **d,** A cross secti

onal SEM image of an OVTFT, clearly illustrating layers of the vertical stack. Graphene is highlig hted by the dashed line. The scale bar is 100 nm.

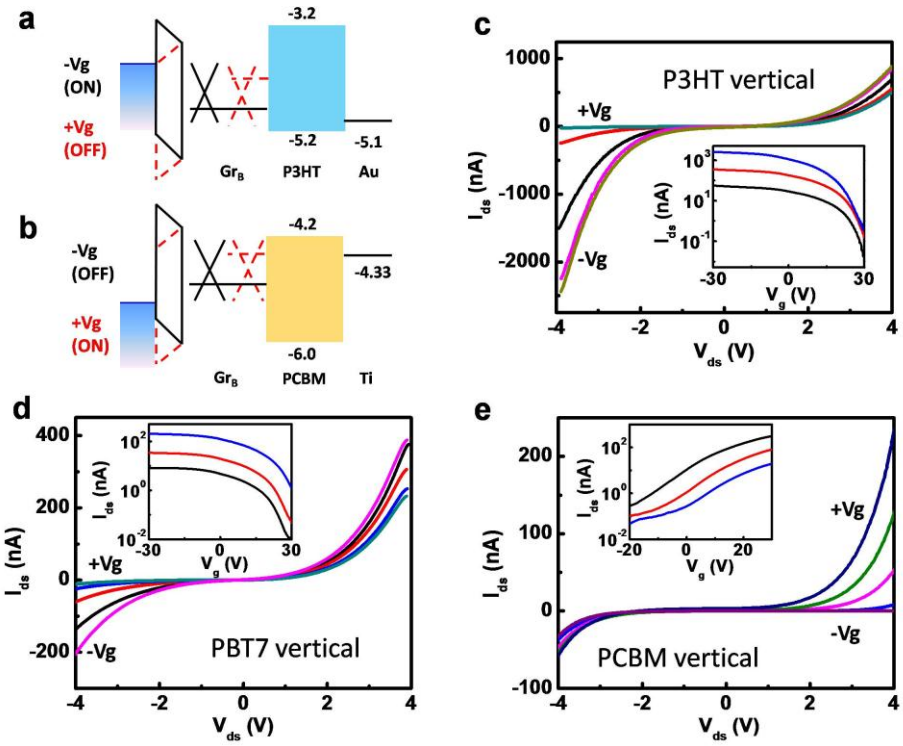

Figure 4-2. Room temperature electrical properties of the OVTFTs. **a,** The band diagram for p-type OVTFTs under a negative gate voltage (ON state, solid line) and positive gate (OFF state, dashed line). **b,** The band diagram for n-type OVTFTs under a negative gate voltage (OFF state, solid line) and positive gate (on state, dashed line). **c, d,** I_{ds}–V_{ds} output characteristics of a graphene–P3HT–Au (**c**) and graphene–PTB7–Au (**d**) p-type OVTFTs at various gate voltages from −30 V to +30 V (15 V steps). The transfer curve is semilog-plotted in the insets with various bias voltages where V_{ds}= −1 V (blue), −2 V (red), and −4 V (black). **e,** I_{ds}–V_{ds} output characteristics of a graphene–PCBM–Ti n-type OVTFT at various gate voltages from −30 V to +30 V (15 V steps). The transfer curve is semilog-plotted in the inset with various bias voltages where V_{ds} = 1 V (black), 2 V (red), and 4 V (blue).

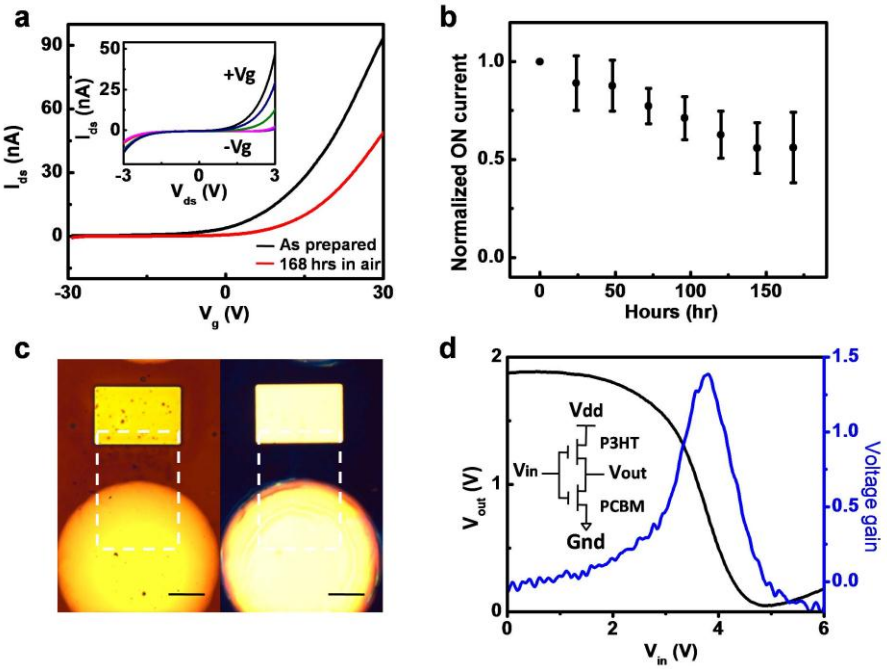

Figure 4-3. Air-stability of the OVTFTs. a, Transfer characteristics of a graphene–PCBM–Ti OVTFT. The black curve is measured directly as prepared, while the red curve is measured 1 week later after being exposed to air. The bias is 3 V. Inset is the output characteristic after exposure in air for 1 week at various gate voltages from −30 V to 30 V (15 V steps). **b,** Normalized ON current as a function of exposure time in air. The ON current remains at more than a half of the original after being exposed in air for 1 week, indicating very good stability. **c,** Optical image of graphene–PCBM–Ti OVTFT before (left panel) and after (right panel) being immersed in chloroform, suggesting the top electrode also acts as an etching mask to pattern OVTFTs. The scale bar is 50 μm. **d,** Output voltage (black line) and voltage gain (blue line) as a function of the input voltage for complementary OVTFTs.

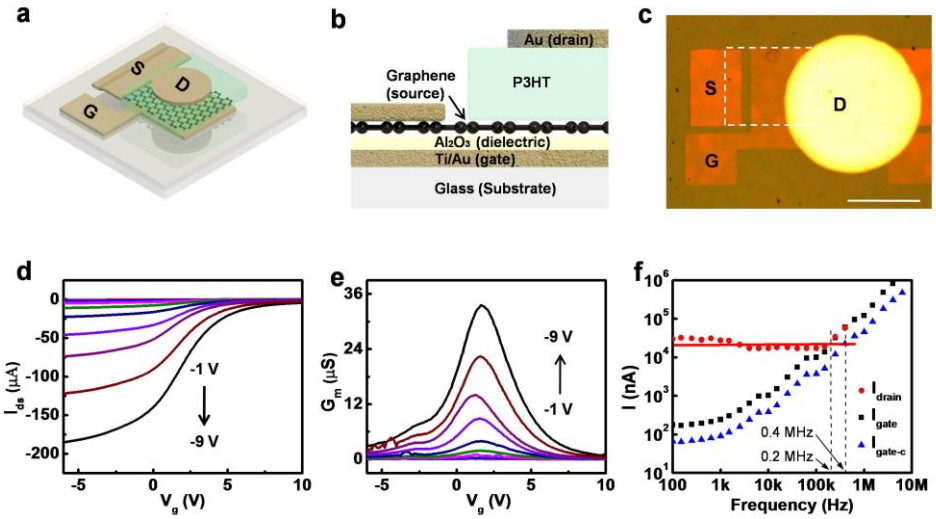

Figure 4-4. Operation frequency of a graphene–P3HT–Au OVTFT on glass. a, A schematic illustration of the three-dimensional perspective view of the device layout on glass. **b,** A schematic illustration of the cross-sectional view of the device, where the glass serves as the substrate, Ti/Au as the gate, ALD Al_2O_3 as the dielectric, and the graphene and top gold thin film functioning as the source and drain electrodes, respectively. **c,** Optical image of a typical OVTFT, where graphene is highlighted by the dashed line. The scale bar is 100 μm. **d,** Transfer characteristics of an OVTFT on glass at different bias voltages from −1 V to −9 V (1 V steps). **e,** Transconductance as a function of the gate voltage at different bias voltages. **f,** Gate and drain AC current as a function of input frequency signal. The red dot is the measured drain current and the black square is the measured gate current. The blue triangle is the calibrated gate current by condering the effective gate area and gate capacitance.

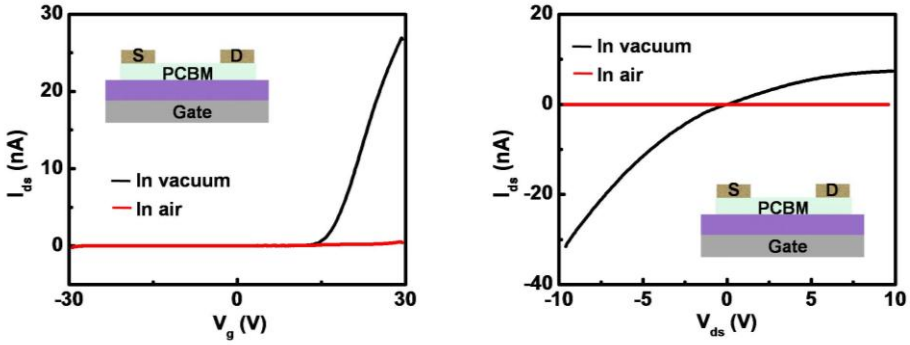

Figure 4-5. Air stability of a planar PCBM thin film transistor. a, Transfer characteristic of the PCBM planar OTFT measured in vacuum (black) and in air (red). The bias voltage is 9 V. **b,**

I_{ds}−V_{ds} curve of the PCBM TFT measured in vacuum (black) and in air (red). The gate voltage is 30 V.

Chapter IV: TOWARDS BARRIER FREE CONTACT TO MOLYBDENUM DISULFIDE USING GRAPHENE ELECTRODES

A. Introduction of MoS_2 transistor and its Schottky contact

Two-dimensional (2D) layered semiconductors such as molybdenum disulfide (MoS_2) are of considerable interest for a new generation of ultrathin electronics and optoelectornics.[1-11] However, their promises have been largely stalled by the difficulties in making optimized metal contacts to these atomically thin materials. Substantial efforts have been devoted towards addressing this challenge by using low work function metal electrodes, high temperature annealing, or phase engineering.[12-22] Although some of these approaches have successfully reduced the contact resistance, it is not yet possible to achieve linear Ohmic contact particularly at low temperature, where a finite Schottky barrier dominates the carrier transport due to Fermi level pinning at conventional metal-MoS_2 interface.[16] This contact barrier prevents fundamental investigation of the intrinsic charge transport properties in these atomically thin semiconductors and poses a serious challenge towards optimized device performance.

Herein we present a new strategy by using graphene as a tunable contact for achieving an Ohmic contact to 2D semiconductors. With a finite density of states, the Fermi level of graphene can be readily modified by a gate potential to ensure a nearly perfect match with MoS_2 when in the ON-state. We demonstrate graphene can make a transparent contact to MoS_2 under a proper gate voltage, thus achieving essentially zero barrier and linear output behaviour at cryogenic temperatures (down to 1.9 K). Furthermore, benefited from the minimized contact barrier, our device displays a record high extrinsic (two-terminal) field effect mobility up to 1300 $cm^2/V\cdot s$ at low temperature. We believe our strategy of using graphene as a barrier-free contact could shed

light on contact engineering in atomically thin semiconductors as well as other conventional semiconductors in general.

B. Device fabrication

To fabricate our devices, two strips of single layer graphene are first mechanically exfoliated onto a silicon/silicon dioxide (300 nm) substrate and used as the back contact electrodes, with the distance between these two graphene strips defining the channel length of the device (Fig. 5-1a). Next, a mechanically exfoliated monolayer or multi-layer MoS_2 (confirmed by PL in Fig. 5-6) strip is directly transferred on top of two graphene electrodes, using a dry alignment transfer technique (see Method section and Fig. 5-7). This direct integration of exfoliated graphene contact with the exfoliated MoS_2 without contacting any other material is essential for avoiding lithography/etching process introduced polymeric residues that can adversely impact the charge transport behaviour across the graphene/MoS_2 vertical contact. The residue-free dry transfer method provides an atomically sharp and ultraclean interface between graphene and MoS_2 (Figure 5-7), which can ensure pure *van der Waals* contacts and minimize defects and charge trapping sites. Finally, Cr/Au thin film (10/50 nm) electrodes are used to contact graphene to yield the final device with standard e-beam lithography, metal deposition and lift-off processes (Fig. 5-1b). A cross sectional transmission electron microscope (TEM) images of the graphene/MoS_2 stack show atomically smooth interfaces (Fig. 5-1c).

C. Barrier free contact using graphene electrode

All electrical transport studies are carried out in a dark environment. Figure 5-2a and 5-2c shows standard *I-V* output characteristics at room temperature for monolayer and multilayer MoS_2 (20 to 30 layers) with similar W/L ratios around 1. Without any post-fabrication annealing process,

our devices exhibit linear *I-V* output characteristic in both cases. As the temperature is lowered down to 1.9 K, a slight non-linearity is observed near zero source-drain bias at small gate voltages (< 40 V). Nonetheless, it is important to note that the linear *I-V* and Ohmic behaviour remains when the gate voltage is sufficiently high (80 V for monolayer and 60 V for multilayer) (Fig. 5-2b, d), suggesting a transparent and barrier free contact for MoS_2 at cryogenic temperatures under such gate voltages. This behaviour is observed in all of our devices (over 20 samples) with additional data at different temperatures shown in figure 5-8 and figure 5-9**.** To the best of our knowledge, this low temperature Ohmic contact behaviour has never been achieved before. The closest case is a high-temperature annealed titanium contact in which obvious nonlinear behaviour is still observed at 5 K.[20]

The excellent contact in our devices may be attributed to two reasons. First, due to the unique linear dispersion relationship with a finite density of states in the vicinity of graphene's K points, the Fermi level could be easily shifted by the gate voltage and result in a perfect band matching with MoS_2.[23,24] With 80 V gate voltage, the work function of graphene could be shifted up to ~4.15 eV,[25] which is lower than the electron affinity of MoS_2 (~4.2 eV).[26] The tunable work function provides an excellent band match, leading to a barrier-free contact. The barrier free behaviour is further confirmed using an Arrhenius plot of $\ln(I_d/T^2)$ versus 1000/T, where a Schottky barrier height of zero can be extracted from the slope (Fig. 5-10). Second, compared with conventional metal-MoS_2 systems, our dry-transfer integration strategy does not involve E-beam lithography and metal deposition processes on top of the MoS_2 contact area, which could leave residue and damage the underlying MoS_2. Unlike metals, graphene is highly inert and stable without any diffusion or reaction with MoS_2.[18,27] This non-damaging *van der Waals* bonding approach provides an atomically sharp and ultraclean interface between graphene and MoS_2 to

minimize defects, reduce interface charge trapping states, and prevent Fermi level pinning, which dominate the contact behaviour in conventional metal-MoS_2 systems.[16,18] It should be noted that graphene has been previously used as the contact electrodes on top of MoS_2,[28-31] but typically with an obvious contact barrier likely due to lithography induced residues at the interface and partial screening of the electrical field by MoS_2 (especially thick layers) below the graphene.[32]

We now examine the transfer characteristic of these devices at various temperature. Figure 5-3a shows a temperature dependent transfer curve of a monolayer MoS_2 device. The corresponding temperature dependent sheet conductivity (σ) is plotted in Figure 5-3b, which can provide useful information about metallic or insulating behaviour of the device. Our studies show that conductivity decreases with increasing temperature when $V_g < 50$ V, indicating an insulating behaviour. On the other hand, with larger gate voltages, the conductivity increases with decreasing temperature, suggesting the monolayer MoS_2 enters metallic state with a critical conductivity ~ e^2/h. These observations indicate the presence of a metal−insulator transition (MIT) in the sample, consistent with previous observations in monolayer MoS_2[12,20]. Benefiting from the barrier-free contact, we have observed such MIT in 2-terminal monolayer MoS_2 FETs, which could not be observed in conventional metal-MoS_2 devices, as shown in figure 5-11. In multi-layer MoS_2 devices, similar MIT behaviour is also observed (Fig. 5-3c,d). The difference is that the critical gate voltage required to enter a metallic state decreases to ~20 V, which may be attributed to larger carrier concentration and the smaller band gap in multi-layer MoS_2. We would like to note the two-terminal MIT have been observed in previous report[33], but was only achieved by using high dielectric constant ion-liquid as the gate dielectric to ensure sufficient doping in MoS_2. To the best of our knowledge, the MIT has not been observed in two-terminal devices with normal solid gate dielectrics.

D. Mobility engineering by BN encapulation

With the barrier-free contact, it is possible to approach the optimized device performance limited only by the intrinsic materials properties. To this end, we have evaluated the two-terminal extrinsic FET mobility based on the transconductance using the equation $\mu=[dI_{ds}/dV_{bg}] \times [L/(WC_iV_{ds})]$, where L/W is the ratio between channel length and width (~between 0.5 to 2 in all devices in Figure 5-4) and $C_i = 1.15\times 10^{-8}$ F cm^{-2} is the capacitance between the channel and the back gate per unit area (300 nm thick SiO_2). The back gate capacitance is also confirmed using Hall measurement (Fig. 5-12). To gain further insight into the charge scattering mechanism, we have plotted the field-effect mobility of the monolayer and multi-layer MoS_2 devices as a function of temperature in the logarithmic scale. In both monolayer (Fig. 5-4a) and multilayer (Fig. 5-4d) MoS_2 devices, the mobility values increase with decreasing temperature. In the phonon limited temperature range (100- 300 K), the mobility best fits the expression $\mu \sim T^{-\gamma}$, with the exponent γ around 0.66 to 0.84 for monolayer devices and 1.26 to 1.74 for multi-layers. A power law dependence with a positive exponent is indicative of a phonon scattering mechanism, which is consistent with other materials that show band-like transport such as graphene, Bi_2Te_3 and other layered materials.[34-36] Further decreasing the temperature to 100 - 50 K, the mobility of multilayer devices drops due to impurity scattering, consistent with previous calculations and measurements.[12,19,37] In monolayer device, the mobility is relatively stable in this temperature range, indicating lower impurity density in the monolayer samples.

To further optimize device performance, we have used borne nitride (BN) as the encapsulation layer to minimize the extrinsic environmental scattering effect and probe the mobility-limiting scattering mechanism. BN is integrated into the system using a pickup dry transfer technique to ensure the *van der Waals* stack is free of polymeric residue or any other

impurities.[38] Figures 5-4b, e show the mobility versus temperature plots of the monolayer and multilayer MoS_2 devices encapsulated by a top-BN flake (around 30 to 50 layers). The top-encapsulation of BN would not significant change the gate capacitance, and the field-effect carrier mobility can be derived using the same approach described above. Compared with non-encapsulated device, the multi-layer device shows a similar trend but with a higher γ value (2.12 vs. 1.92) (Fig. 5-4e), approaching the value for bulk MoS_2.[39] On the other hand, the mobility of the monolayer device keeps increasing with decreasing temperature with no apparent saturation (Fig. 5-4b), suggesting that the impurity scattering in monolayers can be largely suppressed using top-BN encapsulation and the phonon scattering dominates at all temperatures in this case. Overall, compared to the devices with no BN encapsulation, the mobility values of the top-encapsulated devices increase by ~110% for monolayer and ~30% for multi-layer MoS_2. The much smaller improvement in multilayer devices can be understood by the existence of the top MoS_2 layer that already functions as a screening layer for extrinsic absorbent scattering sources, resulting in a smaller effect from top-BN encapsulation.

Furthermore, we have used both bottom and top BN encapsulation to create sandwiched devices. With bottom BN encapsulation, the effective gate capacitance will vary and can be obtained by considering the dielectric thicknesses of both the silicon oxide and the underlying BN. The monolayer MoS_2 shows a similar trend with further mobility increasing up to 328 cm^2/Vs (Fig. 5-4c). For the multilayer device, the mobility keeps increasing with decreasing temperature (without saturation or peak around 80 K observed in Fig. 5-4e) (Fig. 5-4f), indicating the quenching of impurities by the bottom BN encapsulation layer. This suggests that the bottom substrate phonon scattering could be an important limitation to thick MoS_2 devices and the mobility can thus be increased up to 650 cm^2/V s by reducing the substrate scattering effect (Fig.

5-4f). The quenching of surface-phonon scattering can also be confirmed by the decreased γ value, which is a strong indication of optical phonon damping. Furthermore, comparing the monolayer devices (Fig. 5-4a-c) with multilayer devices (Fig. 5-4d-f), the exponent γ of the monolayer device measured here is overall considerably lower than that of the multilayer, suggesting different electron-phonon coupling in the monolayer due to a shift of the band valley from Γ–K to K and K′.[39] Lastly, it should be noted such BN/MoS_2/ BN sandwich structure could only be achieved by using a graphene electrode due to its atomic thickness, further highlighting the importance of the graphene contact electrode architecture.

Although the contact barrier is minimized, we note that the contact resistance (including graphene resistance) could still limit the apparent carrier mobility determined from the two-terminal transistor measurements. To further reduce the impact of contact resistance and approach the intrinsic field effect mobility limit, we have fabricated a long channel device with large L/W ratio (35/1.7 µm) using the same BN/MoS_2/graphene/BN sandwich structure (Fig. 5-5a). The MoS_2 here has a thickness of 5 layers. Figures 5-5b, c show the optical image of a long MoS_2 strip after being picked up by a large flake of BN and final device with contact electrodes. The transfer characteristics at different temperatures show that the ON-current increases very rapidly with decreasing temperature and the I_{on} at 1.9 K is 12 times larger than the I_{on} at 300 K (Fig. 5-5d). Compared with a regular device geometry (W/L~1), the much larger temperature modulation $I_{1.9\ K}/I_{300\ K}$ here strongly indicates less contribution from contact resistance in this long channel device. The field effect mobility can be extracted from the transfer characteristics using the same equation mentioned before by considering both the silicon oxide and BN gate dielectrics. Importantly, the temperature dependent measurements show that the two-terminal extrinsic mobility can reach up to 1300 cm^2/Vs at 1.9 K (Fig. 5-5e), which represents, to the best of our knowledge, a record high

extrinsic field effect mobility for MoS_2 determined from two-terminal measurement.

E. Summary

In summary, we have demonstrated for the first time that a barrier-free contact to MoS_2 can be achieved with Ohmic, linear *I-V* output behaviour down to1.9 K, by using graphene contact electrodes with atomically clean interfaces. With the transparent Ohmic contacts, we show a metal-insulator-transition (MIT) can be achieved in two terminal device for both monolayer and multi-layer MoS_2, and demonstrate a record high extrinsic mobility up to 1300 cm^2/Vs. We believe our strategy of using graphene as a tunable contact opens up a new pathway toward contact engineering for 2D semiconductors and other semiconductors in general, and can enable new opportunities for future electronics and low temperature quantum transport in 2D materials.

F. Methods

To fabricate the BN sandwiched devices, the bottom BN, graphene strips (as electrodes), and MoS_2 stripes were first peeled on clean silicon/silicon oxide (300 nm) substrate, while the top BN was peeled on polymer stack PMMA/PPC (polypropylene carbonate) spun on a silicon wafer. The PMMA/PPC/top BN layer was slowly peeled off from substrate under room temperature. This PMMA/PPC/top BN stack was used to pick up MoS_2 and two graphene stripes, sequentially from another substrate. The final PMMA/PPC/top BN/MoS_2/graphene stack were alignment transferred on to bottom BN encapsulation layer. No solvent was involved during the entire transfer process to ensure ultraclean and atomic sharp interface between graphene and MoS_2.

G. References

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H. Figures and Legends

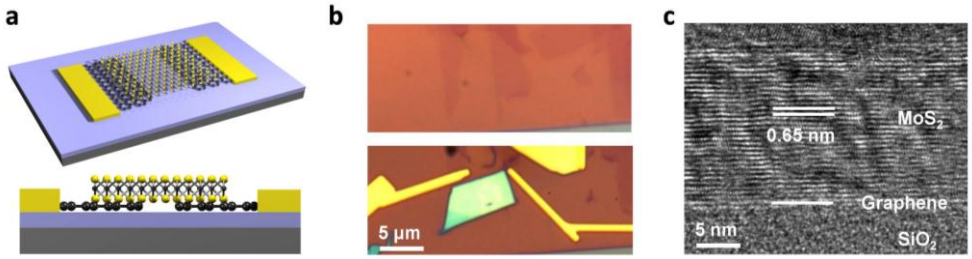

Figure 5-1. Device schematics and characterizations. a, Perspective and cross-sectional schematics of MoS_2 device structure with bottom-graphene electrodes. **b,** Optical image of two graphene strips placed close to each other (top panel) and the final device after MoS_2 transfer and metal electrode deposition (bottom panel). **c,** Cross-sectional TEM image of the graphene-MoS_2 interface, indicating the ultraclean and sharp interface resulted from the dry transfer technique.

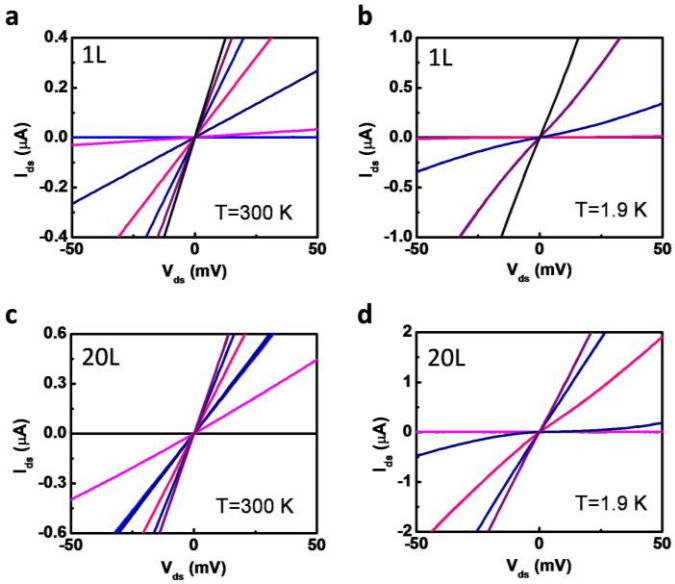

Figure 5-2. Output characteristics of MoS_2 devices contacted by graphene. a, **b**, Output characteristics of a monolayer MoS_2 device at room temperature **a** and low temperature (1.9 K) **b,** at varying gate voltages. Linear *I-V* behaviour is observed in both cases, particularly at high positive gate voltages. Gate voltages range from -60 V to 80 V with a 20 V step. **c**, **d**, Output characteristics of a multilayer MoS_2 device at room temperature (**c**) and low temperature (1.9 K) **d**. Linear *I-V* behaviour is observed in both cases, particularly at high positive gate voltages. Gate voltages range from -60 V to 60 V with a 20 V step.

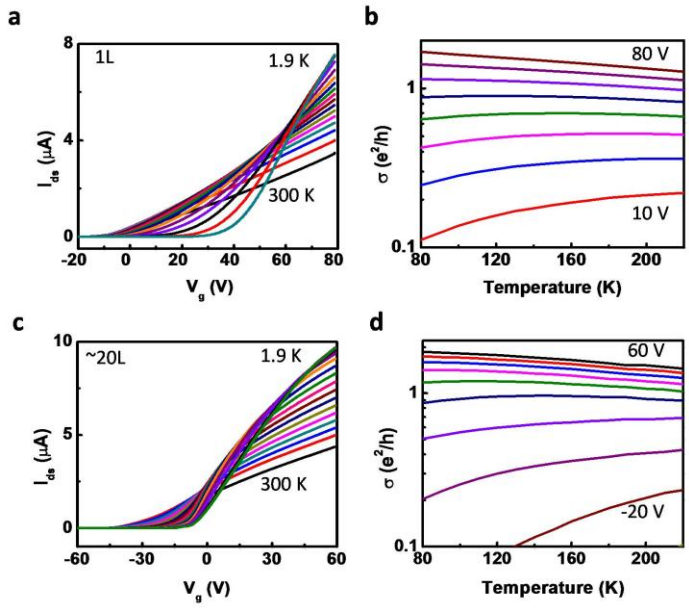

Figure 5-3. Transfer characteristics of MoS_2 devices contacted by graphene. a, Transfer characteristics of a monolayer device**,** at various temperatures (300 K to 1.9 K with 20 K steps). V_{ds} is 100 mV. **b,** The corresponding sheet conductivity of the monolayer device shown in **a** at different gate voltages (10V to 80 V with a 10 V step). **c**, Transfer characteristics of a multilayer MoS_2 device**,** at various temperatures (300 K to 1.9 K with 20 K step). V_{ds} is 100 mV. **d**, The corresponding sheet conductivity of the multilayer device shown in **c** at different gate voltages from -20 V to 60 V with a 10 V step.

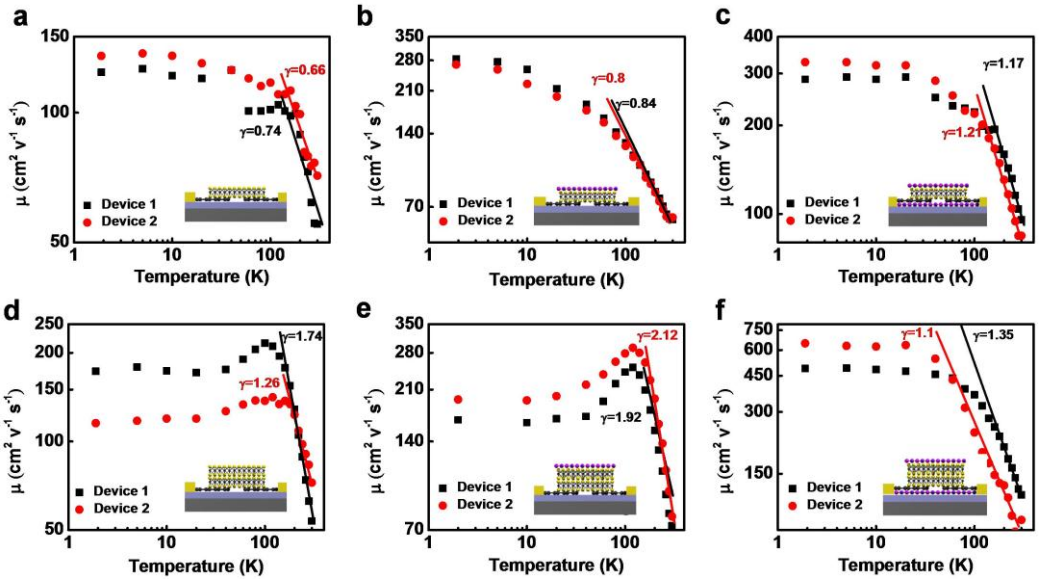

Figure 5-4. Mobility engineering by BN encapsulation. a, **d**, Extrinsic field effect mobility of monolayer and multilayer MoS_2 devices as a function of temperature (300 K to 1.9 K). Linear fitting is used in phonon control region (100 K to 300 K) to extract γ. **b**, **e**, Extrinsic field effect mobility of monolayer and multilayer devices with top BN encapsulation. **c**, **f**, Extrinsic field effect mobility of monolayer and multilayer MoS_2 devices with bottom and top BN encapsulation, forming a sandwich structure.

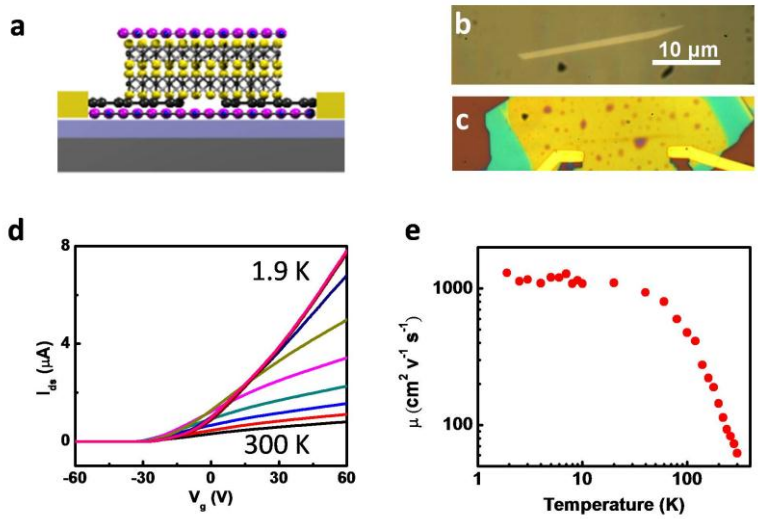

Figure 5-5. Long channel sandwiched device to reduce the impact of contact resistance. a, Schematics of a BN/graphene/MoS_2/ BN sandwich structure with edge graphene contacts. **b**, Optical image of MoS_2 strip picked up by the BN layer. (**c**), Device optical image after device fabrication with edge contacts. **d**, Corresponding transfer characteristics of the device shown in **c**. **e**, Corresponding extrinsic field effect mobility of the device shown in **c** as a function of temperature, with the highest mobility over 1300 cm^2/Vs.

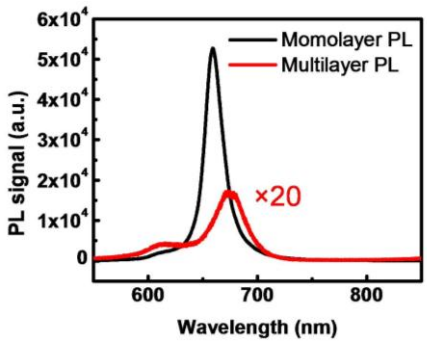

Figure 5-6. Photoluminescence (PL) spectrum of MoS_2. PL data for monolayer MoS_2 (black). Strong luminescence is observed, indicating the existence of direct bandgap. PL data for multilayer MoS_2 (red). Much weaker luminescence is observed due to the indirect bandgap.

Figure 5-7. Schematic illustration of the dry transfer process. The mechanical peeled graphene and MoS_2 have a clean top surface, which are brought together without touching any other foreign materials.

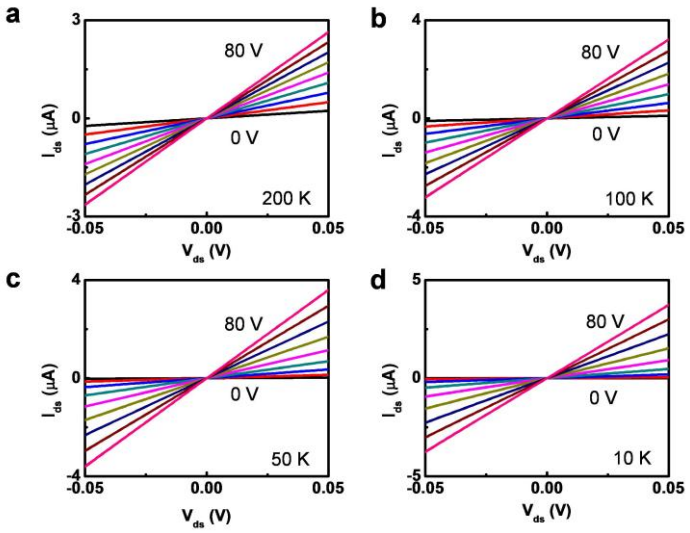

Figure 5-8. Output characteristic (*I-V*) curve of monolayer MoS_2 with graphene contact at various temperature, at different gate voltage (0 V to 80 V, 10 V step), at **a**, 200 K , **b**, 100 K, **c**, 50 K, and **d**, 10 K temperatures.

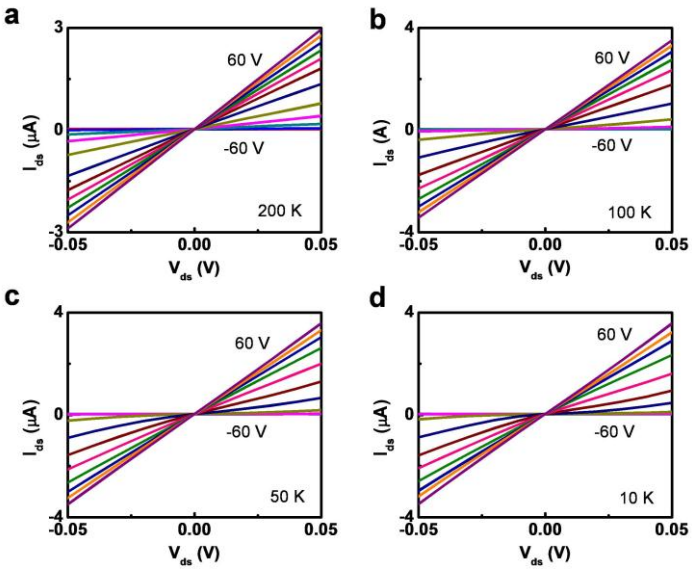

Figure 5-9. Output characteristic (*I-V*) curves of multilayer MoS_2 with graphene contact at different gate voltage (-60 V to 60 V, 10 V step), a, at 200 K, **b**, at 100 K, **c**, at 50 K, and **d**, at 10

K temperatures.

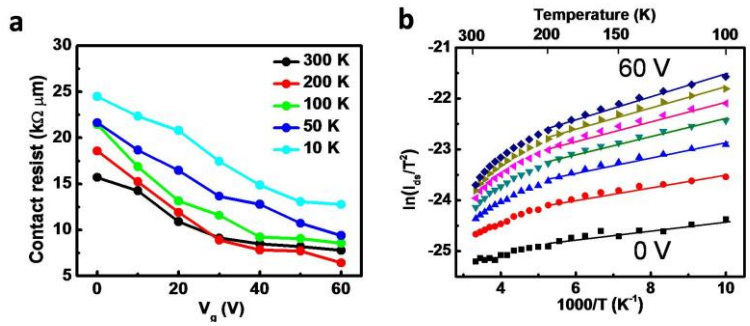

Figure 5-10. Contact resistance, Schottky barrier height of graphene contacted devices. a, Contact resistance of our device versus gate voltages under different temperatures.

b, Arrhenius plot of $\ln(I_d/T^2)$ versus 1000/T for various values of gate voltage from 60 V to 0V. The positive slope here indicates zero measured barrier between graphene and MoS_2.

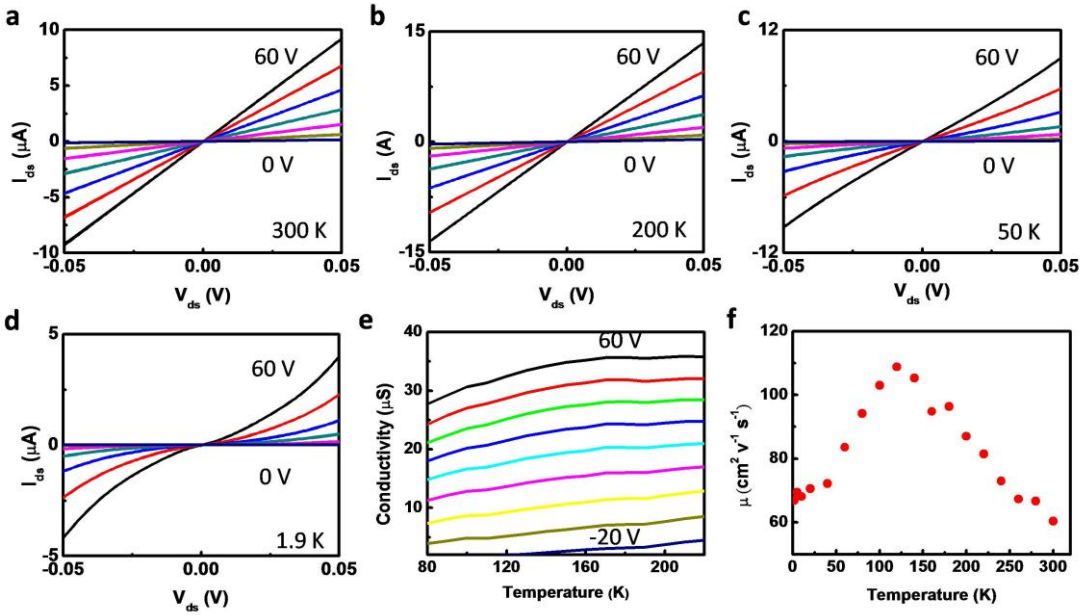

Figure 5-11. Electrical properties of Ni contacted multilayer MoS_2 at various temperatures. *I*-

V curves at different gate voltage (0 V to 60 V, 10 V step) **a**, at 300 K, **b**, at 200 K, **c**, at 50 K, and **d**, at 1.9 K temperatures. **e**, Conductivity versus T at different gate voltage from -20 V to 60 V, 10 V step. At all gate voltage, the conductivity drops with the decreasing temperature, indicating the insulator state at all gate voltage. **f**, Extracted carrier mobility as a function of temperature. The mobility drops significantly with temperature below 100 K, due to the non-ideal Ni contact under low temperature.

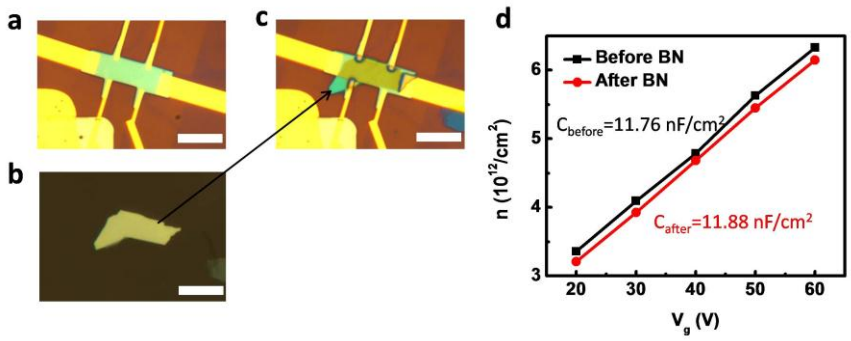

Figure 5-12. Back gate capacitance measurement by Hall effect with/without top BN. a, Optical image of Ni contacted MoS_2 device with Hall bar structure before top BN cover. The MoS_2 is ~20 layers thick. **b**, Optical image of BN flake with thickness ~30 layers. **c**, Optical image Ni contacted MoS_2 device with Hall bar structure after top BN cover (same piece from **b**). **d**, Gate dependent carrier concentration before and after top BN cover. The back gate capacitance could be derived from the slope of the curve. Similar capacitance is obtained with or without the top BN encapsulation. Scale bar is 10 μm in **a**,**b**,**c**.