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Built-in-Self-Test Circuits for Wideband Phased Arrays and Circuits for Millimeter-wave Radiometry and Low-noise Applications

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Tumay Kanar

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor Peter M. Asbeck
Professor James F. Buckwalter
Professor Gert Cauwenberghs
Professor Brian Keating

2015

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Chair

University of California, San Diego

2015

DEDICATION

To my family and to Enver Yücel

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ACKNOWLEDGEMENTS

This dissertation would not have been possible without the help and support of many people. First and foremost, I would like to thank my advisor, Prof. Gabriel Rebeiz. His dedication and support over the past five years have been the main motivation for all my accomplishments. Without his guidance, I would not be where I am today. I have learnt a lot from him in both technical and personal aspects. I feel truly privileged to be trained by him, and I still have many things to learn from him.

Next, I would like to thank my dissertation committee members, Prof. Peter M. Asbeck, Prof. James F. Buckwalter, Prof. Gert Cauwenberghs and Prof. Brian Keating for their time, interest, and valuable comments about my research. I also would like to thank my co-author, Samet Zihir, for all his hard-work and dedication. He has provided me the wide-band channel as the DUT for my built-in self-test system, and in overall, he has always been helpful whenever I needed.

I'd like to thank my parents, Nihal and Ersin, for their support, encouragement and never-ending love. They have always found a way to make the most difficult moments much easier for me. Their love kept me going when everything else failed, and I know that they will be there whenever I need them in my life. Also, I would like to thank my grand-parents Gulser and Yusuf for all their love and support. I have spent the most beautiful days of my childhood with them, and their love always made me stronger. I'd also like to thank my beautiful sister, Miray. She was always there for me with her love and support. She was my legal guardian when I first went to a boarding school, and I know that she will be there whenever I need her. She also brought two beautiful people to our family: My brother-in-law, Onursal, and my little nephew Artun. I would like to thank my brother for his sincere love and all the fun times whenever I went back to Turkey. Also, I would like to thank my little Artun for all the joy that he brought to our lives. Finally, I would like to especially thank my sweetheart, Aslihan, for all her love

and support. She always achieved to make me smile even at the hardest times. I have learnt many things over my PhD years but, she taught me the true love.

I'd like to extend my special thanks to Ozgur Inac. I have learnt a lot from him, and his support during the first years of my PhD has been invaluable to me. There are many other San Diego friends that I need to thank for their friendship: Furkan and Ozan for being awesome housemates, Bilgehan and Fatih for being my gym buddies (and partners-in-crime), Mehmet and Berke for being my "go-to" people, Ken and Yang for being my comrades in tapeout misery, Kerim and Umut for being the fresh blood in the group, and finally, Mustafa for all the coffee hours (i.e., deep conversations) and his selfless support whenever I needed. I also would like to thank all the members of TICS group for their support and friendship.

Lastly, I would like to thank Enver Yücel for his trust in me and his never-ending support. He has been a godfather to me throughout the years, and he always motivated me to do better and made me who I am today. I know that he will be there whenever I need him, and I will always try my best to make him proud.

The material in this dissertation is based on the following papers which are either published, or has been submitted for publication.

Chapter 2 is based on and mostly a reprint of the following paper:

- T. Kanar, S. Zihir, and G. M. Rebeiz, "A 2-15 GHz Accurate Built-in Self-Test Circuit for Wide-band Phased Arrays Using Self-Correcting 8-State I/Q Mixers," *IEEE Transactions on Microwave Theory and Techniques*, submitted for publication, November 2015.

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Chapter 4 is based on and mostly a reprint of the following paper:

- T. Kanar and G. M. Rebeiz, "X-and K-Band SiGe HBT LNAs with 1.2-and 2.2-dB Mean Noise Figures," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 10, pp. 2381-2389, October 2014.

Appendix is based on and mostly a reprint of the following paper:

- T. Kanar and G. M. Rebeiz, "A 16-24 GHz CMOS SOI LNA with 2.2 dB mean noise figure," *IEEE Compound Semiconductor Integrated Circuits Symp.*, October 2013, pp. 1-4.

The dissertation author was the primary author of the work in these chapters, and coauthors (Prof. Gabriel M. Rebeiz, Dr. Samet Zihir) have approved the use of the material for this dissertation.

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T. Kanar and G. M. Rebeiz, "A 2-15 GHz VCO with Harmonic Cancellation for Wideband Systems," *IEEE Microwave and Wireless Component Letters*, submitted for publication, July 2015.

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O. Inac, F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90-100 GHz phased-array transmit/receive silicon RFIC module with built-in self-test," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 10, pp. 3774-3782, October 2013.

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ABSTRACT OF THE DISSERTATION

Built-in-Self-Test Circuits for Wideband Phased Arrays and Circuits for Millimeter-wave Radiometry and Low-noise Applications

by

Tumay Kanar

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2015

Professor Gabriel M. Rebeiz, Chair

The thesis presents wide-band built-in self-test circuits (BIST) for phased array systems and high performance circuits for millimeter-wave radiometry and low-noise applications. The 2-15 GHz BIST is designed using a resistive wide-band coupler at the input of each channel and an on-chip oscillator is employed for the test signal and local oscillator generation. An on-chip 8-phase self-correcting I/Q vector receiver and algorithm are introduced for wide-band accuracy. Using the I/Q outputs from 8 different LO phases for one-time calibration, the DC offset, gain and phase imbalance for the system can be determined at each frequency point and eliminated. The BIST can be

done at a rate of 1 MHz with greater than 50 dB signal-to-noise-ratio (SNR) and allows for accurate characterization of the phased array by providing relative gain and phase measurements over a wide frequency range. The BIST results agree well with the VNA measurements, and the 2-15 GHz BIST can determine the channel's relative phase and gain error with $\pm 3^{\circ}$ and $\pm$ 0.3 dB accuracy, respectively. An RMS detector network is also implemented for absolute gain measurements, and the absolute gain is measured using a pair of detectors located at the input and the output ports. The BIST can measure the absolute gain with $\pm$0.5 dB accuracy at 2-15 GHz, and this feature can be employed to detect under-performing units in the field for self-healing mechanisms.

Next, a D-band radiometer centered at 136 GHz is presented. The radiometer is realized with a 35 dB gain low-noise amplifier and a detector in the IBM 90 nm SiGe BiCMOS process. The on-chip radiometer results in a measured minimum NEP of 1.4 fW/Hz$^{1/2}$ and a peak responsivity of 52 MV/W. With a low 1/f corner frequency ($<$100 Hz) and a noise bandwidth $>$10 GHz, this system is suitable for high-resolution imaging applications. For an integration time of 3.125 mS, the minimum noise equivalent temperature difference (NETD) is measured to be 0.25K using different independent methods and is the lowest NETD demonstrated in silicon technologies at D-band frequencies.

Finally, X- and K-band low-noise amplifiers (LNA) in a 0.18 µm SiGe BiCMOS process are presented with measured mean noise figure of 1.2 dB and 2.2 dB, respectively. A method of noise match optimization with respect to base inductance in SiGe LNA design with large transistors is proposed and explained in detail. The LNAs result in peak gain of 24.2 and 19 dB at 8.5 and 19.5 GHz and IIP_3 of -11 and -4 dBm at 10 and 20 GHz, respectively. To the authors' best knowledge, these results outperform all available CMOS designs and achieve the lowest mean noise figure at X- and K-bands in any SiGe or CMOS process at the time of publication. Another K-band LNA is also implemented in 45 nm IBM CMOS SOI process and results in 2.2 dB mean noise figure with 19 dB

peak gain. The details of this design are presented in the appendix.

Chapter 1

Introduction

1.1 Wide-Band Built-in Self-Test Systems for Phased Arrays

Phased arrays have been traditionally used for defense radar and communication systems since the 1970s and have been recently implemented for commercial automotive radars as well [3–5]. The emerging technologies in communications will require directive high-bandwidth links, and the phased arrays are going to be at the heart of high-speed point-to-point and last mile communication systems as well as the more advanced defense applications [6, 7].

The integration of phased-array core chips in silicon technologies allows low-cost and multi-functional phased array systems and has been demonstrated in SiGe and CMOS technologies [8, 9]. The new phased-array chips enable the implementation of very large phased arrays for defense systems as well as the use of small-size and low-power phased arrays for mobile communications. The built-in self-test (BIST) feature for phased arrays is an essential feature since it provides fast, accurate, and low-cost calibration for large systems and in-situ calibration and self-healing opportunities for the small arrays [10–13].

A new generation of wide-band phased arrays will be designed in order to meet the need for multi-functionality and high bandwidth requirements of emerging technologies [14,15]. These systems will be required to maintain their performance for robust links and should be able to re-calibrate themselves in the field. Therefore, the compact wide-band BIST circuits will be an indispensable part of such systems and allow more complex, robust and efficient phased array implementations by facilitating the array characterization and calibration at virtually no additional cost. In this thesis, a wide-band BIST technique and a self-correction algorithm for wide-band BIST measurements are proposed, and the wide-band on-chip testing challenges and design trade-offs are analyzed in detail. A wide-band BIST implementation at 2-15 GHz is presented for demonstration.

1.2 Millimeter-Wave Radiometry and Low Noise Applications

D-band (110 - 170 GHz) is an attractive frequency range for various imaging and monitoring applications [16–21]. Operating at a low atmospheric attenuation windows, D-band radiation can propagate through large obstacles such as fog, dust and clothes, and this makes it especially appealing for low-visibility navigation and concealed weapon detection systems. D-band also offers a better spatial resolution than W-band systems and allows for more compact systems due to its smaller wavelengths. Implementation of such systems in silicon technologies has been an active research area but most systems were demonstrated at W-band frequencies. [22, 23]. This thesis presents a SiGe D-band total power radiometer centered at 136 GHz with a thermal resolution (NETD) of 0.25K at 3.125 ms integration time. The design optimization and accurate measurement and characterization techniques are discussed in detail.

1.3 Thesis Overview

The thesis presents built-in self-test (BIST) circuits for wide-band phased array systems, and high performance circuits for millimeter-wave radiometry and low-noise applications.

Chapter 2 presents a 2-15 GHz BIST system that can perform relative phase measurements and relative and absolute gain measurements to detect under-performing channels in large phased-arrays. The design challenges and trade-offs of wide-band BIST technique are discussed in detail, and a self-correcting algorithm using a multi-phase local oscillator (LO) for the I/Q mixers is introduced. The BIST measurements agree well with the VNA S-parameter measurements over the operation bandwidth. The BIST has enough signal-to-noise ratio to execute measurements at 1 MHz.

Chapter 3 presents a D-band radiometer centered at 136 GHz for low atmospheric attenuation. The radiometer results in a measured minimum NEP of 1.4 fW/Hz$^{1/2}$ and a peak responsivity of 52 MV/W. The radiometer's thermal resolution (NETD) is measured to be 0.25K and confirmed with several independent methods. This presents the state-of-the-art performance for silicon technologies.

Chapter 4 presents X- and K-band low-noise amplifiers (LNA) with 1.2 dB and 2.2 dB mean noise figure. A method of noise optimization for large size SiGe transistors with respect to on-chip inductor loss is proposed. Both LNAs demonstrated the record performance at the time of publication.

The thesis concludes with a summary of the work and suggestions for future work.

Chapter 2

A 2-15 GHz Accurate Built-in-Self-Test Circuit for Wide-band Phased Arrays Using Self-Correcting 8-State I/Q Mixers

2.1 Introduction

Phased arrays are essential for low power and high data-rate communication systems since they allow for directive communications. The antenna beams need to be scanned in space and a typical system employs 8-256 channels, each containing phase shifters and variable gain amplifiers. Published phased array systems are relatively narrow-band [24–28], but a new generation of wide-band phased-arrays are being designed for emerging technologies such as 5G, IoT, and various defense applications. The test and calibration of phased arrays constitutes a significant portion of the system cost for the systems containing a large number of elements. BIST systems are essential for

lowering the phased-array cost since they would eliminate the use of external vector network analyzers (VNA) for measuring the gain and phase of every channel [10–12]. BIST circuits can also determine if a channel is under-performing, and can trigger real-time self-healing algorithms for optimal link performance [13].

The I/Q downconverter architecture has proven to be an effective method for RF and millimeter-wave BIST systems for relatively narrow-band applications [29]. The wide-band BIST implementation introduces additional challenges, such as on-chip harmonically-clean wide-band test signal generation, wide-band coupling for BIST signal injection and sampling, and also, I/Q error compensation throughout the entire bandwidth. Also, keeping the dynamic range and accuracy levels can be challenging for wide bandwidth BIST systems as the signal levels can change significantly due to the differences in coupling loss and gain over the frequency range. Therefore, wide-band BIST systems need to inherently self-correct for accurate measurements.

This chapter introduces a wide-band BIST system with an on-chip ring oscillator that covers 2-15 GHz operation. The BIST consists of a part for relative phase & gain measurements and another part for absolute gain measurements. The BIST section for relative phase and gain measurements employs 8-phase I/Q mixers with a self-correcting algorithm for I/Q errors, such as DC offset, gain and phase imbalance. The multi-phase LO is provided using a four-stage ring voltage controlled oscillator (VCO) and LO selection network. The same VCO also provides the harmonically-clean test signal for the phased array channels using a weighted summer for the cancellation of higher harmonics. The BIST section for absolute gain measurements consists of an RMS power detection network and can provide absolute gain measurements for each channel at 2-15 GHz.

The chapter is organized as follows. Section II introduces the wide-band BIST receiver errors and explains the multi-phase LO self-correction method. Section III

presents the BIST architecture and the circuit implementations for wide-band operation. Section IV overviews the wide-band phased array channel used as the DUT. Section V presents the measurements for the BIST circuit and compares the BIST obtained data with VNA measurements. Finally, section VI summarizes the results with a conclusion.

2.2 Built-in-Self-Test Receiver Errors and Multi-phase Correction Algorithm

2.2.1 Wideband BIST Receiver Errors

The BIST system relies on a homodyne I/Q down-converter which measures the signal after it passes by the phased-array channel (Fig. 2.1). In this topology, the channel gain and phase are obtained from the I and Q data as $G = \sqrt{(I^2 + Q^2)}, \quad \phi = tan^{-1}(Q/I)$. Therefore, any error in the I/Q receiver, such as phase or amplitude imbalance or DC offsets, will directly affect the accuracy of the BIST system, and de-embedding of these errors is hard for wide-band systems as their effects differ over bandwidth. Therefore, a frequency independent I/Q error model should be developed. In this error model, we consider three major I/Q receiver errors, namely, DC offset, gain imbalance, and phase skew. As shown in Fig. 2.1, the I and Q path gains are labeled as G_I and G_Q and the phase imbalance between the I and Q paths is considered to be symmetrical and labeled as α. The phase skew (imbalance) between the I and Q channels is relative and the symmetry can be assumed without the loss of generality. The DC offset results in a shifted origin for the I and Q vectors in Fig. 2.1 and will be labeled as E_I and E_Q, respectively [30].

Fig. 2.2 presents an overview of the correction algorithm presented in this chapter. In each correction step, V_n is a sample output vector, which is the combination of I and Q DC readings. The raw DC readings has a shifted origin due to the DC offsets, unequal

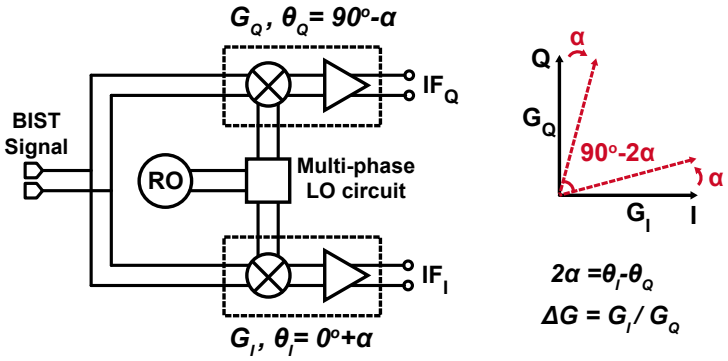


Figure 2.1: Frequency independent error model for I/Q receiver for relative phase and gain measurements.

Table 2.1: I/Q Error Modeling with Multiple LO States

LO_{st}	LO_I	LO_Q	V_I	V_Q
LO_1	0°	90°	$G_I[cos(\phi)cos(\theta+\alpha)]+E_I$	$G_Q[-cos(\phi)sin(\theta-\alpha)]+E_Q$
LO_2	45°	135°	$G_I[cos(\phi)cos(\theta+\alpha+45)]+E_I$	$G_Q[-cos(\phi)sin(\theta+45-\alpha)]+E_Q$
LO_3	90°	180°	$G_I[-cos(\phi)sin(\theta+\alpha)]+E_I$	$G_Q[-cos(\phi)cos(\theta-\alpha)]+E_Q$
LO_4	135°	-135°	$G_I[-cos(\phi)sin(\theta+\alpha+45)]+E_I$	$G_Q[-cos(\phi)cos(\theta+45-\alpha)]+E_Q$
LO_5	180°	-90°	$G_I[-cos(\phi)cos(\theta+\alpha)]+E_I$	$G_Q[cos(\phi)sin(\theta-\alpha)]+E_Q$
LO_6	-135°	-45°	$G_I[-cos(\phi)cos(\theta+\alpha+45)]+E_I$	$G_Q[cos(\phi)sin(\theta+45-\alpha)]+E_Q$
LO_7	-90°	0°	$G_I[cos(\phi)sin(\theta+\alpha)]+E_I$	$G_Q[cos(\phi)cos(\theta-\alpha)]+E_Q$
LO_8	-45°	45	$G_I[cos(\phi)sin(\theta+\alpha+45)]+E_I$	$G_Q[cos(\phi)cos(\theta+45-\alpha)]+E_Q$

magnitudes due to gain imbalance and a rotational skew due to the phase imbalance. These errors are corrected step by step using the self-correction algorithm described below.

2.2.2 Multi-phase Correction Algorithm

Table 2.1 presents the time-independent V_I and V_Q DC voltages for 8 different phases of LO signal shown in Fig. 2.1. Note that DC voltages are considered since the BIST system is based on a homodyne mixing technique. Also, the LO phases are taken to be 90° apart ensuring an "I" and "Q" response. A sequential method is used to extract the error terms and eliminate them from the DC readings. The correction algorithm starts with DC offset cancellation for which two outputs with LO_n and LO_{n+4} (where n = 1,2,3,4) are used to calculate E_I and E_Q as:

$$E_I = \sqrt{\frac{I_n + I_{n+4}}{2}}, \quad E_Q = \sqrt{\frac{Q_n + I_{n+4}}{2}} \tag{2.1}$$

The DC offset is eliminated from the I and Q outputs by simply subtracting E_I and E_Q from the voltage readings. After the DC offset are de-embedded using the 8 LO phases (only two LO phased are required, but 8 are used for added accuracy), the de-embedded outputs for LO_n and LO_{n+2} are then used for gain imbalance calculation as:

$$G_{I/Q} = \sqrt{\frac{I_n'^2 + I_{n+2}'^2}{Q_n'^2 + Q_{n+2}'^2}} \tag{2.2}$$

where I_n' and Q_n' are the DC offset de-embedded outputs. Since the gain imbalance is also relative between the I and Q paths, it can be corrected on either of them by scaling the output for the corresponding path. After the gain imbalance correction, the outputs I_n'' and Q_n'' are then used in order to determine the phase skew between the I and Q paths. It

should be noted that the phase imbalance is mainly due to the path length differences and component mismatches. Using the outputs for LO_n and LO_{n+1}, the phase imbalance is calculated as:

$$\alpha = tan^{-1}\left(\frac{\sqrt{2}I''_{n+1} - I''_n + Q''_n}{\sqrt{2}Q''_{n+1} - Q''_n + I''_n}\right) \tag{2.3}$$

where I''_n and Q''_n are both DC offset and gain imbalance de-embedded outputs. The phase imbalance is eliminated by multiplying the outputs I''_n and Q''_n by $\sec(\alpha)$. The final I and Q voltages are now compensated from DC offset, gain and phase imbalance, and can be used to calculate the relative gain and phase measurements for the phased array channels. This algorithm can theoretically be employed using only a quadrature LO source ($LO_{1,3,5,7}$) but the algorithm may result in a $tan(0°)$ or $tan(90°)$ at certain frequencies, leading to very small or large values, and large de-embedding errors. Therefore, the use of 45° LO states ($LO_{2,4,6,8}$) is essential since they ensure that I/Q data is available around $tan(45°)$ and results in high accuracy over a wide-band frequency range.

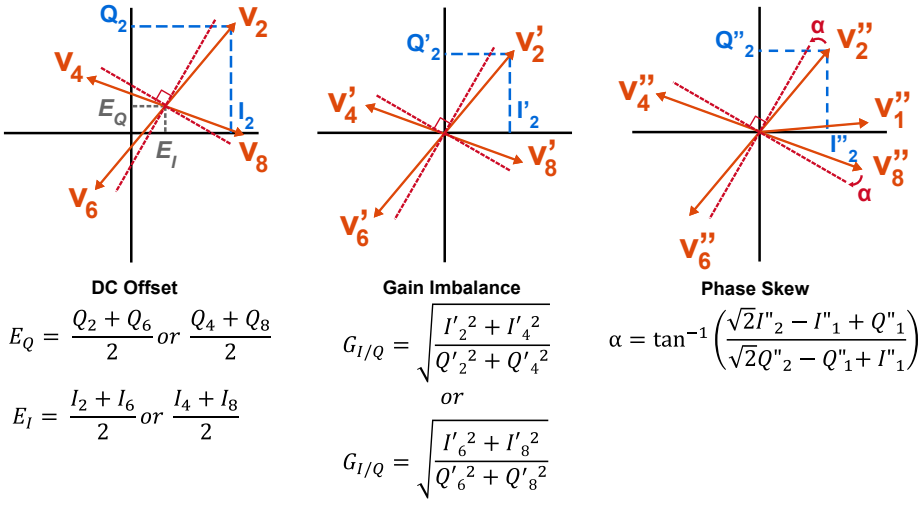


Figure 2.2: Outline of multi-phase correction algorithm explained for DC offset, gain imbalance, and phase imbalance with sample test vectors.

The correction algorithm is based on two assumptions. First, it is assumed that the four-stage ring oscillator outputs are approximately 45° apart, and second, the phase difference due to the LO selection switch network is low. If the LO phases are not exactly 45° (or 90°) apart, then the LO phase imbalance will a part of the I/Q phase skew, and will be automatically corrected.

The correction algorithm is a one-time procedure done at each frequency point, and once the error terms are determined, only one I and Q reading using a single LO phase state is needed for the BIST measurements. Therefore, after the initial corrections, this algorithm does not introduce a measurement time overhead.

2.3 BIST Implementation at 2-15 GHz

The BIST architecture is presented in Fig. 2.3. A two channel phased-array is used for test purposes (DUT), but the channels can be scaled to 8-256 in full systems. The wide-band BIST is based on a direct-conversion receiver with the on-chip oscillator providing both the test and the LO signals. The test signal is injected to and sampled from the phased array channels using the resistive couplers for wide-band and non-invasive coupling and down-converted to DC outputs by the I/Q mixers. The DC outputs are processed off-chip using a Matlab routine for demonstration, but they can also be processed on-chip in the future for feedback-controlled self-healing features.

The chip including the BIST system with multi-phase correction feature and two phased array channels as DUT is implemented in the 0.18 μm Jazz SiGe BiCMOS SBCH3 process with f_t/f_{max} of 240/260 GHz (Fig. 2.4). The total chip area is 1710x2010 μm^2, and the BIST core occupies 1350x610 μm^2. The BIST distribution networks are implemented on the top metal layer for demonstration purposes, and the BIST area can be decreased further by using lower metal layers and more compact distribution networks.

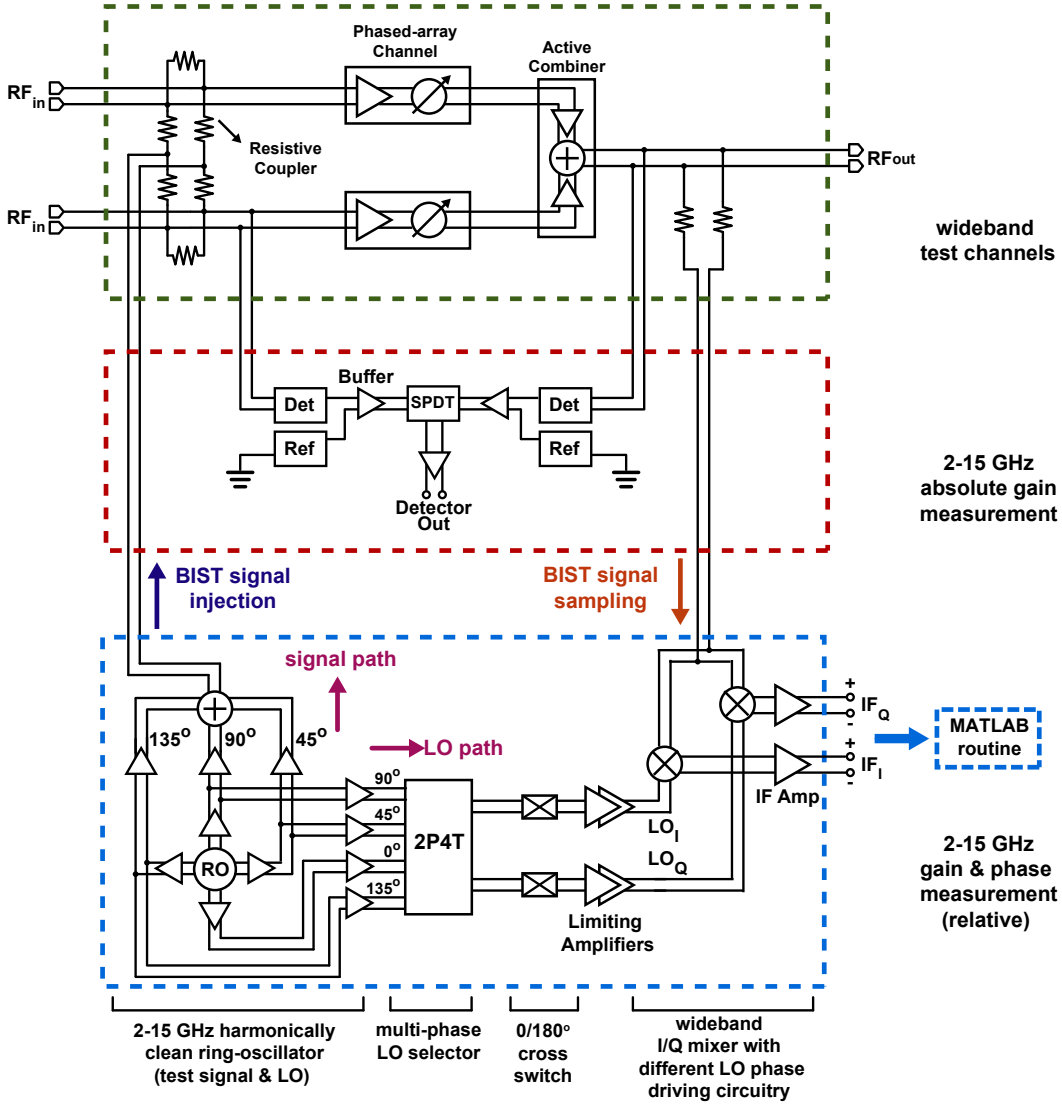


Figure 2.3: Overall BIST architecture including the circuitry for absolute gain (rms power detectors) and relative gain & phase measurement (wideband I/Q mixer with mullti-phase LO selector).

The BIST system consumes 110-123 mA from 2.5 V for different oscillator frequencies, but is only turned on for a short time for testing.

2.3.1 On-Chip Wideband Signal Generation and Multi-phase LO Distribution

The wide-band test signal generation introduces several challenges [31]. To sustain a large dynamic range over the entire bandwidth, the BIST signal injection should be kept around the same amplitude and the upper harmonics which fall in the operating bandwidth should be avoided. In order to achieve this, a four-stage differential voltage-controlled ring oscillator is used to provide the BIST test signal and the LO generator for the I/Q receiver [32].

The architecture for the ring VCO together with the harmonic-cancellation method are presented in Fig. 2.5. The ring oscillator employs 4 delay cells and consumes a total of 4.4-17 mA for 2-15 GHz operation. The delay unit-cell for the ring oscillator with ECL differential pair and emitter followers is presented in Fig. 2.6(a). The VCO is designed without any inductors in order to result in a compact design.

For a ring oscillator with n stages, the oscillation frequency is determined by the two poles at the V_{out} and V_a nodes and is given by [33]:

$$\omega_o = -\frac{\omega_{p1}+\omega_{p2}}{2k} + \frac{1}{2}\sqrt{\left(\frac{\omega_{p1}+\omega_{p2}}{k}\right)^2 + 4\omega_{p1}\omega_{p2}} \tag{2.4}$$

where $k = tan\left(\frac{\pi}{n}\right)$. For a four-stage oscillator, the widest tuning range is achieved when the V_{out} pole is set to be dominant. Frequency tuning is realized by controlling the current in the emitter follower, which shifts the V_{out} pole depending on the corresponding Q2 g_m value. For a tuning range of 2-15 GHz, the Q2 g_m is changed from $\sim$0.25 mS to $\sim$65 mS for a current of 0.1- 1.7 mA in M2.

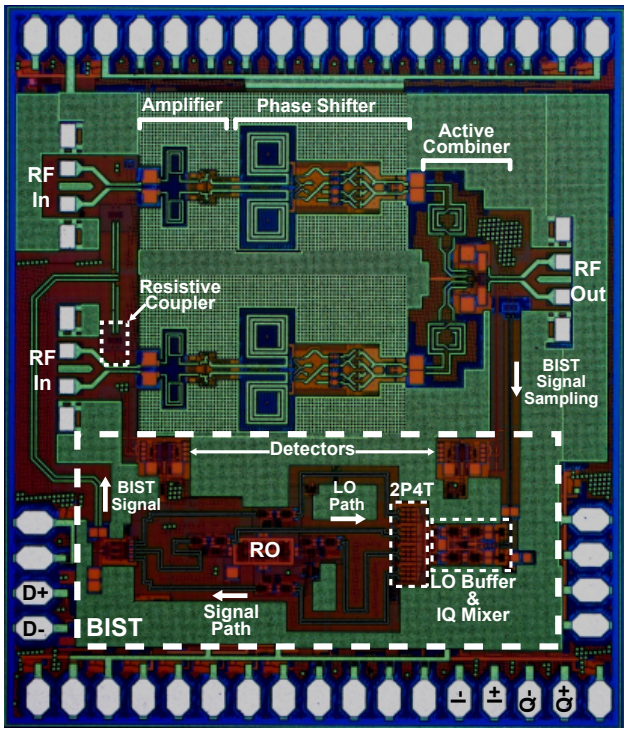


Figure 2.4: Chip micrograph for BIST system with two phased-array channels.

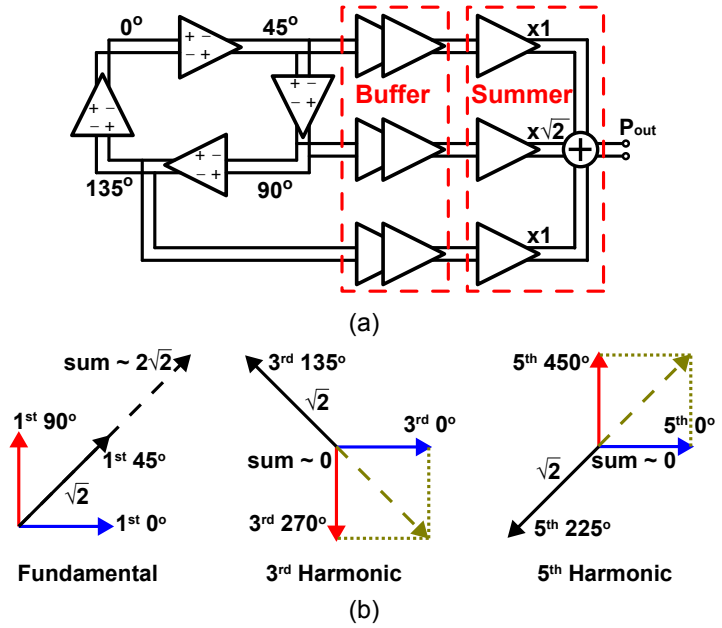


Figure 2.5: Harmonic-cancellation architecture based on a multiple phase ring oscillator for test signal generation.

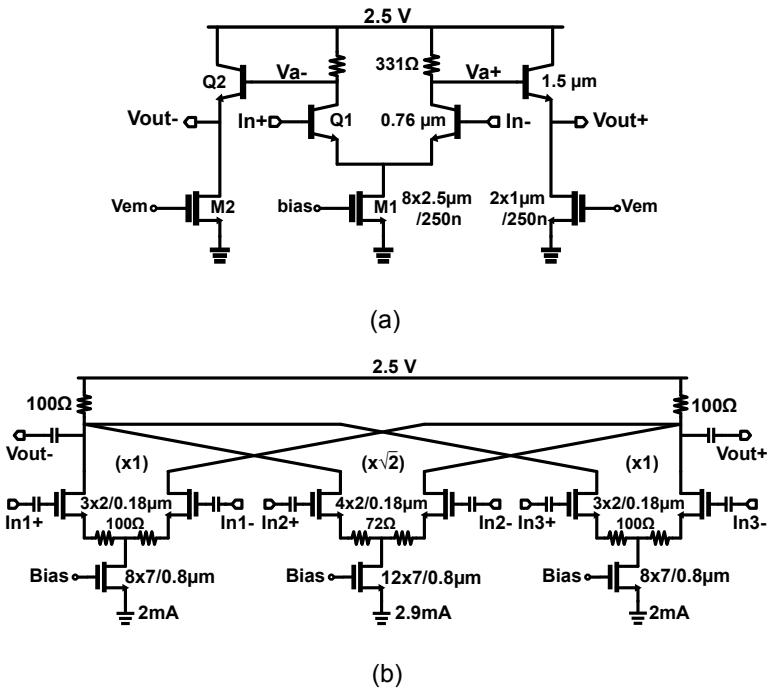


Figure 2.6: (a) Ring VCO differential delay cell (4 units used), (b) weighted active current combiner schematic.

The ring VCO's three outputs, which are 45° apart, are summed with a $\sqrt{2}$ weighted summer in order to eliminate the 3rd and 5th harmonics [34, 35]. The 45^o, 90^o and 135^o outputs are followed by two wide-band resistively-loaded buffer stages with a voltage gain of 12-2 dB at 2-15 GHz and then fed into a 0.18 μm CMOS active summer (Fig. 2.6(b)). In order to obtain a wide-band weighting of $\sqrt{2}$, different transistor sizes and bias currents are chosen for the x1 and x$\sqrt{2}$ paths, along with weighted emitter degeneration. The voltage gain of the branches is kept constant over a wide frequency by the proper choice of DC blocking capacitors at the summer input and the output ports. The gain difference is actually 2.57 dB instead of 3.0 dB and is optimized using Cadence for the best harmonic cancellation performance. The differential summer output impedance is 200 Ω at 2 GHz and drops to 118 Ω at 15 GHz due to the transistor loading capacitance.

The harmonically cancelled BIST signal maintains an output power of -9$\pm$1 dBm at 2-15 GHz (Fig. 2.7), and cancels the upper harmonic levels to below -50 dBc for the entire frequency range.

Fig. 2.8(a) presents the spectrum of a single output for the ring-oscillator at 2.84 GHz, and the high harmonic levels are clearly seen. Note that due to the wideband nature of the measurement system, single-ended measurements are done and therefore, the 2^{nd} harmonic content is present, but this cancels out in a differential system. The output spectrum after the weighted summer is shown in Fig. 2.8(b), and the 3^{rd} harmonic level is $<$-40 dBc (2^{nd} harmonic is again due to the single-ended measurements).

Table 2.2 presents detailed measurements for the 3^{rd} and 5^{th} harmonic levels. The harmonic-cancellation technique lowers the 3^{rd} and 5^{th} harmonic levels by $>$30 dB as compared to a non-weighted output over a wide frequency range. The dynamic range of the harmonic level measurements is limited by the jitter characteristics of the free-running VCO. Frequency drift due to the jitter sets a relatively high minimum value

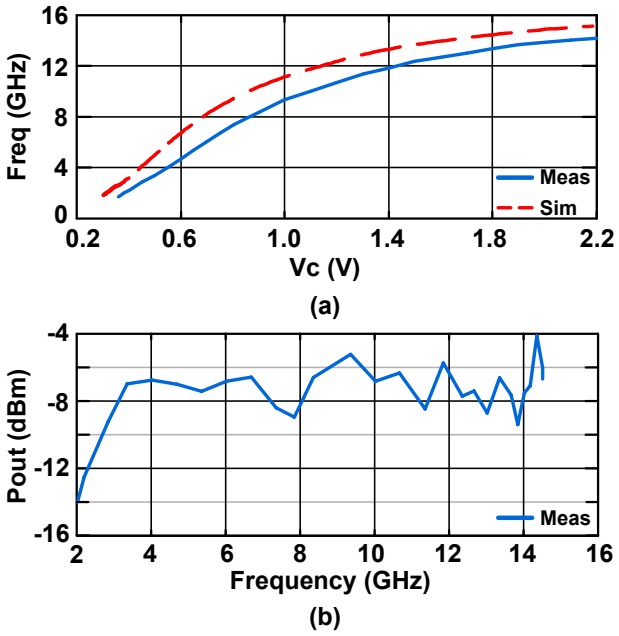


Figure 2.7: (a) Measured and simulated output frequency, and (b) power level.

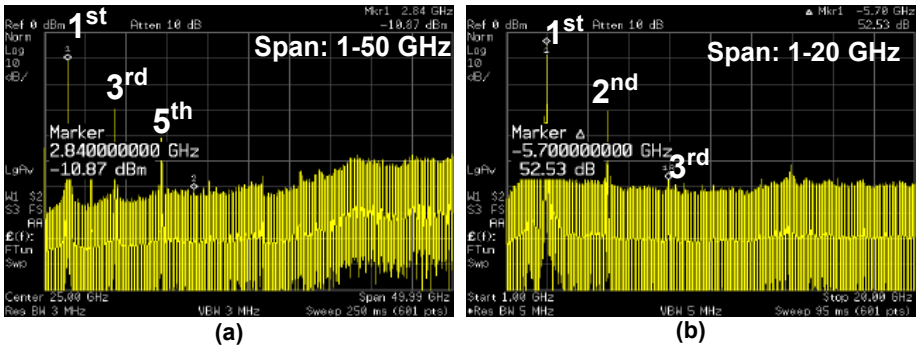


Figure 2.8: Spectra for: (a) Single-phase output without harmonic cancellation at 2.84 GHz, and (b) 2.84 GHz signal showing 3^{rd} harmonic suppression at 8.52 GHz.

Table 2.2: VCO Measured Output Harmonic Content

	Harm. Cancelled		Single VCO Out	
Fund. Freq. (GHz)	3^{rd} Harm. (dBc)	5^{th} Harm. (dBc)	3^{rd} Harm. (dBc)	5^{th} Harm. (dBc)
2.84	-52.3	n.d.	-18.1	-30.3
3.42	-57.9	n.d.	-14.0	-30.2
4.11	-58.6	n.d.	-15.3	-32.7
4.83	-53.7	n.d.	-17.0	-33.9
6.68	<-60	n.d.	-21.9	-39.3
8.34	<-60	n.d.	-21.2	-38.4
10.67	<-60	n.d.	-23.0	o.r.
n.d.: not detectable, o.r.: out-of-range				

Table 2.3: VCO Phase Noise and Power Performance Summary & Comparison

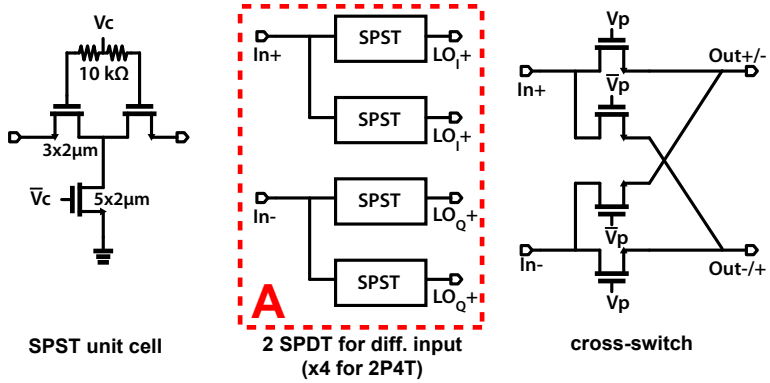
	Freq. (GHz)	Out. Pow. (dBm)	Pow. Cons. (mW)	Phase Noise (dBc)
This work	**2-15**	**-6 to -8**	**88-120**	**-112 (10 MHz)**
[36] (SiGe)	8-17	-15	115	-
[37] (InP)	14-22	-4	130	-90 (1 MHz)
[38] (CMOS)	3-11	-1	-	-110 (10 MHz)
[39] (SiGe)	5-9	-9 to -14	40-94	-70 (1 MHz)

for the resolution bandwidth, and it increases the noise floor of the spectrum analyzer.

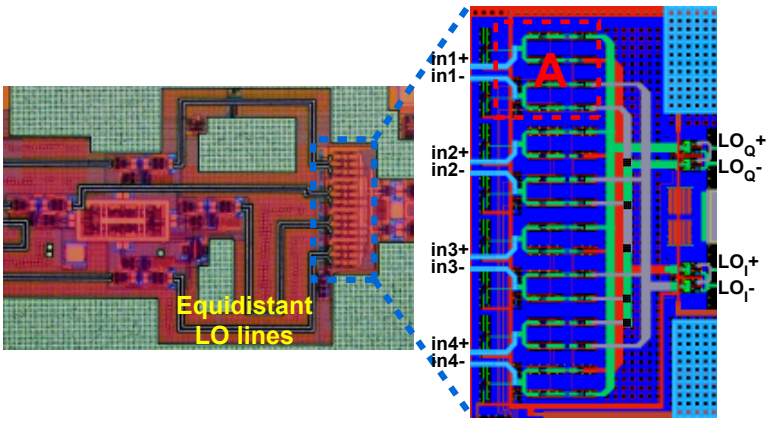
The harmonically cancelled output retains the upper harmonic levels below -50 dBc for the whole frequency range and has a measured phase noise of around -110 dBc at 10 MHz offset. The ring-based VCO results in a relatively high phase noise, but is adequate for built-in-self-test systems. The phase noise is comparable to, if not better than, published work (Table 2.3).

The ring VCO provides both the test and LO signals for the BIST system as previously shown in Fig. 2.3. Since the BIST is based on a sef-mixing homodyne approach, the phase noise is suppressed at base-band by the cancellation due to self-mixing and does not affect the measurement dynamic range [40, 41].

The ring oscillator generates 4 differential LO phase states, and a multi-phase



(a)



(b)

Figure 2.9: (a) Schematics for the switch network components for multi-phase LO selection, (b) layout of LO distribution network and 2P4T switch.

(8-state) LO selector is required to feed the I/Q mixers (Fig. 2.9(a)). The unit switch-cell is implemented in differential series-shunt-series configuration for high isolation between the different LO paths, and are integrated together to form a 2P4T switch network. This 2P4T switch selects two of the four oscillator outputs as LO_I and LO_Q, and the cross-switch alternates the sign of the LO signals to generate the 8 phases. Limiting amplifiers are used between the VCO and the switch to ensure that the LO swing for the I/Q mixers stays over 0.9 V (peak) for the entire bandwidth. The buffers introduce high impedance to the switch network so the entire LO path operates mostly in the voltage domain. Also, the connecting transmission lines from the 4 oscillator outputs are implemented on the top metal layer with equal lengths for phase accuracy between the LO states (Fig. 2.9(b)).

2.3.2 Wideband BIST Coupling

A key part of wide-band BIST system is the signal coupling to and from the channel-under-test [42]. The coupling ratio should not deviate significantly over the operating bandwidth in order to maintain a similar signal-to-noise ratio. Therefore, a resistive coupler is chosen and its loss is minimized by using a high resistance values. Also, the coupler resistance can be incorporated into the DUT matching network for a wide-band impedance match.

Fig. 2.10 presents the test signal coupling scheme at the input of each phased array channel with 400 Ω resistors. The BIST test signal is distributed to the channel inputs using equal-length distribution networks, and the resistive couplers are placed close to the input nodes. The BIST distribution line has a characteristic impedance of 118 Ω and is therefore terminated with a differential 118 Ω load in order to avoid reflections. Even tough a resistive coupler is used, the coupling ratio changes with frequency due to parasitics and complex source and load impedances impedances. The BIST coupling network is optimized to work properly, when the input port is terminated with antennas

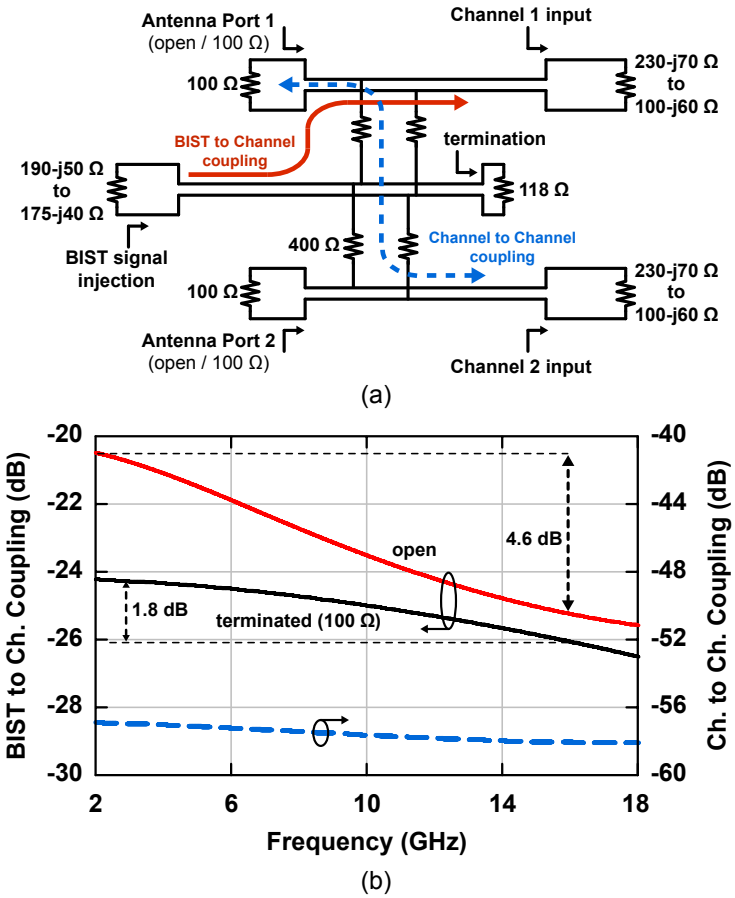


Figure 2.10: (a) Resistive coupler configuration for BIST signal injection to two channel, and (b) BIST to channel and channel-to-channel coupling values when the input (antenna) port is terminated and open.

(100 Ω differential). For the terminated case, the coupling ratio changes by 1.8 dB at 2-15 GHz, whereas for an open antenna port, the coupling ratio differs by 4.6 dB. Fig. 2.10 (b) presents the channel to channel coupling ratio which is less than -56 dB when the channel inputs are terminated with a differential 100 Ω load.

2.3.3 Wideband BIST I/Q Receiver Implementation

The I/Q receiver consists of a pair of passive double-balanced mixers followed by operational amplifiers. The passive mixers are designed with relatively small-size transistors for good isolation, and their layout is optimized in terms of symmetry for good matching (Fig. 2.11(a)). Each mixer block is also enclosed in a deep trench ring for a better isolation between the I and Q channels. Fig. 2.11(b) presents the simulated mixer conversion gain and single-sideband noise figure. The LO swing (V_{peak}) at the mixer gates varies between 0.9 V to 1.8 V at 2-15 GHz. However, the conversion gain does not vary significantly for LO voltages above 0.8 V. The passive mixer is followed by an operational amplifier (op-amp) in a feedback configuration (Fig. 2.12). The op-amp has 26 dB closed-loop gain and a 3-dB bandwidth of 7.5 MHz to accommodate fast BIST measurements.

Fig. 2.13 presents the BIST normalized frequency response. In this case, an ideal short is used as the DUT, and the BIST I/Q output is obtained versus frequency. The response includes the harmonically clean VCO output power versus frequency, the input and output resistive coupler frequency response, and the I/Q mixer response. The simulated BIST system response peaks at 8 GHz with a maximum of 3 dB magnitude difference at 2-15 GHz. This is mainly due to the DC decoupling capacitors at the lower-end and the parasitics from the distribution lines and couplers at the higher-end of the frequency range. This 3-dB difference does not affect the BIST measurement dynamic range.

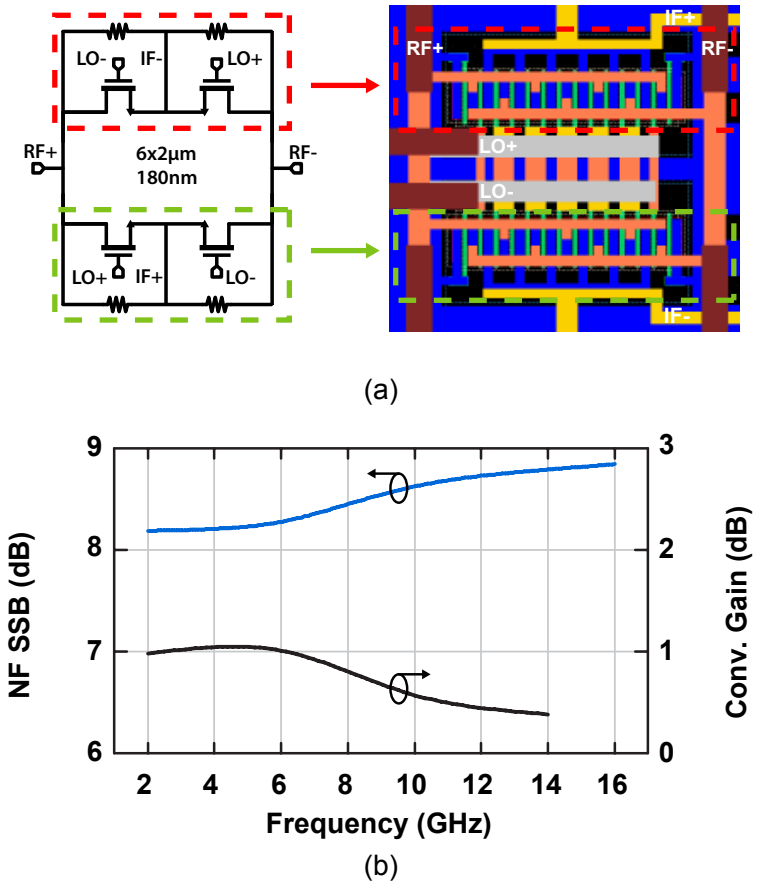


Figure 2.11: Passive mixer: (a) Schematic and layout, (b) simulated NF and conversion gain.

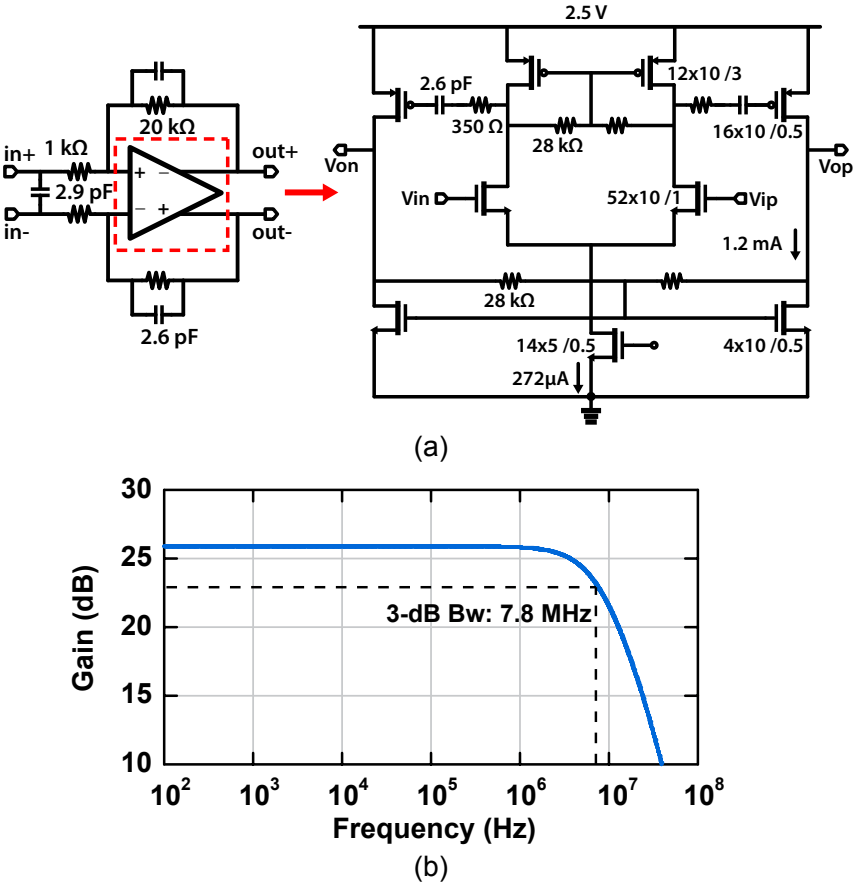


Figure 2.12: IF amplifier: (a) Schematics, (b) closed-loop gain.

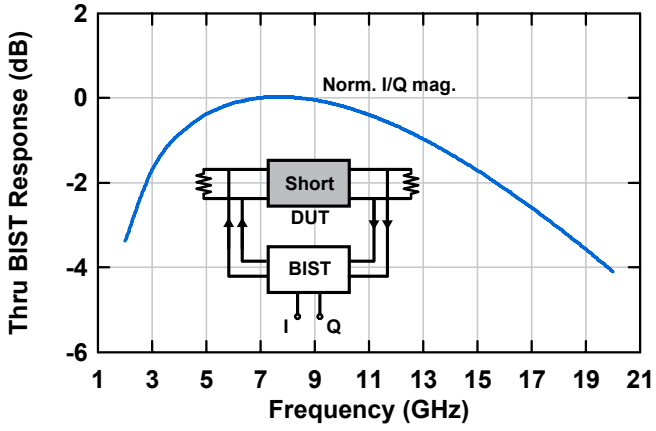


Figure 2.13: Normalized BIST I/Q output magnitude when an ideal short ($\ell = 0$) is used as the DUT.

2.3.4 Wideband BIST Absolute Gain Power Detector Implementation

A network of RMS power detectors has been implemented for the absolute gain measurements of the channel as shown in Fig. 2.3. After their corresponding DC off-sets are de-embedded, the ratio of the DC readings from the input and output detectors can be used to determine the absolute gain of the DUT. Meyer type differential detectors are implemented with a reference pair in order to eliminate the offsets due to process mismatch (Fig. 2.14(a)). Also, the detectors at the input and output share the same op-amp through a symmetrical mux structure to avoid any possible discrepancies from the use of separate op-amps. The detectors consume 10 μA per branch with a high input impedance so that they can be attached to the RF signal line non-invasively without using an additional coupler. As shown in Fig. 2.14(b), the detector's input impedance can be modeled as 800 Ω in parallel with 57 fF, and this results in 0.8-1.4 dB loss for a differential 100 Ω transmission line at 2-15 GHz.

For low power levels (<-20 dBm for a 50 Ω), the Meyer detector operates in the square-law region and results in a DC output directly proportional to (V_{in}^2) [43, 44]. The detectors are designed to maintain a constant responsivity for input powers of -45 to -25 dBm. The detector responsivity is measured on a separate test break-out including buffer & op-amp and is presented in Fig. 2.14(c). The detector responsivity is 317-202 kV/W at 2-15 GHz, but this variation does not affect the absolute gain measurements due to the use of the input and output detector ratio. For the detector network implemented in this work, without the use of 4-port (isolated) coupler, the different impedances at the channel input and output ports over the bandwidth result in a difference between S_{21} and V_{out}^2/V_{in}^2. This causes ± 1 dB deviations in the absolute gain readings versus the VNA S_{21} measurements at various frequencies. However, this effect can be simulated and

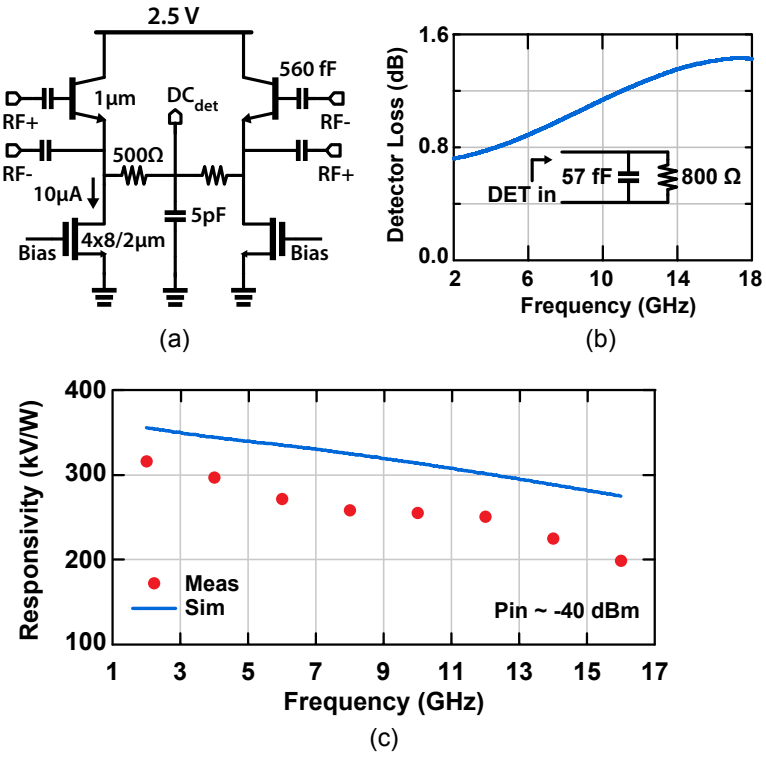


Figure 2.14: (a) RMS power detector schematic, (b) the loss in 100 Ω transmission line due to the detector, (c) measured and simulated detector responsivity.

de-embedded from the measurements for more accurate absolute gain measurements.

2.4 Wideband Phased Array Channel

A pair of wide-band phased array channel is designed and implemented as the DUT for the BIST demonstration. The phased array channel consists of a variable-gain amplifier followed by a 5-bit phase shifter (Fig. 2.3). The phase shifter design is based on the active vector modulator with a wide-band quadrature all-pass filter I/Q network [45]. Two channels are combined together using an active combiner at the output port. The measured RMS phase and gain errors for each channel remain below 6° and 0.8 dB at 2-15 GHz, respectively. VNA measurements for the magnitude and phase of a single channel with the combiner are shown in Fig. 2.15. The main purpose of the BIST system is to replace these VNA measurements with enough accuracy to determine the gain and phase state of the channel at 2-15 GHz.

2.5 Wideband BIST Measurements

Fig. 2.16 presents the simultaneous BIST and VNA measurements setup for the single-ended VNA measurements. VNA measurements are performed in a single-ended configuration by terminating one port of the GSSG probes with 50 Ω loads and also, differentially using Agilent N5242A 4-port PNA-X Network Analyzer. The channel common-mode rejection is simulated to be $>$ 50 dB and therefore, the single-ended measurements do not cause any problems but result in a 6 dB drop in the gain value, which is later added to single-ended VNA measurements. BIST measurements are performed after the VNA is powered down and without lifting the probes in order to maintain the same termination characteristics at the input and output nodes.

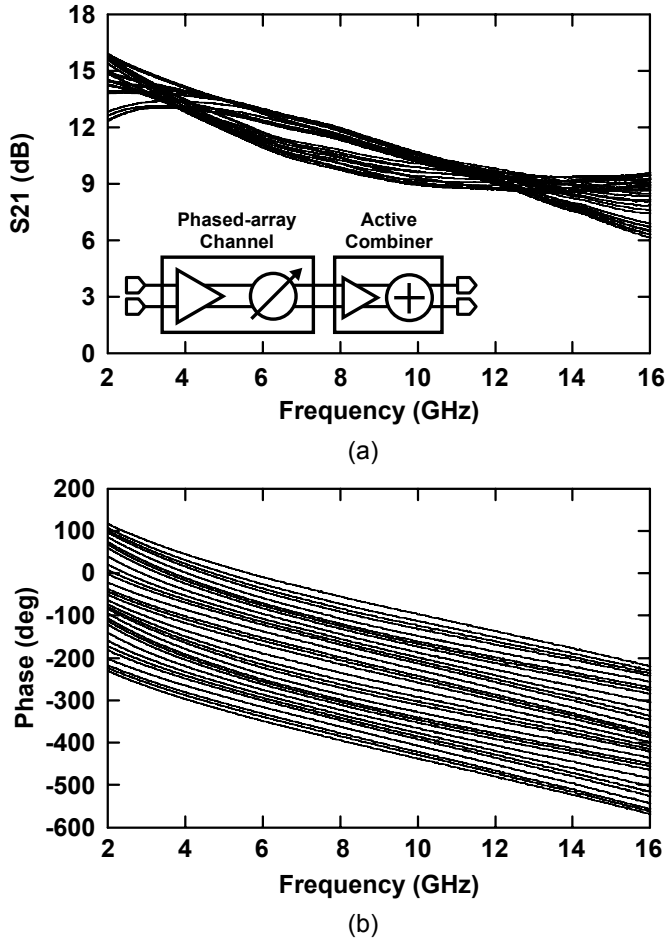


Figure 2.15: Phased-array channel with output power combiner S_{21} VNA measurements.

I and Q DC outputs are measured using the Agilent 34401A multimeters. Fig. 2.17 presents the I/Q readings for all 32 phase states at 2 GHz and 14.5 GHz for a single phase BIST measurement and after the multi-phase correction. The errors are more significant at higher frequencies, and the correction algorithm is particularly more effective towards the higher end of the operation bandwidth.

2.5.1 Relative Phase and Gain Measurements

After the self-correction algorithm is applied to the I/Q DC readings, the relative magnitude and phase of the phased array channel are calculated using:

$$A = \sqrt{I^2 + Q^2} \tag{2.5}$$

$$\phi = tan^{-1}(\frac{Q}{I}) \tag{2.6}$$

Fig. 2.19 presents the measured phase and gain errors at various frequencies. The phase error is calculated by subtracting the VNA and BIST measurements from ideal phase state values. The plots show that the correction algorithm reduces the measurement error significantly both for gain and phase measurements, and allows accurate BIST measurements at 2-15 GHz. Fig. 2.18 presents the BIST measurements for the channel's RMS gain and phase error. The BIST results agree well with the VNA measurements, and the BIST can determine the channel's relative gain and phase error within $\pm$ 0.3 dB and $\pm 3^{\circ}$ accuracy, respectively.

2.5.2 Absolute Gain Measurements

The detector DC outputs at the channel input and output ports are measured using an Agilent 34401 multimeter. In order to obtain accurate absolute gain measurements,

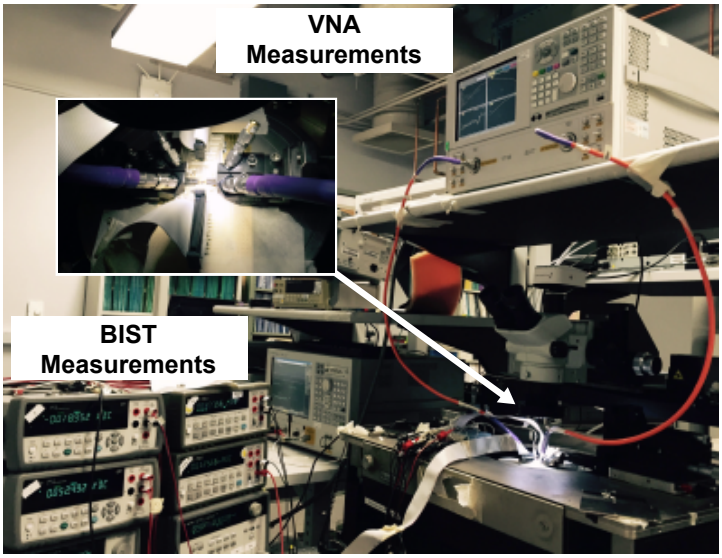


Figure 2.16: BIST and VNA measurement setup.

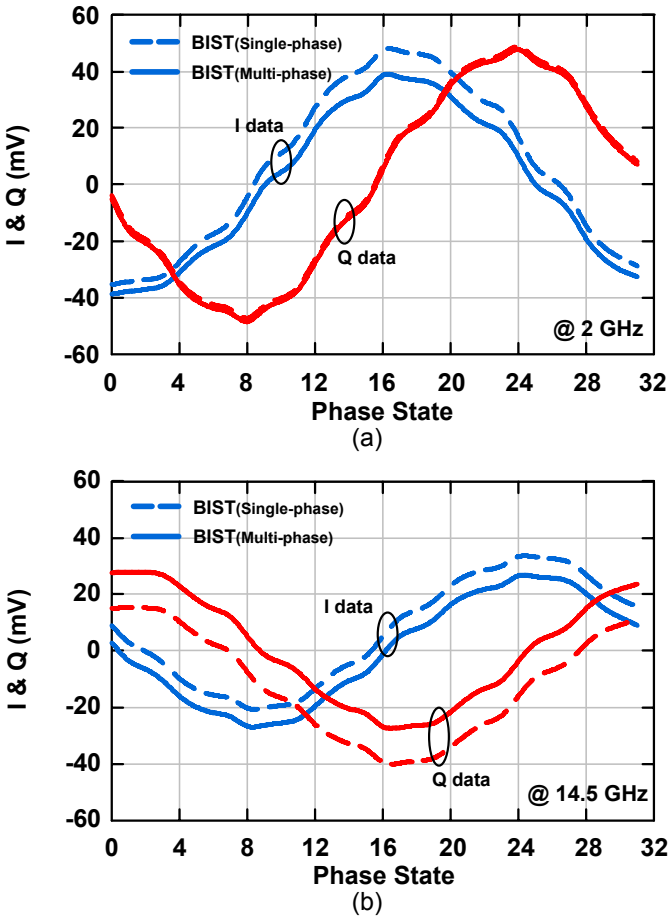


Figure 2.17: Measured single and multi-phase I/Q DC readings at different frequencies.

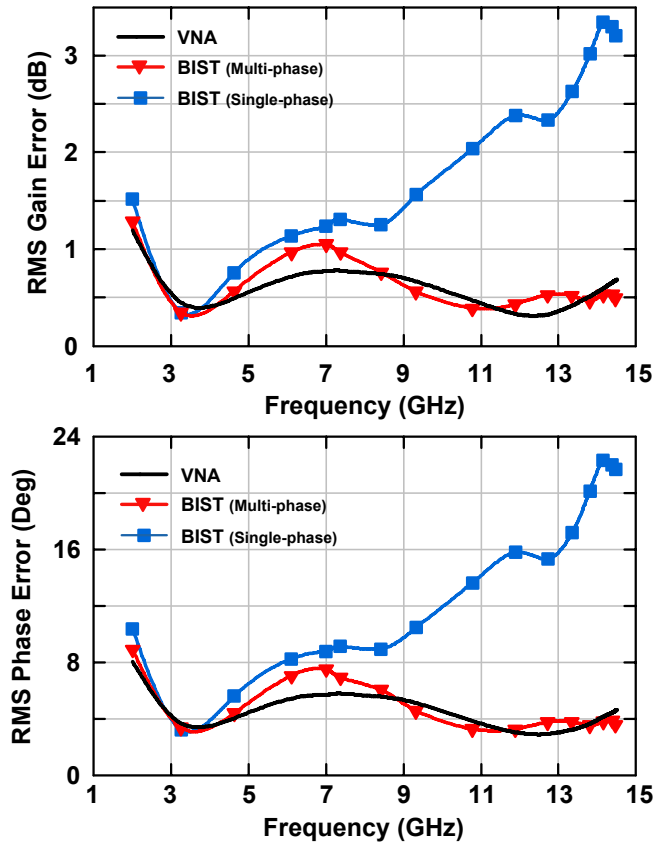


Figure 2.18: BIST and VNA measurements for RMS phase and gain error.

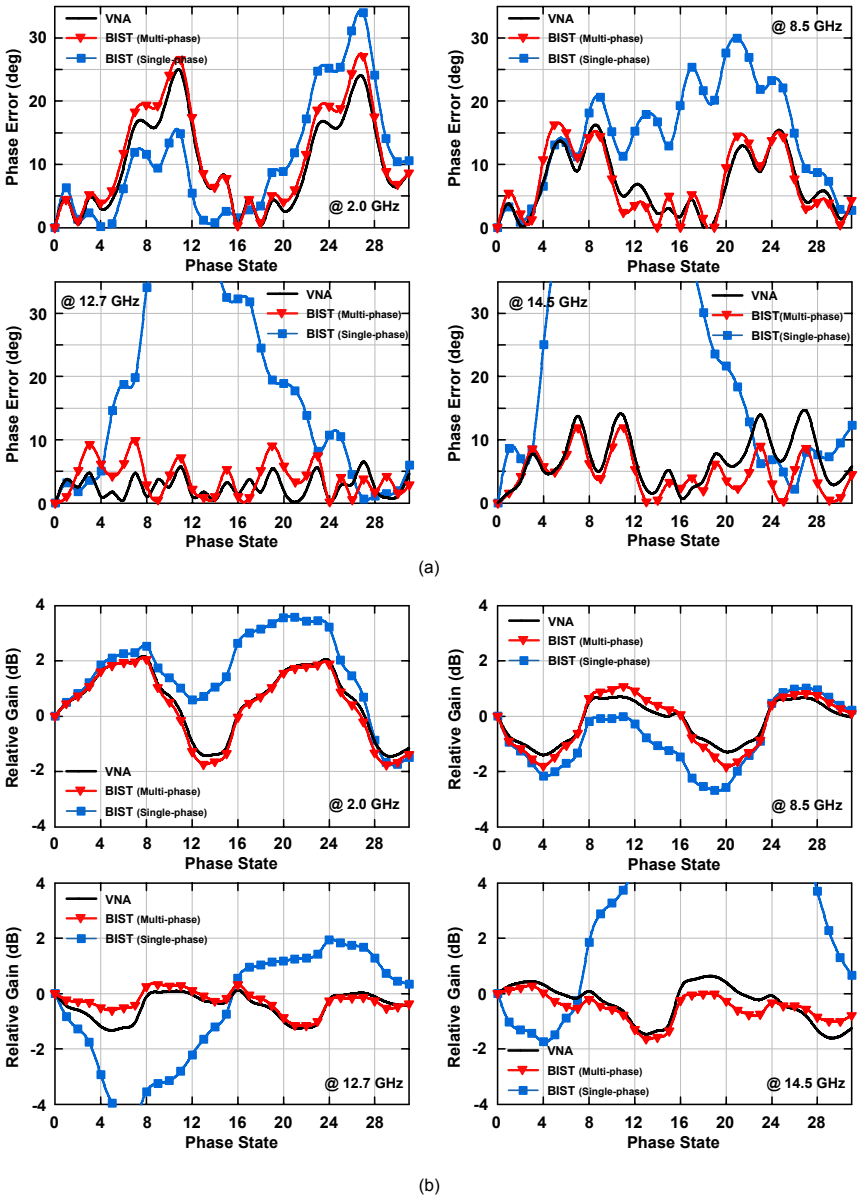


Figure 2.19: VNA and BIST measurements at various frequencies: (a) Phase error, (b) Relative gain error.

first the DC offset of both detectors are determined by the DC readings when both channels are powered down. After the DC-offsets are de-embedded from the readings, the ratio of the output and input detector readings provides the channel absolute gain. As explained above, the simulated impedance deviation effect is de-embedded for accurate results. The detector absolute gain measurements at 2-15 GHz are presented in Fig. 2.20 and agree with the VNA measurements to $\pm$0.5 dB. This type of measurements can be used in order to detect under-performing channels for self-healing feedback controls.

2.5.3 System Settling Time Measurements and Signal-to-Noise Ratio

The time domain response of the BIST system is measured in order to determine the maximum speed for accurate measurements. Fig. 2.21 presents the DC output for the Q path, measured using an oscilloscope with 14 pF input capacitance, when the phase shifter is changed between two phase states with a 180° difference. For 5-bit phase resolution (i.e., $\pm$ 5° error), a 2% I/Q accuracy should be present. Therefore, the 98% system settling time determines the required time for accurate BIST measurements and is 497 ns. This shows that the BIST measurements can be performed at 1 MHz rate, the 8-phase calibration for a single frequency point can be executed in $<$10 µs, and a full 5-bit channel measurements would be completed in $<$40 µs per frequency point including the initial self-calibration.

Fig. 2.22 presents the signal power and noise levels at certain nodes of the BIST system with a 2-channel DUT. The BIST test signal power at plane A is around -35 dBm. The simulated average single-sideband noise figure at plane M is 39.5 dB, and this corresponds to a noise figure of 26.6 dB at plane A and a noise power of -87.4 dBm for a

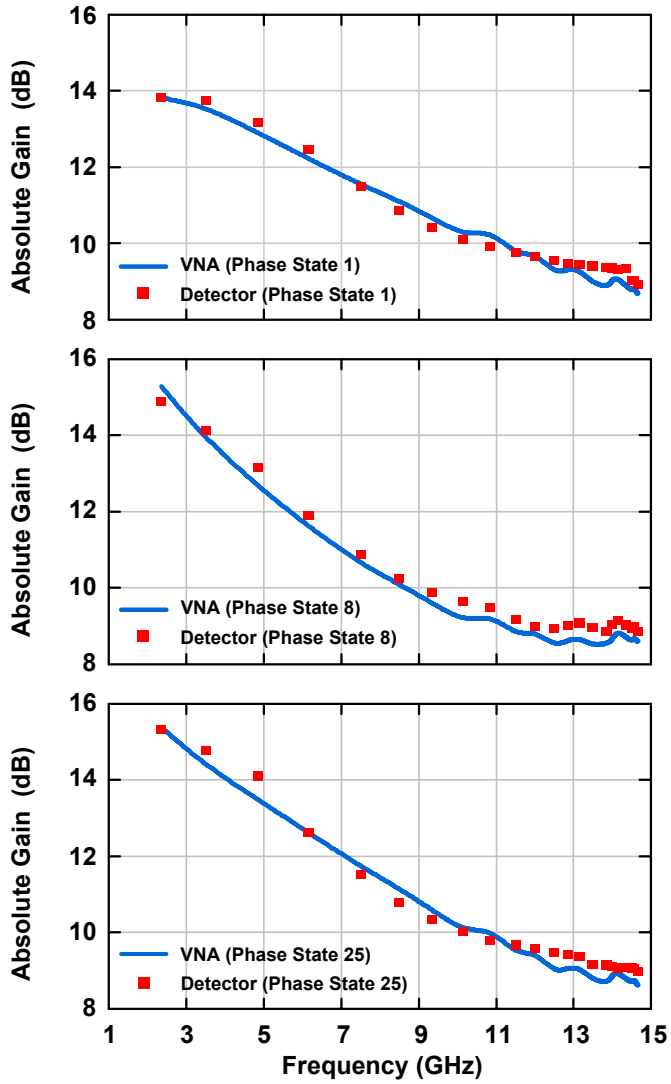


Figure 2.20: Absolute gain versus frequency from on-chip detector and VNA measurements.

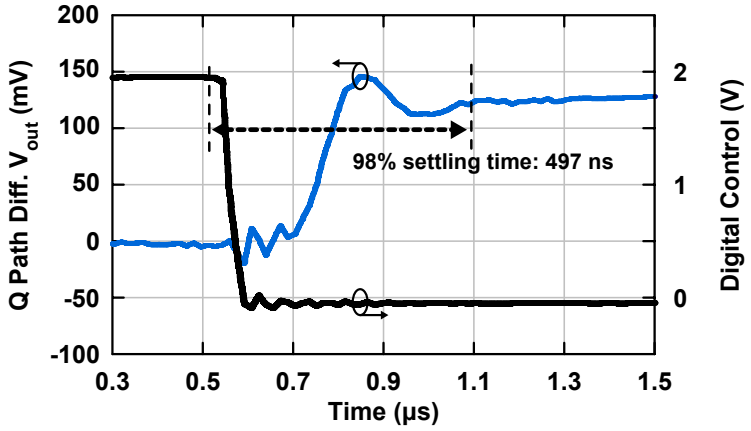


Figure 2.21: Oscilloscope measurement for worst-case settling time of BIST measurements.

1 MHz bandwidth. The SNR at plane is:

$$SNR_A = -34 - (-174 + 26.6 + 60) = 53.4 \text{ dB (at 1 MHz)} \quad (2.7)$$

This SNR provides a high measurement accuracy at 1 µs sampling time per point.

2.6 Conclusion

A wide-band BIST system with self-correction algorithm is presented and implemented for a 2-15 GHz phased-array channel, but the same principles can be used on any DUT that have amplitude & phase response versus frequency (LNA, PA, VGA, etc.). Also, for wide-band I/Q up and down-converters, the I/Q receiver can be fed using 8-different LO states for DC offset, gain and phase imbalance calibration for more accuracy. It has been shown that the one-time calibration procedure can be quickly executed and does not add a significant measurement time overhead.

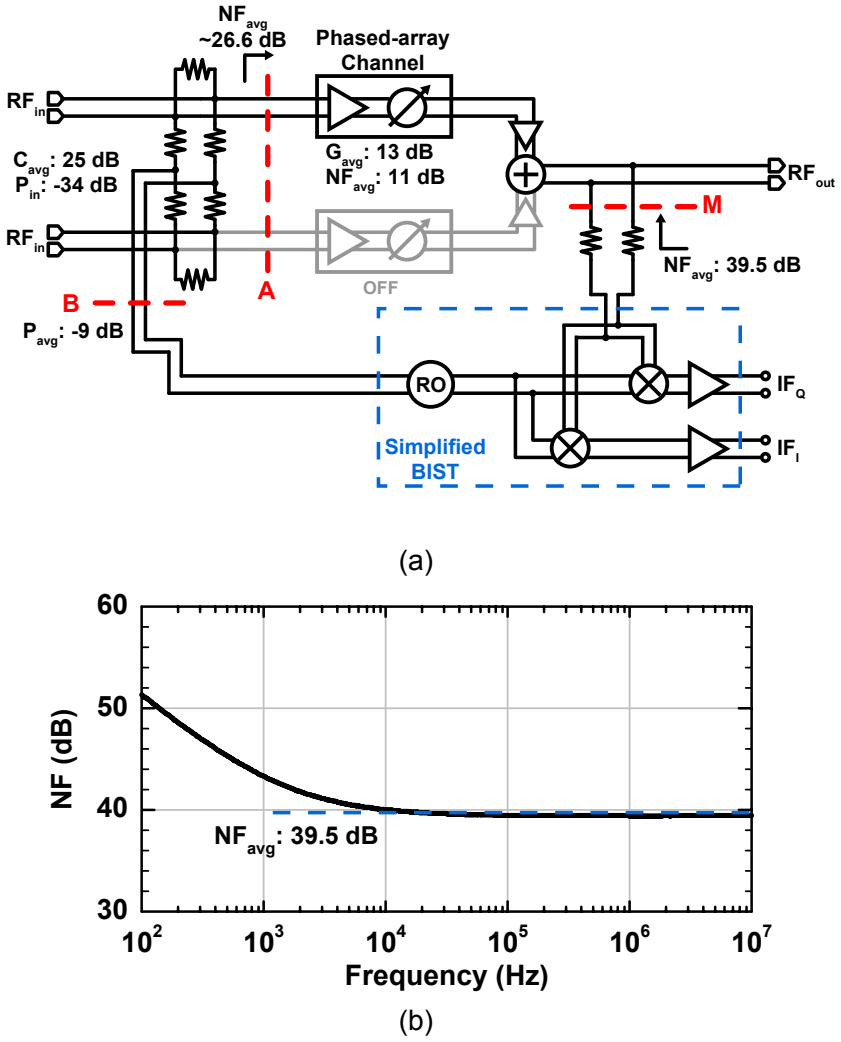


Figure 2.22: (a) Noise and power levels at various nodes for dynamic range calculation, (b) noise figure of the down-converter.

This chapter also demonstrated the first closed-loop wide-band BIST system at 2-15 GHz with an on-chip signal generator. The wide-band BIST design trade-offs and challenges are studied in detail. For the new application areas of phased arrays, it is expected that wide-band BIST methods would be used for calibration and in-situ self-healing features.

2.7 Acknowledgements

This work was supported in-part by Professor Gabriel M. Rebeiz Chair Funds at the University of California, San Diego.

Chapter 2 is mostly a reprint of the material as submitted to IEEE Transactions on Microwave Theory and Techniques, 2015. Tumay Kanar; Samet Zihir; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 3

A Low-Power 136 GHz SiGe Total Power Radiometer with NETD of 0.25K

3.1 Introduction

The use of passive imaging systems at millimeter-wave frequencies results in high resolution detection due to the relatively small wavelength and low-loss propagation in different frequency windows. The main application areas are passive surveillance sensors, concealed weapon detection, and navigation and landing systems for low-visibility conditions [16–21]. The low atmospheric attenuation windows at 35, 94, and 135 GHz allow propagation through large obstacles such as fog, dust, and clothing and therefore, these frequencies are especially appealing for low-visibility navigation systems and concealed weapon detection (Fig. 3.1). W-band imaging systems, which utilize the window centered around 94 GHz, are already available in III-V technologies [46], and have recently been commercially introduced in SiGe technology as well [47].

D-band imaging systems have a high potential for better spatial resolution and more compact size than the W-band systems due to their smaller wavelength (2.2 mm instead of 3.2 mm). A SiGe D-band radiometer takes advantage of the low atmospheric loss window at 135 GHz and can provide an inexpensive and robust solution for high resolution imaging systems. This has been an active research area in CMOS and SiGe technologies, and some systems with promising noise and temperature resolution have been shown [22,23]. In this chapter, we present a low-power SiGe single-chip total-power radiometer at 136 GHz, which demonstrates state-of-the-art performance for D-band passive imaging applications. The chip consists of a high gain single-ended cascode LNA and a differential square-law detector (Fig. 3.2). A Dicke switch is not integrated on this chip due to the low 1/f noise properties of SiGe, and this function can be done externally using periodic calibration [48].

This chapter is organized as follows. Section II discusses radiometry basics and explains the key radiometer parameters. Section III introduces the SiGe technology used and presents the design, optimization, and experimental characterization of radiometer blocks. Section IV presents the measurements for radiometer characterization both at low and D-band frequencies, and Section V summarizes the results with a conclusion.

3.2 Total Power Radiometry

Total power radiometers are very sensitive receivers which can detect the emitted or reflected thermal radiation (noise) from objects. The main goal of a radiometer is to generate a linear relationship between the input noise power and the output DC voltage, and its thermal resolution is dictated by the radiometer system noise for a given integration time and input noise bandwidth.

Fig. 3.3 presents voltage spectral densities (I_f) at various nodes in a typical total

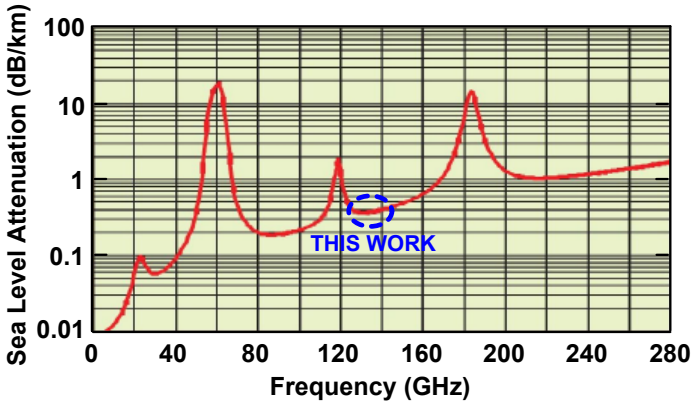


Figure 3.1: Sea-level atmospheric attenuation spectrum [1].

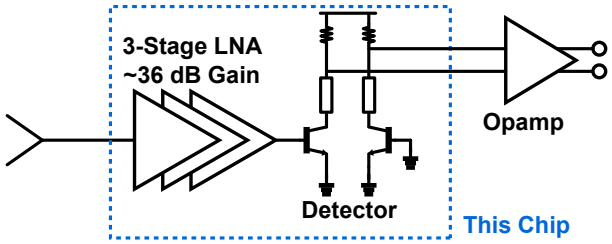


Figure 3.2: Overview of SiGe total power radiometer system.

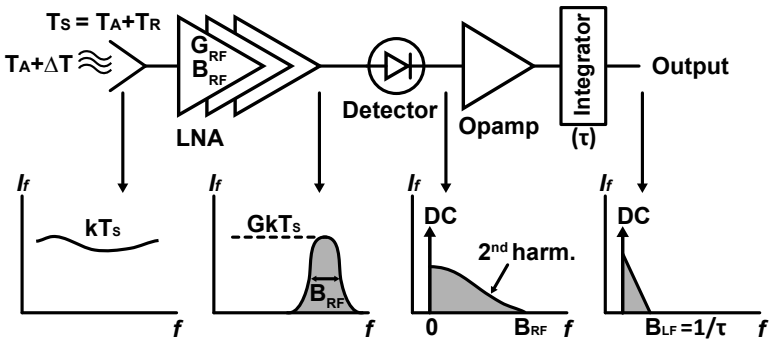


Figure 3.3: Total power radiometer spectral densities at certain nodes in the system.

power radiometer [49]. The white noise at the input (T_S) is due to the combination of the ambient black-body radiation (T_A) and the noise of the radiometer circuits (T_R). This noise is amplified and filtered to a certain bandwidth (B_{RF}) by the RF pre-amplification stages. The amplified and filtered noise power is converted to a DC voltage along with the 2^{nd} harmonic fluctuations by the square-law detector. The op-amp and the integrator further amplify the detector output and filter the harmonic content into a much narrower bandwidth (B_{LF}), which is determined by the integration time ($B_{LF} = 1/2\tau$). The radiometer final output DC voltage is proportional to the thermal input power.

The minimum resolvable temperature for a radiometer (resolution or sensitivity) is quantified by the noise equivalent temperature difference (NETD) and is given by [50–52]:

$$NETD = T_S \sqrt{\frac{1}{\tau B_{RF}} + \left(\frac{\Delta G}{G}\right)^2} \tag{3.1}$$

where $\Delta G/G$ is the low frequency fluctuations of the high gain amplifier, B_{RF} is the radiometer's RF noise bandwidth, and $T_s = T_A + T_R$. Assuming that the LNA gain fluctuations can be removed in radiometer systems by mechanical scanning or periodic reference-target exposure, the NETD expression can be simplified to:

$$NETD = \frac{T_S}{\sqrt{\tau B_{RF}}} \tag{3.2}$$

This equation shows a trade-off between the radiometer system noise and the scanning speed. In order to achieve faster scanning systems with lower integration times, a very low noise radiometer with a wide RF bandwidth is required.

Another key parameter for signal detection is the noise equivalent power (NEP) and is defined as:

$$NEP = \frac{v_{no}}{\mathbb{R}} \quad W/\sqrt{Hz} \quad , \quad \mathbb{R} = \frac{V_{out,DC}}{P_{in,RF}} \quad V/W \tag{3.3}$$

where v_{no} is the radiometer output noise voltage density (V/$\sqrt{\text{Hz}}$) at the offset frequency of $1/2\tau$ and $V_{out,DC}$ is the radiometer DC output voltage. $\mathbb{R}$ is the radiometer responsivity and is the conversion ratio from the RF input power to the output DC voltage level. NEP is a figure-of merit for detectors and dictates the minimum RF input power required to generate a DC voltage which is at the same level as the output noise.

3.3 Radiometer Blocks: Design and Characterization

3.3.1 Technology

SiGe HBT technology is suitable for radiometer systems since it enables high gain LNA at millimeter-wave frequencies with low 1/f noise and gain fluctuations along with wide RF bandwidths. Also, it allows the on-chip integration of high responsivity detectors and high gain op-amps, both with very low noise [22, 52, 53].

The 136 GHz radiometer is designed in a 90 nm IBM SiGe BiCMOS process with 10 metal layers. Fig. 3.4 presents the process metal stack-up and a typical transistor layout with the interconnects up to the top metal. The nominal peak f_t is stated as $\sim$ 300 GHz at a current density of 2 mA/μm [54], whereas a peak f_t of 260 GHz is measured for a 3 μm device with all the interconnects to the top metal (Fig. 3.5). The measured peak f_{max} is $\sim$ 300 GHz at 2.5 mA/μm current density.

Transmission lines are implemented in the top metal layer as a microstrip configuration with a ground layer at M1_4B. A 10 μm wide line in the LD layer results in a characteristic impedance of $\sim$50 Ω and a simulated loss of 0.56 dB/mm at 135 GHz. The matching inductors are based on 8 μm wide transmission lines (Z_o= 58 Ω) and result in a

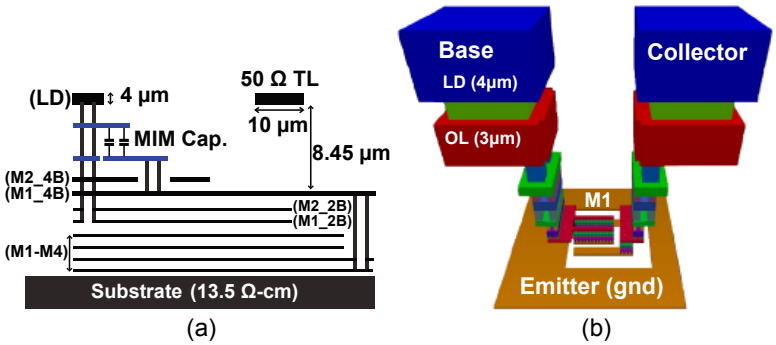


Figure 3.4: (a) Metal stack-up showing 50 Ω transmission line and MIM capacitor layers, (b) HBT transistor layout with connections up to the top metal layer.

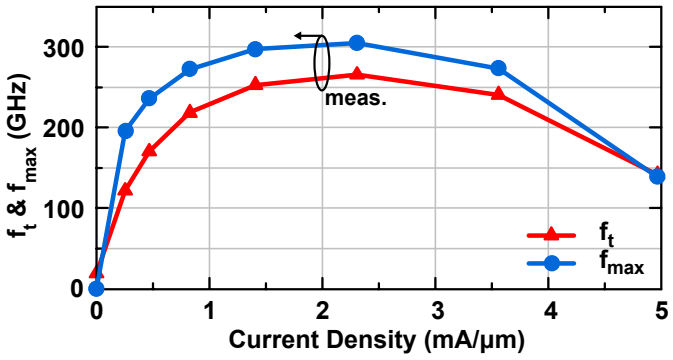


Figure 3.5: f_t & f_{max} measurements for a 3 μm HBT device.

simulated Q of $\sim$36. Note that our experience indicates that the measured line loss at $>$80 GHz is 20-25% higher than the simulations.

The IBM 90 nm SiGe process offers MIM capacitors, which are used as decoupling capacitors (RF shorts) when relatively large capacitors are required. The matching network capacitors, where smaller capacitance values are necessary, are implemented as MOM capacitors with M2_4B and M1_4B metal layers without a ground metal layer underneath them. Capacitors and all the matching circuits are simulated using Sonnet EM Suites [55]. As an example, Fig. 3.6 presents the input matching network for the LNA. Similar capacitors and inductors are used for all the matching networks throughout the design.

3.3.2 LNA Design & Measurements

The schematic for the three-stage LNA is presented in Fig. 3.7(a). In order to achieve a minimum temperature resolution of $\sim$ 0.2K, a gain $>$35 dB is required for the LNA, and this can be achieved using three cascode stages. Fig. 3.8 presents the minimum noise figure (NF_{min}), available gain (G_A), and minimum noise measure (M_{min}) of 3 μm and 6 μm cascode and common emitter (CE) stages at 135 GHz. M_{min} is calculated by plugging in the simulated (NF_{min}) and (G_A) to the equation (3) in [56]. The cascode stage is inherently more prone to stability issues but provides significantly higher gain. Even though its minimum noise figure is $\sim$1.5 dB higher than the common emitter stage, the minimum noise measure for cascode and common emitter stage is very close. Therefore, a careful use of cascode amplifiers enables similar gain and noise performance at a much lower power consumption without any stability issues.

The design of the three stage cascode amplifier is optimized for high gain and low power consumption. The first two stages are realized using 3 μm devices since they offer $\sim$3 dB higher gain than 6 μm devices without a significant difference in NF_{min}.

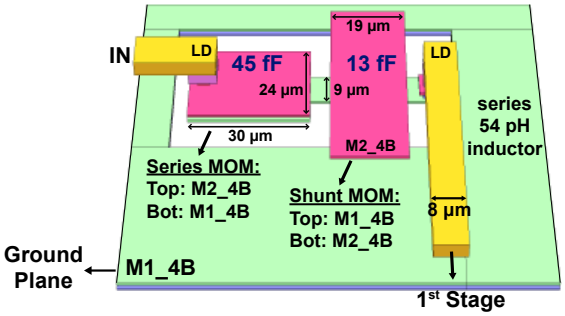


Figure 3.6: LNA input matching network EM simulation setup showing MOM capacitors and transmission line inductor.

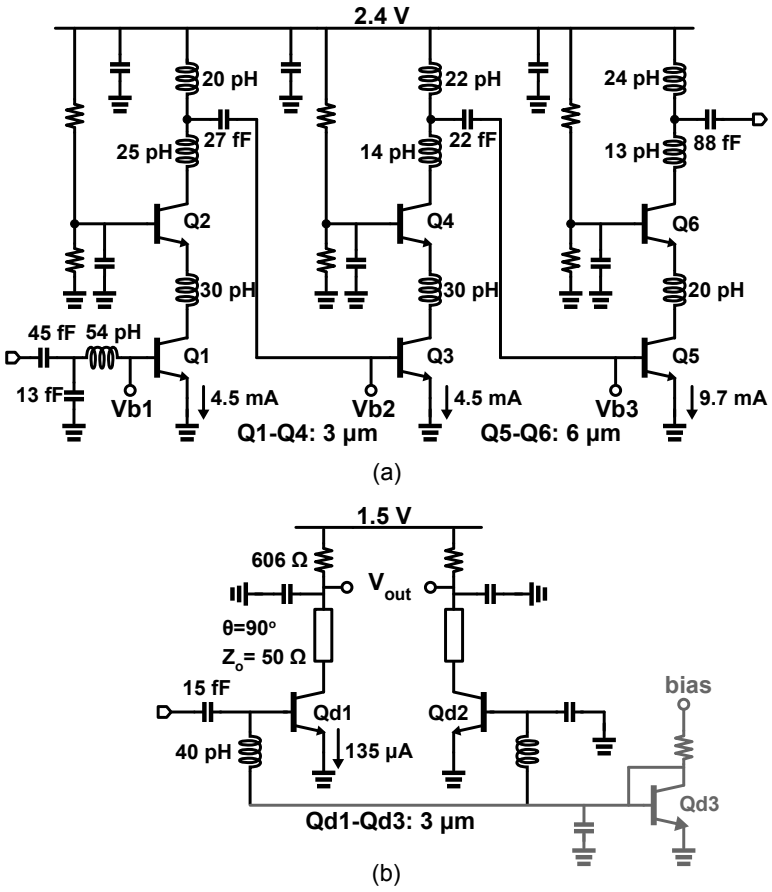


Figure 3.7: Schematics of: (a) Three-stage cascode LNA, (b) Detector with differential output.

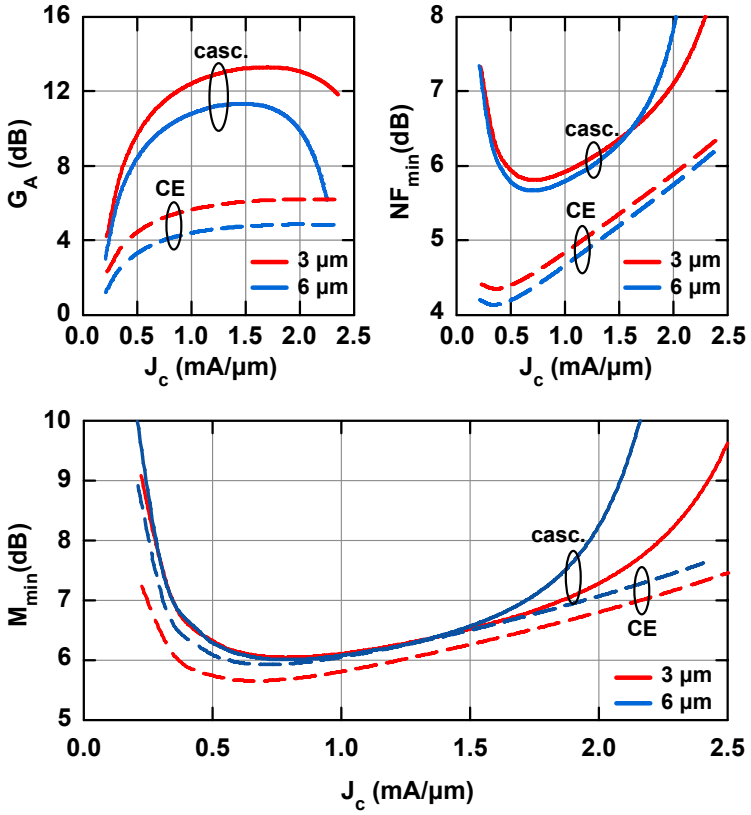


Figure 3.8: Simulated G_a, NF_{min} & M_{min} of 3 µm and 6 µm cascode and common emitter transistors at 135 GHz.

A 6 μm cascode is used as the last stage to result in a more relaxed matching network between the LNA and the detector. The cascode stages are biased using BJT current mirrors, and the bias current is optimized at 1.5 mA/μm for the highest G_A with a low M_{min}. Series-shunt peaking is used at the cascode collector nodes for the maximum gain with a wider bandwidth [57, 58]. In order to further improve the cascode stage gain and bandwidth, the parasitics at the common-base transistor emitter nodes are resonated out using series inductors [59]. A low inductance AC ground at the commmon-base device base nodes is necessary for the cascode stage stability. This AC ground is realized by large size MOM capacitors ($\sim$60x60 μm^2), which are built using lower metal layers (M1_2B and M2_2B) so that they can be implemented very close to the transistor base. The geometry and location of these capacitors are optimized by EM simulations in order to provide a low impedance ground at the base. Another stability concern is the coupling through the V_{DD} bias network since only a single V_{DD} bias pin is used for all three stages. Therefore, an array of MIM capacitors with a simulated Q of $\sim$1.5 at 135 GHz are placed right after the series-shunt peaking inductors. Additional V_{DD} decoupling vncap capacitors are placed along the V_{DD} distribution line for a lower Q decoupling.

Fig. 3.9 shows the micrograph of the LNA test-cell with a size of 500 x 300 μm^2 without the pads. The LNA is biased at 2.4 V using 100 μm probes and without any probe-tip capacitors and draws 18.7 mA current as per simulations.

The S-parameter measurements are performed using the Agilent N5230C VNA along with WR-6 extender modules. On-chip TRL calibration kit is used for de-embedding the cables, probes, and on-chip RF pads. The three stage LNA has a peak gain of 36 dB at 138 GHz with a 3-dB bandwidth of 135.5-141 GHz (Fig. 3.10). The reverse isolation is $<$ -37 dB around the peak gain region. The amplifier's k-factor is $>$1 for the test-cell with 50 Ω termination. No stability issues have been observed with the single-chip radiometer mesurements either (monitoring the bias current, output spectrum,

etc.).

Fig. 3.11 presents the LNA input and output return loss. The LNA input is well-matched at 134-138 GHz. The output is decently well-matched to 50 Ω between 130 GHz to 136 GHz. It should be noted that the matching condition is different for the radiometer as the LNA and detector are designed to be conjugately matched around 136 GHz.

3.3.3 Detector Design & Measurements

The detector is designed according to the method presented in [60]. Instead of introducing an RF short at the collector at the fundamental frequency, a high impedance is introduced at the collector using a quarter-wavelength transformation from an AC ground. This design has been shown to result in higher responsivity by increasing the input impedance and the corresponding voltage swing at the detector input. The transistor size and bias current are optimized in terms of responsivity and NEP using Cadence simulations. Simulations show that a wide range of bias current of 80-140 μA results in a constant NEP of 0.6 pW/$\sqrt{\text{Hz}}$ with a responsivity of 11-14 kV/W since the responsivity and noise increase simultaneously (see the measurement section). An on-chip load resistor of 606 Ω is chosen in order to result in a high responsivity while keeping the output noise at a low level and is realized with wide resistors so as to minimize the 1/f noise contribution. The detector core without the pads occupies an area of 170 μm by 300 μm (Fig. 3.12 (a)). The matching elements and quarter-wave lines are optimized by simulating the whole detector using Sonnet EM-suites (Fig. 3.12 (b)).

The measured S_{11} of the stand-alone detector is presented in Fig. 3.12 (c). The detector is designed to be conjugate matched to the LNA output impedance at 136 GHz. However, in a stand-alone testcell, it is well matched to 50 Ω at 160 GHz. Therefore, all responsivity and NEP measurements are done at 160 GHz for detector characterization.

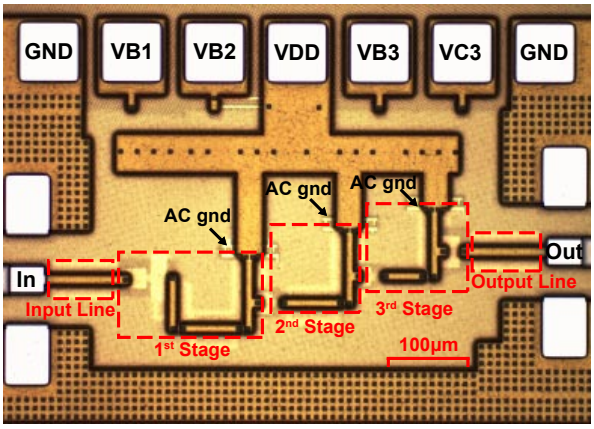


Figure 3.9: Micrograph of the LNA test-cell (740 x 480 µm^2 including pads).

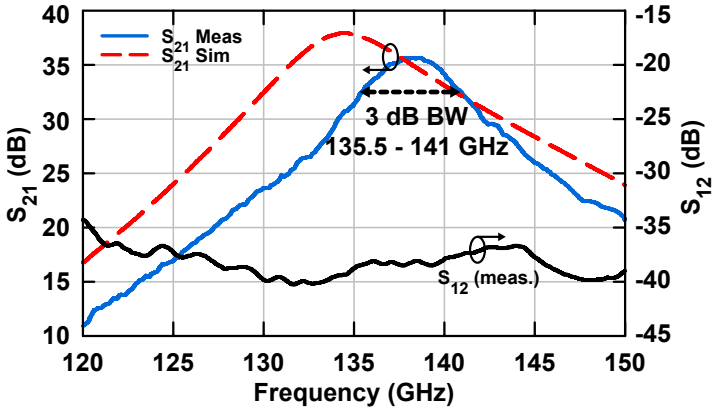


Figure 3.10: Measured and simulated LNA gain and S_{12} versus frequency.

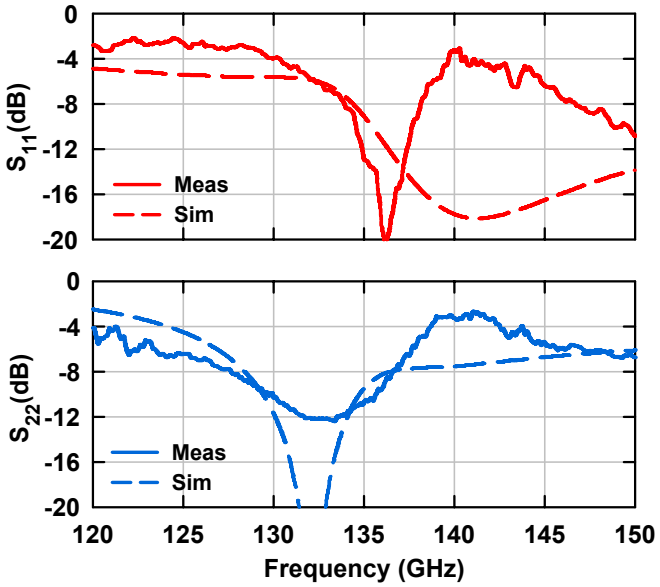


Figure 3.11: Measured and simulated S_{11} and S_{22} for the D-band LNA.

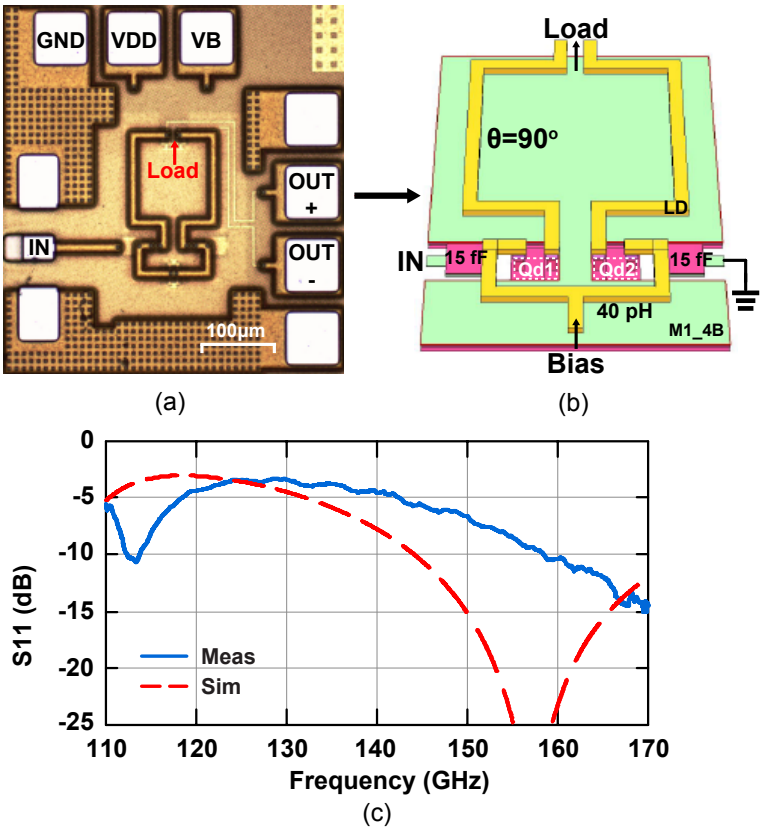


Figure 3.12: Detector: (a) Test-cell micrograph, (b) EM simulation setup, and (c) measured and simulated S_{11} versus frequency.

Table 3.1: Detector Performance Summary & Comparison

	Frequency (GHz)	NEP (pW/Hz$^{1/2}$)	$\mathbb{R}$ (kV/W)	P_{DC} (μW)
This work	**160***	**0.7**	**11**	**405**
[22] (SiGe)	165	6	11	1700
[65] (CMOS SOI)	170	8-10	3	200
[52] (SiGe)	94	4	12	180
[53] (SiGe)	94	5	11	76
[66] (SiGe)	80	0.4	80	32
**Stand-alone detector is characterized at 160 GHz.*				

Fig. 3.13 presents the measured detector responsivity. The input signal is generated by a VDI multiplier chain and is AM modulated at 1 kHz. The input power level is monitored using a PM4 power-meter [61] and a 3-dB coupler. The output voltage is measured using a lock-in amplifier [62] at 1 kHz. A peak responsivity of $\sim$ 11 kV/W is obtained for an input power of -38 dBm at 160 GHz and agrees well with simulations. It is observed that at -25 dBm, the responsivity at 160 GHz drops to 7 kV/W. Note that at 136 GHz, the detector responsivity is 5 kV/W, and this degradation is due to the S_{11} mismatch.

The detector output noise voltage is measured using a 13 dB ENR D-Band noise source [63] in the off-state as a wideband matched load and a low-noise amplifier (SR-552) placed before the spectrum analyzer (Fig. 3.14). The gain of the low-noise amplifier is de-embedded from the measurements, and the measured detector output noise voltage is 7 nV/$\sqrt{\text{Hz}}$ at 1 kHz. Noise measurements show that the detector corner frequency is $\sim$120 Hz. It should be noted that all the measured noise voltages are multiplied by 1.05 dB due to the averaging characteristics of the spectrum analyzer for noise-like input signals [64].

Fig. 3.15 presents the measured detector responsivity and NEP values at 160 GHz for various bias currents. The detector results in an NEP of 0.7 pW/Hz$^{1/2}$ and a responsivity of 11 kV/W at a bias current of 135 μA/branch. The detector demonstrates

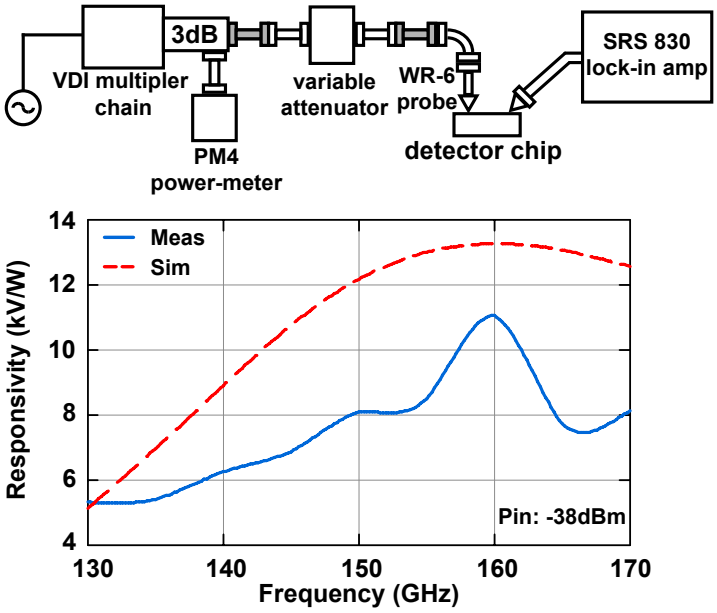


Figure 3.13: Responsivity measurement setup for detector responsivity and detector responsivity vs. frequency (Pin =-38 dBm, Idc =135 μA per branch).

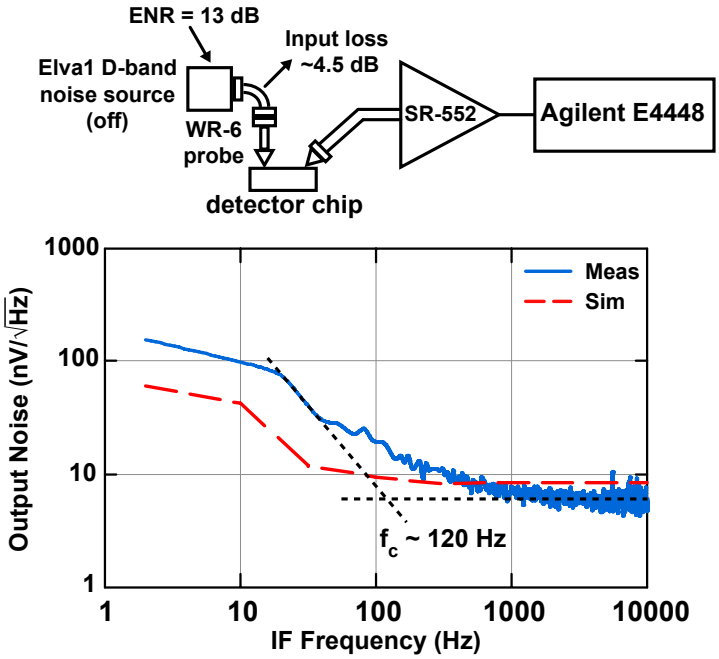


Figure 3.14: Detector noise measurement setup and simulated & measured detector output noise voltage.

state-of-the-art performance at D-band as shown in Table 3.1.

3.4 Radiometer Measurements & Characterization

The SiGe D-band radiometer is realized by the integration of the three stage LNA and the low-noise detector. The interface between the LNA and detector is optimized for conjugate matching and maximum power transfer. This is shown in Fig. 3.16 where the power transfer at 136 GHz is 4 dB higher than at 155 GHz. The active area for the SiGe radiometer is 995 x 525 μm^2 without the pads (Fig. 3.17).

The radiometer is characterized experimentally in both the millimeter-wave and the low frequency domain using on-wafer probes. Measurements are performed for key radiometer performance parameters, such as responsivity, output noise voltage, NEP, DC temperature sensitivity, and eventually, NETD. It is shown that the results from both millimeter-wave and low frequency methods agree well with each other.

3.4.1 High Frequency Radiometer Measurements

The input impedance match for the radiometer is an important parameter as it dictates the antenna loss due to mismatch. As the Fig. 3.18 presents, the on-chip SiGe radiometer is matched to 50 Ω at 134-160 GHz ($S_{11} <$ -8 dB).

The radiometer responsivity is measured using a VDI D-band multiplier chain and a PM4 calorimeter with couplers for tracking the input power level. The radiometer DC output is measured with a lock-in amplifier (SR-830) for accurate results (Fig. 3.19 (a)). The sampling frequency of the lock-in amplifier is set to 1 kHz in order to avoid any flicker noise effects on the responsivity measurements. A peak responsivity of $\sim$52 MV/W is measured at 136 GHz with a 3-dB bandwidth of 133.5-138.5 GHz (Fig. 3.19 (b)). The measured bandwidth is narrower than the simulations due to the sharper LNA

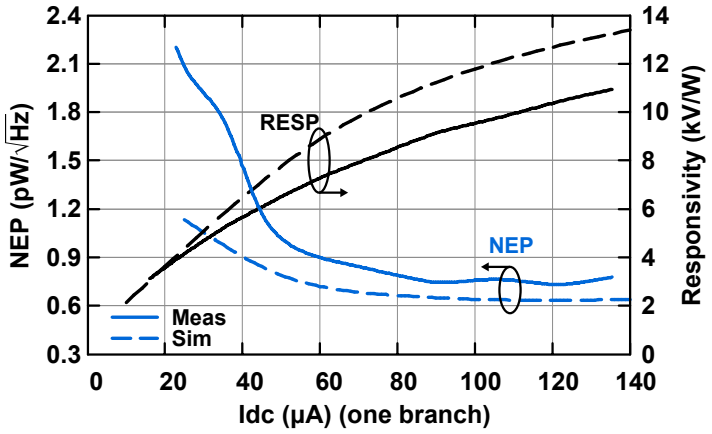


Figure 3.15: Measured and simulated detector responsivity and NEP versus detector bias current (at 160 GHz when input power is -38 dBm).

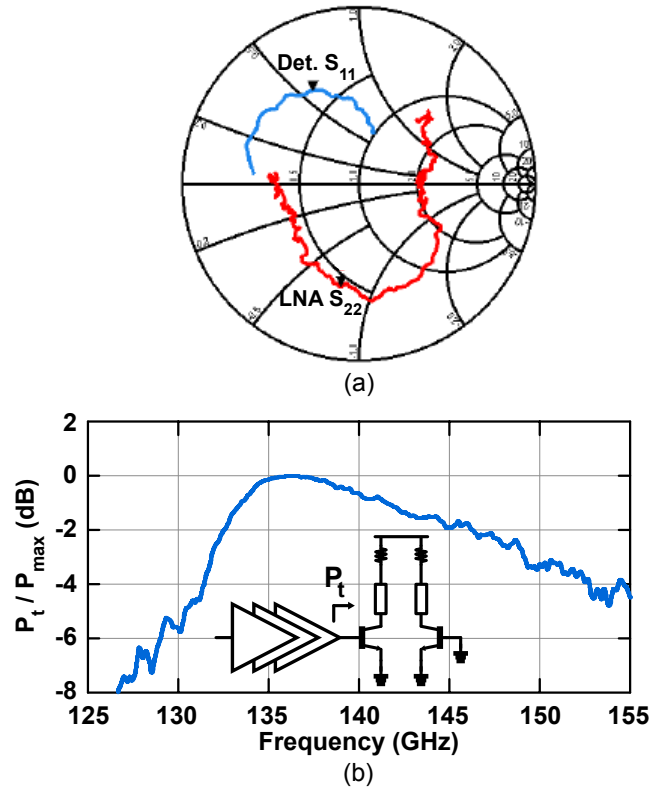


Figure 3.16: (a) De-embedded Detector S_{11} and LNA S_{22} measurements on a Smith chart (markers at 136 GHz), and (b) Maximum power transfer between the LNA and the detector vs. frequency (generated from the LNA and detector test-cell measurements).

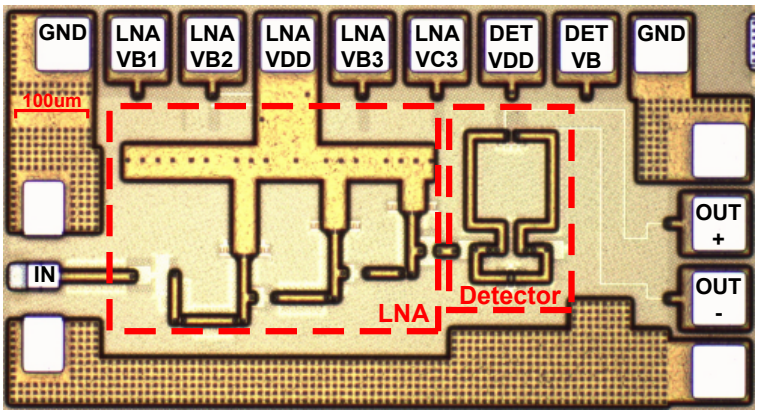


Figure 3.17: Chip micrograph for the SiGe D-band radiometer.

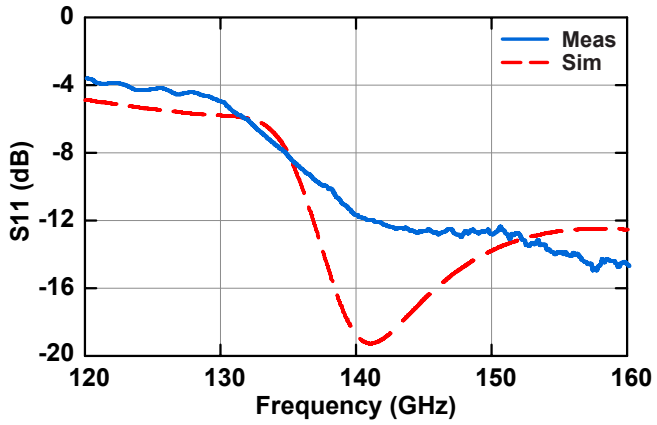


Figure 3.18: Measured and simulated input return loss for the D-band radiometer.

gain response. The responsivity is also measured vs. input power, and the radiometer operates without significant compression ($<$10%) for input power levels up to -57 dBm (Fig. 3.19 (c)). The power sweep is limited by the available power settings, attenuators, and measurement ranges of the D-band test equipment. The setup for the radiometer noise measurement is presented in Fig. 3.20(a). A D-Band noise source with an ENR of 13 dB (T_{hot} = 5786K) is used for Y-factor measurements, and the setup introduces 4.5 dB loss at the input including the WR-6 probe loss. The output noise spectrum is measured using a spectrum analyzer. The output noise is amplified using a low-noise pre-amplifier, and the gain of this amplifier is de-embedded from the measured results (Fig. 3.20(b)). The harmonics of 60 GHz dominate the lower frequency noise but, it is clear that the corner frequency for the radiometer is lower than 100 Hz. This low flicker-noise characteristic of the radiometer shows that it suitable for high resolution imaging applications. The radiometer output noise levels out at $\sim$ 65 nV/$\sqrt{\text{Hz}}$ when the noise source is in its cold state (T_{cold} = 290K) and increases to $\sim$ 140 nV/$\sqrt{\text{Hz}}$ for its hot state (T_{hot} = 2053K, input-loss = 4.5 dB).

The radiometer NEP is calculated from the measured output noise and the responsivity values, and is presented in Fig. 3.21. The minimum measured NEP is 1.4 fW/$\sqrt{\text{Hz}}$ at 135.5 GHz and agrees with simulations. The NEP is $<$3 fW/$\sqrt{\text{Hz}}$ within the radiometer 3-dB responsivity-bandwidth.

3.4.2 Low Frequency Radiometer Measurements

Low frequency measurements for the radiometer noise characterization are performed in two different methods to accurately verify the radiometer performance. Fig. 3.22(a) presents the measurement setup for the thermal responsivity of the radiometer. The effective ENR for the noise source is changed using a D-band attenuator, and the output DC voltage is measured with an accurate multimeter and a low noise operational

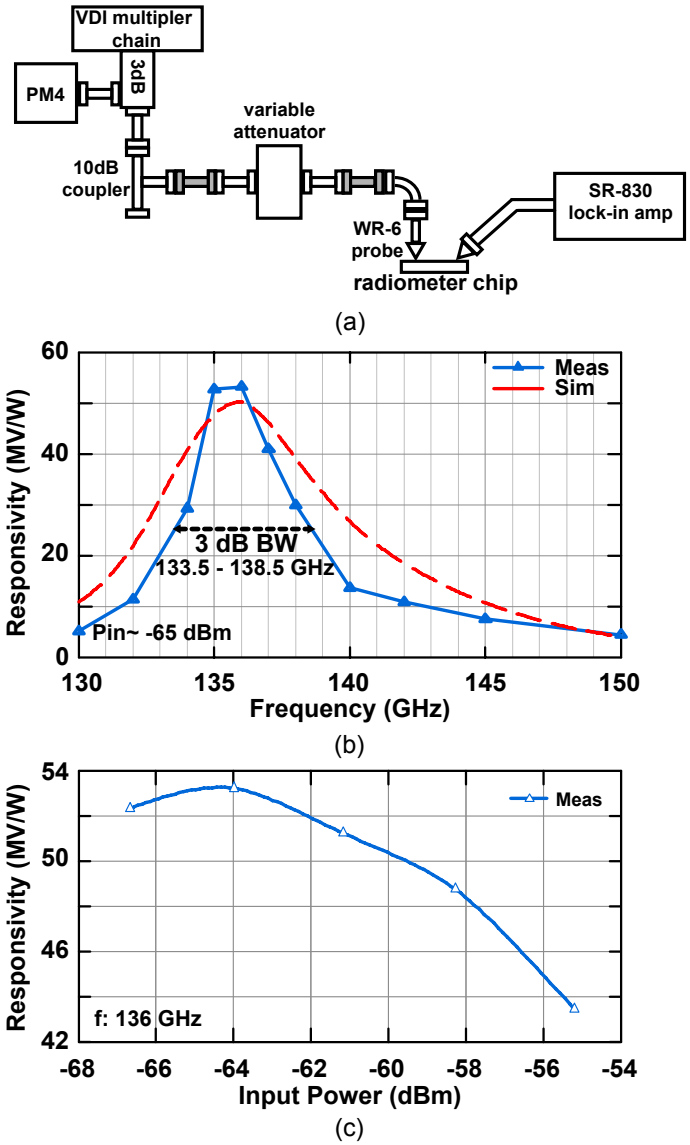


Figure 3.19: (a) Responsivity measurement setup, (b) measured and simulated radiometer responsivity vs. frequency (Pin=-65dBm), and (c) measured responsivity versus input power (f=136 GHz).

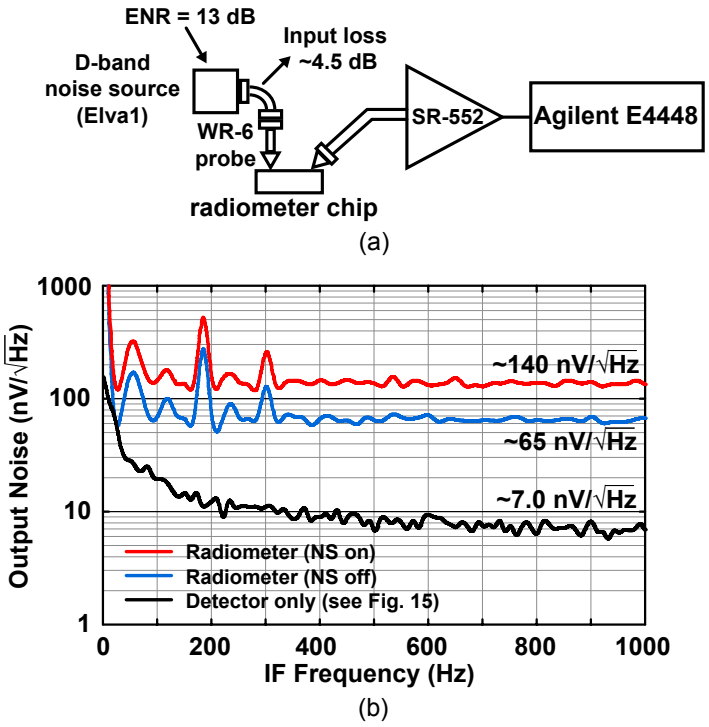


Figure 3.20: (a) Radiometer noise measurement setup, and (b) output noise voltage spectrum for radiometer and detector only.

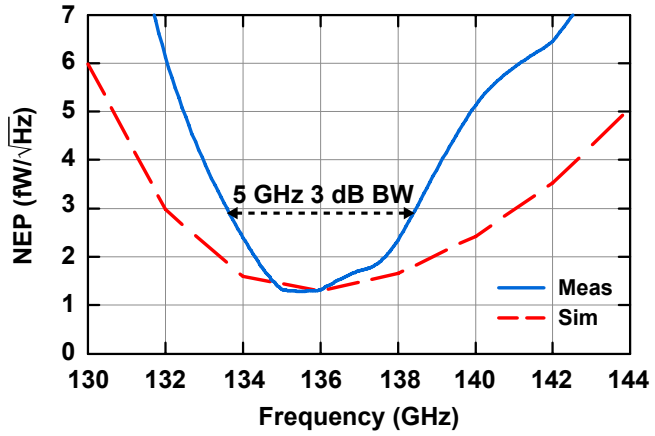


Figure 3.21: Measured and simulated single-chip radiometer NEP.

amplifier (op-amp) [67]. As usual, the gain of the op-amp is de-embedded from the measurements. Fig. 3.22(b) presents the radiometer DC response for various noise input levels. It should be noted that the input loss is ∼7.5 dB for the attenuator lowest loss state and results in a maximum input noise temperature of 1029K. The DC output voltage slope vs. input noise temperature is ∼5.4 μV/K and is called the "thermal responsivity of the radiometer". This value can be greatly increased by using a low noise op-amp after the on-chip detector (i.e. not deembedding the AD620).

Another low-frequency noise measurement setup is presented in Fig. 3.23. The radiometer output DC voltage is measured using a lock-in amplifier (locked at 100 Hz) for the hot and cold state of the radiometer without using the attenuator. In this case, T_{cold} = 290K, T_{hot} = 2053K, and the DC voltage difference is double that of the previous setup in Fig. 3.22.

3.4.3 Radiometer System Characterization

Effective Noise Bandwidth

The radiometer effective noise bandwidth can be determined from the LNA gain, also called the pre-detector gain in Tiuri's paper [50]. Using the LNA measured S_{21} and integrating the gain for the whole D-band, the radiometer effective noise bandwidth is calculated as:

$$B_{RF} = \frac{\left[\int_0^\infty G(f)df\right]^2}{\int_0^\infty G(f)^2 df} = \frac{\left[\int_{110GHz}^{170GHz} S_{21}(f)df\right]^2}{\int_{110GHz}^{170GHz} S_{21}(f)^2 df} \approx 11.8GHz \tag{3.4}$$

The three-stage amplifier forms a three-pole filter system due to the interstage networks. According to [50], the effective noise bandwidth can be approximated by multiplying the 3-dB gain bandwidth with 1.76. This approximation for the on-chip

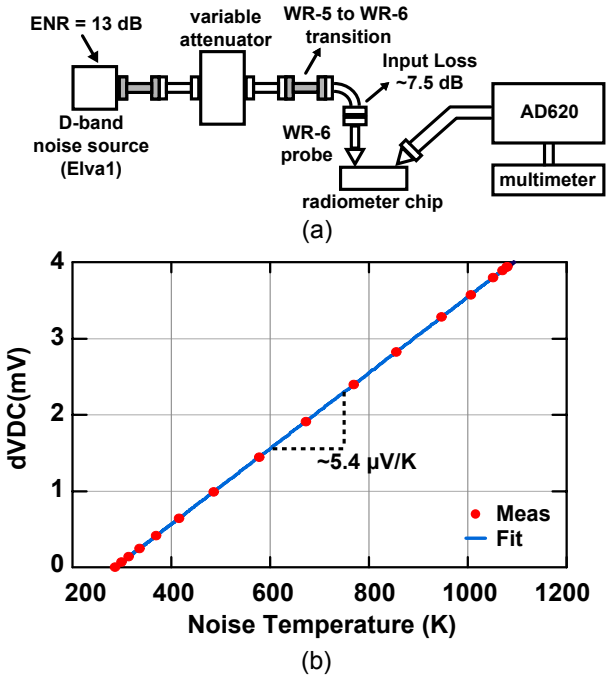
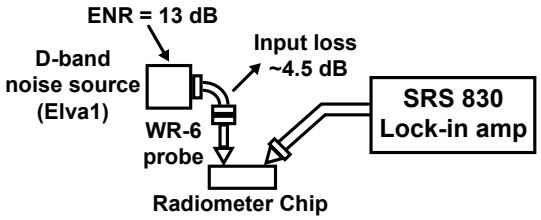


Figure 3.22: Radiometer DC measurement for $\delta V/dT$ characterization.



V_{out} (NS: Off)	V_{out} (NS: On)	V_{diff}
1.55 mV	9.77 mV	8.22 mV

Figure 3.23: Radiometer lock-in amplifier measurements for $\delta V/dT$ and noise bandwidth characterization.

radiometer results in ∼10 GHz, which is close to the calculated value of 11.8 GHz from the S_{21} measurements.

System Noise Temperature and Noise Figure

The Y-factor calculations are performed using the output noise voltage measurement shown in Fig. 3.20:

$$NF_{sys} = ENR - L_{RF} - 10log(Y-1) \tag{3.5a}$$

$$T_{sys} = T_o(F-1) \quad \text{and} \quad Y = \frac{T_{hot}}{T_{cold}} \tag{3.5b}$$

The Y-factor is determined to be 2.15. Assuming an ENR of 13 dB and 4.5 dB setup loss at the input (T_{cold} = 290K, T_{hot} = 2053K), the radiometer NF is calculated as ∼7.9 dB, and the corresponding system noise temperature is T_s=∼1490K.

NETD

The NETD is calculated by various methods using both the low and high frequency measurement results to verify the validity of the measurements. First, using (3.2), the Y-factor measurement results, and the effective noise bandwidth calculated above (B_{RF}=11.8 GHz), the NETD is determined to be 0.25K for τ = 3.125 ms.

The NETD can also be expressed as [22]:

$$NETD = \frac{v_{no}}{k\sqrt{2\tau}V_{out,DC}} 10^{(-204+ENR-L_{RF})/10} \tag{3.6}$$

where, v_{no} is the radiometer output noise voltage density ($V/\sqrt{\text{Hz}}$) at the offset frequency of 1/2τ (noise source off), and $V_{out,DC}$ is the radiometer DC output voltage difference (noise source on). Plugging in the results from the DC measurements (V_{diff} from Fig.

3.23) and the output noise measurements (Fig. 3.20), NETD is determined to be ∼0.21K (τ = 3.125 ms).

The NETD can also be determined using the NEP measurements. The relationship between the NETD and the NEP for the radiometers is [52]:

$$NETD = \frac{NEP}{kB\sqrt{2\tau}} \tag{3.7}$$

The measured average NEP in the noise-bandwidth is ∼3.35 fW/Hz$^{1/2}$, and using (3.7), the NETD is calculated as ∼0.26K. All three methods result in NETD values of ∼0.25K.

Table 3.2 presents a comparison of recent SiGe and CMOS radiometers, together with the classical work from HRL on III-V radiometer chip-sets. It is seen that the D-band SiGe radiometer results in state-of-the-art performance, even when compared to W-band systems.

3.5 Conclusion

A low-noise 136 GHz on-chip radiometer with compact size and state-of-the-art performance was demonstrated in a commercial 90 nm SiGe BiCMOS process. The radiometer NETD is ∼0.25K, and is, to the best of our knowledge, the lowest thermal resolution reported at D-band using silicon technologies. The low flicker-noise characteristics show that the SiGe radiometer is suitable for high resolution imaging applications and can replace III-V systems with lower cost and higher integration opportunity.

3.6 Acknowledgements

This work was supported in-part by Professor Gabriel M. Rebeiz Chair Funds at the University of California, San Diego.

Table 3.2: Radiometer Performance Summary & Comparison

	Frequency (GHz)	RF Noise BW (GHz)	NETD (K) @f_{off}(Hz),τ(ms)	P_{DC} (mW)	NEP (fW/Hz$^{1/2}$)	R (MV/W)	LNA Gain (dB)	T_s (K)
This work	**136**	**11.8**	**0.25** (@160 Hz, 3.125 ms)	**47.2**	**1.4**	**52.0**	**36**	**1295**
[22] (SiGe)	165	10.0	0.35 (@160 Hz, 3.125 ms)	95.0	14.0	28.0	>35	1645
[23] (CMOS)	140	21.0	1.50 (@-, 30 ms)	152.0	26.0	1.2	31	-
[52] (SiGe)	94	20.0	0.69 (@10 KHz, 30 ms)	34.8	23.0	2.5	24	-
[53] (SiGe)	94	26.0	0.40 (@-, 30 ms)	200.0	10.0	43.0	30	-
[51] (InP+AlSb)	90	20.0	0.45 (@-, 3.125 ms)	40.0 mA*	-	∼35.0	31	796
**Only LNA bias is stated without V_{CC}.*								

Chapter 3 is mostly a reprint of the material as submitted to IEEE Transactions on Microwave Theory and Techniques, 2015. Tumay Kanar; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 4

X- and K-Band SiGe HBT LNAs with 1.2 dB and 2.2 dB Mean Noise Figures

4.1 Introduction

SiGe and CMOS technologies have seen tremendous improvement over the past 10 years, and current processes can result in an f_t and f_{max} of 200-300 GHz [68–71]. The SiGe technology is especially important since it comes with a thick copper back-end and thick dielectric layers, which result in on-chip inductor with a Q of $\sim$12 at 10-20 GHz. The advances in device performance and back-end technology not only reduces the power consumption of amplifiers and mixed-signal circuits, but also has the potential to greatly reduce the noise figure of the first-stage amplifier, making it comparable to GaAs designs. For terrestrial applications with an antenna temperature (T_A) of 300^oK, a low-noise SiGe amplifier with high gain and a noise figure of 1.2-2.2 dB at 10-20 GHz is acceptable since the antenna temperature dominates the system noise figure. Such an amplifier can be integrated directly with an LO/down-conversion mixer and an IF amplifier, resulting in a low-cost, low-noise, high performance receiver with no external

components.

This chapter presents the design of low-noise SiGe amplifiers at X and K-band frequencies. The SiGe transistor layout with interconnect metallization to the top level metal is first optimized for best f_t and f_{max}, and then the amplifiers are designed for the lowest noise figure. It is seen that removing the on-chip base inductor with a Q of 10-12 results in better performance than the standard design method of simultaneous power and impedance match. A design method without a base inductor is proposed and implemented, and measurements on X and K-band amplifiers are presented.

4.2 LNA Topology and Technology

Fig. 4.1 presents schematics of the X and K-band LNA together with the biasing circuits. A two-stage design is optimal since it results in more design freedom by allowing a relatively independent noise optimization on the first stage and gain boosting on the second stage. The first stage is a common emitter design and the second stage utilizes a cascode configuration. The cascode stage results in higher gain and isolation than a standard common emitter design, but at the expense of a slightly higher noise, and therefore, it is important that the first stage have enough gain so as to avoid the additional noise from the cascode stage.

The low-noise amplifiers are designed in the Jazz 0.18 μm SBC18H3 SiGe HBT process [68]. The process offers six layers of aluminum metal and high-density stacked MIM capacitors (Fig. 4.2). Grounded CPW transmission-lines have a simulated loss of 0.25-0.47 dB/mm at 8-24 GHz. The HBT transistors have reported f_t and f_{max} nominal values of 240 GHz and 260 GHz, respectively for a 3 μm transistor with metal connections up to metal 1 [72]. However, for low-noise operation, large transistors are needed, and their interconnects up to the top metal have a significant effect on the

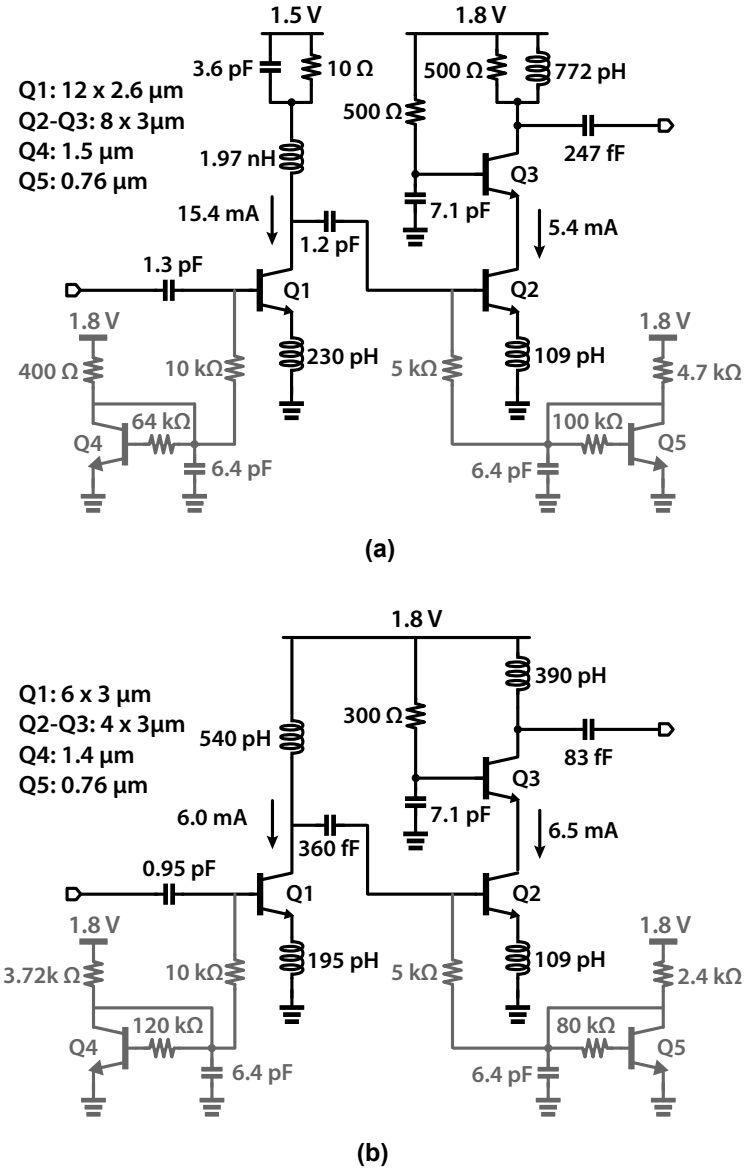


Figure 4.1: (a) Schematic of the (a) X-band LNA, and (b) K-band LNA.

transistor performance.

The use of large-size transistors requires a careful layout optimization. Fig. 4.3 presents the overall layouts of the first stage transistors for both LNAs together with the corresponding parasitics introduced by the interconnects to the top metal layers. Multi-instance transistors are employed in order to achieve the lowest parasitics, and routing in the upper metal layers allows for a lower interconnect resistance and less coupling between the transistor nodes. Cadence simulations with parasitic RC extraction indicate that 12 instances of 2.6 μm and 6 instances of 3 μm transistors result in the optimum noise performance for X and K-band designs, respectively. Since the parasitic resistance at the base is the most critical for noise performance, the base routing is done in the top metal layer (M6). Emitter routing is completed in M5, and being the least critical terminal, the collector is routed in M4. The base and collector nodes are kept away from each other in order to increase the isolation between the input and output nodes. The measured f_t values for the first-stage transistors for X and K-band LNAs agree well with simulations (Fig. 4.4(a)), and are 180-200 GHz which are lower than the nominal value of 240 GHz for a single-instance 3 μm transistor. Fig. 4.4(b) presents the simulated f_t, f_{max}, and F_{min} values for a 12 x 2.6 μm transistor with parasitic extraction for the interconnects up to the top metal layer (as shown in Fig. 4.3). The maximum simulated f_t and f_{max} values for a parasitic extracted transistor are 200 GHz and 160 GHz, respectively, due to the additional interconnect resistance and capacitance at the transistor base.

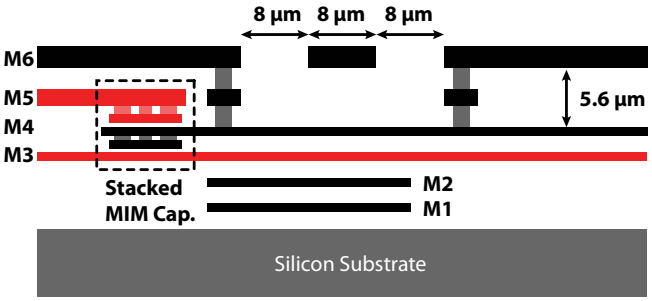


Figure 4.2: G-CPW structure designed in the Jazz SBC18H3 process.

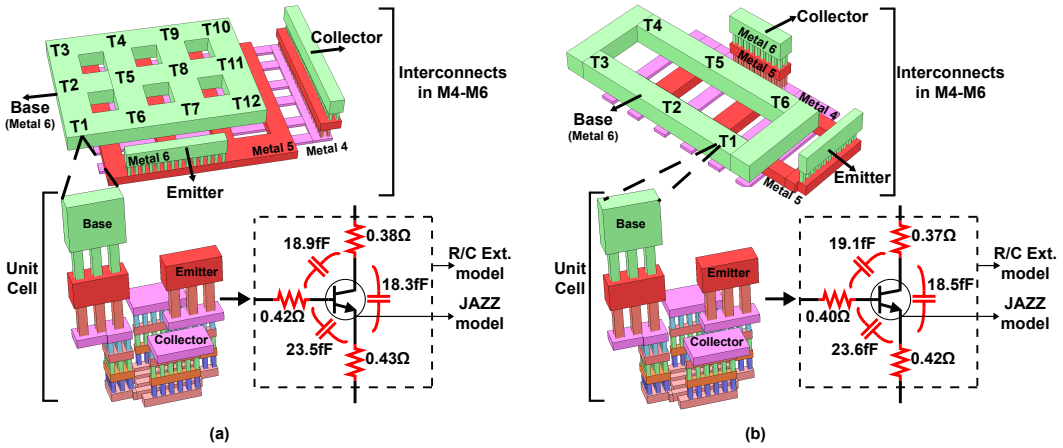


Figure 4.3: First stage transistor layouts and parasitic models: (a) X-band transistor, (b) K-band transistor.

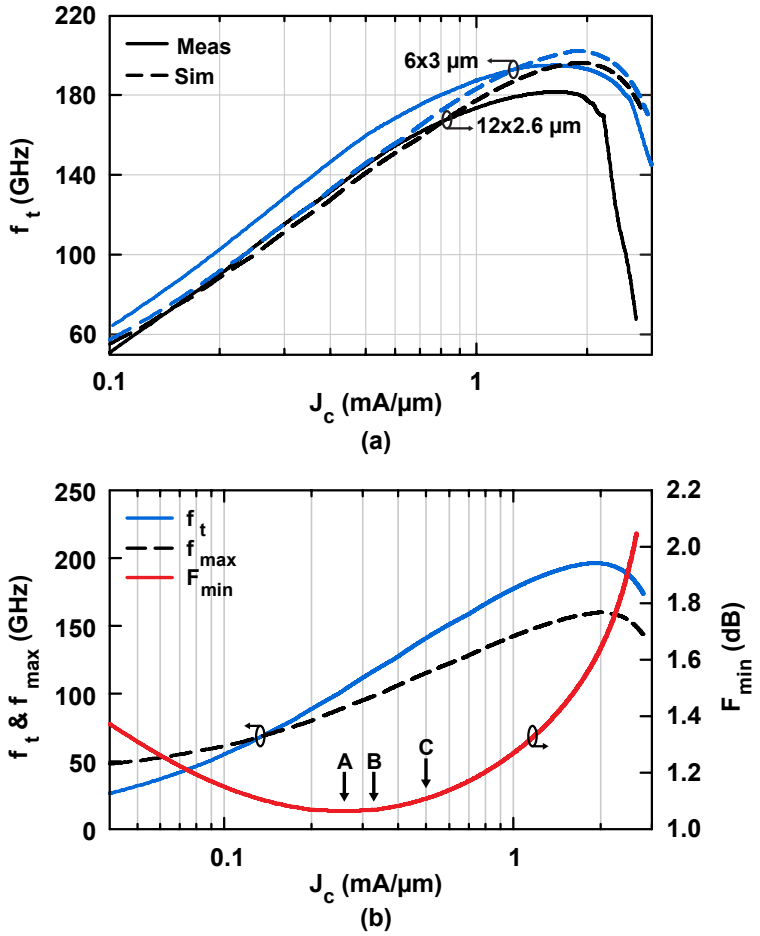


Figure 4.4: (a) Measured and simulated f_t values for first stage transistors of X and K-band LNA, (b) f_t, f_{max}, and F_{min} values for a parasitic-extracted 12x2.6 μm transistor. Point A shows the minimum F_{min} point, and point B and C show the biasing point used for K and X-band LNA designs, respectively.

4.3 Noise Match Optimization with respect to Input Matching

The classical simultaneous noise and power matching method is well explained in [73]. The basic strategy is to size the transistor to achieve an optimum noise source resistance around 50 Ω and cancel the noise correlation susceptance with base and emitter inductors. The emitter degeneration inductor provides a real input impedance of 50 Ω without changing the optimum noise source impedance (if it is lossless). Both emitter and base inductors serve to resonate out the input capacitance for a power match at the input. This method is reconsidered here for low-noise amplifier designs that utilize large size transistors and integrated finite-Q inductors.

Fig. 4.5 presents the small-signal model of a common emitter stage with lossless inductors at the emitter and base nodes. The input impedance is:

$$Z_{in}(s) = r_b + (\frac{1}{g_m R_L})\frac{g_m L_e}{C_\pi} + s[\frac{C_{jc}}{C_\pi}\omega L_e + \omega L_b - \frac{\frac{1}{\omega C_\pi}}{g_m R_L}] \tag{4.1}$$

As (4.1) shows, the emitter inductance directly contributes to the real part of the input impedance, and it cannot be optimized solely for noise performance. On the other hand, the base inductance is used for matching the imaginary part of the transistor base impedance (Z_b) for both noise and power.

Following the classical formalism, the noise figure of a two-port linear system can be expressed as [74]:

$$F = 1 + \frac{G_u + R_n((G_s + G_c)^2 + (B_s + B_c)^2)}{G_s} \tag{4.2}$$

where G_c, B_c, G_s, and B_s are the noise correlation and source termination conductance and susceptance, respectively. R_n, G_u are the noise resistance and uncorrelated

noise conductance for the two-port system.

Assuming that the transistor is sized to provide optimal input conductance, the noise factor of the two-port system can be expressed as [75]:

$$F = F_{min} + \frac{R_n}{G_s}|B_s - B_{s,opt}|^2 \tag{4.3}$$

where F_{min} is the minimum noise factor in a perfect noise-match case, and $B_{s,opt}$ is the optimum source susceptance. Applying the two-port noise model to a common emitter stage results in:

$$B_{s,opt} \approx -\frac{\omega C_\pi}{2g_m r_b + 1} \tag{4.4}$$

and including the base and emitter inductors with their series parasitic resistance model ($r_s = \omega L/Q$), and using the fact that [73]:

$$X_{s,opt_{w/Le}} = X_{s,opt_{w/oLe}} - j\omega L_e \tag{4.5}$$

One finds that (4.3) can be extended as:

$$F = F_{min} + \frac{R_n}{G_s}|\frac{1}{j\omega L_b} + \frac{j\omega C_\pi}{2g_m R_n - \omega^2 C_\pi L_e}|^2 + G_s\omega(\frac{L_b}{Q_{Lb}} + \frac{L_e}{Q_{Le}}) \tag{4.6}$$

where, $R_n \approx r_b + \frac{1}{2g_m}(T = 290^o K)$, and the effect of C_{jc} is neglected. R_n is minimized by the use of large transistors. One can consider R_n as the two-port system's sensitivity factor for the noise mismatch effects. For low values of R_n, the contribution of the input matching elements' loss to noise figure starts to dominate the effect of the noise mismatch. In (4.6), all the parameters except L_b are determined by transistor sizing, bias, and L_e is mostly set by power matching condition. In common emitter stages with large transistors, the noise contribution of the inductor loss is comparable to the other noise

contributors such as the base resistance . Thus, (4.6) can be optimized in terms of L_b. Also, as (4.1) suggests, the inclusion of C_{jc} in (4.6) would transform the imaginary part of the output load to a negative resistance seen at the input, which requires a larger L_e (and a smaller L_b) than the values obtained by using the simple model.

Fig. 4.6 presents a study for the choice of L_b at X-band for a single common-emitter stage. In this case, L_b values are increased from 0 to 225 pH ($Q_{Lb} = 12$) while the emitter degeneration is chosen to provide a power match ($L_e \approx C_\pi/(g_m G_s)$). The F_{min} in Fig. 4.6 refers to the absolute minimum noise figure for the whole two-port system (including the transistor, inductors, and capacitors) assuming a hypothetical perfect noise match condition. It is seen that the F and F_{min} increase with L_b even though large L_b values provide a better noise match (ie., the optimum source reflection coefficient, Γ_{opt}, moves towards the center of the Smith chart). This shows that the noise contribution of the base inductor is significant for large transistor designs and should be considered in noise optimization. Using (4.6) and the case study in Fig. 4.6, it is shown that a lower noise figure can be achieved for large transistor sizes if the on-chip base inductor, required for optimum noise matching, is not employed.

4.4 Design

4.4.1 Noise Figure Optimization

The first stage in both LNAs is designed following the optimization procedure described in section III. The transistor sizes are chosen to provide an optimum noise source impedance with a 50 Ω real part. The emitter degeneration inductance is chosen to provide a reasonable input power match, and its Q value is maximized using a custom layout.

The first stage transistors have a base resistance of $r_b \sim 4$ Ω and 10 Ω for X

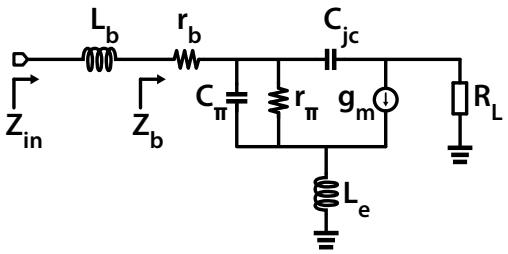


Figure 4.5: Small-signal model of a common-emitter stage with lossless emitter degeneration and base inductance.

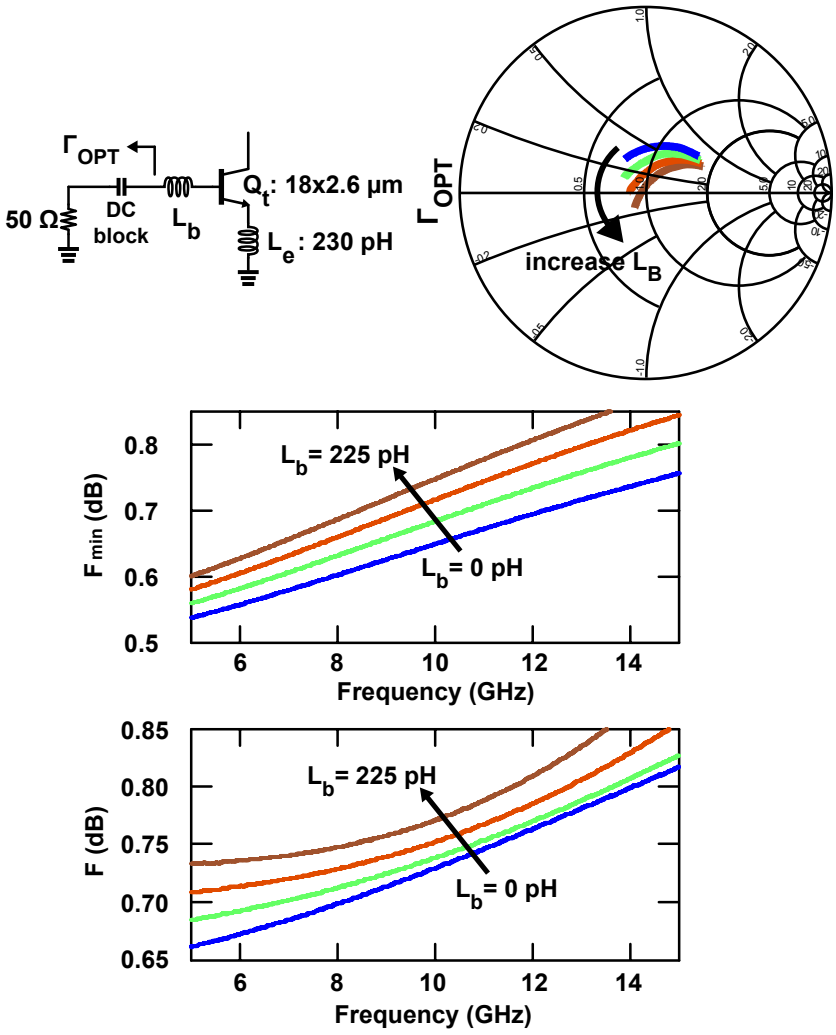


Figure 4.6: Change of noise figure with increasing value of L_B (0-225 pH) for optimal noise match (Q_{Lb}=12).

and K-band designs, and the inductor Q values are $\sim$ 12 at 10-20 GHz. Fig. 4.7(a) and 4.8(a) present the noise mismatch for the X- and K-band LNAs, respectively. Since both Γ_{opt} and Γ_s are on the 50 Ω circle for each LNA, the noise mismatch is only due to the lack of a base inductor. The required inductance values for optimum noise matching are determined to be 500 pH for X-Band and 250 pH for K-band LNAs, and a series RL model is used for simulations with an inductor Q values of 8, 12, and 16 (Fig. 4.7). For the X-band LNA, a base inductor with a Q of 16 still results in a higher noise figure than a design without a base inductor (Fig. 4.7(b)). For the K-band LNA, a Q of 8-12 results in a higher noise figure than without a base inductor, but a Q of 14-16 results in overall better performance (Fig. 4.8(b)). One can conclude that the use of on-chip inductors for large transistor designs does not improve the noise figure even though it provides a better noise match condition, and high quality inductance of bond-wires should be utilized for noise and power match at the input whenever it is possible.

Fig. 4.9 presents the noise figure with respect to the base inductance value at 10 GHz and 20 GHz. It is seen that lower noise figures are achieved for lower inductor values in both LNA designs. The minimum noise figure for the K-band LNA occurs at $L_b \approx$ 100 pH (Q_{Lb}=12) but, considering the fact that the first order inductor model used in the simulations actually underestimates the parasitic effects, and an even smaller inductor would be needed for optimum noise performance, the implementation of such a small inductor at the input is avoided for practical purposes.

4.4.2 Overall Design Procedure

Fig. 4.4(b) presents the biasing scheme for low noise operation. Absolute minimum F_{min} is achieved around a collector current of 0.25 mA/μm (point A), and this scheme holds for various transistor sizes as long as the current density is kept the same. Therefore, bias current can be optimized independent from the transistor size. Even

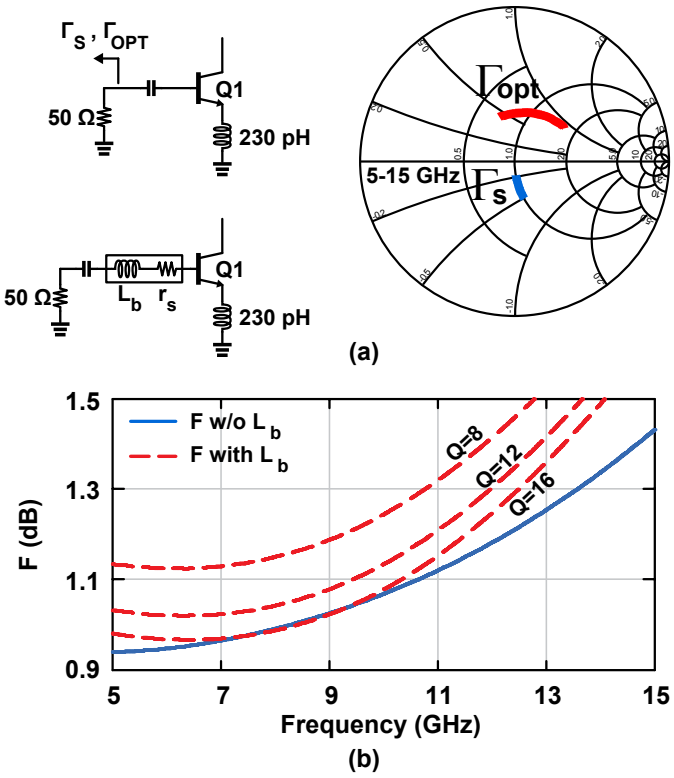


Figure 4.7: (a) Noise matching characteristics for the X-Band LNA (b) F with and without 500 pH base inductor.(Q_{Lb}=8,12,16)

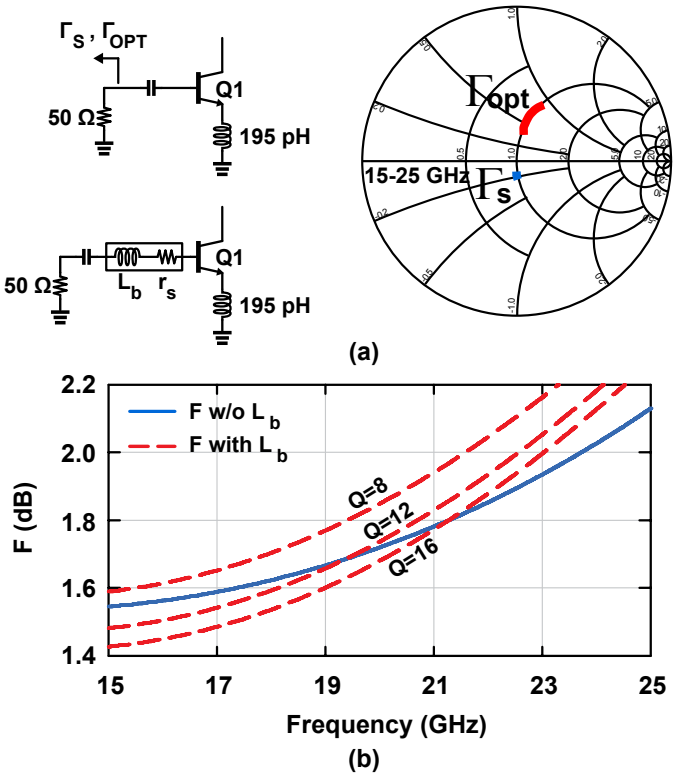


Figure 4.8: (a) Noise matching characteristics for the K-Band LNA (b) F with and without 250 pH base inductor.(Q_{Lb}=8,12,16)

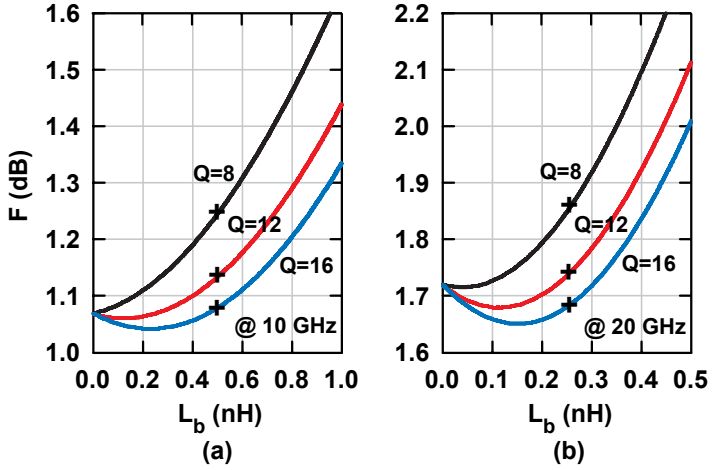


Figure 4.9: Noise figure vs. base inductance value for (a) X and (b) K-band LNAs.('+' indicates the inductor value for perfect noise matching condition.)

though minimum F_{min} is achieved around a collector current of 0.25 mA/μm, the first stage is biased at 0.33 mA/μm and 0.5 mA/μm for the K and X-band LNAs, respectively (points B and C) in order to enhance the first stage gain without degrading its noise performance significantly. The gain and noise figure analysis for the cascaded stages is shown in Fig. 4.10. While the first stage is optimized for noise figure with reasonable gain, the second stage is mostly optimized for a higher gain. This analysis assumes a 50 Ω interstage impedance without any mismatch, which is not the case in the real design. Therefore, the cascaded analysis slightly overestimates the overall simulated gain but it provides an accurate estimate for the overall simulated LNA noise figure.

Interstage matching is another important design aspect if large size transistors are used in a common-emitter configuration. Large transistors provide smaller isolation between their base and collector nodes due to a large C_{jc}. Referring back to (4.1), the load impedance that the first stage sees affects the input impedance through C_{jc}. Therefore, interstage matching is optimized to provide an optimal load impedance for the first stage to achieve the best possible power match at the input of the first stage without using a base inductor at the input stage.

The inductor used at the emitter degeneration is designed to give a high Q factor for low noise contribution. The collector inductor, on the other hand, is optimized to result in a relatively low Q for stability purposes. Since any noise contribution from collector inductor is effectively divided by the first stage gain, its contribution to the overall noise figure is not significant. The use of narrow lines and smaller gaps makes it more compact in terms of area while providing enough parasitic resistance to avoid stability issues. For lower frequency stability, the X-band amplifier utilizes a parallel RC (3.6 pF and 10 Ω) circuit to further decrease the Q of the first stage collector inductor. More information is given in the corresponding section.

Fig. 4.11 presents the microphotographs of the fabricated X- and K-band LNAs.

The X-band LNA occupies an area of 678 x 675 μm^2 while the K-band LNA is 678 x 575 μm^2, both including RF and DC pads.

4.5 Measurements

The S-parameters are measured on-chip with an Agilent E8364B network analyzer using an SOLT calibration up to the probe tips. The power consumption is 32.8 mW and 22.5 mW for the X- and K-band LNAs, respectively. The measured peak gain is 24.2 dB at 8.5 GHz, with a 3-dB bandwidth of 6.4-11 GHz for the X-band LNA (Fig. 4.12a). The K-band LNA results in a measured peak gain of 19 dB at 19.5 GHz with a 3-dB bandwidth of 16-24 GHz (Fig. 4.12b). The X-band LNA gain is also measured at different temperatures, and the peak gain changes only by 1.5 dB from 25^{o}C to 105^{o}C (Fig. 4.13). Both amplifiers provide a good input and output return loss over their operation range and the measured results agree well with the simulated values (Fig. 4.14).

The noise figure measurements are done using an Agilent 346C noise source and the noise figure measurement personality of the Agilent E4448A spectrum analyzer (Fig. 4.15). A 32 dB gain preamplifier is used in order to decrease the effect of the noise floor of the spectrum analyzer. Measuring a noise figure around 1 dB at room temperature has some inherent difficulties due to the setup accuracy limits. First, a noise source with a low excess noise ratio (ENR) results in more accurate F values. The Agilent 346C ENR is 15 dB, and in order to lower its ENR for X-band measurements, a 10-dB attenuator is added after the noise source to result in an overall ENR of 5 dB. Also, a 6 dB attenuator is used between the DUT and the preamplifier in order to enhance the impedance matching between the two amplifiers and to avoid saturation of the spectrum analyzer. Using the embedded uncertainty calculator tool of the spectrum analyzer, the accuracy limit of this

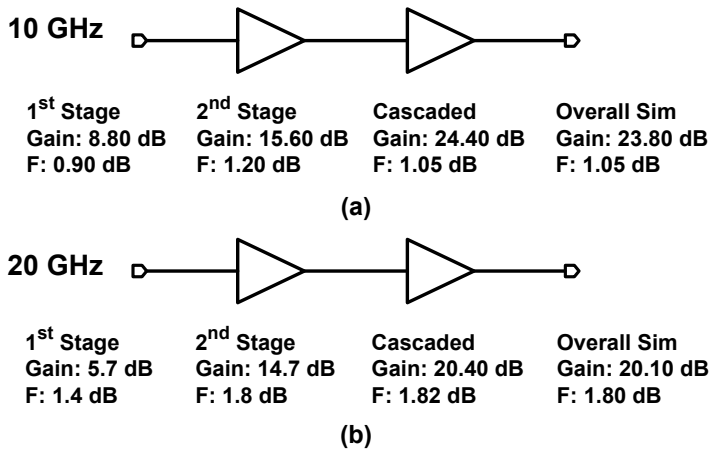


Figure 4.10: Gain and noise figure analysis for cascaded stages: (a) X-band LNA, (b) K-band LNA.

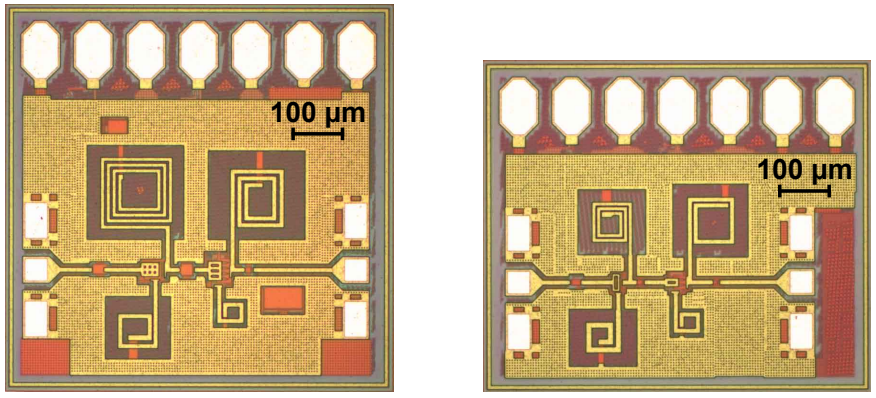


Figure 4.11: Chip microphotographs: (a) X-band LNA: 678 μm x 675 μm, (b) K-band LNA: 678 μm x 575 μm.

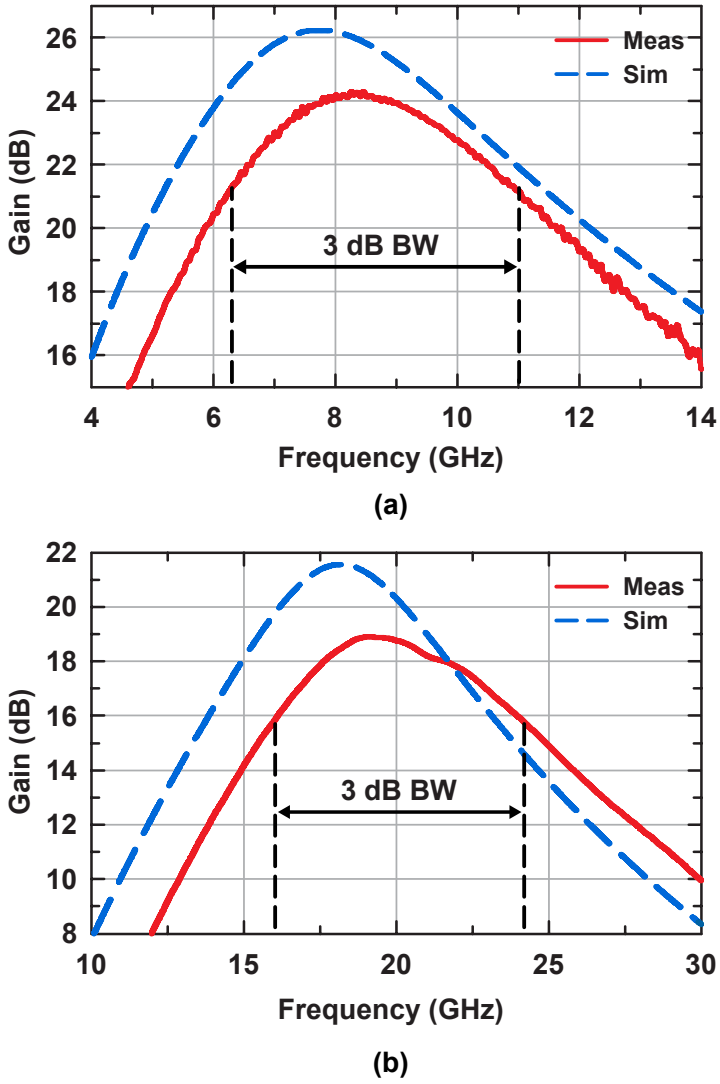


Figure 4.12: Gain vs. frequency for X and K-band LNAs.

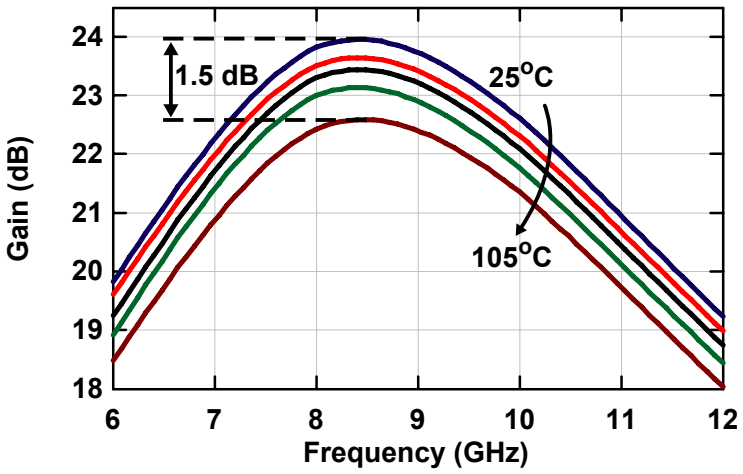


Figure 4.13: Measured gain vs. temperature for the X-band LNA.

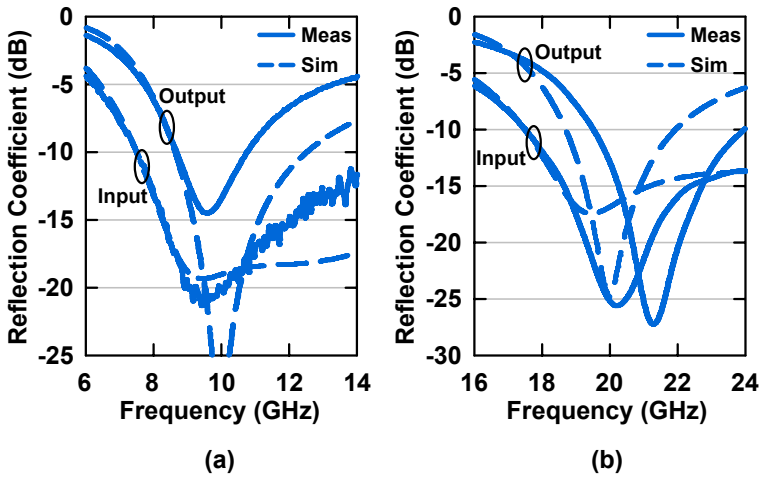


Figure 4.14: Simulated and measured input and output return loss for X and K-band LNAs.

setup is determined to be +/- 0.15 dB [76]. Fig. 4.15(b) shows that the measured noise figures are within the accuracy limits. A spline fit is used to determine the mean F, and a mean noise figure of 1.2 dB is achieved at 6.4-11 GHz. It is determined from the Jazz H3 process characterization measurements that the GSG pads with an underneath N-well passivation layer introduce a higher loss than what is simulated in Sonnet. Therefore, 0.05-0.10 dB is added to the noise figure simulations at 6-14 GHz to account for the GSG pad loss at the input port.

A similar noise figure measurement setup is used for the K-band LNA (Fig. 4.16(a)). This measurement does not require a low ENR noise source since the amplifier itself has a noise figure of $\sim$2 dB. A 6 dB attenuator is utilized between the DUT and preamplifier and the accuracy limit is determined to be +/- 0.2 dB. Fig. 4.16(b) presents the measured and simulated noise figures and a spline fit for the measurements. A mean noise figure of 2.2 dB is achieved at 16-24 GHz. Note that 0.11-0.20 dB is added to the noise figure simulations to account for the GSG pad loss.

The measured input and output P_{1dB} for the X-band LNA are -19 dBm and +2.5 dBm at 10 GHz (Fig. 4.17(a)). The measured IIP_3 is -11 dBm at 10 GHz. P_{1dB} and IP_3 measurements are performed at various frequencies, and the results agree well with simulations (Fig. 4.17(a)). Fig. 4.17(b) presents the measured P_{1dB} and IP_3 values for the K-band LNA, and also agree well with simulations. The X and K-band LNAs deliver a saturated power of 7 and 6 dBm at 10 and 20 GHz, respectively.

Table 4.1 presents a comparison with published LNA results at X and K-bands. It is seen that this work has the best reported noise figure using SiGe and CMOS technologies.

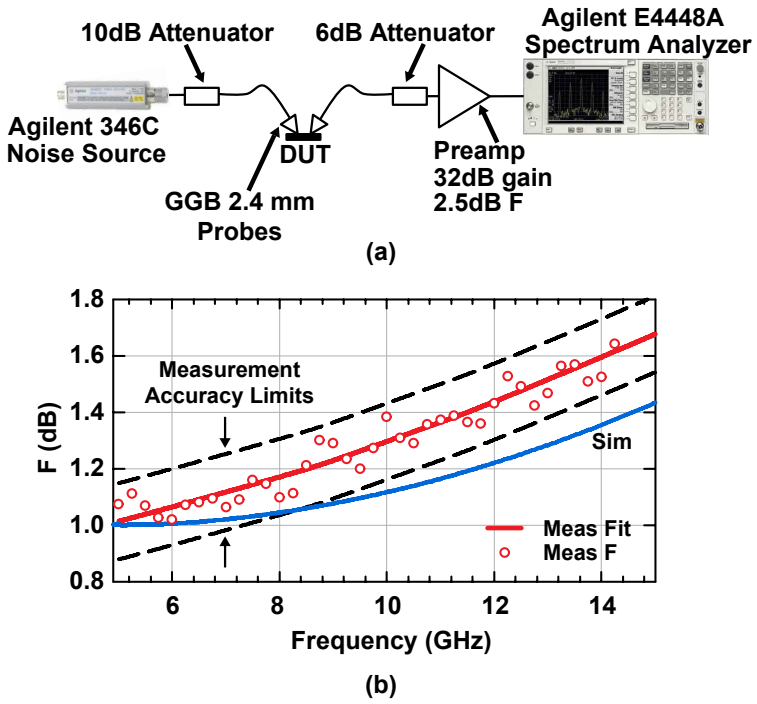


Figure 4.15: X-band noise figure measurements: (a) Noise figure measurement setup (b) Simulated and measured F with accuracy limits.

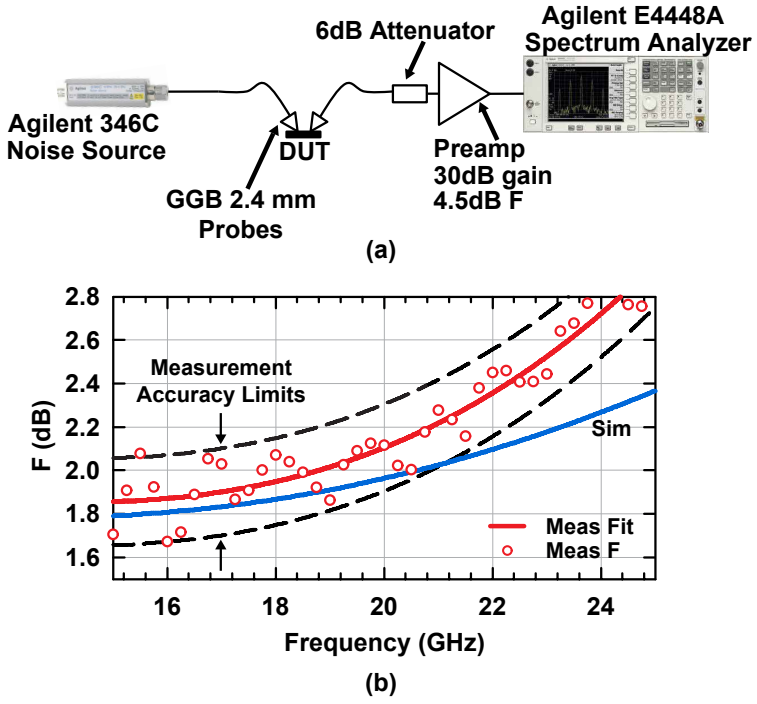


Figure 4.16: K-band noise figure measurements: (a) Noise figure measurement setup (b) Simulated and measured F with accuracy limits.

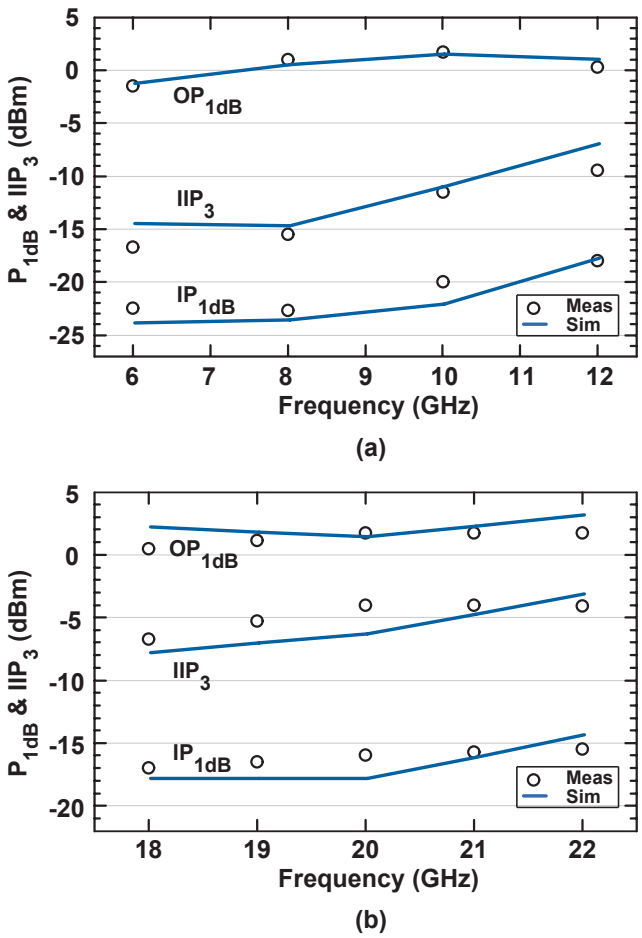


Figure 4.17: Measured and simulated P_{1dB} and IIP_3 values for X and K-band LNAs.

4.6 Inductor Design and Measurements

Fig. 4.18 presents the inductors used in the first stage of the K-band LNA. Custom design inductors utilize dummy-fill exclusion in order to achieve higher Q factors. Their metal width and gap are optimized using Sonnet EM modeling [77] to achieve the required inductance and Q values. Since the inductors are critical for low noise amplifier design, inductance and Q factor measurements are also performed on an inductor test cell. Fig. 4.19 presents the simulated and measured inductance and Q values for the 540 pH inductor used in the first stage collector node of the K-band LNA. It is shown that a Q factor of $\sim$ 12.5 is achieved at K-band. As is seen, the measured and simulated values agree well.

4.7 Conclusion

This chapter presented record low-noise X- and K-band amplifiers using an advanced SiGe technology. The removal of the base inductor with a Q of 10-12 results in better performance than the standard simultaneous power/noise match design. The gain, noise figure and linearity measurements all agree well with simulations, showing the maturity of the device modeling and the design technique.

4.8 Acknowledgements

This work was supported in part by TowerJazz under a subcontract, under the Defense Advanced Research Projects Agency (DARPA) GRATE Program.

Chapter 4 is mostly a reprint of the material as it appears in IEEE Transactions on Microwave Theory and Techniques, 2014. Tumay Kanar; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

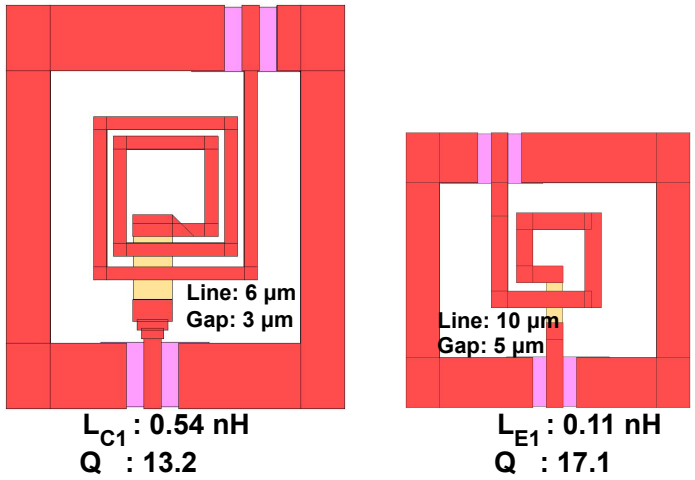


Figure 4.18: First stage inductors for the K-band LNA.

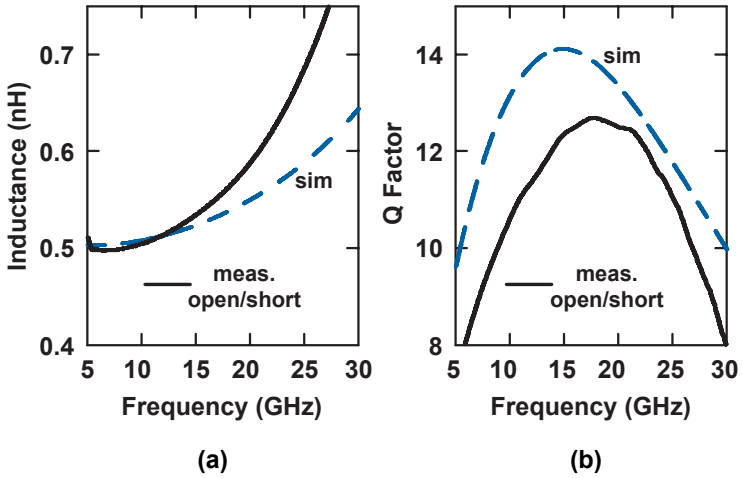


Figure 4.19: Measured and simulated inductance and Q factors for K-band amplifier's first-stage collector inductor. Open/short deembedding is used [2].

Table 4.1: LNA Performance Summary & Comparison

X-Band LNA							
	Technology	Frequency (GHz)	Power Consumption (mW)	Gain (dB)	Mean F (dB)	IP_{1dB} (dBm)	IIP_3 (dBm)
This work	**0.18 µm SiGe BiCMOS**	**6.4-11.0**	**32.8**	**24.2**	**1.20**	**-19**	**-11.0**
[78]	0.13 µm SiGe BiCMOS	8.5-10.5	15.0	19.0	1.36	-10	+0.8
[79]	0.18 µm SiGe BiCMOS	8.0-12.0	33.6	24.2	1.68	-	-7.0
[80]	0.18 µm RF-CMOS	8.1-9.5	27.6	20.5	1.85	-21	-
[81]	70 nm GaAs MMIC	7.0-11.0	62.2	29.0	1.10	-27	-
K-Band LNA							
	Technology	Frequency (GHz)	Power Consumption (mW)	Gain (dB)	Mean F (dB)	IP_{1dB} (dBm)	IIP_3 (dBm)
This work	**0.18 µm SiGe BiCMOS**	**16-24**	**22.5**	**19.0**	**2.20**	**-16.0**	**-4.0**
[82]	0.18 µm SiGe BiCMOS	22-26	41.6	12.0	3.51	-8.7	-1.8
[83]	0.18 µm SiGe BiCMOS	23-32	13.0	12.0	5.52	-	-5.5
[84]	0.25 µm SiGe BiCMOS	16-26	20.0	11.0	4.38	-	-
[85]	45 nm CMOS SOI	16-24	32.5	19.5	2.20	-18.5	-8
[86]	90 nm RF-CMOS	18-23	19.2	8.6	3.60	-	+5.6
[87]	0.18 µm CMOS	21-25	18.0	13.7	3.88	-8.0	+1.5
[88]	0.15 µm InGaP/InGaAs HEMT	23-30	37.5	14.5	1.75	-	-

Chapter 5

Conclusion

The thesis presented built-in self-test (BIST) circuits for wide-band phased array systems, and high performance circuits for millimeter-wave radiometry and low-noise applications. First, a 2-15 GHz BIST system that can perform relative phase measurements and relative and absolute gain measurements on phased-array channels was presented in Chapter 2. Wide-band BIST technique, including design challenges, was studied in detail, and a multi-phase LO self-correcting algorithm for the I/Q mixers was introduced. The BIST measurements agreed well with the VNA S-parameter measurements over the operating bandwidth. The thesis demonstrated that the wide-band BIST system will become an integral part of a new generation of wide-band phased arrays.

Chapter 3 presented a D-band total power radiometer centered at 136 GHz for low atmospheric attenuation. Low-noise design techniques and radiometer optimization were presented in detail. Independent methods have been used for radiometer characterization and measurements. The radiometer resulted in a thermal resolution (NETD) of 0.25K with 3.125 ms integration time which is the lowest NETD reported in silicon technologies at D-band.

Chapter 4 presented X- and K-band low-noise amplifiers (LNA) with 1.2 dB and

2.2 dB mean noise figure. A noise optimization method for large size SiGe transistors with respect to on-chip inductor loss was proposed and implemented. Both LNAs demonstrated the record performance at the time of publication.

5.1 Future Work

In chapter 2, a wide-band BIST system has been demonstrated with an on-chip ring VCO. The BIST measurements for this implementation were performed with a free-running VCO. It is well-known that ring oscillators inherently have a high level of jitter, and it would adversely affect the accuracy of the BIST measurements with short integration times. Therefore, an on-chip oscillator with an integrated phase-locked-loop (PLL) would result in a more robust and lower noise measurement system. The embedded PLL with additional phase-detectors and multi-phase test signals may also introduce opportunities for additional BIST features, such as noise characterization of the phased-array channels as it is possible to discriminate the phase noise from amplitude noise if the phase data is available.

In chapter 3, a D-band total power radiometer has been presented with only LNA and detector on-chip. The promising performance of this system suggests that a more complete system with competitive specification would be implemented with high-efficiency on-chip antennas at the input and low-noise op-amps and integrators at the output.

Appendix A

A 16-24 GHz CMOS SOI LNA with 2.2 dB Mean Noise Figure

A.1 Introduction

A K-band LNA is also implemented in 45 nm SOI technology in order to compare its performance with the SiGe and III-V designs. This chapter presents the details of the SOI LNA design and gives the comparison with other technologies.

A.2 Technology

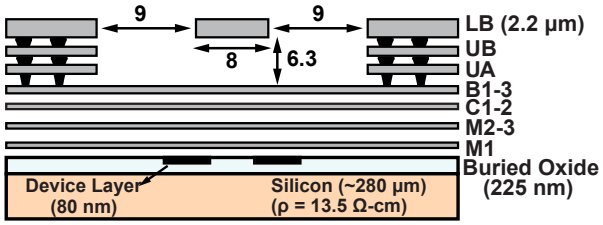
The IBM 45-nm SOI CMOS process offers partially depleted floating-body transistors which decreases the noise coupling to the high resistivity substrate and enables lower noise designs. Due to its lower coupling to the substrate, SOI transistors have inherently better performance at higher frequencies than bulk CMOS counterparts [89], and IBM reports a peak f_t of 485 GHz for the 45-nm CMOS SOI process [90]. However, the main performance limitation comes from the parasitics introduced by their interconnec-

tions used to connect the transistor to the top metal layer. Therefore, a careful transistor layout is very important so as not to degrade the f_t and f_{max} as referenced to the top metal layer. The IBM 45-nm process is composed of 11 metal layers, all copper except the top aluminum layer, with tungsten vias between the layers. The process stack-up and a 50 ohm grounded coplanar waveguide (GCPW) transmission line is shown in fig. A.1(a). Fig. A.1(b) and A.1(c) present the connections for a 100 x 0.8 μm wide transistor and its extracted parasitic performance values. It is seen that the peak f_t is lowered from 485 GHz (referenced to M1) to 200 GHz (referenced to the top metal). Also, at a bias current of 0.2mA/μm which is used for lowest noise performance, the f_t/f_{max} values are 180 GHz/220 GHz which are still 10x higher than the operating frequency of 20 GHz.

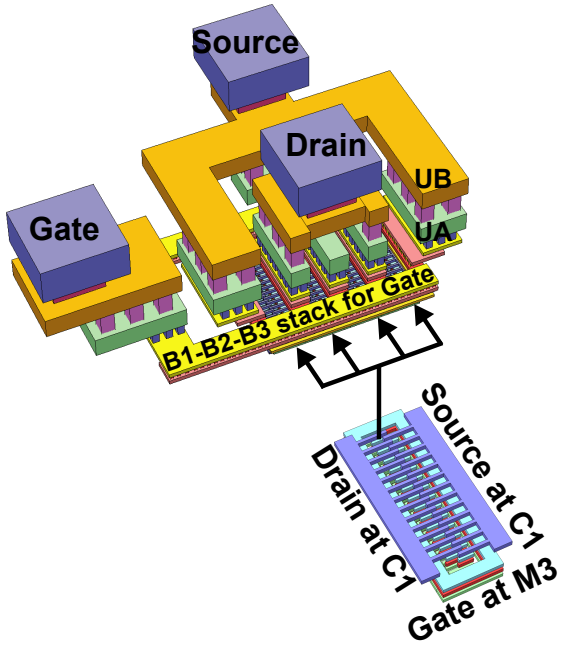
A.3 Design

The two-stage K-band LNA is presented in Fig. A.2. The first stage is mostly optimized for low noise while the second stage is designed to result in a higher gain with a reasonable noise figure (Fig. A.3). Since the gain of the first stage is not high, the noise contribution of the second stage should also be taken into consideration. The common source stage utilizes an 80 μm transistor and is biased at the minimum noise figure point, which is 0.2 mA/μm (see Fig. A.1(c)). The second stage consists of a cascode with 62.5 μm transistors for higher gain and isolation, and is also biased at the minimum noise figure point. V_{dd} for the first stage is set to 1 V while 1.5 V V_{dd} is used for second stage for a higher output swing. Gate bias network is realized using high value resistive dividers.

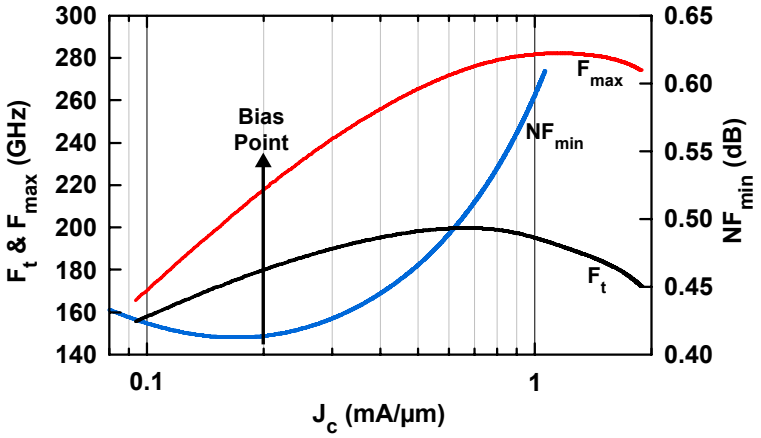
Fig. A.4 presents the optimum reflection coefficient at 10-30 GHz for the first stage transistor with source degeneration. The reflection coefficient that the input matching network provides to the transistor is also shown. It is seen that a wide-band input



(a)



(b)



(c)

Figure A.1: (a) GCPW structure and stack-up of CMOS SOI process, (b) extracted f_t, f_{max}, and nf_{min} values for the first stage transistor (b) Layout of the first stage multi-instance transistor.

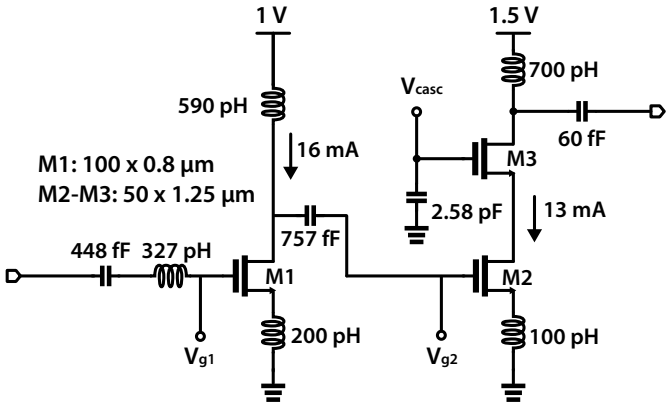


Figure A.2: Schematic of the K-band LNA.

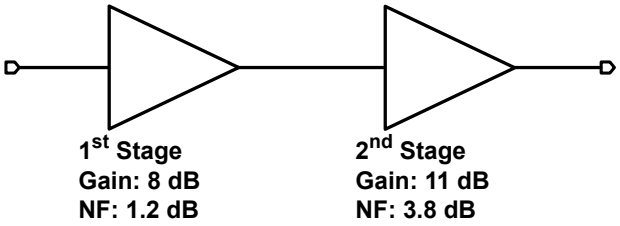


Figure A.3: Gain and noise figure of cascaded stages for the two-stage LNA.

matching is achieved without sacrificing the noise performance significantly. The source degeneration in the first stage is mostly used for stability purposes, while the degeneration in the second stage serves for the interstage impedance match. The interstage impedance match is optimized around 50 Ω and therefore, both stages are well matched to 50 Ω at their input and output ports. Since the loss in the gate path is the most critical for noise figure, a large set of stacked-up metals are used for gate connections (Fig. A.1(b)). Also, drain node is connected to the top metal right above the transistors in order to minimize its coupling to the substrate.

Certain trade-offs need to be considered in order to achieve the lowest noise figure in a CMOS SOI process. MOS transistors present highly capacitive input impedances and their parasitic capacitance is significant when large transistors are used so as to achieve

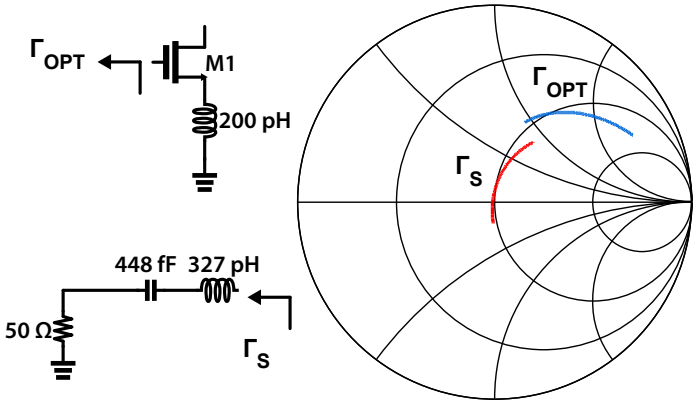


Figure A.4: Γ_{OPT} and Γ_S for the first stage transistor with source degeneration.

smaller gate resistance values. The large transistors can result in high parasitic values which degrade the transistor performance. Therefore, careful attention is placed on the transistor layout as shown in Fig. A.1(b). In this case, 4 discrete instances with 25 fingers are used while keeping the finger width at 0.8 µm so as to result in the best performance from a single transistor (several layouts were considered and this was found to be the best).

As is well know, large transistors result in lower isolation between the transistor nodes, and therefore, the transistor layout is optimized in order to reduce the coupling between its nodes.

The planar inductors used for degeneration and in the input and output matching circuits are also an important aspect of the design. The layout should result in a high Q in order to achieve the lowest noise figure without causing any stability issues. The low metal filling option is also utilized underneath the inductors for a higher Q. Fig. A.5 presents the source and drain inductors. It is seen that a high-Q inductor layout is used in the source degeneration for lower noise contribution, while a lower Q inductor is utilized at the drain for better stability.

Another consideration for stability is the V_{dd} decoupling capacitors.As is well

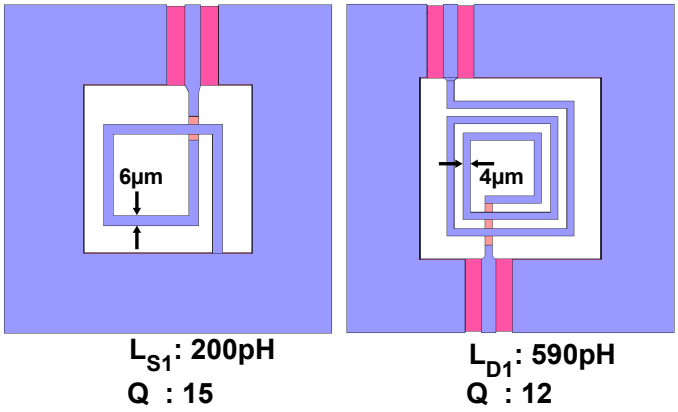


Figure A.5: Custom designed inductors with different Q values.

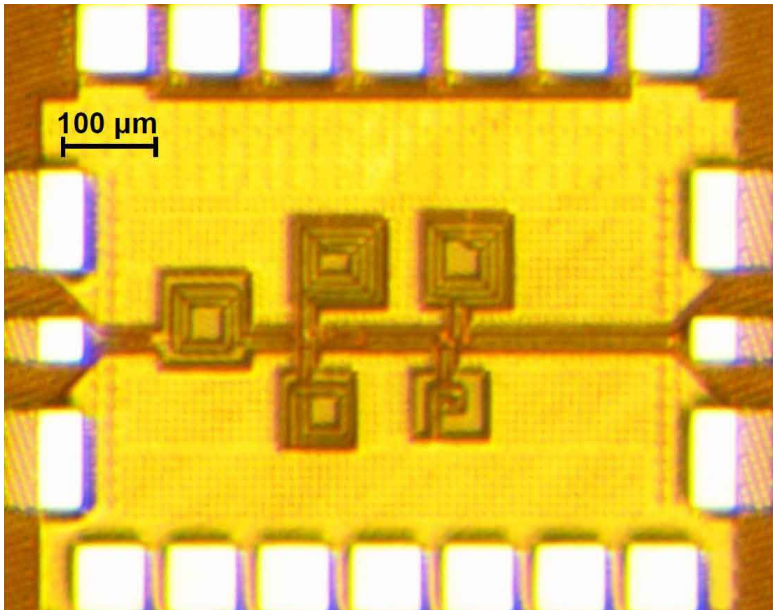


Figure A.6: K-Band LNA chip microphotograph: 770 μm x 675 μm including pads.

known, several decoupling capacitors are used in parallel to provide a proper AC ground path from V_{dd}. Decoupling capacitor Q values are intentionally decreased using 2-5 Ω series resistors in order to prevent any self-resonant effects on the bias line to cause stability problems. Each stage has a total decoupling capacitance of around 120 pF with 2.8 pF instances used in parallel. The LNA is unconditionally stable at 0.1-40 GHz (k>1). The simulated LNA results in a gain of 18 dB at 20 GHz with a noise figure of 1.6 dB,

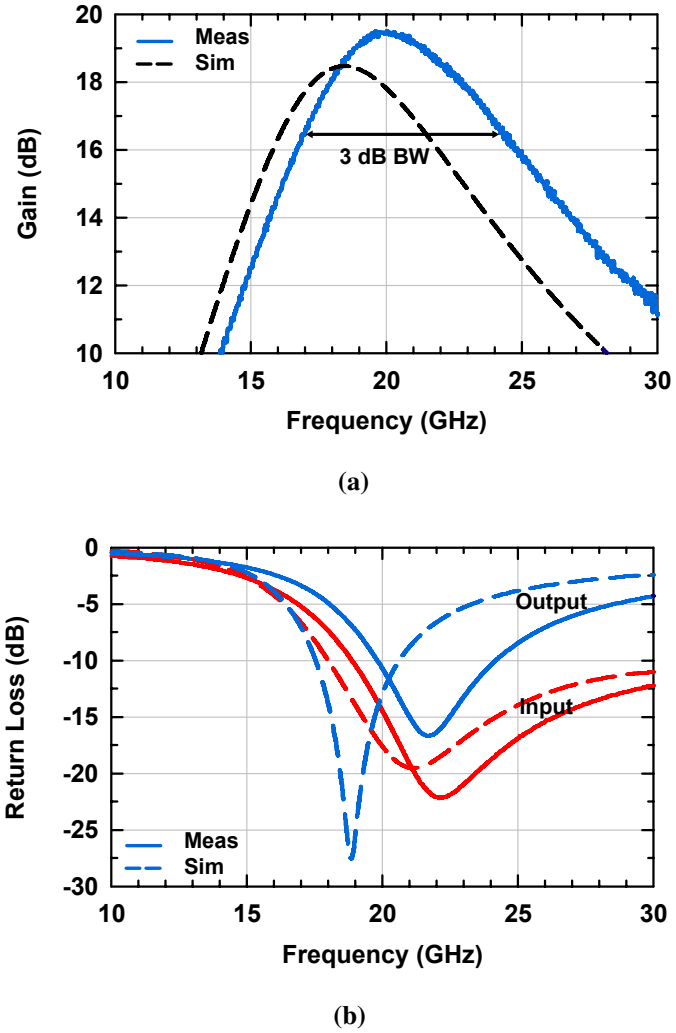


Figure A.7: (a) Measured and simulated gain, and (b) measured and simulated return loss

and a power consumption of 32.5 mW. The LNA occupies 500 x 300 μm^2 without pads, and 770 x 675 μm^2 with pads (Fig. A.6).

A.4 Measurements

The LNA S parameters are measured on-chip using an Agilent E8364B network analyzer and SOLT calibration to the probe tips. The measured peak measured gain at 20

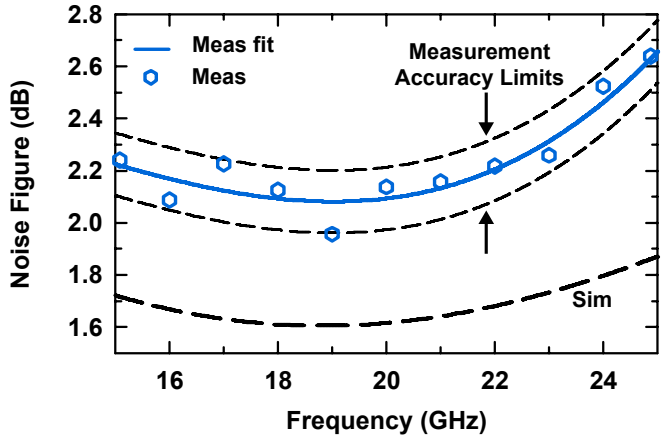
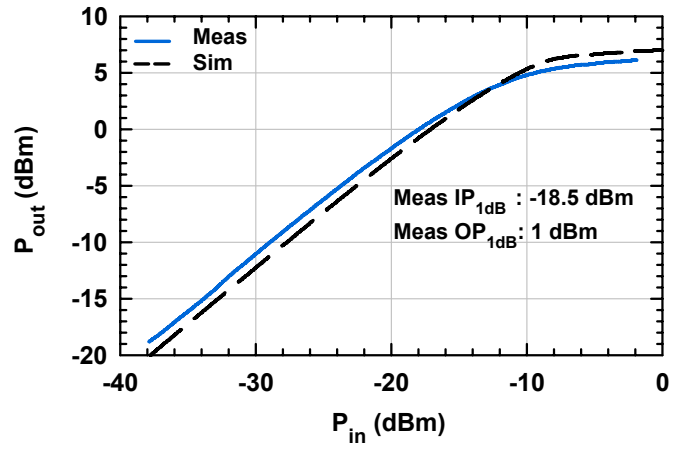


Figure A.8: Measured and simulated LNA noise figure.

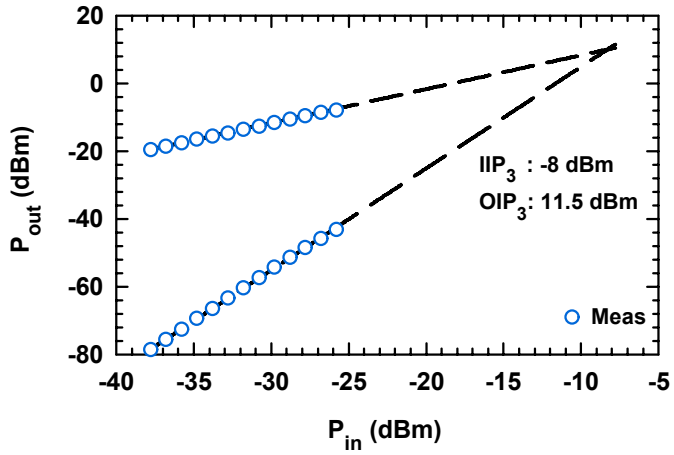
GHz is 19.5 dB with a 3 dB bandwidth of 16-24 GHz (Fig. A.7(a)). The input and output match agree well with simulations and are $<$ -10 dB at 20 GHz (Fig. A.7(b)).

The LNA noise figure is measured using an Agilent 346CK01 noise source and the noise figure personality of the Agilent E4448A spectrum analyzer. A K band preamplifier is used before the spectrum analyzer and this setup results in +/-0.1 dB NF uncertainty [76]. The measured mean NF for this LNA is 2.2 dB in 16-24 GHz range with a minimum value of 2.0 dB at 19 GHz (Fig. A.8). The simulated RF pad loss at 20 GHz is $<$ 0.05 dB whereas the measured loss is around 0.2 dB. The pad loss at the input directly reflects to the noise figure. Taking this into consideration, measured NF values agree well with simulations.

The measured 1 dB gain compression point (P_{1dB}) at 20 GHz is -18.5 dBm and 0 dBm for the input and output ports (Fig. A.9(a)). The LNA is able to provide $>$ +5 dBm when saturated. The measured third order intermodulation products at 20 GHz are -8 dBm and +10 dBm for IIP_3 and OIP_3, respectively (Fig. A.9(b)). Table A.1 presents a comparison with state-of-the-art CMOS and SiGe amplifiers. It is seen that this design provides the best CMOS noise figure to-date, and is very close to the SiGe performance. As expected, the GaAs pHEMT amplifiers are still $\backsim$1 dB better than CMOS and SiGe



(a)



(b)

Figure A.9: (a) Measured and simulated output vs. input power at 20 GHz (b) measured intermodulation products of the LNA at 20 GHz

amplifiers at 20 GHz.

A.5 Conclusion

A two-stage K band LNA is optimized in order to achieve the lowest noise figure in CMOS SOI process in K-band. The CMOS SOI LNA gives a comparable noise performance to SiGe LNA's and shows that CMOS SOI can be used in very low noise

front-ends as an alternative to other technologies.

A.6 Acknowledgments

Appendix is mostly a reprint of the material as it appears on IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), 2013. Tumay Kanar; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Table A.1: Performance Summary

	Technology	Frequency (GHz)	Power Consumption (mW)	Peak Gain (dB)	Min NF (dB)	IP_{1dB} (dBm)	IIP_3 (dBm)
This work	45 nm CMOS SOI	16-24	32.5	19.5	2.0	-18.5	-8.0
[91]	0.13 µm CMOS	20-29	22.1	16.2	3.1	-	-12.0
[92]	90 nm RF CMOS	18-23	19.2	8.6	3.0	-	5.6
[93]	0.18 µm CMOS	19-21	9.6	9.3	4.4	-10.0	0.7
[94]	0.25 µm SiGe BiCMOS	26-32	98.0	12.4	1.8	-11.0	-1.3
[95]	0.15 µm GaAs PHEMT	1-20	175.0	20.0	1.1	-9.0	3.0

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