

# UC Irvine

## UC Irvine Electronic Theses and Dissertations

### Title

Design and Implementation of mm-Wave Wireless Transceiver System

### Permalink

<https://escholarship.org/uc/item/2sp746dx>

### Author

Zhao, Hang

### Publication Date

2022

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA,  
IRVINE

Design and Implementation of mm-Wave Wireless Transceiver System

DISSERTATION

submitted in partial satisfaction of the requirements  
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

by

Hang Zhao

Dissertation Committee:  
Professor Michael Green, Chair  
Professor A. Lee Swindlehurst  
Assistant Professor Hamidreza Aghasi

2022



# DEDICATION

To my parents and grandparents.



# TABLE OF CONTENTS

	Page
<b>LIST OF FIGURES</b>	<b>v</b>
<b>LIST OF TABLES</b>	<b>viii</b>
<b>ACKNOWLEDGMENTS</b>	<b>ix</b>
<b>VITA</b>	<b>x</b>
<b>ABSTRACT OF THE DISSERTATION</b>	<b>xi</b>
<b>1 Introduction</b>	<b>1</b>
1.1 5G Communication via mm-Wave Frequency . . . . .	1
1.2 Challenges of Communication via mm-Wave Frequency . . . . .	3
1.3 Organization of This Thesis . . . . .	5
<b>2 A 28-GHz MIMO Receiver Element</b>	<b>6</b>
2.1 Introduction . . . . .	6
2.1.1 Review of Architectures of MIMO System . . . . .	7
2.1.2 Review of Circuits Design Considerations at mm-Wave frequency . . . . .	9
2.2 Methods of Lowering the Complexity and Cost of Massive MIMO System . . . . .	12
2.2.1 Use of Wireless Synchronization for Massive MIMO . . . . .	12
2.2.2 Use of Low-order Modulation for Massive MIMO . . . . .	13
2.3 Technical Approach . . . . .	15
2.3.1 Direct Detection Receiver - Theory and System . . . . .	15
2.3.2 Noise and Linearity Analysis . . . . .	18
2.4 Circuit Design . . . . .	21
2.4.1 Square-Law Detector and the Other Blocks . . . . .	23
2.5 Measurement Results . . . . .	24
<b>3 A 28GHz 2-by-2 MIMO Transceiver Deploying Transformer Gain Equalization Techniques for 5G New Radio</b>	<b>30</b>
3.1 Introduction . . . . .	30
3.2 System Architecture . . . . .	31
3.3 Transformer Peak-Gain Equalization Methods . . . . .	34
3.3.1 Unbalanced Peak-Gain of A Lossy Transformer . . . . .	34

3.3.2	Method I - Gain Equalization Based on Unmatched Transformer . . . . .	37
3.3.3	Method II - Gain Equalization Based on Resistive Coupling . . . . .	39
3.4	Circuits Design . . . . .	42
3.4.1	Trasceiver System And Circuits . . . . .	42
3.4.2	LO Amplifier Chain and Phase-Shifter . . . . .	48
3.5	MIMO System Measurement Results . . . . .	52
<b>4</b>	<b>Modeling the Frequency Behavior of the Two-Stage Transimpedance Amplifier's Odd-Order Nonlinearity</b>	<b>60</b>
4.1	Introduction . . . . .	60
4.2	General Nonlinearity Model of a Single-Stage Amplifier . . . . .	62
4.2.1	Definition of the Input- and Output-Related Nonlinearity . . . . .	63
4.2.2	General Model for $N^{th}$ -Order Nonlinearity of a Single-Stage Open-Loop Amplifier . . . . .	75
4.2.3	Modeling the Nonlinearity of Open-Loop Two-Stage TIA . . . . .	77
4.3	Model of the Closed-Loop Two-Stage TIA . . . . .	83
4.3.1	Closed-loop Analysis of the Two-Stage Amplifier (without considering the interaction) . . . . .	84
4.3.2	Frequency Response of the Interaction in A Feedback System . . . . .	86
4.3.3	Nonlinear-feedback Frequency Response Analysis for Two-Stage TIA's $5^{th}$ -Order Nonlinearity . . . . .	89
4.3.4	Nonlinear-Feedback Frequency Analysis for Two-Stage $N^{th}$ -order Nonlinearity . . . . .	94
4.3.5	Model Verification . . . . .	97
<b>5</b>	<b>Conclusion</b>	<b>99</b>
5.1	mmWave MIMO Receiver Element for High-Speed and Low-Power Communication . . . . .	99
5.2	mmWave Transceiver for 5G Communication . . . . .	100
5.3	Model for Amplifier's High-Frequency Nonlinearity Behavior . . . . .	101
	<b>Bibliography</b>	<b>102</b>

# LIST OF FIGURES

	Page
1.1 MIMO receiver array deploying direct detection [1] . . . . .	2
2.1 Phase array for beamforming [2]. . . . .	8
2.2 Types of MIMO beamforming sytem. . . . .	10
2.3 Different types of the transmission line[2]: (a)microstrip line, (b)CPW line. . . . .	11
2.4 Example of on-board implementation of the MIMO system with: (a) wired and (b) wireless LO distribution. . . . .	14
2.5 Two different Rx systems that deploy the wireless synchronization with (a) separate RF and LO antenna and (b) shared RF and LO antenna. . . . .	14
2.6 MIMO receiver array deploying direct detection. . . . .	16
2.7 The envelopes of added LO and RF with different power levels: (a) when $P_{LO}/P_{RF} = -10$ dB, glitches appear at the phase reversing region; (b) when $P_{LO}/P_{RF} = 10$ dB, the glitches are largely reduced and can be ignored. . . . .	17
2.8 Simplified noise figure analysis model for the system. . . . .	18
2.9 Simplified Rx noise figure with sweeping the input LO power. . . . .	19
2.10 Receiver-chain architecture. . . . .	21
2.11 Three-stage LNA with switchable notch filters. When the switches is open, two notch filters can provide up to 10dB gain difference between the LO and RF band. . . . .	22
2.12 LNA S11 and S21 for both switch states. When the switches are open, the notch filter suppresses the gain at RF band (27GHz) for around 8dB compared with the LO (29GHz). . . . .	22
2.13 single-gate mixer with notch filter. . . . .	23
2.14 Test bench for the receiver IC. . . . .	25
2.15 Recovered IF signal's constellation with different data rates and modulation schemes. . . . .	26
2.16 (a) Simulated NF with input RF power sweeping from -60dBm to -35dBm, with the LO power -40dBm; (b) measured EVM of QPSK with symbol rate of 100MS/s, with sweeping the input RF power from -60 to -35dBm, and LO power -40dBm. . . . .	27
2.17 Measured receiver gain vs. input RF power with received -40dBm LO power. . . . .	27
2.18 Power breakdown of MIMO receiver element. . . . .	28
2.19 Die photo of four receiver elements. . . . .	28
3.1 The system of the 2-by-2 MIMO Transceiver. . . . .	33

3.2	MIMO receiver array deploying direct detection. . . . .	35
3.3	Frequency response of $ Z_{21} $ with different $R_w$ . . . . .	37
3.4	The peak-gain equalization method based on the unmatched transformer with $\xi = 1.2(\xi = 1$ as initial condition). The fixed transformer components values are $L_1 = L_2 = 200pH, k = 0.5$ . (a) Equalization by increasing $R_1$ and decreasing $R_2$ , (b) by decreasing $R_2$ with a fixed $R_1 = 400\Omega$ . . . . .	39
3.5	Transformer model with the coupling resistor for gain equalization . . . . .	40
3.6	the equalization by using resistive coupling. The fixed transformer component values are: $L = 200pH, C = 150fF, R = 400\Omega$ with (a) $k = -0.5$ , and (b) $k = 0.5$ . . . . .	42
3.7	The SPDT RF switch with an area efficient artificial quarter-wavelength T-line.	43
3.8	The receiver schematic with two-stage LNA and the mixer. . . . .	45
3.9	Tx and Rx side mixers and LO buffers. . . . .	46
3.10	(a)wide-band Wilkinson power combiner/splitter with single-ended drawing. The circled T-lines with different colors are also circled on the die photo correspondingly on Fig. 3.18; (b)the S-parameters of the combiner/splitter, the port 1 and 2 are the TRX_IF and TRX_RF1 port in (a). . . . .	47
3.11	(a) Simulated and measured Rx gain; (b) the noise figure of the Rx, simulation results compared w/o and w/. the RF switch's NF; (c) input S11. . . . .	49
3.12	Schematic of two-stage class-AB PA. . . . .	50
3.13	Measurement results (at 28GHz) of the Tx's gain (include mixer), the output power, and the output phase. . . . .	50
3.14	(a) Simulated and measured Tx gain; (b) output compression power over frequency. . . . .	51
3.15	Measurement results of 16QAM of Tx output with different power backoff. . . . .	51
3.16	(a) LO amplifying and phase shifting system; (b) the circuits of the phase interpolator together with the phase-tuning T-line. . . . .	53
3.17	The simulation results of the (a) phase rms error; (b) maximum gain difference.	54
3.18	Die photo of the 2-by-2 MIMO system. The colored box circles are the different artificial quarter-wavelength T-line sections appeared in Fig. 3.10(a) with the corresponding colors. . . . .	55
3.19	PCB design for measuring the die. . . . .	56
3.20	Measured antenna array radiation pattern at 27.5GHz of (a) E-plane with both co-polar and cross-polar; (b) H-plane with both co-polar and cross-polar.	57
3.21	Measurement setup for (a) single-chip measurement and (b) modulation test of Tx-to-Rx EVM for both single-channel 2-by-2 antenna array. . . . .	58
3.22	Measured Tx-to-Rx constellation of (a) single channel and (b) antenna array.	59
4.1	The two-stage closed-loop TIA topology. . . . .	61
4.2	Large-signal TIA bandwidth vs. input current amplitude. . . . .	62
4.3	Frequency response verification of network with nonlinear R or nonlinear C.	63
4.4	$3^{rd}$ -order harmonic frequency response verification of RC network with only R or C nonlinear. . . . .	67
4.5	$3^{rd}$ -order harmonic Frequency response verification of RC network with both R and C are nonlinear. . . . .	68

4.6	Circuits of TIA's first-stage amplifier . . . . .	69
4.7	Frequency response at node P of the first-stage amplifier. . . . .	71
4.8	Frequency response model of the Fig. 4.6 single-stage transimpedance amplifier 71	
4.9	Explanation of the frequency response of the 3 <sup>rd</sup> -order nonlinearity when dominant pole is at the output node of the single-stage amplifier. . . . .	74
4.10	circuits setup for finding the IRN coefficients $a_{ni}$ . . . . .	75
4.11	3 <sup>rd</sup> -order nonlinearity simulation and model results comparison. . . . .	77
4.12	(a)5 <sup>th</sup> -order nonlinearity simulation and model results comparison. (b)Simulation results of first-stage amplifier's 3 <sup>th</sup> -, 5 <sup>th</sup> -, 7 <sup>th</sup> -, 9 <sup>th</sup> -order nonlinearities over frequency. . . . .	78
4.13	Circuits of TIA's two-stage amplifier. . . . .	79
4.14	Comparison of the simulation and model results of (a) Closed-loop 3 <sup>rd</sup> -order harmonic distortion voltage, (b) 5 <sup>th</sup> -order harmonic distortion voltage. . . . .	80
4.15	the closed-loop circuits model of the second-stage amplifier. . . . .	82
4.16	frequency response model of a closed-loop feedback system of the TIA. The input voltage amplitude $V_i = I_{in}(R_{IN}  R_F)$ . . . . .	83
4.17	Comparison of the simulation and model results of (a) Closed-loop 3 <sup>rd</sup> -order harmonic distortion voltage, (b) 5 <sup>th</sup> -order harmonic distortion voltage. . . . .	85
4.18	Simplified model for analyzing the nonlinear-feedback. . . . .	86
4.19	Frequency response verification of network with nonlinear R and linear C ( $C_3 = 0$ ). . . . .	88
4.20	The two-stage nonlinear amplifier's model with the equivalent two sub-models. The input voltage amplitude $V_i = I_{in}(R_{IN}  R_F)$ . . . . .	91
4.21	Comparison of the simulation and model results of the 5 <sup>th</sup> -order nonlinearity, with considering the interactions between lower-order harmonics. . . . .	94
4.22	Harmonic interactions of the odd-order nonlinearities. . . . .	96
4.23	A set of four sub-floats. . . . .	98

## LIST OF TABLES

	Page
2.1 PERFORMANCE COMPARISON WITH OTHER 28-GHz RECEIVERS . . .	29
3.1 PERFORMANCE COMPARISON WITH OTHER 28-GHz TRANSCEIVERS	56
4.1 FIRST STAGE AMP. ODD-ORDER HARMONIC COEFFICIENTS . . . . .	77
4.2 DESIGN PARAMETERS OF TIA . . . . .	80
4.3 COMPARISON OF P/Z AT EACH NODE . . . . .	81
4.4 SECOND STAGE AMP. ODD-ORDER HARMONIC COEFFICIENTS . . .	81

# ACKNOWLEDGMENTS

This work would not have been possible without the help of many brilliant and wonderful people. I would first thank my PhD advisor Prof. Michael Green for his great help and support in many aspects. He introduced to me those very challenging topics that I was very interested in, which made me keep the passion for learning and exploring during my PhD. Moreover, Prof. Green's solid circuits analysis fundamentals, deep understanding of circuits design and rich experience in the industry help me move forward every time when my research is in a bottleneck. Prof. Green is always nice and patient to me, and always encourages me when I make mistakes or the research is not going well. Those encouragement let me fully enjoy the happiness of doing research during my PhD, and also helps me keep the passion to learn and explore the new knowledge and technologies. No doubt that those days with Prof. Green to explore the unknown and solve the challenging problems become the most memorable days in my life.

I would like to express my sincere thanks to Prof. Lee Swindlehurst for his great support on the MIMO project. And this project is based on Prof. Swindlehurst group's rich research outcomes of MIMO system. And I also thank him for serving on my dissertation committee. I want to thank Prof. Franco De Flaviis. During the antenna measurement of the MIMO project, he provides me with the advanced antenna measurement equipment, and also teach me very useful antenna measurement knowledge for getting accurate results. I want to thank Prof. Hamidreza Aghasi for kindly agreeing to serve on my dissertation committee, and providing many valuable suggestions.

I have been so lucky to work with my lab colleagues, Khaled Abdelfattah, Saba Mohammadi, Yaoyu Cao, Behnam Shahrabak. I learn a lot from them. The discussions during the group meetings with them really help me to find the potential issues of the design that I have never thought about. And their passion always encourages me along this long journey.

I would also like to acknowledge all the staffs in EECS department. I especially thank Amy Pham, for answering every question patiently that related to school work. And I also like to thank Amy Johnson who helped me receive and keep safely many important (expensive) lab equipment. And I would like to thank John Mangrich for quickly solving the software related issue and securing my tapeout several times.

I acknowledge the support under NSF grant for the MIMO projects. And I also acknowledge the two companies I interned during 2021, Skyworks Inc., and Mobixlabs Inc., in which I worked on the RF front-end products and learned a lot.

# VITA

Hang Zhao

## EDUCATION

<b>Doctor of Philosophy in Electrical Engineering</b> University of California, Irvine	<b>2016</b> <i>Irvine, California</i>
<b>Master of Science in Electrical Engineering</b> University of California, Irvine	<b>2015</b> <i>Irvine, California</i>
<b>Bachelor of Science in Electrical Engineering</b> Sichuan University	<b>2011</b> <i>Chengdu, Sichuan</i>

## RESEARCH EXPERIENCE

<b>Graduate Research Assistant</b> University of California, Irvine	<b>2019–2022</b> <i>Irvine, California</i>
--	---

## TEACHING EXPERIENCE

<b>Teaching Assistant</b> University of California, Irvine	<b>2018 Winter</b> <i>Irvine, California</i>
<b>Teaching Assistant</b> University of California, Irvine	<b>2022 Spring</b> <i>Irvine, California</i>



# ABSTRACT OF THE DISSERTATION

Design and Implementation of mm-Wave Wireless Transceiver System

By

Hang Zhao

Doctor of Philosophy in Electrical Engineering

University of California, Irvine, 2022

Professor Michael Green, Chair

Deploying large arrays of antennas for wireless communications, an idea referred to as massive MIMO, is seen as a critical technology for achieving the huge gains in spectral efficiency (SE) needed to meet the ever-increasing demand for wireless services. The main challenges of this technique are its high cost (in terms of both power consumption and hardware complexity) and achieving good performance of the transceiver elements, especially at mmWave frequencies.

In order to reduce the cost of the mmWave receiver, a 28-GHz one-bit receiver element deploying wireless LO distribution is studied and fabricated using the TowerSemi 0.18um BiCMOS process. Unlike conventional MIMO structures, in this work both the RF and the broadcast single-ended local oscillator (LO) signal are received through the RF input port and directly converted to an IF signal by using a simple low-power square-law detector. Moreover, since the composite LO and RF signals share the same amplifying chain, additional LO buffers are not needed. The analysis of the noise performance and challenges for designing the receiver element are also presented.

For the second work, a four-channel mmWave MIMO transceiver array, which operates at 28GHz for the 5G New Radio (n257). Each channel includes a transmitter (Tx) a receiver (Rx), and a LO phase shifter that combines the passive and active phase-shifting techniques.

To achieve a flatter and wider bandwidth for both Rx and Tx, a novel passive matching network, based on a transformer, is analyzed and implemented on chip. The chip was fabricated in TowerSemi 0.18um BiCMOS process.

The transimpedance amplifier (TIA) is another critical block following the frequency converter, which can be the bottleneck of the system's linearity. With the increasing of communication data rates, the TIA is required to obtain a wider bandwidth with good linearity. As a result, it is important to model the high-frequency nonlinear behavior of the TIA. In the third work, the filtering behaviors of various nonlinear sources are analyzed. Based on this analysis, new frequency behavior models of both single-stage and open-loop two-stage amplifiers have been found. Finally, by applying feedback theory together with those models to a closed-loop two-stage TIA, high-frequency behavior of odd-order nonlinearities are accurately modeled.

# Chapter 1

## Introduction

### 1.1 5G Communication via mm-Wave Frequency

The ever-increasing demand for high-speed communications drives the wireless communication technology that has evolved from the first generation to the recent fifth generation (5G). Compared with the 4G/LTE benchmarks, the 5G communication standard targets data rates up to 20Gbps, with latency as low as 1ms, and with over one million simultaneous connections per square kilometer according to the International Telecommunications Union Radio communications (ITU-R) [1]. Confronted with these challenges, the currently used wireless bands are not enough, even when higher-order modulation schemes are used. In order to achieve the desired high performance, the best solution is to move the carrier up to a higher frequency, into the millimeter-wave(mmWave) frequency band as shown in Fig. 1.1, which shows the communication bands that have already been proposed for mobile use. These defined bands, also known as FR2 (radio frequency 2), refer to an operating frequency range from 24.25GHz to 52.6GHz. In this way, wider unoccupied frequency bands can be utilized to satisfy the demands for future wireless communication.

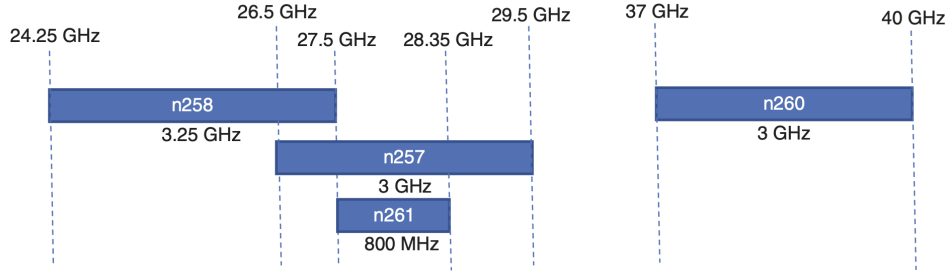


Figure 1.1: MIMO receiver array deploying direct detection [1]

The mmWave frequencies used for the cellular communication are partitioned into two separate bands: low-band (24–30GHz) and high-band (35–49GHz). The bands contains an aggregate bandwidth of more than 20GHz, which is much more than the sum of the previous generations of communication band. In this way, higher data rates can be achieved.

In addition to unlocking a rich frequency band, an added benefit of using mmWave for communication is the reduction of the size of the passive components used both on- and off-chip. Unlike a digital IC, whose size is highly dependant on the scaling of the active devices, the size of an RFIC depends primarily on the operating frequency of the circuits because the passive on-chip devices, such as spiral inductors or transmission lines, use the majority of the area. Thus when designing circuits at mmWave frequencies, all the passives will scale down accordingly, thereby reducing the size of the front-end circuitry. Similarly, the size of each off-chip antenna can also be reduced, allowing a multiple antenna system to occupy an area similar to that of a single antenna operating at low frequency, thus making multi-input multi-output (MIMO) feasible. In reality, the MIMO technique becomes a desirable choice for mmWave front-end transceiver design since it enables increases in both the output power (defined as array gain) and the spectrum efficiency. With a higher data rate and the smaller antenna size, many more Internet of things (IoT) devices can be connected to the internet. Moreover, some high-data rate applications such as 8K TV, VR/AR and edge computing will work more smoothly.

## 1.2 Challenges of Communication via mm-Wave Frequency

Though utilizing the mm-Wave frequency bands provides a number of benefits, such as higher data rate, lower latency and smaller passive size, designing the transceiver chips and systems operating at mmWave frequencies poses a number of challenges at both the system and device levels. First, channel loss, which refers to the loss of the transmitting signal through a simple light-of-sight link, will increase due to the increased frequency. Ideally, the power received at the antenna depends on both the antenna area and the distance between the source and the antenna, which is described in the Friis transmission equation:

$$P_r = \frac{P_t G_r G_t \lambda^2}{(4\pi R)^2} \quad (1.1)$$

where  $P_r$  and  $P_t$  are the transmitted and received power respectively;  $G_r$  and  $G_t$  are the antenna gain at Rx and Tx sides, respectively;  $\lambda$  is the wavelength; and  $R$  is the communication distance. This equation shows that with higher frequency (shorter wavelength), the channel loss will be higher. However, in the next chapter it will be shown that by using the MIMO technique, the channel loss can be compensated and even improved by using multiple antennas on both the Tx and Rx sides.

Another challenge is the penetration loss, which is the power loss that results when the signal propagate through certain types of material. Recent research and experiments [3–5] have shown that the penetration loss increases at higher frequencies compared, especially for certain building materials. Moreover, [6] also shows that different weather conditions, particularly rain, will increase the loss of the signal at high frequencies.

The third challenge pertains to having multiple antennas implemented on either the Tx or Rx side for compensating the loss. In a conventional architecture, where RF front-end circuitry

is placed behind each of those antennas, the whole system will consume very high power, proportional to the antenna array size. In order to reduce this excessive power dissipation, the MIMO system can be implemented using shared IF/Baseband processing; however, sharing the RF front-end, especially the low-noise amplifier (LNA) and the power amplifier (PA), can be difficult. For example, in order to share the PA/LNA, a power splitter/combiner must be implemented in front of those two blocks, which will introduce substantial loss at mmWave frequencies. For the LNA, this loss will increase the noise figure (NF), which is a critical parameters for the LNA performance, and an excessive NF increase will result in a significant reduction of the communication distance, thereby dramatically increasing the number of base stations required to cover a certain area. On the other hand, the PA is the most power hungry block in the RF front-end, and even a 10% efficiency reduction can substantially increase the power consumption for the entire receiver chain. The passives added after the PA output will dramatically reduce the power delivered to the output of the antenna, and also reduce the efficiency. As a result, the best way to implement a MIMO system is to equip each antenna with its own RF front-end, which includes at minimum a PA, LNA, and an RF switch. This thesis provides a detailed comparison of the power consumption and the beamforming flexibility for different MIMO structures.

The fourth challenge is the device performance degradation at high frequency. Typically the device gain will drop with the increase of the frequency. In order to maintain the desired gain, higher bias currents and more stages would be required, which will introduce higher NF. In addition, carefully modeling and simulating both active and passive devices is critical at mmWave frequencies, in order to minimize the unwanted parasitics. Moreover, the layout of the critical high-frequency and high-power circuits will also influence the circuits performance.

In this thesis, some possible ways to improve the performance of the critical circuits blocks and to reduce the cost and the complexity of the antenna system are provided.

## 1.3 Organization of This Thesis

This thesis is organized as follows. Chapter 2 analyzes and compares the modulation schemes and the MIMO architectures, and then presents a receiver element that deploys the LO wireless distribution with the direct detection. Chapter 3 describes techniques for designing the MIMO TRx front-end, the phase shifter, and the matching network at mm-Wave, and presents a novel design of a TRx system. Chapter 4 focuses on the baseband amplifier design, which is also critical due to the increased communication bandwidth. Finally, a complete analysis of a transimpedance amplifier (TIA) nonlinearity's high-frequency behavior is presented in Chapter 5, which helps to understand the dominant limitations of the TIA's linearity throughout the desired bandwidth.

# Chapter 2

## A 28-GHz MIMO Receiver Element

### 2.1 Introduction

Deploying large arrays of antennas for wireless communications, an idea referred to as massive MIMO [7], is a critical technology for achieving the high spectral efficiency needed to meet the ever-increasing demand for wireless services. This technology enables the deployment of higher (e.g., millimeter wave) frequencies, since shorter wavelengths mean a large array can be compact in size, and the large array gain can compensate for the increased propagation losses [8]. On the other hand, direct implementation of massive MIMO can be very costly in terms of both hardware complexity and power consumption due to the fact that each array element will require a power-consuming RF front-end, high-quality phase shifting blocks, and the distribution of a coherent LO to hundreds of those elements. Confronted with those challenges, new techniques and hardware implementations are needed that reduce the size, cost and power consumption of the MIMO transceiver element. In this chapter, a receiver element that deploys wireless LO distribution and coarse quantization is presented, and it is shown how those approaches simplify the receiver system while greatly reducing the power



consumption.

The chapter organized as follows: Section 2.2 introduces methods to reduce the cost and complexity of the massive MIMO system by deploying wireless LO distribution, and analyzes the benefits of having a large-sized array while using lower-order modulation. Section 2.3 introduces the receiver element's system topology and analyses the influence of noise and other nonidealities on the performance. Section 2.4 describes the details of the receiver circuit design. Sections 2.5 gives the measurement results.

### 2.1.1 Review of Architectures of MIMO System

The channel loss is a critical issue when designing a communication physical layer at mm-Wave frequencies. As discussed in Chapter 1, the light-of-sight loss is in proportional to the square of the operating frequency. To compensate this loss, more antennas are needed so that the antenna gain in (1.1) can be increased. The benefit of designing high-frequency antennas is the size of each individual antenna can be small, so within the same area more antennas can be implemented. As an approximation, we assume that the number of antennas  $N$  within a certain area is inversely proportional to the square of wavelength. When multiple antennas are placed closely to each other and sending (or receiving) the same modulated data with different phase shifts, the transmitted signals will interact with each other either constructively or destructively. As shown in Fig. 2.1 [2],  $d$  is the distance between any two adjacent antennas, and  $k = 2\pi/\lambda$  is the propagation constant. If the spacing between antennas is uniform, then the phase shift between two adjacent antennas will be constant, and there will be one phase angle  $\theta$  where the amplifier outputs will be constructive; for all other directions, those outputs will be partially or fully destructive. This phenomenon causes the transmitted (or received) signal of the phase array to become strong at one direction, which forms a "beam." However, in the other directions, the signal will partially cancel with

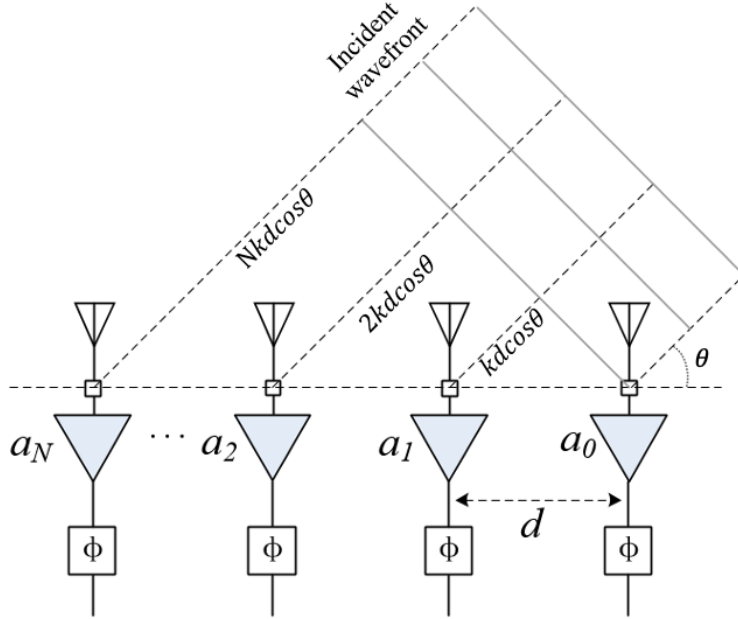


Figure 2.1: Phase array for beamforming [2].

each other, and becomes the "sidelobe."

From this analysis it can be seen that the power will be strengthened due to the use of multiple antennas, whose number is proportional to the total antenna area and inversely proportional to the square of the wavelength. Here we define the antenna gain as:

$$G_{ant} = \frac{4\pi A}{\lambda^2} \tag{2.1}$$

where  $A$  is the antenna gain defined in (2.1) is the same as the  $G_r$  or  $G_t$  defined in (1.1). Thus when an antenna array is implemented, the channel loss can not only be compensated but there are also additional power gain benefits as the operating frequency is increased. However, this is at the cost of implementing transceiver elements after each added antenna, which will increase the power consumption of the phase array system.

Fig. 2.2 shows four typical ways to implement a MIMO array system. For simplicity, the mixers and other RF blocks are not shown. The digital beamformer has the advantage of

providing full beamforming flexibility without requiring any high-performance analog phase shifters or sidelobe cancellers, which usually consume considerable power and can be complex to design. Thus the digital approach can achieve higher dynamic range with better linearity [9]. As alternatives to the digital beamformer architecture, the other three architectures save power by sharing at least one AD/DA converter. Among those architectures, the hybrid beamformer is commonly used [10, 11] due to its good RF front-end performance, and certain degrees of beamforming flexibility. To make use of the benefits of the digital beamformer architecture while avoiding implementing power-consuming high-resolution AD/DA converters, one possible way is to instead implement low-resolution converters, even down to one bit per in-phase and quadrature component. Although high-order modulation schemes exist, the lower power consumption for each individual channel enables a larger array of antennas with a fixed power budget. In this way a higher overall spectral efficiency can be achieved as discussed in [12]. In addition to increasing the overall spectral efficiency, the use of low-order modulation also allows for better tolerance of higher amplitude/phase noise and less stringent linearity requirements.

The main focus of this chapter is to implement a receiver element used in a digital beamformer that includes a one-bit ADC that supports low-order modulation (such as QPSK), while sharing the RF and LO amplifying chain to further reduce the power consumption required for each receiver element.

### **2.1.2 Review of Circuits Design Considerations at mm-Wave frequency**

For designing circuits at mmWave frequencies, there are additional design considerations, not required at lower frequencies, to ensure good agreement between the measurement and the simulation results. First of all, more passives will require EM simulation instead of the

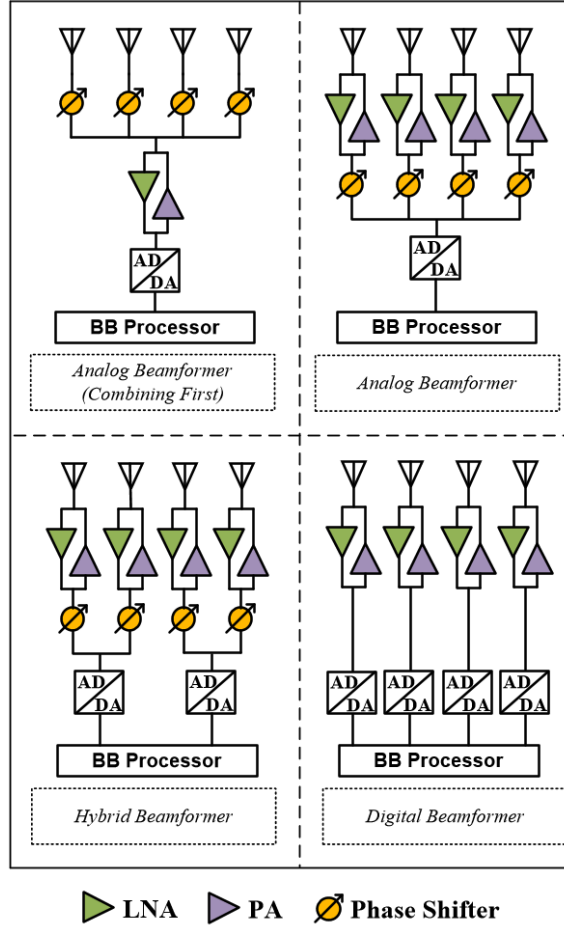


Figure 2.2: Types of MIMO beamforming system.

usual RC parasitic extraction. The reason is that when the layout dimension is larger than  $\lambda/10$ , the passives can no longer be treated as lumped elements. For example, the  $\lambda$  of a 30GHz sine wave in free space is 10mm, but on the silicon (with a normal dielectric constant of 11.9) is 2.9mm. In practice, EM simulation is required for any circuitry dimension higher than  $30\mu\text{m}$ , in order to have sufficient simulation accuracy. Passives with large dimensions, such as long traces for connecting the blocks, must be modeled as transmission lines (Tline) with appropriate termination on both sides for good matching. This also addresses the importance of T-line design at the mmWave frequencies.

The conventional methods of designing microstrip lines and coupler waveguides (CPW) are shown in Fig. 2.3 [13]. With the grounded lines placed on either side of the signal trace,

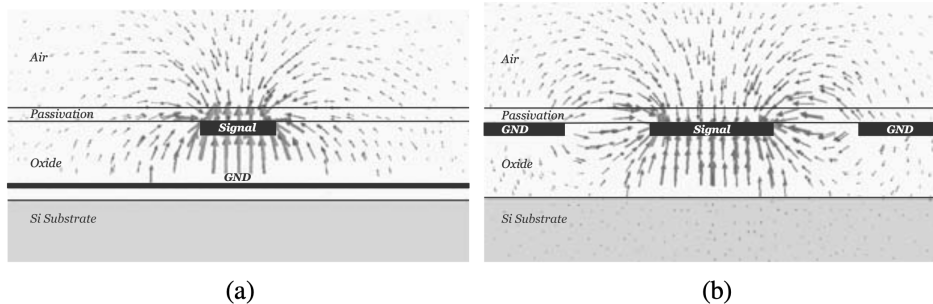


Figure 2.3: Different types of the transmission line[2]: (a)microstrip line, (b)CPW line.

the majority of the field lines will not penetrate the high-loss substrate, thereby reducing the loss. The lower loss CPW is widely accepted when designing Tlines at high-frequencies. To further minimize the loss of the Tline, [14] presents a good comparison of designing with different Tline dimensions, and with different substrate and ground shielding options to optimize the performance. The slow-wave CPW Tline [15] is also used to reduce the total length of the Tline in order to reduce the area cost of implementing long Tlines. In addition, by using the advanced fabrication technologies, for example the silicon-on-isolator (SOI), the high-resistivity substrate can reduce the induced current introduced by the passives so as to lower the loss.

In addition to the passive design considerations, the power and ground distribution is another important consideration at mm-Wave frequency. Even a short narrow trace ( $L = 50\mu\text{m}$ ,  $W = 10\mu\text{m}$ ) will introduce tens of pH inductance to the circuitry. Though the IR drop influence of this trace can be ignored, the introduced inductance is directly added to the amplifier's load or source terminal which can shift operating frequency down. For example, an LNA design usually requires inductive degeneration at the source of the common-source amplifier. This inductor's value is typically small for mmWave design, and an additional inductance introduced by a poorly designed ground distribution trace can dramatically reduce the matching performance. One simple way to reduce this effect is to place the ground pad as close as possible to the circuitry, and use as many ground bumps as possible in parallel

to reduce the inductance.

The design of active devices at mmWave frequencies also requires some considerations in order to unlock the full capability of the device. To compare the performance of different active device, there are two main parameter: transition frequency  $f_T$  and maximum oscillation frequency  $f_{max}$ . With small transistor gate lengths, the fringing capacitors and the terminal resistance will have significant influence on the  $f_T$  and  $f_{max}$  [16]. As a result, in order to optimize those two parameters, very careful attention needs to be paid at to the device layout so as to achieve the best performance of those two parameters.

## 2.2 Methods of Lowering the Complexity and Cost of Massive MIMO System

### 2.2.1 Use of Wireless Synchronization for Massive MIMO

For transceivers employing large arrays, the generation and distribution of the LO can be very challenging. As shown in Fig. 2.4(a), in order to uniformly distribute the LO through a wireline from its source at the center of the MIMO array to the array of beamformer chips, the signal will not only travel through a long on-board trace, but will also need to be split multiple times. At millimeter-wave frequencies, significant losses will be introduced by the long traces and the points where the power must be split, which will require the use of multiple buffers to compensate for those losses. As a result, additional power is required for implementing those buffers, and the complexity of the board design will increase as well. In addition, the large LO distribution tree structure is susceptible to interference from other traces, which can potentially add noise to the LO signal.

A different approach, which can potentially solve the issue mentioned above, is to wirelessly

broadcast the LO signal. As illustrated in Fig. 2.4(b), the basic idea of wireless LO distribution is to deploy a “dummy” radiating antenna placed a short distance (several wavelengths) away from the intended receiving antenna array to be radiated, and thus wirelessly broadcast a low-power carrier signal for LO distribution. Practical designs for wireless LO distribution and clock distribution have been proposed in, for example, [17, 18]. The advantage of wireless LO distribution is that the LO power attenuation follows the inverse square law of free space propagation with respect to the array dimension, which is less severe at mmWave frequencies than the attenuation of on-board traces. Another benefit of wireless LO distribution is reduced complexity of the board design.

A receiver system based on wireless LO distribution can be implemented in two possible ways. When the LO frequency is selected to be relatively far from the RF band, an additional antenna must be used to receive the LO as illustrated in Fig. 2.5(a), as well as a separate amplifier chain for the LO, which consumes additional power for each transceiver element. A different approach, illustrated in Fig. 2.5(b), entails selecting the LO frequency to be very close to the edge of the RF band. In this case each antenna receives the composite of the LO and RF, requiring only a single amplifier chain. As a result, the system will achieve a better power efficiency. The primary challenge for this topology is to separate the RF from the LO. Thus a special mixer topology is required to down-convert this mixed signal to IF. A single-gate mixer as reported in [19, 20] is a good choice to achieve this downconversion. For the receiver system presented in this paper, the Fig. 2.5(b) topology is used with the single-gate mixer, which will be discussed in detail in Section 2.3.

### **2.2.2 Use of Low-order Modulation for Massive MIMO**

Typically higher-order modulation such as m-QAM is used in communication systems to increase the spectral efficiency (SE). To enable such high-order modulation, each symbol is

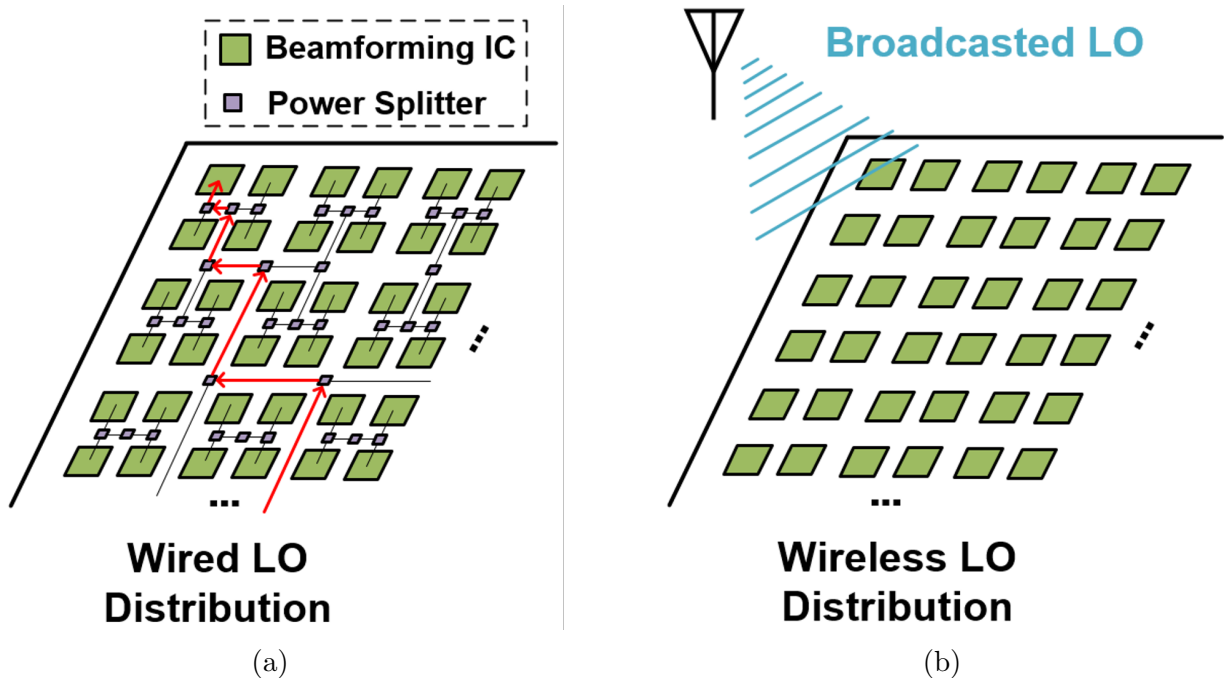


Figure 2.4: Example of on-board implementation of the MIMO system with: (a) wired and (b) wireless LO distribution.

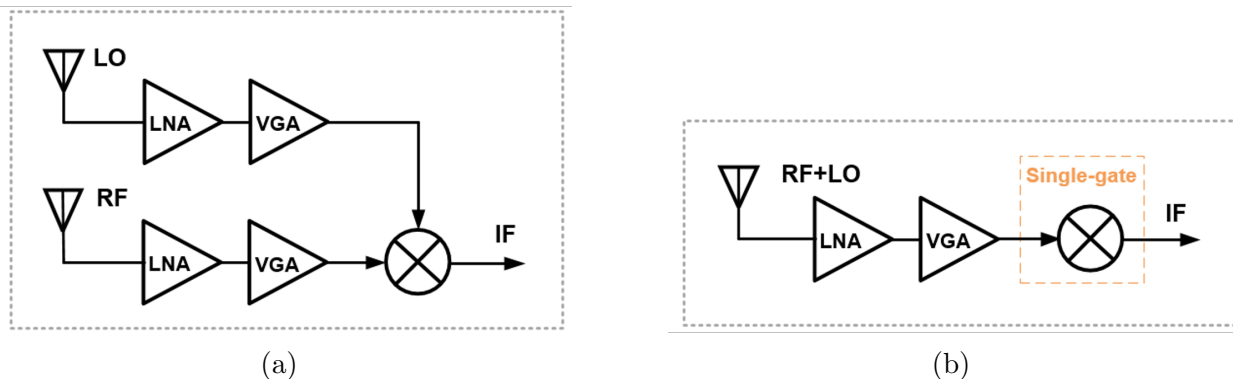


Figure 2.5: Two different Rx systems that deploy the wireless synchronization with (a) separate RF and LO antenna and (b) shared RF and LO antenna.

quantized into many levels (more than 2) in order to contain more information. While this is advantageous for the SE, it will lead to many potential challenges compared with using lower-order modulation.

Firstly, the smallest symbols' amplitude will decrease as the order of the modulation is increased. In addition, the distance between the adjacent symbols will also decrease accord-



ingly, leading to the increase of the minimum SNR requirements which will also increase the minimum detectable signal (MDS) of the system. As a result, in order to ensure that the received smallest symbols' power is above the increased MDS, a higher output power from the TX side is required to avoid reduce the communication distance, resulting in a larger array size and higher power consumption for boosting up the array gain. Moreover, the phase noise requirements for both the TX and RX will also increase with the modulation's order, making the synthesizer design more challenging. The second challenge with high-order modulation is the more stringent linearity requirement. With the decreased symbol distance, the system is more susceptible to certain types of distortion that can result in perturbing the symbol to another region, leading to a wrong decision. As a result, more power backoff will be required, which reduces the output power and the efficiency of the power-hungry PA. The third challenge is that the power consumption of the higher-order modulation system will be higher. This is due not only to the higher required noise and linearity, but also to the higher-resolution ADC/DACs are needed together with a more complex baseband processing unit to modulate and demodulate the symbols. Moreover, the design complexity and the power consumption will grow rapidly with the data converter's resolution and speed.

## 2.3 Technical Approach

### 2.3.1 Direct Detection Receiver - Theory and System

As mentioned in the previous section, with the LO frequency selected near the RF band, a single RF amplifier chain can be used to amplify both the RF and LO signals. A MIMO receiver based on this idea is illustrated in Fig. 2.6, where the envelope of the composite LO and RF signal at node  $a$  contains the desired IF signal; this envelope can be extracted by a simple square-law detector. To illustrate this process, the demodulation of a BPSK-

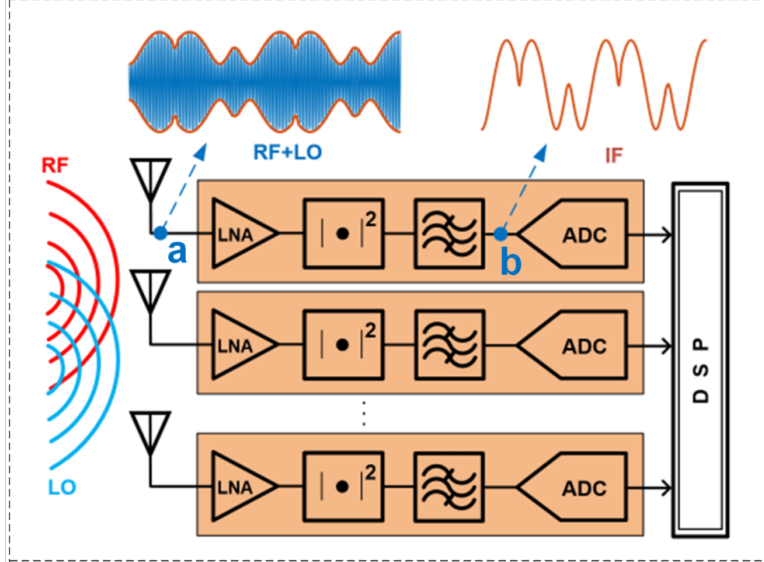


Figure 2.6: MIMO receiver array deploying direct detection.

modulated signal is first considered. The input signal at node  $a$  (ignoring the channel losses) can be expressed as:

$$V_A = V_{RF}(t) \cdot \cos(\omega_{CR}t) + V_{LO} \cdot \cos(\omega_{LO}t) \quad (2.2)$$

where  $V_{RF}$  and  $V_{LO}$  are the amplitudes of the baseband and the received LO, respectively;  $\omega_{CR}$  and  $\omega_{LO}$  are the carrier and LO frequencies, respectively. The first term in (2.2) represents the modulated RF signal.

This composite RF and LO signal is amplified and then fed to a square-law detector, such as a diode [19] or a single-gate mixer [20], along with proper filtering, from which the IF can be fully recovered. While the benefit of sharing the LO and RF chain can help improve the power efficiency, the composite signal is only available as a single-ended signal, and thus some unwanted components will appear at the mixer output that can't be canceled due to its single-ended topology as shown in Fig. 2.7(a). This phenomenon is analyzed as follows. The square-law detector's conversion gain  $A_{conv}$ , defined as the amplitude ratio between the output IF signal and the input RF band signal, is proportional to the input LO's amplitude,

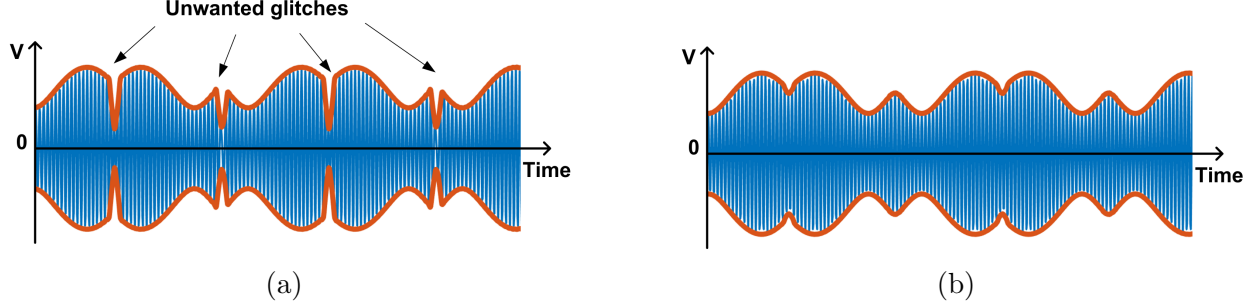


Figure 2.7: The envelopes of added LO and RF with different power levels: (a) when  $P_{LO}/P_{RF} = -10$  dB, glitches appear at the phase reversing region; (b) when  $P_{LO}/P_{RF} = 10$  dB, the glitches are largely reduced and can be ignored.

and its implementation with the detailed expression will be discussed in a later section. Here it is expressed in (2.3) with a coefficient  $\alpha$  having units of  $V^{-1}$ :

$$A_{conv} = \alpha V_{LO} \quad (2.3)$$

After the composite input signal (2.2) is fed to this detector, the detected output voltage with high-frequency components filtered is given by:

$$V_{out} = \frac{\alpha}{2} \{ V_{RF}^2(t) + V_{LO}^2 + 2V_{LO}V_{RF}(t) \cos [(\omega_{CR} - \omega_{LO})t] \} \quad (2.4)$$

For an ideal unshaped BPSK baseband signal with instantaneous phase changes, its baseband and RF amplitudes are constant. Thus the first two terms in (2.4) introduce only a dc term to  $V_{out}$ , which can be easily filtered out. However, in the more realistic case where the phase inversion is not instantaneous during each transition, the value of  $V_{RF}^2(t)$  will momentarily decrease toward zero and then return back, resulting in a glitch in the recovered IF signal as shown in Fig 2.7(a). When the LO is at least 10 dB higher than the RF, the glitches' influence on the IF becomes small enough to be ignored, as illustrated in Fig. 2.7(b). In order to achieve this condition, either the LO power should be boosted or the RF power reduced. In this work, a low-Q notch filter is used to reduce the RF power, which will be

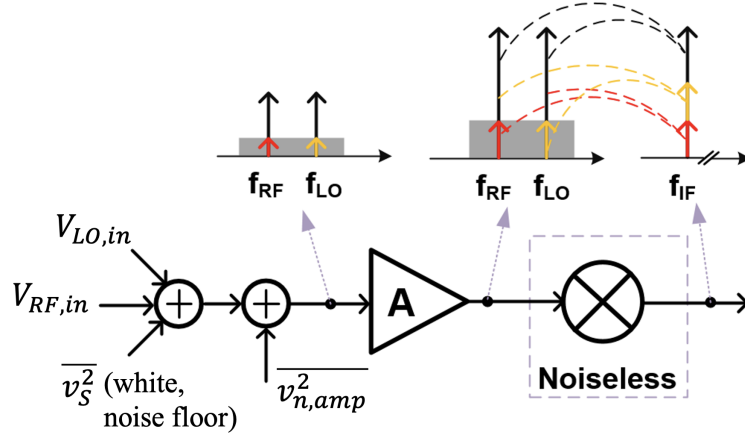


Figure 2.8: Simplified noise figure analysis model for the system.

discussed in the next section.

Conventional quadrature demodulation systems require a quadrature sampling clock for separating the I/Q signals, which will require circuits for single-ended to quadrature conversion, I/Q calibration and two identical ADCs. To further reduce the analog system's complexity, digital quadrature demodulation [21] could be applied in the proposed receiver system, where the recovered IF signal is applied directly to one ADC with four sampling points per unit interval. In this way, both the I and Q components would be digitized and could be separated within the DSP block. Though an additional sampling clock needs to be provided off-chip, converting this clock signal to quadrature is not needed, at the cost of having a higher sampling rate.

### 2.3.2 Noise and Linearity Analysis

As mentioned in the previous section, when the LO frequency is selected within the communication band, for some applications there may be strict regulatory restrictions on its radiated power. In such a case the weak LO power can be amplified by the following shared LNA and VGA, which can help to provide enough conversion gain at the mixer. However,

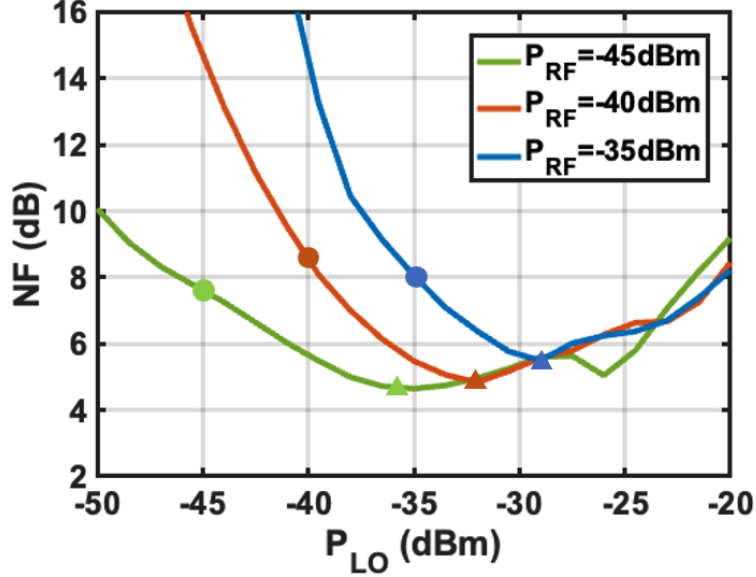


Figure 2.9: Simplified Rx noise figure with sweeping the input LO power.

due to the fact that the received LO signal has finite SNR, the noise influence of the LO signal must also be analyzed. This can be done using the simplified noise model shown in Fig. 2.8. The system is comprised of an amplifier with voltage gain  $A$ , and a mixer whose conversion gain is given by  $\alpha V_{LO}$ , defined in (2.3). To simplify the noise analysis, single-tone RF and LO signals with amplitudes of  $V_{LO,in}$  and  $V_{RF,in}$ , respectively, are applied to the system. It is assumed that these input signals are accompanied by white noise whose mean-square value is given by  $\overline{v_S^2}$ . In addition, we assume the input-referred noise  $\overline{v_{n,amp}^2}$  of the amplifier is white over the amplifier's bandwidth, and the mixer's noise is ignored for simplicity. Thus the overall noise at the input of the amplifier can be expressed as:

$$\overline{v_{n,in}^2} = \overline{v_S^2} + \overline{v_{n,amp}^2} \quad (2.5)$$

According to (2.4), the amplitude  $V_{IF}$  of the desired tone and the noise  $\overline{v_{n,IF}}$  at the output of the mixer can be expressed as:

$$V_{IF} = \alpha A^2 V_{LO,in} V_{RF,in} \quad (2.6)$$

$$\overline{v_{n,IF}^2} = \alpha^2 A^2 (A^2 V_{LO,in}^2 \overline{v_{n,in}^2} + A^2 V_{RF,in}^2 \overline{v_{n,in}^2}) \quad (2.7)$$

The SNR at the output of the mixer, and the noise figure of this simplified system can be expressed as:

$$SNR_{mix,out} = \frac{V_{IF}^2}{\overline{v_{n,IF}^2}} = \frac{V_{LO,in}^2 V_{RF,in}^2}{V_{LO,in}^2 \overline{v_{n,in}^2} + V_{RF,in}^2 \overline{v_{n,in}^2}} \quad (2.8)$$

$$NF = \frac{SNR_{RF}}{SNR_{mix,out}} = \frac{V_{RF,in}^2}{v_S^2} \cdot SNR_{mix,out} = \left[ 1 + \frac{V_{RF,in}^2}{V_{LO,in}^2} \right] \cdot \left[ 1 + \frac{\overline{v_{n,amp}^2}}{v_S^2} \right] \quad (2.9)$$

This expression in (2.9) gives the noise figure of the additive mixing system. Both noise sources will influence the overall noise figure of this kind of system. Notice that the term in the second parentheses corresponds to the noise figure normally seen in conventional RF systems. The overall noise figure of the additive mixing system will be larger than that of a conventional RF system, particularly when the input LO amplitude is less than or equal to that of RF. With a larger LO amplitude, the NF will be closer to that of a conventional receiver system. To demonstrate this conclusion, the simulated NF for a range of LO and RF amplitudes is shown in Fig. 2.9. These results show that when the LO input power decreases below that of the RF, the NF increases substantially. In addition, when the LO and RF power are equal, the NF is approximately 3dB higher than the minimum NF value, consistent with (2.9). At higher LO input power, the NF is increasing with the LO power due to the gain distortion caused by the presence of a strong LO tone. Compared with the conventional mixer such as the passive switch-based or Gilbert cell active mixer, the square-law based mixer will suffer more from the LO's amplitude noise. For this receiver, -40dBm input LO power is used in order to reduce the NF for a wide range of input RF power, while

avoiding introduction of a strong tone that could desensitize the receiver gain.

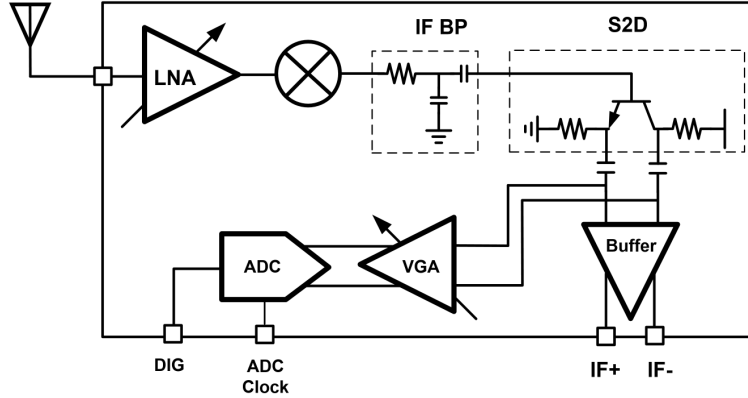


Figure 2.10: Receiver-chain architecture.

## 2.4 Circuit Design

The block diagram of one receiver chain is shown in Fig. 2.10. In order to suppress the glitches and increase the RF input power range, the LNA is implemented with a set of switched third-order notch filters, shown in Fig. 2.11. When the switches are open, the notch filter together with the LNA can provide up to 10 dB gain suppression at the RF center frequency while maintaining a gain variation of less than 2 dB over the RF band.

The passive notch filter can provide a low impedance at unwanted frequencies, corresponding to the RF band, while maintaining a high impedance at the LO frequency. As discussed in [22] the inductor and capacitor values can be determined by the following equations:

$$f_{RF-center} = \frac{1}{2\pi\sqrt{L_1 \cdot (C_1 + C_2)}} \quad (2.10)$$

$$f_{LO} = \frac{1}{2\pi\sqrt{L_1 \cdot C_1}} \quad (2.11)$$

The gain difference between the unwanted and desired bands is limited by both the Q of inductor  $L_1$  and the frequency difference between these two bands. To further increase the

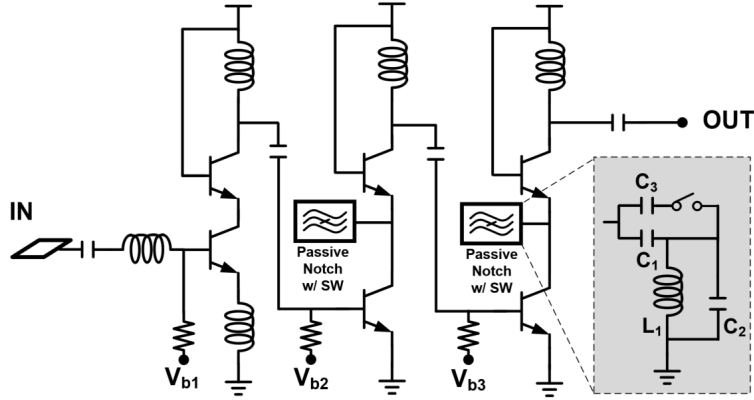


Figure 2.11: Three-stage LNA with switchable notch filters. When the switches is open, two notch filters can provide up to 10dB gain difference between the LO and RF band.

gain difference, two identical filters are used at both the second and third stages of the LNA. The first stage of the LNA does not include the notch filter in order to obtain good input matching. The LNA's simulated gain and S11 over frequency are shown in Fig. 2.12. For

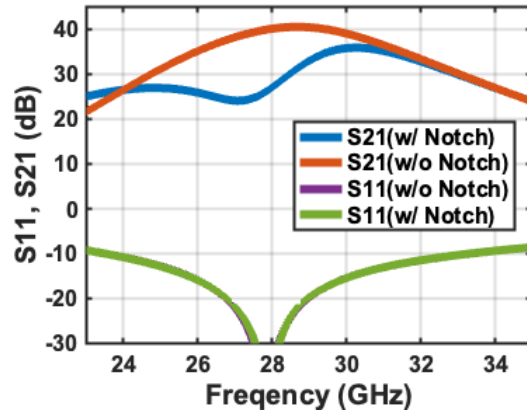


Figure 2.12: LNA S11 and S21 for both switch states. When the switches are open, the notch filter suppresses the gain at RF band (27GHz) for around 8dB compared with the LO (29GHz).

the case where the input LO power is already higher than that of the RF, the use of a notch filter is not necessary. In this case the switches can be closed to connect capacitor  $C_3$ , together with the finite on-resistance of the switch, in parallel with  $C_1$ . The larger effective capacitance will shift the notch to a much lower frequency with lower Q. As a result, the frequency response within the RF band becomes similar to that of a normal multi-stage



LNA.

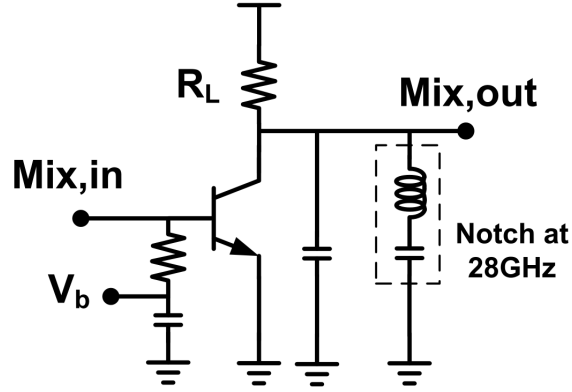


Figure 2.13: single-gate mixer with notch filter.

### 2.4.1 Square-Law Detector and the Other Blocks

Following the LNA is a square-law detector that is implemented using a common-emitter amplifier as shown in Fig. 2.13. The collector current of the amplifier, which is an exponential function of  $V_{mix,in}$ , can be represented by the following Taylor series:

$$I_C \approx I_{CQ} \left[ 1 + \frac{V_{mix,in}}{V_T} + \frac{1}{2} \left( \frac{V_{mix,in}}{V_T} \right)^2 + \dots \right] \quad (2.12)$$

where  $I_{CQ}$  and  $V_T$  are the quiescent collector current and the thermal voltage, respectively. The frequency components of third and higher-order harmonics will be filtered out by the mixer's capacitive load together with the following IF bandpass filter, and the fundamental frequency is filtered out by the 28-GHz notch filter at the load. After the filtering provided by the IF bandpass filter shown in Fig. 2.13, the second harmonic in (2.12) provides the amplified IF signal. Using (2.3) and (2.4), the conversion gain and the  $\alpha$  defined in previous

section are expressed as:

$$A_{conv} = \frac{V_{IF}}{V_{RF,in}} = I_{CQ}R_L \frac{V_{LO}}{2V_T^2} \quad (2.13)$$

$$\alpha = \frac{A_{conv}}{V_{LO}} = \frac{I_{CQ}R_L}{2V_T^2} \quad (2.14)$$

The  $I_{CQ}$  can be reduced to achieve a given conversion gain if the provided LO power is increased. The signal feed-through noise can be largely filtered by the IF-bandpass filter shown in Fig. 2.10. The recovered single-ended IF is then converted to differential and fed to the VGA, which provides additional gain for the IF signal. The power consumption of each receiver chain is further reduced by using a simple one-bit ADC, which is sufficient for QPSK modulation. The one-bit ADC is implemented on-chip as a comparator.

## 2.5 Measurement Results

A 2-by-2 four-channel receiver chip has been fabricated using the TowerSemi 0.18  $\mu\text{m}$  BiCMOS process that includes npn BJTs with  $f_T = 240$  GHz. Each channel is implemented with an LNA, a mixer, a VGA, and an ADC. The four channels are identical and the measurement results are from channel1 with the other channels verified to have similar performance. The measurement setup is shown in Fig. 2.14. The modulated IF signal (centered at 1 GHz) is generated by the Keysight M8190A waveform generator, which is mixed with a 28-GHz LO using an up-conversion mixer, moving the center frequency to 27 GHz. A power combiner is used to provide the composite RF + LO signal, which is then fed to the DUT. At the output side, the differential IF band output is connected to the Keysight MXR604A real-time oscilloscope to measure the IF band signal's EVM.

The constellations resulting from different modulations are shown in Fig. 2.15. The results

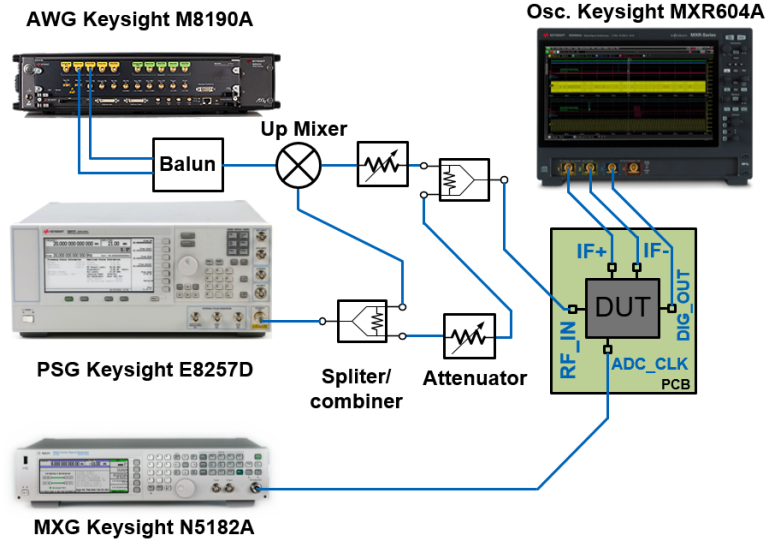


Figure 2.14: Test bench for the receiver IC.

verify that the chip is capable of supporting low-order modulation such as QPSK and 16-QAM. When the modulation order is higher than 16-QAM, the large amplitude variation of the symbols will cause severe signal interference due to the single-gate mixer, and the output signal doesn't exhibit a clear constellation diagram. The transmitted waveforms use both shaped (root-raised cosine with the roll-off factor set to 0.35) and unshaped modulation, both of which can achieve relatively high symbol rates with  $\text{EVM} < -14$  dB. The results also show that with the increase of the data bandwidth the EVM is degraded due to the limited in-band gain flatness, as well as the single-gate mixer's limitations. The results show that the receiver can support unshaped and shaped QPSK with data rates up to 1GS/s and 800MS/s, respectively. In addition to the low-level modulation test, the system can support both unshaped and shaped 16-QAM with a data rate up to 800MS/s and 200MS/s, respectively. Fig. 2.16(a) shows the simulated NF performance vs. RF input power when the LO power is -40dBm. In addition, it shows when the notch is turned on, the NF drops due to the decrease of the LNA gain. However, with the decreased gain when notch is activated, the NF curve starts rising at a higher RF input power (around 8 dB higher). As a result, within a certain input power range (-43 to -36 dBm), the output SNR can be higher if the notch












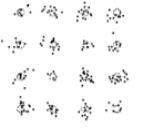
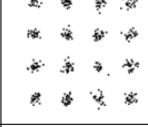
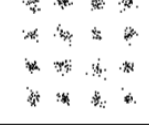
SR	100MS/s	200MS/s	400MS/s	1GS/s
EVM	-29dB	-26dB	-22.6dB	-16.5dB
QPSK Unshaped				
SR	100MS/s	200MS/s	400MS/s	800MS/s
EVM	-21dB	-20.6dB	-18.5dB	-14.1dB
QPSK Shaped				
SR	100MS/s	200MS/s	400MS/s	800MS/s
EVM	-24.2dB	-22.5dB	-20.3dB	-16.6dB
16QAM Unshaped				
SR	100MS/s	200MS/s(shaped)		
EVM	-19.2dB	-18.3dB		
16QAM Shaped				

Figure 2.15: Recovered IF signal's constellation with different data rates and modulation schemes.

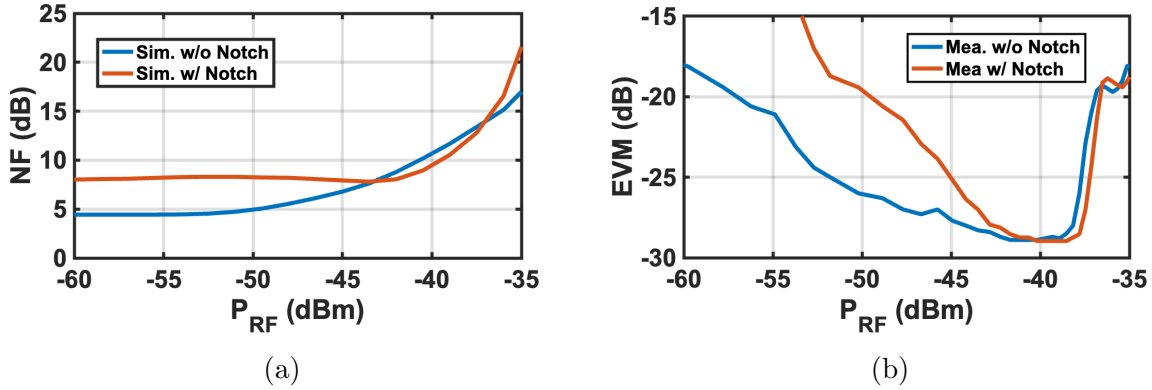


Figure 2.16: (a) Simulated NF with input RF power sweeping from -60dBm to -35dBm, with the LO power -40dBm; (b) measured EVM of QPSK with symbol rate of 100MS/s, with sweeping the input RF power from -60 to -35dBm, and LO power -40dBm.

filter is activated. The measured EVM performance of a QPSK modulation with 100MS/s in Fig. 2.16(b) shows that when the RF input power is larger than -40 dBm, the output EVM value quickly degrades due to both the degraded NF and the glitch issue discussed in the previous sections. In addition, turning the notch on shifts the EVM curve to the right by 1.5dBm for  $P_{in} \geq -40$ dBm, which provides an additional method for increasing the dynamic range while the input RF power is relatively large. However, the EVM is degraded for lower values of  $P_{in}$  when using this method, due to the increased NF.

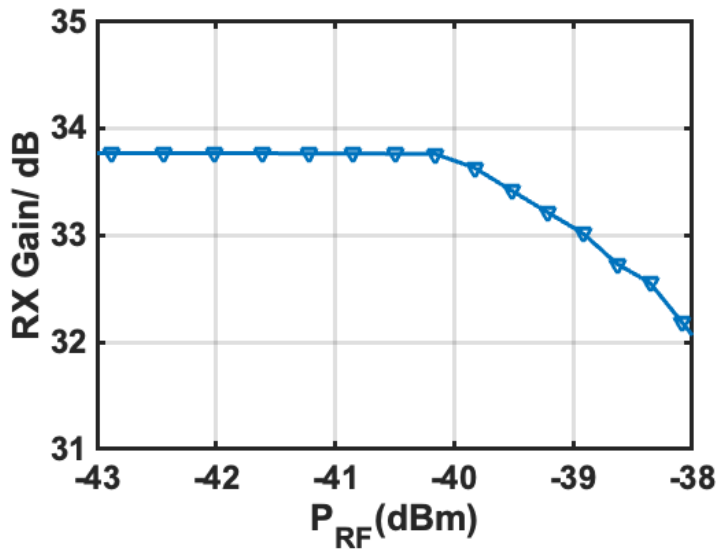


Figure 2.17: Measured receiver gain vs. input RF power with received -40dBm LO power.

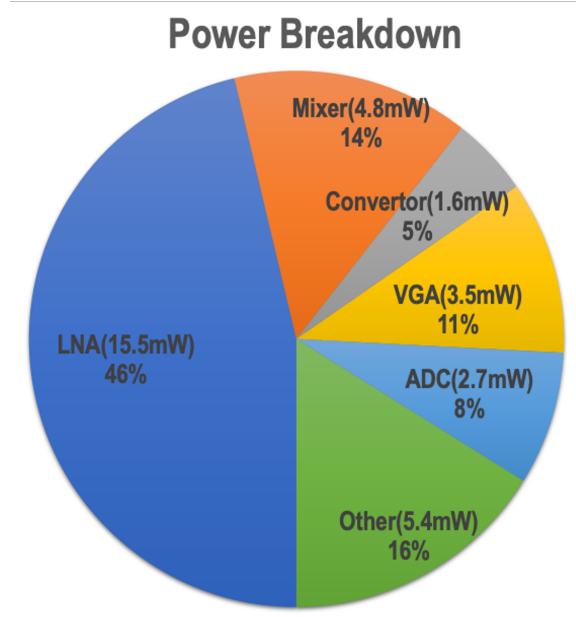


Figure 2.18: Power breakdown of MIMO receiver element.

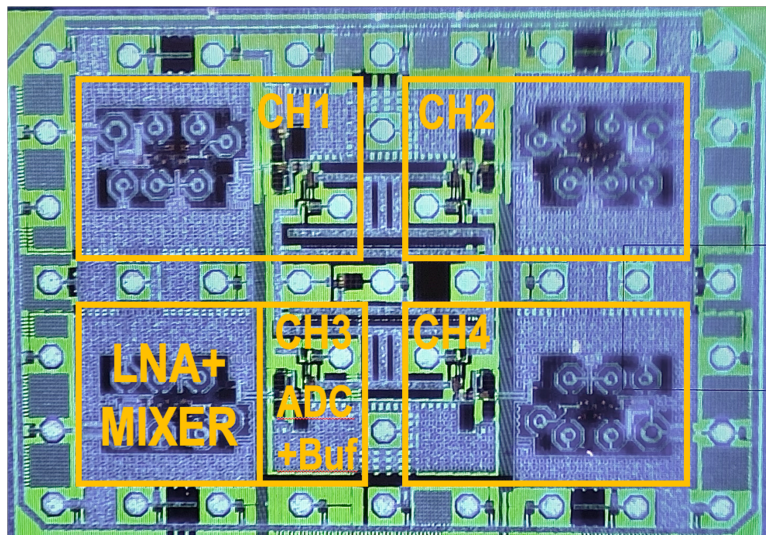


Figure 2.19: Die photo of four receiver elements.

The RX channel's measured gain as a function of the input RF power is shown in Fig. 2.17, with the 1-dB compression point corresponding to  $P_{in} = -38.7$  dBm. The power consumption required to achieve the 33.8 dB gain is 35 mW, including the on-chip one-bit ADC. Fig. 2.18 shows the power breakdown of the Rx channel. The die photo is shown in

Table 2.1: PERFORMANCE COMPARISON WITH OTHER 28-GHz RECEIVERS

Comparison Table	This work	[23]	[24]	[25]
Process	0.18 SiGe	0.18 SiGe	65nm	28nm
Freq. (GHz)	28	28	28	28
NF (dB)	4.8	4.6	4.1	4.4
Symbol Rate, Max (GS/s)	1	1.5	2.5	0.4
Data Rate, Max (Gb/s)	3.2	6	15	2.4
Supply Voltage (V)	1.6/1.8	1.2/2.2	-	1/1.8
RX Power/ch. (mW)	35*	130	148	42
Chip Area/ch. (mm <sup>2</sup> )	0.94**	2.92	3	1.16

\*Includes the on-chip ADC. \*\*Receiver only.

Fig. 2.19. A table comparing this work with other MIMO transceivers operating at a similar frequency band is shown in Table 2.1. This system achieves a very low power consumption compared with the other works benefiting from the deployment of the direct detection.

# Chapter 3

## A 28GHz 2-by-2 MIMO Transceiver

## Deploying Transformer Gain

## Equalization Techniques for 5G New

## Radio

### 3.1 Introduction

Fifth-generation (5G) mobile networks target a higher data-rate with lower latency to meet the ever-increasing demand for the wireless services. This target can be achieved by unlocking a wider communication bandwidth at mmWave frequencies with higher-order modulation schemes such as n-QAM. The 5G New Radio (NR) band n257 provides a 3-GHz bandwidth centered at 28GHz, which is much wider than the current commercial communication band. However, a higher carrier frequency leads to increased loss through the same communication distance, and higher-order modulation increases the required link's SNR. Facing those chal-



lenges, MIMO becomes a promising technique [7] since the loss can be compensated by the array gain. Moreover, a large antenna array is capable of serving multiple users simultaneously so as to achieve a higher spectral efficiency (SE). The main challenges for designing a MIMO system for the n257 band are realizing a flat gain with minimum in-band variation over the wide RF bandwidth, and the design of a high-performance phase shifter to introduce less influence to the RF signal with fine phase shifting resolution. This work presents a 28GHz 2-by-2 MIMO transceiver for the n257 band. The novel methods of transformer-based matching networks are studied and implemented to provide wider and flatter gain over the required frequency band, and a phase shifter based on using a combination of active and passive phase-shifting methods is presented for achieving good performance. The design considerations for designing other critical front-end blocks using the BiCMOS process are also discussed in this chapter.

The chapter organized as follows: Section 3.2 describes the main considerations for the system architecture of the transceiver. Section 3.3 gives the detailed modeling and analysis for the transformer and the peak-gain equalization methods. Section 3.4 describes in detail the core circuit blocks and their performance. System-level measurement results are given in Sections 3.5.

## 3.2 System Architecture

MIMO arrays used in base stations, requires a large size (e.g., 128 antennas) to serve multiple users simultaneously while achieving a large array gain. The design is consist of an array of antennas with its own transceiver and AD/DA converters separately, which refers to the structure of a digital beamformer. However, the power consumption will be high due to the separate high-speed and high-resolution AD/DA converters in each antenna element. Instead, an analog beamformer can be implemented by sharing the AD/DA converters

with multiple antenna elements. Though the full flexibility of multiple-beam forming is lost compared with the digital beamformer, the overall power consumption can be reduced. As illustrated in Fig. 3.1, a 2-by-2 MIMO system deploys analog beamforming in which four transceivers share one IF processing path. Following each antenna, an RF switch is implemented to select between the Rx/Tx modes. The Rx contains a two-stage LNA with a double-balanced mixer. The down-converted IF signals are combined together through a 4-to-1 wideband Wilkinson combiner/splitter. The outputs of all of the mixers need to be matched to  $50\Omega$  over the IF band. For the Tx, the input IF signal is fed to the wideband Wilkinson combiner/splitter and then split to each Tx channel's up-converter. Then the PA stage will amplify the up-converted RF signal and deliver the high-power output to the RF pads.

The frequency plan of this transceiver is as follow. For the Rx, the received RF band (26.5GHz to 29.5GHz, centered at 28GHz) signal is down-converted to the IF band (centered at 6.5GHz) by mixing with a high-frequency LO (21.5GHz). The entire RF band will be down-converted to the IF band (5GHz to 8GHz, centered at 6.5GHz). Then, the channel selection, and the I/Q demodulation can be performed by applying another low-frequency LO (range from 5-8GHz) through the on-board traces. For the Tx, the first up-conversion will convert the baseband signal to the IF band by mixing with the low-frequency LO (centered at 6.5GHz), then the second up-conversion is performed by mixing the IF with high-frequency LO (21.5GHz) to convert the IF to the RF band. In this work, the quadrature modulation/demodulation with the corresponding low-frequency LO and the baseband processing parts are not implemented on the chip.

In order to perform the beamforming, each transceiver element in the 2-by-2 MIMO should be able to precisely shift the phase of the received/transmitted signals from 0 to  $360^\circ$ . Moreover, it should exert minimal influence on the RF amplifying chain's performance. In [26] a variable-delay Tline is implemented as an RF phase shifter, and in [23] active cells are

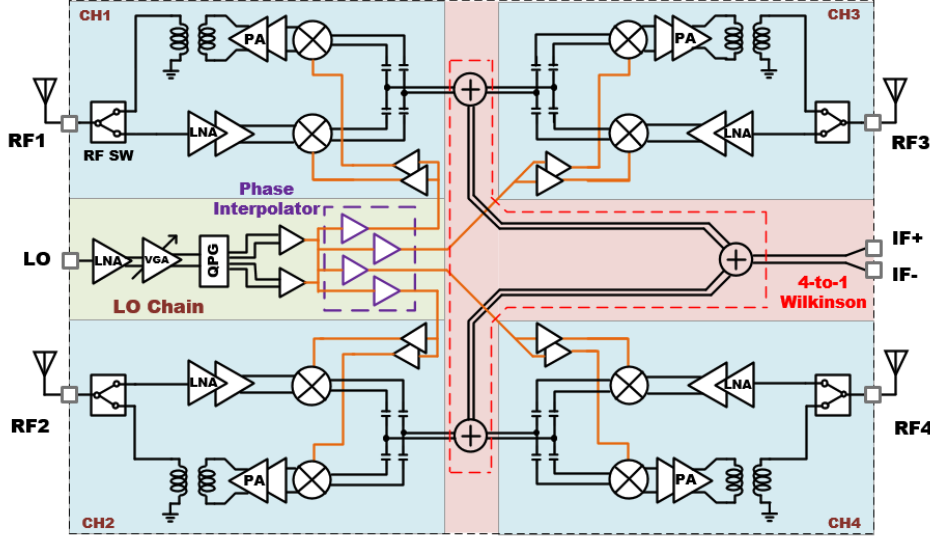


Figure 3.1: The system of the 2-by-2 MIMO Transceiver.

implemented for to achieve the same purpose. Both works introduce relatively large RF gain variations over different shifted phases. In [24] a different way of implementing the phase shifter is presented. Instead of directly shifting the RF signal, the phase shifting can be performed on the LO signal, and shift the RF by multiplying the phase-shifted LO at the mixer. The main innovation of [24] is that its system doesn't require any phase shifting blocks inserted in the RF path, thereby optimizing the RF signal's quality and gain variation. In this work, the phase shifting is performed by shifting the LO's phase. The received LO signal is first amplified, and then an RC ladder converts the signal into quadrature. The quadrature signals are then fed to four phase interpolators that shift the LO's phase for each transceiver independently. Each interpolator provides  $1^\circ$  phase shifting resolution over the entire  $360^\circ$  range. Each shifted LO is fed to two LO buffers that drive the transceiver's up/down-converters.

As described in [27], the in-band gain flatness of both Tx and Rx is one of the key factors to achieve good error vector magnitude (EVM). In this work, because the channel selection is performed in the IF band, a flat gain is required for both the RF and IF bands. Detailed analysis of the challenges and the solutions we provided are discussed in the following

sections.

### 3.3 Transformer Peak-Gain Equalization Methods

#### 3.3.1 Unbalanced Peak-Gain of A Lossy Transformer

As described in previous section, the gain flatness over both the RF and IF bands is one of the key factors to achieve a good EVM. Use of a transformer-based load has been demonstrated to be a very effective way to achieve flat gain over a wide bandwidth [28–30] while avoiding the need for higher-order band-pass filters. In this work, the transformer loads are used in all of the RF amplifiers and the LO amplifiers. This section we use the lossy model of the transformer to analysis its transconductance ( $Z_{21}$ ) peaks' inequality, and introduce two methods to equalize its peaks.

A general model of a transformer is shown in Fig. 3.2. Resistors  $R_1$  and  $R_2$  are the port terminations, and the serise loss of the windings are modeled as  $R_{w1}$  and  $R_{w2}$ , respectively. Here the total shunt resistance of each individual winding (without considering the coupling from the other side winding) are expressed as:

$$\begin{aligned} R_{tot1} &= R_1 || R_{p1} \approx R_1 || (R_{w1} Q_{w1}^2), \\ R_{tot2} &= R_2 || R_{p2} \approx R_2 || (R_{w2} Q_{w2}^2) \end{aligned} \tag{3.1}$$

where  $R_{p1}$  and  $R_{p2}$  are the equivalent shunt resistance converted from the windings' series loss, and  $Q_{w1}$  and  $Q_{w2}$  are the quality factors of each winding's individual LC tank (without considering the coupling from the other side). By converting the series resistor  $R_{w1}$  and  $R_{w2}$  to shunt resistance, the y-parameters of the transformer (near the resonant frequency of the

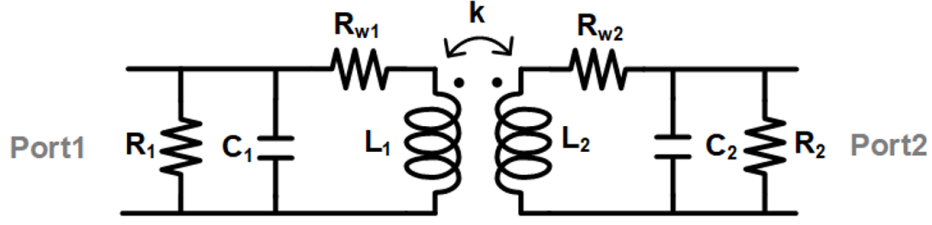


Figure 3.2: MIMO receiver array deploying direct detection.

each side LC tank) are:

$$Y_{11} = \frac{1}{R_{tot,1}} \left( 1 + Q_1 \left( \frac{s}{\omega_{01}} + \frac{\omega_{01}}{s} \right) \right) \quad (3.2)$$

$$Y_{22} = \frac{1}{R_{tot2}} \left( 1 + Q_2 \left( \frac{s}{\omega_{02}} + \frac{\omega_{02}}{s} \right) \right) \quad (3.3)$$

$$Y_{12} = Y_{21} = \frac{k}{s\sqrt{L_1 L_2} (1 - k^2)} \quad (3.4)$$

where:

$$Q_1 = \frac{R_{tot1}}{\omega_{01} L_1 (1 - k^2)} \quad (3.5)$$

$$Q_2 = \frac{R_{tot2}}{\omega_{02} L_2 (1 - k^2)} \quad (3.6)$$

$$\omega_{01} = \frac{1}{\sqrt{L_1 C_1} (1 - k^2)} \quad (3.7)$$

$$\omega_{02} = \frac{1}{\sqrt{L_2 C_2} (1 - k^2)} \quad (3.8)$$

The transimpedance  $Z_{21}$  of the transformer can be expressed as:

$$\begin{aligned} Z_{21} &= \frac{-Y_{21}}{Y_{11}Y_{22} - Y_{21}Y_{12}} \\ &= -\frac{k\sqrt{Q_1 Q_2 R_{tot1} R_{tot2} \omega_{01}^3 \omega_{02}^3 s}}{[s\omega_{01} + Q_1(s^2 + \omega_{01}^2)] [s\omega_{02} + Q_2(s^2 + \omega_{02}^2)] - k^2 Q_1 Q_2 \omega_{01}^2 \omega_{02}^2} \end{aligned} \quad (3.9)$$

To study transformer's  $Z_{21}$  under the matching condition, for simplicity, we assume all the components on both sides are identical. Then we have  $R_1 = R_2 = R$ ,  $C_1 = C_2 = C$ ,  $L_1 = L_2 = L$  and  $R_{w1} = R_{w2} = R_w$ . Likewise, we assume that the parameters defined for the two windings are also equal under this matching condition; i.e.,  $Q_1 = Q_2 = Q$ ,  $\omega_{01} = \omega_{02} = \omega_0$ , and  $R_{tot1} = R_{tot2} = R_{tot}$ . Then this simplified model under the matching condition is the same as the model discussed in [30, 31], and there will be two peaks in the frequency response of  $|Z_{21}|$ . Those peaks' frequencies and their corresponding  $|Z_{21}|$  values are:

$$\omega_{L,H} = \frac{1}{\sqrt{LC(1 \pm |k|)}} \quad (3.10)$$

$$|Z_{21,\omega=\omega_L}| = \frac{1}{2} \frac{L(1 + |k|)}{R_w C} \|R \quad (3.11)$$

$$|Z_{21,\omega=\omega_H}| = \frac{1}{2} \frac{L(1 - |k|)}{R_w C} \|R \quad (3.12)$$

It can be seen from the above equations that, there will be two peaks with different values appear on the  $|Z_{21}|$  frequency response. With the component values in Fig. 3.2 (under the matching condition) set to be:  $L = 200\text{pH}$ ,  $C = 150\text{fF}$ ,  $R = 400\Omega$ ,  $k = 0.5$ , the  $|Z_{21}|$  frequency response is shown in Fig. 3.3. When increasing the value of  $R_w$ , likewise, we assume that peak  $|Z_{21}|$  difference between the peaks becomes larger. While the  $|Z_{21}|$  response with  $R_w = 5$  already shows a flat region over 25GHz to 32GHz, later we will show that when the two peak values are adjusted to be equal, the overall bandwidth achieved by the transformer can be even larger. Because the gain of the amplifier's frequency response is determined by the  $Z_{21}$  of the transformer, we refer to the process of optimizing the two peaks of  $|Z_{21}|$  as gain equalization in this chapter. In the following subsections we will discuss two different methods in detail for equalizing the two peaks.

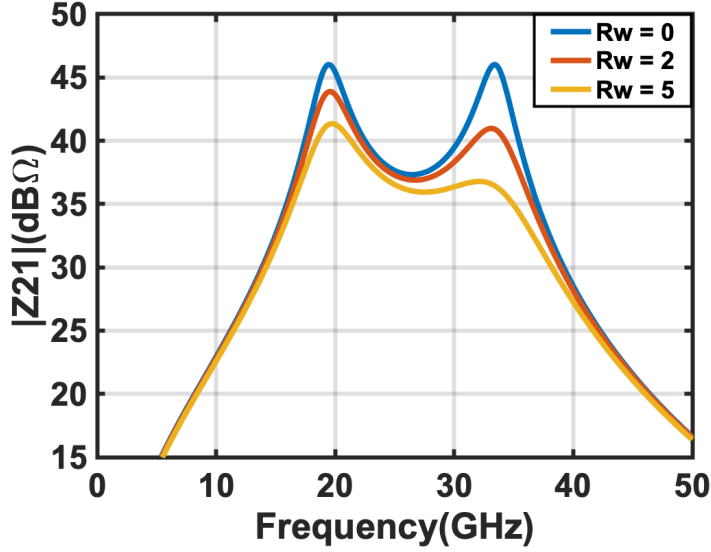


Figure 3.3: Frequency response of  $|Z_{21}|$  with different  $R_w$

### 3.3.2 Method I - Gain Equalization Based on Unmatched Transformer

The gain equalization by using the unmatched transformer has been discussed in [28]. We will show more detailed analysis and design considerations for this method. With the two windings unmatched, the LC will not be equal on both sides. Using the same notation as in [28] and [32], the ratio of the two sides' LC products is defined as:

$$\xi = \frac{L_2 C_2}{L_1 C_1} \quad (3.13)$$

The general idea of this method is to arrange for  $\xi \neq 1$ , so that the two peaks can be equalized even when  $R_{w1}$  and  $R_{w2}$  are not zero. Below we show that the  $R_{tot1}$  and  $R_{tot2}$  defined in (3.1) also need to be unequal in order to equalize the gain. The first analysis is based on the assumption that  $\xi \neq 1$  due to the different values of  $C_1$  and  $C_2$ , while the other components of both sides of the transformers are kept identical, and the  $Z_{21}$  expression that

results from (3.9) is given by:

$$Z_{21} = \frac{-(\omega_{01}\omega_{02})^{\frac{3}{2}}kQR_{tot}s}{[s\omega_{01} + Q(s^2 + \omega_{01}^2)][s\omega_{02} + Q(s^2 + \omega_{02}^2)] - k^2Q^2\omega_{01}^2\omega_{02}^2} \quad (3.14)$$

The two peak frequencies of  $|Z_{21}|$  (given in [32]) and the ratio between two peaks'  $|Z_{21}|$  (assume the  $R_1$  and  $R_2$  on both sides are infinite to simplify the expression) are:

$$\omega_{L,H}^2 = \frac{1 + \xi \pm \sqrt{(1 + \xi)^2 - 4\xi(1 - k^2)}}{2L_2C_2(1 - k^2)} \quad (3.15)$$

$$\alpha = \frac{|Z_{21,\omega=\omega_L}|}{|Z_{21,\omega=\omega_H}|} = \frac{1 + \xi + \sqrt{(1 + \xi)^2 - 4\xi(1 - k^2)}}{1 + \xi - \sqrt{(1 + \xi)^2 - 4\xi(1 - k^2)}} \quad (3.16)$$

Since  $\alpha$  will always be larger than unity, so the two peaks cannot be equalized. In order to equalize the gain,  $R_{tot1}$  should also not equal to  $R_{tot2}$ . With this condition, we will need to directly use (3.9) for solving the peak frequencies and the value of  $|Z_{21}|$  at those frequencies. To simplify the expression, we assume one side winding's resonant frequency is much higher than another side, for example,  $\omega_{01} \gg \omega_{02}$ . Under this assumption, the  $\xi$  is close to infinity in (3.13), and from (3.15) it can be find that the lower-side peak frequency  $\omega_L \approx \omega_{02}$ , and higher-side peak frequency  $\omega_H \approx \omega_{01}$ . The  $|Z_{21}|$  magnitude at these two peaks are:

$$|Z_{21,\omega=\omega_L}| = \frac{k}{\sqrt{\xi}} \sqrt{\frac{L_1}{L_2}} R_{tot2} \quad (3.17)$$

$$|Z_{21,\omega=\omega_H}| = k \sqrt{\frac{L_2}{L_1}} R_{tot1} \quad (3.18)$$

The results show that lower- (higher-) side peaks are only proportional to the  $R_{tot}$  of the windings with low (high) resonant frequency  $\omega_0$ . The ratio between  $L1$  and  $L2$  can also help equalize the gain, and here we assume that this ratio is unity. Thus the gain equalization can be performed simply by reducing the low resonant frequency side's  $R_{tot}$ . In practice, to



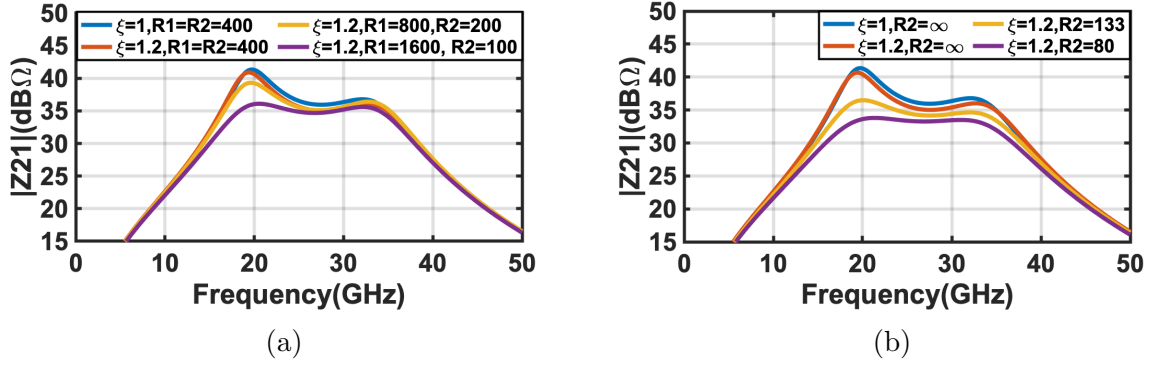


Figure 3.4: The peak-gain equalization method based on the unmatched transformer with  $\xi = 1.2$  ( $\xi = 1$  as initial condition). The fixed transformer components values are  $L_1 = L_2 = 200pH$ ,  $k = 0.5$ . (a) Equalization by increasing  $R_1$  and decreasing  $R_2$ , (b) by decreasing  $R_2$  with a fixed  $R_1 = 400\Omega$

achieve a given  $\xi$ , one can either change the values of  $R_1$  and  $R_2$  in order to equalize the gain as shown in Fig. 3.4(a), or reduce the low resonant frequency side resistance as shown in Fig. 3.4(b).

### 3.3.3 Method II - Gain Equalization Based on Resistive Coupling

The equalization method described in the previous section requires an unmatched transformer. Another set of equalization methods are based on adding the coupling components between the two sides of a matched transformer. Capacitive coupling has been demonstrated effective to equalize the gain [31]. However, the capacitive coupling could increase both bandwidth and the in-band ripple, and for some applications the bandwidth extension is not desirable for filtering purpose. In this section we will introduce the resistive coupling method to equalize the peak-gain of the matched transformer. The transformer model with the coupling resistor is shown in Fig. 3.5.

We first consider the transformer's  $Z_{21}$  when both sides are matched. We first consider the y-parameters of this network are given by:

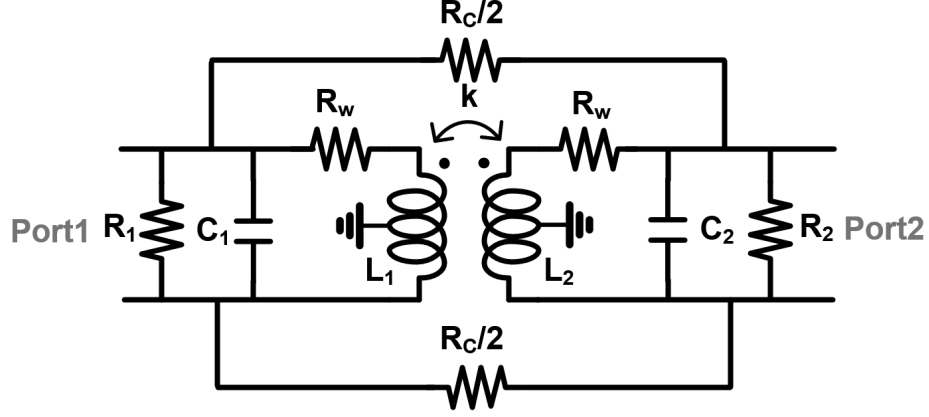


Figure 3.5: Transformer model with the coupling resistor for gain equalization

$$Y_{11} = Y_{22} = \left( \frac{1}{R_{tot}} + \frac{1}{R_C} \right) + \frac{1}{sL(1-k^2)} + sC = \frac{1}{R_{tot,c}} \left( 1 + Q \left( \frac{s}{\omega_0} + \frac{\omega_0}{s} \right) \right) \quad (3.19)$$

$$Y_{12} = Y_{21} = -\frac{k}{sL(1-k^2)} - \frac{1}{R_C} - \frac{k\omega_0 Q}{sR_{tot,c}} - \frac{k_R}{R_{tot,c}} \quad (3.20)$$

where

$$R_{tot,c} = R_{tot} || R_C \quad (3.21)$$

$$k_R = \frac{R_{tot}}{R_{tot} + R_C} \quad (3.22)$$

$$\omega_0 = \frac{1}{\sqrt{L(1-k^2)C}} \quad (3.23)$$

$$Q = \frac{R_{tot,c}}{\omega_0 L(1-k^2)} = \omega_0 R_{tot,c} C \quad (3.24)$$

The expression of  $Z_{21}$  is:

$$Z_{21} = \frac{QkR_{tot,c}s\omega_0^3 - k_R s^2 \omega_0^2}{[Qs^2 + s\omega_0(1+k_R) + Q(1+k)\omega_0^2][Qs^2 + s\omega_0(1-k_R) + Q(1-k)\omega_0^2]} \quad (3.25)$$

The two peak frequencies are:

$$\omega_{L,H} = \frac{1}{\sqrt{LC(1 \pm k)}} \quad (3.26)$$

When  $k < 0$ , the two peaks' magnitude are:

$$|Z_{21,\omega=\omega_L}| = \frac{1}{2} \left( \frac{L(1+|k|)}{R_w C} ||R||R_C \right) \quad (3.27)$$

$$|Z_{21,\omega=\omega_H}| = \frac{1}{2} \left( \frac{L(1-|k|)}{R_w C} ||R||R_C \right) \quad (3.28)$$

The results shows that the lower-side peak can be reduced by adding a coupling resistance  $R_C$ , but the higher-side peak magnitude will not be influenced by the added  $R_C$ . In this way, the peak-gain can be equalized. In addition, the peak-gain frequencies (4.18) are the same as (3.10), which means the resistive coupling doesn't influence the peak-gains' frequencies.

When  $k > 0$ , the two peaks' magnitude are:

$$|Z_{21,\omega=\omega_L}| = \frac{1}{2} \left( \frac{L(1+|k|)}{R_w C} ||R||R_C \right) \quad (3.29)$$

$$|Z_{21,\omega=\omega_H}| = \frac{1}{2} \left( \frac{L(1-|k|)}{R_w C} ||R||R_C \right) \quad (3.30)$$

Similarly, when  $k > 0$ , the higher-side peak will be reduced by the added  $R_C$ , leading to a larger difference between the two peaks. As a result, the resistive coupling only works for the transformer with  $k < 0$ . Fig. 3.6 shows the equalization example for both positive and negative  $k$  values.

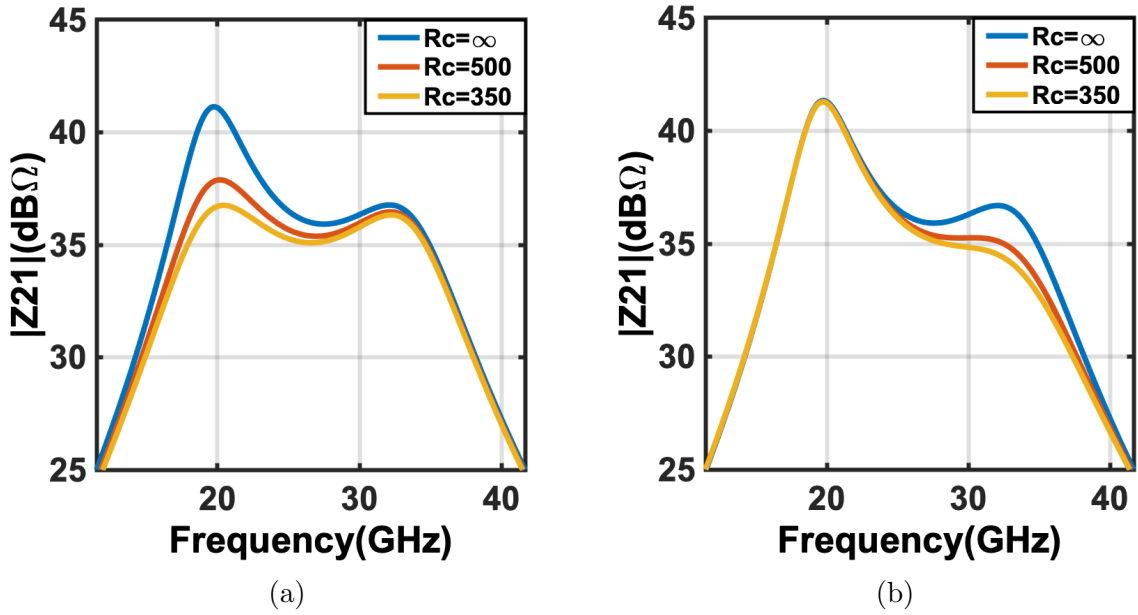


Figure 3.6: the equalization by using resistive coupling. The fixed transformer component values are:  $L = 200pH$ ,  $C = 150fF$ ,  $R = 400\Omega$  with (a)  $k = -0.5$ , and (b)  $k = 0.5$ .

## 3.4 Circuits Design

### 3.4.1 Trasceiver System And Circuits

A single-pole-double-throw (SPDT) switch is designed to switch between the Rx and Tx modes. In general, the switch is designed to exhibit good isolation between the Tx and Rx, while also introducing low loss. A parallel-switch based structure is used as shown in Fig. 3.7. The structure contains one single-ended quarter-wavelength T-line, with the PA's load directly connected to the RF pad. Compared with the typical architecture where both Tx and Rx sides are identically connected to the quarter-wavelength T-line [33], the benefits without the Tx side T-line can help reduce the propagation loss of the PA's output signal, which improve the PA's efficiency. To further reduce the loss seen by the PA's output, the RF pad is implemented very close to the PA's load, in order to minimize the trace-introduced finite losses. In Tx mode, the T-line can transform the small impedance introduced by the parallel on-state switch to a high impedance, thus ensuring that the majority of the PA's

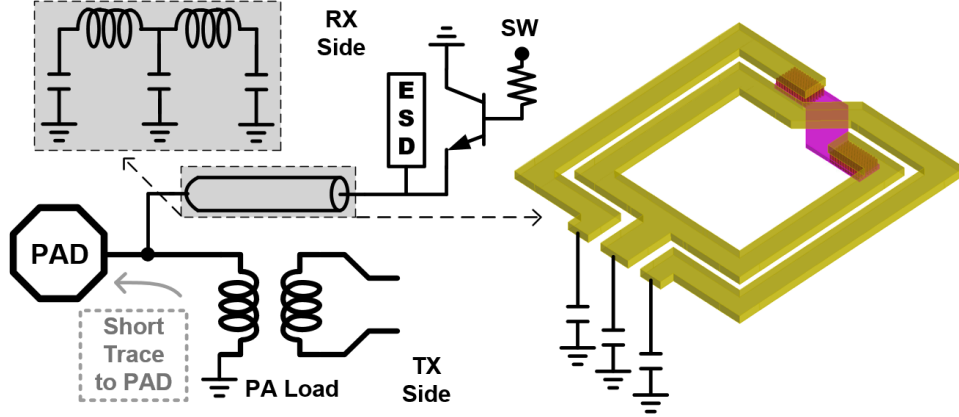


Figure 3.7: The SPDT RF switch with an area efficient artificial quarter-wavelength T-line.

output power is delivered to the pad. The quarter-wavelength T-line implementation at the Rx side, which takes less chip area than a distributed T-line, is implemented using the artificial delay line (L and C sections). The bandwidth of the LC section (critical frequency discussed in [34, 35]) is important. If the quarter wavelength T-line is implemented by just one LC section, the critical frequency  $f_c = \pi\omega_n$  and the center operating frequency  $f_0 = 4\omega_n$  are very close. Here the  $\omega_n$  is the resonant frequency of each the LC section. For wideband applications, it may introduces more loss at high frequency part of the band. To reduce this effect, the delay line is designed to have two smaller LC sections instead of one. In this way, the  $f_c$  of each section will be doubled, and a flat response can be obtained within a wider bandwidth . To further reduce the area of this quarter-wavelength T-line, as shown in Fig. 3.7, a capacitor is connected at the center tab of the inductor to avoid implementing two smaller inductor separately. The parallel switch BJT are connected in the reverse-saturated way to farther increase the off-state resistance [36].

The first block of the Rx is a two-stage LNA as shown in Fig. 3.8, where the first stage is a stacked common-emitter amplifier with inductive degeneration. The load of the first stage is a single-end-to-differential transformer. To equalize the peak gain, an unmatched transformer based equalization is used. The difference between  $R_1$  and  $R_2$  of the two sides of this transformer is proportional to the coupling coefficient  $k$ . With the desired flat response

band from 26.5GHz to 29.5GHz, the  $k$  is designed around -0.4 to keep a flat bandwidth without adding too small parallel resistor. It is achieved by, as shown in Fig. 3.8, offsetting the two windings to reduce the overlap between them. Two identical resistor  $R_T$  is added on the differential output side to equalize the peak gain. The second stage is a differential amplifier with stacked transistors. The load of the second stage is designed based on the matched transformer with the resistive coupling. A capacitor is inserted in series with each coupling resistor in order to isolate the different DC levels on each side. To implement this transformer with the additional resistive coupling path, the trace through the bottom metal layer (Metal1) is added with the desired resistor and the capacitor. In order to keep the structure symmetric, the coupling resistor is equally split between the two sides of the capacitor. Though the Metal1 layer has a higher sheet resistance than the top metal layers, that added resistance is already in series with the larger coupling resistance. The use of lower layer can also reduce the coupling between the resistive coupling path with the transformer.

Following the two-stage LNA a double-balanced mixer, which is designed to have a  $52\Omega$  load to match to the following T-lines for the power combining. Due to the fact that the Rx mixer output is connected to the Tx mixer input, and also will need to be connected to the power combiner/splitter, the matching at the output node will be important. One simple way is to implement series switches between the two stages. This way, each side can match to a power combiner individually in either Tx or Rx mode. However, since the IF band is 5 to 8GHz, the 0.18um CMOS based series switch will introduce relative higher loss at this frequency band. As a result, it is not realistic to implement any switches in between those two mixers. The solution is shown in Fig. 3.9. With the  $52\Omega$  of the Rx down-converter's load resistance directly connected to the Tx mixer input through the DC blocking capacitors, the impedance will match to  $50\Omega$  when one of the mixer is turned off (by changing the biasing voltage of the mixer to 0V).

The power combiner is used for combining (splitting) the down (up) converted IF signals. The

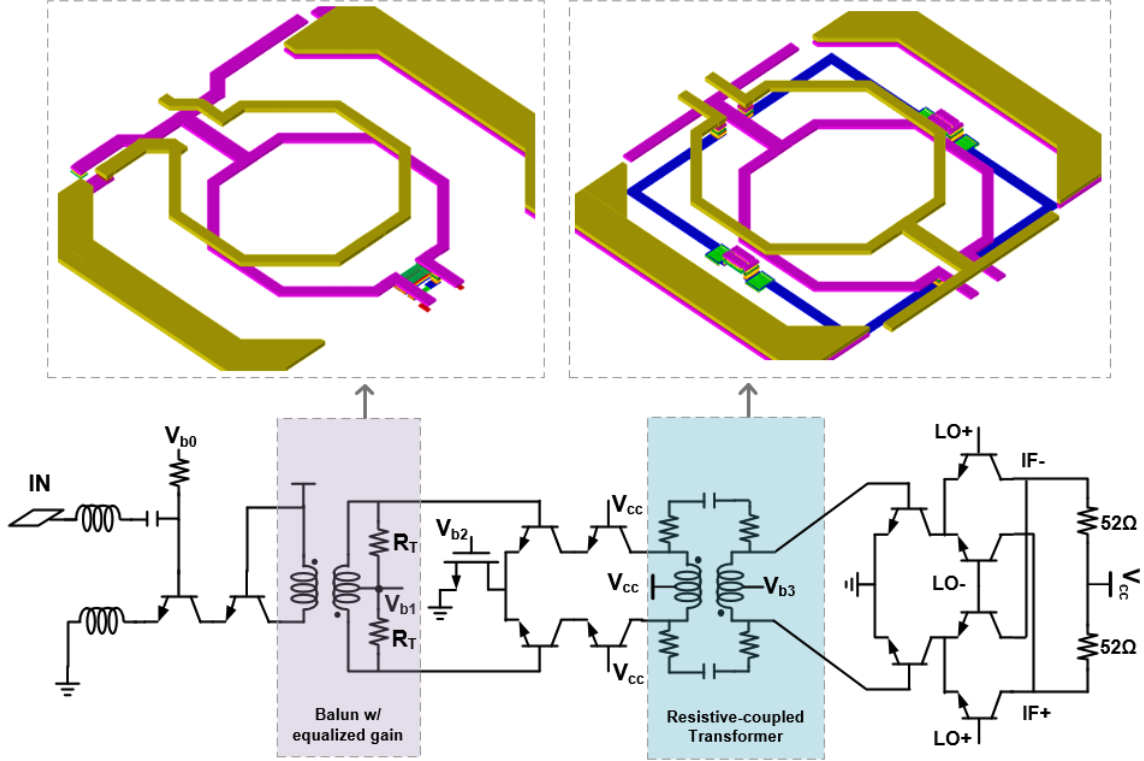


Figure 3.8: The receiver schematic with two-stage LNA and the mixer.

conventional Wilkinson power combiner is not sufficient to cover the desired IF band from 5GHz to 8GHz. The bandwidth of the Wilkinson can be extended by using the wideband topology [37, 38] as shown in Fig. 3.10(a). This structure contains two types of a quarter-wavelength T-line: with  $Z_T = 70.7\Omega$  and the other with  $Z_0 = 50\Omega$ . The T-line's center frequency is 6.5GHz, which means it will consume a very large area and will not be practical for the on-chip implementation. The solution, similar to the SPDT's T-line design, is to use a two-section artificial delay line in which the critical frequency can be shifted beyond 9GHz, thereby satisfying the required bandwidth. While the required inductor's size is relatively large, it is far smaller than the distributed one, which becomes practical to be implemented on chip. The entire wideband Wilkinson combiner structure is implemented on different locations throughout the chip to reduce the chip area. And the implementation for each sections of the T-line is circled on the die photo shown in the Fig. 3.18 with the same color circled in Fig. 3.10(a) correspondingly. The matching results for the input/output of the

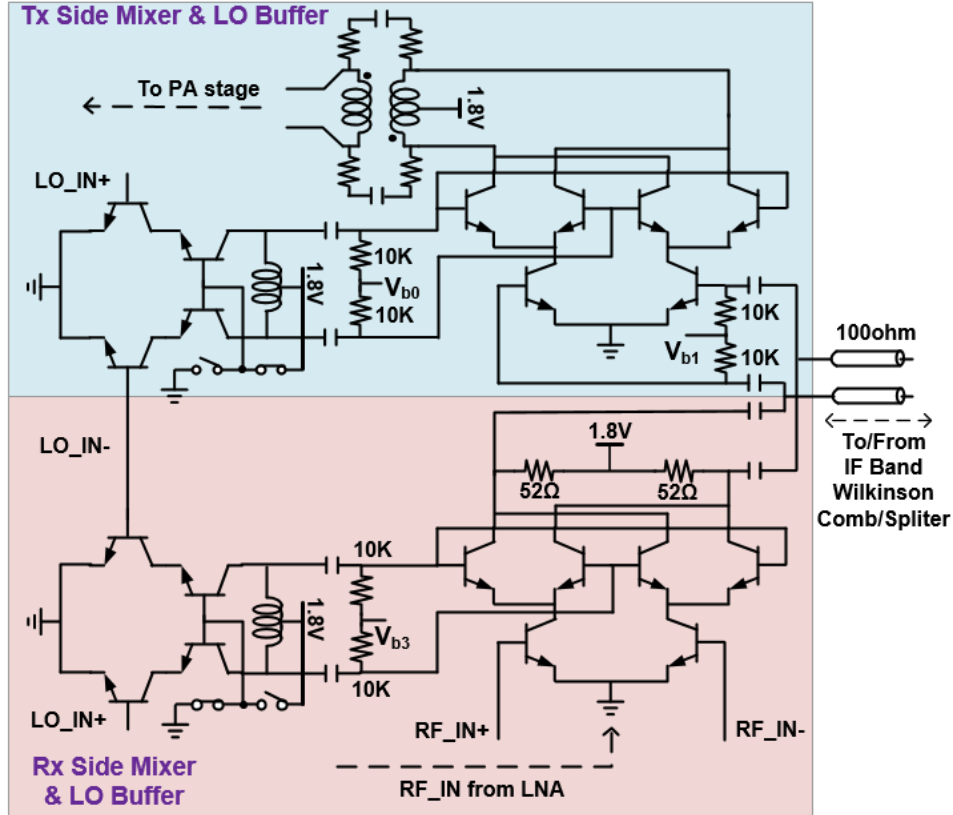


Figure 3.9: Tx and Rx side mixers and LO buffers.

combiner are shown in Fig. 3.10(b) with the measured  $S_{11}$  from the differential IF pads. It achieves less than -10dB  $S_{11}$  and  $S_{22}$  over a bandwidth of 2.5-9.5GHz, and a flat 7.7dB loss (simulated) from the input port to the four output ports over this bandwidth. Together with the combiner/splitter, the measured overall Rx gain is shown in Fig. 3.11(a). The measured results verify that the receiver achieves a flat gain (within 1dB variation) over the desired RF band, 26.5-29.5GHz. The measured results obtained a smaller bandwidth compared with the simulation, resulting in more roll-off at the lower frequency side. In Fig. 3.11(b), simulated NF values for the condition with and without the RF switch is shown. The simulation results shows the RF switch introduces around 1.7dB loss at the front of the Rx, which directly increases the Rx's NF, and this figure also shows the measured NF of single Rx channel. Fig. 3.11(c) shows the input matching performance. The measured  $S_{11}$  peak is about 10% lower than the simulated results, and exhibits a good matching over 23.5-28.5GHz.



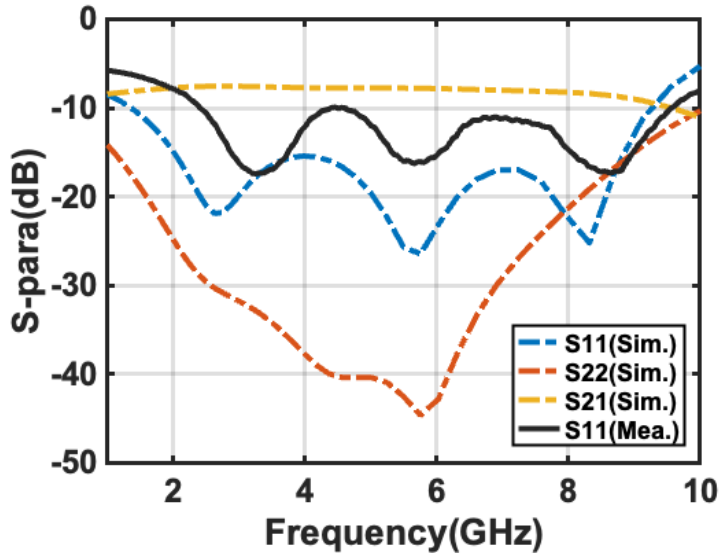
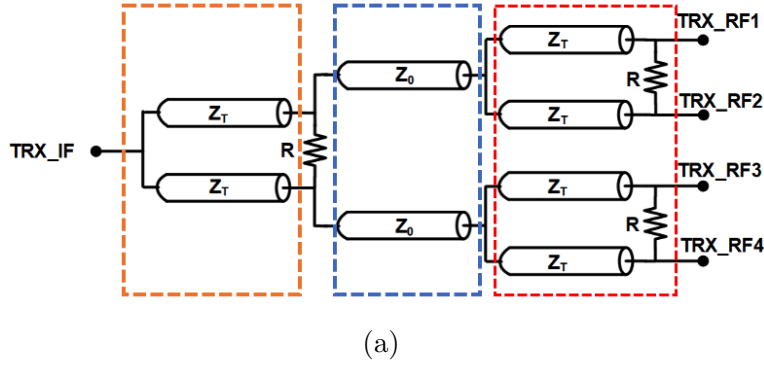


Figure 3.10: (a) wide-band Wilkinson power combiner/splitter with single-ended drawing. The circled T-lines with different colors are also circled on the die photo correspondingly on Fig. 3.18; (b) the S-parameters of the combiner/splitter, the port 1 and 2 are the TRX\_IF and TRX\_RF1 port in (a).

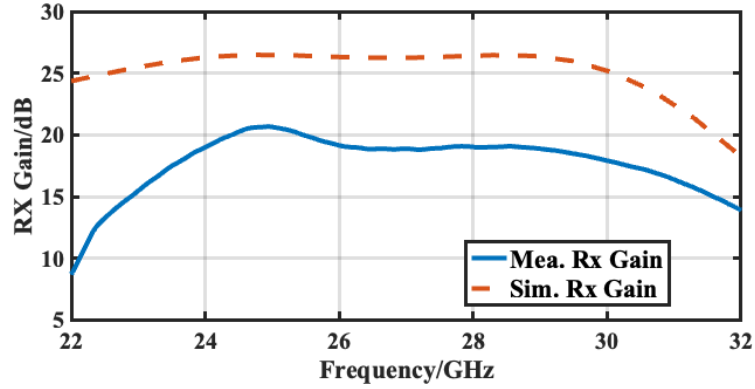
For the Tx, the critical block is the power amplifier. A class-AB PA is targeted to achieve high PAE, high output power and a good AM-AM and AM-PM distortion at the compression point. As shown in Fig. 3.12, the PA contains two stages. The drive-stage is a differential pair with a transformer load, in order to keep a flat gain over the RF band. The neutralization capacitors are used for both the driver stage and the PA stage to improve the stability. The inductive source degeneration is used to reduce the AM-to-PM distortion. An additional small resistor is added at the base terminal of the PA-stage's transistor to further improve the stability of the PA. Fig. 3.13 shows the main measured parameters of the PA. The PAE

at the 1dB compression point is 7.6%, the peak PAE value is 13.2%, and the saturated output power is 11.6dBm. The DC power used for calculating the PAE includes both DA and PA stages, and the Tx gain measurement also includes the conversion mixer stage's gain, together with the DA and PA. The AM-PM distortion at the 1dB compression point is 8.2°. The Tx gain simulations and measurements are shown in Fig. 3.14(a) and (b). The gain and output compression power are flat (within 1dB difference) over the desired RF frequencies. The modulation test for single-channel Tx performance is also performed by sending a 100MS/s 16QAM modulated signal to the system. The constellations (16-QAM) associated with different Tx power backoff values are shown in Fig. 3.15. It shows that the linear output power requires 8dB back off from the saturated output power.

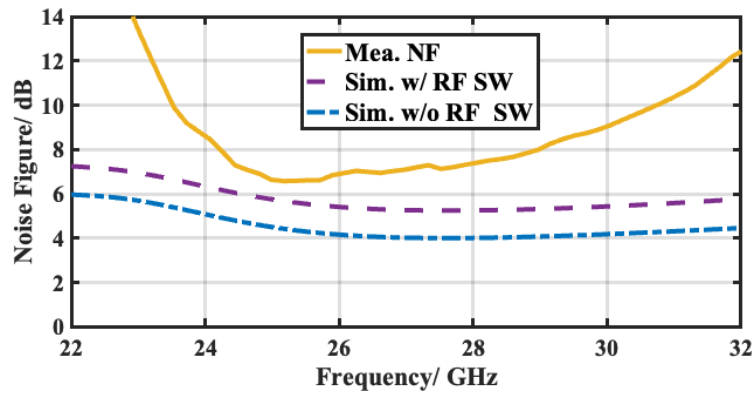
### 3.4.2 LO Amplifier Chain and Phase-Shifter

The phase shifter plays important roles for the beamforming, and prior works have discussed phase shifter design by using the active or passive cells [39–43]. As shown in Fig. 3.16(a), the received single-ended LO signal will be amplified by the single-ended LNA and converted to differential by the load balun. The LNA is followed by a VGA, which provides sufficient gain for LO amplification. The gain could also be provided by the following phase interpolators and buffers. However, this approach would require four times more power as compared to the buffers than using the shared VGA. To reduce the power consumption, we allocate as much gain as possible to the VGA stage. At each transceiver side, there are independent LO buffers for both Tx and Rx, which will be turned on corresponding to the Tx/Rx mode.

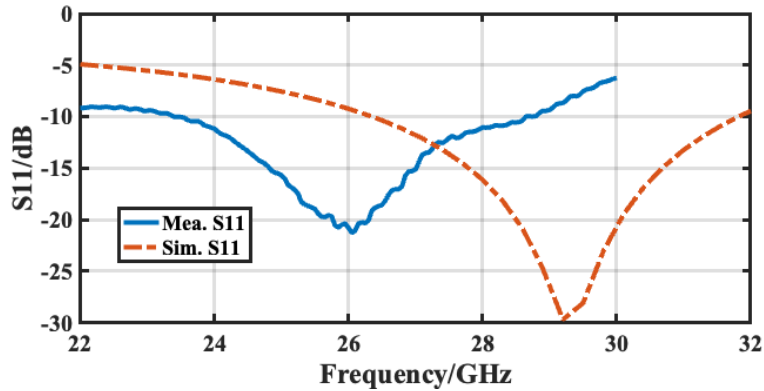
A quadrature phase generator (QPG) generates the quadrature signals from the differential inputs by using a two-stage passive RC. Then the four quadrature signals will be fed to an 11-bit controlled phase-interpolator as shown in Fig. 3.16(b). For each I and Q phase combination, the different weights only need to achieve 90° phase shifting with certain resolution.



(a)



(b)



(c)

Figure 3.11: (a) Simulated and measured Rx gain; (b) the noise figure of the Rx, simulation results compared w/o and w/. the RF switch's NF; (c) input S11.

The control bit S0 selects the phase either 0 or 180°, and S1 selects either I or Q phase. A cascode low-voltage current mirror [44] topology is used here to obtain good current matching. Control bits S2-S4 set the transconductance weights of the I and Q branches, and the

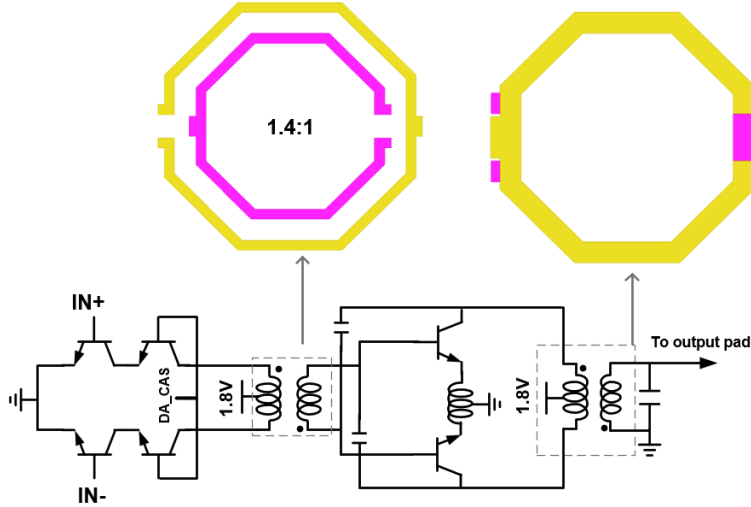


Figure 3.12: Schematic of two-stage class-AB PA.

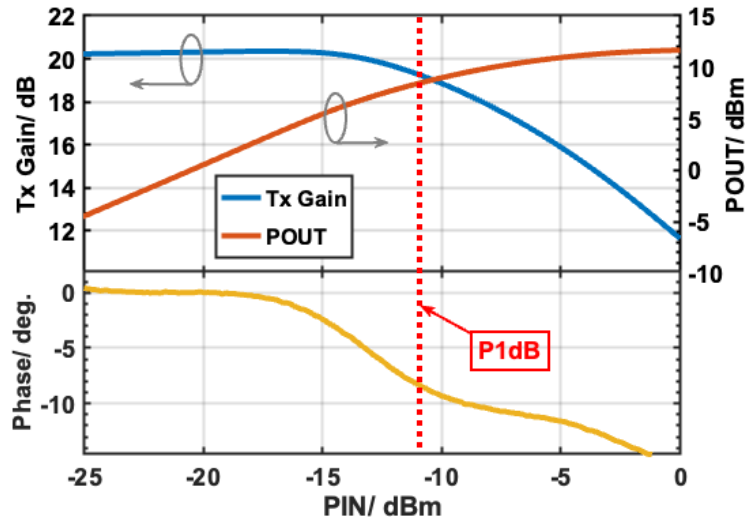
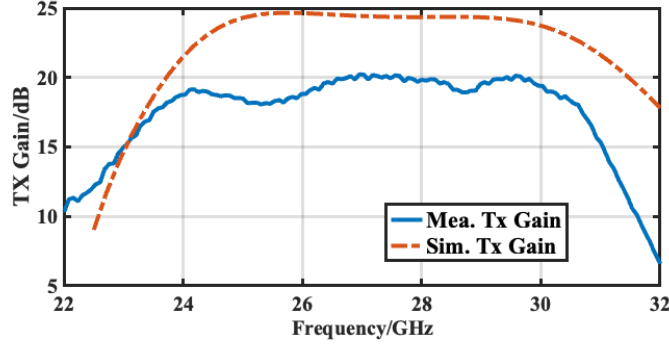
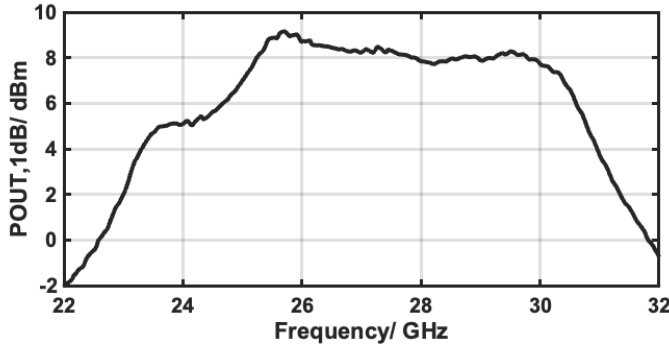


Figure 3.13: Measurement results (at 28GHz) of the Tx's gain (include mixer), the output power, and the output phase.

active part of the phase interpolator can achieve  $0 - 360^\circ$  phase shift with a step size of  $22.5^\circ$ . To achieve finer resolution, control bit S5 sets the capacitance at the load to achieve an  $11.25^\circ$  step size. For achieving even finer phase shifting resolution, one simple way is to use the capacitor bank at the load of the phase interpolator with smaller size. However, with small-sized capacitors, the mismatch between the design and the fabrication results can be



(a)



(b)

Figure 3.14: (a) Simulated and measured Tx gain; (b) output compression power over frequency.

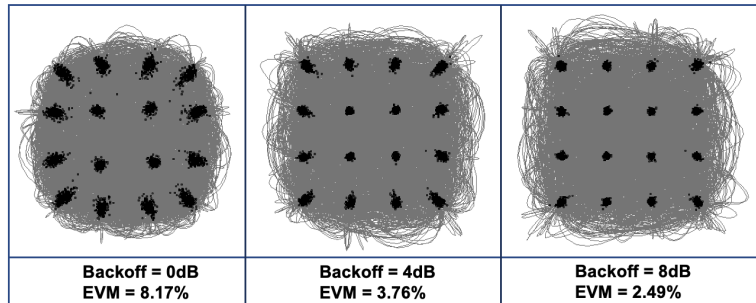


Figure 3.15: Measurement results of 16QAM of Tx output with different power backoff.

large. To improve the accuracy of realizing  $1^\circ$  phase shifting resolution, the delay-variable T-line is used to achieve overall  $11^\circ$  phase shift with  $1^\circ$  resolution. The capacitor used for each section of the delay element is larger than that used in the capacitor bank for directly achieving  $1^\circ$  phase shifting, which improves the accuracy. To further prevent variation and mismatch of the delay-variable T-line, an additional delay-variable section has been added

with  $0.5^\circ$  phase delay for calibration.

The load of the phase interpolator is a transformer directly matched to a variable-delay T-line. The unit cell of this T-line is a fixed  $L$  with an  $C_x$  that can be included when switch is on. The delay time can be selected between the  $\tau_1 = \sqrt{LC}$  and  $\tau_2 = \sqrt{L(C + C_x)}$ . On the other hand, the characteristic impedance  $Z_0$  of each unit cell will reduce from  $Z_{01} = \sqrt{\frac{L}{C}}$  to  $Z_{02} = \sqrt{\frac{L}{C+C_x}}$ . For a fixed  $L$ , the  $C_x$  can be designed to be sufficiently small to prevent large  $Z_0$  variation, but the variable delay achieved by each unit will be small, requiring in more unit cells to achieve the same amount of the phase shifting, which consumes a larger chip area. The design target of the unit cell is to achieve a larger delay difference between  $C_x$  switch on and off, while maintaining good matching for both conditions. To achieve this, the differential  $Z_{01}$  of the T-line (without the  $C_x$ ) is designed to be  $130\Omega$ . With the  $C_x$ ,  $Z_{02}$  drops to  $70\Omega$ , both conditions achieve return loss  $< -20\text{dB}$ . Fig. 3.16(c) shows the layout of this delay variable T-line. Each unit cell of the T-line is implemented in "S" shape to save area. Though the impedance is not uniform along this S shape T-line, the overall section can provide the desired impedance and the phase delay as well. The whole delay variable T-line is implemented in serpentine-shape to constrain the structure into certain area. The output of the shifted LO will feed to each transceiver's LO buffers. The LO buffers (differential pair) are designed using the HBT device to provide adequate gain at the LO frequency. Fig. 3.17 shows the simulated gain and amplitude variations at the output of the LO buffer. The phase rms error is less than  $0.68^\circ$  and the rms gain variation is below  $0.085\text{dB}$  over  $24\text{-}30\text{GHz}$ .

### 3.5 MIMO System Measurement Results

A 2-by-2 MIMO transceiver chip has been fabricated using the TowerSemi  $0.18\ \mu\text{m}$  BiCMOS process that includes HBT device with  $f_T = 240\ \text{GHz}$ . The die photo is shown in Fig. 3.18. The total chip area is  $4.3 \times 3\text{mm}^2$ , with each transceiver block taking  $1.7 \times 1\text{mm}^2$  and the

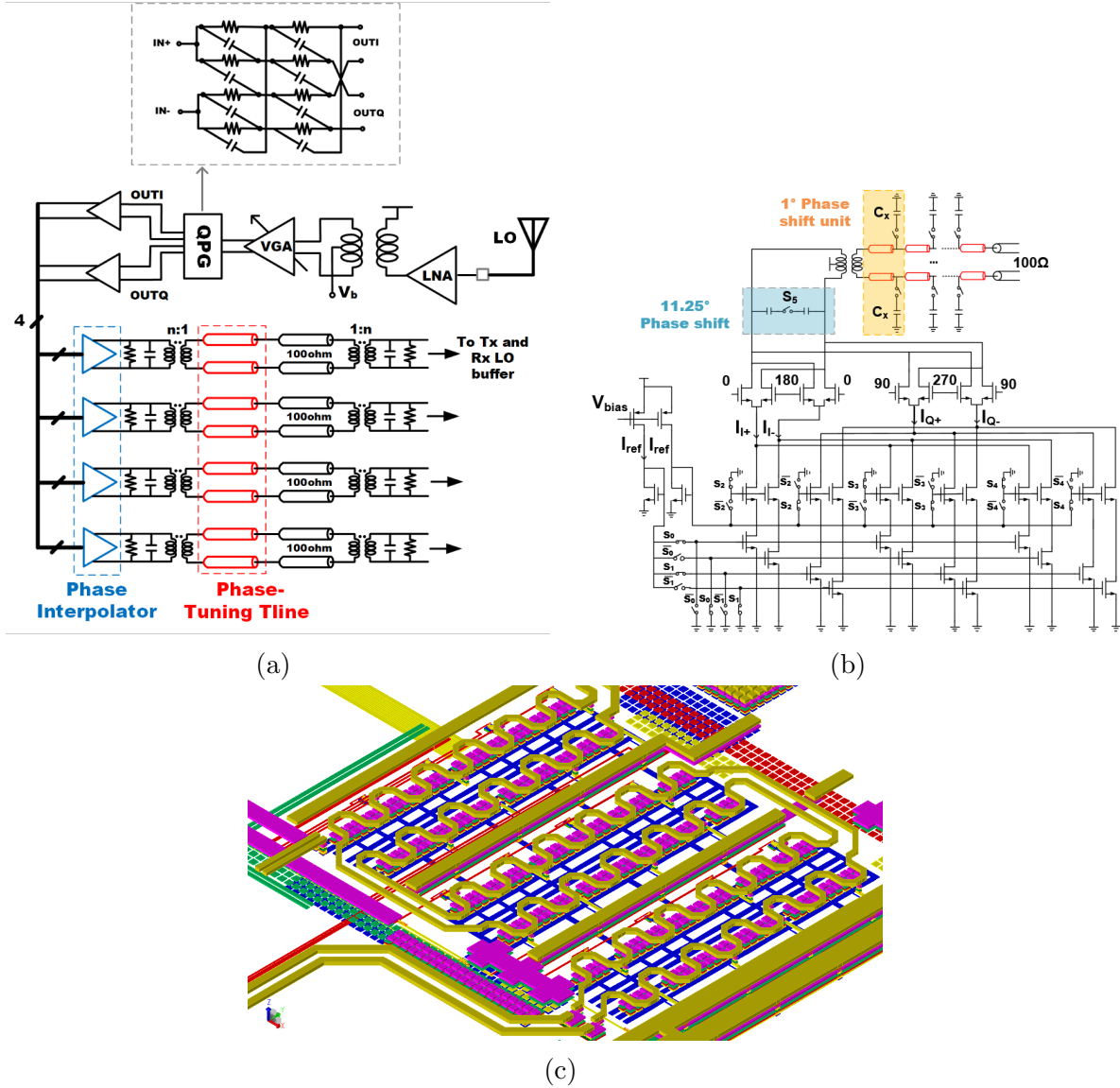
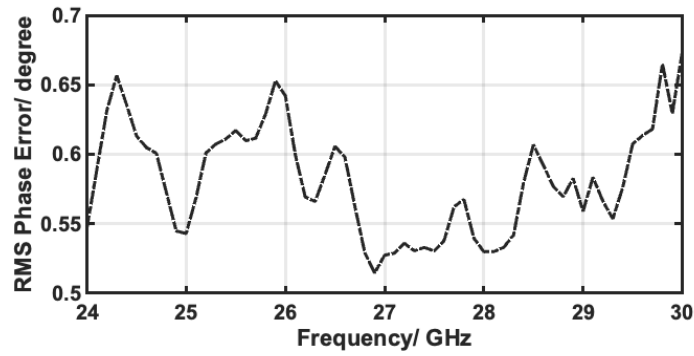


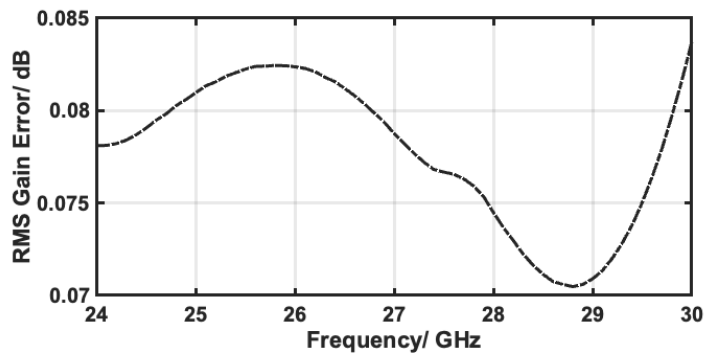
Figure 3.16: (a) LO amplifying and phase shifting system; (b) the circuits of the phase interpolator together with the phase-tuning T-line.

LO amplifying chain together with the phase shifter taking around  $2.2 \times 1.2\text{mm}^2$ .

The PCB used for measurements is shown in Fig. 3.19, which enables both onboard measurement through cables and wireless measurement using four antennas implemented on the back side of the PCB for each channel. The die is attached to the PCB by using flip-chip techniques in order to greatly reduce the interconnection impedance between the die and the board. The measured normalized array radiation pattern for both H-plane and E-plane



(a)



(b)

Figure 3.17: The simulation results of the (a) phase rms error; (b) maximum gain difference.



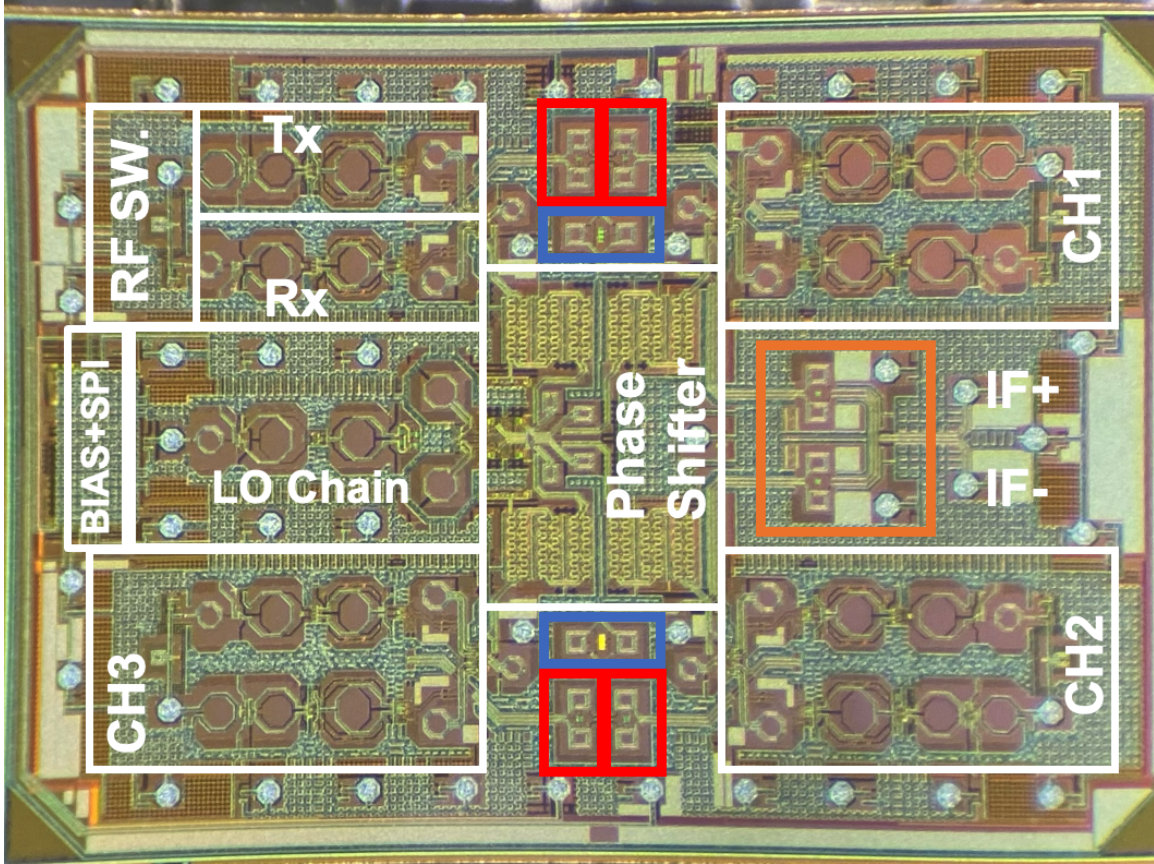


Figure 3.18: Die photo of the 2-by-2 MIMO system. The colored box circles are the different artificial quarter-wavelength T-line sections appeared in Fig. 3.10(a) with the corresponding colors.

are shown in Fig. 3.20. The results show that this four antenna array realizes a beamwidth (3dB) of  $42^\circ$  for E-plane and  $62^\circ$  for the H-plane. The H-plane beamwidth can be further optimized. And with the increasing of the array size, the array's beamwidth can be reduced.

The modulation test has been performed for both single channel Tx-to-Rx through the cable, and also the entire system Tx-to-Rx through the antenna array. The test setup for both measurements are shown in Fig. 3.21. The measured constellation diagram for both measurements are shown in Fig. 3.22. The system performance comparison with the other MIMO transceiver works at the same frequency range is shown in Table 3.1. Compared with the other work, this work achieves a higher Tx/Rx gain and good phase-shifting resolution with a moderate power consumption.

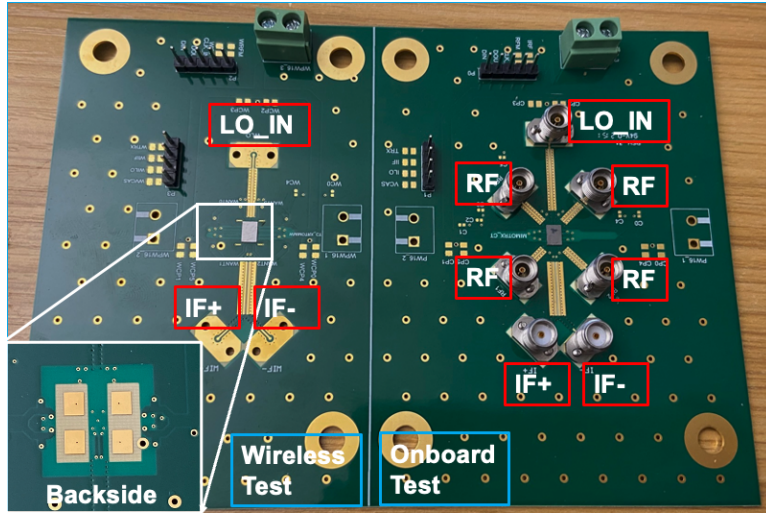
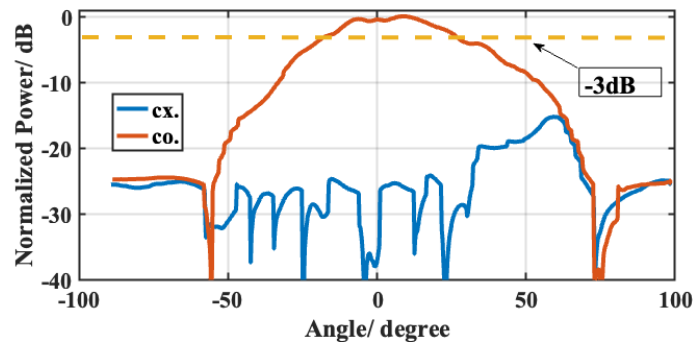


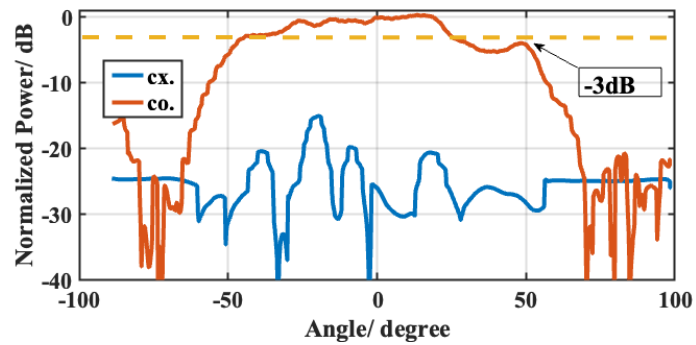
Figure 3.19: PCB design for measuring the die.

Table 3.1: PERFORMANCE COMPARISON WITH OTHER 28-GHz TRANSCEIVERS

Comparison Table	This work	[24]	[25]	[23]
Process	0.18um SiGe	65nm CMOS	28nm CMOS	0.18um SiGe
P1dB/ch.	7.8dBm	15.7dBm	12dBm	10.5dBm
Psat/ch.	11.6dBm	18dBm	14dBm	12.5dBm
Tx Gain/ch. @28GHz	20dB	10dB	15dB	17dB
Tx DC/ch.	167.8mW	299mW	119mW	200mW
NF	6.8dB	4.1dB	4.4dB	4.6dB
RX Gain/ch. @ 28GHz	19dB	12dB	15dB	17dB
RX DC/ch.	93mW	148mW	42mW	130mW
Phase Res.	1	0.3	45	6
Constellation	64-QAM	64-QAM	64-QAM	64-QAM
Symbol Rate, Max (GS/s)	400MS/s	2.5GS/s	400MS/s	1.5GS/s
Tx-to-Rx EVM	9%	1.7%	0.9%	6.1%
Chip Area	12.9mm <sup>2</sup>	12mm <sup>2</sup>	29mm <sup>2</sup>	12mm <sup>2</sup>

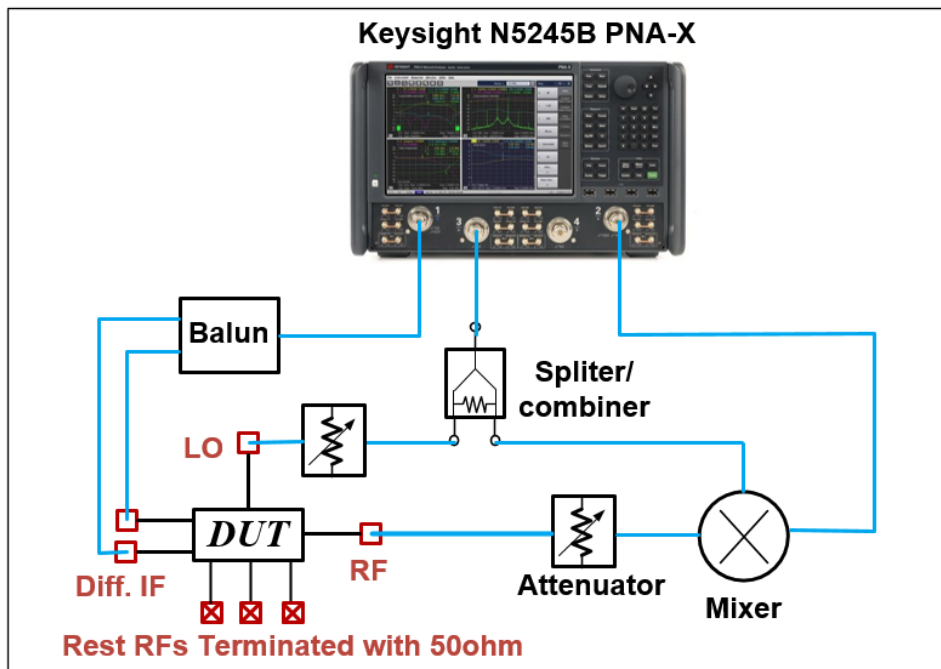


(a)

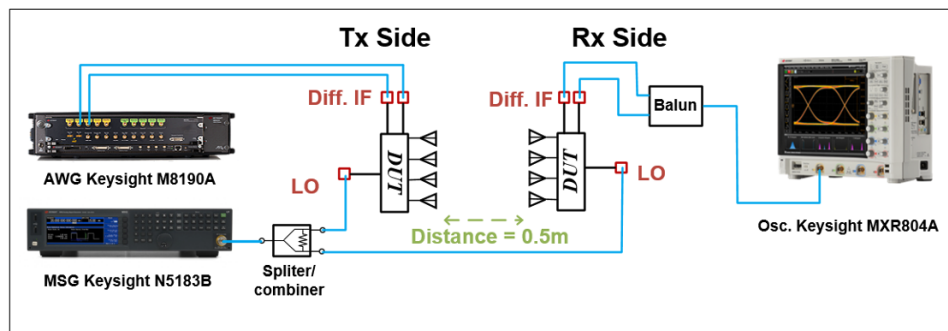
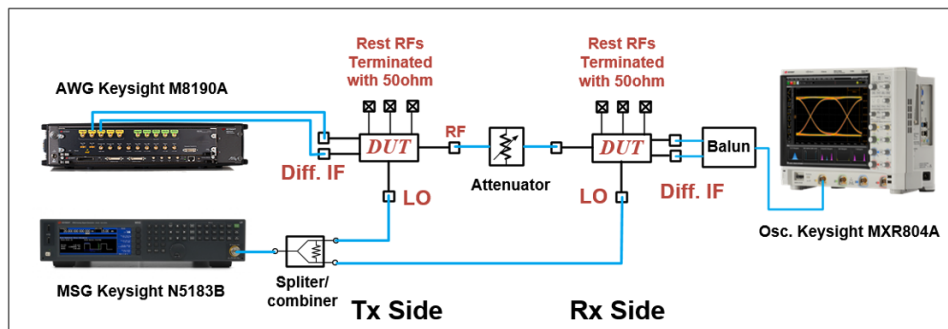


(b)

Figure 3.20: Measured antenna array radiation pattern at 27.5GHz of (a) E-plane with both co-polar and cross-polar; (b) H-plane with both co-polar and cross-polar.

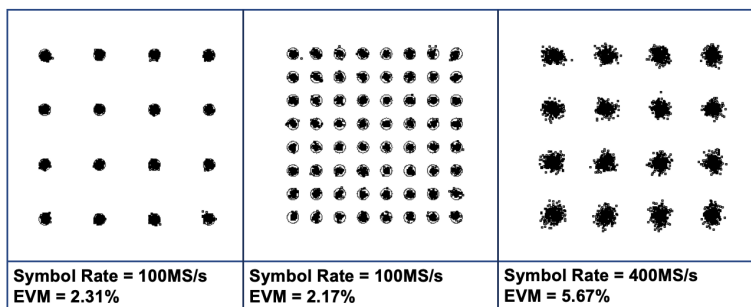


(a)

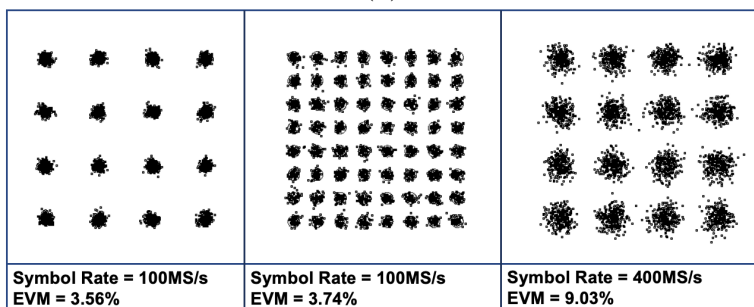


(b)

Figure 3.21: Measurement setup for (a) single-chip measurement and (b) modulation test of Tx-to-Rx EVM for both single-channel 2-by-2 antenna array.



(a)



(b)

Figure 3.22: Measured Tx-to-Rx constellation of (a) single channel and (b) antenna array.

# Chapter 4

## Modeling the Frequency Behavior of the Two-Stage Transimpedance Amplifier's Odd-Order Nonlinearity

### 4.1 Introduction

Linearity is critical for the baseband amplifier in a wireless transceiver system. For example, in the receiver, it is used to amplify signals coming from the last mixer and provide adequate output swing for the following ADCs. To improve the linearity of the baseband amplifier, instead of using a voltage-mode amplifier, the transimpedance amplifier (TIA) becomes attractive because its input can be a large current with relatively small voltage swing. [45] presents the low distortion performance of a closed-loop two-stage differential TIA, as well as a way to model the nonlinearity at low frequencies. With the ever-increasing demand for the communication data rate, wider bandwidth with good linearity is required for baseband amplifiers. In many cases, it becomes harder to achieve good linearity as the frequency

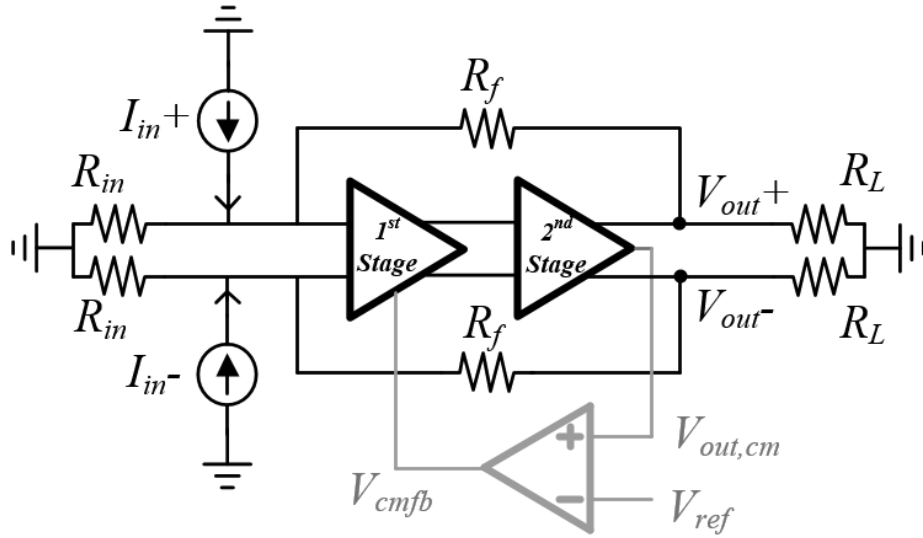


Figure 4.1: The two-stage closed-loop TIA topology.

increases. An example of a TIA circuit, including a common-mode feedback circuit (CMFB) circuit, is shown in Fig. 4.1. The details of this system will be discussed in the following sections. Fig. 4.2 shows how the 3-dB bandwidth decreases as the TIA's input current amplitude is increased. The results indicate that the nonlinear distortion will have larger influence at higher frequencies.

Research works have modeled the nonlinearity of the multistage amplifiers at high frequencies [46–53], and most of those works studied the second- and third-order nonlinearities of a multistage amplifier. One method to analyze the distortion due to weakly nonlinear sources in the frequency domain is the Volterra series [53–56]. However, as mentioned in [48], this method is complex and difficult to apply, particularly when the circuits have a large number of nonlinear elements, is in the case for multistage amplifiers. As a result, in this work, we directly analyze the nonlinearities in a feedback loop, similar to [46] and [47], without using the Volterra series. In this chapter, we give a complete analysis of the different nonlinearity sources, together with the detailed analysis of the poles and zeros of the multistage amplifier. Moreover, the interactions of the harmonics are also discussed.

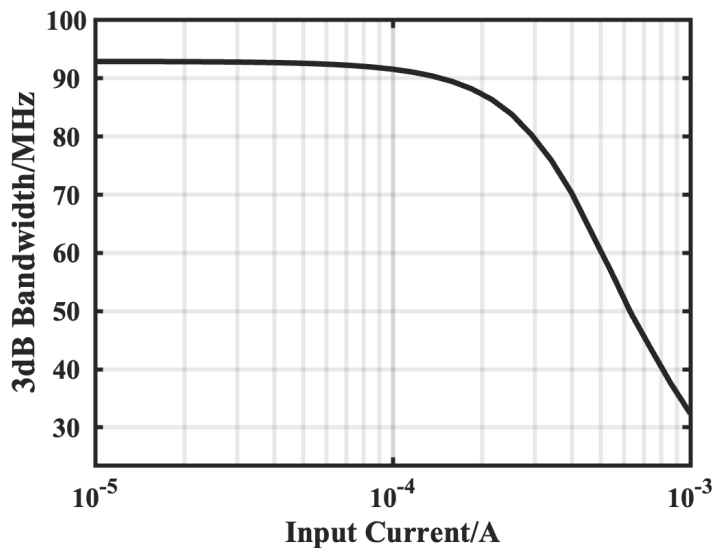


Figure 4.2: Large-signal TIA bandwidth vs. input current amplitude.

This chapter is organized as follows: in Section 4.2 a general model for the odd-order nonlinearities of a single-stage amplifier is discussed. Based on this model, Section 4.3 models the closed-loop frequency behavior of an entire two-stage TIA, and the developed model is compared to the simulation.

## 4.2 General Nonlinearity Model of a Single-Stage Amplifier

The conventional method of modeling a nonlinear amplifier is to characterize the entire amplifier with a linear gain and a set of nonlinear coefficients that determines the different orders of harmonics, without distinguishing the sources of the nonlinearity. However, this way of modeling will not be sufficient for modeling the frequency behavior of the harmonics. In fact, depending on the origins of those nonlinearities, their frequency responses are different. In this section, we first model the frequency behavior for both nonlinear resistor and capacitor in a one-pole system. Then we show the frequency behavior of the nonlinearity that originates



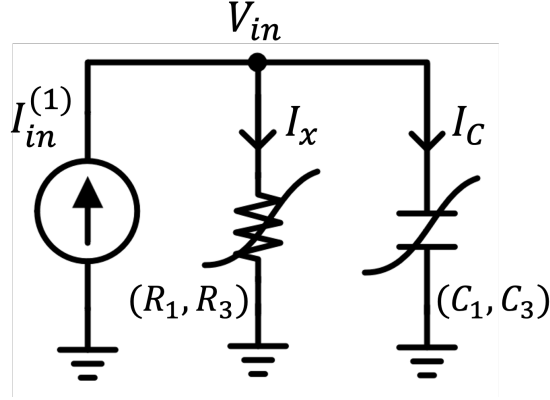


Figure 4.3: Frequency response verification of network with nonlinear R or nonlinear C.

from the nonlinear transconductance of the differential amplifier. A new model is introduced with the separation of those different nonlinearities. Finally, we apply this new model to the first and second stages of the TIA.

#### 4.2.1 Definition of the Input- and Output-Related Nonlinearity

In general, both passives and actives will introduce nonlinearities to the amplifier. For the passives, the two main sources are the nonlinear resistor and the capacitor. The following two examples model the frequency behavior for both nonlinear resistor and capacitor in a one-pole system. To simplify the model, only 3<sup>rd</sup>-order nonlinearity is studied for those nonlinear components, but generalizing to higher order nonlinearities is straightforward.

Firstly, we study the frequency response of the parallel connection of a nonlinear resistor and capacitor. As shown in Fig. 4.3, a single-tone current  $I_{in}(t) = I_{in}^{(1)} \sin \omega t$  is applied to the RC network. The resistor and capacitor in the figure are modeled with coefficients  $(R_1, R_3)$  and  $(C_1, C_3)$ , respectively, where  $R_1$  and  $C_1$  represent the resistor and capacitor's linear values, and the  $R_3$  and  $C_3$  are their 3<sup>rd</sup>-order nonlinear coefficients. To study the nonlinear resistor's influence, we will first keep the capacitor linear; i.e., set  $C_3 = 0$ . From Fig. 4.3 we can write:

$$V_{in} = R_1 I_x + R_3 I_x^3 \quad (4.1)$$

In the presence of a single-tone input current,  $V_{in}$  can be expressed as:

$$V_{in}(t) = V_{in}^{(1)} \sin(\omega t + \phi_1) + V_{in}^{(3)} \sin(3\omega t + \phi_3) \quad (4.2)$$

Where  $\phi_1$  and  $\phi_3$  are the phases of the generated fundamental and 3<sup>rd</sup>-order harmonic, respectively, which is added here to distinguish with the fundamental tone's phase. To simplify the model, the phase's frequency behavior is not discussed in this chapter. The current  $I_x$  is expressed as:

$$I_x(t) = I_{in}(t) - C_1 \frac{dV_{in}}{dt} = I_{in}^{(1)} \sin \omega t - \omega C_1 V_{in}^{(1)} \cos \omega t - 3\omega C_1 V_{in}^{(3)} \cos(3\omega t + \phi_3) \quad (4.3)$$

By substituting (4.3) in (4.1), the expression for  $V_{in}$  will include both fundamental and 3<sup>rd</sup>-order harmonic terms. Together with (4.2), the expression of the fundamental tone is:

$$V_{in}^{(1)} e^{j\phi_1} \approx R_1 \left[ I_{in}^{(1)} - j\omega C_1 V_{in}^{(1)} e^{j\phi_1} \right] \quad (4.4)$$

The above equation is an approximation with ignoring the small value terms such as the term contains  $R_3 I_{in}^{(1)3}$ , because the  $I_{in}^{(1)}$  applied to the circuits is typically several milliamperes so that  $R_3 I_{in}^{(1)3} \ll R_1 I_{in}$ . The same way of approximation is applied to the analysis throughout this chapter. Solving (4.4), the fundamental tone's magnitude of the input node voltage is:

$$\left| V_{in}^{(1)} e^{j\phi_1} \right| = \left| \frac{R_1 I_{in}^{(1)}}{1 + j\omega R_1 C_1} \right| = R_1 I_{in}^{(1)} |H(\omega)| \quad (4.5)$$

where:

$$H(\omega) = \frac{1}{1 + j\omega R_1 C_1} \quad (4.6)$$

The transfer function  $H(\omega)$  includes all poles and zeros in the network with the unity magnitude at DC. With this way of expression, the harmonic voltages' frequency response expression can be simplified. Moreover, the chapter interested in the magnitude, and the model of the phases' frequency response is not discussed.

The equation for the  $3^{rd}$ -order harmonic is as below:

$$V_{in}^{(3)} e^{j\phi_3} = -3j\omega R_1 C_1 V_{in}^{(3)} e^{j\phi_3} - \frac{R_3 I_{in}^{(1)3}}{4(1 + j\omega R_1 C_1)^3} \quad (4.7)$$

The equation above shows the  $3^{rd}$ -order tone of the input node voltage is given by:

$$\left| V_{in}^{(3)} e^{j\phi_3} \right| = \left| \frac{R_3 I_{in}^{(1)3}}{4(1 + 3j\omega R_1 C_1)(1 + j\omega R_1 C_1)^3} \right| = \frac{1}{4} R_3 I_{in}^{(1)3} |H(\omega)| \cdot |H(3\omega)| \quad (4.8)$$

The model is verified by applying a sinusoidal current with 1mA amplitude in a simulation of the parallel RC network with only R to be the nonlinear component. The results in Fig. 4.4 show that the frequency response of the  $3^{rd}$ -order nonlinearity is the same as that predicted by (4.8).

Next, we consider the nonlinear capacitor's influence ( $C_3 \neq 0$ ). In this model, we assume that the resistor will be linear, i.e., set  $R_3 = 0$ . As before,  $I_{in}(t) = I_{in}^{(1)} \sin \omega t$  is applied to the RC network. The current conducted by this nonlinear capacitor can be expressed as:

$$I_C(t) = \frac{d}{dt} [C_1 V_{in}(t) + C_3 V_{in}^3(t)] \quad (4.9)$$

The resistor is linear, so the input node voltage can be expressed as:

$$V_{in} = R_1 \cdot I_x \quad (4.10)$$

As before, we express  $V_{in}$  as:

$$V_{in}(t) = V_{in}^{(1)} \sin(\omega t + \phi_1) + V_{in}^{(3)} \sin(3\omega t + \phi_3) \quad (4.11)$$

The current  $I_x$  conducted by the resistor is given by:

$$I_x(t) = I_{in}(t) - I_C(t) = I_{in}^{(1)} \sin \omega t - \omega C_1 V_{in}^{(1)} \cos(\omega t + \phi_1) - 3\omega C_1 V_{in}^{(3)} \cos(3\omega t + \phi_3) \\ - 3\omega C_3 V_{in}^2(t) \left[ V_{in}^{(1)} \cos(\omega t + \phi_1) + 3V_{in}^{(3)} \cos 3(\omega t + \phi_3) \right] \quad (4.12)$$

By substituting (4.12) into (4.10), the expression of the  $V_{in}$  will include both fundamental and 3<sup>rd</sup>-order harmonic as predicted. With the assumption that  $C_3 V_{in}^{(1)3} \ll C_1 V_{in}^{(1)}$ , the equation for the fundamental tone voltage at input node is:

$$V_{in}^{(1)} e^{\phi_1} \approx R_1 \left[ I_{in}^{(1)} - j\omega C_1 V_{in}^{(1)} e^{\phi_1} \right] \quad (4.13)$$

Solving the equation above, the fundamental tone of the input node voltage's magnitude is:

$$\left| V_{in}^{(1)} e^{\phi_1} \right| = \left| \frac{R_1 I_{in}^{(1)}}{1 + j\omega R_1 C_1} \right| = R_1 I_{in}^{(1)} |H(\omega)| \quad (4.14)$$

The equation for the 3<sup>rd</sup>-order harmonic is given by:

$$V_{in}^{(3)} e^{\phi_3} \approx -3j\omega R_1 C_1 V_{in}^{(3)} e^{\phi_3} - \frac{3}{4} j\omega R_1 C_3 V_{in}^{(1)3} e^{3\phi_1} \quad (4.15)$$

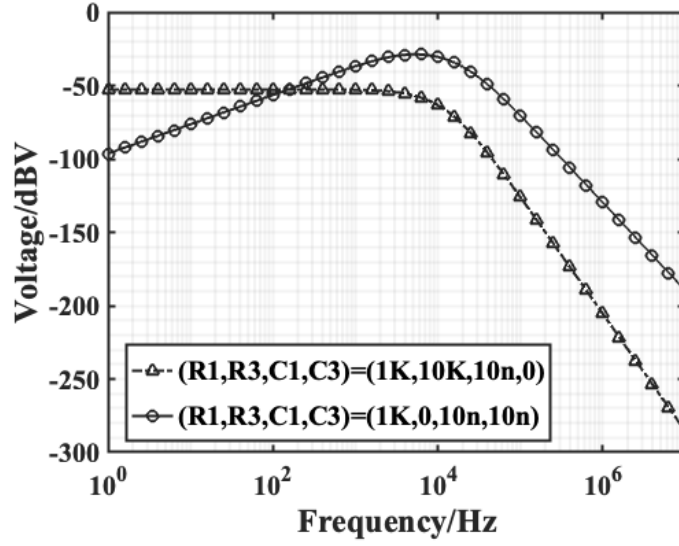


Figure 4.4:  $3^{rd}$ -order harmonic frequency response verification of RC network with only R or C nonlinear.

By solving the equation above, the  $3^{rd}$ -order tone of the input node voltage's magnitude is:

$$\left| V_{in}^{(3)} e^{j\phi_3} \right| = \left| \frac{3\omega R_1^4 C_3 I_{in}^{(1)3}}{4(1 + 3j\omega R_1 C_1)(1 + j\omega R_1 C_1)^3} \right| = \frac{3}{4} \omega R_1^4 C_3 I_{in}^{(1)3} |H(3\omega)| \cdot |H^3(\omega)| \quad (4.16)$$

The model is verified by applying a sinusoidal current with 1mA amplitude in a simulation of the parallel RC network with only C to be the nonlinear component. The results in Fig. 4.4 show that the frequency response of the  $3^{rd}$ -order nonlinearity is the same as that predicted by (4.16) predicted. Moreover, the above model for both nonlinear R and C can be extended to  $n^{th}$  order.

This chapter focuses on modeling the magnitude of the voltage, so the phase expression is ignored. For the expressions in the following sections, the phase terms will be ignored, and the modeling results and the simulation results are all the magnitudes.

The above model shows the frequency response of the RC network when only one of R or C is nonlinear. When the nonlinearities of both elements are taken into account, their

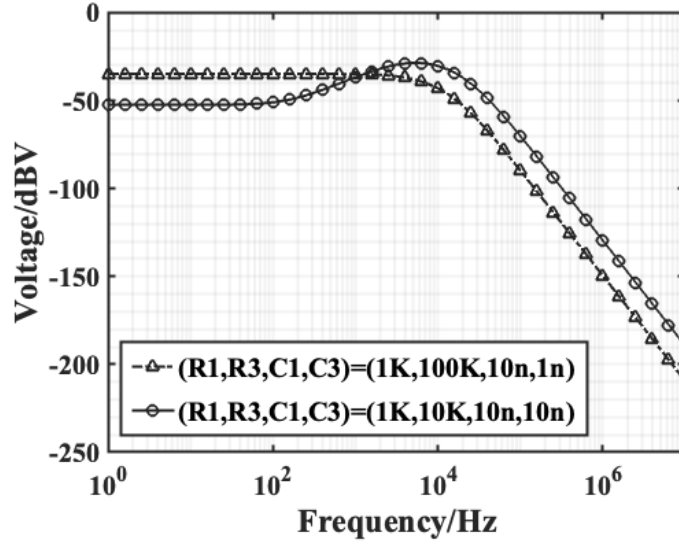


Figure 4.5:  $3^{rd}$ -order harmonic Frequency response verification of RC network with both R and C are nonlinear.

overall effect is the superposition of each of the individual effects. When the 1-mA single-tone current is applied to this nonlinear RC network, the frequency response curves for two different sets of coefficients – nonlinear-R dominant and nonlinear-C dominant – are shown in Fig. 4.5.

We now consider the effect of the nonlinearity associated with the transconductance of a differential pair transistors. The following analysis shows how this square-law relationship will introduce the nonlinearity. The nonlinear channel length modulation, which gives rise to the finite  $r_o$  that appears at the amplifier load, will be considered separately from the previous derivation for the nonlinear RC circuit. Fig. 4.6 shows a differential amplifier with an active load, which is used as the first stage of the TIA system. When applying an differential input  $V_{in(dm)}(t) = \frac{1}{2}V_i^{(1)} \sin \omega t$  to the differential pair, a second harmonic will appear at node P, whose amplitude is expressed according to [57]:

$$V_P^{(2)} = \frac{V_i^{(1)2}}{16(V_{GS} - V_{th})} \quad (4.17)$$

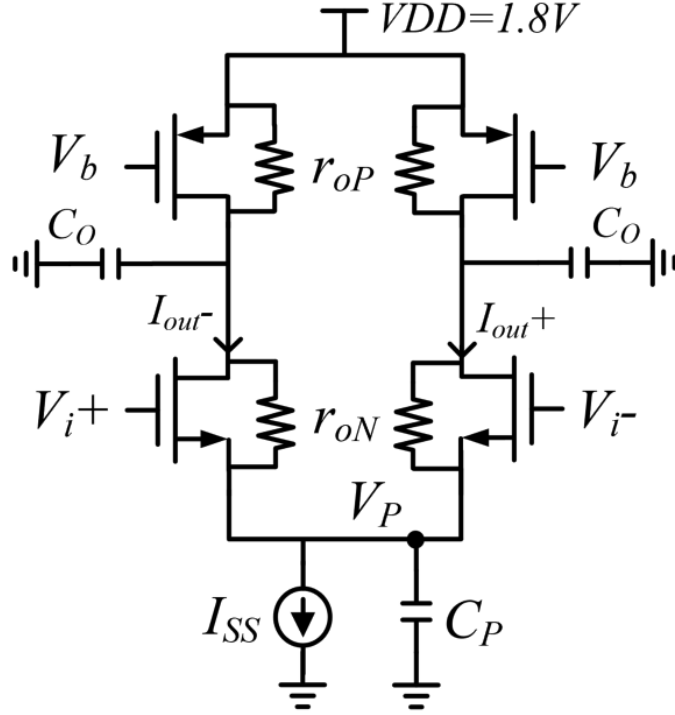


Figure 4.6: Circuits of TIA's first-stage amplifier

This  $2^{nd}$ -order harmonic voltage will interact with the input differential signal to produce a  $3^{rd}$ -order harmonic current at the output:

$$I_{out}^{(3)} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_i^{(1)} V_P^{(2)} \quad (4.18)$$

The analysis above is helpful to find the accurate frequency response of the distortion at high frequency. First of all, the input voltage will introduce a  $2^{nd}$ -order harmonic at the common node P. This common node  $2^{nd}$ -order harmonic voltage will be filtered by the capacitance at this node, then interact with the fundamental tone at the input to produce the  $3^{rd}$ -order harmonic current at the output. The driving point impedance at node P is:

$$Z_P(\omega) = \frac{1}{2} \cdot \frac{r_{oP} + r_{oN}}{1 + g_m r_{oN}} \cdot H_P(\omega) \quad (4.19)$$

where:

$$H_P(\omega) = \frac{(1 + j\frac{\omega}{\omega_{z1}})}{(1 + j\frac{\omega}{\omega_{p1}})(1 + j\frac{\omega}{\omega_{p2}})}; \quad (4.20)$$

$$\omega_{p1} = \frac{1}{r_{oP}C_O}; \omega_{p2} = \frac{1}{\frac{r_{oP}+r_{oN}}{1+g_m r_{oN}}C_P}; \omega_{z1} = \frac{1}{(r_{oN}||r_{oP})C_O}$$

For the first-stage amplifier studied in this work shown in Fig. 4.6, due to the relatively large value of  $C_O$  at the outputs,  $\omega_{p1}$  and  $\omega_{z1}$  are at much lower frequencies than  $\omega_{p2}$ .

In order to model the complete frequency response of the first-stage amplifier, the poles and zeros at the input and output of this amplifier should be included in the model. The first stage of the TIA in Fig. 4.6 can be modeled as a cascaded system as shown in Fig. 4.8, and the input current is converted to voltage by multiplying BY the input resistance  $R$ , then the system can be analyzed all in voltage for simplicity. The poles and zeros originating from the input and output resistances interacting with the device parasitic capacitors are modeled as transfer function  $H_i(\omega)$  and  $H_o(\omega)$ . With this model, the differential input signal of this amplifier can be expressed as  $V_{i(dm)}(\omega) = \frac{1}{2}V_i^{(1)}H_i(\omega)$ . Then the frequency response of the  $2^{nd}$ -order harmonic at the common node P will also be filtered by  $H_P(2\omega)$ , and the output  $3^{rd}$ -order harmonic current can be rewritten according to (4.17) and (4.18) as:

$$V_P^{(2)}(\omega) = V_P^{(2)}(0)H_i^2(\omega)H_P(2\omega) \quad (4.21)$$

$$I_{out}^{(3)}(\omega) = I_{out}^{(3)}(0)H_i^3(\omega)H_P(2\omega) \quad (4.22)$$

The  $V_P^{(2)}(0)$  and  $I_{out}^{(3)}(0)$  are the amplitudes expressed in (4.17) and (4.18), respectively. The simulation result of the  $2^{nd}$ -order harmonic that appears at the common node P is shown in Fig. 4.7. Its frequency behavior matches that predicted by (4.21). The  $3^{rd}$ -order harmonic of the output voltage due to  $I_{out}^{(3)}(\omega)$  will also need to be multiplied by the  $H_o(3\omega)$  at the



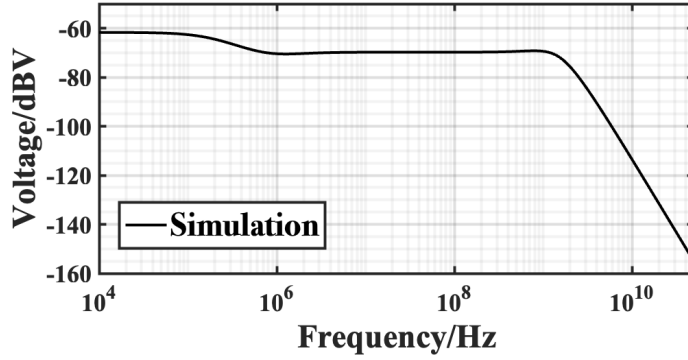


Figure 4.7: Frequency response at node P of the first-stage amplifier.

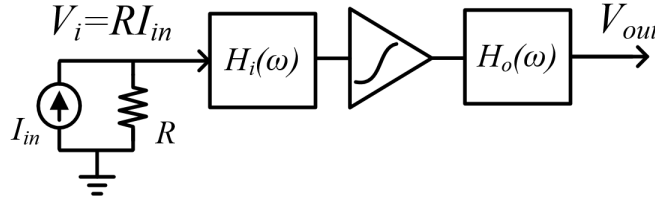


Figure 4.8: Frequency response model of the Fig. 4.6 single-stage transimpedance amplifier

output, which is expressed as:

$$V_{out,act}^{(3)}(\omega) = I_{out}^{(3)}(\omega)r_{out}H_o(3\omega) = I_{out}^{(3)}(0)(r_{oP}||r_{oN})H_i^3(\omega) H_P(2\omega)H_o(3\omega) \quad (4.23)$$

Here  $r_{out} = r_{oP}||r_{oN}$  is the load resistance.

The above models of both passive and active devices have been used to analyze the frequency response due to the major nonlinearities in the circuit. In real circuits, as modeled in the prior works [52, 58–60], the sources of the nonlinearities can be more complex, and it is not practical to find each source’s nonlinear coefficient and include them separately into the overall model. We now consider two dominant nonlinearity sources, one from the nonlinear output drain conductance  $g_{ds}$ , and the other from the square-law distortion introduced by the differential pair.

The nonlinear harmonics originated by the nonlinear conductance  $g_{ds}$  with the capacitor  $C_O$  at both outputs of the differential amplifier shown in Fig. 4.6, can be modeled as an RC network shown in Fig. 4.3, where the capacitor is linear and the resistor is nonlinear with coefficients  $R_1 = a_{gd,1}$  and  $R_3 = a_{gd,3}$ . The differential output fundamental tone current  $I_{out}^{(1)}(\omega)$  and the output voltage  $V_{o,gd}(\omega)$  are used here to replace the  $I_{in}^{(1)}$  and  $V_{in}$  in Fig. 4.3. The  $I_{out}^{(1)}(\omega)$  and the generated 3<sup>rd</sup>-order harmonic voltage  $V_{o,gd}^{(3)}$  can be expressed according to (4.8) as:

$$I_{out}^{(1)}(\omega) = V_i^{(1)} g_m H_i(\omega) \quad (4.24)$$

$$V_{o,gd}^{(3)}(\omega) = \frac{1}{4} a_{gd,3} \left[ I_{out}^{(1)}(\omega) \right]^3 H_o^3(\omega) H_o(3\omega) \quad (4.25)$$

where the  $g_m$  is the transconductance of the differential pair in Fig.4.6. Together with the nonlinearity generated by the square-law distortion, which is expressed in (4.23), the overall 3<sup>rd</sup> harmonic of the output voltage  $V_{out}^{(3)}$  is expressed as:

$$\begin{aligned} V_{out}^{(3)} &= V_{out,act}^{(3)}(\omega) + V_{o,gd}^{(3)}(\omega) \\ &= I_{out}^{(3)}(0)(r_{oP}||r_{oN})H_i^3(\omega) H_P(2\omega)H_o(3\omega) + \frac{1}{4}a_{gd,3} \left[ I_{out}^{(1)}(\omega) \right]^3 H_o^3(\omega) H_o(3\omega) \end{aligned} \quad (4.26)$$

Comparing the first and second term on the right side in (4.26), the filtering behavior due to the output transfer function  $H_o(\omega)$  is different. It is necessary to separate those two nonlinearities into two different categories. We distinguish two components of any  $n^{th}$ -order nonlinearity: that only includes a factor of  $H_o(\omega)$  with a power of one is known as the  $n^{th}$ -order input related nonlinearity (IRN); the component that includes  $H_o(\omega)$  with a power of  $n$  is known as the  $n^{th}$ -order output related nonlinearity (ORN). Based on those definitions, we now use  $a_{3i}$  and  $a_{3o}$  to represent the  $n^{th}$ -order IRN and ORN nonlinearity coefficients, respectively, while the linear voltage gain is denoted as  $a_1$ . With these new parameters

defined, we can rewrite the  $3^{rd}$ -order nonlinearity modeled in (4.26) as follows:

$$V_{out}^{(3)}(\omega) = \frac{1}{4}a_{3i} [V_i H_i(\omega)]^3 H_p(2\omega) H_o(3\omega) + \frac{1}{4}a_{3o} [V_i a_1 H_i(\omega) H_o(\omega)]^3 H_o(3\omega) \quad (4.27)$$

The first term on the right side of the equation (4.27) represents the IRN, and according to (4.17), (4.18) and (4.23), the coefficient  $a_{3i}$  can be expressed as:

$$a_{3i} = \frac{\mu_n C_{ox} \frac{W}{L} r_{out}}{8 (V_{GS} - V_{th})} \quad (4.28)$$

The second term on right side of the equation (4.27) represents the ORN, and the linear voltage gain is expressed as:

$$a_1 = g_m r_{out} \quad (4.29)$$

According to (4.25) and (4.29), the  $a_{3o}$  is expressed as:

$$a_{3o} = \frac{a_{gd,3}}{r_{out}^3} \quad (4.30)$$

With the definition of IRN and ORN, for the high-gain amplifier with the dominant pole at the output, a predicted  $3^{rd}$ -order harmonic voltage frequency response according to (4.26) is shown in Fig. 4.9. The solid line is the overall distortion voltage appear at the output, and the dashed line is the interpolation of the IRN and ORN distortion voltages, respectively. The ORN will be dominant at low frequencies but will exhibit a steep rolloff of 80 dB/dec at frequencies higher than  $f_0$ , while the IRN will maintain a rolloff of 20dB/dec. As a result, after a certain frequency, the IRN starts to dominate the overall nonlinearity. At the second pole  $f_1$ , the IRN will exhibit a rolloff of 80 dB/dec.

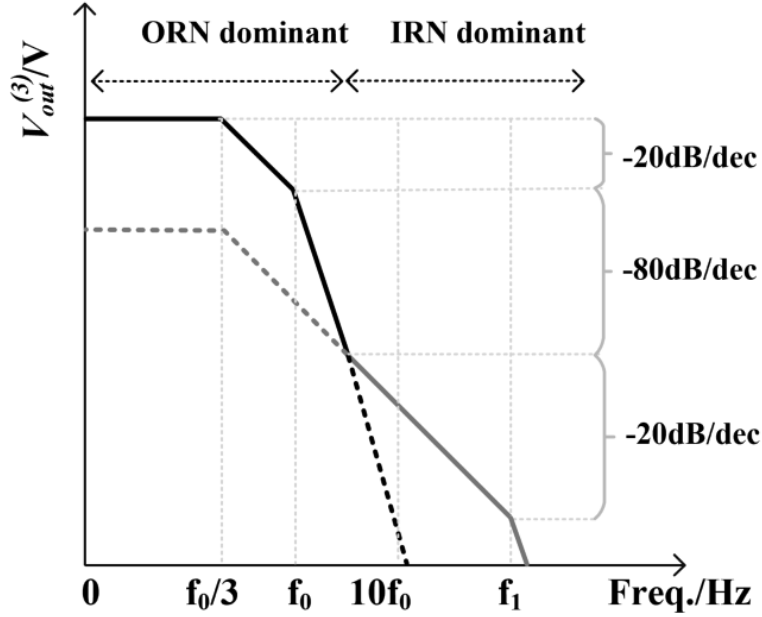


Figure 4.9: Explanation of the frequency response of the 3<sup>rd</sup>-order nonlinearity when dominant pole is at the output node of the single-stage amplifier.

For the two-stage amplifier, since a large compensation capacitor is used, the dominant pole is determined by the output of the first-stage amplifier. As a result, it is necessary to distinguish the IRN and ORN for the first-stage amplifier when modeling the nonlinearity's frequency behavior. On the other hand, for the second-stage amplifier, the dominant pole is determined by the input, and both IRN and ORN will drop with the same slope after this pole frequency. For the latter case, the ORN will dominant over the frequency range until the second pole. As a result, it can be modeled using the conventional method with only one distortion coefficient for each order of harmonic.

Due to the complexity of the different sources and their interactions, directly calculating the IRN and ORN from the device model parameters will be very complex. In the following section, a practical way to find the nonlinear coefficients of IRN and ORN will be introduced.

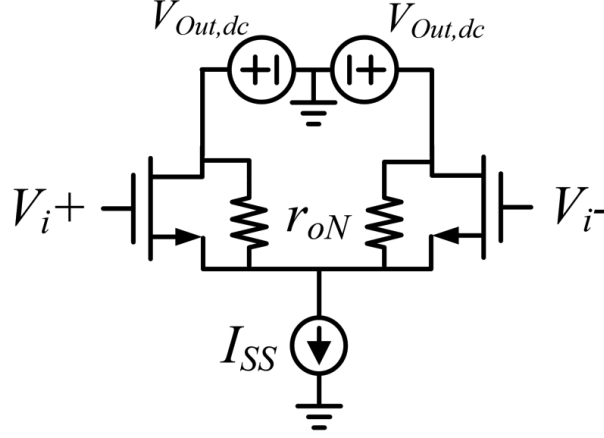


Figure 4.10: circuits setup for finding the IRN coefficients  $a_{ni}$ .

#### 4.2.2 General Model for $N^{th}$ -Order Nonlinearity of a Single-Stage Open-Loop Amplifier

The model that distinguishes the IRN and ORN can be extended to  $n^{th}$ -order nonlinearity of the single-stage amplifiers with the dominant pole at the output. For the amplifier's non-linear coefficients, we use  $a_{ni}$  and  $a_{no}$  to represent the  $n^{th}$ -order IRN and ORN nonlinearity coefficients, respectively. With these new parameters defined, we can generalize the  $n^{th}$ -order nonlinearity modeled in (4.27) as follows:

$$V_{out}^{(n)}(\omega) = \frac{1}{2^{n-1}} a_{ni} [V_i H_i(\omega)]^n H_p(2\omega) H_o(n\omega) + \frac{1}{2^{n-1}} a_{no} [V_i a_1 H_i(\omega) H_o(\omega)]^n H_o(n\omega) \quad (4.31)$$

We now describe a practical method to find the  $n^{th}$ -order IRN and ORN's coefficients.

Step1: With the first-stage TIA shown in Fig. 4.6, perform a DC voltage sweep at the input of the amplifier and obtain the output voltage curves versus input. By performing a numerical regression on this curve, the  $n^{th}$ -order coefficient can be expressed in terms of the

IRN and ORN as [45].

$$a_n = a_{ni} + a_{no}a_1^n \quad (4.32)$$

Step2: Perform a DC simulation to find the outputs DC voltage, then replace the PMOS with the ideal voltage source as shown in Fig.4.10. Because the output now is shorted to ac ground at the output nodes, so those harmonic currents are originated from the IRN only. Similar to Step 1, a numerical regression can be performed on the DC characteristic of  $I_{out}r_{out}$  vs.  $V_i$ , where  $r_{out} = r_{oP}||r_{oN}$  is the load resistance. In this way, the IRN's coefficients  $a_{ni}$  can be directly found from the regression. Together with (4.32), the ORN coefficients  $a_{no}$  can also be found.

The simulator's resolution is also critical for accurately find the amplifier's nonlinearity coefficients. The resolution of the voltage is set to be 1fV for all simulations which provides sufficient precision for determining nonlinearities up to 9<sup>th</sup>-order.

With the above steps, the odd-order nonlinearity coefficients for both IRN and ORN of the first stage TIA in Fig. 4.6 have been found and listed in Table 4.1. Fig. 4.11 shows the comparison of the 3<sup>rd</sup>-order nonlinearity predicted by the model and the simulation results from 10kHz to 10GHz with 30 $\mu$ A input current amplitude. When this model is applied to a 5<sup>th</sup>-order nonlinearity, as shown in Fig. 4.12(a), larger discrepancies can be observed, which can be attributed to the more pronounced contribution of the capacitor nonlinearities. Fig. 4.12(b) shows all the odd-order nonlinearities simulation results up to 9<sup>th</sup> order. The results show the nonlinear harmonics are likely influenced more by the nonlinear capacitors for higher-order harmonics. More accurate model can be built considering the nonlinear capacitor's effects. In this work, we use the model with only nonlinear resistance effect considered for simplicity.

Table 4.1: FIRST STAGE AMP. ODD-ORDER HARMONIC COEFFICIENTS

Harmonic Order	$a_{ni,1}$	$a_{no,1}a_{1,1}^n$
1(linear gain)	23.75	0
3	-216	-816
5	-85	$-8.1 \times 10^4$
7	$-1.4 \times 10^4$	$-8.6 \times 10^6$
9	$-4.5 \times 10^5$	$-9.0 \times 10^7$

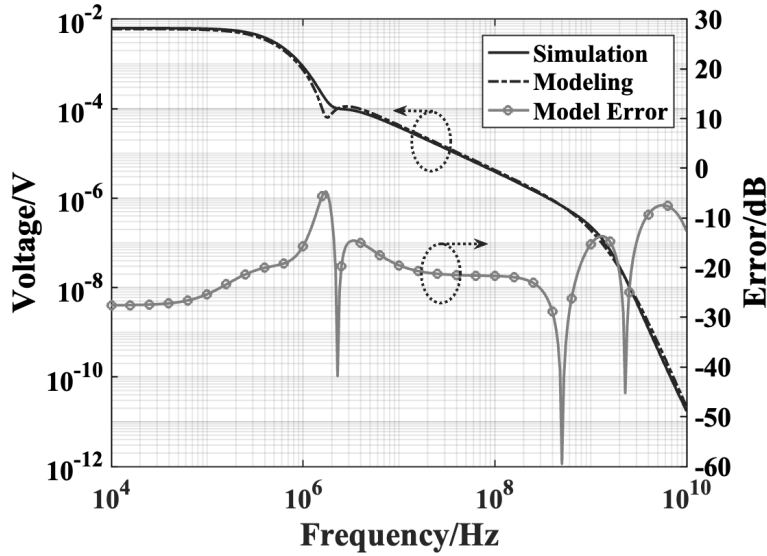


Figure 4.11: 3<sup>rd</sup>-order nonlinearity simulation and model results comparison.

### 4.2.3 Modeling the Nonlinearity of Open-Loop Two-Stage TIA

The open-loop two-stage TIA topology is shown in Fig. 4.13, with the key design parameters shown in Table 4.2. The system is simplified, as shown in Fig. 4.14(a), using the single-end topology with breaking the feedback loop according to the feedback theory. Similar to the previous modeling methods, we model this open-loop two-stage amplifier as shown in Fig. 4.14(b). The model includes the transfer functions corresponding to the input, middle, and output nodes denoted by  $H_i(\omega)$ ,  $H_m(\omega)$  and  $H_o(\omega)$ , respectively. And the nonlinearity coefficients are all included into the amplifiers as  $a_{ni,1}$  and  $a_{oi,1}$  as the IRN and ORN for the first-stage amplifier, and  $a_{n,2}$  for the second-stage amplifier.

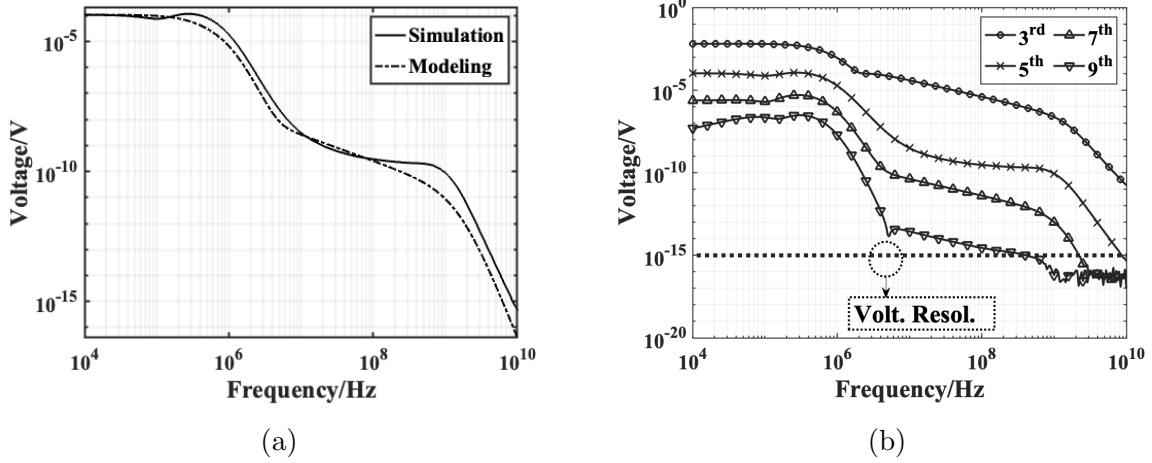


Figure 4.12: (a) 5<sup>th</sup>-order nonlinearity simulation and model results comparison. (b) Simulation results of first-stage amplifier's 3<sup>th</sup>-, 5<sup>th</sup>-, 7<sup>th</sup>-, 9<sup>th</sup>-order nonlinearities over frequency.

In order to accurately model the frequency behavior of this two-stage amplifier, it is important to find the transfer function expressions for each node. For the input node, there is only one pole due to the input RC, which is expressed as:

$$H_i(\omega) = \frac{1}{1 + j\omega(R_{IN} || R_F)C_{IN}} \quad (4.33)$$

To study the transfer function of  $H_m(\omega)$  and  $H_o(\omega)$ , we use the circuits model shown in Fig. 4.14(a). Since the compensation capacitor is much larger than the parasitic capacitance at the input and output of the second stage amplifier, we will ignore all other capacitors  $C_{o1}$  and  $C_{OUT}$  for simplicity. Typically, it is important to know the poles and zeros at the output node. However, when study the nonlinearity's frequency response, poles and zeros at the output of the first stage ( $V_1$  node on the Fig. 4.14(a)) is also important. Having input current  $I_{in} = 0$  and applying a test current  $I_x$  at  $V_1$  node, we get the transfer functions



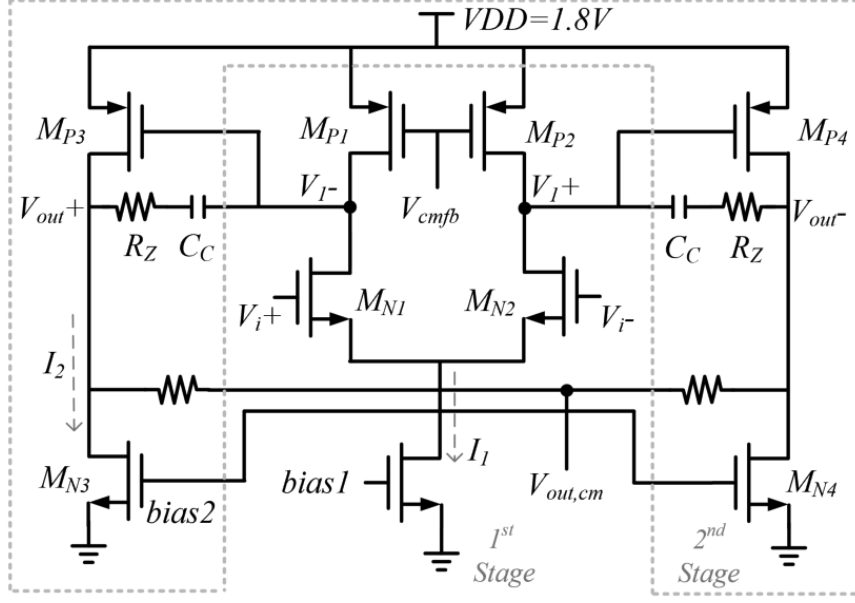


Figure 4.13: Circuits of TIA's two-stage amplifier.

$H_m(\omega)$  and  $H_o(\omega)$  expressed as:

$$H_m(\omega) = \frac{1 + j\omega C_c(R_L + R_z)}{1 + j\omega C_c [R_L + R_z + (1 + g_{m2}R_L)R_{IN}]} \quad (4.34)$$

$$H_o(\omega) = \frac{1 + j\omega C_c(R_z - g_{m2}^{-1})}{1 + j\omega C_c(R_L + R_z)} \quad (4.35)$$

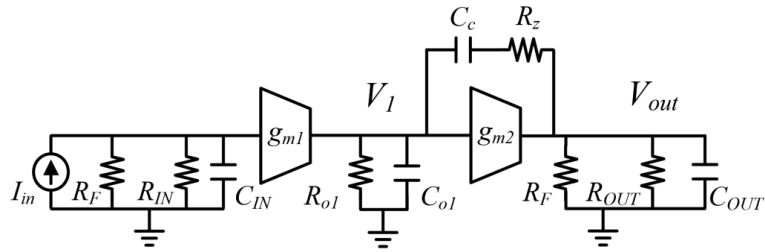
where  $R_L = R_F || R_{OUT}$ . The comparison of the calculated results of the poles/zeros and the poles/zeros found by the simulator at  $V_1$  node and output node of the circuits, are listed in Table. 4.3.

With the coefficients and the transfer function defined in Fig. 4.14(b), the  $n^{th}$ -order non-linearity originated from the first-stage amplifier can be expressed according to (4.31) as:

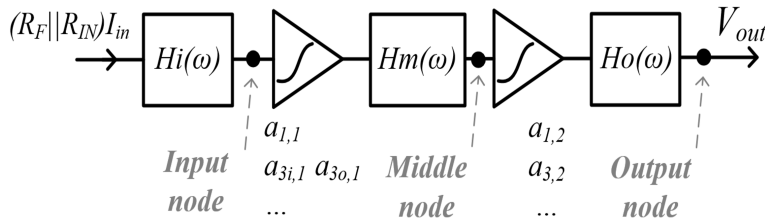
$$V_1^{(n)}(\omega) = \frac{1}{2^{n-1}} \{ a_{ni,1} [V_i H_i(\omega)]^n H_p(2\omega) H_m(n\omega) + a_{no,1} [V_i a_{1,1} H_i(\omega) H_m(\omega)]^n H_m(n\omega) \} \quad (4.36)$$

Table 4.2: DESIGN PARAMETERS OF TIA

Parameter	Value	Parameter	Value
$I_1$ (mA)	1	$r_{o,P3}$ (k $\Omega$ )	2.5
$I_2$ (mA)	2	$R_Z$ ( $\Omega$ )	160
$g_{m,N1}$ (mS)	6.17	$R_F$ (k $\Omega$ )	1.2
$g_{m,P3}$ (mS)	15	$R_L$ (k $\Omega$ )	0.8
$r_{o,N1}$ (k $\Omega$ )	5.8	$R_{IN}$ (k $\Omega$ )	5
$r_{o,P1}$ (k $\Omega$ )	12.1	$C_{g,N1}$ (fF)	98
$r_{o,N3}$ (k $\Omega$ )	3.9	$C_c$ (pF)	6



(a)



(b)

Figure 4.14: Comparison of the simulation and model results of (a) Closed-loop 3<sup>rd</sup>-order harmonic distortion voltage, (b) 5<sup>th</sup>-order harmonic distortion voltage.

Table 4.3: COMPARISON OF P/Z AT EACH NODE

Nodes	$p/z$	Cal. Value	Sim. Value
Input	$p_{in}$	-1.64GHz	-1.53GHz
Middle	$p_m$	-972KHz	-918KHz
	$z_m$	-47.4MHz	-52MHz
Output	$p_{o1}$	-47.4MHz	-52MHz
	$p_{o2}$	N/A	-5.04GHz
	$z_o$	-284MHz	-255MHz

For the second stage amplifier, its  $n^{th}$ -order nonlinearity coefficients can be found using the conventional methods, and their values are listed in Table. 4.4. In addition, there is a compensation loop formed by the  $C_c$  and  $R_z$  in the second-stage amplifier. This compensation loop's influence on the poles and zeros has already been included in the transfer functions. However, the generated nonlinear harmonics at the output will also feed back through the loop that includes  $C_c$  and  $R_z$ , and the following analysis gives the closed-loop expression of the  $n^{th}$ -order harmonics at the second stage.

Table 4.4: SECOND STAGE AMP. ODD-ORDER HARMONIC COEFFICIENTS

Harmonic Order	1	3	5	7	9
$a_{n,2}$	6.0	-25.2	-168.7	-950.0	$-2.08 \times 10^4$

Fig. 4.15 is the model of the second-stage amplifier with the compensation loop. The model only includes the  $3^{rd}$ -order nonlinearity for simplicity. With the input current provided from the first stage, the amplifier will generate  $3^{rd}$  harmonic voltage  $V_{out,open}^{(3)}(\omega)$  at the output. Then it will feedback to the input node as  $V_{1,fb}^{(3)}(\omega)$ , which is expressed as:

$$V_{1,fb}^{(3)}(\omega) = V_{out,open}^{(3)}(\omega) \frac{\frac{1}{\frac{1}{R_{o1}} + j\omega C_{o1}}}{R_z + \frac{1}{j\omega C_c} + \frac{1}{\frac{1}{R_{o1}} + j\omega C_{o1}}} \quad (4.37)$$

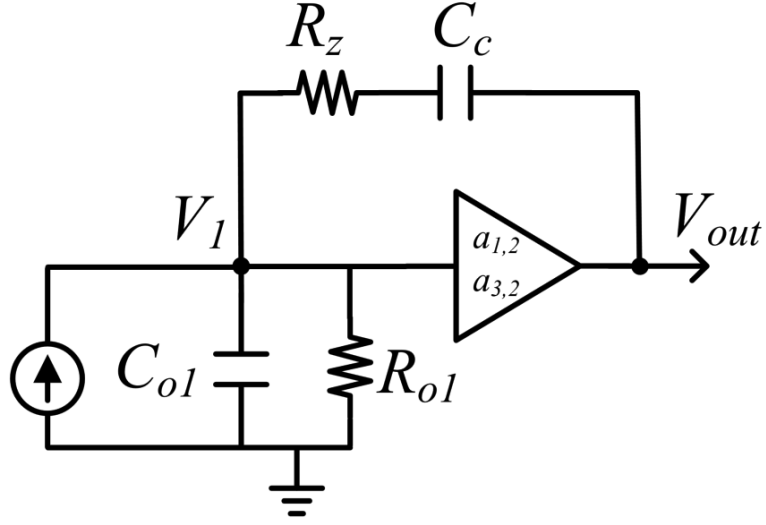


Figure 4.15: the closed-loop circuits model of the second-stage amplifier.

Considering the compensation feedback loop, the closed-loop 3<sup>rd</sup>-order harmonic  $V_{out}^{(3)}$  is:

$$V_{out,open}^{(3)}(\omega) - a_{1,2}V_{1,fb}^{(3)}(\omega) = V_{out}^{(3)}(\omega) \quad (4.38)$$

$$\begin{aligned} V_{out}^{(3)}(\omega) &= V_{out,open}^{(3)}(\omega) \cdot H_{a2}(\omega) \\ &= \frac{V_{out,open}^{(3)} [R_z R_{o1} C_c C_{o1} s^2 + (R_{o1} C_{o1} + R_z C_c + R_{o1} C_c) s + 1]}{R_z R_{o1} C_c C_{o1} s^2 + [R_{o1} C_{o1} + R_z C_c + (1 + a_{1,2}) R_{o1} C_c] s + 1} \end{aligned} \quad (4.39)$$

Ignore the high-frequency second pole, the expression shows that compared with the open-loop distortion voltage, the closed-loop distortion voltage originated from the second-stage amplifier contains an additional pole and a zero at:

$$p_a = \frac{1}{R_s C_{o1} + R_z C_c + (1 + a_{1,2}) R_{o1} C_c} \quad (4.40)$$

$$z_a = \frac{1}{R_{o1} C_{o1} + R_z C_c + R_{o1} C_c} \quad (4.41)$$

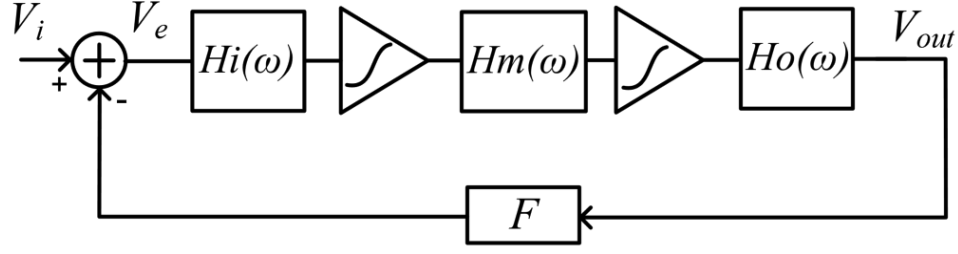


Figure 4.16: frequency response model of a closed-loop feedback system of the TIA. The input voltage amplitude  $V_i = I_{in}(R_{IN}||R_F)$ .

The introduced pole value is the same as the dominant pole. However, the introduced zero (-5MHz) is different from the zero at middle node. The additional pole and zero can be included in a transfer function  $H_{a2}(n\omega)$ . With the consideration of the  $H_{a2}(n\omega)$ , the  $n^{th}$ -order harmonic voltage originated from the second-stage amplifier can be expressed as:

$$V_{out,2nd}^{(n)}(\omega) = \frac{1}{2^{n-1}} a_{n,2} [V_1^{(1)}(\omega)]^n H_o(n\omega) H_{a2}(n\omega) \quad (4.42)$$

$$V_1^{(1)}(\omega) = a_{1,1} V_i H_i(\omega) H_m(\omega) \quad (4.43)$$

Here the  $V_i H_i(\omega)$  and  $V_1^{(1)}(\omega)$  represent the input fundamental tone voltages of the first- and second-stage amplifier.

### 4.3 Model of the Closed-Loop Two-Stage TIA

In this section, the model of the closed-loop two-stage TIA's nonlinearity is analyzed. The prior works have discussed the ways to analyze the nonlinearities in the feedback system [61–64]. In this chapter, the nonlinearity of each amplifier stage modeled in Section 4.2 will be directly applied to a closed-loop feedback system.

### 4.3.1 Closed-loop Analysis of the Two-Stage Amplifier (without considering the interaction)

Based on the open-loop system topology shown in Fig. 4.14(b), the closed-loop amplifier presented in Fig. 4.1 can be modeled as the feedback system shown in Fig. 4.16. In order to find the expression of the overall closed-loop nonlinear harmonics at the output, we first need to know the expressions of the overall open-loop nonlinear harmonics at the output, denoted by  $V_{out,open}^{(n)}(\omega)$ . Those nonlinear harmonic voltages can be used for the closed-loop analysis. Each of these nonlinear harmonics is comprised of two parts, one originating from the first-stage amplifier and then amplified by the second-stage's gain  $a_{1,2}$  and the other originating from the second-stage amplifier. Here we ignored the harmonics' interaction. The overall open-loop  $n^{th}$ -order harmonic distortion is given by:

$$V_{out,open}^{(n)}(\omega) = a_{1,2}V_1^{(n)}(\omega)H_o(n\omega) + V_{out,2nd}^{(n)}(\omega) \quad (4.44)$$

The expressions for  $V_1^{(n)}$  and  $V_{out,2nd}^{(n)}$  have already been derived with (4.31) and (4.43), respectively. Notice that the input signal now is the error voltage  $V_e(\omega)$ . So the input voltage in both expressions need to be replaced by  $V_e(\omega)$ . The loop-gain  $LG(\omega)$ , the feedback factor  $F(\omega)$ , and  $V_e(\omega)$  can be expressed as:

$$LG(\omega) = a_{1,1}a_{1,2}F(\omega)H_i(\omega)H_m(\omega)H_o(\omega) \quad (4.45)$$

$$F(\omega) = \frac{R_{IN} \parallel \frac{1}{j\omega C_{IN}}}{R_{IN} \parallel \frac{1}{j\omega C_{IN}} + R_F} \quad (4.46)$$

$$V_e(\omega) = V_i - V_e(\omega)LG(\omega) \rightarrow V_e(\omega) = \frac{V_i}{1 + LG(\omega)} \quad (4.47)$$

Noticed that the feedback loop is formed by the  $R_{IN}$  in parallel with the  $C_{IN}$  and the  $R_F$  of the TIA system shown in Fig. 4.1. The term  $V_{out,open}^{(n)}$  can be regard as the overall  $n^{th}$ -order

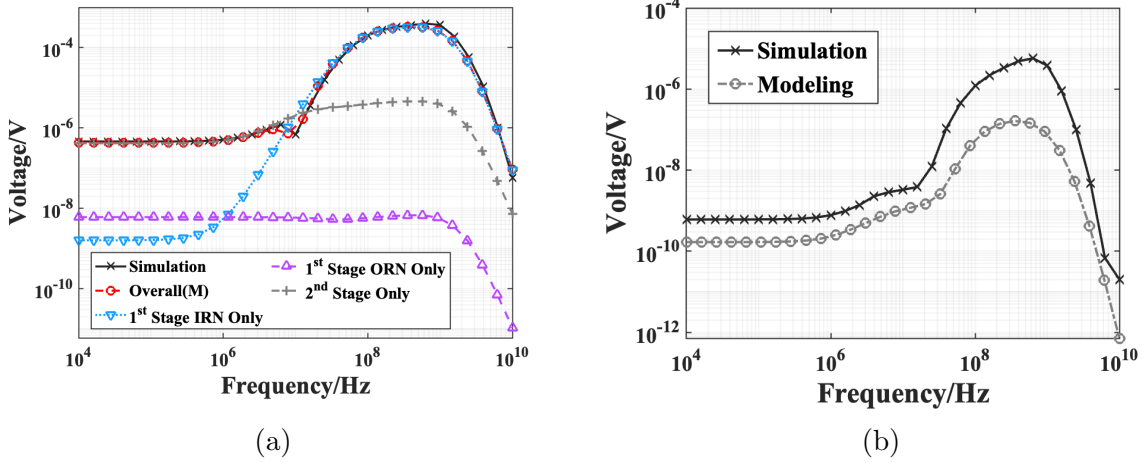


Figure 4.17: Comparison of the simulation and model results of (a) Closed-loop 3<sup>rd</sup>-order harmonic distortion voltage, (b) 5<sup>th</sup>-order harmonic distortion voltage.

harmonic injected at the output (open loop). The close-loop  $n^{\text{th}}$ -order harmonic voltage  $V_{out,ini}^{(n)}(\omega)$  can be derived as below:

$$V_{out,ini}^{(n)}(\omega) = V_{out,open}^{(n)}(\omega) - V_{out,ini}^{(n)}(\omega)LG(n\omega) \quad (4.48)$$

$$V_{out,ini}^{(n)}(\omega) = \frac{V_{out,open}^{(n)}(\omega)}{1 + LG(n\omega)} \quad (4.49)$$

Up to now only the  $n^{\text{th}}$ -order harmonics individually in the feedback loop have been studied without considering any interactions between them. It could explain all the high-frequency behaviors of the 3<sup>rd</sup>-order nonlinearity since it contains no interactions from the lower order distortion (second harmonic is neglected in the differential amplifier). Fig. 4.17(a) shows the comparison of the model results with the simulation of the closed-loop 3<sup>rd</sup>-order harmonic. The results also contain the separated first and second stage introduced 3<sup>rd</sup>-order harmonics. It shows the nonlinearity is dominated by the second stage at low frequencies, and by the first stage at high frequencies. However, the results for the 5<sup>th</sup>-order nonlinearity, as shown in Fig. 4.17(b), no longer matches with the simulation. This difference is primarily due to the interactions between the harmonics. This effect will be modeled in the following sections.

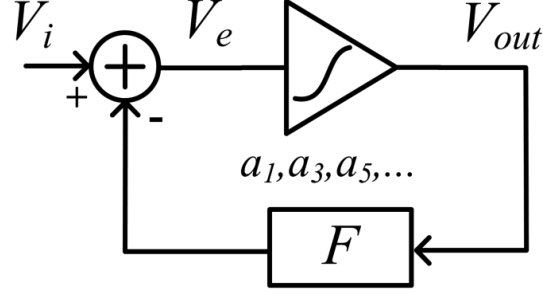


Figure 4.18: Simplified model for analyzing the nonlinear-feedback.

### 4.3.2 Frequency Response of the Interaction in A Feedback System

To model the harmonic interaction, we first consider the simple feedback system shown in Fig. 4.18. Using the same notations in [65], the closed-loop output voltage can be expressed as (even-order nonlinearity is neglected):

$$V_{out} = b_1 V_i + b_3 V_i^3 + b_5 V_i^5 \dots \quad (4.50)$$

The closed-loop coefficients can be expressed in terms of the open-loop coefficients and the feedback factor  $F$ :

$$b_1 = \frac{a_1}{1 + a_1 F} \quad (4.51)$$

$$b_3 = \frac{a_3}{(1 + a_1 F)^4} \quad (4.52)$$

$$b_5 = \frac{a_5 (1 - b_1 F)^3 - 3a_3 b_3 F}{(1 + a_1 F)^3} = \frac{a_5}{(1 + a_1 F)^6} - \frac{3a_3 b_3 F}{(1 + a_1 F)^3} \quad (4.53)$$

It can be observed that no interactions appear in the expressions for  $b_1$  and  $b_3$ . However, the second term of the expression for  $b_5$  includes the interaction related with the  $3^{rd}$  harmonic. After multiplying on both sides of (4.53) by  $(V_{in} \cos \omega t)^5$ , the  $5^{th}$  harmonic voltage is given



by:

$$\underbrace{\frac{1}{16} b_5 (V_i)^5}_{V_{out}^{(5)}} \cos 5\omega t = \underbrace{\frac{1}{16} \frac{a_5}{1 + a_1 F} \left( \frac{V_i}{1 + a_1 F} \right)^5}_{V_{out,ini}^{(5)}} \cos 5\omega t - \frac{3F}{4} \underbrace{\frac{a_3}{1 + a_1 F}}_{a_{3,cls}} \underbrace{\frac{b_3 V_i^3}{4}}_{V_{out}^{(3)}} \underbrace{\left( \frac{V_i}{1 + a_1 F} \right)^2}_{V_e^2} \cos 5\omega t \quad (4.54)$$

The second term of the right-hand side of (4.54) represents the interaction between the  $3^{rd}$ -order harmonic with the fundamental tone. The equation can be rewritten as:

$$V_{out}^{(5)} = V_{out,ini}^{(5)} - \frac{3F}{4} \frac{a_3}{1 + a_1 F} V_{out}^{(3)} V_e^2 \quad (4.55)$$

Firstly, the initial closed-loop  $5^{th}$ -order distortion frequency response  $V_{out,ini}^{(5)}$  has been discussed and expressed in (4.49). The following model can be used to analyze the interaction's frequency response of the  $5^{th}$ -order nonlinearity. We first analyze the frequency response of the general case when applying two tones – the fundamental and the  $3^{rd}$  harmonic – to a nonlinear RC network with only  $3^{rd}$ -order nonlinear resistance, as shown in Fig. 4.19. The input current can be expressed as:

$$I_{in} = I_{in}^{(1)} \sin \omega t + I_{in}^{(3)} \sin 3\omega t \quad (4.56)$$

The voltage will have exhibit harmonics up to the  $9^{th}$  order due to the  $3^{rd}$ -order nonlinear resistance; here we only consider additional  $5^{th}$  nonlinear harmonic together with the  $3^{rd}$ -order harmonic, which is expressed as:

$$V_{in} = V_{in}^{(1)} \sin \omega t + V_{in}^{(3)} \sin 3\omega t + V_{in}^{(5)} \sin 5\omega t \quad (4.57)$$

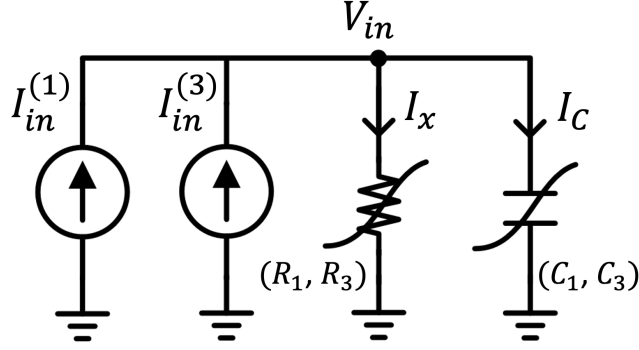


Figure 4.19: Frequency response verification of network with nonlinear R and linear C ( $C_3 = 0$ ).

Using a technique similar to that shown in Section 4.2.1, the expression for the 5<sup>th</sup> harmonic is given by:

$$\left| V_{in}^{(5)}(\omega) \right| = \left| \frac{3}{4} \frac{R_3 \left[ I_{in}^{(1)}(\omega) \right]^2 I_{in}^{(3)}(\omega)}{(1 + j\omega R_1 C_1)^2 (1 + 3j\omega R_1 C_1) (1 + 5j\omega R_1 C_1)} \right| \quad (4.58)$$

This technique for higher-order harmonics can be applied to the differential amplifier shown in Fig. 4.6 as follows. We apply a superposition of a fundamental tone and 3<sup>rd</sup>-harmonic tone currents at the input of the differential pair. The input differential voltage now is rewritten as:

$$V_{i(dm)}(\omega) = \frac{1}{2} V_i^{(1)} \sin \omega t + \frac{1}{2} V_i^{(3)} \sin 3\omega t \quad (4.59)$$

This input interacts with the second harmonic  $\Delta V^{(2)}(\omega)$  that appears at the common node P, which results in a 5<sup>th</sup> harmonic current output:

$$I_{out,act,inter}^{(5)}(\omega) = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_i^{(3)} \Delta V^{(2)}(\omega) H_i^2(\omega) H_i(3\omega) H_P(2\omega) \quad (4.60)$$

The resulting  $5^{th}$  nonlinear harmonic voltage at the output of the first-stage amplifier is given by:

$$V_{out,act,inter}^{(5)}(\omega) = I_{out,act,inter}^{(5)}(\omega)r_{out}H_o(5\omega) \quad (4.61)$$

A similar analysis can be applied to the  $2^{nd}$ -stage amplifier. Similar as (4.42) and (4.43), here we directly give the expression of the interaction's frequency response:

$$V_{out,2nd,inter}^{(5)}(\omega) = \frac{3}{4}a_{3,2} \left[ V_1^{(1)}(\omega) \right]^2 V_1^{(3)}(3\omega)H_{a2}(5\omega)H_o(5\omega) \quad (4.62)$$

where the  $V_1^{(1)}(\omega)$  and  $V_1^{(3)}(3\omega)$  are the feedback fundamental tone and  $3^{rd}$ -order harmonic appear at the input of the second stage amplifier that will interact to produce the  $5^{th}$ -order harmonics.

Equations (4.58) and (4.62) show that for the interactions' frequency response, the nonlinearity originated from RC network still has the different filtering behavior compared with the nonlinearity originated from the amplifier's nonlinear gain. As a results, for the interaction at first-stage amplifier, it is still necessary to distinguish the IRN and ORN, with its corresponding coefficients listed in Table 4.1.

### 4.3.3 Nonlinear-feedback Frequency Response Analysis for Two-Stage TIA's $5^{th}$ -Order Nonlinearity

For the TIA studied in this chapter, the interaction between the lower-order harmonics will appear at both the first and second stages. In particular, the overall interactions are comprised of two parts, one is the interaction between feedback  $3^{rd}$ -order harmonic with the fundamental tone at the first stage and then amplified by the second stage. Another is the

interaction between the amplified fundamental tone and the feedback  $3^{rd}$ -order harmonic at the second stage amplifier. To model those two different interactions in this two-stage amplifier, the method is to separate this two-stage system into two sub-models as shown in Fig. 4.20. In each sub-model one of the amplifiers remains nonlinear while the other is replaced by a linear model. Then the harmonics of each sub-model is determined, and their effects are superimposed.

For the submodell in Fig. 4.20, which considers the first stage as nonlinear and second stage as linear. When one amplifier is considered linear, it will not generate any nonlinear harmonics and only provide the linear gain. Though this submodel totally ignored the nonlinearity generated from the second-stage amplifier, due to the fact the first-stage amplifier's nonlinear harmonic will dominant at the high frequency, so this submodel can still be relatively accurate at high-frequency range.

The feedback of the harmonics to the first-stage amplifier's input is expressed in (4.49). According the previoius section, the interaction part of the  $5^{th}$ -order distortion introduced by submodell can be expressed at low frequencies as:

$$V_{inter,1st}^{(5)} = \frac{3F}{4} \frac{a_{3,1i}a_{1,2} + a_{3,1o}a_{1,2}}{1 + a_{1,1}a_{1,2}F} V_{cls,1st}^{(3)} V_e^2 \quad (4.63)$$

Here the  $V_{cls,1st}^{(3)}$  is the total  $3^{rd}$ -order closed-loop nonlinear harmonic of the submodell, which is the  $3^{rd}$ -order nonlinearity originated from the first-stage amplifier then amplified by the second stage's linear gain. To model the frequency response for the submodell, the following filtering behavior need to be considered when express the frequency response:

1. For the interaction between the  $3^{rd}$ -order harmonic and the fundamental tone, the  $3^{rd}$ -order harmonic will be filtered by  $H_i(3\omega)$  at the input, and the fundamental tone will be filtered by  $H_i(\omega)$  at the input.

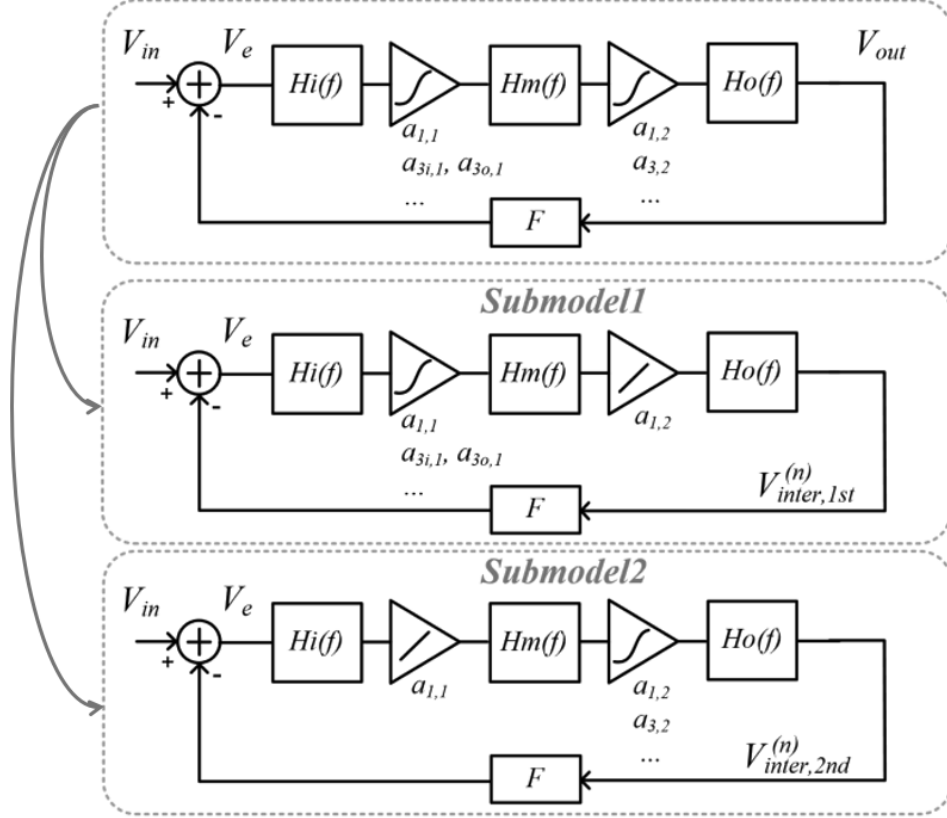


Figure 4.20: The two-stage nonlinear amplifier's model with the equivalent two sub-models. The input voltage amplitude  $V_i = I_{in}(R_{IN}||R_F)$ .

2. The first-stage interaction needs to distinguish the IRN and ORN. For the ORN, the filtering behavior of the interaction due to the nonlinear  $g_d$  is expressed in (4.58). For the IRN, the filtering behavior is as expressed in (4.61).

Based on these two considerations, the interaction's frequency response of the 5<sup>th</sup> harmonic can be expressed as (4.64). The  $V_{cls,1st}^{(3)}(\omega)$  expression in (4.65) is the overall closed-loop expression of 3<sup>rd</sup>-order harmonic originated from the first stage.

$$V_{inter,1st}^{(5)}(\omega) = \frac{3FV_{cls,1st}^{(3)}(\omega)V_e^2(\omega)}{4[1+LG(5\omega)]}H_i^2(\omega)H_i(3\omega)H_m(5\omega)H_o(5\omega)[a_{3,1i}a_{1,2}H_p(2\omega) + a_{3,1o}a_{1,2}H_m^2(\omega)H_m(3\omega)] \quad (4.64)$$

$$V_{cls,1st}^{(3)}(\omega) = \frac{1}{4[1 + LG(3\omega)]} \{a_{3i,1} [V_e(\omega)H_i(\omega)]^3 H_p(2\omega) + a_{3o,1} [V_e(\omega)a_{1,1}H_i(\omega)H_m(\omega)]^3 H_m(3\omega) H_o(3\omega)\} \quad (4.65)$$

Similar to the submodel1, the submodel2 can also be simplified as a single-stage amplifier. Though this submodel totally ignored the nonlinearity generated from the first-stage amplifier, due to the fact the second-stage amplifier's nonlinear harmonic will dominant at the low frequency, so this submodel can still be relatively accurate at low-frequency range.

The interaction at low frequency between the input fundamental tone and the feedback 3<sup>rd</sup>-order harmonic can be expressed as:

$$V_{inter,2nd}^{(5)} = \frac{3F}{4} \frac{a_{1,1}^3 \cdot a_{3,2}}{1 + LG} V_{cls,2nd}^{(3)} V_e^2 \quad (4.66)$$

where the  $V_{cls,2nd}^{(3)}$  is the closed-loop nonlinear harmonic originated from the second-stage amplifier, with a input fundamental tone current generated from the first stage. Notice that, there is another feedback loop from the output of the second-stage amplifier to its input through the compensation loop. However, this feedback voltage is too small compared with the voltage feedback through the main loop and amplified by the first amplifier. So for simplicity, we ignored the influence of this feedback loop. To model the frequency response using the submodel2, the following filtering behaviors need to be considered:

1. The fundamental input will be filtered by  $H_i(\omega)$  at the input and  $H_m(\omega)$  middle nodes.
2. The 3<sup>rd</sup>-order harmonic will be filtered by  $H_i(3\omega)$  at the input and  $H_m(3\omega)$  middle nodes.
3. The filtering at the second-stage, for example the additional poles/zeros and the output

poles/zeros, need to be expressed as  $H_{a2}(5\omega)$  and  $H_o(5\omega)$ .

With the above considerations, the 5<sup>th</sup>-order nonlinearity due to the interaction of the sub-model2 can be expressed as (4.67), and the closed-loop 3<sup>rd</sup>-order nonlinearity due to the second-stage amplifier's frequency response is expressed in (4.68):

$$V_{inter,2nd}^{(5)}(\omega) = \frac{3F(\omega)}{4[1 + LG(5\omega)]} a_{3,2} a_{1,1}^3 [V_e H_i(\omega) H_m(\omega)]^2 V_{cls,2nd}^{(3)}(\omega) H_m(3\omega) H_{a2}(5\omega) H_o(5\omega) \quad (4.67)$$

$$V_{cls,2nd}^{(3)}(\omega) = \frac{1}{4[1 + LG(3\omega)]} a_{3,2} [a_{1,1} V_e(\omega) H_i(\omega) H_m(\omega)]^3 H_{a2}(3\omega) H_o(3\omega) \quad (4.68)$$

The superposition of those two sub-models' harmonic voltages is the overall 5<sup>th</sup>-order distortion originated by the interaction of the lower-order harmonic. Then the overall 5<sup>th</sup>-order distortion voltage at the output can be expressed as:

$$V_{out}^{(5)}(\omega) = V_{out,ini}^{(5)}(\omega) - V_{inter,1st}^{(5)}(\omega) - V_{inter,2nd}^{(5)}(\omega) \quad (4.69)$$

With the modified model, the new modeling result compared with simulation is shown in Fig. 4.21. It can be observed that this model matches much better with the simulation compared with previous model shown in Fig. 4.17(b).

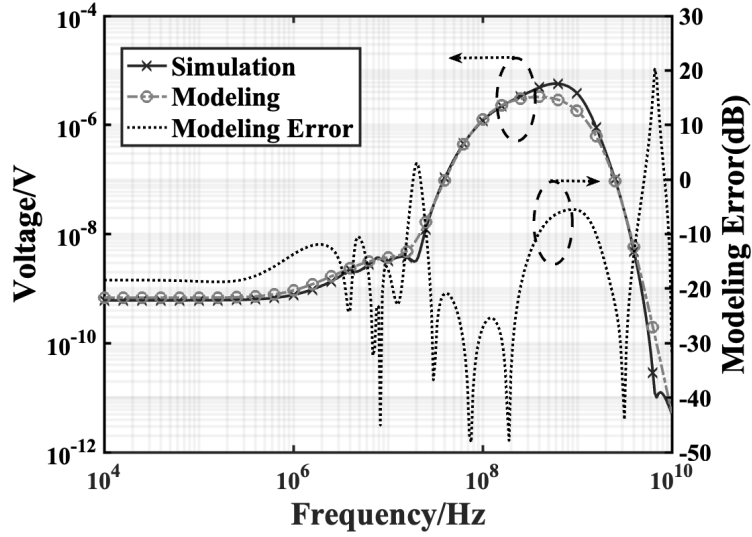


Figure 4.21: Comparison of the simulation and model results of the 5<sup>th</sup>-order nonlinearity, with considering the interactions between lower-order harmonics.

#### 4.3.4 Nonlinear-Feedback Frequency Analysis for Two-Stage $N^{\text{th}}$ -order Nonlinearity

For nonlinearities that are of order higher than three, both the initial nonlinearity originating from the devices, as well as the interactions originating from the interaction between the lower-order harmonics, are present. For the TIA studied in this chapter, it is the interaction component that is dominant. For example, for a 7<sup>th</sup>-order nonlinearity, the interactions of both the 5<sup>th</sup> harmonic with the fundamental, and the 3<sup>rd</sup>-order harmonic with the fundamental, must be accounted for. This can be generalized as follows:

$$V_{out}^{(n)} = V_{out,ini}^{(n)} - \sum_{k=1}^{\frac{n-3}{2}} \frac{(2k+1)F}{2^{2k}} \frac{a_{1+2k}}{1+LG} V_{out}^{(n-2k)} V_e^{2k} \quad (4.70)$$

where  $V_{out,ini}^{(n)}$  is the initial closed-loop nonlinearity originating from the two-stage TIA's



$n^{th}$ -order nonlinear sources, and given in (4.44). The  $V_{out}^{(n-2)}$  includes the initial  $(n - 2k)^{th}$ -order nonlinearity, together with all the interactions between lower-order harmonics with the fundamental tone. Fig. 4.22 shows the composition of the overall  $n^{th}$ -order nonlinearity according to (4.70).

Next, we need to include the frequency response into expression (4.70), similar to the analysis for the 5<sup>th</sup>-order harmonic frequency response analysis discussed in the last section. The  $n^{th}$ -order nonlinearity's frequency response also need to separate into two submodels, as shown in Fig. 4.20. The consideration for the frequency response analysis for submodel1 can be extend to the  $n^{th}$ -order as follows:

1. For the interaction between the  $(n - 2k)^{th}$ -order harmonic and the fundamental tone, the  $(n - 2k)^{th}$ -order harmonic will be filtered by  $H_i [(n - 2k)\omega]$  at the input, and the fundamental tone will be filtered by  $H_i (\omega)$  at the input.
2. The first-stage interaction also needs to distinguish the IRN and ORN. For the IRN, at the output of the first-stage amplifier, the  $n^{th}$ -order interaction distortion has been generated and the frequency response at this node and the following signal chain will need to change to  $H (n\omega)$ . For the ORN, the filtering condition is the case when apply both fundamental tone and the  $(n - 2k)^{th}$ -order distortion are applied at the load.

Based on these two considerations, the interaction part of the  $n^{th}$ -order harmonic of the simplified submodel1 can be expressed as (4.71). The  $V_{cls,1st}^{(n-2k)} (\omega)$  expression in (4.72) is the overall closed-loop expression of  $(n - 2k)^{th}$ -order harmonic contributed by the first stage.

$$\begin{aligned}
 V_{inter,1st}^{(n)} &= \sum_{k=1}^{\frac{n-3}{2}} \frac{(2k+1) FV_{cls,1st}^{(n-2k)} [(n-2k)\omega]}{2^{2k} [1 + LG(n\omega)]} V_e^{2k}(\omega). \\
 &H_i^{2k}(\omega) H_i [(n-2k)\omega] \{ a_{1+2k,1i} H_p(2k\omega) + \\
 &a_{1+2k,1o} a_{1,1}^{1+2k} H_m^{2k}(\omega) H_m [(n-2k)\omega] \} a_{1,2} H_m(n\omega) H_o(n\omega)
 \end{aligned} \tag{4.71}$$

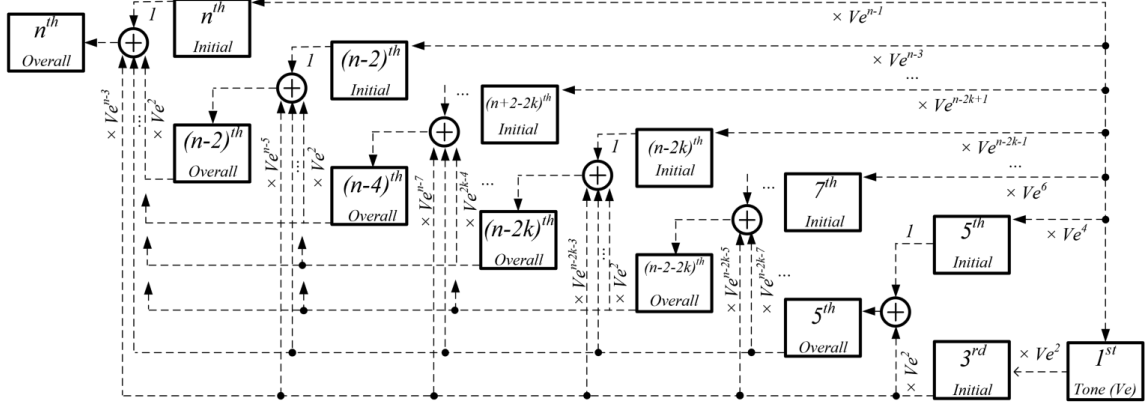


Figure 4.22: Harmonic interactions of the odd-order nonlinearities.

$$V_{cls,1st}^{(n-2k)}(\omega) = V_{out,ini,1st}^{(n-2k)}(\omega) - V_{inter,1st}^{(n-2k)}(\omega) \quad (4.72)$$

Similarly, for the sub-model 2, whose first-stage amplifier is considered linear and second-stage amplifier is considered nonlinear. When modeling the filtering behavior of the nonlinearity, the followings need to be considered:

1. The fundamental tone at the input will be filtered by  $H_i(\omega)$  at the input and  $H_m(\omega)$  middle nodes.
2. The  $(n-2k)^{th}$ -order harmonic will be filtered by  $H_i[(n-2k)\omega]$  at the input and  $H_o[(n-2k)\omega]$  middle nodes.
3. For the second stage amplifier's additional poles/zeros and the output node poles/zeros, their filtering for the  $n^{th}$ -order nonlinearity are expressed as  $H_{a2}(n\omega)$  and  $H_o(n\omega)$ .

With the above considerations, the  $n^{th}$ -order nonlinearity due to the interaction of the sub-model2 can be expressed as (4.73), the closed-loop  $(n-2k)^{th}$ -order nonlinearity frequency

response with consideration is expressed in (4.74).

$$V_{inter,2nd}^{(n)} = \sum_{k=1}^{\frac{n-3}{2}} \frac{(2k+1)F}{2^{2k}[1+LG(n\omega)]} a_{1,1}^{1+2k} a_{1+2k,2} H_i^{2k}(\omega) H_m^{2k}(\omega) H_i[(n-2k)\omega] \cdot H_m[(n-2k)\omega] V_{cls,2nd}^{(n-2k)}(\omega) V_e^{2k}(\omega) H_{a2}(n\omega) H_o(n\omega) \quad (4.73)$$

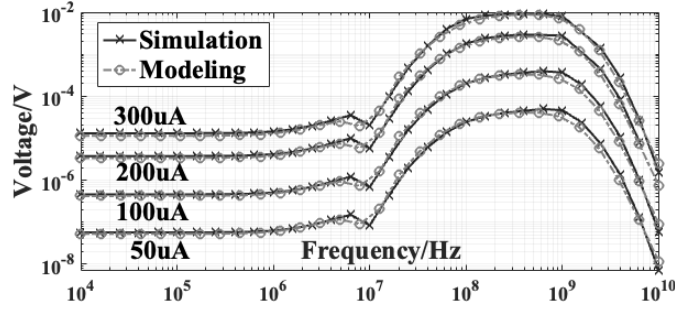
$$V_{cls,2nd}^{(n-2k)}(\omega) = V_{out,ini,2nd}^{(n-2k)}(\omega) - V_{inter,2nd}^{(n-2k)}(\omega) \quad (4.74)$$

The overall frequency response of the  $n$ th-order harmonic is given:

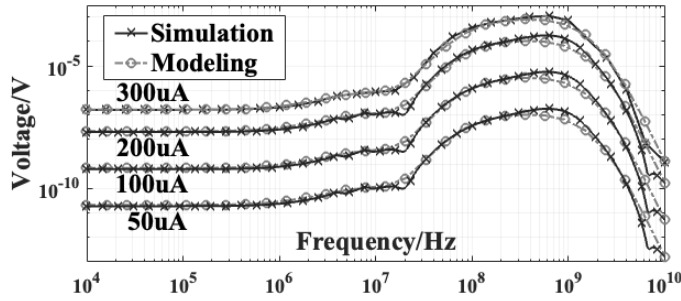
$$V_{out}^{(n)}(\omega) = V_{out,ini}^{(n)}(\omega) - V_{inter,1st}^{(n)}(\omega) - V_{inter,2nd}^{(n)}(\omega) \quad (4.75)$$

### 4.3.5 Model Verification

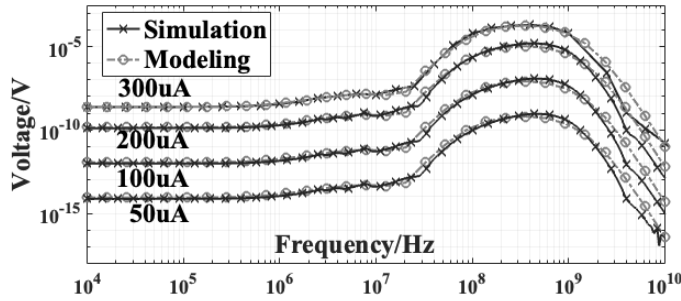
The model for the  $n^{th}$ -order nonlinearity expressed in (4.75) has been verified by using the device model from TowerSemi 0.18 $\mu$ m BiCMOS process sbc18h3 through simulation. A pseudo-steady-state simulation was used to directly find the output voltage harmonics. As mentioned in the previous section, in order to increase the accuracy of the simulation results, the voltage resolution of the simulator is set to be 1fV. To verify the model, multiple input current amplitudes are compared for both simulator and the model, and the comparison results are shown in Fig. 4.23. As the results show, the model results match the simulation results well at both the low-frequency (10kHz-10MHz) and the mid-frequency (10MHz-1GHz) bands, under a number of different input current amplitude conditions.



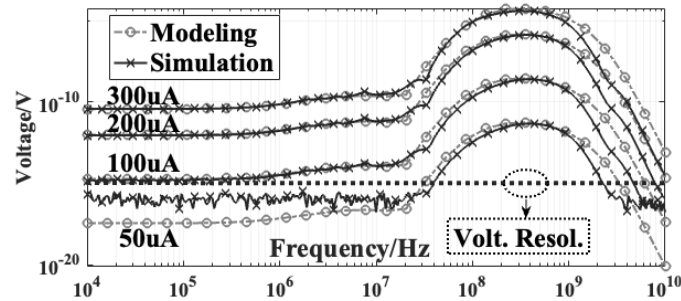
(a)



(b)



(c)



(d)

Figure 4.23: Comparison of closed-loop two-stage TIA's nonlinearities simulation and model results with different input current amplitude: a  $3^{rd}$ -order nonlinearity; b  $5^{th}$ -order nonlinearity; c  $7^{th}$ -order nonlinearity, d  $9^{th}$ -order nonlinearity.

# Chapter 5

## Conclusion

In this thesis, the design of two highly-integrated circuits for mmWave communication have been presented. In addition, analysis for the high-frequency nonlinearity behavior of a transimpedance amplifier (TIA) has also been presented. The conclusion for each work and their future potential research directions are discussed in the following sections.

### **5.1 mmWave MIMO Receiver Element for High-Speed and Low-Power Communication**

In the first work, a 28-GHz receiver element deploying one-bit direct detection for full-flexibility beamforming MIMO has been implemented. Low power consumption for each individual channel is achieved by using an additive-mixing based structure. A low-power one-bit ADC is also implemented on-chip, which allows for significant power savings thanks to coarse quantization and signal processing for each Rx element. The symbol-rate of 0.8GS/s with 16-QAM and 1GS/s with QPSK has been achieved with the total power consumption of 35 mW.

For future research, one possible direction would be to separate the single-ended LO from the composite LO and RF input signal, which would require a greater frequency separation between the two bands. With the separation between the LO and RF, one could make the circuit differential to enable the double-balanced mixing, thereby achieving a better performance for the Rx system. New filtering or antenna design techniques could possibly help to properly separate those two signals.

## 5.2 mmWave Transceiver for 5G Communication

In the second work, a 2-by-2 phased-array MIMO transceiver is presented which is targeted for the 5G NR (n257) band. The novel techniques for the transformer-based matching techniques to equalize the unbalanced gain have been analyzed and implemented to achieve a wider and flatter bandwidth. The wideband Wilkinson power combiner/splitter is also implemented on chip for combining the wideband down-converted IF band signal. The phase shifter is implemented with the combined passive and active techniques to achieve the phase shifting capability with  $1^\circ$  resolution and relatively low rms phase/gain errors. A 11.6dBm PA saturated output power is designed for a single Tx channel with 13.2% peak PAE. The modulation test has also been performed on the chip, which achieves a 5.7% EVM for single Tx-to-Rx and 9% for a 2-by-2 array wireless test for 16-QAM modulation.

The future research work could be the design of a larger antenna array with the chip implemented on this chip, so as to study the antenna patterns and communication qualities of a large antenna system. Another direction is to study and improve the performance of the on-chip phase shifter. The phase shifter can target at a wider LO phase shifting bandwidth with a smaller chip area. For the transceiver system, more techniques to flatten the in-band gain and sharper the out of band filtering can be studied.

## 5.3 Model for Amplifier's High-Frequency Nonlinearity Behavior

This work modeled the frequency behavior of the odd-order nonlinearities of a differential TIA. By distinguishing the filtering effect between the input and output of the amplifier, a definition of the IRN and ORN are given. Practical methods are given to find these nonlinear coefficients. By applying feedback theory to this two-stage amplifier system, the odd-order nonlinearities have been modeled, resulting in good matching with the simulation results.

For future research, one possible direction is trying to design and implement a high-linear TIA with wider linear bandwidth. Some new linear-bandwidth extension techniques could possibly come out with the known sources of the dominant linearity limitation components.

# Bibliography

- [1] M. Enescu, *5G New Radio: A beam-based air interface*. John Wiley & Sons, 2020.
- [2] A. M. Niknejad and H. Hashemi, *mm-Wave silicon technology: 60 GHz and beyond*. Springer Science & Business Media, 2008.
- [3] H. Zhao, R. Mayzus, S. Sun, M. Samimi, J. K. Schulz, Y. Azar, K. Wang, G. N. Wong, F. Gutierrez, and T. S. Rappaport, “28 GHz millimeter wave cellular communication measurements for reflection and penetration loss in and around buildings in New York city,” in *2013 IEEE International Conference on Communications (ICC)*, 2013, pp. 5163–5167.
- [4] I. Rodriguez, H. C. Nguyen, N. T. K. Jorgensen, T. B. Sorensen, and P. Mogensen, “Radio Propagation into Modern Buildings: Attenuation Measurements in the Range from 800 MHz to 18 GHz,” in *2014 IEEE 80th Vehicular Technology Conference (VTC2014-Fall)*, 2014, pp. 1–5.
- [5] M. K. Samimi and T. S. Rappaport, “3-D statistical channel model for millimeter-wave outdoor mobile broadband communications,” in *2015 IEEE International Conference on Communications (ICC)*, 2015, pp. 2430–2436.
- [6] Z. Pi and F. Khan, “An introduction to millimeter-wave mobile broadband systems,” *IEEE Communications Magazine*, vol. 49, no. 6, pp. 101–107, 2011.
- [7] L. Lu, G. Y. Li, A. L. Swindlehurst, A. Ashikhmin, and R. Zhang, “An Overview of Massive MIMO: Benefits and Challenges,” *IEEE Journal of Selected Topics in Signal Processing*, vol. 8, no. 5, pp. 742–758, 2014.
- [8] H. Q. Ngo, E. G. Larsson, and T. L. Marzetta, “Energy and Spectral Efficiency of Very Large Multiuser MIMO Systems,” *IEEE Transactions on Communications*, vol. 61, no. 4, pp. 1436–1449, 2013.
- [9] S. H. Talisa, K. W. O’Haver, T. M. Comberiate, M. D. Sharp, and O. F. Somerlock, “Benefits of Digital Phased Array Radars,” *Proceedings of the IEEE*, vol. 104, no. 3, pp. 530–543, 2016.
- [10] A. Alkhateeb, J. Mo, N. Gonzalez-Prelcic, and R. W. Heath, “Mimo precoding and combining solutions for millimeter-wave systems,” *IEEE Communications Magazine*, vol. 52, no. 12, pp. 122–131, 2014.



- [11] S. Han, C.-l. I, Z. Xu, and C. Rowell, “Large-scale antenna systems with hybrid analog and digital beamforming for millimeter wave 5G,” *IEEE Communications Magazine*, vol. 53, no. 1, pp. 186–194, 2015.
- [12] H. Pirzadeh and A. L. Swindlehurst, “Spectral Efficiency under Energy Constraint for Mixed-ADC MRC Massive MIMO,” *IEEE Signal Processing Letters*, vol. 24, no. 12, pp. 1847–1851, 2017.
- [13] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, “Millimeter-wave CMOS design,” *IEEE Journal of solid-state circuits*, vol. 40, no. 1, pp. 144–155, 2005.
- [14] F. Vecchi, M. Repposi, W. Eyssa, P. Arcioni, and F. Svelto, “Design of Low-Loss Transmission Lines in Scaled CMOS by Accurate Electromagnetic Simulations,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2605–2615, 2009.
- [15] T. Cheung and J. Long, “Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1183–1200, 2006.
- [16] G. Dambrine, C. Raynaud, D. Lederer, M. Dehan, O. Rozeaux, M. Vanmackelberg, F. Danneville, S. Lepilliet, and J.-P. Raskin, “What are the limiting parameters of deep-submicron MOSFETs for high frequency applications?” *IEEE Electron Device Letters*, vol. 24, no. 3, pp. 189–191, 2003.
- [17] C. Chen and A. Babakhani, “Wireless synchronization of mm-wave arrays in 65nm CMOS,” in *2015 IEEE Custom Integrated Circuits Conference (CICC)*. Citeseer, 2015, pp. 1–4.
- [18] B. Floyd, C.-M. Hung, and K. O, “Intra-chip wireless interconnect for clock distribution implemented with integrated antennas, receivers, and transmitters,” *IEEE Journal of Solid-State Circuits*, vol. 37, no. 5, pp. 543–552, 2002.
- [19] S. Emami, C. Doan, A. Niknejad, and R. Brodersen, “A 60-GHz down-converting CMOS single-gate mixer,” in *2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers*, 2005, pp. 163–166.
- [20] M. A. Abdelghany, R. K. Pokharel, H. Kanaya, and K. Yoshida, “Low-voltage low-power combined LNA-single gate mixer for 5GHz wireless systems,” in *2011 IEEE Radio Frequency Integrated Circuits Symposium*, 2011, pp. 1–4.
- [21] C. Ziomek and P. Corredoura, “Digital I/Q demodulator,” in *Proceedings Particle Accelerator Conference*, vol. 4, 1995, pp. 2663–2665 vol.4.
- [22] T.-K. Nguyen, N.-J. Oh, C.-Y. Cha, Y.-H. Oh, G.-J. Ihm, and S.-G. Lee, “Image-rejection cmos low-noise amplifier design optimization techniques,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 538–547, 2005.

- [23] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, “A Low-Cost Scalable 32-Element 28-GHz Phased Array Transceiver for 5G Communication Links Based on a  $2 \times 2$  Beamformer Flip-Chip Unit Cell,” *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, 2018.
- [24] J. Pang, R. Wu, Y. Wang, M. Dome, H. Kato, H. Huang, A. Tharayil Narayanan, H. Liu, B. Liu, T. Nakamura, T. Fujimura, M. Kawabuchi, R. Kubozoe, T. Miura, D. Matsumoto, Z. Li, N. Oshima, K. Motoi, S. Hori, K. Kunihiro, T. Kaneko, A. Shirane, and K. Okada, “A 28-GHz CMOS Phased-Array Transceiver Based on LO Phase-Shifting Architecture With Gain Invariant Phase Tuning for 5G New Radio,” *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1228–1242, 2019.
- [25] J. D. Dunworth, A. Homayoun, B.-H. Ku, Y.-C. Ou, K. Chakraborty, G. Liu, T. Segoria, J. Lerdworatawee, J. W. Park, H.-C. Park, H. Hedayati, D. Lu, P. Monat, K. Douglas, and V. Aparin, “A 28ghz bulk-cmos dual-polarization phased-array transceiver with 24 channels for 5g user and basestation equipment,” in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 70–72.
- [26] B. Sadhu, Y. Tousei, J. Hallin, S. Sahl, S. K. Reynolds, Renström, K. Sjögren, O. Haapalahti, N. Mazor, B. Bokinge, G. Weibull, H. Bengtsson, A. Carlinger, E. Westesson, J.-E. Thillberg, L. Rexberg, M. Yeck, X. Gu, M. Ferriss, D. Liu, D. Friedman, and A. Valdes-Garcia, “A 28-GHz 32-Element TRX Phased-Array IC With Concurrent Dual-Polarized Operation and Orthogonal Phase and Gain Control for 5G Communications,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, 2017.
- [27] R. Wu, R. Minami, Y. Tsukui, S. Kawai, Y. Seo, S. Sato, K. Kimura, S. Kondo, T. Ueno, N. Fajri, S. Maki, N. Nagashima, Y. Takeuchi, T. Yamaguchi, A. Musa, K. K. Tokgoz, T. Siriburanon, B. Liu, Y. Wang, J. Pang, N. Li, M. Miyahara, K. Okada, and A. Matsuzawa, “64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2871–2891, 2017.
- [28] M. Vigilante and P. Reynaert, “On the Design of Wideband Transformer-Based Fourth Order Matching Networks for  $E$  -Band Receivers in 28-nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2071–2082, 2017.
- [29] C.-H. Li, C.-N. Kuo, and M.-C. Kuo, “A 1.2-V 5.2-mW 20–30-GHz Wideband Receiver Front-End in 0.18- $\mu$ m CMOS,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 11, pp. 3502–3512, 2012.
- [30] F. Vecchi, S. Bozzola, E. Temporiti, D. Guermandi, M. Pozzoni, M. Repossi, M. Cusmai, U. Decanis, A. Mazzanti, and F. Svelto, “A wideband receiver for multi-Gbit/s communications in 65 nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 3, pp. 551–561, 2011.
- [31] V. Bhagavatula, T. Zhang, A. R. Suvarna, and J. C. Rudell, “An Ultra-Wideband IF Millimeter-Wave Receiver With a 20 GHz Channel Bandwidth Using Gain-Equalized Transformers,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 323–331, 2016.

- [32] A. Mazzanti and A. Bevilacqua, “On the phase noise performance of transformer-based CMOS differential-pair harmonic oscillators,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 9, pp. 2334–2341, 2015.
- [33] I. Kallfass, S. Diebold, H. Massler, S. Koch, M. Seelmann-Eggebert, and A. Leuther, “Multiple-throw millimeter-wave FET switches for frequencies from 60 up to 120 GHz,” in *2008 38th European Microwave Conference*. IEEE, 2008, pp. 1453–1456.
- [34] B. Analui and A. Hajimiri, “Statistical analysis of integrated passive delay lines,” in *Proceedings of the IEEE 2003 Custom Integrated Circuits Conference, 2003.*, 2003, pp. 107–110.
- [35] J. Sewter and A. Carusone, “A CMOS finite impulse response filter with a crossover traveling wave topology for equalization up to 30 Gb/s,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 4, pp. 909–917, 2006.
- [36] R. L. Schmid, A. Ulusoy, P. Song, and J. D. Cressler, “A 94 GHz, 1.4 dB Insertion Loss Single-Pole Double-Throw Switch Using Reverse-Saturated SiGe HBTs,” *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 1, pp. 56–58, 2014.
- [37] Y. Xu and R. G. Bosisio, “Design of Multiway Power Divider by Using Stepped-Impedance Transformers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 9, pp. 2781–2790, 2012.
- [38] J. Zhou, K. A. Morris, and M. J. Lancaster, “General Design of Multiway Multisection Power Dividers by Interconnecting Two-Way Dividers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 10, pp. 2208–2215, 2007.
- [39] A. Musa, R. Murakami, T. Sato, W. Chaivipas, K. Okada, and A. Matsuzawa, “A Low Phase Noise Quadrature Injection Locked Frequency Synthesizer for MM-Wave Applications,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 11, pp. 2635–2649, 2011.
- [40] A. Nagra, J. Xu, E. Erker, and R. York, “Monolithic GaAs phase shifter circuit with low insertion loss and continuous 0-360° phase shift at 20 GHz,” *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 1, pp. 31–33, 1999.
- [41] Z. Duan, Y. Wang, W. Lv, Y. Dai, and F. Lin, “A 6-bit CMOS Active Phase Shifter for Ku-Band Phased Arrays,” *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 7, pp. 615–617, 2018.
- [42] B. Wang, H. Gao, M. K. Matters-Kammerer, and P. Baltus, “A 60 GHz 360° Phase Shifter with 2.7° Phase Resolution and 1.4° RMS Phase Error in a 40-nm CMOS Technology,” in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2018, pp. 144–147.
- [43] S. Y. Kim, D.-W. Kang, K.-J. Koh, and G. M. Rebeiz, “An Improved Wideband All-Pass I/Q Network for Millimeter-Wave Phase Shifters,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 11, pp. 3431–3439, 2012.

- [44] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS. Circuit design layout and simulation*. IEEE Press, 1998.
- [45] M. A. Ghanad, C. Dehollain, and M. M. Green, "TIA Linearity Analysis for Current Mode Receivers," in *2018 16th IEEE International New Circuits and Systems Conference (NEWCAS)*, 2018, pp. 53–56.
- [46] G. Palumbo and S. Pennisi, "High-frequency harmonic distortion in feedback amplifiers: analysis and applications," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 3, pp. 328–340, 2003.
- [47] P. Wambacq, G. Gielen, P. Kinget, and W. Sansen, "High-frequency distortion analysis of analog integrated circuits," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 3, pp. 335–345, 1999.
- [48] S. Cannizzaro, G. Palumbo, and S. Pennisi, "Distortion analysis of Miller-compensated three-stage amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 5, pp. 961–976, 2006.
- [49] R. Meyer, M. Shensa, and R. Eschenbach, "Cross modulation and intermodulation in amplifiers at high frequencies," *IEEE Journal of Solid-State Circuits*, vol. 7, no. 1, pp. 16–23, 1972.
- [50] G. Shi, "Symbolic Distortion Analysis of Multistage Amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 1, pp. 369–382, 2019.
- [51] Y. Miao and Y. Zhang, "Distortion Modeling of Feedback Two-Stage Amplifier Compensated With Miller Capacitor and Nulling Resistor," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 93–105, 2012.
- [52] B. Hernes and W. Sansen, "Distortion in single-, two- and three-stage amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 5, pp. 846–856, 2005.
- [53] B. Hernes and T. Saether, "Design criteria for low distortion in feedback opamp circuits," 01 2003.
- [54] A. Borys, "On analysis of harmonic distortion in op amps based circuits via Volterra series," in *2016 MIXDES - 23rd International Conference Mixed Design of Integrated Circuits and Systems*, 2016, pp. 330–335.
- [55] H. Yu, K. El-Sankary, and E. I. El-Masry, "Distortion Analysis Using Volterra Series and Linearization Technique of Nano-Scale Bulk-Driven CMOS RF Amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 1, pp. 19–28, 2015.
- [56] R. Minasian, "Intermodulation Distortion Analysis of MESFET Amplifiers Using the Volterra Series Representation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 28, no. 1, pp. 1–8, 1980.

- [57] P. J. H. S. H. L. Gray, Paul R. and R. G. Meyer., “Analysis and design of analog integrated circuits. John Wiley Sons, 2009.”
- [58] A. Khadr and R. Johnston, “Distortion in high-frequency FET amplifiers,” *IEEE Journal of Solid-State Circuits*, vol. 9, no. 4, pp. 180–189, 1974.
- [59] R. Baki, T. Tsang, and M. El-Gamal, “Distortion in RF CMOS short-channel low-noise amplifiers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 1, pp. 46–56, 2006.
- [60] S. Kang, B. Choi, and B. Kim, “Linearity analysis of CMOS for RF application,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 3, pp. 972–977, 2003.
- [61] S. Cannizzaro, G. Palumbo, and S. Pennisi, “Effects of nonlinear feedback in the frequency domain,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 2, pp. 225–234, 2006.
- [62] G. Palumbo, M. Pennisi, and S. Pennisi, “Miller Theorem for Weakly Nonlinear Feedback Circuits and Application to CE Amplifier,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 10, pp. 991–995, 2008.
- [63] G. Palumbo and S. Pennisi, “High-frequency harmonic distortion in feedback amplifiers: analysis and applications,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 3, pp. 328–340, 2003.
- [64] P. Wambacq and W. M. Sansen, *Distortion analysis of analog integrated circuits. Vol. 451*. Springer Science & Business Media, 2013.
- [65] W. Sansen, “Distortion in elementary transistor circuits,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 3, pp. 315–325, 1999.