Title

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A Multi-Time Programmable Memory Technology in a Native 14nm FINFET Process using Charge Trap Transistors (CTTs)

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***Abstract*—**Described is a Multi-Time Programmable Memory (MTPM) solution, manufactured in a 14 nm bulk FINFET technology, which requires no process adders or additional masks, using Charge Trap Transistors (CTTs). Outlined are the technological breakthroughs required to support multi-time program and erase of CTTs for this secure embedded non-volatile memory (eNVM) technology. For the first time, hardware results demonstrate an endurance of > 10^3 Program/Erase cycles. Data retention lifetime of > 10 years at 125 °C and scalability to 7 nm has been confirmed.

I. Introduction

Charge Trap Transistors (CTTs), Fig. 1, are as-fabricated high-k metal gate (HKMG) logic transistors [1], whose threshold voltages (V_T) may be modified by application of appropriate logic compatible voltages, where device self-heating enhanced charge trapping in the high-k gate dielectric ensures high data retention [2]. Unlike other charge trapping [3] and anti-fuse [4] memories, CTTs offer a process-free and multi-time programmable memory (MTPM) solution for embedded applications. CTTs are programmed using short gate bias (V_G) pulses of 1.8-2.0V with a drain bias (V_D) of 1.4-1.6V, while the source bias (V_S) and the substrate bias (V_X) are at 0V. We have developed a 1.5Mb CTT One-Time-Programmable-Memory (OTPM) product [5], Fig. 2, partially funded by the Defense MicroElectronics Activity (DMEA). However, poor erase efficiency, and consequent low Program/Erase (P/E) cycling endurance, has restricted the use of CTTs for multi-time programmable memory (MTPM) applications thus far. We introduce a technique that drastically improves the erase efficiency, and in turn, the cycling endurance of the CTT MTPM. For the first time, hardware results demonstrate support for > 10^3 P/E cycles, a 100× improvement in endurance, which is adequate for most embedded MTPM applications such as hardware security, encryption, firmware, chip ID, configuration, and repair. CTT eNVM is a secure solution, as the coded bitmaps cannot be decoded using any presently known failure analysis techniques.

II. "Self-Heating Temperature Assisted Erase" (STAR) for Improved Erase Efficiency

Conventional erase operations, Fig. 3 (a), are typically performed using a negative V_G of magnitude > |2.5V|, while V_S, V_D, and V_X are at 0V, to electrostatically emit trapped charge and reduce the V_T. The conventional erase method, however, leads to a partial V_T recovery. The "Self-heating Temperature Assisted eRase" (STAR) technique, Fig. 3 (b), utilizes the source-substrate-drain structure of the device as a parasitic NPN bipolar junction transistor (BJT) to pass a current (comparable to the channel current during programming) through the device body during the erase operation. The device terminals are biased such that the BJT is in the active mode while there is a negative gate-to-substrate bias (V_{GX}) at the same time, without the need for any negative voltages. The device self-heating caused by the BJT current, in combination with the negative V_{GX}, significantly enhances the charge de-trapping process and allows for an erase efficiency of up to ~100% to be achieved using lower voltages and shorter time, as compared to the conventional erase method (100% erase within 1ms using STAR vs. < 50% even after 1s of conventional erase). Pre-program, post-program, and post-erase I_D-V_G measurements of CTTs erased using the conventional method and STAR are shown is Figs. 4 (a) and (b), respectively. Measured post-program and post-erase 'read' currents vs. P/E cycle number for CTTs cycled using conventional erase and STAR are shown in Figs. 5 (a) and (b), respectively. With the conventional method, incomplete erase after each cycle causes the memory window to dynamically drift and become narrower, resulting in a shrinking read margin. This severely limits the endurance (< 15 P/E cycles) and makes it challenging for implementation of CTTs as an MTPM technology, as circuits to dynamically change the reference current are difficult to implement. On the other hand, the STAR technique yields a flat memory window with no sign of narrowing for 1500 P/E cycles.

High-temperature charge retention bake tests, Fig. 6, performed on 14 nm FINFET CTTs (cycled using V_G = 1.95V, V_D = 1.55V for programming and erased using the STAR technique), show a projected 10 year charge loss of < 30% at 125 °C. The charge de-trapping activation energy (E_a), extracted using the conventional Arrhenius model, is ~1.85 eV. This is comparable to the reported E_a for one-time programmable 14nm bulk FINFET CTTs [5].

III. Conclusions and Outlook

We have demonstrated the feasibility of an MTPM with > 10^3 P/E cycling endurance using CTTs in 14nm FINFET technology as an embedded non-volatile memory solution for HKMG technologies that is logic voltage compatible and exhibits > 10 year data retention at 125 °C, without the need for any added processes or masks. The predicted MTPM IP is

256kb/mm^2. The scalability of CTTs to 7 nm FINFET technologies has been confirmed: ~100% erase efficiency and P/E cycling using STAR are shown in Fig. 7.

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REFERENCES

[1] J. Singh *et al.*, Symp. VLSI Technology, 2017, pp. T140-T141.
[2] F. Khan, IEEE EDL, Jan. 2016, pp. 88-91.
[3] S. Tsuda *et al.*, Proc. IEEE IEDM, Dec. 2017, pp. 469-472.
[4] S.-Y. Chou *et al.*, ISSC, 2017, pp. 199-202.
[5] E. Hunt-Schroeder *et al*, Symp. VLSI Circuits, 2018, pp. 87-88.

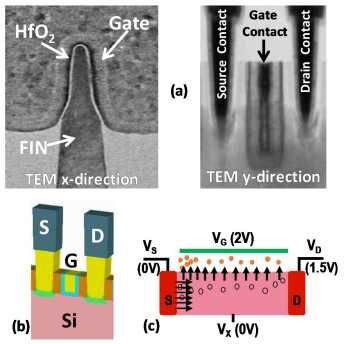

Fig. 1. 14nm FINFET CTT (a) TEM cross-sections in x- and y-directions, (b) 3D schematic, and (c) schematic of the programming operation.

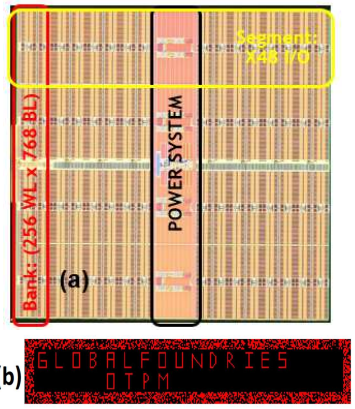

Fig. 2. (a) Chip photomicrograph of the 1.5Mb OTPM product IP for 14nm FINFET node, (b) Bitmap displaying "GLOBALFOUNDRIES OTPM".

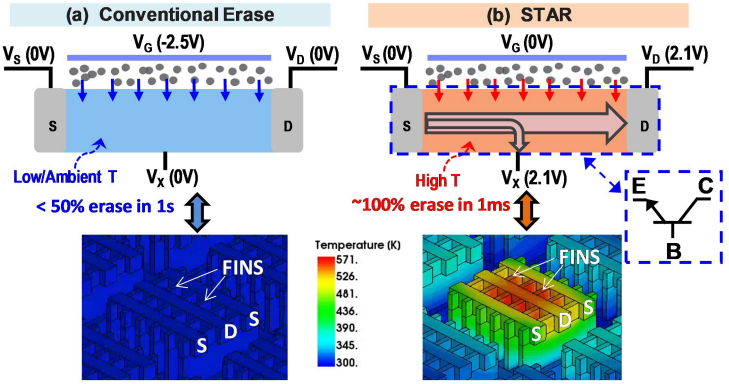

Fig. 3. Schematic showing (a) Conventional erase and (b) "Self-heating Temperature Assisted eRase" (STAR). Corresponding thermal profiles are also shown for comparison of bitcell temperatures during the erase.

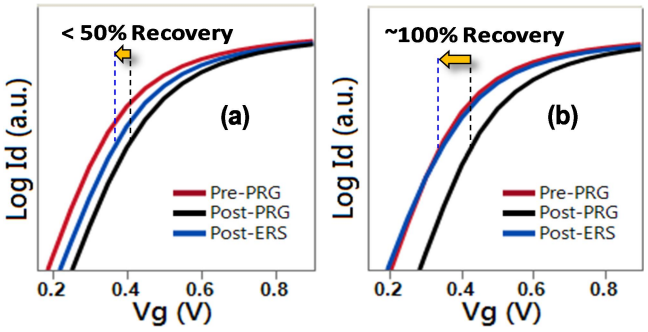

Fig. 4. Measured Pre-program, Post-program, and Post-erase I_D-V_G for CTTs erased using (a) conventional erase and (b) STAR.

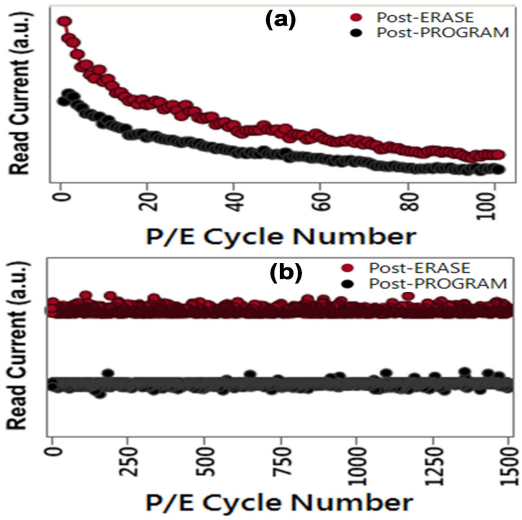

Fig. 5. Post-Program/Erase 'read' currents vs. P/E cycles for 14 nm CTTs using (a) conventional erase and (b) STAR.

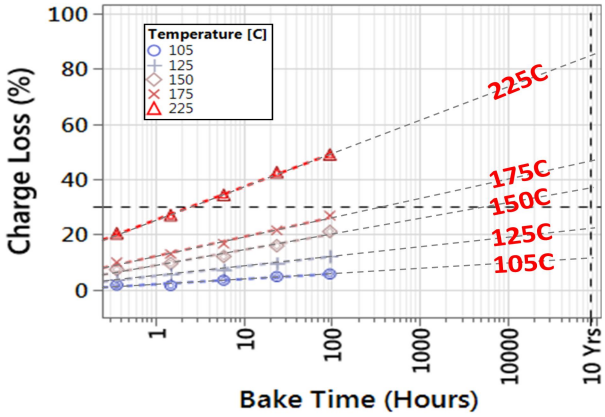

Fig. 6. High temperature charge retention bake tests (@ 105, 125, 150, 175, 225 °C) for cycled CTT MTPM devices. The extracted Arrhenius E_a is ~1.85 eV.

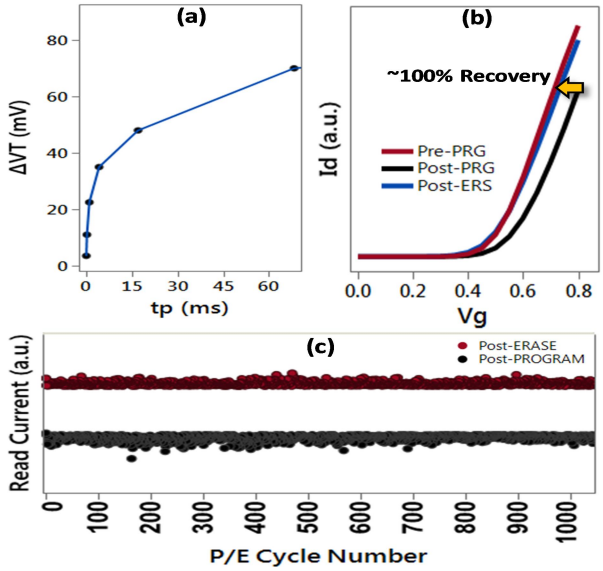

Fig. 7. Preliminary hardware results for 7nm FINFET CTTs: (a) ΔV_T vs. t_P for programming at V_G = 1.9V, V_D = 1.5V (b) pre-program, post-program, post-erase I_D-V_G, and (c) P/E cycling. The erase in (b) and (c) was done using STAR.