UNIVERSITY OF CALIFORNIA,
IRVINE

Preparation of Power Distribution System for High Penetration of Renewable Energy
Part I. Dynamic Voltage Restorer for Voltage Regulation
Pat II. Distribution Circuit Modeling and Validation

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

by

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Dissertation Committee:
Professor Keyue Smedley, Chair
Professor Michael Green
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DEDICATION

To

Sima who is not just my wonderful wife, but also the greatest friend I could ever have,

Our exuberant, sweet, and kind-hearted little son, Elvin, to recharge and revitalize my mind and spirit every day after coming back home from school,

and

My always encouraging parents, Fatemeh and Jafar, for teaching me love, generosity and good manners.

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PUBLICATIONS

[1] A. Khoshkbar-Sadigh and K. M. Smedley, "Review of voltage compensation methods in dynamic voltage restorer (DVR)," in IEEE Power and Energy Society General Meeting, 2012, pp. 1–8.

[2] A. Khoshkbar-Sadigh and K. M. Smedley, "Fast voltage sag detection method for single-/three-phase application," in 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2013, pp. 881–888.

[3] A. Khoshkbar-Sadigh and K. Smedley, "A Fast and Precise Voltage Sag Detection Method for Dynamic Voltage Restorer (DVR) Application," IEEE Trans. Power Electron., (Revision has been submitted).

[4] A. Khoshkbar-Sadigh and K. Smedley, "The Necessity of Time-Series Simulation for Investigation of Large-Scale Solar Energy Penetration," in 6th Innovative Smart Grid Technologies, (Accepted for publication).

[5] A. Khoshkbar-Sadigh, M. Heydari, M. Tedde, R. Arghandeh, K. Smedley, and A. Von-Meier, "A Unified Platform Enabling Power System Circuit Model Data Transfer Among Different Software," in 6th Innovative Smart Grid Technologies, (Accepted for publication).

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ABSTRACT OF THE DISSERTATION

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Part I: Dynamic Voltage Restorer

In the present power grids, voltage sag is recognized as a serious threat and a frequently occurring power-quality problem and has costly consequences such as sensitive loads tripping and production loss. Consequently, the demand for high power quality and voltage stability becomes a pressing issue. Dynamic voltage restorer (DVR), as a custom power device, is more effective and direct solutions for "restoring" the quality of voltage at its load-side terminals when the quality of voltage at its source-side terminals is disturbed.

In the first part of this thesis, a DVR configuration with no need of bulky dc link capacitor or energy storage is proposed. This fact causes to reduce the size of the DVR and increase the reliability of the circuit. In addition, the proposed DVR topology is based on high-frequency isolation transformer resulting in the size reduction of transformer. The proposed DVR circuit, which is suitable for both low- and medium-voltage applications, is based on dc-ac converters connected in series to split the main dc link between the inputs of dc-ac converters. This feature makes it possible to use modular dc-ac converters and

utilize low-voltage components in these converters whenever it is required to use DVR in medium-voltage application. The proposed configuration is tested under different conditions of load power factor and grid voltage harmonic. It has been shown that proposed DVR can compensate the voltage sag effectively and protect the sensitive loads.

Following the proposition of the DVR topology, a fundamental voltage amplitude detection method which is applicable in both single/three-phase systems for DVR applications is proposed. The advantages of proposed method include application in distorted power grid with no need of any low-pass filter, precise and reliable detection, simple computation and implementation without using a phased locked loop and lookup table. The proposed method has been verified by simulation and experimental tests under various conditions considering all possible cases such as different amounts of voltage sag depth (VSD), different amounts of point-on-wave (POW) at which voltage sag occurs, harmonic distortion, line frequency variation, and phase jump (PJ). Furthermore, the ripple amount of fundamental voltage amplitude calculated by the proposed method and its error is analyzed considering the line frequency variation together with harmonic distortion. The best and worst detection time of proposed method were measured 1ms and 8.8ms, respectively. Finally, the proposed method has been compared with other voltage sag detection methods available in literature.

Part 2: Power System Modeling for Renewable Energy Integration

As power distribution systems are evolving into more complex networks, electrical engineers have to rely on software tools to perform circuit analysis. There are dozens of powerful software tools available in the market to perform the power system studies.

Although their main functions are similar, there are differences in features and formatting structures to suit specific applications. This creates challenges for transferring power system circuit models data (PSCMD) between different software and rebuilding the same circuit in the second software environment. The objective of this part of thesis is to develop a Unified Platform (UP) to facilitate transferring PSCMD among different software packages and relieve the challenges of the circuit model conversion process. UP uses a commonly available spreadsheet file with a defined format, for any home software to write data to and for any destination software to read data from, via a script-based application called PSCMD transfer application. The main considerations in developing the UP are to minimize manual intervention and import a one-line diagram into the destination software or export it from the source software, with all details to allow load flow, short circuit and other analyses. In this study, ETAP, OpenDSS, and GridLab-D are considered, and PSCMD transfer applications written in MATLAB have been developed for each of these to read the circuit model data provided in the UP spreadsheet. In order to test the developed PSCMD transfer applications, circuit model data of a test circuit and a power distribution circuit from Southern California Edison (SCE) – a utility company – both built in CYME, were exported into the spreadsheet file according to the UP format. Thereafter, circuit model data were imported successfully from the spreadsheet files into above mentioned software using the PSCMD transfer applications developed for each software.

After the SCE studied circuit is transferred into OpenDSS software using the proposed UP scheme and developed application, it has been studied to investigate the impacts of large-scale solar energy penetration. The main challenge of solar energy integration into power grid is its intermittency (i.e., discontinuity of output power) nature

due to cloud shading of photovoltaic panels which depends on weather conditions. In order to conduct this study, OpenDSS time-series simulation feature, which is required due to intermittency of solar energy, is utilized. In this study, the impacts of intermittency of solar energy penetration, especially high-variability points, on voltage fluctuation and operation of capacitor bank and voltage regulator is provided. In addition, the necessity to interpolate and resample unequally spaced time-series measurement data and convert them to equally spaced time-series data as well as the effect of resampling time-interval on the amount of error is discussed. Two applications are developed in Matlab to do interpolation and resampling as well as to calculate the amount of error for different resampling time-intervals to figure out the suitable resampling time-interval. Furthermore, an approach based on cumulative distribution, regarding the length for lines/cables types and the power rating for loads, is presented to prioritize which loads, lines and cables the meters should be installed at to have the most effect on model validation.

Chapter 1: Dynamic Voltage Restorer (DVR)

1.1. Introduction

Sensitive loads such as medical equipment, factory automations, semiconductor-device manufacturer, and paper manufacturer are vulnerable to power-supply disturbances [1], [2]. Consequently, the demand for high power quality and voltage stability becomes a pressing issue. In the present, voltage sags are recognized as a serious threat to the power grid and are a frequently occurring power-quality problem and have costly consequence such as sensitive loads tripping and production loss [3]–[6]. Both the "Canadian Power Quality Survey" conducted by the Canadian Electrical Associate (CEA) in 1991 on 550 customer sites and the "Distribution System Power Quality Survey" conducted by the Electric Power Research Institute (EPRI) on 222 utility distribution feeders between 1993 and 1995 have shown that voltage sags are the most frequent power quality events [7]. According to an EPRI report, the economic losses due to poor power quality are $400 billion dollars a year in the U.S. alone [8], [9]. These disturbances occur due to, *e.g.,* short circuits in upstream power transmission line or parallel power distribution line connected to the point of common coupling (PCC), inrush currents involved with the starting of large machines, sudden changes of load, energizing of transformers or switching operations in the grid [10], [11]. According to the IEEE STD 1959-1995 and IEEE STD 1564-2014 (IEEE Guide for Voltage Sag Indices), voltage sag is defined as a decrease of 0.1 to 0.9 p.u. in the rms voltage at system frequency and with the duration of half a cycle to one minute [12]–[14]. According to the definition and nature of voltage sag, it can be found that this kind of disturbance is a transient phenomenon whose causes are classified as low- or medium-frequency transient events [12].

Due to the above mentioned effects of voltage sags on sensitive loads, compensating voltage sags and minimizing their effects is necessary. Traditional methods of suppressing voltage variations include static transfer switches (STS), tap-changing transformers, and uninterruptible power supplies (UPS) [15]. However, tap-changing transformer is bulky, costly and not fast enough to eliminate the voltage sag effects at load side. On the other hand, UPS is bulky and expensive device which needs energy storage such as battery. Furthermore, UPS systems are typically designed for small loads, such as a computer mainframe or low-power safety critical systems. Since voltage sags are the most troublesome on the distribution network, where loads can range from tens of kilowatts to a few megawatts, the cost of a UPS system is prohibitive as the UPS would need to be able to withstand not only the load current, but also the full load voltage [15]. There are custom power devices such as static synchronous compensator (STATCOM), distribution-STATCOM (D-STATCOM), unified power-quality conditioner (UPQC), and dynamic voltage restorer (DVR) as power electronics based solutions to minimize costly outcomes of voltage sags [15]. The custom power devices are developed and installed at consumer point to meet the power quality standards such as IEEE-519. Among the available technologies, DVR is more effective and direct solution (it only needs to withstand part of the load voltage) for "restoring" the quality of voltage at its load-side terminals when the quality of voltage at its source-side terminals is disturbed [16]–[21].

DVRs compensate voltage sags by injecting the proper amount of voltages in series with the supply voltage, in order to maintain the load side voltage within the specification [22]–[25]. Typically, a DVR consists of an energy storage device and an inverter which is

coupled via a series transformer to the grid. The purpose of inverter is injecting the series voltage with a controlled magnitude and phase angle to restore the quality of load voltage and avoid load tripping [6], [26], [27]. The basic concept of DVR is depicted in Figure 1.1.

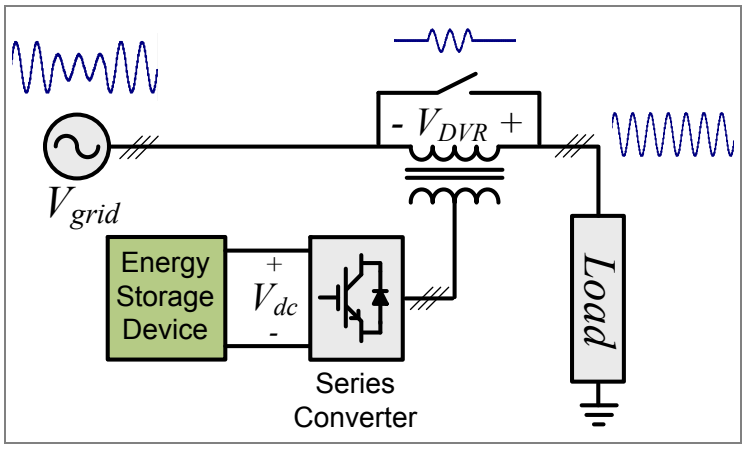

Figure 1.1. General schematic of DVR.

The control system of DVR has two main parts: detection of the voltage sag and determination of the reference signal. The voltage sag detection part measures and analyzes the grid voltage to detect any voltage disturbance. There are different detection methods such as peak measurement, rms measurement, *dq0* components measurement [1], [28], decoupled positive- and negative-sequence *dq0* components measurement [27], [29]–[31] and phasor parameters estimation using Kalman filters [32], [33] or complex Fourier Transformation as reported in articles [34], [35]. The voltage sag detection methods will be investigated in detail in Chapter 2. The second part of DVR control system is determination of the DVR reference signal of series injected voltage. The method to determine reference signal of series injected voltage is based on the type of voltage sag compensation method, type of energy storage device and its ability to support active power. There are four basic methods of voltage compensation which are in-phase, pre-sag,

energy minimized and hybrid compensation methods.

This chapter is organized as follows. Section 1.2 investigates four mentioned compensation methods with the detailed discussions and analysis. Moreover, a comparison of the mentioned compensation methods is conducted to highlight their advantages and disadvantages. In Section 1.3, DVR circuit topologies are discussed regarding the possible configurations and approaches to feed active power to DVR dc link since DVR may need active power to restore the voltage quality of sensitive loads. In addition, effect of the upstream step-down transformer on causing the zero-sequence voltage sag is discussed in Section 1.4. In Section 1.5, DVR reference voltage determination is explained in detail and the required equations are obtained based on d-q synchronous reference frame. In Section 1.6, a new topology of DVR based on high-frequency isolation transformer is proposed to reduce the size of transformer and its control strategy is presented. Another advantage of the proposed DVR configuration is that it does not need any bulky dc link capacitor or energy storage to make a flat dc link voltage. This fact causes to reduce the size of the DVR and increase the reliability of the circuit. The proposed DVR circuit is based on dc-ac converters connected in series to split the main dc link between the inputs of dc-ac converters. This feature makes it possible to use modular dc-ac converters and utilize low-voltage components in these converters whenever it is required to use DVR in medium-voltage application. In Section 1.7, simulation results of the proposed DVR topology are provided to show its performance and effectiveness to compensate the voltage sag.

1.2. Review of Voltage Sag Compensation Methods

As mentioned previously, there are four different compensation methods to restore the voltage quality of sensitive loads by DVR. In the following subsections, these four methods are explained in detail and compared to emphasize their pros and cons.

1.2.1. In-Phase Voltage Sag Compensation Method

The in-phase compensation strategy is the straightest forward method in which the injected DVR voltage is in phase with the supply side voltage regardless of pre-fault condition [1], [5], [7], [22]. The phasor diagram of the in-phase compensation strategy is shown in Figure 1.2 in which the dashed quantities (V'_{grid}, V'_{load}, V'_{dvr} and I'_{load}) indicate variables after the sag. The phasors prior to the sag are represented by V_{grid}, V_{load} and I_{load}. Moreover, angle of ϕ is phase angle difference between the load voltage and load current phasors and angle of δ is phase jump of grid voltage during the voltage sag. All of the load and grid voltage phasors are line-to-neutral voltages. To realize this strategy, phase-locked loop (PLL) has to be synchronized to the grid voltage all the time and therefore, PLL will not be locked during the compensation [1], [22].

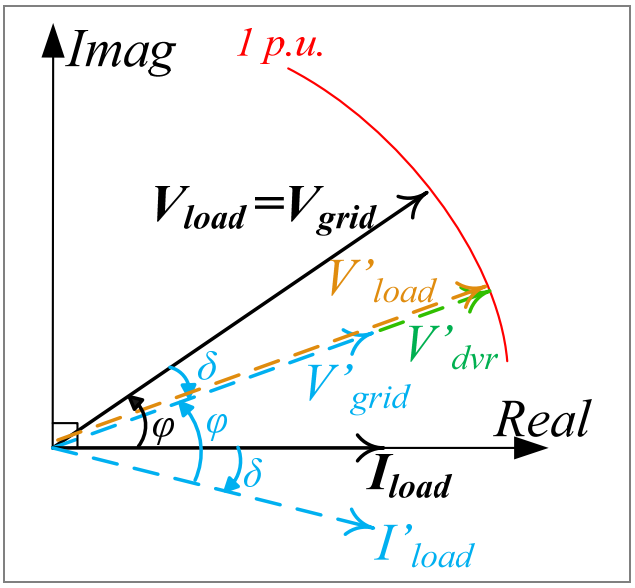

Figure 1.2. Phasor diagram of in-phase compensation strategy.

It is worth mentioning that this compensation strategy leads to minimize the magnitude of series injected voltage by DVR in comparison with other compensation methods [1], [5]. Consequently, voltage rating of dc link in this method is minimal. However, in-phase compensation method just leads to correct the load voltage magnitude and can't correct the phase jump at load voltage if voltage sag occurs with phase jump. Therefore, the distortions of phase changes are not compensated and as a consequence, a phase jump will occur at the load side which may lead to transient and circulating currents depending on the load type [1]. Regarding the amount of active power exchanged between DVR and power grid, this method injects both active and reactive power. The reason for injecting active power is that injected voltage phasor is not certainly perpendicular to the load current phasor. Consequently, it needs the active power to be supplied at dc link side otherwise this method can't compensate deep voltage sags for a long time. Thus, without supporting the active power at the dc link, it will drop during the compensation and as a

result, the maximum producible voltage of DVR will decrease. Furthermore, the modulation index of series converter will increase continuously and may hit the maximum value; therefore, over-modulation may occur causing undesirable harmonics at the output voltage of power converter.

The power rating of DVR controlled by in-phase compensation method is as follows:

$$S_{DVR} = \sum_{k=a\ ,\ b\ ,\ c} \left[V'_{DVR,k} \cdot I_{load} \right] \qquad \text{Eq. 1.1}$$

where, $V'_{DVR,k}$ is the rms of DVR injected voltage in phase *k* and I_{load} is rms of load current. The amount of active power exchanged between the DVR and power grid is as follows:

$$P_{DVR} = P_{load} - P_{grid} = \left[\begin{array}{l} 3 \cdot V_{load} \cdot I_{load} \cdot \cos(\phi) \\ - \sum_{k=a\ ,\ b\ ,\ c} \left[V'_{grid,k} \cdot I_{load} \cdot \cos(\phi) \right] \end{array} \right] \qquad \text{Eq. 1.2}$$

where, $V'_{grid,k}$ is the rms of line-to-neutral grid voltage in phase *k* and V_{Load} is rms of line-to-neutral load voltage. The magnitude of injected voltage is:

$$V'_{DVR,k} = \sqrt{2} \cdot \left| V_{load} - V'_{grid,k} \right| \text{ and } k = a, b, c \qquad \text{Eq. 1.3}$$

and the phase angle of injected voltage phasor is the same as phase angle of grid voltage phasor.

1.2.2. Pre-Sag Voltage Compensation Method

A commonly used method for compensating voltage sags is restoring the load voltage to the level and condition before the sag [6], [22]. Therefore, the amplitude and the phase of the voltage before the sag have to be exactly restored [6], [22]. The phasor diagram of the pre-sag compensation strategy is shown in Figure 1.3. In this figure, the dashed quantities (V'_{grid}, V'_{load}, V'_{dvr} and I'_{load}) indicate variables after the sag. The phasors prior to the sag are represented by V_{grid}, V_{load} and I_{load}. Moreover, angle of ϕ is phase angle difference between the load voltage and load current phasors and angle of δ is phase jump of grid voltage during the voltage sag. All of the load and grid voltage phasors are line-to-neutral voltages. For this strategy, the PLL is synchronized with the load voltage. As soon as a failure occurs, the PLL will be locked and so, the phase angle can be restored [1], [22].

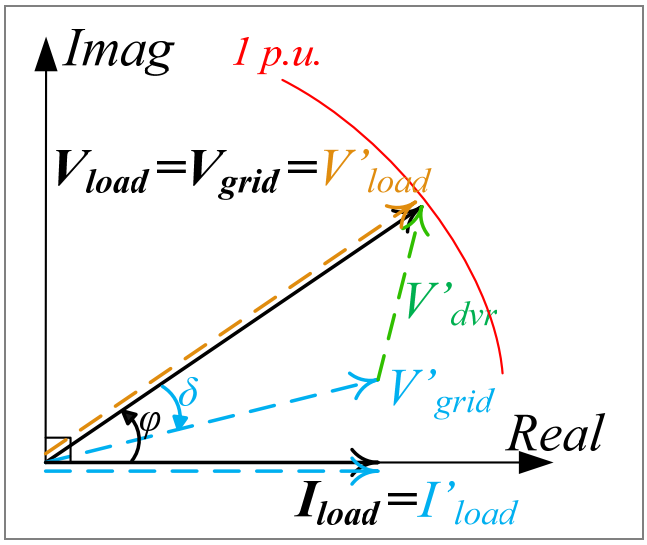

Figure 1.3. Phasor diagram of pre-sag compensation strategy.

The magnitude of DVR injected series voltage in this compensation method is not

minimal and it depends on both amount of voltage drop and phase jump during the voltage sag because the phase jump of the grid voltage has also to be compensated by the DVR. Consequently, DVR has to be designed for the highest possible voltage sag compensation. Furthermore, voltage rating of dc link in DVR controlled with this method needs to be larger than one controlled with in-phase compensation method. Moreover, this compensation strategy leads to the lowest distortions at the load-side because both phase angle and magnitude of the voltage at the load-side are restored during the sag. Thus, the sensitive load doesn't sense any voltage disturbance. This method is so reliable and proper to protect sensitive loads without having any possible transient and circulating currents. Moreover, even if the phase jumps of grid voltage in each phase are not the same, DVR controlled with pre-sag compensation method can eliminate the voltage disturbance completely. This strategy is able to compensate any kind of voltage sags including balanced or unbalanced voltage sags with or without any phase-variations in each phase of grid voltages.

Regarding the amount of power exchanged between DVR and power grid, pre-sag compensation method injects both active and reactive power depends on magnitude of injected voltage, grid voltage phase jump and phase angle difference between load voltage and load current phasors. The reason for injecting active power is that the injected voltage phasor is not certainly perpendicular to the load current phasor in this method as like as in-phase compensation method. Consequently, it needs the active power to be supplied at dc link side otherwise this method can't compensate deep voltage sags for a long time. Thus, without supporting the active power at the dc link, dc link voltage will drop during the

compensation and as a result, the maximum producible voltage of DVR will decrease and the modulation index of series converter will increase continuously and therefore, over-modulation may occur.

The power rating of DVR controlled by pre-sag compensation method is same as Eq. 1.1. The amount of active power exchanged between the DVR and power grid is as follows:

$$P_{DVR} = P_{load} - P_{grid} = \begin{bmatrix} 3 \cdot V_{load} \cdot I_{load} \cdot \cos(\phi) \\ - \sum_{k=a\,,\,b\,,\,c} \left[V'_{grid,k} \cdot I_{load} \cdot \cos\left(\phi - \delta_k\right) \right] \end{bmatrix} \quad \text{Eq. 1.4}$$

where, δ_k is the phase jump in phase *k*. The magnitude of injected voltage is:

$$V'_{DVR,k} = \sqrt{2} \cdot \sqrt{\left(V_{load}\right)^2 + \left(V'_{grid,k}\right)^2 - 2 \cdot V_{load} \cdot V'_{grid,k} \cdot \cos\left(\delta_k\right)} \quad \text{Eq. 1.5}$$

and the phase angle of injected voltage phasor is:

$$\angle V'_{DVR,k} = \arctan\left(\frac{V_{load} \cdot \sin\left(\varphi\right) - V'_{grid,k} \cdot \sin\left(\varphi - \delta_k\right)}{V_{load} \cdot \cos\left(\varphi\right) - V'_{grid,k} \cdot \cos\left(\varphi - \delta_k\right)} \right) \quad \text{Eq. 1.6}$$

1.2.3. Energy-Minimized Voltage Compensation Method

As mentioned and discussed in subsections 1.2.1 and 1.2.2, the in-phase and pre-sag compensation methods injects active power during compensation time. Thus, the active power should be supported at the dc link; otherwise, the dc link voltage will drop continuously. However, there is another compensation method called energy minimized compensation method to minimize any exchange of active power in compensation process.

The basic principle of this method is injecting to or absorbing from power grid as much reactive power as possible to compensate the voltage sag [1], [5], [22], [36], [37]. Therefore, the DVR voltage must be controlled in such a way that the DVR does not exchange active power with power grid and as a result, the amount of active power needed from the dc-link can be minimized. Compensating voltage sags with pure reactive power is possible as long as the voltage sag is quite shallow and satisfies the required condition (will be discussed later) and therefore, the compensation time is not limited.

Besides the significant advantage of not requiring active power, this strategy has in most cases two major disadvantages. First, a phase jump occurs when this method is applied as voltage sag compensation method; thus, it is not suitable for sensitive loads in which the voltage jump is a critical issue [1]. Even if there is not any phase jump in grid voltage during the voltage sag, this method causes a phase jump at load voltage to minimize the amount of active power exchanged between DVR and power grid. Second drawback of this method is that the amplitude of DVR injected voltage may become quite high in comparison with two previous methods explained in subsections 1.2.1 and 1.2.2. Thus, the voltage rating of dc link is higher than the case in which the DVR controlled by two previously mentioned methods. This compensation strategy is explained in detail for two cases of balanced and unbalanced voltage sags as following subsections.

1.2.3.1. Balanced voltage sag:

In this case, it is assumed that the phase jump and amplitude drop of grid voltage in all three phases during the voltage sag are equal. The voltage phasors for the energy minimized compensation strategy in the balanced voltage sag are depicted in Figure 1.4 in

which α is the phase variation of load voltage after compensation. As shown in Figure 1.4, the phasor of DVR series injected voltage is perpendicular to the load current phasor to avoid exchanging the active power between DVR and power grid. In Figure 1.4, the dashed quantities (V'_{grid}, V'_{load}, V'_{dvr} and I'_{load}) indicate variables after the sag. The phasors prior to the sag are represented by V_{grid}, V_{load} and I_{load}. All of the load and grid voltage phasors are line-to-neutral voltages.

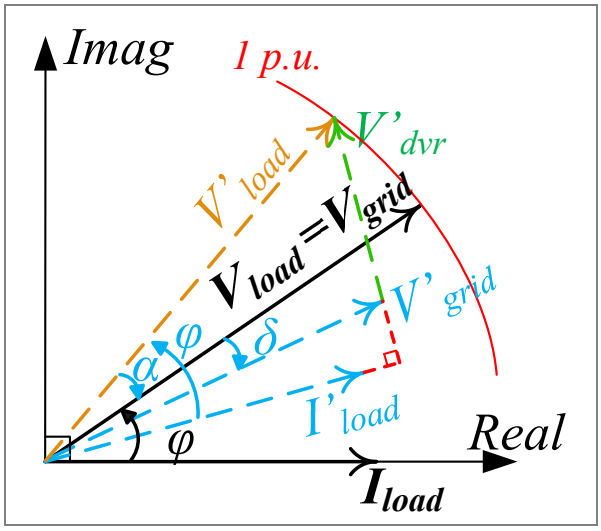

Figure 1.4. Phasor diagram of energy minimized compensation strategy for balanced voltage sag.

In Figure 1.4, the angle of α is unknown which is calculated by making the required active power of DVR equals to zero as follows:

$$P_{DVR} = P_{load} - P_{grid} = 0 \qquad \text{Eq. 1.7}$$

$$P_{load} = 3 \cdot V_{load} \cdot I_{load} \cdot \cos(\phi) \qquad \text{Eq. 1.8}$$

$$P_{grid} = 3 \cdot V'_{grid} \cdot I_{load} \cdot \cos(\phi - \alpha - \delta) \quad \text{Eq. 1.9}$$

where, P_{grid}, P_{load} and P_{DVR} are the supplied active power by power grid, required active power of load and the exchanged active power of DVR, respectively. By substituting Eq. 1.8 and Eq. 1.9 into Eq. 1.7, it can be written as follows:

$$\alpha = \phi - \delta - \cos^{-1}\left(\frac{V_{load} \cdot \cos(\phi)}{V'_{grid}}\right) \quad \text{Eq. 1.10}$$

According to above equation, following condition must be satisfied:

$$V_{load} \cdot \cos(\phi) \leq V'_{grid} \quad \text{Eq. 1.11}$$

Otherwise, the angle of α should be obtained from Eq. 1.12 and in this condition, the amount of active power exchanged between DVR and power grid can't be zero.

$$\frac{d}{d\alpha}(P_{DVR}) = 0 \quad \text{Eq. 1.12}$$

which results in:

$$\sin(\varphi - \delta - \alpha) = 0 \quad \text{Eq. 1.13}$$

and:

$$\alpha = \varphi - \delta \quad \text{Eq. 1.14}$$

The magnitude of DVR series injected voltage can be calculated as follows:

$$V_{DVR} = \sqrt{2} \cdot \sqrt{\left(V_{load}\right)^2 + \left(V'_{grid}\right)^2 - 2 \cdot V_{load} \cdot V'_{grid} \cdot \cos\left(\delta + \alpha\right)} \qquad \text{Eq. 1.15}$$

If Eq. 1.11 is satisfied, the phase angle of DVR series injected voltage phasor is:

$$\angle V'_{DVR} = \alpha + \frac{\pi}{2} \qquad \text{Eq. 1.16}$$

otherwise:

$$\angle V'_{DVR} = \arctan\left(\frac{V_{load} \cdot \sin\left(\varphi + \alpha\right) - V'_{grid} \cdot \sin\left(\varphi - \delta\right)}{V_{load} \cdot \cos\left(\varphi + \alpha\right) - V'_{grid} \cdot \cos\left(\varphi - \delta\right)}\right) \qquad \text{Eq. 1.17}$$

As explained, the Eq. 1.11 should be satisfied to avoid exchanging active power between DVR and power grid. It means that exchanging active power is not avoidable for all conditions. Figure 1.5 shows the conditions in which avoiding active power exchange is possible (illustrated with light gray color) or impossible (illustrated with purple color).

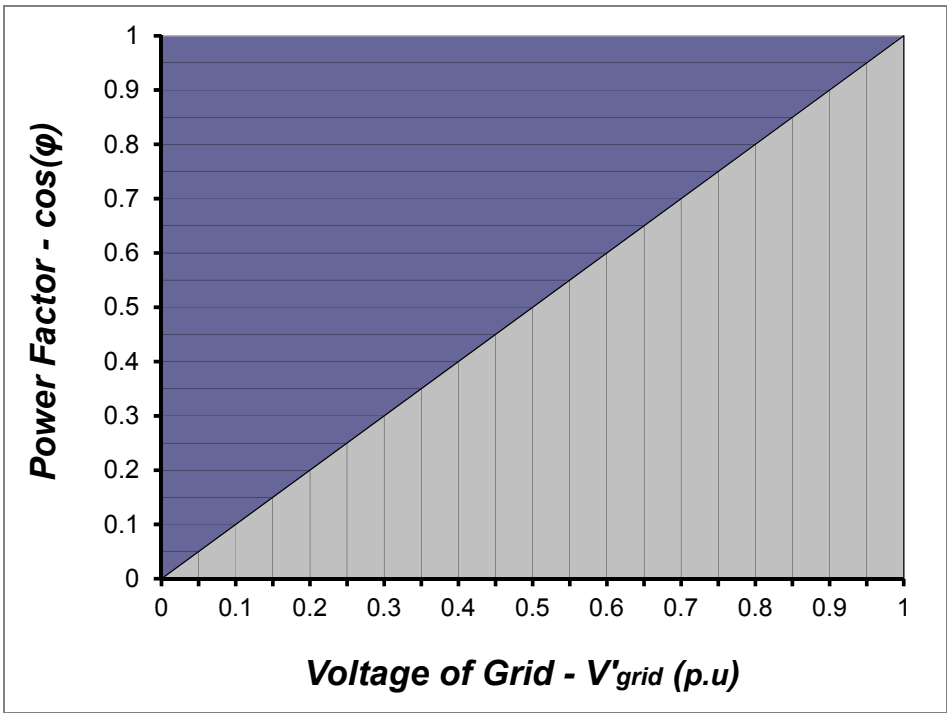

Figure 1.5. Possibility (illustrated with gray color) and impossibility (illustrated with purple color) of avoiding active power exchanged between DVR and power grid during the balanced voltage sag.

As shown in Figure 1.5, the power factor of load should be less than grid voltage (in p.u.) to avoid active power exchange. For example, if the grid voltage drops to 0.7 p.u., the power factor should be less than 0.7 to avoid exchanging active power between DVR and power grid. However, this is not likely in industry because industries prefer to increase power factor from financial point of view by using shunt switching capacitor bank or reactive power compensator. Thus, in most cases of deep voltage sag, energy minimized compensation method is not able to avoid active power exchange completely but it can minimize it. To suppress this drawback, a solution has been presented in [36] to decrease the power factor intentionally during the voltage sag by connecting a thyristor-switched inductor in parallel with load as shown in Figure 1.6. In this configuration, the thyristor switch turns on during the voltage sag to connect the inductor parallel with load to lower

the power factor and make it possible to compensate voltage sag without exchanging active power between DVR and power grid. However, drawback of this solution is high-power low-frequency inductor which can be a bulky and costly.

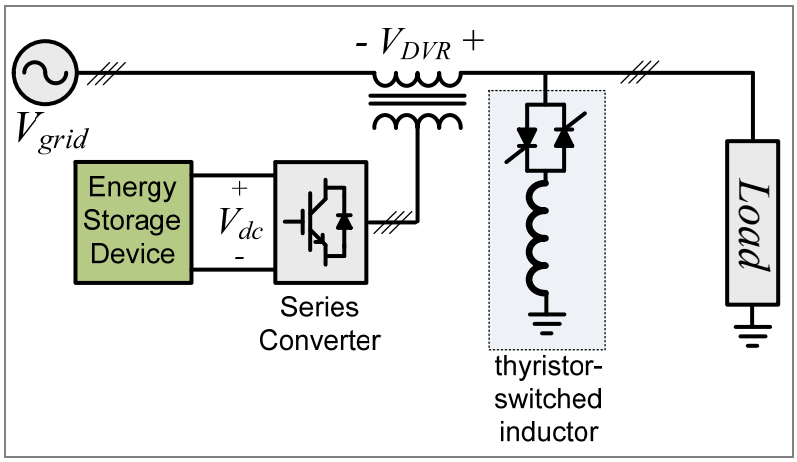

Figure 1.6. Schematic of DVR with shunt thyristor-switched inductor to lower the power factor intentionally during the voltage sag.

1.2.3.2. Unbalanced voltage sag:

In this case which is more common than previous one discussed in subsection 1.2.3.1, it is assumed that the variations of voltage phase angle and amplitude in all three phases are not the same. The voltage phasors for the energy minimized strategy in the unbalanced voltage sag are shown in Figure 1.7 just for one phase. In this method, the phasor of DVR series injected voltage is not perpendicular to the load current phasor. Thus, the amount of active power exchanged between DVR and power grid in each phase is not zero. But the reference signal for series injected voltage can be determined in such a way that total exchanged active power in all three phases becomes zero. It means that, for example, the exchanged active power in one phase is positive and in other two phases is negative but the total exchanged active power is zero.

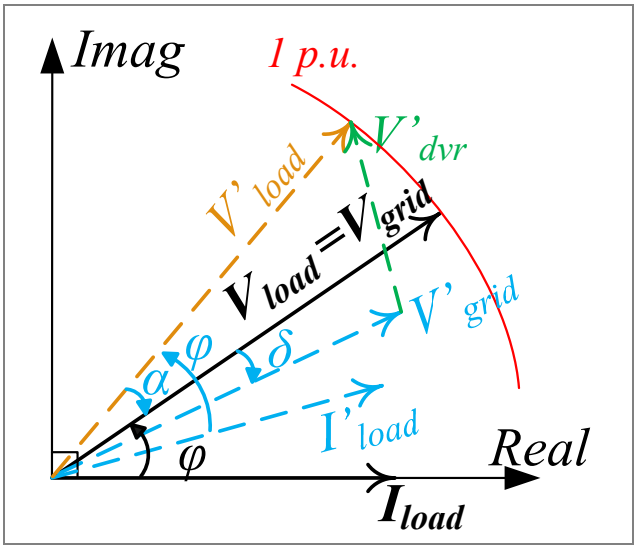

Figure 1.7. Phasor diagram of energy minimized compensation strategy for unbalanced voltage sag.

This compensation method either minimizes or avoids the requirement of supporting active power in dc link depending on load power factor and amount of voltage drop. It is worth mentioning that all three power converters in each phase should have common dc link capacitor to add the exchanged active power of each phase together and as a result, make the total exchanged active power equal to zero. Otherwise, if there is not common dc link for all three power converters of each phase, it is not possible to minimize/avoid the required active power as well as to compensate the unbalanced voltage sag and make the load voltage balanced.

As shown in Figure 1.7, the angle of α is unknown and should be calculated in such a way that the total exchanged active power in all three phases becomes zero. Thus, it can be written as follows:

$$P_{DVR} = P_{load} - P_{grid} = 0 \qquad \text{Eq. 1.18}$$

$$P_{load} = 3 \cdot V_{load} \cdot I_{load} \cdot \cos(\phi) \quad \text{Eq. 1.19}$$

$$P_{grid} = \sum_{k=a\,,\,b\,,\,c} \left[V'_{grid,k} \cdot I_{load} \cdot \cos\left(\phi - \alpha - \delta_k\right) \right] \quad \text{Eq. 1.20}$$

By substituting Eq. 1.20 and Eq. 1.19 into Eq. 1.18, it can be written as follows:

$$\alpha = \phi - \lambda - \cos^{-1}\left(\frac{3 \cdot V_{load} \cdot \cos(\phi)}{\sqrt{X^2 + Y^2}} \right) \quad \text{Eq. 1.21}$$

where,

$$X = \sum_{k=a\,,\,b\,,\,c} \left[V'_{grid,k} \cdot \cos\left(\delta_k\right) \right] \quad \text{Eq. 1.22}$$

$$Y = \sum_{k=a\,,\,b\,,\,c} \left[V'_{grid,k} \cdot \sin\left(\delta_k\right) \right] \quad \text{Eq. 1.23}$$

$$\lambda = \tan^{-1}\left(\frac{Y}{X} \right) \quad \text{Eq. 1.24}$$

According to Eq. 1.21, Eq. 1.25 must be satisfied; otherwise, the angle of α should be obtained from Eq. 1.26 and in this condition, the required active power of DVR can be minimized rather than be zero.

$$3 \cdot V_{load} \cdot \cos(\phi) \leq \sqrt{X^2 + Y^2} \quad \text{Eq. 1.25}$$

$$\frac{d}{d\alpha}\left(P_{DVR}\right) = 0 \quad \text{Eq. 1.26}$$

which results as:

$$\frac{d}{d\alpha}\left(P_{grid}\right)=0 \qquad \text{Eq. 1.27}$$

$$\sum_{k=a\ ,\ b\ ,\ c}\left[V'_{grid,k}\cdot\sin\left(\phi-\alpha-\delta_k\right)\right]=0 \qquad \text{Eq. 1.28}$$

and, it can be pointed out:

$$\alpha=\varphi-\lambda \qquad \text{Eq. 1.29}$$

The magnitude of DVR series injected voltage in each phase can be calculated as follows:

$$V'_{DVR,k}=\sqrt{2}\times\sqrt{\left(V_{load}\right)^2+\left(V'_{grid,k}\right)^2-2\cdot V_{load}\cdot V'_{grid,k}\cdot\cos\left(\delta_k+\alpha\right)} \qquad \text{Eq. 1.30}$$

and, the phase angle of DVR series injected voltage phasor in each phase is:

$$\angle V'_{DVR,k}=\arctan\left(\frac{V_{load}\cdot\sin\left(\varphi+\alpha\right)-V'_{grid,k}\cdot\sin\left(\varphi-\delta_k\right)}{V_{load}\cdot\cos\left(\varphi+\alpha\right)-V'_{grid,k}\cdot\cos\left(\varphi-\delta_k\right)}\right) \qquad \text{Eq. 1.31}$$

As like as balanced voltage sag, compensation of deep unbalanced voltage sag with higher power factor without requiring the active power is impossible. Thus, using thyristor-switched inductor, as shown in Figure 1.6, during the voltage sag to lower the power factor can make it possible to compensate deep unbalanced voltage sag without any active power.

1.2.4. Hybrid Voltage Compensation Method

As discussed in subsections 1.2.1 to 1.2.3, each compensation method has its own advantages and disadvantages. From advantages point of view, the magnitude of injected voltage is minimal in the in-phase compensation method and the amount of active power exchanged between DVR and power grid is minimal in the energy minimized compensation method. About the pre-sag compensation method, it minimizes the amount of distortion at the load side and can compensate both voltage drop and phase jump. From disadvantages point of view, the in-phase compensation method can't compensate the unbalanced voltage sag completely if the phase variations in all three phases are not the same; it means that although the magnitude of load voltage can be restored but the phase angle of load voltages may remain unbalanced. The energy minimized compensation method can't avoid phase jump at the load voltage and the magnitude of injected voltage is quite high. About the pre-sag compensation method, it needs active power during the voltage sag which requires supporting active power at dc link or using ultra capacitor or battery at the dc link. However, it can be beneficial to combine methods with each other and use their collective advantages. It has been presented in [38], [39] to combine the in-phase compensation method and pre-sag compensation method. Thus, it makes it possible to have minimum distortion at load voltage due to the pre-sag compensation method and to have minimum voltage amplitude due to in-phase compensation method. The procedure of method proposed in [38], [39] is as follows. When the voltage sag is detected, DVR controlled by pre-sag compensation method injects the series voltage to restore both magnitude and phase angle of load voltage and thus, the load doesn't sense any distortion.

This method requires the active power which requires use the stored energy of dc link capacitor, discharge it and decrease the dc link voltage continuously. This issue results in increase of the modulation index of power converter. After a while, depends on voltage sag depth and phase jump, the modulation index reaches to a pre-determined value. At this time, the PLL which was locked to pre-sag condition is unblocked and starts to be synchronized with power grid voltage. The synchronization process and changing the compensation method from pre-sag to in-phase is accomplished in several cycles to avoid any sudden phase jump at load voltage. Therefore, due to controlling DVR with in-phase compensation method, the magnitude of required injected voltage reduces and dc link capacitor can be discharged even more.

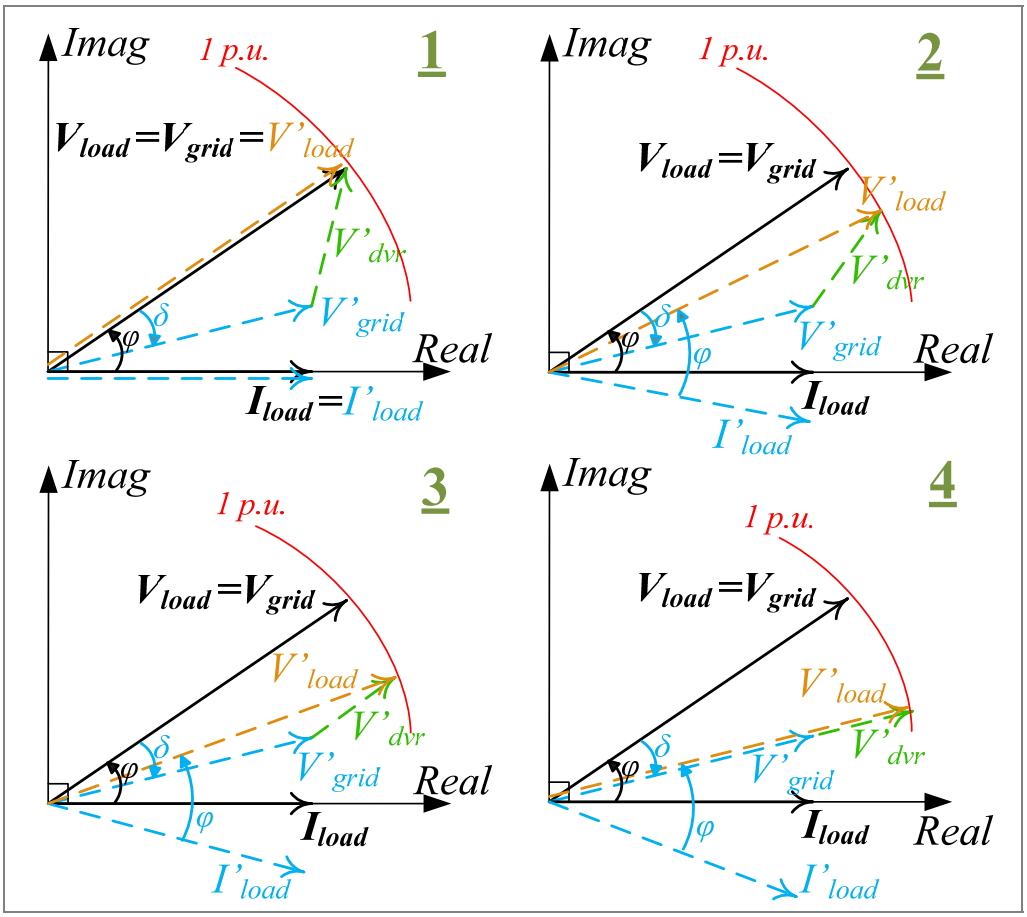

Figure 1.8. Phasor diagram showing the procedure of hybrid voltage compensation method.

Figure 1.8 shows the explained procedure in 4 steps. Although this hybrid method has advantages of pre-sag and in-phase methods simultaneously, it still has disadvantage of in-phase compensation method. It means that if the phase variations of all three phases are not the same, the hybrid method can't restore the phase jump at load voltage. The reason is that after changing the compensation method from pre-sag to in-phase, DVR can't compensate phase jumps at each phase individually. On the other hand, the procedure which should be applied when the voltage sag is cleared has not been discussed in [38], [39] and it can be a drawback for the hybrid compensation method. Moreover, it has not been discussed how the hybrid method works if the voltage sag is cleared during the

transition from pre-sag method to in-phase method. Because, in real cases, it is unknown how long the voltage sag takes and when it will be cleared after starting. Table 1.1 illustrates the comparison between four mentioned methods to summarize the advantages and disadvantages.

TABLE 1.1

COMPARISON OF IN-PHASE, PRE-SAG, ENERGY-MINIMIZED AND HYBRID COMPENSATION METHODS.

Method	Advantage	Disadvantage
In-Phase	1) The magnitude of the injected voltage is minimal. 2) The voltage rating of the dc link and DVR is minimal.	1) It needs active power during compensation. 2) It can't restore the phase jump if the variations of phase jump in three phases are asymmetric.
Pre-Sag	1) It restores both the voltage drop and the phase jump. Thus, the sensitive load doesn't sense any distortion. 2) It avoids any circulating or transient current at load side. 3) It can compensate any kind of voltage sag regardless of unbalanced voltage drop or unbalanced phase jump.	1) It needs active power during compensation.
Energy Minimized	1) The amount of exchanged active power between DVR and power grid is minimal. 2) It may not require active power during compensation.	1) The magnitude of injected voltage is almost high. 2) The voltage rating of dc link and DVR is almost high. 3) For a load with high power factor, compensation of deep voltage sag requires active power. 4) It causes phase jump at load voltage even if there is not any phase jump in gird voltage during voltage sag.
Hybrid (in-phase pre-sag)	1) It restores both voltage drop and phase jump just at the beginning. 2) It avoids any circulating or transient current at load side just at the beginning.	1) It needs active power during compensation. 2) It can't restore the phase jump if the variations of phase jump in three phases are asymmetric.

1.3. Review of Configurations to Support Active Power at DVR DC Link

Several configurations have been presented in literature to support active power at DVR dc link. This section discusses about the different configurations and their pros and cons.

1.3.1. Capacitor Supported DVR

Figure 1.9 shows a schematic of a capacitor-supported DVR connected via a line-frequency transformer in series with power grid and critical load [5], [17], [27], [36], [40]–[43]. In [18], the super capacitor has been used at dc link to increase the amount of stored active power to be able to compensate the long-duration voltage sag. In this configuration, the required active power needs to be provided by capacitor since there is not any energy storage which results in decreasing the capacitor terminal voltage. Decrease of dc link capacitor voltage leads to increase of the modulation index of series converter and therefore, over-modulation may occur causing undesirable harmonics at the output voltage of power converter. Consequently, there is a minimum dc voltage below which the inverter of the DVR cannot generate the required voltage. Thus, the size of the dc capacitor needed to supply active power can be expressed as Eq. 1.32 in terms of maximum allowable dc-link voltage ($V_{DC,max}$), minimum allowable dc-link voltage ($V_{DC,min}$), sag duration (T_{sag}), DVR injected active power (P_{inj}) and power loss (P_{loss}). According to Eq. 1.32, it is clear that large capacitors in the dc-link energy storage are needed to effectively mitigate long-duration and deep voltage sags.

$$C_{dc} = \frac{2 \cdot \left(P_{inj} + P_{loss} \right) \cdot T_{sag}}{\left(V_{DC,\max}^2 - V_{DC,\min}^2 \right)} \qquad \text{Eq. 1.32}$$

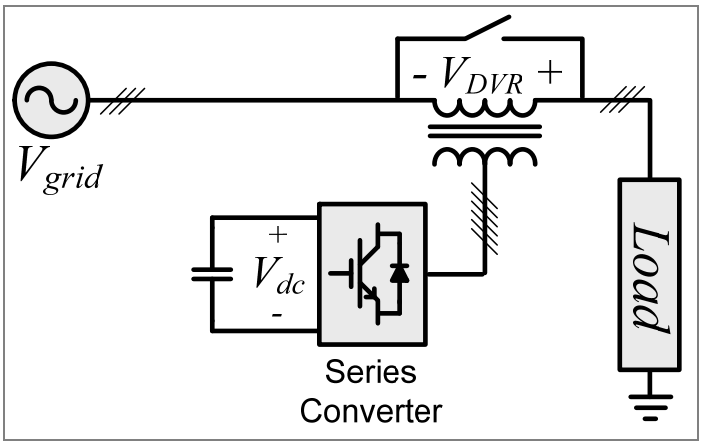

Figure 1.9. Schematic of the capacitor supported DVR.

In order to reduce the size of the dc link capacitor, it is better to utilize the energy-minimized strategy as a control method of DVR which is explained in detail in Section 1.2.3. Otherwise, the voltage of dc link capacitor drops very quickly during the compensation and as a result, the maximum producible voltage of DVR decreases. It is worth mentioning that if the energy-minimized strategy is applied to DVR, the common dc link capacitor should be used and shared between all three phases. Because in the energy-minimized strategy, one or two phases of DVR absorb the active power from grid and remaining phase(s) inject(s) the active power to grid in unbalanced voltage sags to minimize the overall amount of required active power by DVR. Therefore, common dc link capacitor is essential to make the circulation of active power between phases possible. According to [44]–[47], unbalanced voltage sags are statistically over 90% of voltage sags in power grid. In balanced voltage sag, the implementation of energy-minimized strategy

in capacitor supported DVR is pretty straightforward since the injected voltages in all three phases need to be perpendicular to load currents which are the same as the grid current. However, the implementation of energy-minimized strategy in capacitor supported DVR requires pretty higher voltage in comparison to other compensation methods since the amplitude of required injected voltage is pretty high as shown in Figure 1.4.

In [2], [48], [49], a concept of interline DVR (IDVR) in which a capacitor at dc link is shared between several DVRs connected between different distribution lines/feeders has been presented. An example of IDVR with two DVRs is shown in Figure 1.10. In this configuration, whenever one of the DVRs compensates the voltage sag in the relevant feeder, other DVR(s) provide(s) the required active power to regulate the common dc link at the reference value. However, there is always a limitation in absorbing energy from a healthy feeder in an IDVR. The DVRs at healthy lines where there are not any voltage sags need to inject such a voltage to keep the amplitude of load voltage at the nominal value as well as to absorb the active power to regulate the common dc link. This is only possible if the injected voltages in healthy lines are not in-phase with grid voltages. This means that the loads will notice the phase jump which may not be acceptable for some sensitive loads. The amount of active power supplied by the healthy feeder(s) has certain limitations due to the operational characteristics of these feeder(s). On the other hand, the amount of energy required for compensation (in the faulty feeder) is not constant and depends on other parameters, such as the phase and magnitude of injected voltage. The principle of the IDVR is the same as the interline power-flow controller (IPFC) which addresses the power flow control in the number of transmission lines. The application of this scheme can be in

an industrial park where different loads are electrically, not physically, far apart from each other which means that the loads are fed from different feeders connected to different grid substations, perhaps at different voltage levels. In [32], [48], [49], the control method of DVRs at healthy lines in IDVR configuration are discussed when either pre-sag or energy-minimized compensation method is used for DVR which compensates the voltage sag in faulty line. In [32], however, it has been shown that DVRs in healthy lines cannot always regulate the common dc link properly by providing all required active power consumed with DVR compensating the voltage sag in faulty line and it depends on voltage sag depth and loads power factors. In [50], the limitations of IDVR regarding the exchanged active power are discussed and compensation range of IDVR is compared with two separate capacitor-supported DVRs. It has been illustrated that the compensating range of IDVR is larger than that of separate DVRs with similar ratings (The voltage rating of each DVR is assumed to be the same in both structures of separate DVR and IDVR). This means that for the same range of compensation, the IDVR has the converters with lower power rating rather than DVR. Moreover, the compensation range in the IDVR structure increases when the rating of the healthy feeder is higher than that of the faulty feeder.

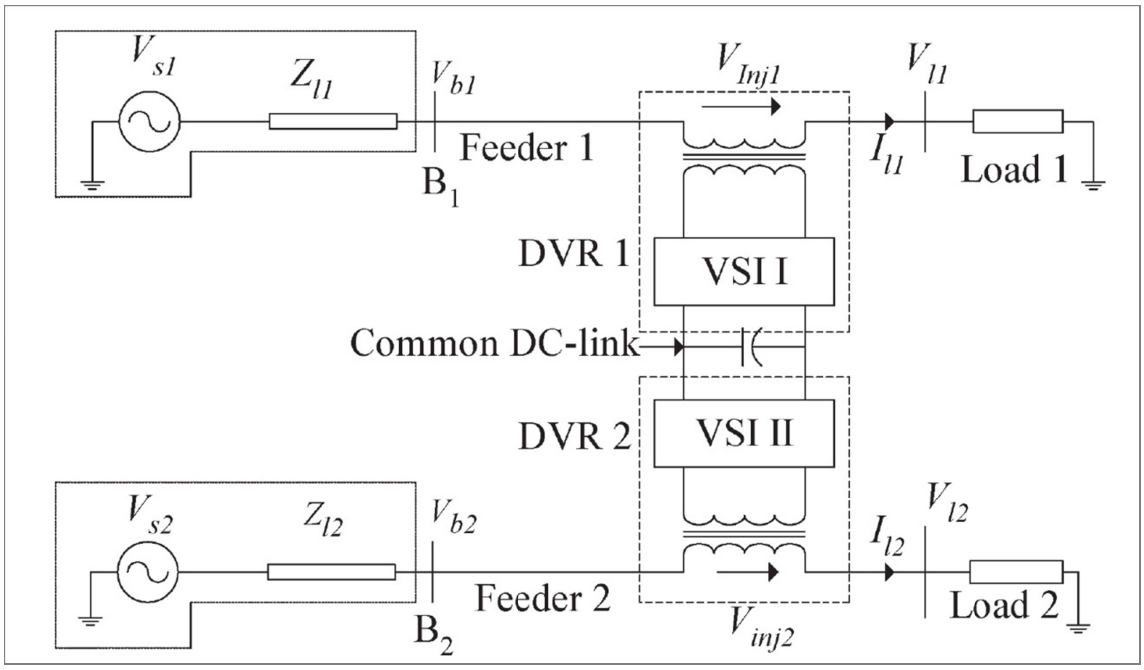

Figure 1.10. Schematic of the interline DVR presented in [32], [48], [50].

1.3.2. Battery Supported DVR

In [51]–[62], battery supported configuration of DVR is presented and discussed in which the battery is connected to dc link to provide the active power required by DVR to compensate the voltage sag. The schematic of battery supported DVR is shown in Figure 1.9 while the battery is connected at dc link. DC capacitors are connected in parallel with the batteries to act as a filter to cancel out the switching ripple. Otherwise, it can cause to overheat the battery and reduce its life-time [56]. In [52], the lead-acid battery is modeled for battery supported DVR application and two short-term and long-term models are presented to predict the terminal voltage, state of charge, battery capacity and good description of the battery response during both discharge and charge modes. The short-term and long-term models are used during the voltage sag compensation and the self-charging mode, respectively.

In the battery supported DVR, the battery can be charged either with external converter or DVR's converter itself [56], [57]. Second option in which the self-charging control is required to be considered is more suitable since no extra converter is required. In the self-charging mode when no disturbance exists in the line, DVR can inject such voltage to absorb active power from the power supply to recharge the batteries and provide the reactive power to maintain the load voltage at 1 p.u. As shown in Figure 1.11 depicting the self-charging mode, there is a charging angle α between the load voltage phasor and the grid voltage phasor. This means that the self-charging mode of battery supported DVR causes the phase jump at load voltage which can be a problematic for some sensitive loads. Therefore, the charging angle α should gradually increase to target value at beginning of self-charging process and gradually decrease to zero at the end of process to avoid any sudden phase jump at the load voltage.

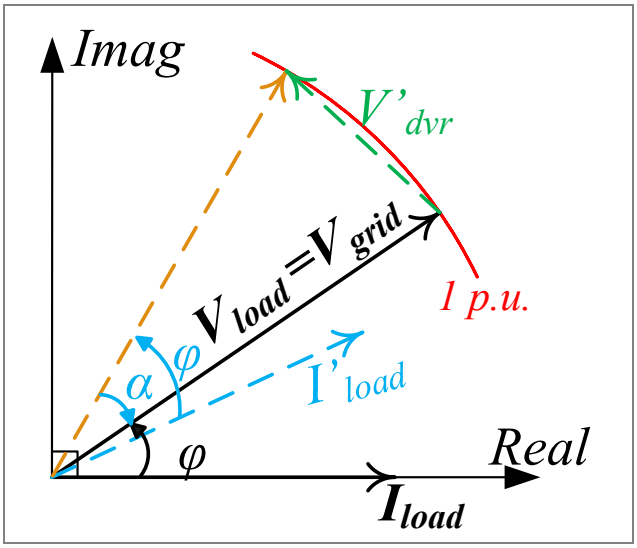

Figure 1.11. Phasor diagram of the self-charging mode in battery supported DVR.

The amount of active power exchanged between the DVR and power grid, which is

provided to recharge the battery, is as follows:

$$P_{DVR} = P_{load} - P_{grid} = 3 \cdot V_{load} \cdot I_{load} \cdot \cos(\phi) - 3 \cdot V_{grid} \cdot I_{load} \cdot \cos(\phi - \alpha) \quad \text{Eq. 1.33}$$

$$Q_{DVR} = Q_{load} - Q_{grid} = 3 \cdot V_{load} \cdot I_{load} \cdot \sin(\phi) - 3 \cdot V_{grid} \cdot I_{load} \cdot \sin(\phi - \alpha) \quad \text{Eq. 1.34}$$

where, V_{load} and V_{grid} are both 1 p.u.. The magnitude of injected voltage is:

$$V'_{DVR} = \sqrt{2} \cdot \sqrt{(V_{load})^2 + (V_{grid})^2 - 2 \cdot V_{load} \cdot V_{grid} \cdot \cos(\alpha)} \quad \text{Eq. 1.35}$$

and the phase angle of injected voltage phasor is:

$$\angle V'_{DVR,k} = \arctan\left(\frac{\sin(\varphi + \alpha) - \sin(\varphi)}{\cos(\varphi + \alpha) - \cos(\varphi)}\right) \quad \text{Eq. 1.36}$$

The amount of load power factor and charging angle α are determining factors on the recharging process (V_{grid} and V_{load} are 1 p.u.) of battery as shown in Figure 1.12 and Figure 1.13. In Figure 1.14, the peak voltage of battery supported DVR working in self-charging mode is illustrated.

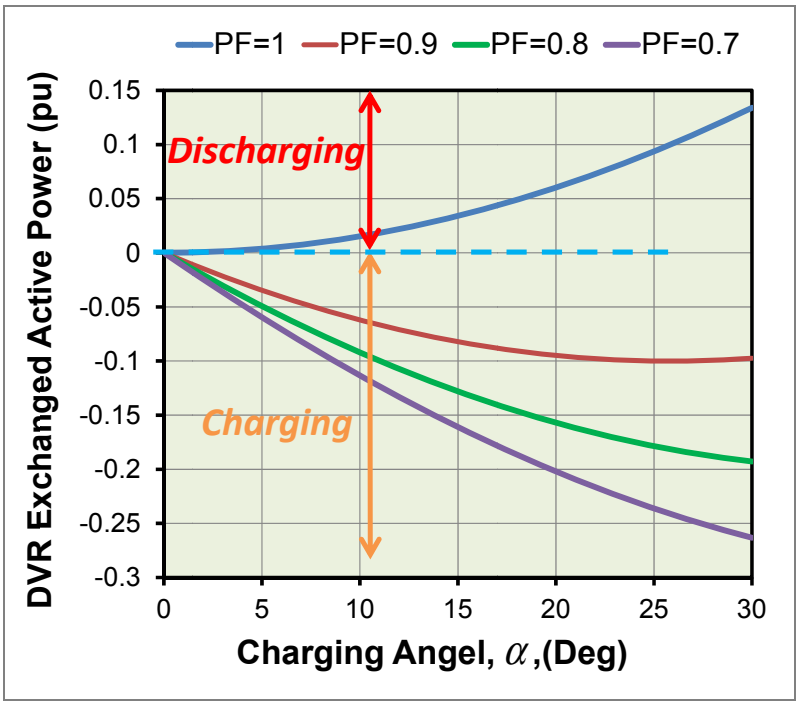

Figure 1.12. Exchanged active power of battery supported DVR in self-charging mode.

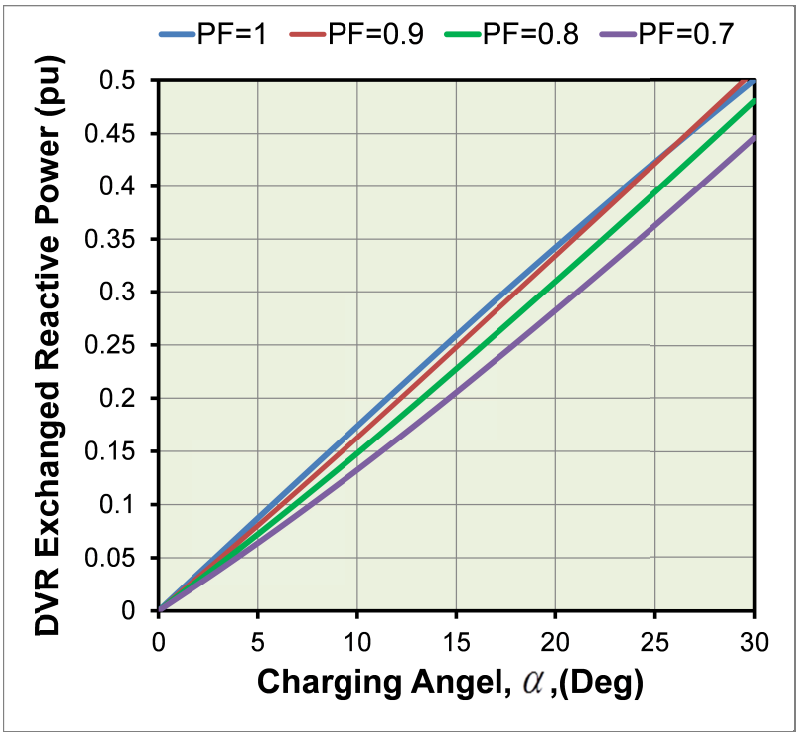

Figure 1.13. Exchanged reactive power of battery supported DVR in self-charging mode.

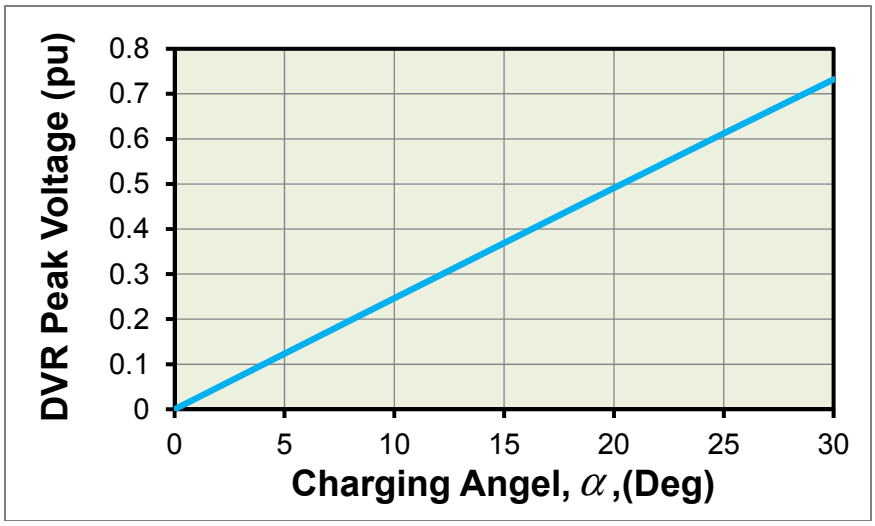

Figure 1.14. Peak voltage of battery supported DVR in self-charging mode.

1.3.3. Diode Rectifier or Shunt Converter Based DVR

A traditional DVR mainly consists of series and shunt converters connected back-to-back and a common dc capacitor used as an energy-storage element [63]–[67]. The shunt converter can also be implemented as shunt three-phase diode rectifier. Figure 1.15 shows two different types of DVR configurations. Each consists of a set of shunt and series converters connected back-to-back and a common dc capacitor. The series converter consists of a three-phase voltage-source converter or three single-phase voltage-source converters. It depends on whether or not it is required to compensate zero sequence voltage during unbalanced earth faults. DVR starts to inject compensating voltages in series into the power grid as soon as voltage sag occurs. It is noted that in Figure 1.15(a), the shunt rectifier/converter is installed at the source-side [63]–[66], whereas in Figure 1.15(b), it is installed at the load-side [10], [67], [68]. In both systems, the shunt rectifier/converter charges the dc capacitor in normal conditions. There exists a significant operational difference between the shunt rectifier/converter in Figure 1.15(a) and (b) during the

occurrence of voltage sags. Suppose a voltage drop occurs at the source-side or at the ac terminals of the shunt rectifier/converter. In Figure 1.15(a), the shunt rectifier/converter loses its rectification capability when the maximum source voltage becomes lower than the dc-link voltage. Therefore, the series rectifier/converter requires a large dc capacitor as an energy-storage element intended for feeding electric dc power to it. On the other hand, in Figure 1.15(b), no voltage drop appears at the load-side or at the ac terminals of the shunt rectifier/converter when a voltage drop occurs at the source-side, because the series converter compensates the voltage sag. This makes it possible to keep the shunt rectifier/converter active in regulating the dc link voltage, even for long-duration voltage sags. In this case, the active power required for voltage-sag compensation is injected from the shunt rectifier/converter to the series converter. In other words, the dc capacitor does not play any role in feeding active power, required for compensation, to the series converter. This system configuration allows the use of small dc capacitor intended for smoothing the common dc-link voltage. Thus, the DVR in Figure 1.15(b) can operate properly independent of duration (long or short) of voltage sags.

In [69]–[71], a DVR based on square waveform injection is presented to protect the sensitive loads. This configuration, shown in Figure 1.16, contains a line-frequency transformer at grid side and at its secondary winding, a full-bridge diode rectifier is used to build a dc link. As the next stage, a full-bridge inverter working at line-frequency injects square-wave series voltage to shift up/down the gird voltage and protect the sensitive load from the voltage sag/swell. This configuration results in elimination of LC filter at the output of inverter as well as switching loss. However, this configuration cannot control the

amount of series injected voltage since the inverter injects exactly the dc link voltage without modulating it.

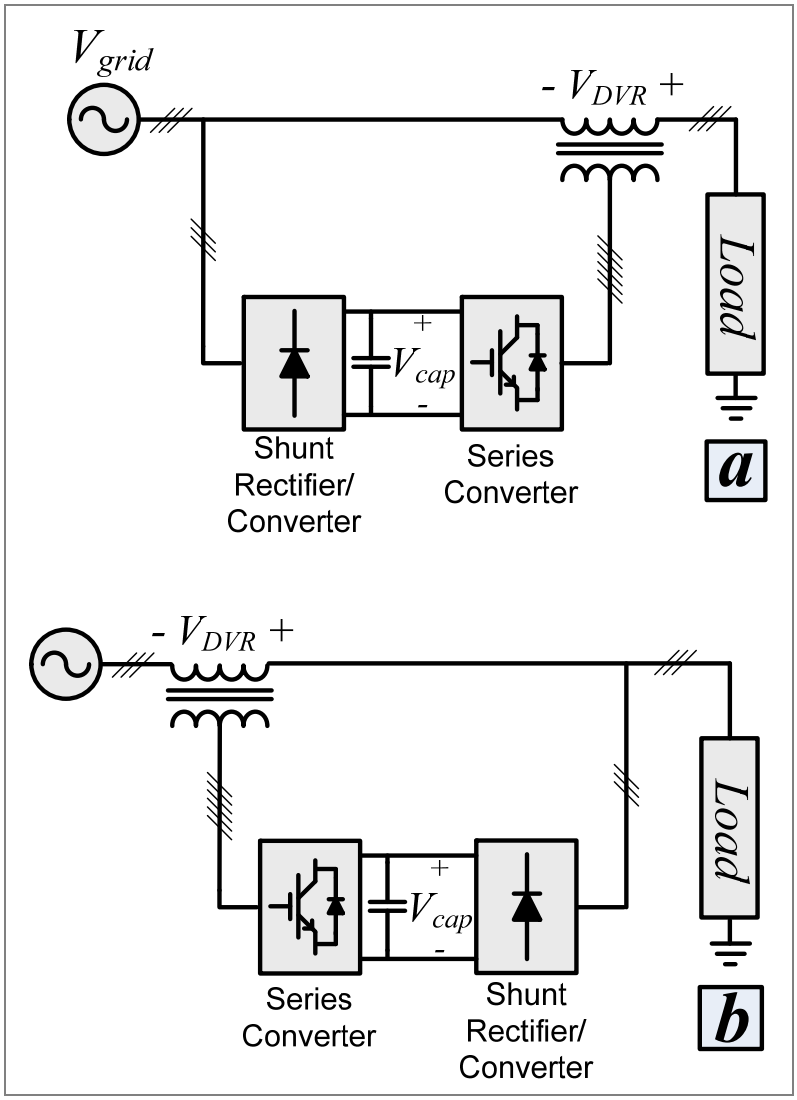

Figure 1.15. DVR configuration with series isolation transformer and shunt rectifier/converter at the: (a) source-side; (b) load-side.

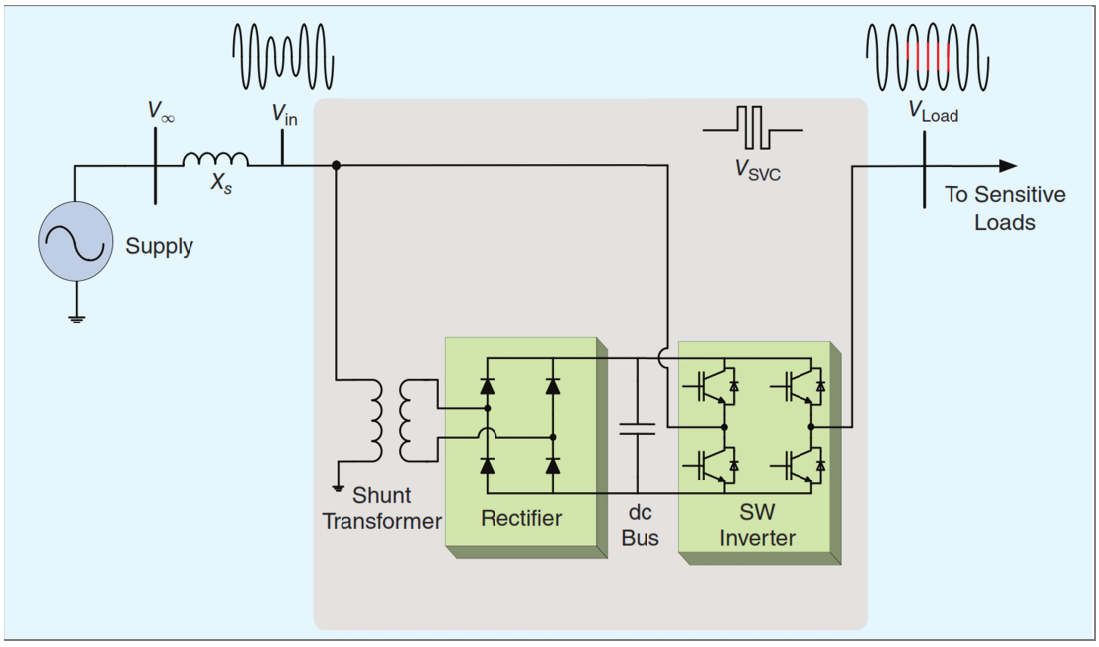

Figure 1.16. DVR based on the square-wave injection presented in [69]–[71].

1.4. Effect of Upstream Step-Down Transformer

The knowledge of the distribution transformer winding is important as this determines whether or not there is a need for zero sequence voltage compensation during unbalanced earth faults; thus, this affects the choice of DVR inverter configuration together with the injection transformer winding [51]. The vector diagram of voltages under faulty conditions for △/Y and △/△ connection of the step-down distribution transformer is shown in Figure 1.17. The black straight-line vectors represent the voltages for normal operating conditions and blue dashed-line vectors represent the voltages for short-circuit operating conditions.

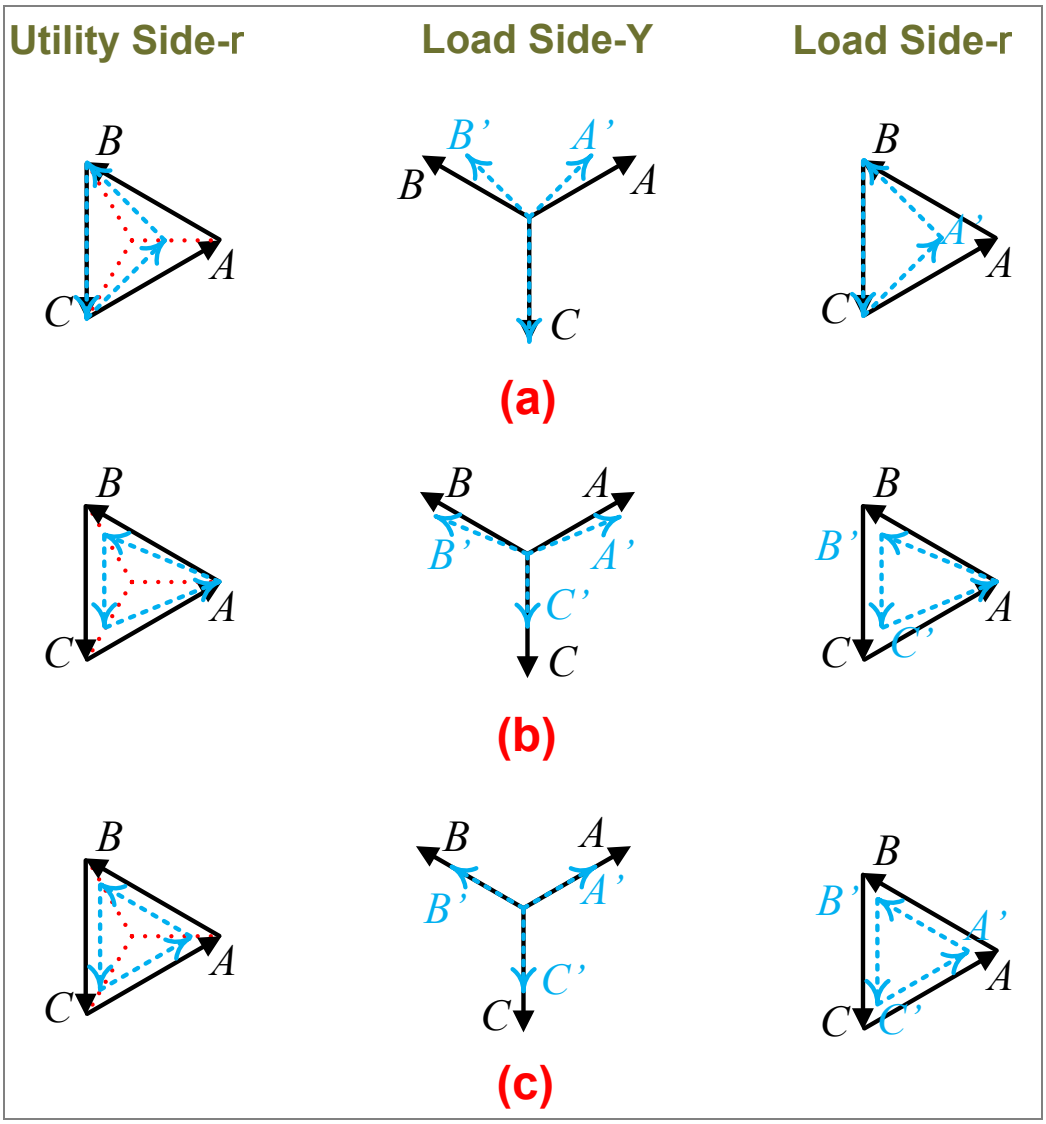

Figure 1.17. The vector diagram of a faulted distribution system (partial voltage collapse): (a) Single line to ground fault; (b) Double line to ground fault; (c) Three lines to ground fault.

1.5. DVR Reference Voltage Determination:

The control system of DVR has two main parts; the first one is the voltage sag detection part which will be explained and investigated in more detail in Chapter 2 of this thesis. The second part of DVR control system is determining the reference of DVR series injected voltage. The approach to determine reference signal of DVR series injected voltage is based on the type of energy storage device and its ability to support active power. As explained in Section 1.2.2, one of the methods for compensating voltage sags is restoring the load voltage to the level and condition before the sag, called pre-sag method [6], [22]. Therefore, the amplitude and the phase angle of the voltage before the sag have to be exactly restored. For this strategy, the PLL is synchronized with the grid voltage and its phase angle is backed up and stored in memory continuously. As soon as a voltage sag is detected, the PLL will be locked to the phase angle stored in the memory and so, the phase angle can be restored [6], [22]. The magnitude of DVR injected series voltage in the pre-sag compensation method depends on both amount of voltage drop and phase jump during the voltage sag; because the phase jump of the grid voltage has also to be compensated by the DVR. In the synchronous reference frame (SRF)-based method, the first step of determining the reference of DVR series injected voltage is to measure the line-to-neutral grid voltages and transfer them from *abc* coordinate system to SRF as follows:

$$\begin{bmatrix} V_{grid,d} \\ V_{grid,q} \\ V_{grid,0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - 120) & \cos(\omega t + 120) \\ \sin(\omega t) & \sin(\omega t - 120) & \sin(\omega t + 120) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} V_{grid,a} \\ V_{grid,b} \\ V_{grid,c} \end{bmatrix} \quad \text{Eq. 1.37}$$

where, $V_{grid,a}$, $V_{grid,b}$, $V_{grid,c}$ are the measured line-to-neutral grid voltages of phases *a*, *b* and *c*, respectively and $V_{grid,d}$, $V_{grid,q}$, $V_{grid,0}$ are the *d*-component, *q*-component and *zero*-component of grid voltages in the SRF, respectively. The phase angle of phase *a* voltage in the pre-sag state (no-fault condition) is stored as the reference angle as follows:

$$\theta^{ref} = \arctan\left(\frac{V_{grid,d}\big|_{dc}}{V_{grid,q}\big|_{dc}} \right) \quad \text{Eq. 1.38}$$

where, $V_{grid,d}\big|_{dc}$ and $V_{grid,q}\big|_{dc}$ are dc values of *d*- and *q*-components of grid voltages in the SRF, respectively. After a voltage sag is detected using the proper detection method, the reference fundamental amplitude of line-to-neutral grid voltages (V_{g1}^{ref}) and the obtained reference angle (θ^{ref}) are used to determine the values of reference grid voltages in the SRF as follows:

$$V_{grid,d}^{ref} = V_{g1}^{ref} \cdot \sin\left(\theta^{ref}\right) \quad \text{Eq. 1.39}$$

$$V_{grid,q}^{ref} = V_{g1}^{ref} \cdot \cos\left(\theta^{ref}\right) \quad \text{Eq. 1.40}$$

where, $V_{grid,d}^{ref}$ and $V_{grid,q}^{ref}$ are the reference *d*- and *q*-components of grid voltages in

the SRF, respectively. Next, the differences between the *dq0* values of line-to-neutral grid voltages and the *dq0* values of reference line-to-neutral grid voltages are taken into account as *dq0* values of DVR reference injected voltages as follows:

$$V_{dvr,d}^{ref} = V_{grid,d}^{ref} - V_{grid,d} \quad \text{Eq. 1.41}$$

$$V_{dvr,q}^{ref} = V_{grid,q}^{ref} - V_{grid,q} \quad \text{Eq. 1.42}$$

$$V_{dvr,0}^{ref} = -V_{grid,0} \quad \text{Eq. 1.43}$$

where, $V_{dvr,d}^{ref}$, $V_{dvr,q}^{ref}$ and $V_{dvr,0}^{ref}$ are the reference *d*-component, *q*-component and *zero*-component of DVR series injected voltages in the SRF, respectively. These values are transferred to *abc* coordinate system and then, three single-phase reference voltages of DVR are obtained as follows:

$$\begin{bmatrix} V_{dvr,a}^{ref} \\ V_{dvr,b}^{ref} \\ V_{dvr,c}^{ref} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 1 \\ \cos(\omega t - 120) & \sin(\omega t - 120) & 1 \\ \cos(\omega t + 120) & \sin(\omega t + 120) & 1 \end{bmatrix} \cdot \begin{bmatrix} V_{dvr,d}^{ref} \\ V_{dvr,q}^{ref} \\ V_{dvr,0}^{ref} \end{bmatrix} \quad \text{Eq. 1.44}$$

where, $V_{dvr,a}^{ref}$, $V_{dvr,b}^{ref}$ and $V_{dvr,c}^{ref}$ are the DVR reference injected voltages of phase *a*, *b* and phase *c*, respectively.

1.6. Proposed DVR configuration

Large passive storage components such as electrolytic capacitors, which exist in the grid connected converters, not only decrease the reliability of the equipment but also increase the cost and the size as well [72]. Therefore, a new topology of DVR based on isolated dc-ac converter is proposed in this section which does not need bulky dc link capacitor or energy storage. General scheme of the proposed configuration of DVR is shown in Figure 1.18 which is suitable for both low- and medium-voltage applications. In low-voltage application, the number (N) of dc-ac converters connected in series in each phase is one while this number depends on grid voltage rating in medium-voltage application. The operation principle of the high-frequency (HF) transformer-based dc-ac converter in the proposed DVR is illustrated in Figure 1.19. As shown in Figure 1.18 and Figure 1.19, the proposed configuration has a single-phase active/diode rectifier as the first stage to rectify the single-phase ac sinusoidal input and feed it to inputs of the dc-ac converters connected in series. It is worth mentioning that the capacitor at the input dc link of dc-ac converter is not a bulky capacitor to make a flat dc voltage. Its role is just to filter out the high-frequency (HF) switching currents; so, the voltage across it (V_{Rect_Pri}) is the rectified sinusoidal voltage as shown in Figure 1.19. A feedback control of "voltage balancing of rectified voltages" which will be explained later results in splitting the dc link voltage (V_{dc_Rect}) equally between the inputs of dc-ac converters. As the next stage, the phase-shifted full-bridge (FB) converter at the primary side of the HF transformer chops the input voltage (V_{Rect_Pri}) and converts it to HF voltage (V_{Pri}) which is fed into primary side of the HF transformer. It is worth mentioning that changing the duty cycle (D) of the

phase-shifted FB converter at the primary side causes to control the amplitude of the output voltage (V_{out}). The FB diode-rectifier at the secondary side of the HF transformer rectifies the secondary side voltage and generates the V_{Rect_Sec}. Afterwards, the low-pass filter attenuates HF contents and generates the smooth rectified sinusoidal waveform ($V_{Rect\_Sec\_F}$). As the final step, the secondary side FB converter flips the smooth rectified sinusoidal waveform ($V_{Rect\_Sec\_F}$) at the negative cycle and generates the sinusoidal voltage (V_{out}) at the output of the isolated dc-ac converter. Output voltages of all dc-ac converters connected in series are added together to make DVR reference voltage. The control scheme of the proposed DVR configuration is depicted in Figure 1.20.

The proposed DVR configuration is simulated in PSIM software to validate its performance and control strategy. Since the operation of the proposed DVR is independent at each phase, single-phase circuit is considered for the conducted studies. The main parameters of the simulated circuit are provided in Table 1.2. As the first case study, the circuit is simulated for the load with power factor of 0.98 and the grid voltage with no harmonic distortion. The grid voltage, grid current (increased with factor of 2), DVR reference and injected voltages, rectifier input current (increased with factor of 2), load voltage and load current (increased with factor of 2) are illustrated in Figure 1.21. The grid voltage decreases to 70% of nominal voltage at $t = 0.02s$ while DVR starts to operate after 2ms and compensate the voltage sag. As it is shown, the load voltage is restored to its nominal value thus the sensitive load does not sense the voltage sag disturbance. Hereinafter, voltage sag depth (VSD) is amount of voltage drop regarding the nominal value. For example if the voltage decreases to 70% of nominal value, the residual voltage

is 70% and VSD is 30%.

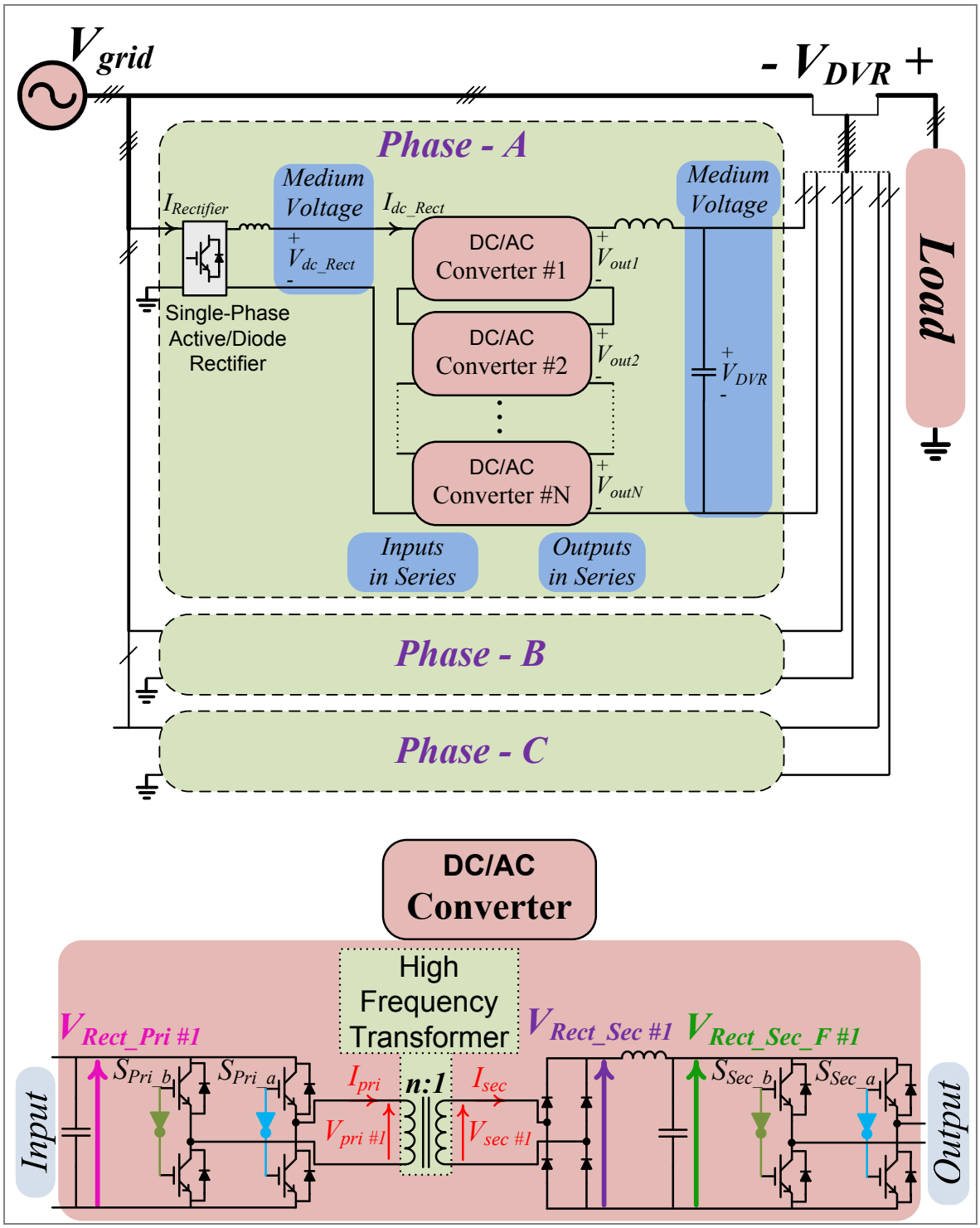

Figure 1.18. The proposed configuration of DVR based on high-frequency transformer dc-ac converter without any bulky dc link capacitor.

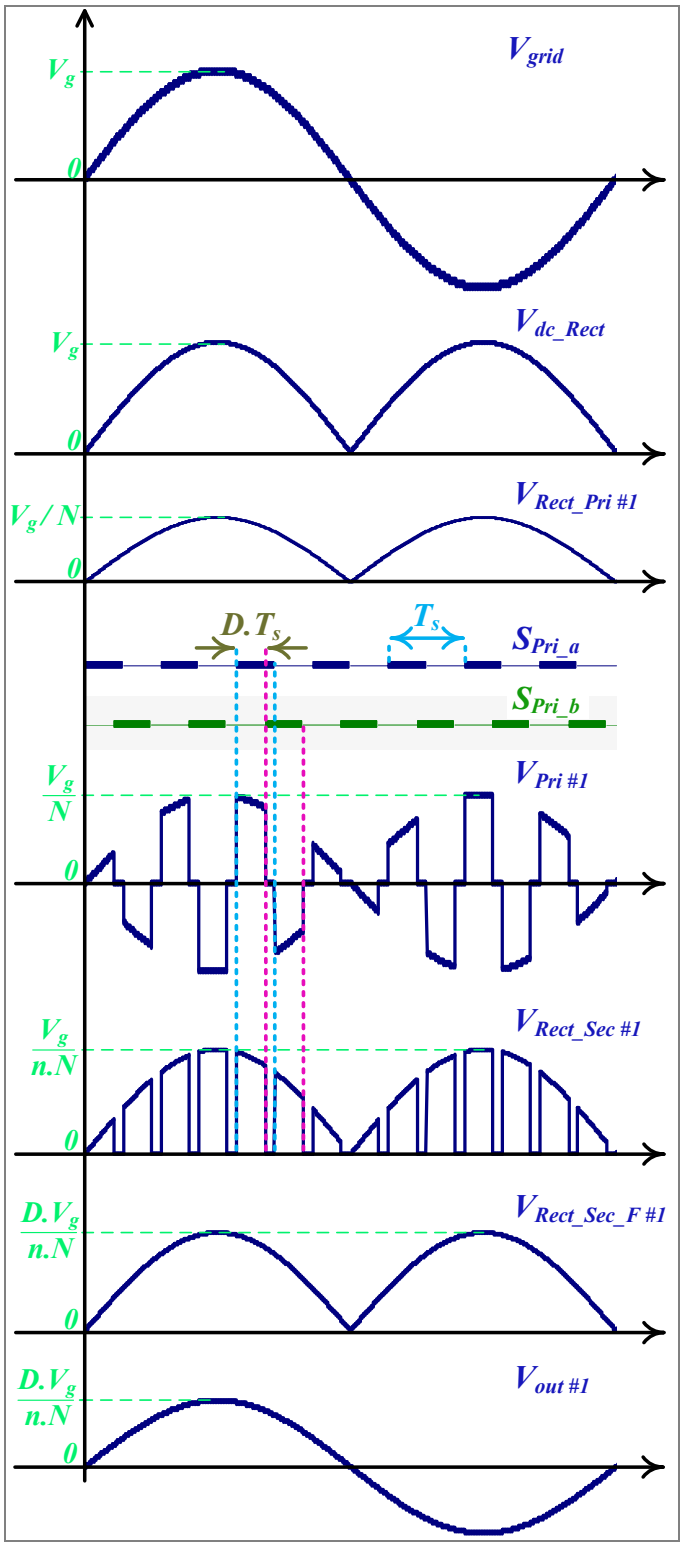

Figure 1.19. Operation principle of high-frequency transformer based dc-ac converter in the proposed DVR configuration.

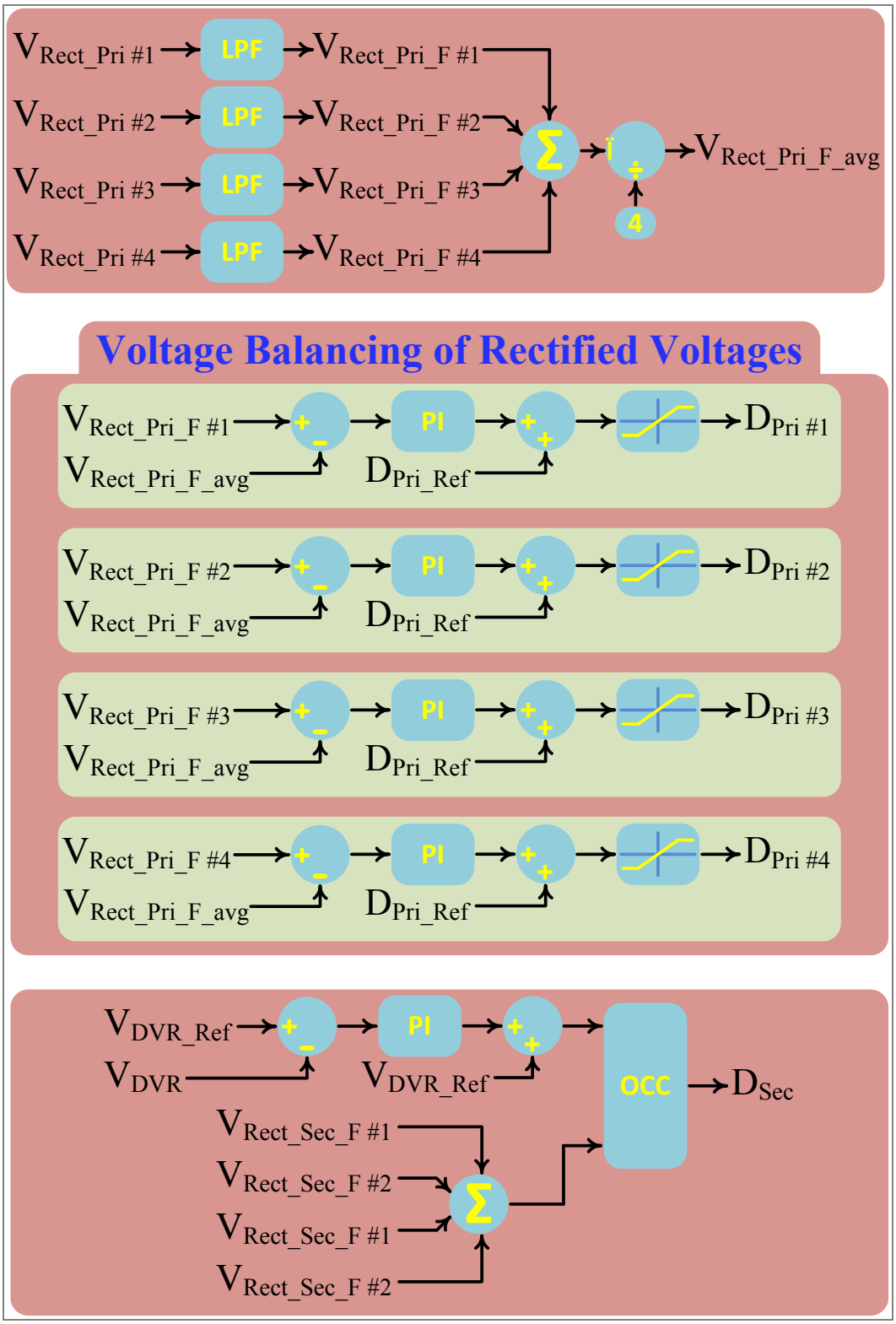

Figure 1.20. Control scheme of the proposed DVR configuration based on high-frequency isolated dc-ac converter.

TABLE 1.2

MAIN PARAMETERS OF THE SIMULATED PROPOSED DVR CONFIGURATION.

System Parameters	Values
Nominal grid rms voltage (line-line), V_{grid}	4.16 kV
System frequency	60 Hz
Load power rating	1.6 MVA
Inductor used at the main input dc link (L_{Pri})	100 µH
Capacitor used at the input of dc-ac converter (C_{Pri})	20 µF
Inductor and capacitor of LC filter at secondary side of the high-frequency transformer (L_{Sec} - C_{Sec})	50 µH -150 µF
Inductor and capacitor of LC filter at DVR output	300 µH - 150 µF
Switching frequency of dc-ac converter	10 kHz
Number of isolated dc-ac converters	4
IGBT voltage drop and ON resistance (V_{CE} - R_{CE})	1 V – 20m
Diode voltage drop (V_F)	1.5 V
The Number of turns at secondary side of high-frequency transformer (N_{Pri})	70
The Number of turns at secondary side of high-frequency transformer (N_{Sec})	100

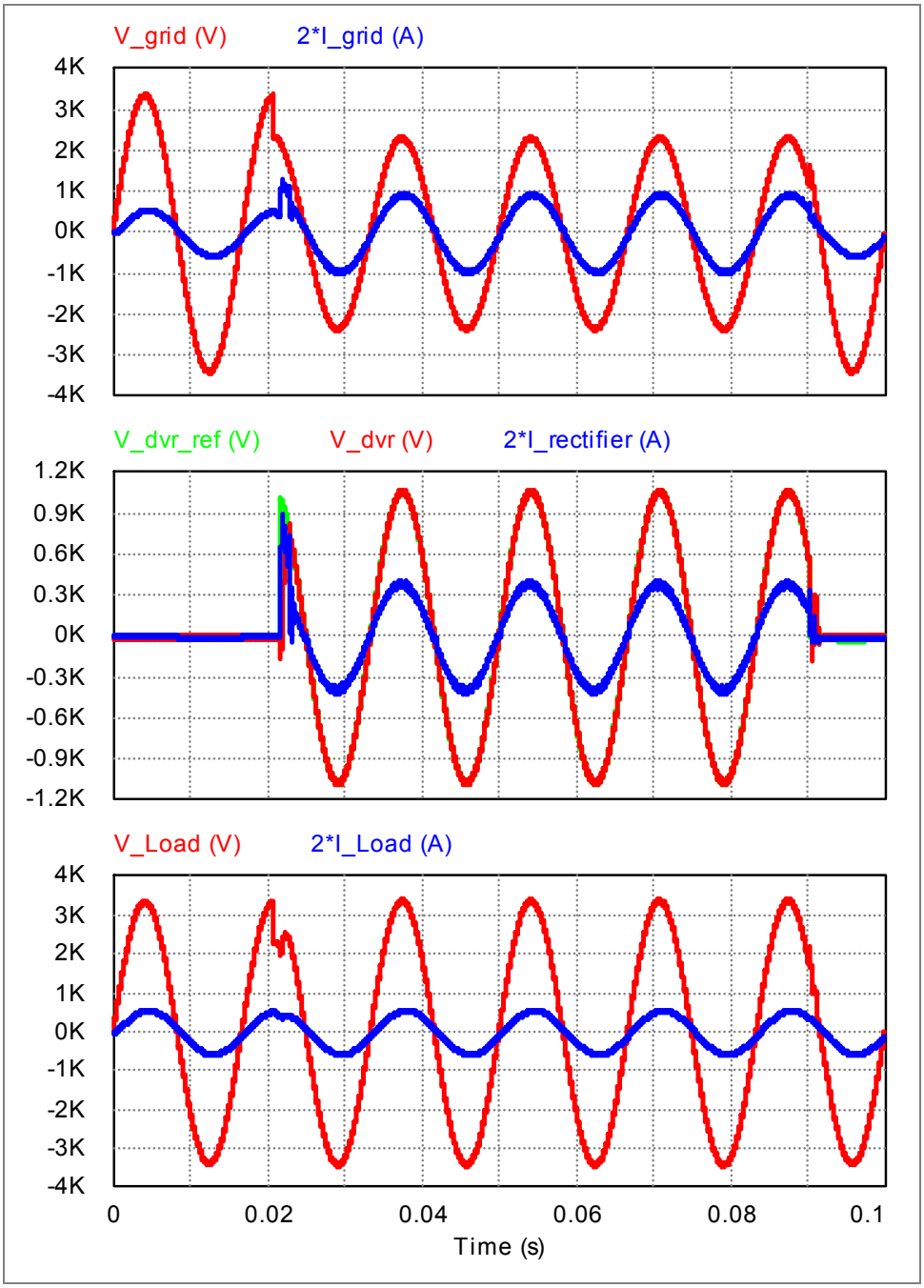

Figure 1.21. Simulation result of the proposed DVR compensating the voltage sag with VSD of 30% and PF of 0.98.

It should be mentioned that the impedance and capacitance characteristic of the capacitors used at the input of isolated dc-ac converter, voltage drop and ON resistance of

diodes and IGBTs as well as the parameters of HF transformer at isolated dc-ac converter may vary from converter to converter. This leads to unequal split of main rectified voltage (V_{dc_Rect}) between inputs of isolated dc-ac converters if all operate with the same duty cycle. The components parameters used in the first isolated dc-ac converter are the same as ones illustrated in Table 1.2. The components parameters in other isolated dc-ac converters which are regarding to the parameters of the first isolated dc-ac converter are as follows:

- $C_{Pri\_2} = 1.1C_{Pri}$ $C_{Pri\_3} = 0.9C_{Pri}$ $C_{Pri\_4} = 1.1C_{Pri}$
- $C_{Sec\_2} = 0.95C_{Sec}$ $C_{Sec\_3} = 1.1C_{Sec}$ $C_{Sec\_4} = 1.1C_{Sec}$
- $V_{CE\_2} = 1.05V_{CE}$ $V_{CE\_3} = 1.05V_{CE}$ $V_{CE\_4} = 0.95V_{CE}$
- $R_{CE\_2} = 1.3R_{CE}$ $R_{CE\_3} = 0.9R_{CE}$ $R_{CE\_4} = 1.2R_{CE}$
- $V_{F\_2} = 1.2V_F$ $V_{F\_3} = 0.9V_F$ $V_{F\_4} = 1.15V_F$
- $N_{Sec\_2} = 0.95N_{Sec}$ $N_{Sec\_3} = 1.02N_{Sec}$ $N_{Sec\_4} = 0.96N_{Sec}$

Figure 1.22 shows the simulation result of effect of the components parameters variation in isolated dc-ac converters which has consequence of unequal split of main rectified voltage (V_{dc_Rect}) between inputs of isolated dc-ac converters (V_{Rect_Pri}). This issue can damage the components, such as capacitor, IGBT and diode, of isolated dc-ac converter if its input voltage exceeds the voltage rating of the components. In order to solve this problem and equally split the main input dc link voltage (V_{dc_Rect}) between the inputs of the dc-ac converters (V_{Rect_Pri}), a feedback control called "voltage balancing of rectified voltages" is utilized. In this feedback control illustrated in Figure 1.20, the inputs

of all dc-ac converter (V_{Rect_Pri}) are passed through the LPF, added together and the summation are divided by number of dc/ac converters (herein 4) to obtain the average of all dc/ac converters' inputs ($V_{Rect\_Pri\_F\_avg}$). Afterwards, the filtered input of each dc/ac converter ($V_{Rect\_pri\_F}$) is compared with the average of all dc-ac converters' inputs ($V_{Rect\_Pri\_F\_avg}$). The output of the comparison is passed through the PI controller to adjust the duty cycle of each dc-ac converter and as a result, the main input dc link voltage (V_{dc_Rect}) can be equally split between the inputs of the dc-ac converters (V_{Rect_Pri}). By enabling the feedback control of "voltage balancing of rectified voltages" shown in Figure 1.20, the main rectified voltage (V_{dc_Rect}) is split equally between the inputs of the isolated dc-ac converters and its result is depicted in Figure 1.23.

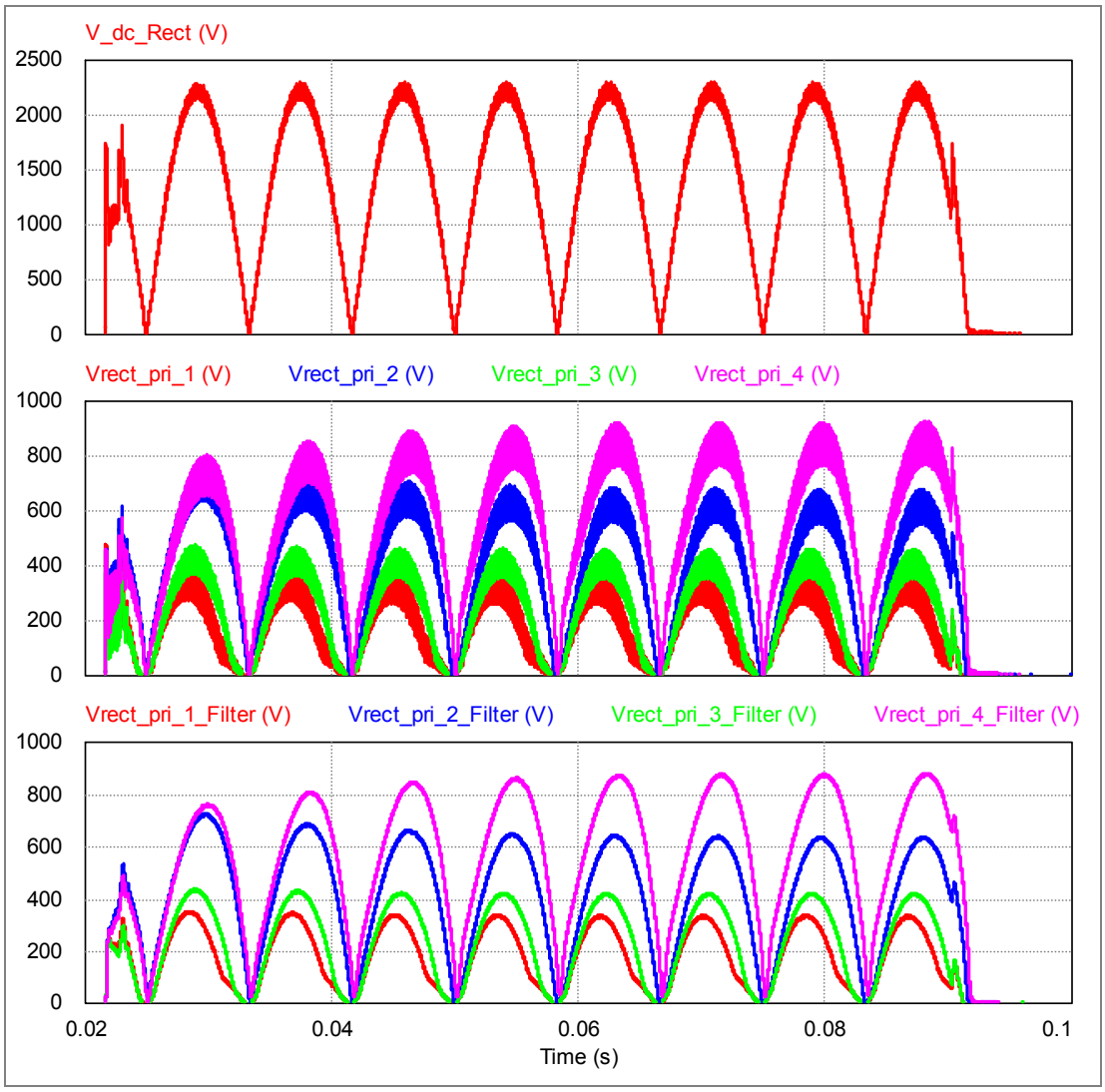

Figure 1.22. Simulation result of the main rectified voltage (V_{dc_Rect}), and actual and filtered input voltage of each isolated dc-ac converter in the proposed DVR while "voltage balancing of rectified voltages" is disabled.

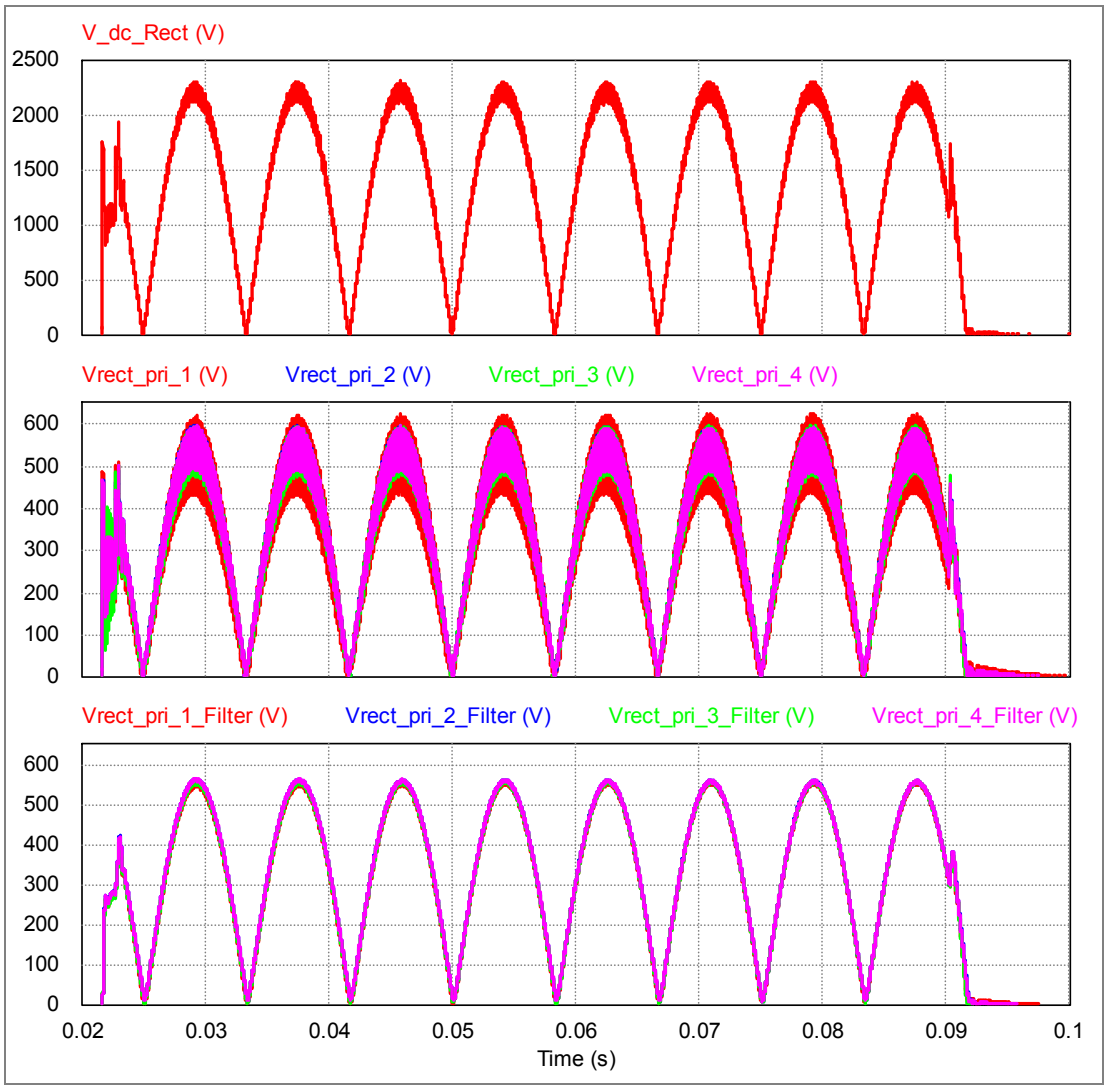

Figure 1.23. Simulation result of the main rectified voltage (V_{dc_Rect}), and actual and filtered input voltage of each isolated dc-ac converter in the proposed DVR while "voltage balancing of rectified voltages" is enabled.

As another case study, the circuit is simulated for the load with power factor of 0.8 and the grid voltage with no harmonic distortion. The grid voltage, grid current (increased with factor of 2), DVR reference and injected voltages, rectifier input current (increased with factor of 2), load voltage and load current (increased with factor of 2) are illustrated in Figure 1.24. The grid voltage decreases to 80% of nominal voltage at $t = 0.02s$ while DVR

starts to operate after 3ms and compensate the voltage sag. As it is shown, the load voltage is restored to its nominal value thus the sensitive load does not sense the voltage sag disturbance. Moreover as shown in Figure 1.25, the main rectified voltage (V_{dc_Rect}) is split equally between the inputs of isolated dc-ac converters due to the well performance of the "voltage balancing of rectified voltages".

As the last case study, the circuit is simulated for the load with power factor of 0.8 and the grid voltage with harmonic distortion of $V_{g5} = V_{g7} = 0.03V_{g1}$. The grid voltage, grid current (increased with factor of 2), DVR reference and injected voltages, rectifier input current (increased with factor of 2), load voltage and load current (increased with factor of 2) are illustrated in Figure 1.26. The grid voltage decreases to 70% of nominal voltage at $t = 0.02s$ while DVR starts to operate after 2ms and compensate the voltage sag. As it is shown, the load voltage is restored to its nominal value thus the sensitive load does not sense the voltage sag disturbance. Moreover as shown in Figure 1.27, the main rectified voltage (V_{dc_Rect}) is split equally between the inputs of isolated dc-ac converters due to the well performance of the "voltage balancing of rectified voltages".

As it is shown in the simulation results, the most advantage of the proposed DVR is that it does not need any bulky capacitor or energy storage device. This causes to reduce the size of DVR and increase its reliability. Moreover, the required isolation in the proposed DVR is implemented using the HF transformer resulting in size reduction of isolation part.

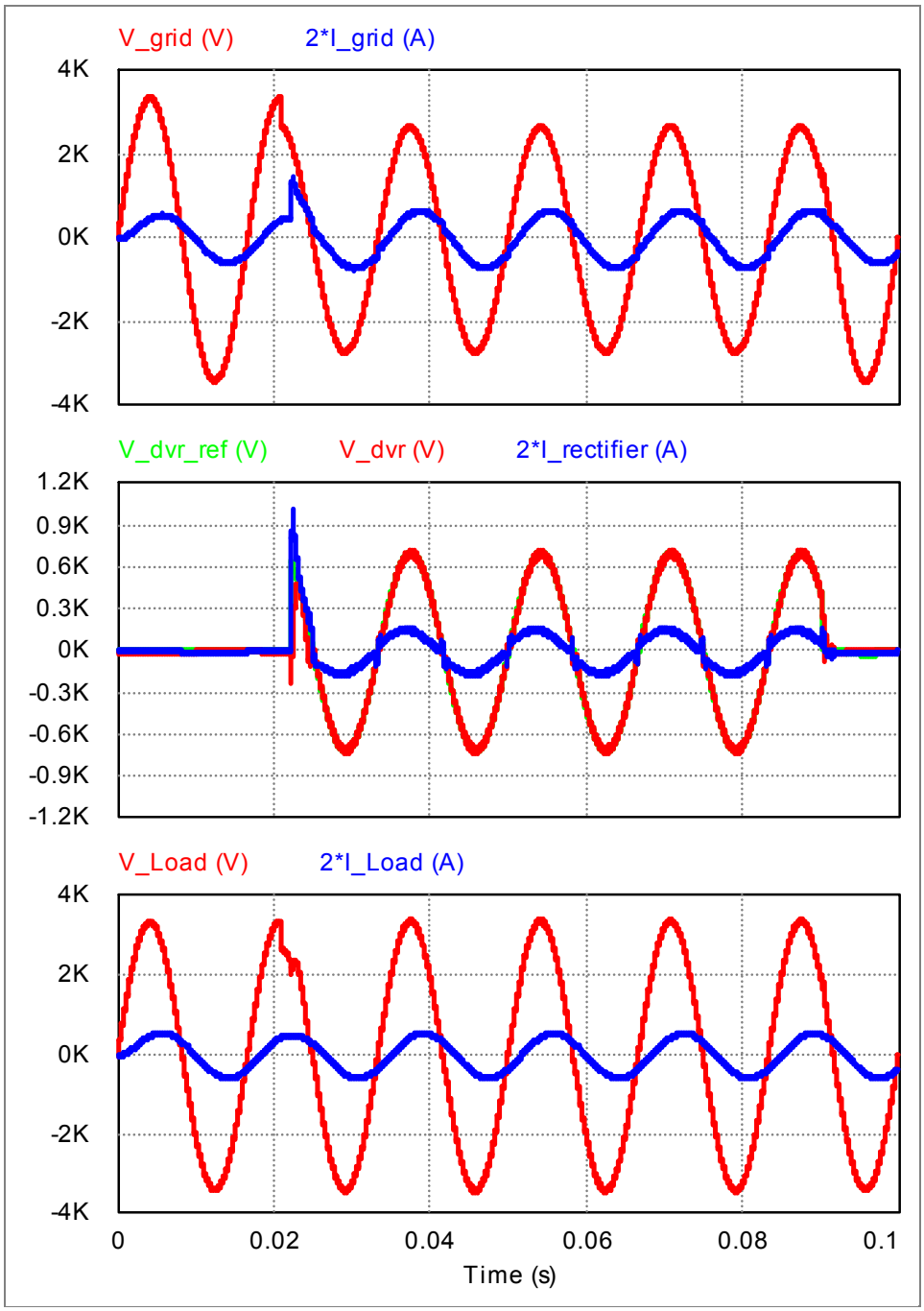

Figure 1.24. Simulation result of the proposed DVR compensating the voltage sag with VSD of 20% and PF of 0.8.

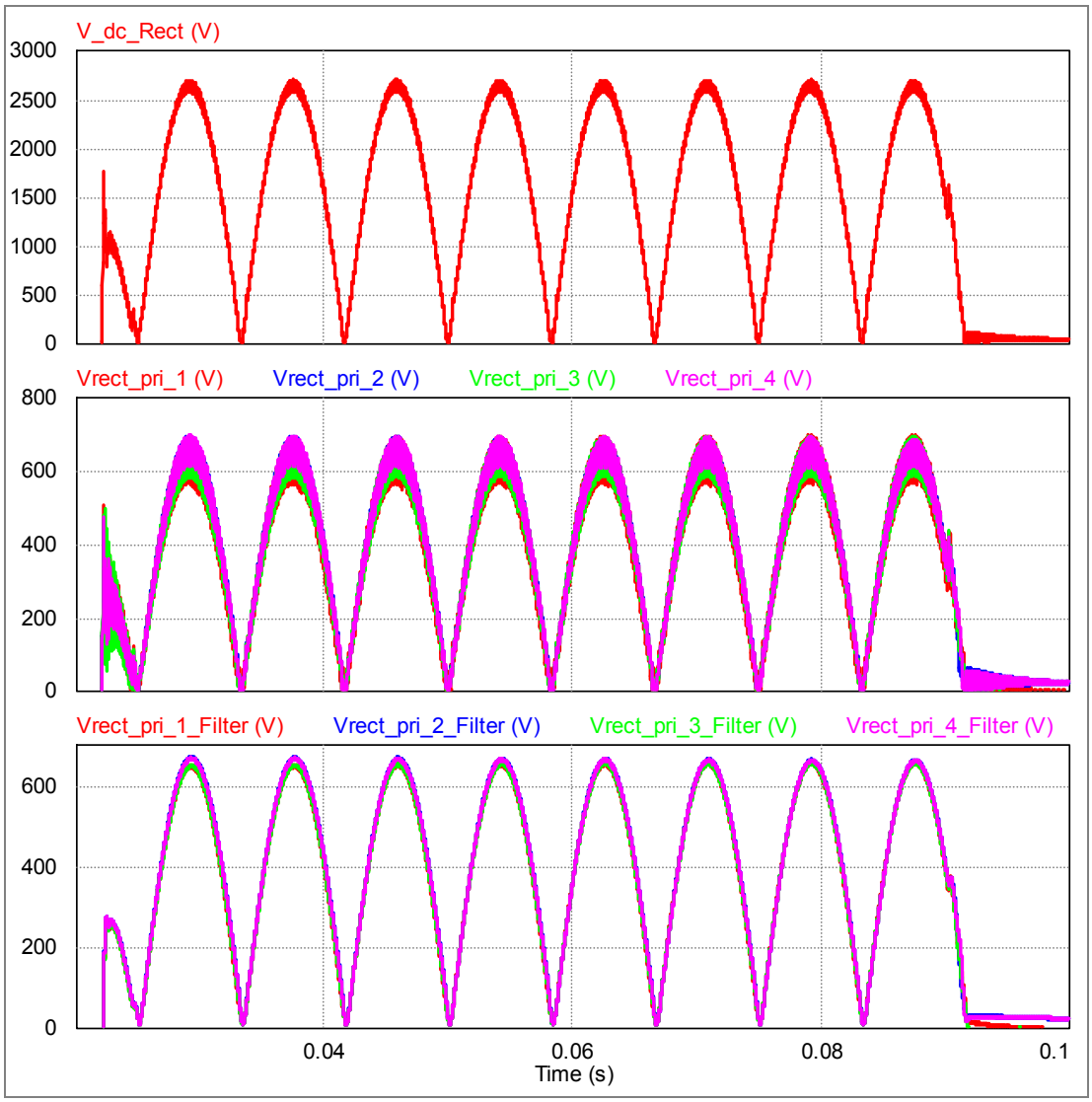

Figure 1.25. Simulation result of the main rectified voltage (V_{dc_Rect}), and actual and filtered input voltage of each isolated dc-ac converter in the proposed DVR while "voltage balancing of rectified voltages" is enabled.

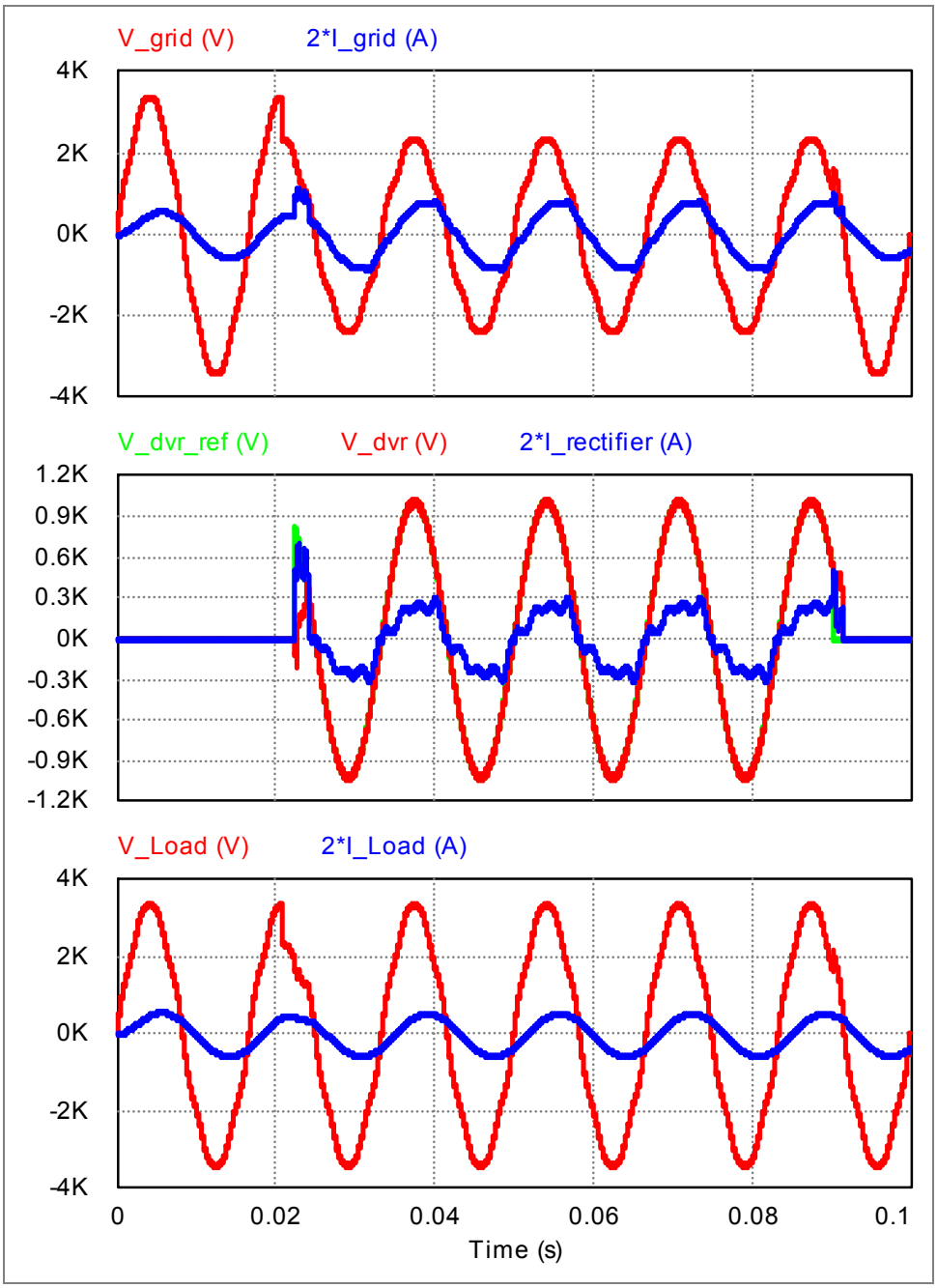

Figure 1.26. Simulation result of the proposed DVR compensating the voltage sag with VSD of 30%, PF of 0.8 and harmonic distortion of $V_{g5} = 0.03V_{g1}$ and $V_{g7} = 0.03V_{g1}$.

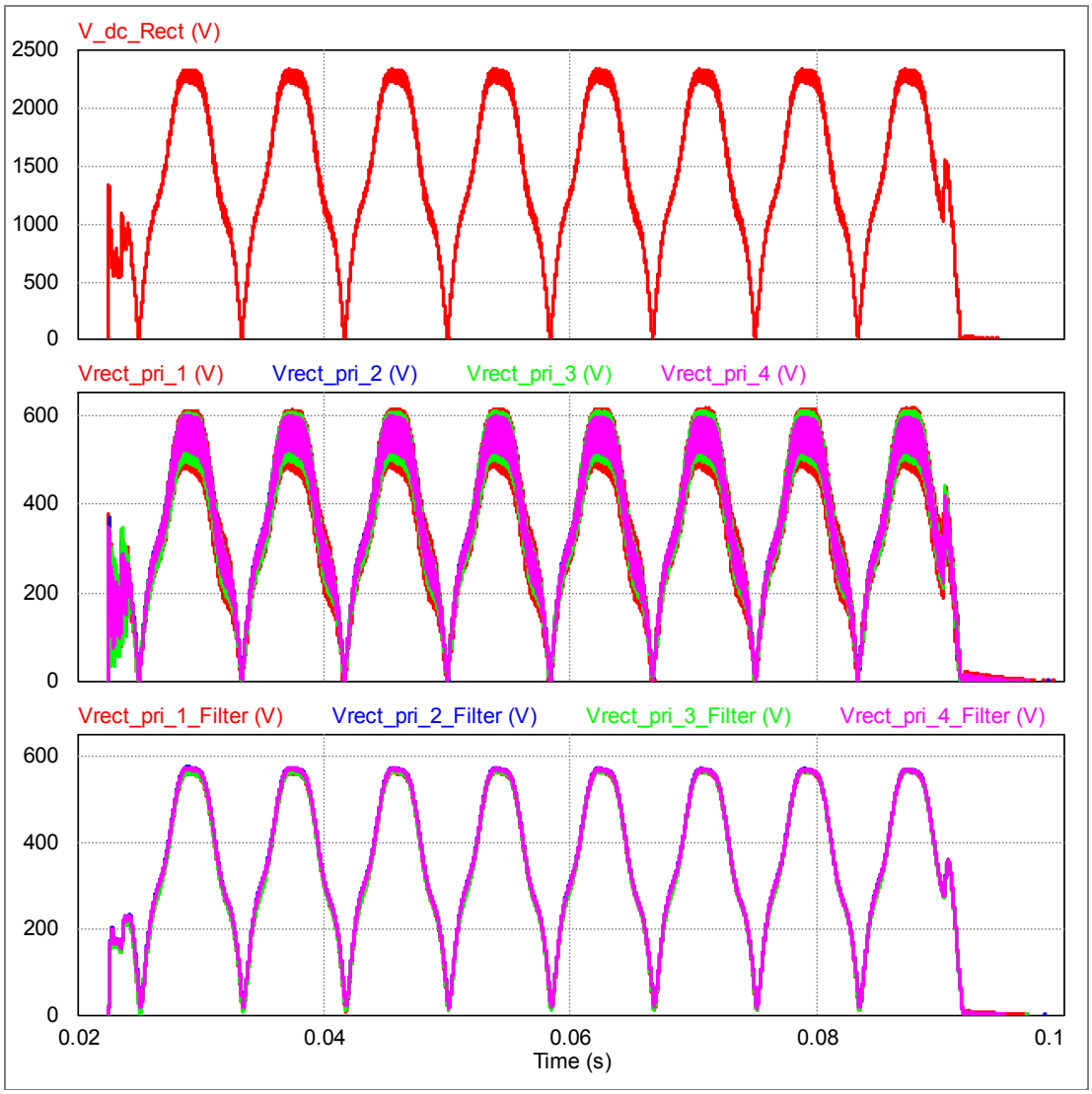

Figure 1.27. Simulation result of the main rectified voltage (V_{dc_Rect}), and actual and filtered input voltage of each isolated dc-ac converter in the proposed DVR while "voltage balancing of rectified voltages" is enabled.

1.7. Conclusion

Voltage sag is a major and frequently occurring problem in the present power grids. Voltage sags are not acceptable for sensitive loads because they cause power loss for sensitive loads, which is a costly problem. Recently due to the increased integration of sensitive loads into power grid, providing high quality power is an important requirement. To suppress the problem of voltage sag, DVRs are suitable devices to compensate these voltage sags, protect sensitive loads and restore their voltage during voltage sag. In this section, the procedures and methods of voltage sag compensation are reviewed, investigated and discussed in detail. The amplitude of the injected voltage by DVR and amount of active power exchanged between DVR and power grid are analyzed for each compensation method. Moreover, all four voltage sag compensation methods are compared with each other and their pros and cons are summarized. Furthermore, different approaches and configurations to provide DVR required active power are reviewed and analyzed. In addition, DVR reference voltage determination method is discussed in detail and the required equations to calculate the reference voltage are obtained. Finally, a new configuration of DVR suitable for both low- and medium-voltage applications is proposed. The proposed configuration of DVR contains several dc-ac converters which are connected in series to split the input medium-voltage between dc-ac converters so that each converter can be implemented using components with low-voltage rating in medium-voltage application. Moreover, HF transformer is utilized in dc-ac converters in order reduce the size of DVR required isolation part. The most important advantage of the proposed DVR is that it does not need any bulky dc capacitor or energy storage causing to reduce the size of

DVR and increase its reliability. The proposed configuration is tested under different conditions of load power factor and grid voltage harmonic. It has been shown that proposed DVR can compensate the voltage sag effectively and protect the sensitive loads. Moreover, the feedback control of "voltage balancing of rectified voltages" is implemented to split the main rectified voltage equally between the inputs of dc-ac converters connected in series in order to guarantee the safe operation of all converters within their voltage limit.

1.8. References

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Chapter 2: Voltage Sag Detection

2.1. Introduction

In recent years, the number of sensitive loads such as medical equipment, factory automations, semiconductor-device manufacturer, and paper manufacturer integrated to power grid has been increased. One of the common characteristics of these sensitive loads is their vulnerability to voltage sags. According to the IEEE STD 1159-2009, voltage sag (also called voltage dip in the IEC terminology) is defined as a decrease of 0.1 to 0.9 p.u. in the voltage at system frequency with the duration of half cycle to one minute [1]–[5]. Recently, a new IEEE Std 1564-2014 "Guide for Voltage Sag Indices" has been approved by IEEE Review Committee in March 2014 which identifies appropriate voltage sag indices and characteristics of electrical power and supply systems [3]. Voltage sags are recognized as a serious and frequently occurring power-quality problem with a costly consequence such as sensitive loads tripping and production loss [6]–[8]. There are several methods for compensating the voltage sag, including static transfer switches, uninterruptible power supplies and dynamic voltage restorer (DVR). The DVR configuration, operation and control methods are discussed in detail in Chapter 1 of this thesis. For all mentioned compensation methods, voltage sag detection is the first step whose response speed is critical for the performance of these compensation methods [9]–[12].

In literature [13]–[83], several methods have been reported to detect the voltage sag such as peak value monitoring based on gradient calculation of voltage, root-mean-square (rms), *dq* transformation, differential controller, obtaining dc voltage from a rectified voltage, wavelet transformer, Kalman filtering, phase-corrected wavelet transform known

as S-transform, numerical matrix based methods, or hybrid methods. These methods generally require complex computation, precise phase-locked-loop, excessive look-up table, and/or low-pass filter.

In Section 2.2 of this chapter, reported methods as well as their advantages and disadvantages are mentioned. In Section 2.3, important criteria and evaluation procedure which should be considered in design of voltage sag detection method are discussed in detail. In Section 2.4, two methods, one is applicable in non-harmonic cases and another is applicable in harmonically distorted cased, are proposed. The first method has a very fast response time and its concept is based on derivative of d-q components of grid voltage. The second method is based on Fourier series and has a very precise and stable detection. Both methods have advantages of easy implementation without using a PLL, look-up table, and low-pass filter and without any complex computation. In addition, the performance of the proposed methods under line-frequency variation condition is analytically investigated in Section 4, whose outcomes are matched exactly with simulation results. The presented methods are simulated in PSCAD and PSIM and experimentally implemented in DSP F28335 and their performance are analyzed in detail considering all important criteria mentioned in Section 2.3 and some of the obtained simulation and experimental results are presented in Section 2.5 and 2.6, respectively. Since the second voltage sag detection method is able to operate in both non-harmonic and harmonically-distorted cases, its DT is obtained in detail for different amounts of VSD, POW and phase jump (PJ) and compared with other methods available in literature in Section 2.7. Due to high number of acronyms in this chapter, a list of acronyms is illustrated in Table 2.1.

TABLE 2.1

LIST OF ACRONYMS

Acronym	Definition
low-pass filter	LPF
phased locked loop	PLL
voltage sag depth	VSD
point-on-wave	POW
phase jump	PJ
detection time	DT
dynamic voltage restorer	DVR
dq-transformation	DQT
wavelet transform	WT
kalman filter	KF
extended kalman filter	EKF
least error square	LES
S-transform	ST
standard deviation	SD
digital signal processor	DSP
calculated fundamental voltage amplitude	CFVA
analog to digital converter	ADC
upper limit	UL
lower limit	LL

2.2. Review of Voltage Sag Detection Methods

2.2.1. Peak Value Monitoring (PVM)

The PVM is the simplest conceptual method that calculates the peak value at the moment at which the gradient of voltage is zero [13]. The drawback of this method is that it may take up to half cycle to detect the voltage sag as well as the high sensitivity of differential function to noise. Moreover, this method is not very practical since the grid voltage is usually harmonically distorted; therefore, there may be several points with the zero gradient in one cycle of fundamental line-frequency [13]. In [14], a method was proposed to phase shift the measured voltage by 90 degrees to obtain the in-quadrature

component of the measured voltage. Then, summing the square of the measured voltage and its in-quadrature component and performing square root of the summation to calculate the grid voltage. However, this method has the delay of quarter of line- cycle and it is not suitable for harmonically distorted voltage [14], [15].

2.2.2. RMS Calculation

The most common and traditional method used for voltage measurement in power system is the calculation of the rms voltage and its performance is analyzed in [16]–[19] and investigated in detail regarding the frequency variation, synchronized and desynchronized calculation in [20]. The rms values can be computed each time a new sample is obtained. If the rms value are updated whenever a new sample is obtained, the calculated rms is called continuous; otherwise, it is called discrete [18]. Simplicity is the main advantage of this method; in contrary, its performance depends on the window length of rms calculation and the time interval for updating the values. The voltage sag DT of this method is up to one cycle of fundamental line-frequency, without any low-pass filter (LPF), for less severe voltage sags. This DT may increase up to two cycles if the LPF is utilized for highly distorted grid voltage. In [21], a new method based on rms calculation has been proposed. This method calculates the ratio of new coming sample, $V(t_n)$, with the previous cycle samples, $V(t_n - T)$ (T is the period of line cycle), continuously and if this ratio for three continuous samples is less than one, it assumes the voltage decreased with the same calculated ratio. This method has been tested just for 50% VSD while the threshold of voltage sag detection is set to 80% instead of 90%. VSD is amount of voltage drop regarding the nominal value. For example if the voltage decreases to 80% of nominal

value, the residual voltage is 80% and VSD is 20%.

2.2.3. D/Q Transformation (DQT)

Since dq-transformation (DQT) is a powerful tool in three-phase systems, the voltage sag detection based on DQT has been proposed and analyzed in [13], [22]–[34]. It is worth mentioning that DQT based voltage sag detection works perfectly with a great detection time (DT), i.e., less than 1ms, for the balanced three-phase voltage sag, i.e., the drop of voltage in all three phase are the same, in the cases of pure sinusoidal voltages (In this topic, DT is the period of time from the moment at which the voltages sag happens to the moment that voltage detection method detects it). However, the grid voltage is not pure sinusoidal in practice and in fact, it is harmonically distorted; in such cases, the components with the frequency of *6k*50/60Hz* (i.e., 360, 720, 1080 … Hz) will be added to d/q components where *k* is integer number. To filter out these undesired components, a LPF can be added to this process at the cost of increasing the DT. Another significant concern is the performance of this method in the case of single-phase voltage sag which constitutes more than 90% of voltage sags in power grid [35]–[38]. In this chapter, the terminology "single-phase voltage sag" refers to the voltage sag that happens in only one of the phases in three-phase system. In these cases, another sinusoidal component at twice of the line frequency with considerable amplitude will be added to d/q components. Three solutions have been reported in literature to solve this problem [28]–[34]. The first solution is to add a LPF with a small cut-off frequency to cancel out the component at twice of the line-frequency resulting in a significant increase of DT. The second solution is to add a differentiator to the DQT based voltage sag detection which has been reported and

analyzed in [28]–[33]. And the last one is constructing the virtual three-phase voltages by measuring one phase voltage in single-phase applications and then, implementing DQT based voltage sag detection [34]. However, the main problem of all three-phase DQT based methods is their inability to detect the single-phase voltage sag with VSD less 30% [22]–[33], [66], [68]–[71]. The reason is that the dc value of the d/q components will change exactly the same as the average of all three phases' voltage drop while the detected voltage drop just depends on dc value drop of the d/q components. For example, if the voltage sag happens only in phase *a* with a 20% VSD, the dc value of d/q components, which will be used to detect the voltage sag, will drop only 6.7% ($=\frac{20\%}{3}$). This means that these methods will finally conclude a voltage drop of 6.7% resulting in no voltage sag event while the threshold value to detect the voltage sag is assigned to 10%. Therefore, all DQT-based voltage sag detection which are measuring the three-phase voltages [13], [22]–[33], [66], [68]–[71] [13], [22]–[33], even the modified ones [28]–[33], are not practical no matter how fast, accurate, or stable they are since they can't detect the single-phase voltage sag with VSD less 30%. All these methods have been tested and analyzed in literature for single-phase voltage sag with VSD more than 30% [22]–[33], [66], [68]–[71].

2.2.4. Rectified Voltage (RV)

Another method reported in [39] is to obtain the dc voltage from a rectified voltage in which the three-phase voltage is rectified by a diode rectifier and then, the rectified voltage is analyzed in order to detect the voltage sag. According to presented results in [39], this method is applicable just for sever three-phase voltage sag while it had around 4% missed detections and 1% false detection for 20% three-phase VSD. Moreover, this

method had a malfunction for three-phase voltage sag with VSD of 15% and the method has not been tested for the single-phase voltage sags since it cannot be applicable for single-phase events with VSD less than 30%.

2.2.5. Wavelet Transform (WT)

In the power system studies, WT has drawn attention of researchers in the area of power system transients' analysis. Wavelet analysis is based on the decomposition of a signal according to time domain, rather than frequency, using basic functions with adaptable scaling properties; this is also known as multi-resolution analysis. The discrete wavelet transform provides a non-uniform division of the time-frequency plane which means short-time intervals for high-frequency components and long-time intervals for low-frequency components. It has been reported in [40] that shorter wavelets are best suited for detecting fast transients while longer wavelets for detecting slow transients. The main concern of WT application is selection of the most appropriate wavelet mother function which depends on the type of disturbance needed to be detected and analyzed [19], [40]–[43]. In [42], different wavelet functions for the analysis of voltage sag disturbances has been analyzed and compared with each other and it has been recommended to use the Daubechies with 6 coefficients. The WT based voltage sag detection has been reported and tested in [19], [40]–[50] but none of them has considered the harmonically distorted voltages which is common in reality. The reason is that the first-level decomposition coefficient is highly sensitive to harmonic and thus, the WT based voltage sag detection method can't be applicable in real cases without any extra consideration [19], [41], [43]. Furthermore, the magnitude of the calculated first-level decomposition coefficient for the

same VSD is function of the sampling frequency and specially, the point-on-wave (POW) [13], [19], [41], [43]. POW is the moment at which the voltage sag disturbance happens and it is between 0^o to 360^o of one line cycle. According to presented results in [43], the magnitude of the calculated first-level decomposition coefficient for different POWs changes from 1 to 47 units for the same VSD which shows that the obtained signals from the WT-based method highly depends on POW. Therefore, the adequate threshold level of comparator, which is variable and highly depends on POW, should be defined offline and stored in the memory of processor for real-time applications requiring precise phased locked loop (PLL) and excessive lookup table which make the implementation of this method very difficult in reality.

2.2.6. Kalman Filtering (KF)

The KF, which uses a mathematical model of the signal in state variable form, is another accurate algorithm for signal tracking and has been utilized in the power system studies for disturbance detection [41], [44], [51]–[53]. One of the main advantages of the KF is its capability to provide the best estimation of the state variables with the smallest number of samples [44]. Though, the complexity of the system model used in KF affects performance and accuracy of the method in detection and analysis of voltage disturbances [19], [41], [43]. It means that the more complicated the model of system, the slower the dynamic response of the filter. Thus, the voltage sag detection method based on KF may have a delay time in practical cases including the harmonics since each frequency component requires two state variables, the components in phase and in quadrature with respect to its respective rotating reference [19], [41], [43], [44], [54]. To carry out KF

calculation, it is necessary to perform four multiplications and four sums in real time for each pair of state variables. A possible solution to improve the performance of a linear KF is to use an extended KF (EKF) [41], [54], [55] where the nonlinear model is linearized using a first-order Taylor series to form a linear process and then, the linear KF equations are applied. EKF show faster time response than linear KF, but they could present convergence problems if the filter is not properly tuned which can be consider a difficulty for this method [41] in practical cases. In addition, the size of matrices required for computation process in KF based voltage sag detection methods directly depends on number of existent harmonics in the voltage which causes to increase the complexity and time response in practical cases. Moreover, KF is sensitive to the information of disturbances and has a weak response to critical transients in the input signal parameters [56]. In order to minimize the estimation error of KF and keep it as low as possible, the specific statistical settings about disturbances and noise must be chosen close enough to realty [56]. In [56], brief details of the KF and more importantly, the necessity of statistical information of the disturbances for the KF is explained.

2.2.7. Hybrid Methods

Several hybrid methods of voltage sag detection have been reported in [41], [43], [54], [55], [59]–[64]. In [41], [43], a method which is a combination of WT and EKF has been presented in which the voltage sag can be detected either by EKF directly or initially can be detected by WT and then, be finalized after it is confirmed by EKF. This hybrid method has a 10ms waiting time as an event confirmation between the EKF and WT methods if the voltage sag is detected by WT first. In [54], a method based on the

combination of rms calculation and KF has been proposed. The reason of this combination is that the KF has faster DT than the rms calculation for some POWs while for other POWs, the rms calculation has faster DT. Thus, with such a combination it is possible to take the advantages of both KF and rms calculation simultaneously.

In [55], a method as a combination of phase-corrected wavelet transform known as S-transform (ST) and EKF has been presented in which is obtained from the ST matrix and can be used to visually classify the nature of disturbance event. Afterwards, the standard deviation (SD) of obtained contour has been calculated for different cases such as voltage sag, swells and interruption, short-duration power frequency disturbance, with and without harmonic. The SD of obtained contour has been found as a good indicator to distinguish the event between the short-duration power-frequency disturbance and high-frequency oscillatory transient. Once the SD is more than the offline calculated threshold, the EKF is used to estimate the amplitude of grid voltage to detect the voltage sag, swells and interruption. However, no information has been provided about the accuracy and time response of this method.

In [56], a detection method based on combination of KF and LES techniques has been presented. As explained previously, KF needs specific statistical settings about disturbances and noise available in input signal and has a weak response to critical transients in the input signal parameters. Lowering the level of disturbances and noise leads to less deviation between these settings and the real values. Therefore, in [56] LES filtering is utilized to refine the input signal, detect the large changes in the signal parameters and produce another periodic signal that meets the requirements of the KF while KF operates as a core of detection method.

In [59]–[62], the method based on combination of instantaneous comparison, between the reference voltage and actual voltage, and continuous rms measurement has been presented. In this method, the grid voltage is compared with 90% of reference voltage, obtained from PLL, continuously and once there is difference between the grid voltage and 90% of reference voltage, initial sag flag triggers. Whenever the initial sag flag triggers, the current rms value (X1) is stored in the memory. The continuous rms measurement keeps updating the rms value for each new coming sample and it checks new rms value (X2) after previously defined period (1.7 ms) regarding the time of the initial sag flag activation. If the rms variation (X1-X2) is more than threshold (which is variable and depends on POW and calculated offline and stored in memory), the voltage disturbance is considered as voltage sag. It is worth mentioning that the rms value in this method is updated each sampling cycle. This method needs precise PLL and excessive amount of variable threshold values stored in lookup table.

In [65], a detection method based on the non-linear adaptive filter has been reported which is applicable for both single- and three-phase systems. In [66], a detection method based on combination of LES and DQT techniques is presented where LES filter and instantaneous symmetrical components method is utilized to estimate the positive sequence component of three single-phase voltages. The obtained positive components are provided for DQT to calculate the *d/q* components. Utilization of LES filter results in avoiding the low-pass filter to cancel out the harmonics in d/q components and have fast response to obtain the positive sequence components. Some other advanced mathematical-based voltage sag methods have been presented such as adaptive perceptron [67], cascaded delayed signal cancellation or delayed signal cancellation processes for three-phase

application in [68]–[71] and single-phase application in [72] and neural-network-based techniques (also called Adaline method) in [73]–[75].

2.3. Important Criteria for Design and Evaluation of Voltage Sag Detection Method

It is worth mentioning that one of the important parameters which should be considered during the performance evaluation of voltage sag detection method is DT which highly depends on VSD, POW and PJ. The PJ means a sudden change in angle of voltage phasor and VSD is defined as %100 minus the residual voltage which is in percentage of nominal voltage. Thus, dependence of voltage sag detection method's DT on different amounts of VSD, POW and PJ should be considered during the performance evaluation. Another important parameter, which determines the reliability/stability of detection method, is ripple amount of calculated fundamental voltage amplitude. The ripple is defined as half of the difference between the max and min of the fundamental voltage amplitude calculated by detection method. It is noteworthy that the probability of voltage sag events whose VSD amount is between 5% and 15% is considerable [35]–[38]. On the other hand, the threshold of voltage sag detection is 10% (i.e., the residue voltage is 90% of nominal voltage) according to IEEE STD 1159-2009. Therefore, the stable operation of voltage sag detection method in the mentioned region, where the VSD is between 5% and 15%, is critical. The more ripple the calculated fundamental voltage amplitude, the more instability the detection method; herein, the instability of detection method means continuous triggering of detection logic-signal when calculated fundamental voltage amplitude oscillates around the threshold of voltage sag detection due to ripple.

Consequently, if the ripple of calculated fundamental voltage amplitude is not zero, significant percentage of voltage sags with VSD of 5% to 15% may cause malfunction (unstable) operation of detection method. To avoid this issue, the voltage sag detection method should be designed such a way to minimize the amount of ripple. However, since the zero amount of ripple is not possible practically due to limitation of sampling devices such as digital signal processor (DSP), the constant threshold comparator should be replaced by hysteresis-band-based threshold comparator in design process of voltage sag detection method. The hysteresis band is already presented in international standards dealing with voltage sag detection (e.g. IEC 61000-4-30 and IEEE 1564), but its purpose "in the context of power quality measurements is to avoid counting multiple events when the magnitude of the parameter oscillates around the threshold level". Herein, the hysteresis band is needed for voltage sag detection method to avoid instability of detection method which means continuous triggering and consequently, to avoid the malfunction of DVR. However, adding hysteresis band is not an alternative solution to ignore the necessity of having sufficiently low ripple in design of detection method to. If the ripple of calculated fundamental voltage amplitude is not negligible, a wide threshold band needs to be implemented which increases the DT and causes the malfunction of detection method. In addition, the term of accuracy which means the error between the calculated fundamental voltage amplitude and actual one is another parameter of voltage sag detection method. The reliability/stability and accuracy of the voltage sag detection method should be analyzed for cases of non-harmonic condition, harmonic distortion, line frequency variation and PJ. Typically, available articles have just considered a few of the mentioned criteria, not all of them, for evaluation of their method [13]–[34], [39]–[56],

[58]–[73], [75]–[83]. Following are the list of important criteria and the articles which considered the related criteria:

- Dependence of the DT on VSD [33], [43], [52], [54], [76], [78].
- Dependence of the DT on POW [31], [33], [43], [49], [50], [52], [54], [76], [83].
- The error between the calculated fundamental voltage amplitude and actual fundamental voltage amplitude [55], [69], [70], [72].
- The ripple of calculated fundamental voltage amplitude [34], [69], [70], [72].
- Performance of method under line frequency variation [20], [33], [56], [68]–[73], [75], [76].
- Performance of method under harmonic distortion [30], [31], [34], [43], [44], [54]–[56], [58], [59], [61], [62], [66]–[73], [75].
- Performance of method under phase jump [52], [69].

As it can be pointed out, most of the available papers have considered just one of the mentioned criteria and just some of them ([31], [33], [34], [43], [52], [54]–[56], [68]–[73], [75], [76]) have considered more than one criterion. All of these aspects are considered in this chapter to evaluate the performance of the proposed detection method.

2.4. Proposed Voltage Sag Detection Methods

In this section, two following methods are proposed while one is applicable in non-harmonic cases and another is applicable in harmonically distorted cases.

2.4.1. Non-Harmonic Voltage Sag Detection Method

In this section, a simple voltage sag detection method suitable for both single- and three-phase systems is proposed. As the proposed method is applicable independently to each phase, herein it will be explained in a single-phase system. Although the harmonics are unavoidable in power grid, they can be eliminated using the low-pass filter. After filtering, the grid voltage can be written as follows:

$$v_{grid}(t) = V_g \cdot \sin(\omega \cdot t + \theta) \text{ and } \omega = 2\pi f \quad \text{Eq. 2.1}$$

where, V_g, f and θ are peak value, frequency, and angle, respectively, of the grid voltage. For the convenience of the discussion, the α- and β-components are defined as follows:

$$v_{grid,\alpha}(t) = v_{grid}(t) \cdot \sin(\omega t) = 0.5 \cdot V_g \left[\cos(\theta) - \cos(2\omega t + \theta)\right] \quad \text{Eq. 2.2}$$

$$v_{grid,\beta}(t) = v_{grid}(t) \cdot \cos(\omega t) = 0.5 \cdot V_g \left[\sin(2\omega t + \theta) + \sin(\theta)\right] \quad \text{Eq. 2.3}$$

According to the above equations, both α- and β-components contain a dc value and a sinusoidal component at twice of the line frequency. To extract the dc value (*i.e.,* $0.5 \cdot V_g \sin(\theta)$ and $0.5 \cdot V_g \cos(\theta)$), which represents the peak or rms value, one possible solution is to calculate the average of α- and β-components, which takes half cycle of fundamental frequency. An alternative solution, which is the key of proposed method, is to

manipulate the α- and β-components to cancel out the dc value by calculating the derivation of α- and β-components, and consequently, obtain the peak value instantly. The derivation of α- and β-components can be written as follows:

$$v'_{grid,\alpha}(t) = \frac{d}{dt}\left[v_{grid,\alpha}(t)\right] = \omega V_g \cdot \sin\left(2\omega t + \theta\right) \quad \text{Eq. 2.4}$$

$$v'_{grid,\beta}(t) = \frac{d}{dt}\left[v_{grid,\beta}(t)\right] = \omega V_g \cdot \cos\left(2\omega t + \theta\right) \quad \text{Eq. 2.5}$$

subsequently, the peak value of grid voltage can be detected instantly as follows:

$$\left[\left(v'_{grid,\alpha}(t)\right)^2 + \left(v'_{grid,\beta}(t)\right)^2\right] = \left(\omega V_g\right)^2 \cdot \underbrace{\left[\begin{array}{c}\left(\sin\left(2\omega t + \theta\right)\right)^2 \\ + \\ \left(\cos\left(2\omega t + \theta\right)\right)^2\end{array}\right]}_{=1} \quad \text{Eq. 2.6}$$

$$V_g = \frac{\sqrt{\left(v'_{grid,\alpha}(t)\right)^2 + \left(v'_{grid,\beta}(t)\right)^2}}{\omega} \quad \text{Eq. 2.7}$$

According to Eq. 2.7, any variation in peak value of grid voltage can be detected instantly. As a result, the voltage sag can be detected as soon as there is any voltage drop.

2.4.2. Harmonically-Distorted Voltage Sag Detection Method

The concept of Fourier series is a powerful means to analyze periodic waveforms in terms of sinusoidal waveform and it is applicable in power system studies since it has almost periodic voltage and current waveforms. In this section, a method, applicable for

both single- and three-phase systems, is proposed to detect the fundamental voltage amplitude. Since this method is applicable independently to each phase, herein it will be explained in a single-phase system. By taking into account the fundamental and harmonic components, grid voltage can be written as follows:

$$v_{grid}(t) = V_{g1} \cdot \sin(\omega t + \theta_1) + \sum_{n=3,5,\ldots} V_{gn} \cdot \sin(n \cdot \omega t + \theta_n) \quad \text{Eq. 2.8}$$

where, $\omega = 2\pi f$, V_{g1} is amplitude value of fundamental component, V_{gn} is amplitude of n^{th} harmonic component, f is line frequency (60 Hz), and θ_n is the angle of n^{th} grid voltage phasor. The *d*- and *q*-components in single-phase rotating reference frame is defined as follows:

$$v_{grid,d}(t) = v_{grid}(t) \cdot \sin(\omega t) \quad \text{Eq. 2.9}$$

$$v_{grid,q}(t) = v_{grid}(t) \cdot \cos(\omega t) \quad \text{Eq. 2.10}$$

By recalling Eq. 2.11 and Eq. 2.12, Eq. 2.9 and Eq. 2.10 can be written as Eq. 2.13 and Eq. 2.14.

$$\sin(\alpha) \cdot \sin(\beta) = \frac{1}{2}\left[\cos(\alpha - \beta) - \cos(\alpha + \beta)\right] \quad \text{Eq. 2.11}$$

$$\sin(\alpha) \cdot \cos(\beta) = \frac{1}{2}\left[\sin(\alpha + \beta) + \sin(\alpha - \beta)\right] \quad \text{Eq. 2.12}$$

$$v_{grid,d}(t)=\frac{V_{g1}}{2}\left[\cos(\theta_1)-\cos(2\omega t+\theta_1)\right]+\sum_{n=3,5,\ldots}\frac{V_{gn}}{2}\begin{bmatrix}\cos\left((n-1)\omega t+\theta_n\right)\\-\\\cos\left((n+1)\omega t+\theta_n\right)\end{bmatrix} \quad \text{Eq. 2.13}$$

$$v_{grid,q}(t)=\frac{V_{g1}}{2}\left[\sin(\theta_1)+\sin(2\omega t+\theta_1)\right]+\sum_{n=3,5,\ldots}\frac{V_{gn}}{2}\begin{bmatrix}\sin\left((n-1)\omega t+\theta_n\right)\\+\\\sin\left((n+1)\omega t+\theta_n\right)\end{bmatrix} \quad \text{Eq. 2.14}$$

According to the above equations, both *d*- and *q*-components contain a dc value and a sinusoidal components at 2, 4, 6, … times of the line frequency. To extract the fundamental voltage amplitude (i.e., V_{g1}), required for voltage sag detection, the solution is calculating an average of *d*- and *q*-components, which takes half cycle of fundamental frequency. As a result, it can be written as follows:

$$v_{grid,d}(t)\Big|_{dc}=\frac{2}{T}\cdot\int_{t-T/2}^{t}v_{grid,d}(t)\cdot dt=\frac{V_{g1}}{2}\cdot\cos(\theta_1) \quad \text{Eq. 2.15}$$

$$v_{grid,q}(t)\Big|_{dc}=\frac{2}{T}\cdot\int_{t-T/2}^{t}v_{grid,q}(t)\cdot dt=\frac{V_{g1}}{2}\cdot\sin(\theta_1) \quad \text{Eq. 2.16}$$

where $T=1/f$. Subsequently, the fundamental voltage amplitude of grid voltage can be calculated as follows:

$$\left[\left(v_{grid,d}(t)\Big|_{dc}\right)^2+\left(v_{grid,q}(t)\Big|_{dc}\right)^2\right]=\left(\frac{V_{g1}}{2}\right)^2\cdot\underbrace{\left[\left(\cos(\theta_1)\right)^2+\left(\sin(\theta_1)\right)^2\right]}_{=1} \quad \text{Eq. 2.17}$$

$$V_{g1,calculated} = 2 \cdot \sqrt{\left(v_{grid,d}(t)\big|_{dc}\right)^2 + \left(v_{grid,q}(t)\big|_{dc}\right)^2} \qquad \text{Eq. 2.18}$$

According to Eq. 2.18, any variation in fundamental amplitude of grid voltage can be calculated within half cycle by this method. It should be mentioned that this method is based on half cycle Fourier series but there is not a paper studying the half cycle based Fourier series to detect the voltage sag by considering all important criteria mentioned in Section 2.3 such as different amounts of VSD, POW, PJ, harmonic distortion and line frequency variation. Moreover, performance of the proposed method under line-frequency variation condition is analytically investigated and obtained analytical result is compared with simulation results in following. It is worth mentioning that this method is also applicable to detect the voltage swell since it can follow any change, either decrease or increase, at fundamental voltage amplitude.

Frequency variation might affect the result of the fundamental voltage amplitude calculation since no PLL is utilized in this method to measure line frequency. By considering the frequency variation ($\Delta f \le \pm 1\,\text{Hz} = f/60$), Eq. 2.8 can be written as follows:

$$v_{grid}(t) = V_{g1} \cdot \sin\left(\omega t + \Delta\omega t + \theta_1\right) + \sum_{n=3,5,\ldots} V_{gn} \cdot \sin\left(n \cdot \omega t + n \cdot \Delta\omega t + \theta_n\right) \qquad \text{Eq. 2.19}$$

where, $\Delta\omega = 2\pi \cdot \Delta f$. Afterwards, the *d*- and *q*-components in single-phase rotating reference frame according to Eq. 2.9 and Eq. 2.10 can be expressed as:

$$v_{grid,d}(t)=\frac{V_{g1}}{2}\left[\cos\left(\Delta\omega t+\theta_1\right)-\cos\left(2\omega t+\Delta\omega t+\theta_1\right)\right]+\sum_{n=3,5,\ldots}\frac{V_{gn}}{2}\begin{bmatrix}\cos\left((n-1)\,\omega t+\Delta\omega t+\theta_n\right)\\-\cos\left((n+1)\,\omega t+\Delta\omega t+\theta_n\right)\end{bmatrix} \quad \text{Eq. 2.20}$$

$$v_{grid,q}(t)=\frac{V_{g1}}{2}\left[\sin\left(\Delta\omega t+\theta_1\right)+\sin\left(2\omega t+\Delta\omega t+\theta_1\right)\right]+\sum_{n=3,5,\ldots}\frac{V_{gn}}{2}\begin{bmatrix}\sin\left((n-1)\,\omega t+\Delta\omega t+\theta_n\right)\\+\sin\left((n+1)\,\omega t+\Delta\omega t+\theta_n\right)\end{bmatrix} \quad \text{Eq. 2.21}$$

Substituting Eq. 2.20 in Eq. 2.15 results in Eq. 2.22.

$$v_{grid,d}(t)\Big|_{dc}=\frac{2}{T}\cdot\int_{t-T/2}^{t}v_{grid,d}(t)\cdot dt=\frac{2}{T}\cdot\left(\begin{array}{l}\displaystyle\int_{t-T/2}^{t}\frac{V_{g1}}{2}\left[\underbrace{\cos\left(\Delta\omega t+\theta_1\right)}_{X1}-\cos\left(2\omega t+\Delta\omega t+\theta_1\right)\right]\cdot dt\\[2ex]\displaystyle+\int_{t-T/2}^{t}\sum_{n=3,5,\ldots}\frac{V_{gn}}{2}\begin{bmatrix}\cos\left((n-1)\,\omega t+\Delta\omega t+\theta_n\right)\\-\cos\left((n+1)\,\omega t+\Delta\omega t+\theta_n\right)\end{bmatrix}\cdot dt\end{array}\right) \quad \text{Eq. 2.22}$$

It should be mentioned that term X1 in Eq. 2.22 has a long period whose minimum is 60T since $\Delta f \le \pm 1\,\text{Hz} = f/60$. Consequently, variation of term X1 in time interval of T/2, which is 1/120 or even lesser than its own period, is negligible and therefore, term X1 in Eq. 2.22 can be taken out of integral as expressed in Eq. 2.23.

$$v_{grid,d}(t)\Big|_{dc} = \frac{2}{T}\cdot\left(\begin{array}{l} \dfrac{V_{g1}}{2}\left[\begin{array}{l}\cos\left(\Delta\omega t+\theta_1\right)\cdot 1\Big]_{t-T/2}^{t} \\ -\dfrac{\sin\left(2\omega t+\Delta\omega t+\theta_1\right)}{2\omega+\Delta\omega}\Big]_{t-T/2}^{t}\end{array}\right] \\ +\displaystyle\sum_{n=3,5,\ldots}\frac{V_{gn}}{2}\left[\begin{array}{l}\dfrac{\sin\left(\left(n-1\right)\omega t+\Delta\omega t+\theta_1\right)}{\left(n-1\right)\omega+\Delta\omega}\Big]_{t-T/2}^{t} \\ -\dfrac{\sin\left(\left(n+1\right)\omega t+\Delta\omega t+\theta_1\right)}{\left(n+1\right)\omega+\Delta\omega}\Big]_{t-T/2}^{t}\end{array}\right]\end{array}\right) \qquad \text{Eq. 2.23}$$

By recalling Eq. 2.24 and Eq. 2.25, Eq. 2.26 is obtained where k is an integer number, $\sin\left(\Delta\omega\cdot T/4\right)\cong\Delta\omega\cdot T/4$ since $\Delta\omega\cdot T/4<\dfrac{\pi}{120}<<1$ and $k\cdot\omega+\Delta\omega\cong k\cdot\omega$ since $\Delta\omega<<k\cdot\omega$.

$$\sin\left(\lambda\right)-\sin\left(\theta\right)=2\sin\left(\frac{\lambda-\theta}{2}\right)\cdot\cos\left(\frac{\lambda+\theta}{2}\right) \qquad \text{Eq. 2.24}$$

$$\cos\left(\lambda\right)-\cos\left(\theta\right)=-2\sin\left(\frac{\lambda-\theta}{2}\right)\cdot\sin\left(\frac{\lambda+\theta}{2}\right) \qquad \text{Eq. 2.25}$$

$$\frac{\sin\left(k\cdot\omega t+\Delta\omega t+\theta_1\right)}{k\cdot\omega+\Delta\omega}\Bigg]_{t-T/2}^{t}=\frac{2\sin\left(\frac{\Delta\omega\cdot T}{4}\right)\cdot\cos\left(\begin{matrix}k\cdot\omega t+\Delta\omega t\\+\theta_1-\frac{\Delta\omega\cdot T}{4}\end{matrix}\right)}{k\cdot\omega+\Delta\omega}$$

Eq. 2.26

$$\cong\frac{\Delta\omega\cdot T\cdot\cos\left(\begin{matrix}k\cdot\omega t+\Delta\omega t\\+\theta_1-\frac{\Delta\omega\cdot T}{4}\end{matrix}\right)}{2k\cdot\omega}$$

By considering Eq. 2.26, Eq. 2.23 can be written as Eq. 2.27.

$$v_{grid,d}(t)\Big|_{dc}=\frac{V_{g1}}{2}\cdot\cos\left(\Delta\omega t+\theta_1\right)$$

$$-\underbrace{\frac{V_{g1}\cdot\Delta\omega}{4\omega}}_{X1}\cdot\cos\left(2\omega t+\Delta\omega t+\theta_1-\frac{\Delta\omega\cdot T}{4}\right)$$

Eq. 2.27

$$+\sum_{n=3,5,\ldots}\left[\begin{matrix}\underbrace{\frac{V_{gn}\cdot\Delta\omega}{2(n-1)\omega}}_{X3}\cdot\cos\left((n-1)\omega t+\Delta\omega t+\theta_1-\frac{\Delta\omega\cdot T}{4}\right)\\-\underbrace{\frac{V_{gn}\cdot\Delta\omega}{2(n+1)\omega}}_{X4}\cdot\cos\left((n+1)\omega t+\Delta\omega t+\theta_1-\frac{\Delta\omega\cdot T}{4}\right)\end{matrix}\right]$$

By following the same procedure, Eq. 2.28 to Eq. 2.31 are obtained for $v_{grid,q}(t)\Big|_{dc}$.

$$v_{grid,q}(t)\Big|_{dc} = \frac{2}{T}\cdot \int_{t-T/2}^{t} v_{grid,q}(t)\cdot dt =$$

$$= \frac{2}{T}\cdot \left(\begin{array}{l} \int_{t-T/2}^{t} \frac{V_{g1}}{2}\left[\underbrace{\sin\left(\Delta\omega t+\theta_1\right)}_{X1} + \sin\left(2\omega t+\Delta\omega t+\theta_1\right)\right]\cdot dt \\ \\ + \int_{t-T/2}^{t} \sum_{n=3,5,\ldots} \frac{V_{gn}}{2}\left[\begin{array}{l} \sin\left(\left(n-1\right)\omega t+\Delta\omega t+\theta_n\right) \\ +\sin\left(\left(n+1\right)\omega t+\Delta\omega t+\theta_n\right) \end{array}\right]\cdot dt \end{array}\right) \qquad \text{Eq. 2.28}$$

$$v_{grid,q}(t)\Big|_{dc} = \frac{2}{T}\cdot \left(\begin{array}{l} \frac{V_{g1}}{2}\cdot\sin\left(\Delta\omega t+\theta_1\right)\cdot\frac{T}{2} - \frac{\cos\left(2\omega t+\Delta\omega t+\theta_1\right)}{2\omega+\Delta\omega}\Big]_{t-T/2}^{t} \\ \\ -\sum_{n=3,5,\ldots}\frac{V_{gn}}{2}\left[\begin{array}{l} \frac{\cos\left(\left(n-1\right)\omega t+\Delta\omega t+\theta_1\right)}{\left(n-1\right)\omega+\Delta\omega}\Big]_{t-T/2}^{t} \\ \\ +\frac{\cos\left(\left(n+1\right)\omega t+\Delta\omega t+\theta_1\right)}{\left(n+1\right)\omega+\Delta\omega}\Big]_{t-T/2}^{t} \end{array}\right] \end{array}\right) \qquad \text{Eq. 2.29}$$

$$\frac{\cos\left(k\cdot\omega t+\Delta\omega t+\theta_1\right)}{k\cdot\omega+\Delta\omega}\Big]_{t-T/2}^{t} = \frac{-2\sin\left(\frac{\Delta\omega\cdot T}{4}\right)\cdot\sin\left(\begin{array}{l} k\cdot\omega t+\Delta\omega t \\ +\theta_1-\frac{\Delta\omega\cdot T}{4}\end{array}\right)}{k\cdot\omega+\Delta\omega} \qquad \text{Eq. 2.30}$$

$$\cong \frac{-\Delta\omega\cdot T\cdot\sin\left(\begin{array}{l} k\cdot\omega t+\Delta\omega t \\ +\theta_1-\frac{\Delta\omega\cdot T}{4}\end{array}\right)}{2k\cdot\omega}$$

$$v_{grid,q}(t)\Big|_{dc} = \frac{V_{g1}}{2}\cdot\sin\left(\Delta\omega t+\theta_1\right)$$

$$+\underbrace{\frac{V_{g1}\cdot\Delta\omega}{4\omega}}_{X2}\cdot\sin\left(2\omega t+\Delta\omega t+\theta_1-\frac{\Delta\omega\cdot T}{4}\right)$$

$$+\sum_{n=3,5,\ldots}\left[\begin{array}{l}\underbrace{\dfrac{V_{gn}\cdot\Delta\omega}{2(n-1)\omega}}_{X5}\cdot\sin\left((n-1)\omega t+\Delta\omega t+\theta_1-\dfrac{\Delta\omega\cdot T}{4}\right)\\ \\ +\underbrace{\dfrac{V_{gn}\cdot\Delta\omega}{2(n+1)\omega}}_{X6}\cdot\sin\left((n+1)\omega t+\Delta\omega t+\theta_1-\dfrac{\Delta\omega\cdot T}{4}\right)\end{array}\right] \qquad \text{Eq. 2.31}$$

As it is expressed in Eq. 2.27 and Eq. 2.31, $v_{grid,d}(t)\Big|_{dc}$ and $v_{grid,q}(t)\Big|_{dc}$ have low-frequency (i.e., $\Delta f = f/60$) and high-frequency (i.e., $2,4,...,n\times f$) sinusoidal components due to frequency variation ($\Delta\omega = 2\pi\cdot\Delta f$). However, it should be mentioned that terms X3 to X6 are negligible regarding terms X1 and X2 in Eq. 2.27 and Eq. 2.31. Therefore, Eq. 2.27 and Eq. 2.31 can be approximated as Eq. 2.32 and Eq. 2.33.

$$v_{grid,d}(t)\Big|_{dc} \cong \left[\frac{V_{g1}}{2}\cdot\cos\left(\Delta\omega t+\theta_1\right)-\frac{V_{g1}\cdot\Delta\omega}{4\omega}\cdot\cos\left(2\omega t+\Delta\omega t+\theta_1-\frac{\Delta\omega\cdot T}{4}\right)\right] \qquad \text{Eq. 2.32}$$

$$v_{grid,q}(t)\Big|_{dc} \cong \left[\frac{V_{g1}}{2}\cdot\sin\left(\Delta\omega t+\theta_1\right)+\frac{V_{g1}\cdot\Delta\omega}{4\omega}\cdot\sin\left(2\omega t+\Delta\omega t+\theta_1-\frac{\Delta\omega\cdot T}{4}\right)\right] \qquad \text{Eq. 2.33}$$

By substituting Eq. 2.32 and Eq. 2.33 in Eq. 2.18, Eq. 2.34 is obtained where term X1 is $\leq 7e^{-5}$ that can be absolutely neglected. With good approximation, it can be

assumed that terms X2 and X3 in Eq. 2.34, which are low-frequency components, are constant regarding terms X4 and X5, which are high-frequency components, within one line cycle. Therefore, by recalling Eq. 2.35, Eq. 2.34 can be expressed as Eq. 2.36 and Eq. 2.37 which shows that the calculated fundamental voltage amplitude has dc value plus a sinusoidal component with two times line frequency. According to Eq. 2.37, it can be pointed out that frequency variation doesn't affect the calculated fundamental voltage amplitude considerably.

$$V_{g1,calculated} = V_{g1} \cdot \sqrt{1 + \underbrace{\left(\frac{\Delta\omega}{2\omega}\right)^2}_{X1} + \frac{\Delta\omega}{\omega} \cdot \left[\underbrace{\sin\left(\Delta\omega t + \theta_1\right)}_{X2} \cdot \underbrace{\sin\left(\begin{matrix} 2\omega t + \Delta\omega t \\ +\theta_1 - \dfrac{\Delta\omega \cdot T}{4} \end{matrix}\right)}_{X4} - \underbrace{\cos\left(\Delta\omega t + \theta_1\right)}_{X3} \cdot \underbrace{\cos\left(\begin{matrix} 2\omega t + \Delta\omega t \\ +\theta_1 - \dfrac{\Delta\omega \cdot T}{4} \end{matrix}\right)}_{X5} \right]} \qquad \text{Eq. 2.34}$$

$$A\sin\left(2\omega t\right) + B\cos\left(2\omega t\right) = \sqrt{A^2 + B^2} \cdot \sin\left(2\omega t + \varphi\right) \qquad \text{Eq. 2.35}$$

$$V_{g1,calculated} = V_{g1} \cdot \sqrt{1 + \frac{\Delta\omega}{\omega}\left(\left[\underbrace{\begin{matrix} \sqrt{\sin\left(\Delta\omega t + \theta_1\right)^2} \\ + \\ \sqrt{\cos\left(\Delta\omega t + \theta_1\right)^2} \end{matrix}}_{=1} \right] \cdot \sin\left(2\omega t + \Delta\omega t + \varphi\right) \right)} \qquad \text{Eq. 2.36}$$

$$V_{g1,calculated} = V_{g1} \cdot \sqrt{1 + \frac{\Delta\omega}{\omega} \cdot \sin\left(2\omega t + \Delta\omega t + \varphi\right)} \qquad \text{Eq. 2.37}$$

It is worth mentioning that Eq. 2.19 to Eq. 2.37 are provided to prove the proper operation of the proposed method under deviation of line-frequency and so, they are not part of proposed method and are not required to be used for implementation. Only Eq. 2.9, Eq. 2.10, Eq. 2.15, Eq. 2.16, and Eq. 2.18 are used to implement the method in simulation and experiments. In addition, flow chart of the proposed method is illustrated in Figure 2.1 in which $t_{current}$ is current time coming from DSP timer. As shown in Figure 2.1, part of proposed method has been modified due to instability of method during PJ cases which will be explained in detail in Section 2.6.2.

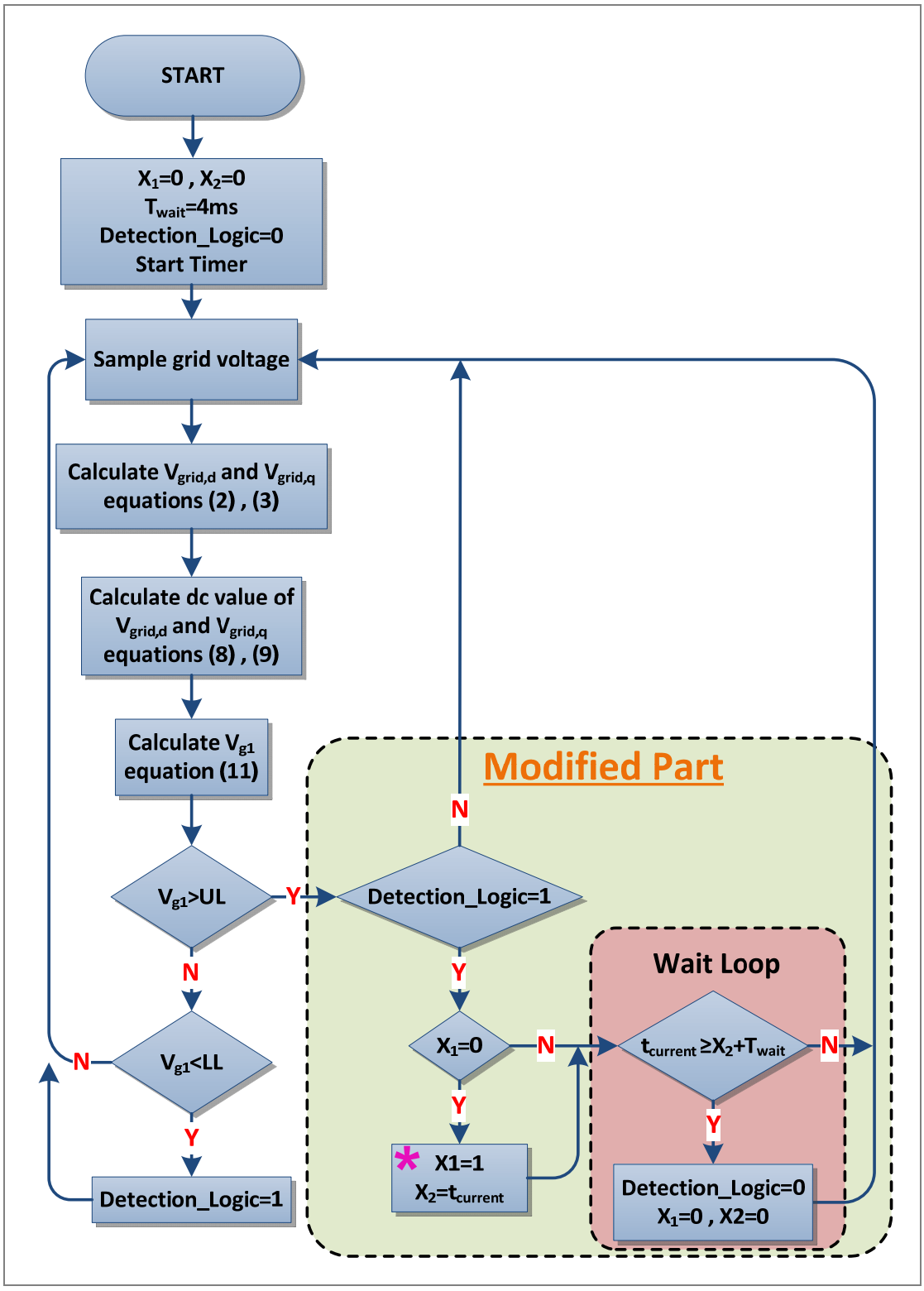

Figure 2.1. Flow chart of proposed voltage sag detection method.

2.5. Simulation Results

Following, two detection methods which are discussed in Section 2.4 of this chapter are simulated and simulation results are provided.

2.5.1. Non-Harmonic Voltage Sag Detection Method

This method is simulated in PSIM software to test its performance under various conditions such as different amount of VSD (between 12% to 50%) and different amount of POW (between 0° to 180°). It should be mentioned that negative POWs (between -180° to 0°) will have the same effect and result on DT as the positive ones; thus, only the positive POWs are considered. The reason is that the final step of the calculation process is to obtain the square of the α- and β-components. For example, if the POW is -60°, its effect is the same as that when the POW is 120° besides inverting the signal.

Thus, herein only the positive POWs are considered. In this subsection, two case studies are illustrated in Figure 2.2 and Figure 2.3 where VS is 12% and 50%, respectively. The nominal voltage V_g is $110\sqrt{2}V$ and the line frequency is 60 Hz. The 1st to 5th POWs in both Figure 2.2 and Figure 2.3 are 0, 30, 90, 120 and 160 degrees, which have been selected based on obtained results of numerous conducted tests to show the best and worst time response of proposed voltage sag detection method. According to results of numerous case studies as well as the illustrated ones, the proposed method can detect the voltage sag in less than 0.2 ms, no matter how much the VS or POW is, which is much faster than the methods reported in the literature. Moreover, the detected amplitude doesn't have any ripple, which ensures very precise detection. However, no harmonic is considered here

since only performance of the method itself is investigated without considering the low-pass filter effect. Existence of any harmonic results in adding suitable low-pass filter tuned properly to eliminate any available harmonic.

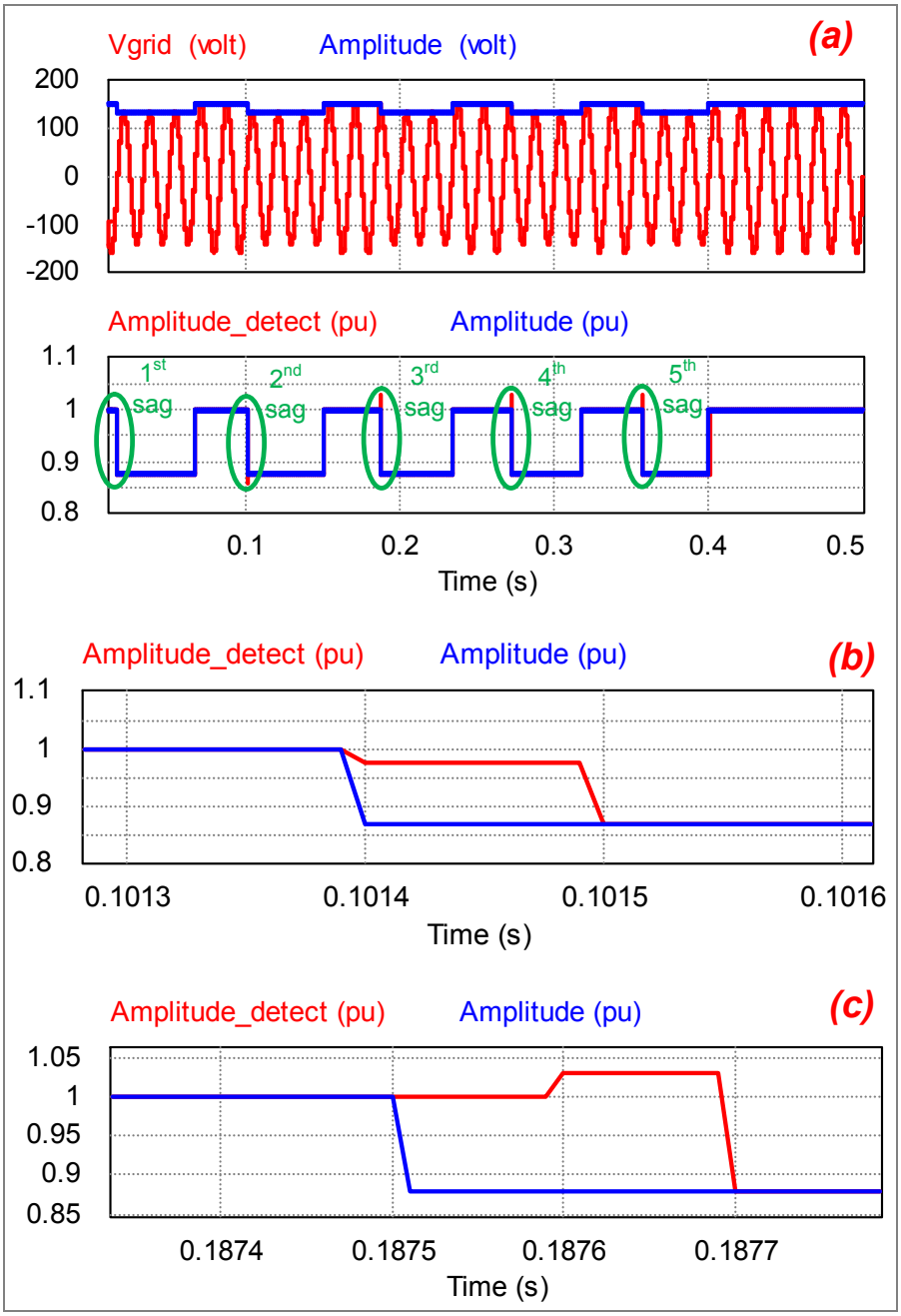

Figure 2.2. Simulation result of VS=12% for different amount of POW with line-frequency of 60 Hz: (a) grid voltage, its amplitude and detected amplitude with proposed method; (b) & (c) more detailed view.

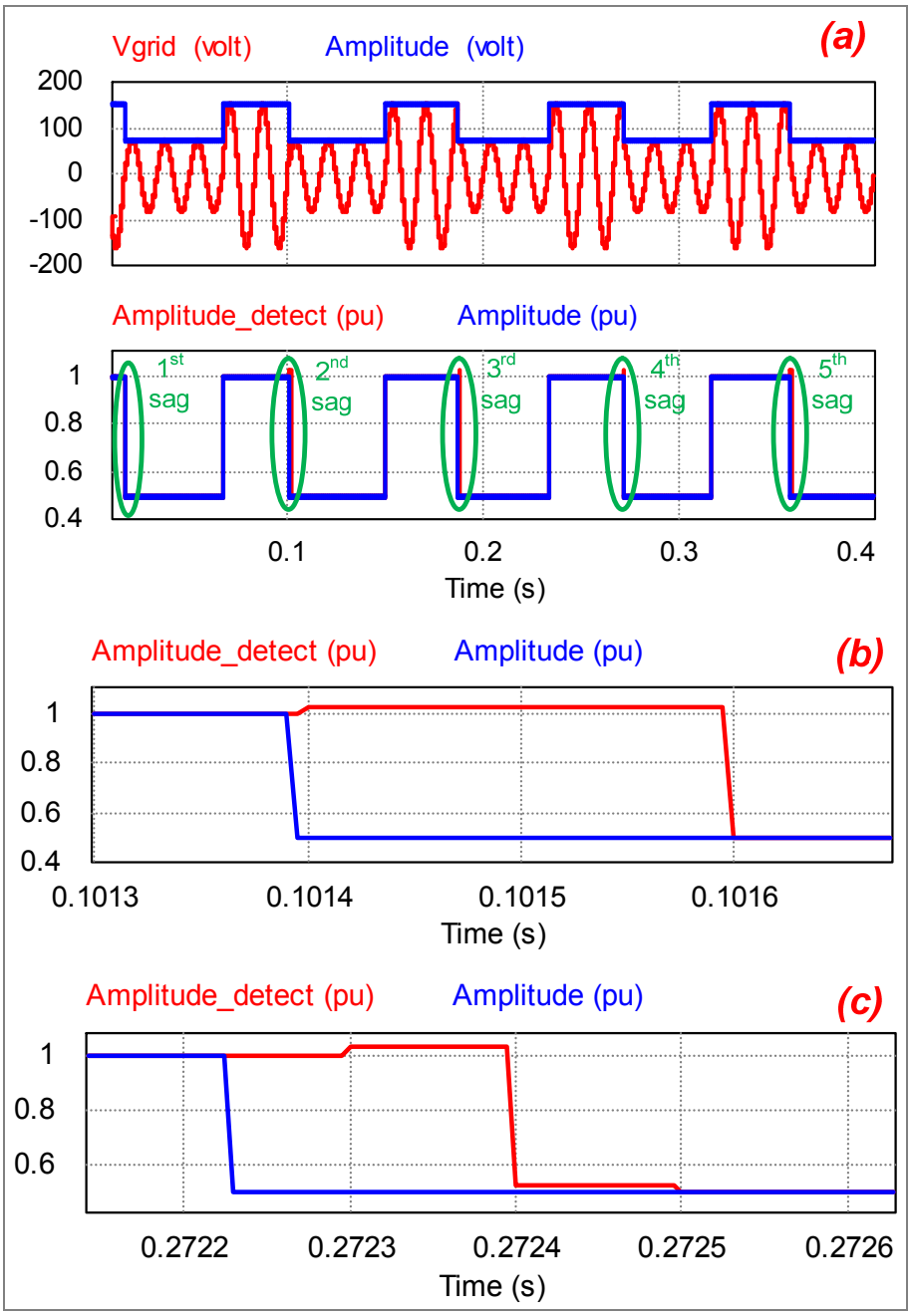

Figure 2.3. Simulation result of VS=50% for different amount of POW with line-frequency of 60 Hz: (a) grid voltage, its amplitude and detected amplitude with proposed method; (b & c) more detailed view.

2.5.2. Harmonically-Distorted Voltage Sag Detection Method

This method is simulated in PSCAD to test its performance considering harmonic distortion under various conditions such as different amounts of VSD (between 10% to 90%), different amounts of POW (between 0° to 180°) and different amount of PJ (between -30° to $+30^\circ$). It should be mentioned that negative POWs (between -180° to 0°) will have the same effect and result on DT as the positive ones; thus, only the positive POWs are considered. The fundamental component (V_{g1}) is $110\sqrt{2}V$ and the line frequency is 60 Hz. According to the obtained results, the best and worst DTs of proposed method are 1 and 8 ms, respectively. Moreover, the calculated amplitude doesn't have any ripple which ensures precise detection even if the voltage is highly distorted. However, a few case studies are illustrated in Figure 2.4 to Figure 2.7 where the VSD is 10%, 40%, 40% and 90%, respectively; also, different amounts of POW are considered. In Figure 2.4 and Figure 2.5, V_{g5}, V_{g7}, and V_{g11} are 10% of the fundamental component and in Figure 2.6 and Figure 2.7, V_{g3}, V_{g7}, and V_{g13} are 15%, 10% and 10% of the fundamental component, respectively. It is worth mentioning that the individual harmonic limit is 3% and THD limit is 5% determined by standards such as IEC STD 61000-3-6 and IEEE STD 519. However, the amount of harmonic distortion implemented in the conducted studies is way beyond of harmonic distortion limits determined by standards. According to results of numerous case studies as well as illustrated ones, the proposed method can detect the voltage sag precisely within half cycle, no matter how much the VSD, POW or distortion is. Moreover, the method is tested for frequency variation case to verify the analytical investigation resulted in Eq. 2.32 and Eq. 2.33 in Section 2.4.2. As shown in Figure 2.8

and Figure 2.9 in which VSD is 10% and $\Delta f = -1\,\text{Hz} = -f/60$ and $\Delta f = +1\,\text{Hz} = +f/60$, respectively, there is exact match between Eq. 2.32 and Eq. 2.33 and obtained simulation result related to calculated dc value of d- and q-components which have a low-frequency ($|\Delta f| = 1\,\text{Hz}$) sinusoidal component with amplitude of 0.45pu and high-frequency ($2f = 120\,\text{Hz}$) sinusoidal component with amplitude around 0.00375pu.

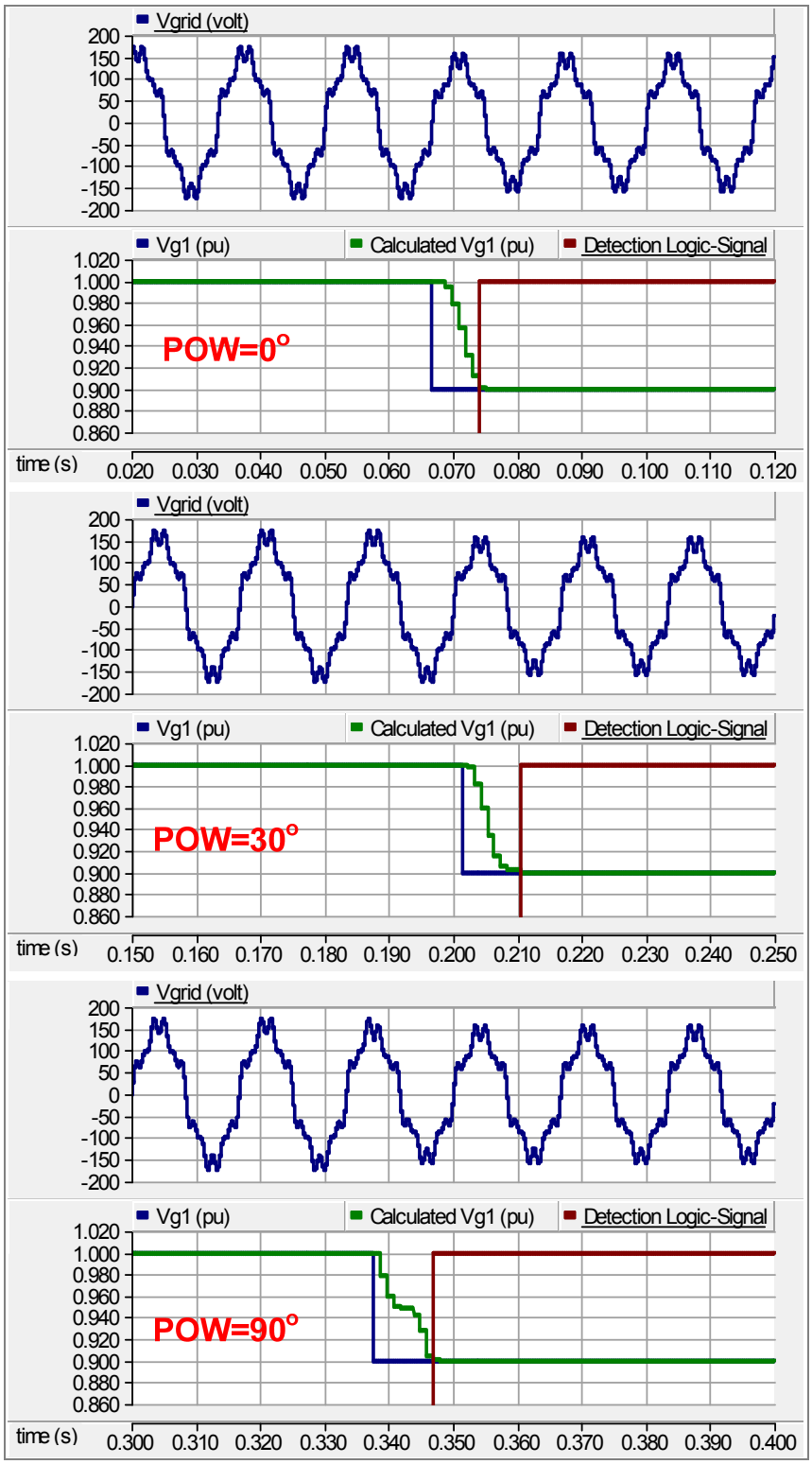

Figure 2.4. Simulation result of 10% VSD for different amounts of POW, $V_{g5} = V_{g7} = V_{g11} = 0.1V_{g1}$: grid voltage, its amplitude (pu), calculated amplitude (pu) and detection logic-signal.

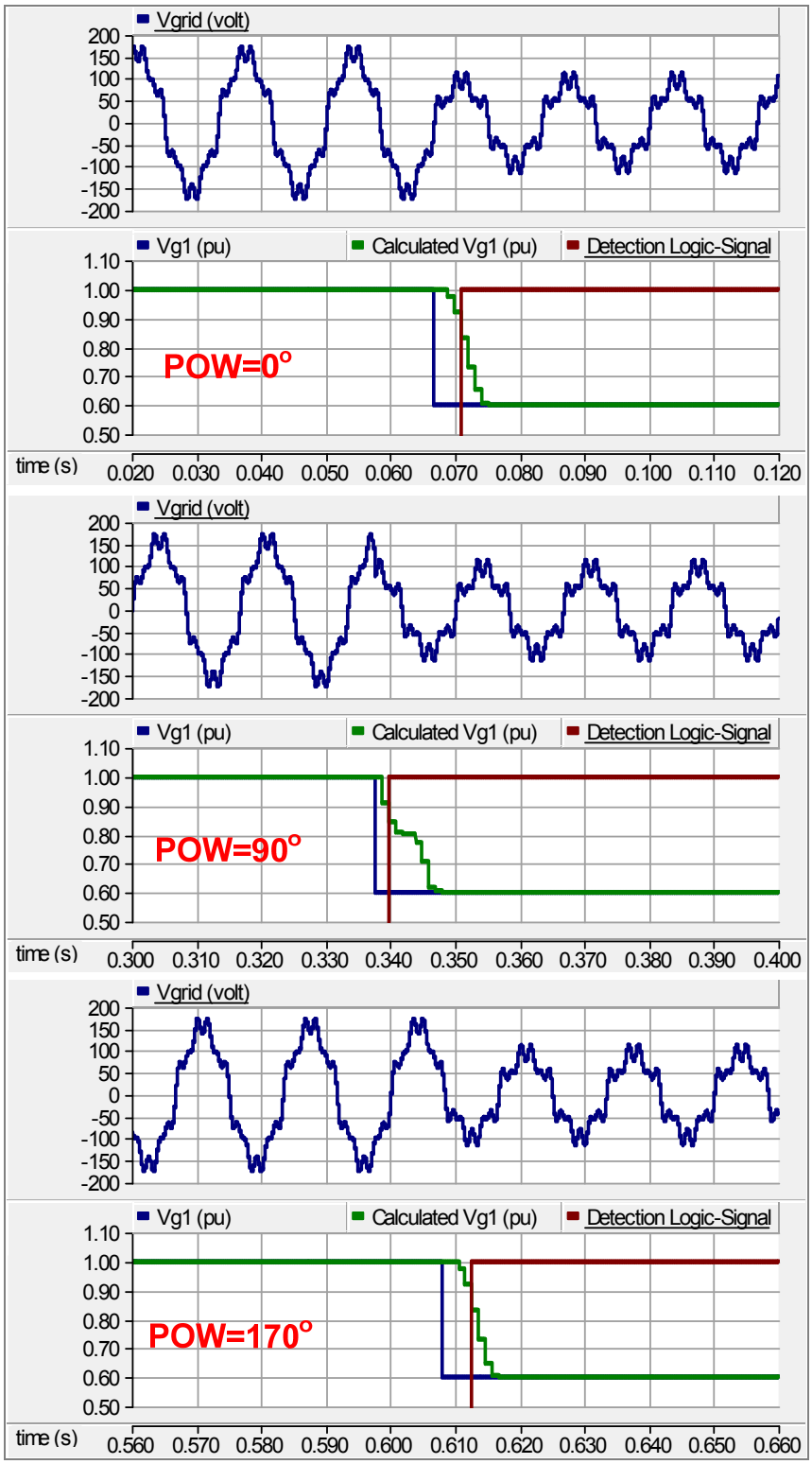

Figure 2.5. Simulation result of 40% VSD for different amounts of POW, $V_{g5} = V_{g7} = V_{g11} = 0.1V_{g1}$: grid voltage, its amplitude (pu), calculated amplitude (pu) and detection logic-signal.

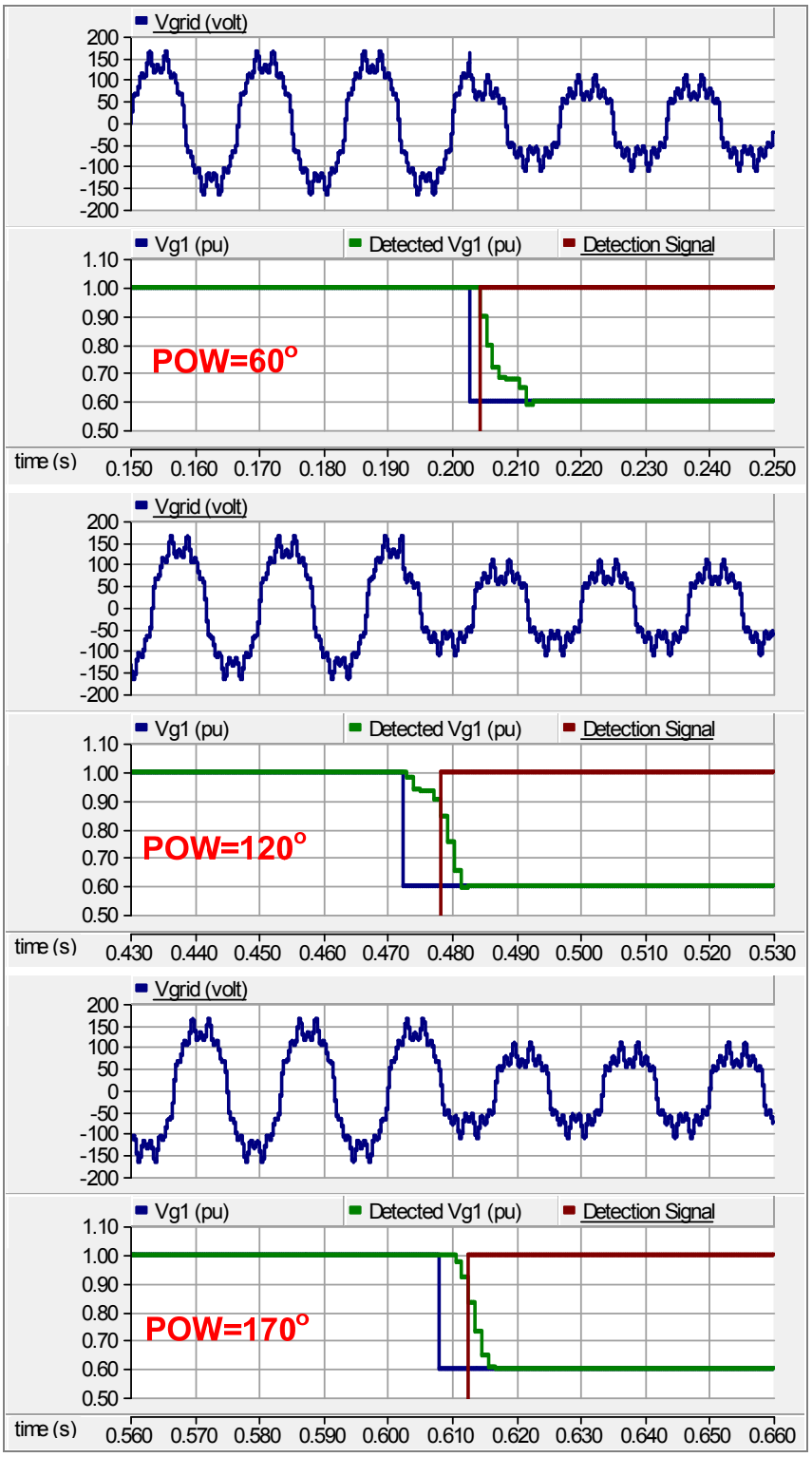

Figure 2.6. Simulation result of 40% VSD for different amounts of POW, $V_{g3} = 0.15V_{g1}$ and $V_{g7} = V_{g13} = 0.1V_{g1}$: grid voltage, its amplitude (pu), calculated amplitude (pu) and detection logic-signal.

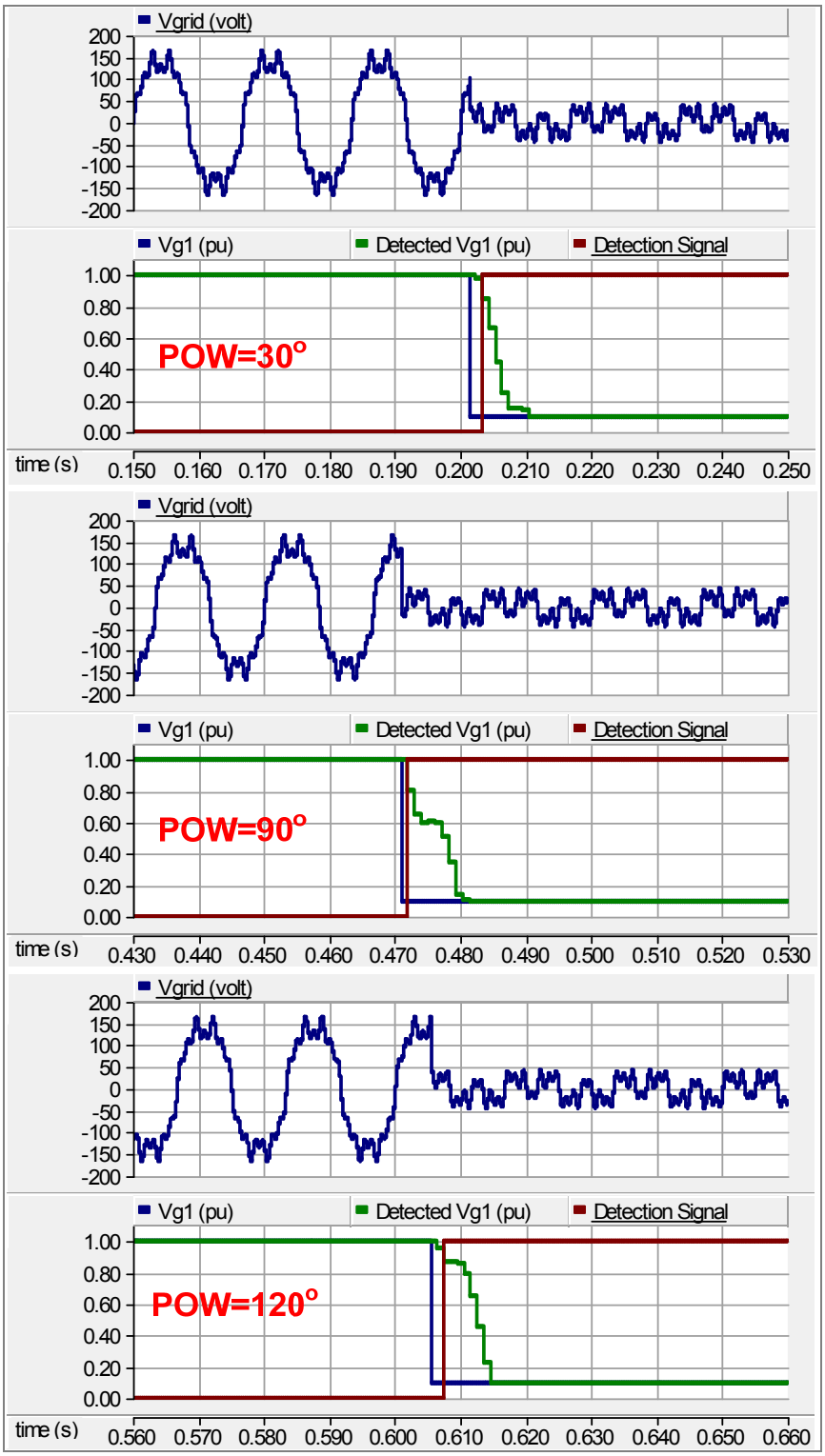

Figure 2.7. Simulation result of 90% VSD for different amounts of POW, $V_{g3} = 0.15V_{g1}$ and $V_{g7} = V_{g13} = 0.1V_{g1}$: grid voltage, its amplitude (pu), calculated amplitude (pu) and detection logic-signal.

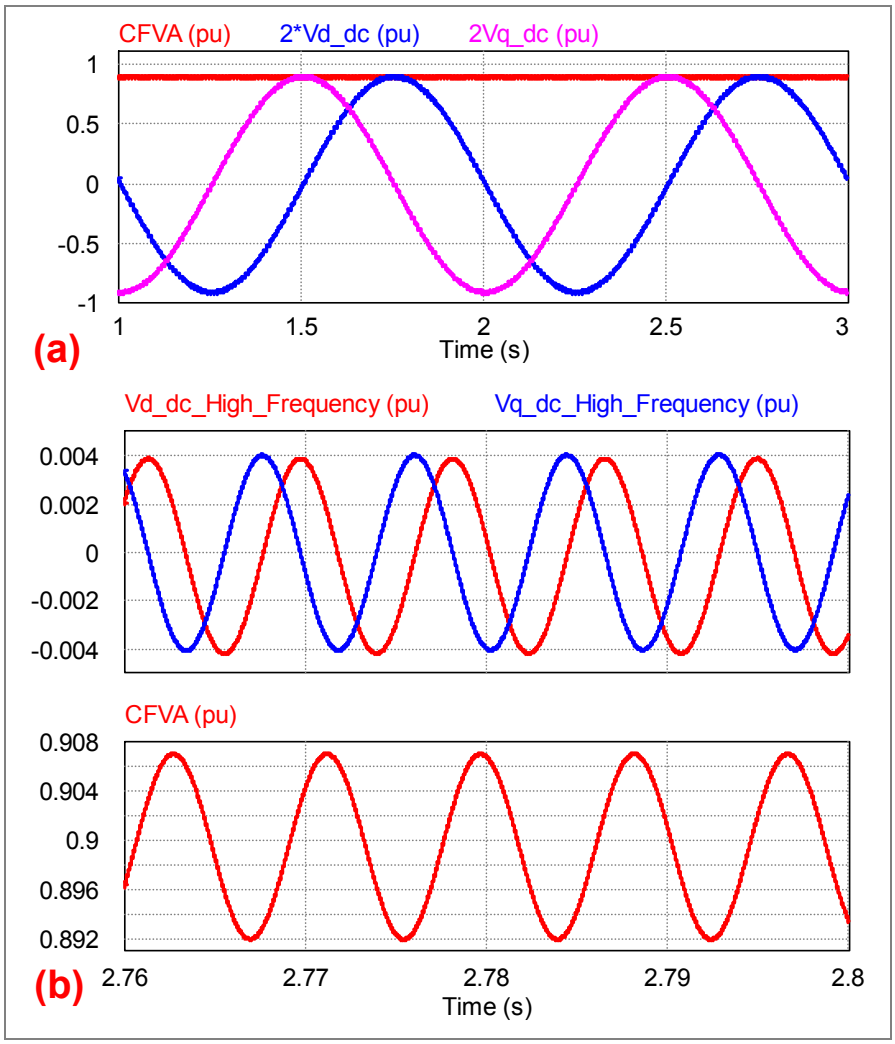

Figure 2.8. Simulation result at steady state for VSD of 10% and line frequency of 59Hz: (a) dc value of d- and q-component as well as calculated fundamental voltage amplitude (CFVA); (b) high-frequency components.

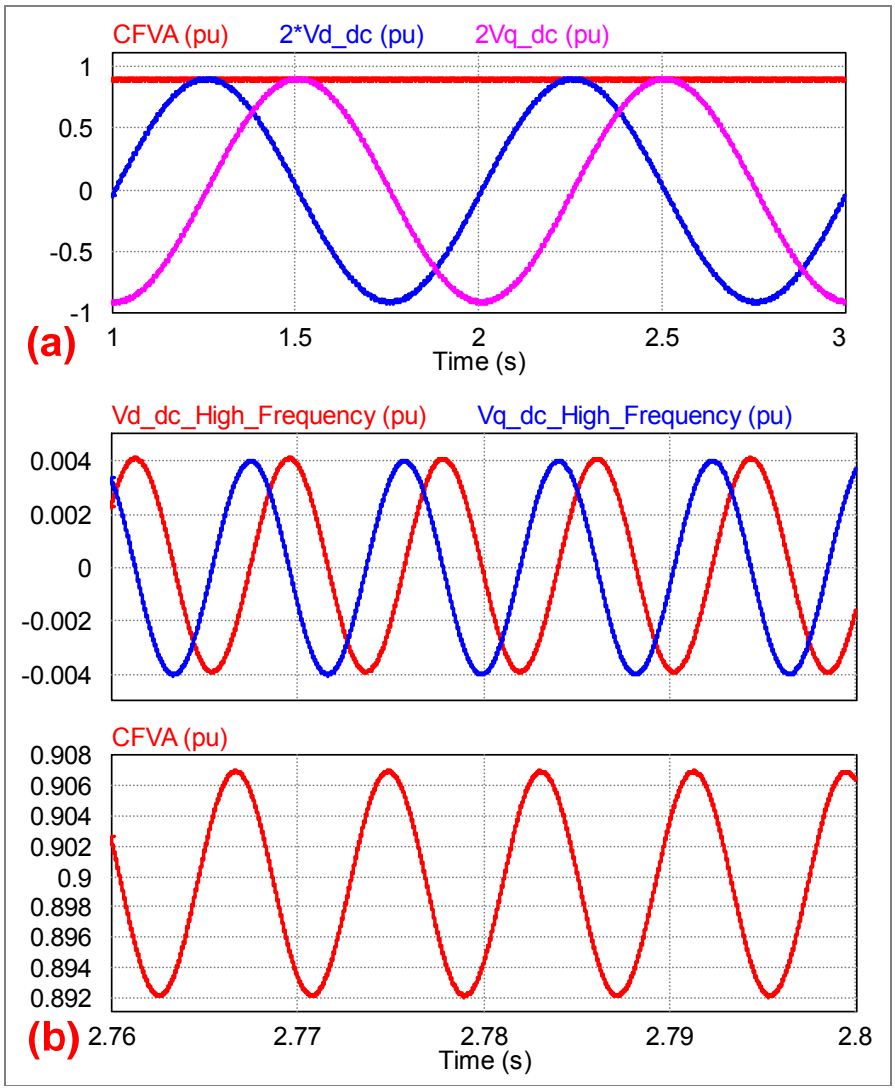

Figure 2.9. Simulation result at steady state for VSD of 10% and line frequency of 60Hz: (a) dc value of d- and q-component as well as calculated fundamental voltage amplitude (CFVA); (b) high-frequency components.

2.6. Experimental Results

Following, two detection methods which are discussed in Section 2.4 of this chapter are implemented in DSP F28335 and numerous experimental results have been obtained. The signal which is assumed as scaled grid voltage is produced by the PWM channel of the DSP at 120kHz rate. The produced signal after filtering out the high-frequency harmonics (120, 240, … kHz) by a low-pass RC filter is sampled at 3 kHz by the ADC channel of the DSP to analyze the voltage sag. It is worth mentioning that producing the scaled grid voltage by DSP gives a great flexibility to make any kind of voltage sag exactly at the predetermined harmonic distortion, VSD, POW and PJ. In addition, this approach causes to have the logic signal showing the start time of voltage sag which makes it easy to measure how long it takes for the proposed method to detect the voltage sag regarding that reference time. Hereinafter in all experimental results, the scaled voltage signal is blue, start time of voltage sag is purple, detection logic-signal is cyan and time delay between cyan and purple waveforms is DT. For the harmonic distortion situation, three cases are considered in; the first case: V_{g5}, V_{g7}, and V_{g11} are 10% of the fundamental component; the second case: V_{g3} and V_{g7} are 10% of the fundamental component; and the third case: V_{g3} and V_{g5} are 15% of the fundamental component. It is worth mentioning that the individual harmonic limit is 3% and THD limit is 5% determined by standards such as IEC STD 61000-3-6 and IEEE STD 519. However, the amount of harmonic distortion implemented in the conducted studies is way beyond of harmonic distortion limits determined by standards. The default case of harmonic distortion is the first case in which V_{g5}, V_{g7} and V_{g11} are 10% of the fundamental

component and the default value of line frequency is 60Hz unless it is stated.

2.6.1. Non-Harmonic Voltage Sag Detection Method

This method is tested under various conditions and numerous results are obtained; however, only some of them under the normal condition of the line-frequency (*i.e.*, 60 Hz) with VSD of 12% and 50% are illustrated in Figure 2.10 and Figure 2.11, respectively, for different amount of POW. As it can be pointed out, the best and worst detection time of proposed method is 0.26 and 0.68 ms, respectively; it means that the proposed method can detect any voltage sag, no matter how much the VSD or POW is, in less than 0.7 ms, which is much faster than the methods reported in the literature. It should be mentioned that the reason for late detection time in experimental results in comparison with simulation results is that a low-pass RC filter is implemented at output of the PWM channel of the DSP. Consequently, added filter causes a delay of voltage sag while in the simulation there is not such a filter to cause delay and thus, voltage drops immediately at predetermined POW in simulation.

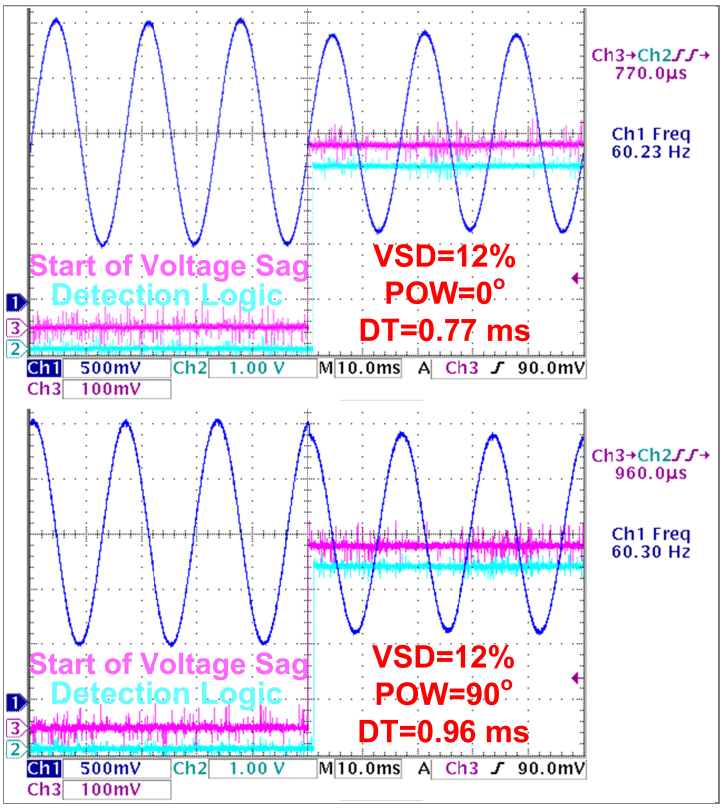

Figure 2.10. Experimental result of 12% VSD for different amounts of POW with line-frequency of 60 Hz.

Another important parameter which should be considered during the performance evaluation of any voltage sag detection method is the error between the calculated fundamental voltage amplitude and actual fundamental voltage amplitude as well as the ripple of calculated fundamental voltage amplitude. To show the error of this method and the amount of ripple, the fundamental voltage amplitude calculated by DSP (data are acquired from DSP memory) for different amount of VSD equals 0% (*i.e.*, normal condition) and 30% are illustrated in Figure 2.12 and Figure 2.13, respectively. It can be pointed out that the calculated fundamental voltage amplitude has maximum of ±1% ripple in different experiment case studies, which can be considered as precise detection. Moreover, the proposed method is studied under $+1\,Hz$ and $-1\,Hz$ frequency variation

(standards require $\pm 0.6\,Hz$) and the obtained results are illustrated in Figure 2.14 and Figure 2.15, respectively, to show its performance. As it can be seen, the proposed method has satisfactory results of voltage sag detection under frequency variation condition. In addition, the fundamental voltage amplitude calculated by DSP (data are acquired from DSP memory) for 0% VSD under frequency variation of $+1\,Hz$ is illustrated in Figure 2.16. It can be stated that the calculated fundamental voltage amplitude under frequency variation has maximum of $\pm 1.5\%$ ripple.

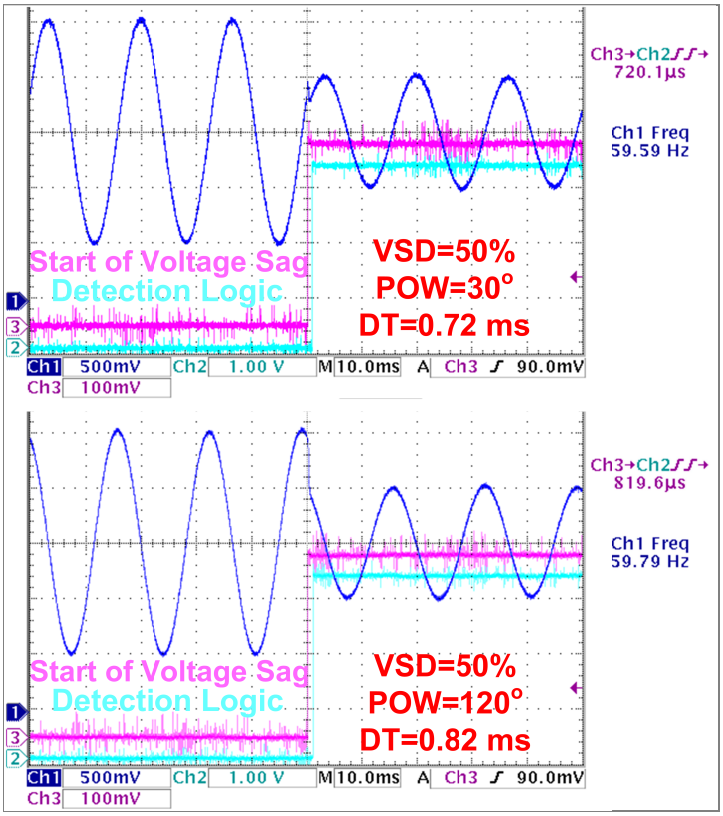

Figure 2.11. Experimental result of 50% VSD for different amounts of POW with line-frequency of 60 Hz.

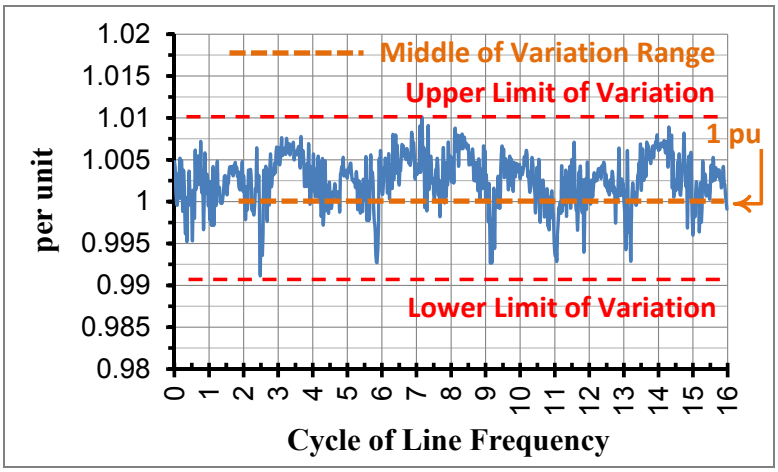

Figure 2.12. Fundamental voltage amplitude calculated by DSP for 0% VSD with line-frequency of 60 Hz.

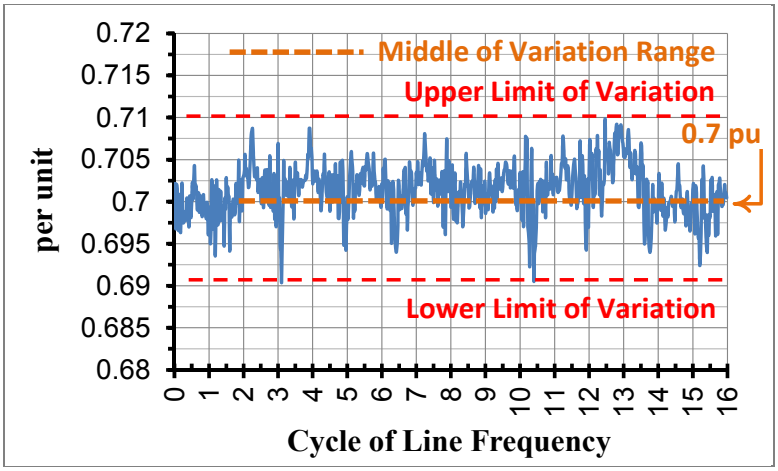

Figure 2.13. Fundamental voltage amplitude calculated by DSP for 30% VSD with line-frequency of 60 Hz.

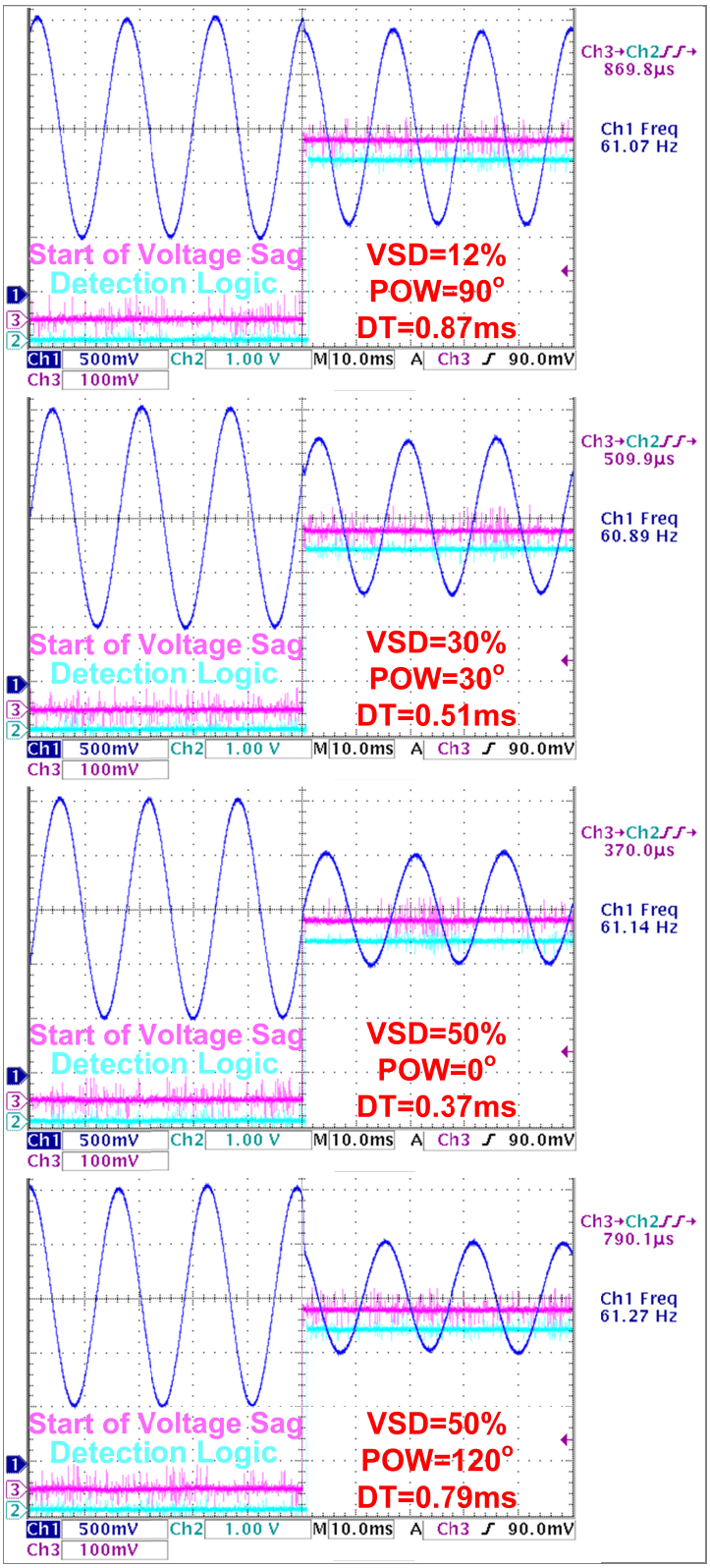

Figure 2.14. Experimental result of for different amounts of VSD and POW with line-frequency of 61 Hz.

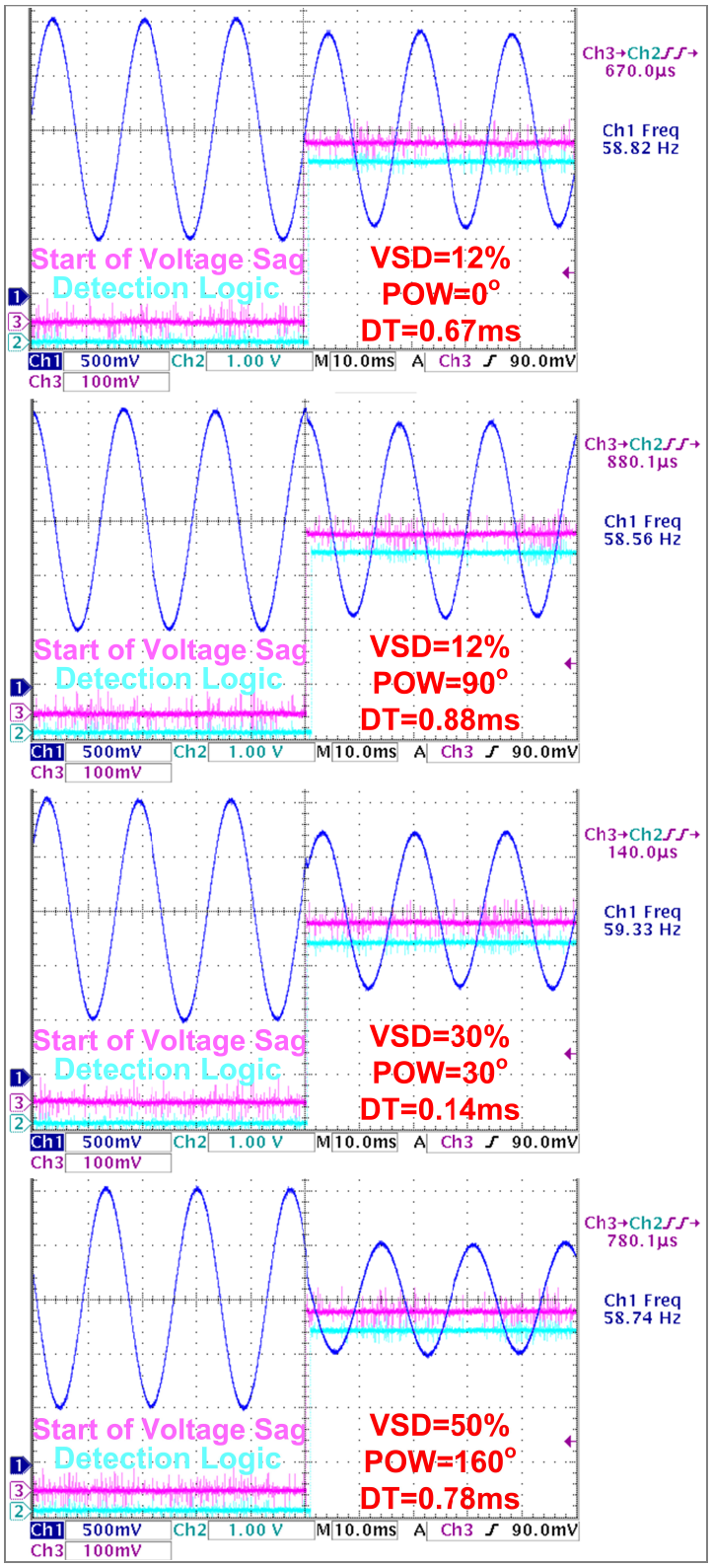

Figure 2.15. Experimental result of for different amounts of VSD and POW with line-frequency of 59 Hz.

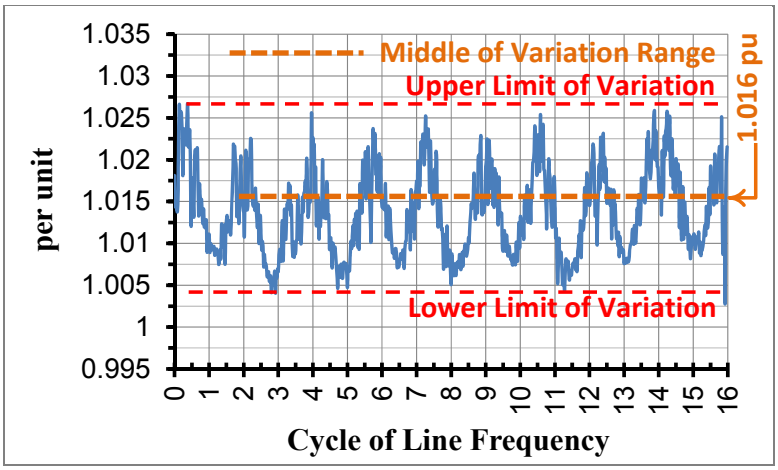

Figure 2.16. Fundamental voltage amplitude calculated by DSP for 0% VSD with line-frequency of 61 Hz.

2.6.2. Harmonically-Distorted Voltage Sag Detection Method

The method is tested for long-time VSD of 10% for non-harmonic condition and all three cases of harmonic distortion. The ripple amount of calculated fundamental voltage amplitude during the experiments is acquired from DSP memory. The middle of the variation range (ripple) of calculated fundamental voltage amplitude is defined as calculated fundamental voltage amplitude and the hysteresis band of threshold comparator is defined based on the ripple amount. The hysteresis band between the upper limit (UL) and lower limit (LL) is greater than two times the biggest ripple which is recorded during the tests. In this case, if the calculated fundamental voltage amplitude decreases to lower than the LL, the detection logic-signal will be activated and if the calculated fundamental voltage amplitude increases to higher than the UL, the detection logic-signal will be deactivated. According to IEC 61000-4-30 and IEEE 1564, the LL of hysteresis threshold comparator to trigger the detection logic-signal should be 90% of grid nominal voltage to recognize the events as voltage sag. According to obtained results, variation range (ripple)

as well as middle of variation range was almost the same in all cases. Here, the obtained results of fundamental voltage amplitude calculated by DSP (data are acquired from DSP memory) are illustrated in Figure 2.17. For the case of line frequency variation, the proposed method is tested for $\pm 1\,Hz$ variation for 60Hz line frequency (standards require $\pm 0.6\,Hz$) together with considering three different harmonic distortion cases mentioned previously. Since variation range (ripple) of calculated fundamental voltage amplitude were almost the same for different harmonic distortion cases, only results of first harmonic distortion case (V_{g5}, V_{g7}, and V_{g11} are 10% of the fundamental component) are illustrated in Figure 2.18 for 61Hz and 59Hz line frequency.

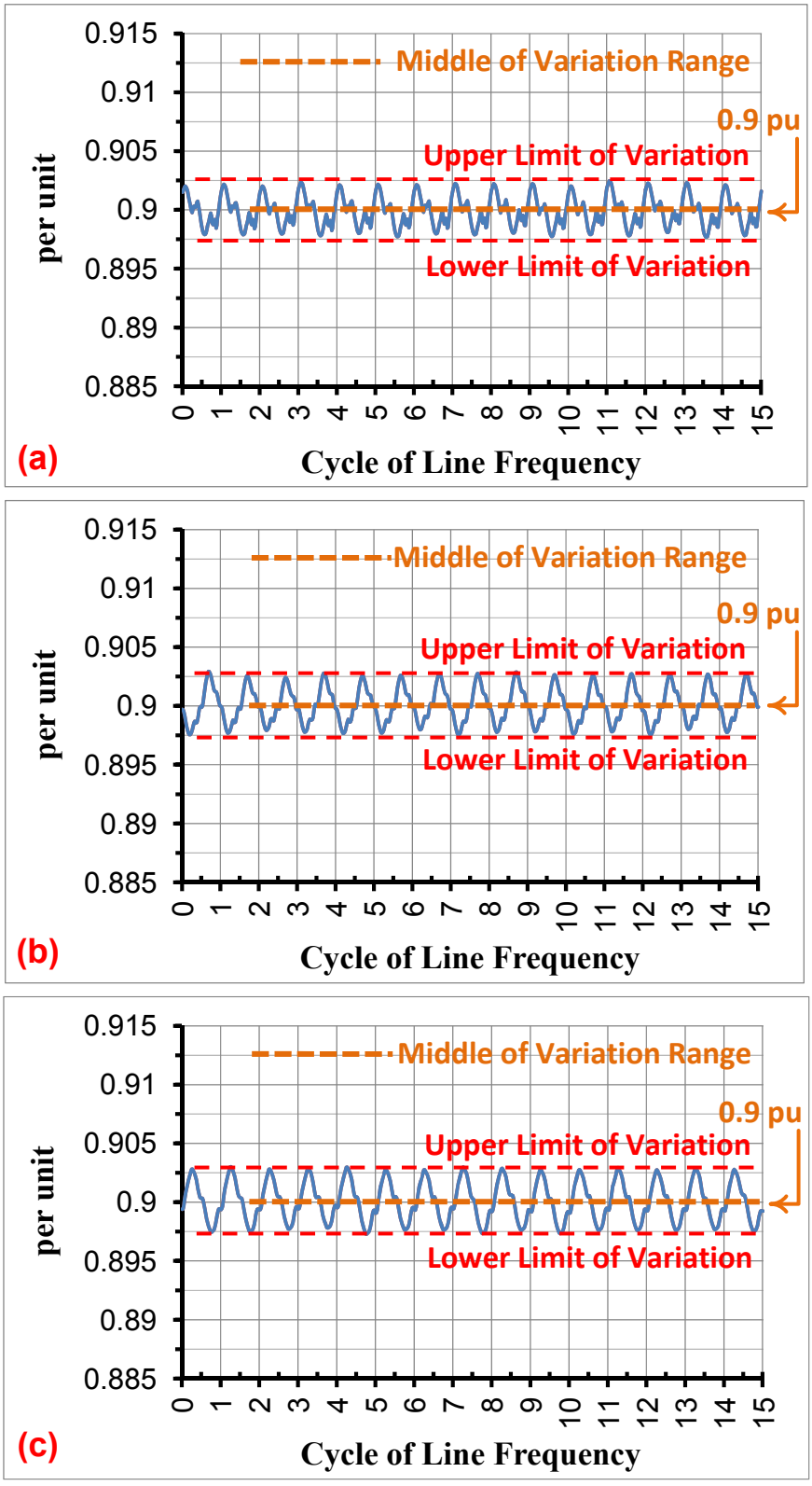

Figure 2.17. Fundamental voltage amplitude calculated by DSP for 10% VSD with line-frequency of 60 Hz for harmonic distortion of: (a) first case; (b) second case; (c) third case.

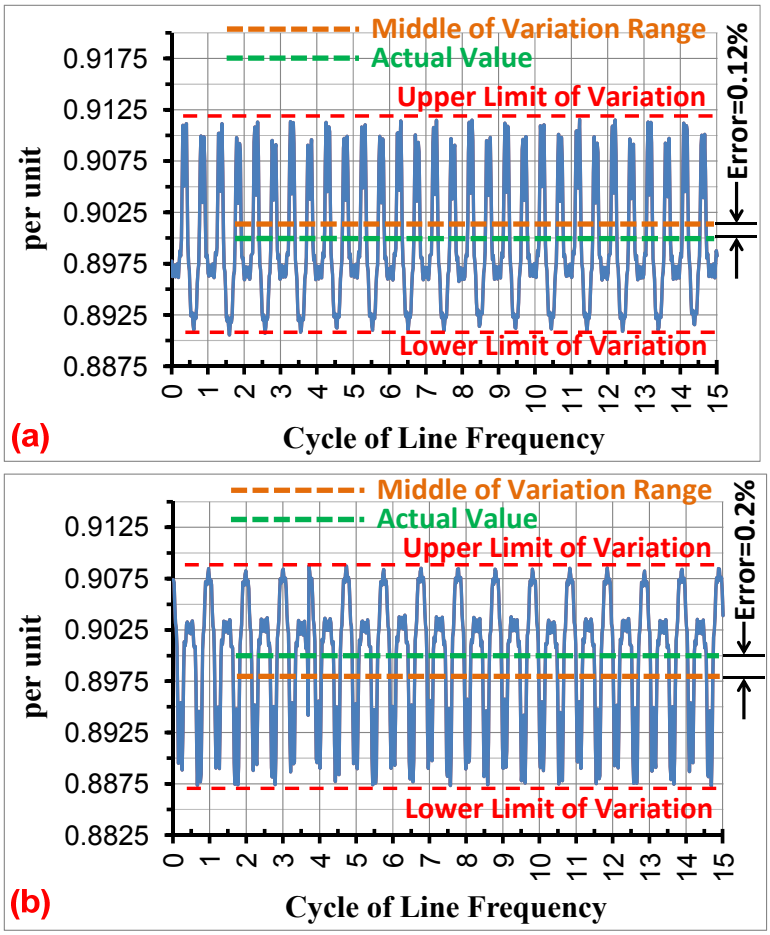

Figure 2.18. Fundamental voltage amplitude calculated by DSP for 10% VSD with line-frequency of: (a) 61 Hz; (b) 59 Hz.

According to numerous obtained results and illustrated ones in Figure 2.17 and Figure 2.18, it can be pointed out that the calculated fundamental voltage amplitude in different experiment case studies considering excessive-harmonic distortion has maximum ripple of ±0.3% in normal condition of line frequency and ±1% in the case of $\pm 1Hz$ variation of 60Hz line frequency. Moreover, the proposed method has almost zero error between the calculated fundamental voltage amplitude (middle of variation range) and actual fundamental voltage amplitude in normal condition of line frequency and maximum of ±0.25% in case of line frequency variation. Therefore, the proposed method can be

considered as a precise method. Herein, the zero error means that the error is too small which can be easily neglected. Based on the obtained result, the hysteresis band of threshold comparator needs to be more than 2% (two time the worst case ripple which is related to $\pm 1 Hz$ line frequency variation) while it has been selected to be 2.2%. Consequently, the UL and LL of hysteresis threshold comparator will be 92.2% and 90%, respectively. Such selection for the UL and LL will cause that the method has a stable operation for the mentioned cases of non-harmonic condition, harmonic distortion and line frequency variation for different POWs (0° to 360° of line cycle). Figure 2.19 shows the detection logic-signal with hysteresis threshold comparator for VSD of 10.5% and line frequency of 61Hz.

As shown in Figure 2.19(a), the detection method will have the unstable performance without the hysteresis threshold comparator. This verifies the necessity of the hysteresis threshold comparator in any detection method and its result is shown in Figure 2.19(b). Moreover as show in Figure 2.20, the method will have an unstable operation in the cases of PJ with hysteresis band of 2.2%. The reason, as shown in Figure 2.20(b), is that the calculated fundamental voltage amplitude after the moment of sag event including the -30° PJ has a large overshoot and undershoot until it reaches to steady state. To avoid this phenomenon causing short-period instability of detection method, the method is modified and the modified part is highlighted in Figure 2.1. The modified method will activate the detection logic-signal immediately if the calculated fundamental voltage amplitude decreases and crosses the LL. On the other hand, the modified method will not deactivate the detection logic-signal immediately if the calculated fundamental voltage amplitude increases and crosses the UL; whenever the

calculated fundamental voltage amplitude increases and crosses the UL, it will wait for 4ms (T_{wait}) and will check the calculated fundamental voltage amplitude after 4ms. If it is less than UL it will keep the detection logic-signal at high logic-level otherwise it will deactivate it. The role of X1 in Figure 2.1 is to enable the 4ms wait time. To do this, it is required to store the current time of the timer ($t_{current}$) once the V_{g1} exceed the UL and the Detection_Logic was 1 before this exceeding. At this moment (the related box is marked with violet star in Fig. 1), the $t_{current}$ is saved into X2 and the X1 is activated to confirm in the next loop of flowchart (if the V_{g1} is still above the UL) that the $t_{current}$ is already saved into X2 and the algorithm already started the 4ms wait time. Otherwise, the $t_{current}$ will be saved in X2 in each loop of flowchart and the algorithm will not be able to finish the 4ms wait time loop. With this modification, the method will not have any unstable operation in the cases of PJ as shown in Figure 2.21 as an example. The 4ms for T_{wait} (shown in Figure 2.1) is figured out to be suitable during the experiments and had a no-failure performance for excessive experiments for different amounts of PJ and VSD.

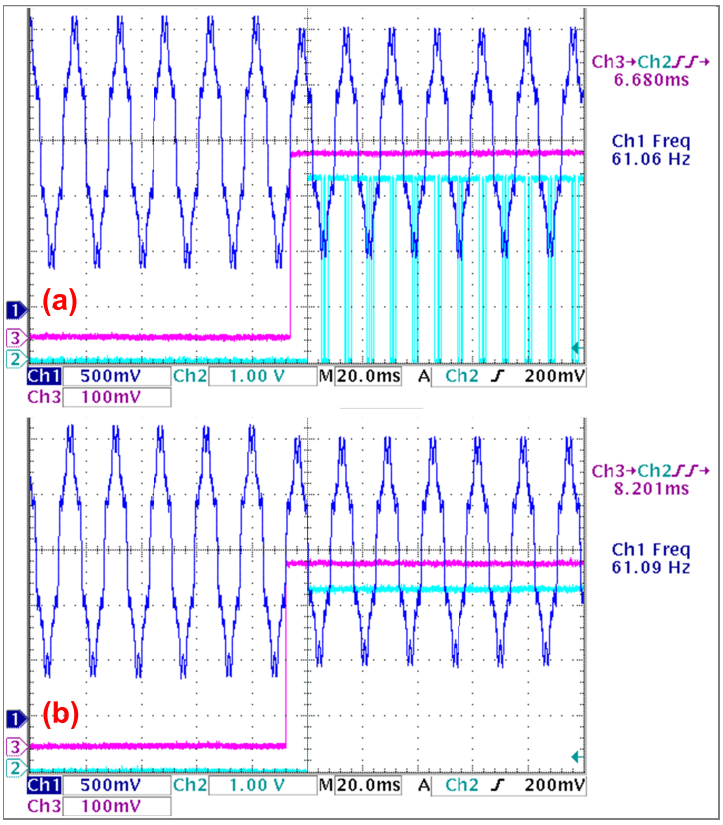

Figure 2.19. Experimental result: VSD of 10.5% with line-frequency of 61Hz and first case of harmonic distortion using the hysteresis threshold comparator.

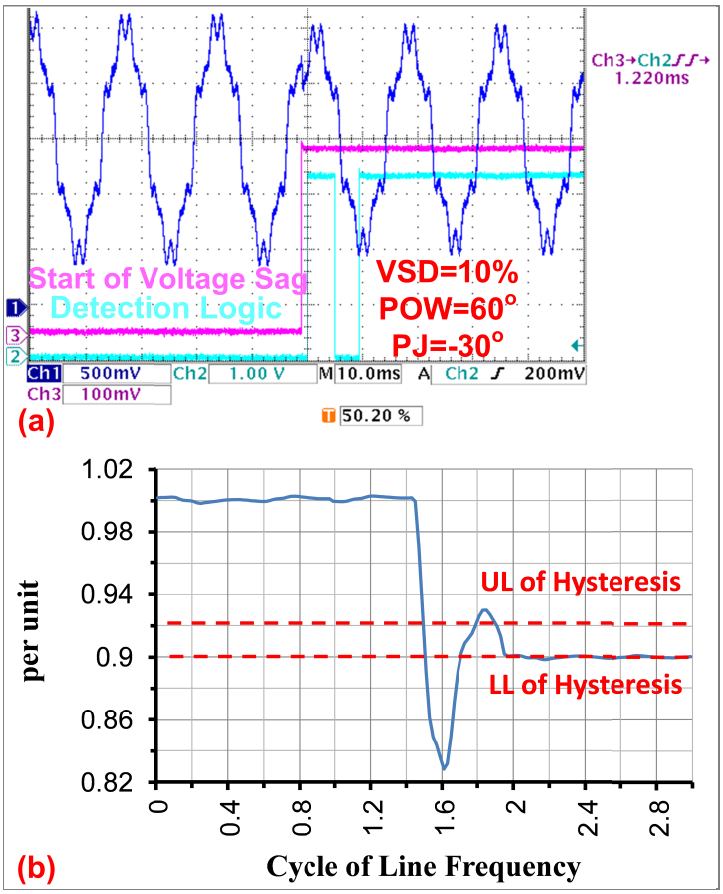

Figure 2.20. Instability of method for VSD of 10%, POW of 60° and PJ of -30° with line-frequency of 60Hz and first case of harmonic distortion: (a) experimental result; (b) fundamental voltage amplitude calculated by DSP.

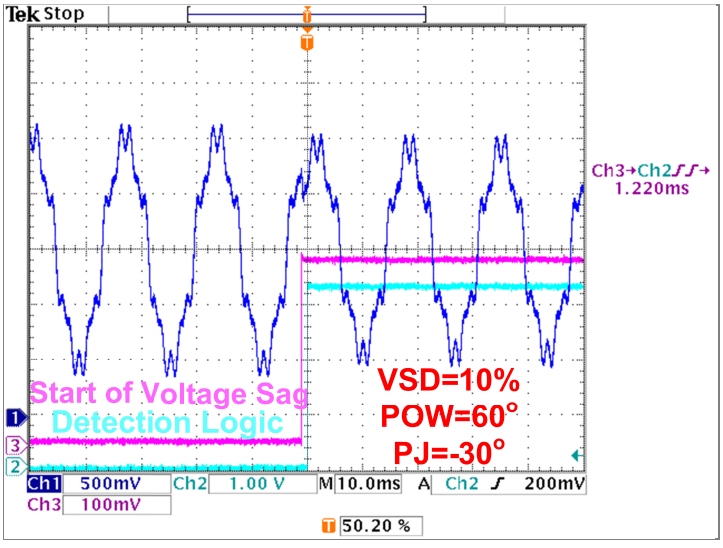

Figure 2.21. Experimental result: stability of modified method for VSD of 10%, POW of 60° and PJ of -30° with line-frequency of 60Hz and first case of harmonic distortion.

After defining the UL (92.2%) and LL (90%) of hysteresis threshold comparator and modifying the method due to the PJ cases instability, the method is tested excessively for long-time and transient sags for all cases of different VSDs, POWs, PJs, harmonic distortions and line frequency variation. It is worth mentioning that the method had the stable and correct response in all tests without any failure.

As the next step, the proposed detection method is evaluated from DT point of view considering different amounts of VSD, POW and PJ as well as line-frequency variation. For this purpose, the detection method is tested for different VSDs from 10% to 90% with interval of 10% and the longest DT for each value of VSD is recorded. Since the DT variation is significant for two cases of VSD equals to 10% and 20%, the DT is obtained for 15% VSD too. For each VSD value (VSD= VSD_T%, 15%, 20%, 30% … 90%), the test is done for different amounts of POW form 0° to 360° of line cycle with interval of 15° while different amounts of PJ from -30° to $+30^\circ$ with interval of 10° are considered for each POW. The obtained results of DT for different amounts of VSD and POW are shown in Figure 2.22. It should be mentioned that for each single POW and VSD, the method has been tested 10 times and the longest DT is depicted in Figure 2.22. It is observed that the DT for VSD of 10%, 15% and 20% is much longer than DT for VSD higher than 20% confirming the significant effect of VSD on the DT. Moreover, Figure 2.22 shows that the DT highly depends on the POW and it may vary 3 to 4 times depending on the POW for the same VSD. Figure 2.22 confirms that effect of the VSD and POW should be considered for DT evaluation of sag detection method which has been considered just in a few of related papers mentioned in Section 2.3. The same data of Figure 2.22 are illustrated in Table 2.2 too. Moreover, the DT of proposed method has

been evaluated for different amounts of PJ with VSD of 10%, line frequency of 60Hz and first case of harmonic distortion. The obtained results are illustrated in Table 2.3. It can be pointed out that the PJ has also significant effect on DT even for the same VSD and POW. A few of numerous obtained experimental results are shown in Figure 2.23 to Figure 2.25.

The method has been tested for some of the mentioned cases with different sampling frequencies rather than 3kHz. The obtained results verified that the DT of the method doesn't depend on the sampling frequency as expected. However, as the same as all other applications, a resolution of ADC can affect the amount of error in calculated fundamental voltage amplitude since the sampled value is different than the actual value due to ADC resolution. The resolution of ADC channel of DSP F28335 used to implement the method is 12bit resulting in voltage resolution of 0.733mV which equals to its overall voltage measurement range (i.e., 3V) divided by the number of voltage intervals (i.e., 2^12-1=4095). As illustrated in simulation results, the proposed method does not results in any ripple in the calculated fundamental voltage amplitude illustrating that the method itself is ripple-free.However as shown in Figure 2.17 and Figure 2.18, the fundamental voltage amplitude calculated by DSP has small ripple in experiments. According to [84], [85], a possible reason for this issue is quantization of each sample in amplitude related to ADC finite number of bit and quantization in time related to sampling rate. Nevertheless, investigation the effect of quantization in amplitude and time is not of interest of this chapter.

Furthermore, in Figure 2.26, the ability of the method to track the voltage has been tested in which the actual fundamental voltage amplitude decreased from 100% nominal value to 0% within 0.417s and then, increased to 100% nominal value within the same

period of time. As shown in Figure 2.26, the proposed method can follow the voltage regarding the mentioned variation with maximum error of ±2% .

According to the obtained results of DT and excessive tests for different cases of VSD, POW and PJ, the best and worst detection time of the proposed method is about 1ms and 8.8ms. It means that any voltage sag can be detected within half line-cycle no matter how much the VSD, POW, PJ or harmonic distortion is which matches with analytical investigation in Section 2.4. It should be added that this method has had the same performance for voltage swell detection because the voltage swell can be considered as voltage sag with negative VSD in the proposed method. Thus, it can be implemented to detect voltage sag, swell or both at the same application.

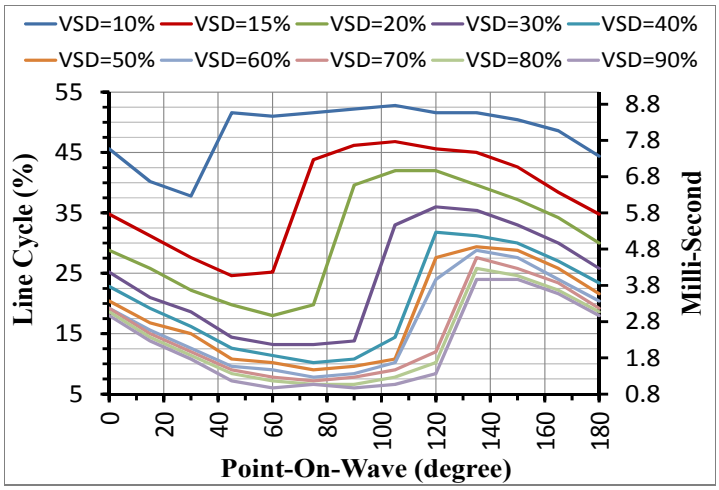

Figure 2.22. Experimental result: DT for different amounts of VSD and POW with line-frequency of 60Hz and first case of harmonic distortion.

TABLE 2.2

DT FOR DIFFERENT AMOUNTS OF VSD AND POW WITHOUT ANY PJ. (THE UNIT FOR DT IS MILLISECOND OUTSIDE OF PARENTHESES AND IS PERCENTAGE OF LINE CYCLE IN PARENTHESES).

Point on Wave (deg)	Voltage Sag Depth (%)									
	10	15	20	30	40	50	60	70	80	90
0	7.6 (46)	5.8 (35)	4.8 (29)	4.2 (25)	3.8 (23)	3.4 (20)	3.2 (19)	3.2 (19)	3.1 (19)	3 (18)
15	6.7 (40)	5.2 (31)	4.3 (26)	3.5 (21)	3.2 (19)	2.8 (17)	2.6 (16)	2.5 (15)	2.4 (14)	2.3 (14)
30	6.3 (38)	4.6 (28)	3.7 (22)	3.1 (19)	2.7 (16)	2.5 (15)	2.1 (13)	2 (12)	1.9 (11)	1.8 (11)
45	8.6 (52)	4.1 (25)	3.3 (20)	2.4 (14)	2.1 (13)	1.8 (11)	1.6 (10)	1.5 (9)	1.4 (8)	1.2 (7)
60	8.5 (51)	4.2 (25)	3 (18)	2.2 (13)	1.9 (11)	1.7 (10)	1.5 (9)	1.3 (8)	1.2 (7)	1 (6)
75	8.6 (52)	7.3 (44)	3.3 (20)	2.2 (13)	1.7 (10)	1.5 (9)	1.3 (8)	1.2 (7)	1.1 (7)	1.1 (7)
90	8.7 (52)	7.7 (46)	6.6 (40)	2.3 (14)	1.8 (11)	1.6 (10)	1.4 (8)	1.3 (8)	1.1 (7)	1 (6)
105	8.8 (53)	7.8 (47)	7 (42)	5.5 (33)	2.4 (14)	1.8 (11)	1.7 (10)	1.5 (9)	1.3 (8)	1.1 (7)
120	8.6 (52)	7.6 (46)	7 (42)	6 (36)	5.3 (32)	4.6 (28)	4 (24)	2 (12)	1.7 (10)	1.4 (8)
135	8.6 (52)	7.5 (45)	6.6 (40)	5.9 (35)	5.2 (31)	4.9 (29)	4.8 (29)	4.6 (28)	4.3 (26)	4 (24)
150	8.4 (50)	7.1 (43)	6.2 (37)	5.5 (33)	5 (30)	4.8 (29)	4.6 (28)	4.3 (26)	4.1 (25)	4 (24)
165	8.1 (49)	6.4 (38)	5.7 (34)	5 (30)	4.5 (27)	4.3 (26)	4 (24)	3.9 (23)	3.7 (22)	3.6 (22)
180	7.6 (46)	5.8 (35)	4.8 (29)	4.2 (25)	3.8 (23)	3.4 (20)	3.2 (19)	3.2 (19)	3.1 (19)	3 (18)

TABLE 2.3

DT FOR DIFFERENT AMOUNTS OF PJ AND POW WITH VSD OF 10%. (THE UNIT FOR DT IS MS OUTSIDE OF PARENTHESES AND IS PERCENTAGE OF LINE CYCLE IN PARENTHESES).

Point on Wave (deg)	Phase Jump (degree)						
	-30	**-20**	**-10**	**0**	**10**	**20**	**30**
0	3.5 (21)	4 (24)	5.2 (31)	7.3 (44)	7.4 (44)	6.9 (41)	6.4 (38)
15	2.7 (16)	3.2 (19)	4.7 (28)	6.7 (40)	6.7 (40)	6.2 (37)	5.5 (33)
30	2.3 (14)	2.5 (15)	3.8 (23)	6.3 (38)	5.8 (35)	5.2 (31)	4.5 (27)
45	1.9 (11)	2 (12)	3.2 (19)	8.3 (50)	5.2 (31)	4.3 (26)	3.6 (22)
60	1.4 (8)	1.6 (10)	8.8 (53)	8.6 (52)	4 (24)	2.9 (17)	2.7 (16)
75	8.8 (53)	8.8 (53)	8.8 (53)	8.5 (51)	3.4 (20)	2.5 (15)	2 (12)
90	8.8 (53)	8.7 (52)	8.8 (53)	8.5 (51)	8.7 (52)	1.9 (11)	1.55 (9)
105	8.7 (52)	8.7 (52)	8.8 (53)	8.5 (51)	8.7 (52)	2.7 (16)	1.7 (10)
120	8.6 (52)	8.6 (52)	8.1 (49)	8.5 (51)	8.8 (53)	8.8 (53)	8.8 (53)
135	6.8 (41)	6.2 (37)	7.3 (44)	8.5 (51)	8.8 (53)	8.7 (52)	8.7 (52)
150	5.5 (33)	5.4 (32)	6.5 (39)	8.4 (50)	8.5 (51)	8.5 (51)	8.6 (52)
165	4.5 (27)	4.7 (28)	6 (36)	8.1 (49)	8.1 (49)	7.9 (47)	7.5 (45)
180	3.7 (22)	4 (24)	5.2 (31)	7.4 (44)	7.2 (43)	6.9 (41)	6.4 (38)

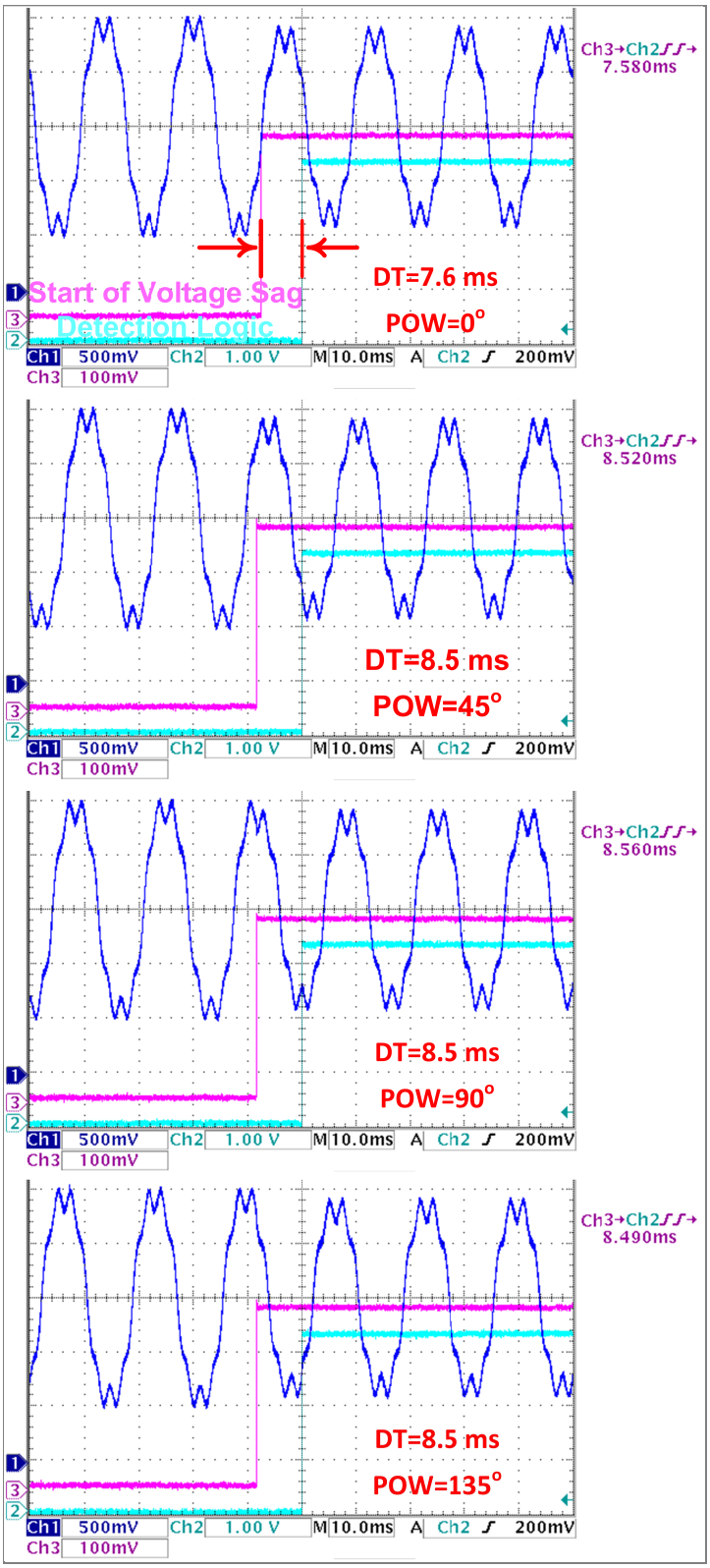

Figure 2.23. Experimental result of 10% VSD for different amounts of POW with PJ=0°, line-frequency of 60 Hz and second case of harmonic distortion.

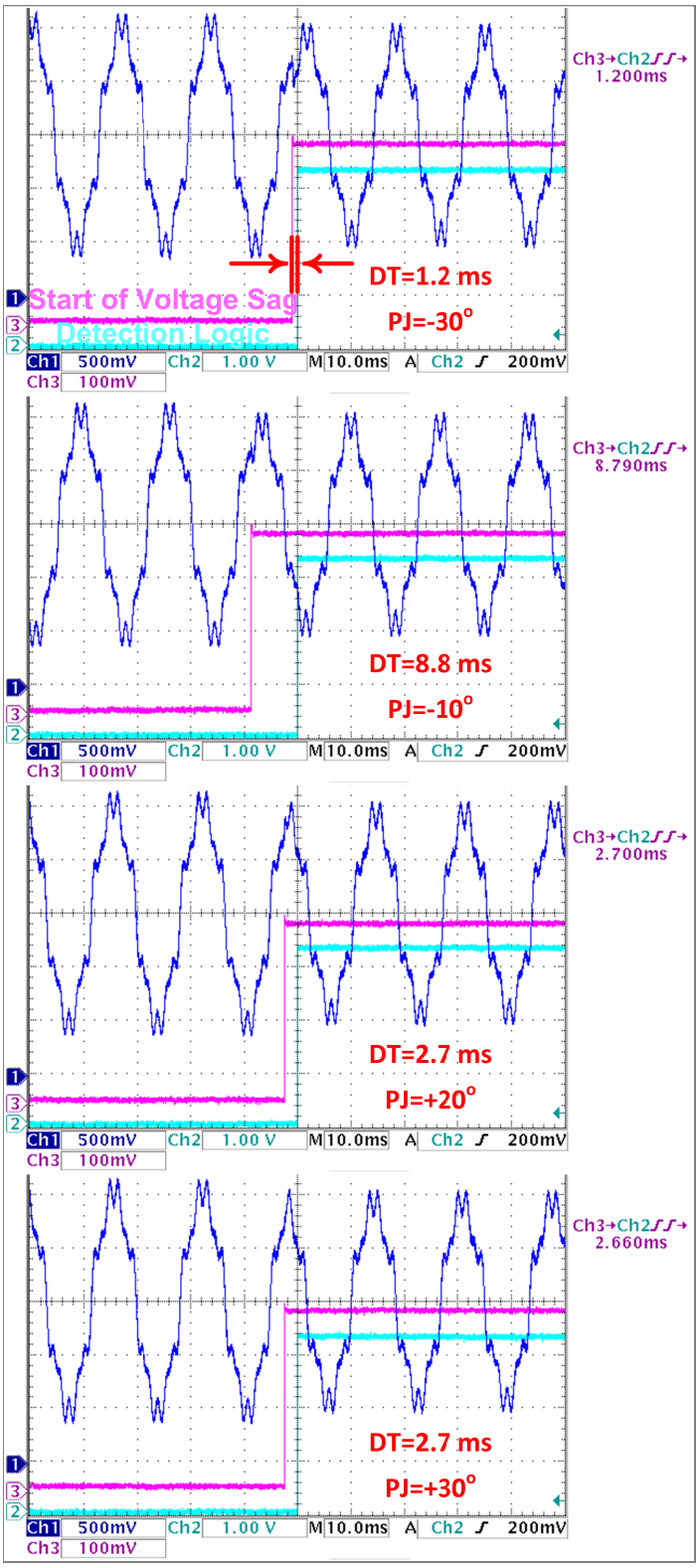

Figure 2.24. Experimental result of 10% VSD for different amounts of PJ with POW=60°, line-frequency of 60 Hz and first case of harmonic distortion.

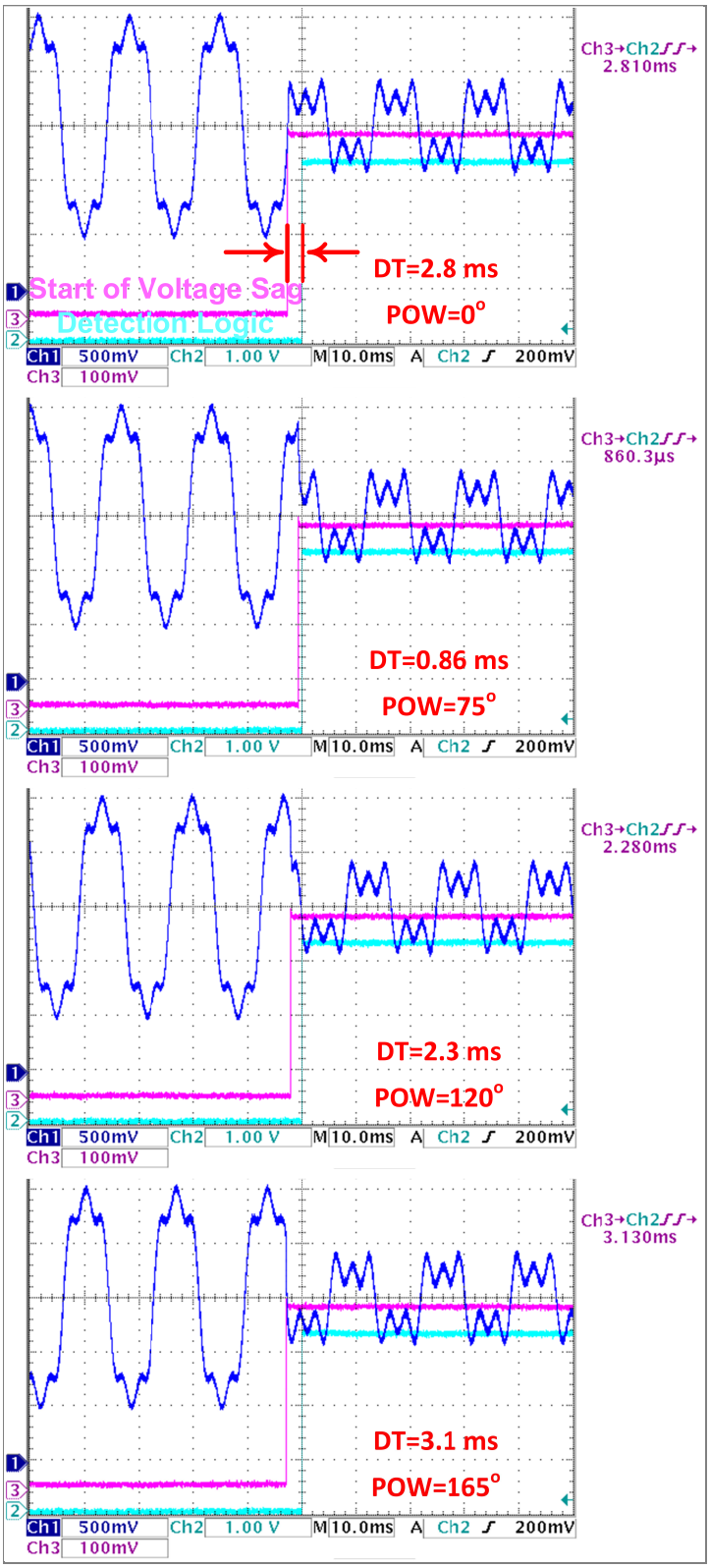

Figure 2.25. Experimental result of 70% VSD for different amounts of POW with PJ=20°, line-frequency of 60 Hz and third case of harmonic distortion.

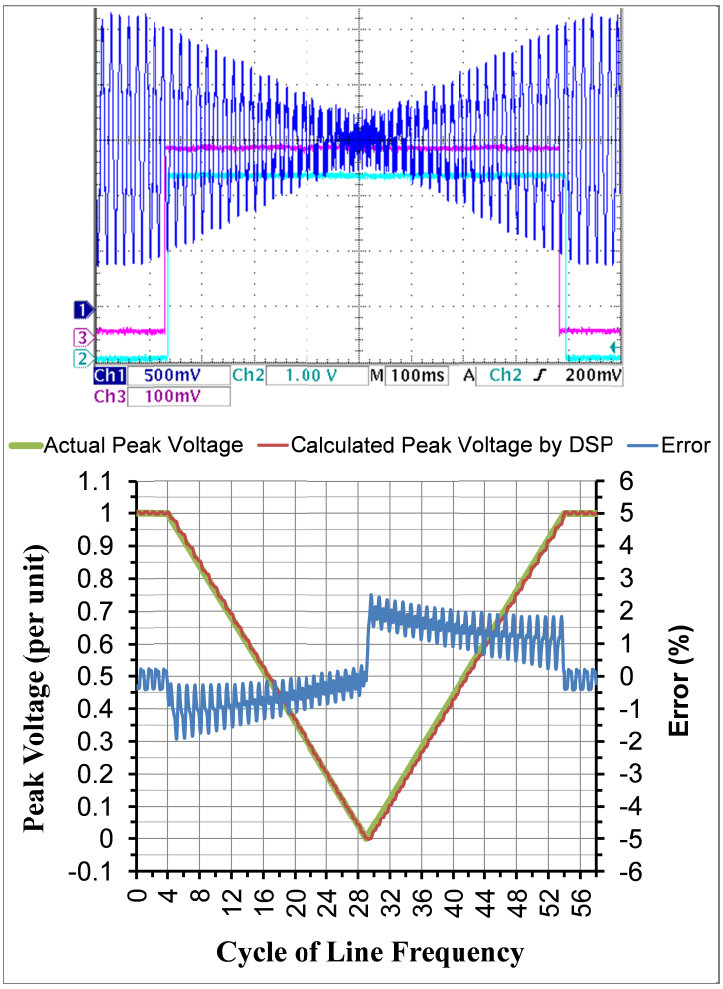

Figure 2.26. Experimental result of continuous decrease and increase (100% within 0.417s) of fundamental voltage amplitude.

2.7. Comparison with Other Methods

In this section, the proposed method is compared with other methods whose DT is provided in previously published articles, except the DQT-based methods [22]–[33], [66], [68]–[71] which can't detect the single-phase voltage sags with VSD less than 30% (as previously explained in Section 2.2.3) as well as WT-based methods which tend to malfunction in harmonic distortion condition [19], [40]–[50], [83].

In [34], the presented method has a DT of half cycle for 50% VSD which is almost

two times of DT of the proposed method for the same VSD. Furthermore, the effect of POW on DT and method's performance under the cases of line frequency variation and PJ has not considered. The best and worst DT of hybrid method presented in [54] is 0.06 ms and 6.9 ms for VSD between 10% to 100% while the LL of constant threshold is set to 94% instead of 90%. In other words, the minimum VSD considered during the DT evaluation of this method is 4% below the LL. This can be translated to 14% VSD for this chapter's proposed method whose LL is set to 90%. Thus, the proposed method has tested for 14% VSD and its best and worst DT is 4.2ms and 8ms, respectively. However, no information about the amount of ripple and accuracy of the method as well as its performance under the cases of excessive-harmonic distortion, line frequency variation and PJ has been provided in [54].

The method presented in [56] detects %10 VSD in half of cycle with 60Hz line frequency which is almost the same as this chapter's proposed method. However, the method presented in [56] is complex from computational point of view since it needs to calculate four matrices offline for different amounts of line-frequency. In [56], it has been mentioned that 200 versions of four matrices are obtained offline for the line-frequency in range of 49Hz to 51Hz at the steps of 0.01Hz and stored in the memory. Moreover, an interpolation will be performed during the real time operation to obtain the required four matrices if the estimated line-frequency does not match with offline cases. This shows that method presented in [56] greatly depends on line-frequency and it requires very precise estimation of line-frequency while the method is tested for 0.05Hz variation of line-frequency. In addition, no information about the amount of ripple and accuracy of the method as well as the effect of POW, PJ and line frequency variation on DT has been

provided.

Authors in [59]–[62] claimed that the presented method can detect the voltage sag in less than 1.7ms which is the calculation time. However, the method doesn't trigger and start the calculation process if the POW is between the -25^{o} and $+25^{o}$ [59]. Thus, if the voltage sag happens at -25^{o} POW, the calculation process will not be triggered until $+25^{o}$ POW which means 50^{o} (=2.3ms in 60Hz) delay. Then, the calculation process will be triggered in $+25^{o}$ POW and after 1.7ms the voltage sag will be detected which means the worst DT of 4ms (1.7ms+2.3ms). However, the method has been tested just for 50% and 100% VSD in [59]–[61] and 30% VSD in [62]. Thus, it is not clear whether or not the presented method can detect the voltage sags with VSD less than 30% since it needs very precise and fast PLL as well as precise lookup table. In addition, no information about the performance of the method under the cases of line frequency variation and PJ as well as dependence of DT on VSD and POW has been provided in [59]–[62].

Another method is the one presented in [76] whose best and worst case DT is 1ms and 4ms, respectively. It is worth mentioning that this method's worst DT, i.e., 4ms, is obtained for 20% VSD while the LL of constant threshold is set to 90%. According to Table 2.2, the best and worst DT of this chapter's proposed method for the case of 20% VSD is 3ms and 7ms, respectively. Nevertheless, the method in [76] hasn't considered the harmonic distortion case, which should definitely take into account in practical cases, and even hasn't mentioned whether or not the method can still operate under the harmonic distortion case. Therefore, it cannot be claimed that the method in [76] is faster than the proposed method. Moreover, the mentioned method has considered just POW of 0, 90 and 180 degrees and no information about the amount of ripple and accuracy as well as its

performance under the case of PJ has been provided in [76].

The method in [78] has the DT of 1.3ms related to 90% VSD and 8.3ms related to 20% VSD with 60Hz line frequency. To compare this method with the proposed method, it should be mentioned that the best and worst DT of the proposed method at 20% VSD are 3ms happens at POW of 60^{o} and 7ms happens at POW of 105^{o} and 120^{o}, respectively. And the best and worst DT of the proposed method related to 90% VSD is 1ms happens at POW of 60^{o} and 3.6ms happens at POW of 165^{o}, respectively. However, the method presented in [78] needs precise PLL and also, no information about the amount of ripple and accuracy of the method as well as the effect of POW, PJ and line frequency variation on DT has been provided. This method had a stable performance under the harmonic distortion with THD of 3% while it had malfunction under the harmonic distortion with THD of 7%.

It is worth mentioning that other articles studying the voltage sag detection hasn't provided any information about the DT of presented method [15], [21], [29], [32], [39], [41], [43]–[45], [47], [48], [50], [51], [55], [62]–[65], [77], [79], [80], [82]. This lack of information does not mean to conclude that the proposed approach outperforms the previous ones (nor even the opposite, of course). Moreover, this lack of information does not lead to implement all previous methods, which is not in the scope of this chapter, and compare with the proposed method.

2.8. Conclusion

First, available voltage sag detection methods are briefly reviewed and their pros and cons are provided. Afterwards, the important criteria such as amount of VSD, POW and PJ, which severely affect the performance of any voltage sag detection method and its DT, are listed; and any available paper which has considered any of these criteria is referred. In addition, the necessity of the hysteresis threshold instead of constant threshold comparator is discussed and the procedure of how to design the threshold band is given. Finally, two methods are proposed while one is applicable in non-harmonic cases and another is applicable in harmonically distorted cases.

a voltage sag detection method to calculate the fundamental voltage amplitude is proposed applicable for both single- and three-phase applications. The advantages of the proposed method are reliable operation, precise detection, simple computation and easy implementation without using a PLL, lookup table and low-pass filter. The method has been simulated and implemented experimentally and tested considering all of the mentioned criteria such as different amounts of VSD, POW, PJ, harmonic distortion and line frequency variation to validate its performance. Moreover, dependency of DT on VSD, POW and PJ is illustrated and DT of the proposed method for different amounts of VSD, POW and PJ is provided. According to obtained results, the best and worse DT was 1ms and 8.8ms, respectively, which means that the proposed method can detect the voltage sag within half cycle regardless of amount of VSD, POW, PJ or harmonic distortion. This fact matches with theoretical proof too. Furthermore, the proposed method had precise detection and stable performance even for the cases where the voltage has excessive-

harmonic distortion and line frequency variation. According to the data obtained from DSP memory, the method had maximum ripple of $\pm 0.3\%$ in normal condition of line frequency and $\pm 1\%$ in the case of $\pm 1 Hz$ variation of 60Hz line frequency causing to have very narrow band of hysteresis for threshold comparator. The proposed method was tested under conditions of excessive-harmonic distortion, line frequency variation, and different amounts of PJ, VSD, and POW in both simulation and experiments while it was able to detect the voltage sag without any failure, which demonstrates high reliability. In addition, the performance of the proposed method was investigated analytically under frequency variation and the obtained analytical results matched perfectly with simulation results. The technique presented in this chapter is also capable to detect voltage swell as well as to follow continuous variation in fundamental voltage amplitude. The performance evaluation of the proposed method to detect the voltage swell may be considered in future work.

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Chapter 3: A Unified Platform Enabling Power System Circuit Model Data Transfer among Different Software

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3.1. Introduction

As power distribution systems are evolving into more complex networks, electrical engineers have to rely on software tools to perform circuit analysis [1]–[4]. Recent advances in engineering sciences have brought a revolution in power system software packages [5]–[15]. There are dozens of powerful software tools available in the market to simulate the power grid. Although their main functions are similar, there are differences in features and formatting structures to suit specific applications. This creates challenges for transferring circuit models between different software. Most utilities use some specific software package according to their needs or preferences, where each stores information about loads and circuit model in its own specific database structure.

With the emergence of new generation resources such as solar energy and wind energy [16]–[19], or new technologies such as power measurement units (PMUs) and micro PMUs [20]–[22], as well as new concepts such as smart grid or micro grid [23]–[26], new circuit phenomena including dynamic behaviors will need to be studied. Therefore, utilities may need to use different software tools to investigate these new phenomena, which may not be supported by their current software platforms. Thus, it becomes necessary to transfer power system circuit model data (PSCMD) from one software to another. However, PSCMD sharing among different software is a cumbersome process that can consume many person-hours. What is needed is a solution that enables cross-platform PSCMD transfer in the form of a complete power distribution network starting from the substation transformer all the way down to the load.

The objective of this chapter is to develop a Unified Platform (UP) to facilitate

transferring PSCMD among different software packages and relieve the challenges of the circuit model conversion process. UP uses a commonly available spreadsheet file with a defined format, for any home software to write data to, and for any destination software to read data from, via a script-based application called the PSCMD transfer application. The main considerations in developing the UP are to minimize manual intervention and import a one-line diagram into the destination software or export it from the source software, with all details to allow load flow, short circuit and other analyses.

In this chapter, ETAP, OpenDSS, and GridLab-D are considered. PSCMD transfer applications written in MATLAB have been developed for each of these to read the circuit model data provided in the UP spreadsheet. Each PSCMD transfer application has been verified by using two sample circuits, a test circuit and an actual circuit from a utility company for all the above listed software. When PSCMD is provided in the UP spreadsheet with defined format, successful reconstruction of the circuit in a destination software is achieved. Load flow analysis is performed in each software for both sample circuits and compared with the available results to verify the correctness of the circuit built by the PSCMD transfer application. The obtained results match accurately in all software for both circuits.

The chapter is organized as follows: Section 3.2 describes the UP and its functions. Sections 3.3 to 3.6 introduce the four software tools considered here –ETAP, OpenDSS, GridLab-D, and DEW– and describe the developed PSCMD transfer applications for each. Section 3.7 presents simulation results to verify the effectiveness of the proposed UP and transfer process. Section 3.8 compares features and capabilities of the mentioned software tools and highlights some specific issues, and Section 3.9 offers concluding observations.

3.2. Proposed Unified Platform Based on Spreadsheet

Conventionally, users develop their own tailor-made applications to transfer PSCMD from one software to another as needed. These applications are typically unidirectional, i.e. one specific application can transfer data from software #1 into software #2, but not vice versa. Therefore, if there are *N* different software packages, $N \cdot (N-1)$ applications will be required. This approach is quite wasteful since there are dozens of software packages in this field. To complicate things, each software has its own terminology. For example, software #1 may name a positive sequence resistance of cable "Line R1 Ohms" while software #2 may name it "Pos. Seq R". Also each software has its own database structure to store their circuit model data. Another issue is the unit of component parameters. For example, conductor impedance can be in ohms or ohms per mile. Moreover, it is possible that one software package might consider certain parameters that other packages do not. Therefore, the developers of the PSCMD transfer applications need to be very familiar with both software and their internal languages (names of components and their parameter) in detail to be able to write the application properly. This section proposes UP to facilitate the PSCMD transfer process. As shown in Figure 2.15, the proposed UP results in developing only two application for each software; one to read PSCMD from the UP spreadsheet file and transfer it to the destination software and the other one to read PSCMD from the source software and import it to the UP spreadsheet with defined format. Consequently, the number of applications required to share data among *N* different software is reduced from $N \cdot (N-1)$ to 2N. The PSCMD transfer applications that transform circuit model data from the UP spreadsheet to commercial

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software packages are written in the MATLAB. Each application is unique to the associated software.

The proposed UP consists of a spreadsheet file with a defined format containing several sheets to include specifications for bus/node, cable, capacitor bank, circuit breaker, generator, load, overhead line, transformer, etc. Each sheet is a library of the parameters of available components in the circuit with details to allow different power system studies. For instance, the sheet called cable contains the required parameters such as ID, from node, to node, phase configuration, positive sequence resistance, positive sequence reactance, positive sequence admittance, zero sequence resistance, zero sequence reactance, zero sequence admittance, length, current rating, etc. A snapshot of the UP spreadsheet is given in Figure 3.2, illustrating the format and required parameters of some components such as transformer, cable, capacitor and load. It is worth mentioning that UP does not include the time-varying data to do time-series simulation since this depends on whether the specific software has the capability to do time-series simulation and if so, it depends on what format the specific software needs data to do time-series simulation. UP allows PSCMD transfer to and from the set of software, and it enables users to explore some new phenomena in their circuits by using a different software without the time consuming data transfer process.

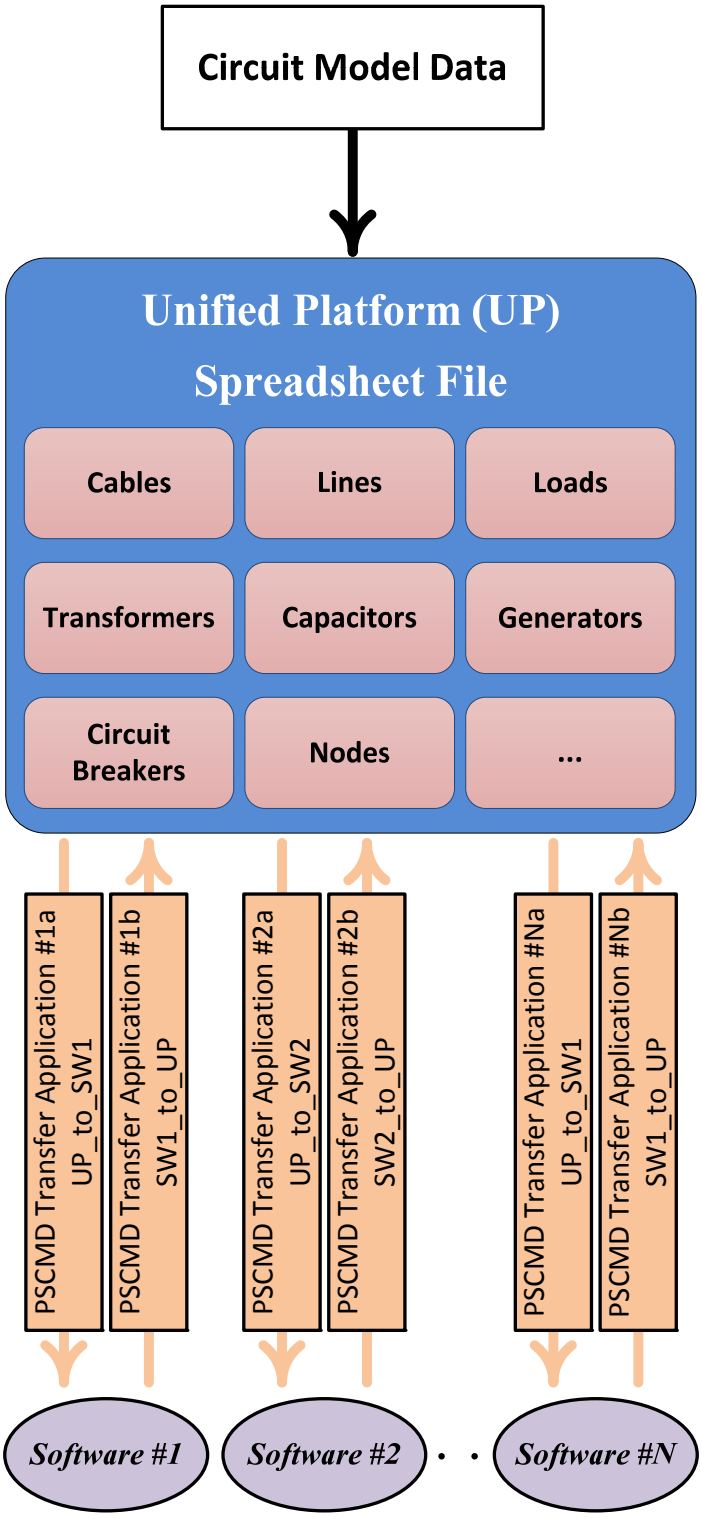

Figure 3.1. Conceptual illustration of the proposed unified platform (UP) to transfer power system circuit model data among different software. SW stands for software.

(a)

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Section Id	From Node	To Node	Cap Nom (kVA)	Prim Volt (kVLL)	Sec Volt (kVLL)	X0 R0 Ratio	X1 R1 Ratio	Z0 (%)	Z1 (%)	Primary Config	Secondary Config		
TR1	N5	N9	1500	12	0.48	10	10	6	6	D	Yg		

(b)

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Section Id	From Node	To Node	Phase	Line R1 Ohms	Line X1 Ohms	Line B1 uS	Line R0 Ohms	Line X0 Ohms	Line B0 uS	Length ft	IA (Amps)	IB (Amps)	IC (Amps)
C1	N1	N2	ABC	0.01	0.012	12.091	0.054	0.015	12.091	341	473	473	473

(c)

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Section Id	From Node	Cap. Control	Cap. Status	kV	Total Cap. Kvar	Phase	Config	Sensing ON	Sensing OFF	PT Ratio			
CAP2	N4	Voltage	On	7.2	1200	ABC	Y	121	126	60			

(d)

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Section Id	From Node	Phase	Config	Spot kVAR A	Spot kVAR B	Spot kVAR C	Spot kW A	Spot kW B	Spot kW C				
LD1	N10	AB	Yg	600	360	0	800	480	0				

Figure 3.2. Snapshot of UP's spreadsheet containing required parameters of: (a) transformer; (b) cable; (c) capacitor and (d) load

3.3. Transferring Power System Circuit Model Data From Unified Platform into ETAP

ETAP electrical engineering software is a fully integrated power systems analysis solution that includes analytical software modules for load flow, arc flash, short circuit, transient stability, relay coordination, cable ampacity, optimal power flow, and more. Its modular functionality can be customized to fit various simulation needs [27].

With the proposed UP, the circuit model data are imported into ETAP through a spreadsheet file with the defined format. One challenge in this process is to match ETAP's internal representation of data. For example, there are options in the ETAP graphical user interface (GUI) of cable parameters to define its length unit (feet, mile, km, m), and to define whether the assigned impedance is a total impedance of cable, or an impedance per unit length. Similar options exist for other components. Therefore, it is necessary to understand how such options are translated in ETAP language and stored inside its database. To overcome this difficulty, a probing mechanism has been formulated to determine how the data should be transferred into ETAP.

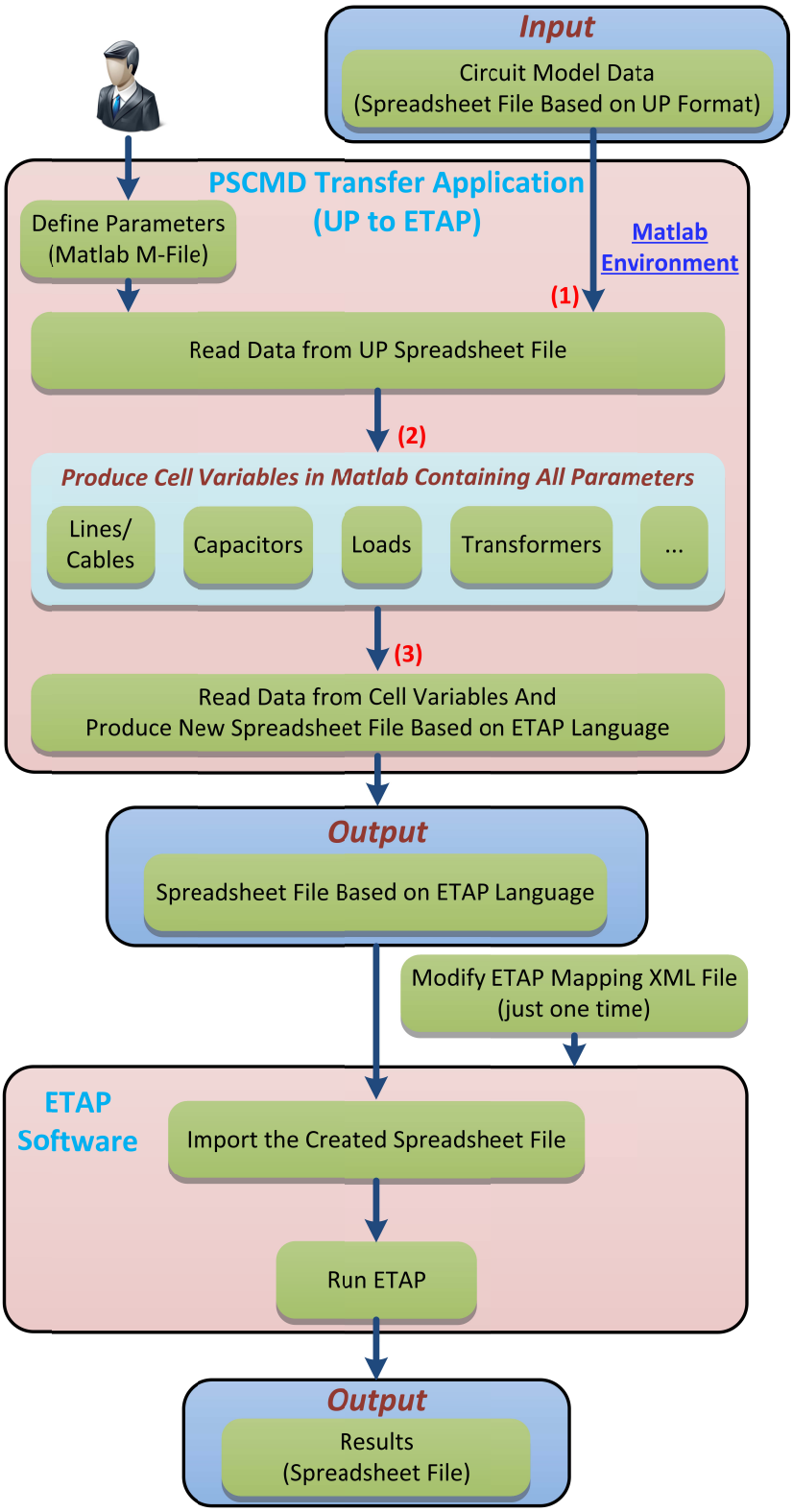

Figure 3.3. General scheme of importing power system circuit model data from UP spreadsheet into ETAP using PSCMD transfer application.

To import a PSCMD provided in the UP spreadsheet, some information must be modified. For example, ABC, A, B, C, AB, BC, CA for loads in the UP spreadsheet are representing what the configuration is while ETAP assigns them as 0, 0, 1, 2, 3, 4, 5 in field named “Phase Connection”, respectively. Therefore, the circuit model data provided in the UP spreadsheet need to be translated to the language readable for ETAP. One option is to do this manually. However, this may cause some unnoticeable errors, and also take more time if multiple circuits need to be transferred. Here an application in MATLAB to do the translation. Such a script is required for each component in the UP spreadsheet, including loads, capacitors, cables, overhead lines. The general import scheme is shown in Figure 3.3, where the arrows indicate movement from the current to the next step.

The first step of the PSCMD transfer application, as numbered (1) in Fig. 3, is to read all data in each sheet of the UP spreadsheet. In the second step, all data from an individual sheet, which will be related to one specific component, are stored in an individual cell variable in MATLAB to contain all parameters of that component. The third step of PSCMD transfer application reads all data of each cell variable one by one and produces the new spreadsheet based on the ETAP language, so the user can import the new spreadsheet file into ETAP. Figure 3.4 and Figure 3.5 show a few snapshots of the PSCMD transfer application in the process of performing the required modifications.

```
for i=1:NofRow
    switch Load_New{i,NofColumn_Phase_CYME}
        case 'ABC'
            Load_New(i,NofColumn_PhaseConnection_Number) = {0};
        case 'A'
            Load_New(i,NofColumn_PhaseConnection_Number) = {0};
        case 'B'
            Load_New(i,NofColumn_PhaseConnection_Number) = {1};
        case 'C'
            Load_New(i,NofColumn_PhaseConnection_Number) = {2};
        case 'AB'
            Load_New(i,NofColumn_PhaseConnection_Number) = {3};
        case 'BC'
            Load_New(i,NofColumn_PhaseConnection_Number) = {4};
        case 'CA'
            Load_New(i,NofColumn_PhaseConnection_Number) = {5};
    end
end
```

Figure 3.4. Snapshot of script to determine variable of PhaseConnection_number for ETAP.

```
for i=1:NofRow
    if (Load_New{i,NofColumn_Phase_abc}==1)
        Load_New(i,NofColumn_GndType_Number) = {0};
    end
    switch Load_New{i,NofColumn_GndConfig_CYME}
        case 'Y'
            Load_New(i,NofColumn_GndType_Number) = {0};
        case 'Yg'
            Load_New(i,NofColumn_GndType_Number) = {1};
        case 'D'
            Load_New(i,NofColumn_GndType_Number) = {2};
    end
end
```

Figure 3.5. Snapshot of script to determine variable of GroundingConnection_type for ETAP

After understanding the internal representations of components parameters in ETAP, modifying PSCMD in UP spreadsheet, and producing a new spreadsheet file which is readable for ETAP, the final step is to expand the ETAP mapping Extensible Markup Language (XML) file. This file contains all mapping data required to import PSCMD from the new spreadsheet file, created by PSCMD transfer application, into ETAP. The reason behind this is that all internal representations of components and their parameters are not

defined in the mapping XML file by default. Modification of mapping XML file trains ETAP to read, for instance, a value in spreadsheet file in sheet named “cable’ under a header named “Line X0Ohms” as a zero sequence reactance of cable and write it in field named “Zero X” in ETAP. Figure 3.6 shows a snapshot of part of the ETAP mapping XML file modifications related to cable as an example.

The user then only needs to follow the following straightforward procedure to transfer the PSCMD prepared based on UP format into ETAP:

- Locate the UP spreadsheet containing all PSCMD in the folder where the PSCMD transfer application is.
- Open MATLAB and run the PSCMD transfer application. After it is run, a new spreadsheet based on the ETAP language is produced in the same folder.
- Locate the modified ETAP mapping XML file in the ETAP folder.
- Import the new produced spreadsheet into ETAP.

```
<!--C A B L E   F I E L D   D I C T I O N A R Y
   -->
 <CableFieldDict FieldName="ID" ColCaption="Section Id" />
 <CableFieldDict FieldName="From Bus" ColCaption="From Node" />
 <CableFieldDict FieldName="To Bus" ColCaption="To Node" />
 <CableFieldDict FieldName="Pos. Seq R" ColCaption="Line R1Ohms" />
 <CableFieldDict FieldName="Pos. X" ColCaption="Line X1Ohms" />
 <!-- <CableFieldDict FieldName="Pos. Y" ColCaption="Line B1uS" /> -->
 <CableFieldDict FieldName="Pos. Y" ColCaption="Line B1_S" />
 <CableFieldDict FieldName="Zero Seq R" ColCaption="Line R0Ohms" />

 <CableFieldDict FieldName="Zero X" ColCaption="Line X0Ohms" />

 <!-- <CableFieldDict FieldName="Zero Y" ColCaption="Line B0uS" /> -->
 <CableFieldDict FieldName="Zero Y" ColCaption="Line B0_S" />
 <CableFieldDict FieldName="Full Load Amp" ColCaption="IA(Amps)" />

 <!--From Bus -->
 <CableFieldDict FieldName="From Bus" ColCaption="From Bus ID" />
 <CableFieldDict FieldName="From Bus" ColCaption="From Element ID" />
 <!--To Bus -->
 <CableFieldDict FieldName="To Bus" ColCaption="To Element ID" />
 <CableFieldDict FieldName="To Bus" ColCaption="To Bus" />
 <!--# / Phase-->
 <CableFieldDict FieldName="# / Phase" ColCaption="No per Phase" />
 <CableFieldDict FieldName="# / Phase" ColCaption="# / Phase" />
 <!--Length-->
 <CableFieldDict FieldName="Length" ColCaption="Cable Length" />
 <CableFieldDict FieldName="Length" ColCaption="Length" />
 <CableFieldDict FieldName="Length" ColCaption="Lengthft" />
 <CableFieldDict FieldName="Length" ColCaption="Length of Cable" />
 <!--Pos. Seq R-->
 <CableFieldDict FieldName="Pos. Seq R" ColCaption="Pos. Seq R" />
 <CableFieldDict FieldName="Pos. Seq R" ColCaption="Positive R" />
 <!--Zero Seq R-->
 <CableFieldDict FieldName="Zero Seq R" ColCaption="Zero Seq R" />
 <CableFieldDict FieldName="Zero Seq R" ColCaption="Zero R" />
 <!--Pos. Seq X-->
 <CableFieldDict FieldName="Pos. X" ColCaption="Pos. Seq X" />
 <CableFieldDict FieldName="Pos. X" ColCaption="Positive X" />
 <!--Zero Seq X-->
 <CableFieldDict FieldName="Zero X" ColCaption="Zero Seq X" />
 <CableFieldDict FieldName="Zero X" ColCaption="Zero X" />
 <!--Pos. Seq Y-->
 <CableFieldDict FieldName="Pos. Y" ColCaption="Pos. Seq Y" />
 <CableFieldDict FieldName="Pos. Y" ColCaption="Positive Y" />
 <!--Zero Seq Y-->
 <CableFieldDict FieldName="Zero Y" ColCaption="Zero Seq Y" />
 <CableFieldDict FieldName="Zero Y" ColCaption="Zero Y" />
 <!--Cable Size-->
 <CableFieldDict FieldName="Cable Size" ColCaption="Cable Size" />
 <CableFieldDict FieldName="Cable Size" ColCaption="Size" />
```

Figure 3.6. Snapshot of ETAP mapping XML file modification related to cable component.

3.4. Transferring Power System Circuit Model Data from Unified Platform into OpenDSS

OpenDSS is an open-source electric power Distribution System Simulator (DSS) for supporting distributed resource integration and grid modernization efforts [28]–[30]. The OpenDSS tool has been used since 1997 in support of various research and consulting projects requiring distribution system analysis and has been publicly-available in 2008. It performs nearly all frequency domain (sinusoidal steady state) analyses commonly performed on electric utility power distribution systems; however, it does not perform time domain studies [31], [32]. In addition, it supports many new types of analyses that are designed to meet future needs related to smart grid, grid modernization, and renewable energy research [31], [33], [34]. One of the significant features of OpenDSS is time-series simulation to study time-varying events, ranging from sub-seconds to years, of renewable energy resources such as wind or solar in power systems [32], [35]. A time-series simulation is a sequence of analysis, typically at successive points in time spaced at uniform time intervals. Examples of time series are the hourly or monthly values of load profile. Many of this program's features were originally intended to support the analysis of distributed generation, and this continues to be a common use. It also supports analysis of phenomena such as energy efficiency in power delivery and harmonic current flow. OpenDSS is designed to be indefinitely expandable, so that it can be modified to meet future needs.

OpenDSS is a script-based tool where all components and their parameters and connectivity are assigned in the script-based environment. In other words, it does not have

any Graphical User Interface (GUI) to drag and drop a component (e.g., load) from its library and make any connection to another component (e.g., cable). Moreover, it does not have any built-in feature yet to import PSCMD from a spreadsheet file as, for example, ETAP does. Therefore, it will take a long time to create any industry-level circuit in OpenDSS containing hundreds of lines, cables, loads etc. Here, an application is developed in MATLAB to read PSCMD provided in the UP spreadsheet. This PSCMD transfer application creates a text file containing all lines, cables, loads, transformers, capacitors, circuit breakers etc., based on the language of OpenDSS. The general scheme of importing PSCMD from the UP spreadsheet into OpenDSS is illustrated in Figure 3.7.

It is worth mentioning that the developed PSCMD transfer application can be customized according to a user-defined format of the spreadsheet file. This means the application works with spreadsheet formats (containing PSCMD) that are not exactly the same as UP. In such cases, the user needs to determine in the first part of PSCMD transfer application, numbered (1) in Figure 3.7, some parameters such as sheet names in user-defined spreadsheet for each specific component and which column in each sheet contains specific component's parameter. However, all parameters of one component, e.g., cable, in PSCMD should be provided in one sheet of the spreadsheet file in both UP or user-defined format. Moreover, users need to provide some parameters such as the directory where the UP spreadsheet is located, the name of the UP spreadsheet, the output file directory, the output file name, the simulation mode etc. in the first part of PSCMD transfer application.

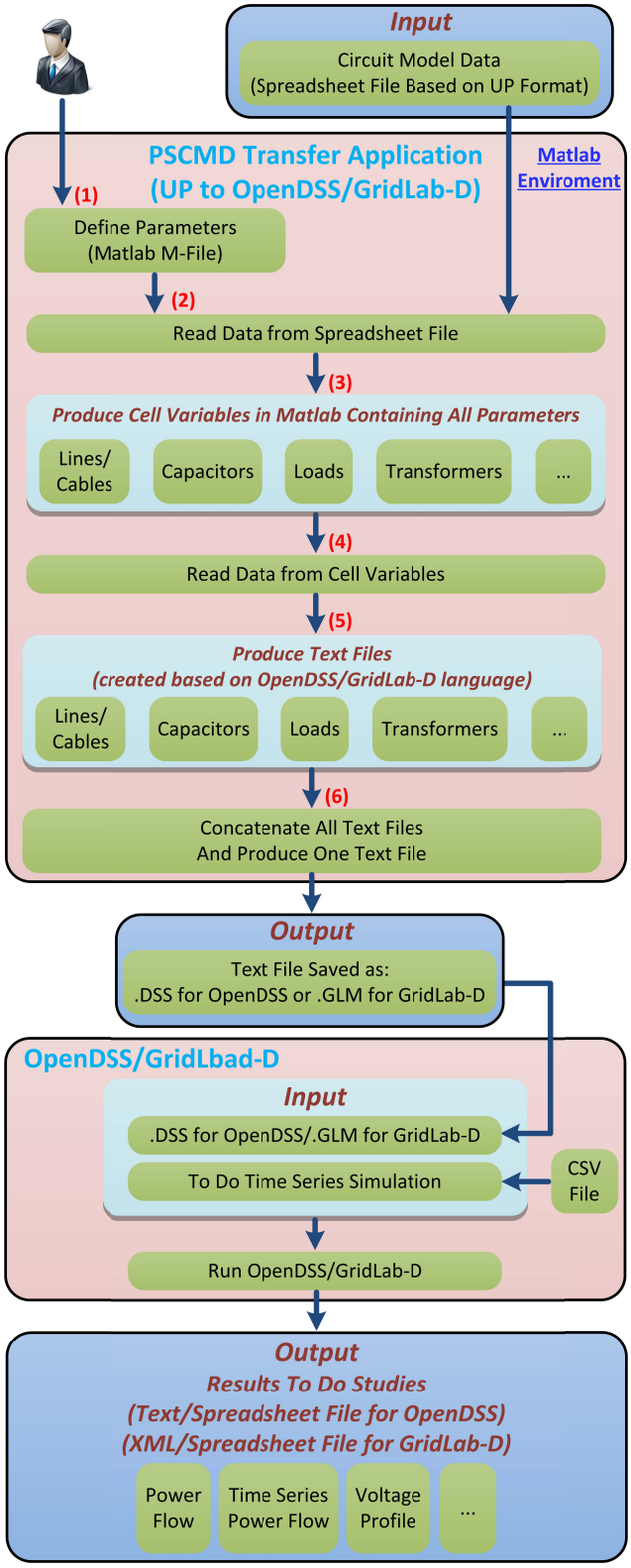

Figure 3.7. General scheme of importing power system circuit model data from UP spreadsheet into OpenDSS using PSCMD transfer application.

The second part of the PSCMD transfer application, numbered (2) in Figure 3.7, is to read spreadsheet data from each of its sheets that is individually related to a specific component. Part (3) stores data in individual cell structure inside the MATLAB. Figure 3.8 shows the part of PSCMD transfer application code for reading overhead lines information. After reading all PSCMD from the UP spreadsheet and storing them in the cell variables inside the MATLAB, step (4) and (5) are to read cell variables and produce a text file for each individual components, respectively. The last step is to concatenate all text files and create a single text file that will be saved as a .dss file later by the user. Figure 3.9 depicts a snapshot of the code for overhead lines information in the PSCMD transformation application. Finally, to verify the correctness of the structured circuit in OpenDSS, a load flow analysis should be performed and the obtained results should be compared with valid results. The created .dss file can be run along with comma-separate value (.csv) files containing the values of time-variant object to do time-series simulation.

The user needs to follow the following straightforward procedure to transfer the PSCMD prepared based on UP format into OpenDSS:

- Locate the UP spreadsheet containing all PSCMD in the folder where the PSCMD transfer application is.
- Open MATLAB, initialize the required parameters, as explained previously, and run the PSCMD transfer application. After it is run, a text file based on OpenDSS language is produced in the same folder. Save it as .dss file.

  Open OpenDSS software and select the related .dss file.

```
% XLines: Start
% ****************************************************************
for k=1:Do_Xline
    [ndata, text, alldata] = xlsread(Excel_file , Xline_Sheet_Name);
    XLine = alldata;

    [NofRow_Xline NofColumn_Xline]=size(XLine);

    for i=Xline_Start_at_Row:NofRow_Xline
        if (isnan(XLine{i,Xline_WhichColumn_Name}))
            NofRow_Xline = i-1;
            break;
        end
    end

    XLine_New = XLine(1:NofRow_Xline,:);
    XLine_New_String_Check = zeros(NofRow_Xline , NofColumn_Xline);


    for i=Xline_Start_at_Row:NofRow_Xline
        for j=1:NofColumn_Xline
            if (strncmp(XLine(i,j),Char_Apstr,1))
                XLine_New{i,j} = XLine{i,j}(2:length(XLine{i,j}));
            end
        end
    end
    fID_Xline_txt = fopen([Text_Files_Dir Xline_txt_file], 'w');
    % ************************************************************
```

Figure 3.8. Snapshot of data parsing part in PSCMD transfer application to transfer power system circuit model data from UP spreadsheet into OpenDSS.

```
    % Define Lines
    % ****************************************************************
    fprintf(fID_Xline_txt,'\n\n!********************************** \n');
    fprintf(fID_Xline_txt,'!Line Codes: Start \n');
    fprintf(fID_Xline_txt,'!Written by Arash \n');
    fprintf(fID_Xline_txt,'!Number of Linecodes = %.1f  \n\n', (NofRow_Xline -↙
Xline_Start_at_Row + 1));
    for i=Xline_Start_at_Row:NofRow_Xline

        if (strcmp( class(XLine_New{i,Xline_WhichColumn_Name}) , 'double' ))
            XLine_New{i,Xline_WhichColumn_Name} = num2str(XLine_New{i, ↙
Xline_WhichColumn_Name});
            if (strcmp( class(XLine_New{i,Xline_WhichColumn_Name}) , 'double' ))
                XLine_New_String_Check(i,Xline_WhichColumn_Name) = 1;
            end
        end
        fprintf(fID_Xline_txt,'New linecode.mtx%s nphases=3 BaseFreq=60\t',XLine_New{i,↙
Xline_WhichColumn_Name});

        fprintf(fID_Xline_txt,'r1 = %f\t',XLine_New{i,Xline_WhichColumn_PosR});
        fprintf(fID_Xline_txt,'x1 = %f\t',XLine_New{i,Xline_WhichColumn_PosX});
        fprintf(fID_Xline_txt,'C1 = %f\t',abs(XLine_New{i,Xline_WhichColumn_PosC}*1e-6/↙
(2*pi*60)*1e9));
        fprintf(fID_Xline_txt,'r0 = %f\t',XLine_New{i,Xline_WhichColumn_ZeroR});
        fprintf(fID_Xline_txt,'x0 = %f\t',XLine_New{i,Xline_WhichColumn_ZeroX});
        fprintf(fID_Xline_txt,'C0 = %f\t',abs(XLine_New{i,Xline_WhichColumn_ZeroC}*1e-6/↙
(2*pi*60)*1e9));
        fprintf(fID_Xline_txt,'units=mi\n');
    end
    fprintf(fID_Xline_txt,'!Line Codes: End');
    fprintf(fID_Xline_txt,'\n!********************************** \n');

    fprintf(fID_Xline_txt,'\n!********************************** \n');
    fprintf(fID_Xline_txt,'!Line Definitions: Start \n');
    fprintf(fID_Xline_txt,'!Written by Arash \n');
    fprintf(fID_Xline_txt,'!Number of Lines = %.1f  \n\n', (NofRow_Xline -↙
Xline_Start_at_Row + 1));
    .
    .
    .
```

Figure 3.9. Snapshot of model constructing part related to overhead lines in PSCMD transfer application to transfer power system circuit model data from UP spreadsheet into OpenDSS.

3.5. Transferring Power System Circuit Model Data From Unified Platform into GridLAB-D

GridLAB-D is a DOE-funded open-source software developed at Pacific Northwest National Laboratory (PNNL) in collaboration with industry and academia [36], [37]. GridLAB-D is a multi-physical domain modeling (power, weather, market) and simulation tool to simulate and analyze power systems, including micro-grids [38], [39]. GridLAB-D is a powerful modeling and simulation tools for time–series simulation in power systems with widely disparate time scales, ranging from sub-seconds to many years. Hence, GridLAB-D provides capabilities for users to analyze the progressive development of smart grids and the power systems with high penetration of renewable integration [40]–[42]. GridLAB-D was first and foremost developed as a residential load simulator; other modules were then added for grid simulations.

Similar to OpenDSS, GridLAB-D is a script-based tool so it does not have a GUI to build a circuit. Here, an application to transfer PSCMD from a UP spreadsheet to GridLAB-D is developed in MATLAB. This application reads the circuit model data stored in the UP spreadsheet and, after some initializations by the user, it generates a text file to build the power system circuit model in ".glm" format file based on the GridLAB-D language and format. The general scheme of importing PSCMD from UP spreadsheet into GridLab-D, as shown in Figure 3.7, is similar to the one for OpenDSS since both of them are script-based software. However, the PSCMD transfer applications are different from each other since their languages and formats to build a circuit are different.

Similar to OpenDSS, the first part of the PSCMD transfer application for GridLab-

D is designed for users to initialize certain parameters. In addition to the previously mentioned ones, these parameters may include ac frequency, the desirable load-flow solver method such as Newton-Raphson (NR) or Forward-Backward-Sweep (FBS), the Swing bus name if FBS method is selected, start and stop time of simulation in time-series simulation, and the nodes where the user wishes to place meters.

The meters provide a measurement point for power and energy on the system at a specific point. The user can select measurement points individually, in a set such as measurement points={'node1','node2',…}, or choose measurement points={'whole nodes'} to place a meter for each nodes of the system. The solver method is assigned through the parameter solver method in the PSCMD transfer application. Furthermore, the user is asked to specify a name for the output ".glm" file in this part. Figure 3.10 shows a snapshot of the user initialization part in developed PSCMD transfer application. Parts (2) and (3) of the PSCMD transfer application are designed to parse PSCMD from the UP spreadsheet and store them in the MATLAB workspace. It is worth mentioning that storing PSCMD in structure fields for each object is more convenient in this case, as shown in the snapshot in Figure 3.11. Parts (4), (5) and (6) of the PSCMD transfer application, shown in Figure 3.7, are organized to replace the value of GridLAB-D objects properties with the object structure field, related to PSCMD , stored in MATLAB workspace. As it can be seen in Figure 3.12, the script structure in this case is divided into two main parts of node object creation and link object creation. The reason is that nearly all objects within the power-flow module of GridLAB-D are derived from two primary objects of node and link. The primary responsibility of nodes is to act as an aggregation point for the links that are attached to it, and to hold the current and voltage values that are used in the matrix

calculations done in the link. Each object, no matter if node or link, has different variables called object properties. Each object property should be initialized with a value at the start of the simulation. As illustrated, the .glm file that describes the circuit with its different components and defines their parameter in GridLAB-D is created by the PSCMD transfer application. After the conversion, the .glm file is sent along with the comma-separate value (.csv) files to be run by GridLAB-D. These .csv files contain the values of time-variant object properties inside the .glm file to do time-series simulation. The user needs to follow a procedure similar to the one for OpenDSS to transfer the circuit model data prepared based on the UP format into GridLab-D.

User Initialization

1 Define SwingBus Structure;

```
// specify the swing bus node parameters
SwingBus.name=NULL;
SwingBus.nominalvoltage=NULL;
SwingBus.phases=NULL;
```

2 Define Power Grid Frequency;

3 Define measured nodes;

```
measurment_node={'whole nodes'};//will place
meter for whole nodes
Or

measurment_node={'N1,N2,…'};//will place
meter for specified nodes
```

4 Define simulation times;

```
Starttime=NULL;// will indicate Simulation
start time
Stoptime=NULL;// will indicate Simulation
stop time
Timezone=NULL;// Set the timezone for
the simulation
```

5 Define solver method;//choose powerflow solver method between "NR" and "FBS"

6 Specify a output ".glm" file name;

Figure 3.10. Snapshot of user initialization part in PSCMD transfer application to transfer power system circuit model data from UP spreadsheet into GridLAB-D.

Read Data from UP Spreadsheet and Store in Structure Fields

```
1   xlsread('Unified Platform', 'node object sheets'); //Read data from node object
    sheets of UP and store in node structure Fields

        nodeobject.name=node object sheet (name);
        //for node, load and cap bank objects
        nodeobject.naminalvoltage=node object sheet (nominal voltage);
        //for node, load and cap bank objects
        nodeobject.phases=node sheet object (phases);
        //for node, load, cap bank objects
        nodeobject.FromNode=node sheet object (From Node);
        //for load and cap bank objects
        nodeobject.constant_power_A =node sheet object (Power A);
        //for load object
        .
        .
        .
2   xlsread('Unified Platform', 'link object sheets'); //Read data from link object
    sheets of UP and store in link structure Fields

        linkobject.name=linekobject sheet (name);
        //for overhead line, cable, trans, regulator and switch objects
        linkobject.naminalvoltage=link object sheet (nominal voltage);
        //for overhead line, cable, trans and regulator objects
        linkobject.phases=link sheet object (phases);
        //for overhead line, cable, trans, regulator and switch objects
        linkobject.FromNode=link sheet object (From Node);
        //for overhead line, cable, trans, regulator and switch objects
        linkobject.ToNode=link object sheet (To Node);
        //for overhead line, cable, trans, regulator and switch objects
        linkobject.PowerRating=link object sheet (Power Rating);
        //for transformer object
        linkobject.status=link object sheet (status);
        //for switch object, "CLOSED" or "OPEN"
        .
        .
        .
```

Figure 3.11. Snapshot of data parsing part in PSCMD transfer application to transfer power system circuit model data from UP spreadsheet into GridLAB-D.

Construct Model Based on GridLAB-D Structure

1 Create Node Objects

```
Object meter{        // for measured nodes
        name= nodeobject.name;
        Phases= nodeobject.phases;
        Bustype= SWING;  //for Swing Bus
        nominal_voltage= nodeobject.naminalvoltage;
        .
        .
        .
        }

Object load{
        name= loadobject.name;
        Phases= loadobject.phases;
        from= loadobject.FromNode;
        Parent= loadobject.parent;
        .
        .
        .
        }

.
.
.
```

2 Create Link Objects

```
Object overhead_line{
        name= overheadobject.name;
        Phases= overheadobject.phases;
        from= overheadobject.FromNode;
        to= overheadobject.ToNode;
        .
        .
        .
        }

Object underground_line{
        name= overheadobject.name;
        Phases= overheadobject.phases;
        from= overheadobject.FromNode;
        to= overheadobject.ToNode;
        .
        .
        .
        }

 .
 .
 .
```

Figure 3.12. Snapshot of model construction part in PSCMD transfer application to transfer power system circuit model data from UP spreadsheet into GridLAB-D.

3.6. Transferring Power System Circuit Model Data From Unified Platform into DEW

The Distribution Engineering Workstation (DEW) software package is developed by Electrical Distribution Design, Inc (EDD). The Integrated System Modeling approach in DEW (DEW-ISM) allows a single model to be used for different functions within a utility, such as design, planning and operation. The DEW scope includes transmission and distribution networks in steady-state and time-series analyses. DEW has a user-friendly GUI and models can be displayed over geographical-based models such as Google Earth, Bin Maps and GIS. DEW is the only solution that relies on a graph theory-based approach called graph trace analysis (GTA). GTA is a topology iterator method that iterates from one node to the neighboring node and updates the network connectivity and physical characteristics like impedance, voltage and current flow. In DEW-GTA, the system equations can only have knowledge of variables that can be measured at the terminals or boundaries of a component. This is in contrast to other software tools in this chapter, all of which use a matrix-based approach. The matrix-based network formulation shows a global view of the system, simultaneously accounting for the admittances between every node. A typical distribution network has a large admittance matrix which, although it is sparse, requires a computationally intensive power flow calculation. The GTA power flow method in DEW is naturally distributed and fast without the need for maintaining a large system admittance matrix. DEW also has the potential to incorporate data from across a utility, such as SCADA measurements and statistical load information.

All components, their parameters and their connectivity in DEW are stored in an

MS Access database, with a GUI to drag and drop components. The model can be saved in the Access database along with component data, or the model can be stored as a standalone file. DEW does not have a built-in application to import models from Excel directly. However, it has the model data mapper tool to import models with MS Access into the DEW environment. Therefore, the first step is to convert the UP Excel sheet into an MS Access version. Figure 3.13 illustrates the general block diagram for UP model conversion into DEW.

The data mapper application then changes the columns format from the UP version into the DEW version (see Step 5 in Figure 3.13). The DEW data mapper loads UP MS Access tables and maps them into a new data structure, then saves them into the new DEW MS Access database. The next step is to check component tables and their nametags to assure that the conversion process is correct. The component tables are checked with the "Component Manger Application" embedded in the DEW software. Figure 3.14 shows the snapshot of a conductor in the DEW database. As noted earlier, different software may present component parameters in different units. For example, conductor impedance can be in ohms, ohms per mile, ohms per 1000 feet, or ohms per kilometer. During the model conversion, unit conversion for component parameters is therefore a crucial task.

The final step for the DEW model conversion is running power flow analysis to check its convergence. Moreover, power flow results will be compared with the model represented in UP format.

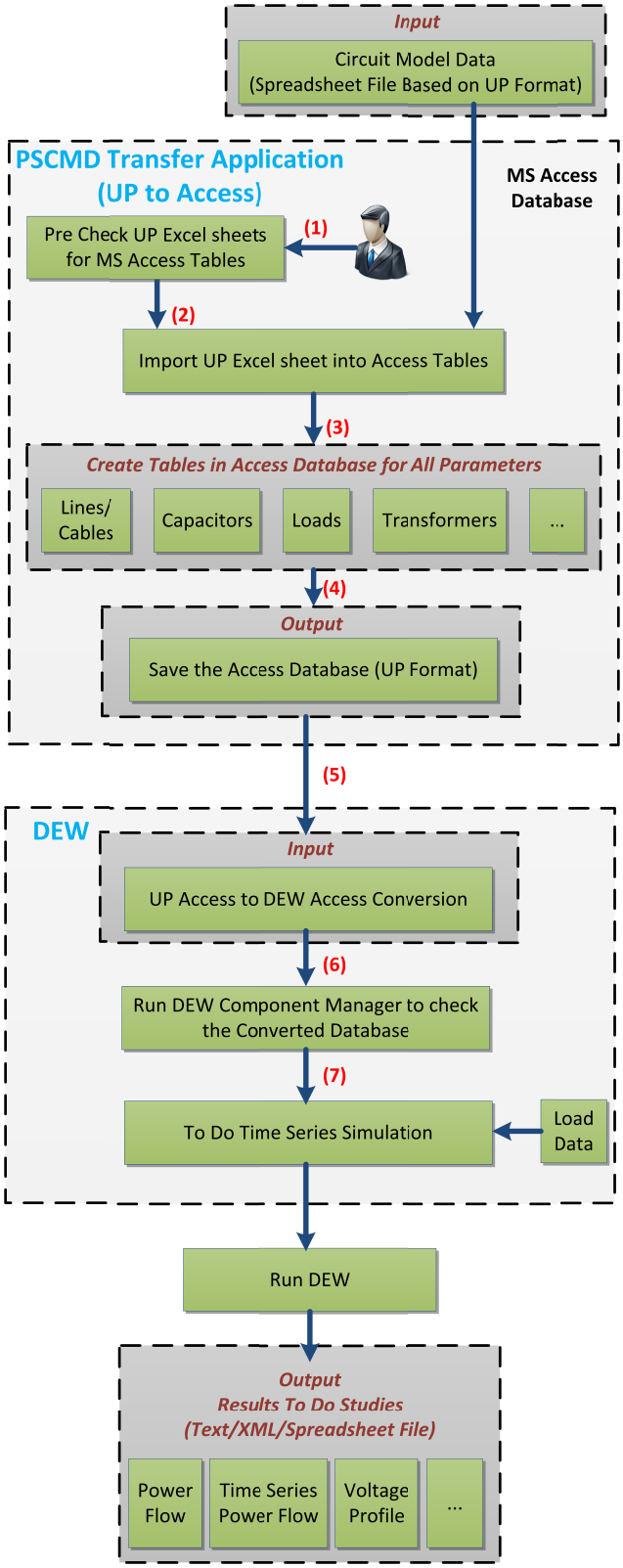

Figure 3.13. General scheme of importing power system circuit model data from UP spreadsheet into DEW using PSCMD transfer application.

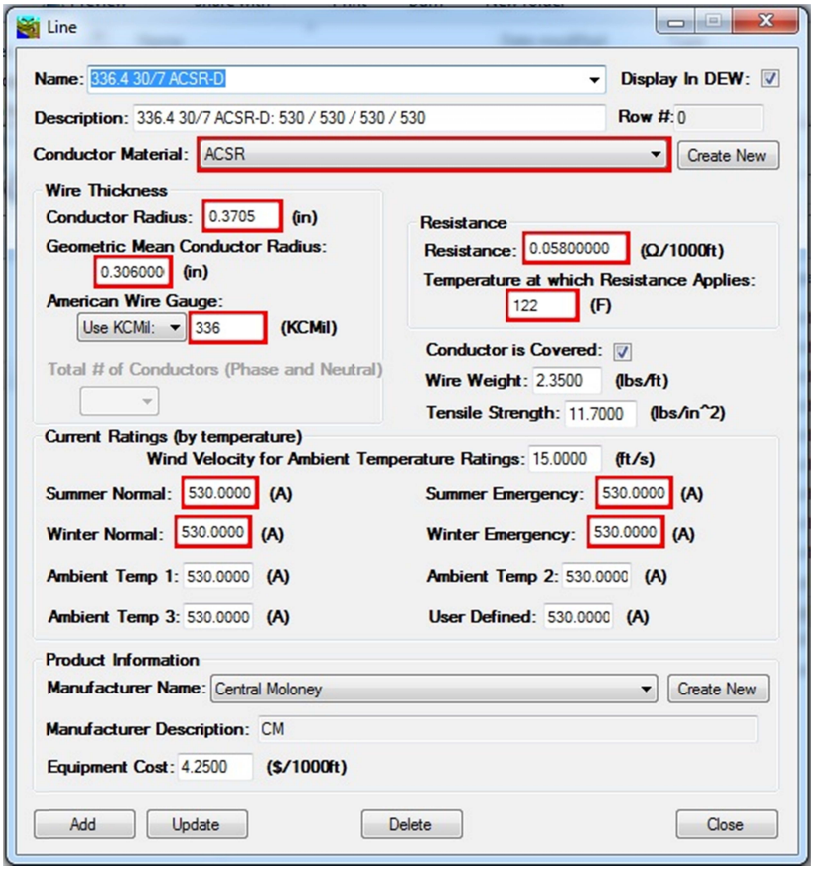

Figure 3.14. Snapshot of component manager in DEW to transfer power system circuit model data from UP spreadsheet into DEW.

3.7. Simulation Results

In order to verify the effectiveness of the proposed UP and test the functionality of developed PSCMD transfer applications, the circuit model data of two different sample circuits were imported into ETAP, OpenDSS, GridLAB-D and DEW using the developed PSCMD transfer applications: (1) a test circuit built by authors as an example and (2) an actual sample circuit from a California utility. The load-flow analysis of structured circuits is performed in each software and the obtained results are compared with provided results from CYME to check the correctness of structured circuits. The following is general

information about two imported circuits:

- The circuit model data of the test circuit contains 6 loads which are illustrated in Table 3.1; two 1200-kVAR capacitor banks connected to nodes N4 and N8; 10 nodes (N1 to N10); 5 cables; one overhead line; and one transformer (12/0.48 kV) connected between nodes N5 and N9.
- The actual sample circuit from California utility contains 39 loads with total rating of 6.4 MW and 4 MVAR; four 1800-kVAR capacitor banks (two of which are connected to the grid in this case of study); 291 nodes; 119 cables; 36 overhead lines; 10 PV generators with total capacity of 5 MW; and 10 transformers (12/0.21 kV).

The obtained load flow results for test circuit are illustrated in Table 3.2. Moreover, partial load flow results of the actual sample circuits are illustrated in Table 3.3 and Table 3.4. We note that the obtained results match precisely with each other as well as results available from CYME, which confirms the correctness of the reconstructed circuit and the proper functionality of PSCMD transfer applications to transfer the circuit model data from UP spreadsheet to each software.

TABLE 3.1
LOAD SUMMARY OF SAMPLE CIRCUIT.

Name	Node	kW	kVAR	Voltage Rating	Power Factor (%)
LD1	N4	3000	1800	7.2 kV	80
LD2	N5	4500	2700	7.2 kV	80
LD3	N7	3000	1307.7	7.2 kV	90
LD4	N8	1500	653.7	7.2 kV	90
LD5	N9	1500	900	0.48 kV	80
LD6	N10	3000	1800	7.2 kV	80

TABLE 3.2

LOAD FLOW RESULTS OF TEST CIRCUIT.

Bus	Active Power (kW)				
	Original (CYME)	ETAP	OpenDSS	GridLAB-D	DEW
N1	14527	14536	14534	14535	14528
N2	14510	14518	14516.8	14517	14513
N3	14510	14518	14516.8	14517	14517
N4	14501	14509	14508	14508.6	14508
N5	8925	8931	8930.4	8931.51	8927
N6	4117	4120	4119.6	4120.16	4115
N7	4050	4053	4052.4	4052.9	4053
N8	1349	1350	1349.8	1350	1349
N9	1199	1200	1199.9	1200	1200
N10	2400	2400	2400	2400	2400

Bus	Reactive Power (kVAR)				
	Original (CYME)	ETAP	OpenDSS	GridLAB-D	DEW
N1	7982	7989	7988.7	7988.6	7986
N2	7963	7969	7969.4	7969.2	7968
N3	7963	7969	7969.4	7969.2	7969
N4	7954	7960	7961.4	7961.25	7957
N5	4852	4857	4857.2	4857.65	4855
N6	1141	1144	1144.1	1144.17	1144
N7	1045	1048	1047.7	1047.94	1047
N8	-265	-263	-263.1	-263.5	-263
N9	899	900	899.9	900	900
N10	1800	1800	1800	1800	1800

TABLE 3.3

PARTIAL LOAD FLOW RESULTS FROM ACTUAL SAMPLE CIRCUIT (ACTIVE POWER).

Bus	Active Power (kW)				
	Original (CYME)	ETAP	OpenDSS	GridLAB-D	DEW
90091686_02658	276	277	276.7	276.7	272
PME4896-3_02658	357	357	356.9	356.9	358
833E_02658	380	380	380	380.1	378
107988591_02658	403	402	402	402.3	401
GS0713-2_02658	449	447	447	447	448
PME4896-4_02658	550	552	550	549.2	554
J057-1P_02658	576	576	575.5	575.5	575
PME5100-1_02658	805	806	805.6	805.6	811
RCSG777-3_02658	833	827	832.1	832.6	836
PMH5099-3_02658	1106	1105	1105.4	1105.5	1104
48201834_02658	1255	1253	1252.8	1252.8	1253
PMH5099-4_02658	1717	1716	1715.5	1715.7	1719
RCS5187-4_02658	2827	2826	2825.7	2826.3	2825
RCS5187-3_02658	3150	3147	3146.7	3147.3	3153
148639376_02658	3584	3584	3581.2	3583.7	3748
PS0372_02658	4207	4209	4205.5	4208.7	4211
02658	3723	3726	3720.9	3729	3725

TABLE 3.4

PARTIAL LOAD FLOW RESULTS FROM ACTUAL SAMPLE CIRCUIT (REACTIVE POWER).

Bus	Reactive Power (kVAR)				
	Original (CYME)	ETAP	OpenDSS	GridLAB-D	DEW
90091686_02658	167	167	166.3	166.8	166
PME4896-3_02658	224	223	223.1	223.24	222
833E_02658	238	237	237	237.2	239
107988591_02658	252	253	252.8	252.9	254
GS0713-2_02658	273	275	264.9	271.25	263
PME4896-4_02658	-1348	-1349	-1358	-1363	-1356
J057-1P_02658	360	360	359.3	359.3	361
PME5100-1_02658	-1233	-1226	-1232.5	-1225.4	-1229
RCSG777-3_02658	1098	1101	1103.9	1105.1	1099
PMH5099-3_02658	693	693	692.8	693.18	689
48201834_02658	-970	-960	-967.6	-958.8	-966
PMH5099-4_02658	-2419	-2402	-2415.9	-2400	-2398
RCS5187-4_02658	-1730	-1712	-1727.1	-1710	-1707
RCS5187-3_02658	-1528	-1509	-1524.4	-1507.4	-1314
148639376_02658	-1301	-1278	-1299.2	-1274.2	-1294
PS0372_02658	-912	-893	-914.9	-888	-904
02658	542	557	547.8	585	574

3.8. Discussion

While the conversion process was successful for all four software tools in this chapter, there are several differences among their features that merit discussion and are summarized in Table 3.5.

• ETAP and DEW have a GUI to drag and drop components from a library, while

both OpenDSS and GridLAB-D have a script-based environment. Thus, users of OpenDSS and GridLAB-D need to write a text file according to the language of related software to define all components, parameters as well as their connectivity.

• ETAP has a useful feature to display a visual circuit schematic even if the XY coordinates of nodes are not imported into ETAP, which helps in the debugging stage. OpenDSS and DEW require XY coordinates to create a circuit schematic. GridLAB-D does not produce a schematic at all.

• GridLAB-D, OpenDSS, and DEW can model the line/cable based on ABC (phase-to-phase) format of line/cable impedances, while ETAP cannot. Moreover, ETAP, OpenDSS, and DEW can model the line/cable based on PNZ (positive-negative-zero) sequence format of line/cable impedances while GridLAB-D cannot.

• Software varies in its capability to model the capacitance of lines/cables, which can be important in distribution level circuit studies since the capacitance of underground cable is considerable and may have a significant impact on the load flow results. ETAP, DEW and OpenDSS have this capability while GridLAB-D does not. According to the simulation results shown in Table II and III, however, GridLAB-D load flow results nevertheless match with the others.. The reason for this is that the capacitances of lines/cables are imported as individual capacitors (such as load) at the beginning and ending-point of lines/cables in the PSCMD transfer application.

• The voltage rating of all nodes should be assigned one by one in GridLAB-D, while ETAP, OpenDSS and DEW get it automatically after connecting the main feeding point and assigning the connectivity of the circuit.

TABLE 3.5

SUMMARY OF SOFTWARE ABOUT LOAD FLOW ANALYSIS.

	ETAP	OpenDSS	GridLAB-D	DEW
GUI	Yes	No	No	Yes
Circuit schematic	Yes	Yes	No	Yes
Line impedances in ABC format	No	Yes	Yes	Yes
Line impedances in PNZ sequence format	Yes	Yes	No	Yes
Capacitance of lines/cables	Yes	Yes	No	Yes
Voltage rating of nodes is required to be assigned	No	No	Yes	No

3.9. Conclusion

Emerging technologies are introducing new devices and phenomena to power distribution circuits, creating a need for new software capabilities to investigate them since the existing software may not support them. Consequently, users may need to transfer their PSCMD among different software tools to take advantage of specific features in new software. Due to the considerable diversity of software tools on the market to simulate and study power system circuits, it has been a challenge to transfer PSCMD and reconstruct circuits in different software tools. With the UP scheme proposed in this chapter, all PSCMD are presented in a spreadsheet file based on a single defined format. As a result, only two unidirectional applications are required to transfer PSCMD from the UP spreadsheet into any software and vice versa, instead of a combinatorial number of conversion applications between multiple software. In this chapter, PSCMD transfer applications were developed in MATLAB for ETAP, OpenDSS, DEW, and GridLAB-D and tested on two circuits to confirm that the load flow results agree and the circuit conversions have been successful.

The conversion applications presented in this chapter is available to utility engineers and researchers to facilitate their work. Future development may expand the conversion applications to include other commonly used software tools.

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Chapter 4: Investigation of Large-Scale Solar Energy Penetration in Power Distribution Circuit

4.1. Introduction

In the recent years, an unprecedented growth in power usage is observed. Renewable and clean alternatives power generation technologies have a significant role to respond future power demand due to an increased concern for power generations which are environmentally friendly and less reliant on fossil fuels. Solar energy is one of the most widely-used and major type of renewable power generation technologies [1]–[3]. Solar energy is continuously integrated into the power grid in the form of customized distributed generation (DG) systems in grid-connected or standalone configurations. The appropriate sizing and placement of solar systems, which generate power locally to fulfill consumer demands, helps to reduce power losses and avoid transmission and distribution system expansion [3]–[6].

Solar energy was mainly used for off grid applications like rural electrification, water pumping and heating until a decade ago while most of the newly installed solar systems are integrated into the distribution-level power grid [1]. Many utilities either receive incentives or are forced by renewable portfolio standard (RPS) to install solar systems on their feeders [2]. For example, California's RPS is one of the most ambitious renewable energy standards in the USA which mandates power utilities and electric service providers to generate 33% of total required electric energy from eligible renewable energy resources by 2020. In addition, recent technological advances in power electronics and energy storage devices have increased the opportunity for solar energy penetration.

In the past couple of years, solar energy has attracted significant attention worldwide in both academia and industry. From the academic pint of view, extensive

researches on viability studies, computer modeling, impact investigation, control, etc., have been done [5]–[11]. In industry, the utility-scale solar plants have been built in the range of hundreds of MW such as 550MW "Topaz Solar Farm" in CA, USA (300 MW completed up through January 2014), 354MW "Solar Energy Generating Systems" in CA, USA, 250MW "Valley Solar Ranch" in CA, USA (completed in 2013), 200MW "Solaben Solar Power Station" in Logrosán, Spain. More projects are under construction such as 2GW power station in Mongolian desert, China, 1.5GW "Solar Energy Project" in Morocco and 1GW "Quaid-e-Azam Solar Park Project" in Bahawalpur, Pakistan. This shows a rapid growth of solar energy in clean power generation in this century. Solar energy is also considered and implemented at the range of couple of MWs in the power distribution network - owned either by the utility or by private power producers - or in the small range for residential applications. However, some technical problems such as voltage variation (especially in application of residential or distribution power circuits), and unpredictability and time-varying (intermittency) nature of solar energy, due to photovoltaic (PV) panel shading, challenge its application.

Large-scale solar plants, in the range of couple of MWs, usually have nominal capacities compatible with medium voltage feeders and thus, require step-up transformers at the point of common coupling. The energy produced by these solar plants decreases the apparent load and possible excess energy flows into the grid [1], [2]. The solar plant inverters usually inject power into the grid at unity power factor and the utility must undertake all the VAR requirements. IEEE 1547 standards on DG interconnection with the grid require that there must be no direct communication or control between the inverter

and the utility which implies that for any deviation in the grid voltage/frequency, the inverter must disconnect itself from the grid until normal conditions resume [8]. Therefore, the inverters in the residential application are required to have overcurrent and under/over voltage protection schemes to prevent islanding and thus prevent the solar plant from injecting power into the grid in the event of a fault.

In order to effectively investigate the impacts of large-scale solar energy penetration on the power distribution system, certain characteristics unique to this type of resources must be considered, namely the previously mentioned time-varying nature of solar energy [12], [13]. Impacts of large-scale solar energy penetration includes, but not limited to, power quality, and operation of load tap changer, capacitor banks and voltage regulator [13], [14]. The industry, as a whole, has been studying and considering the issues related to solar energy penetration into the power distribution grid. However, much of this effort has been limited to using simplified feeder models, typical feeder data, as well as single "snapshot" in time, rather than considering the time-varying nature of the solar energy and how this interacts with the grid [2], [13], [15], [16]. This may be in part, due to lack of detailed distribution feeder data, lack of solar energy time-series data, or perhaps even limitations due to the simulation software utilized for the analysis [17], [18].

This chapter provides an investigation of impacts of large-scale solar energy penetration on a power distribution circuit from Sothern California Edison (SCE), a utility company in California, US. Originally, the mentioned circuit was modeled in CYME software tool. However, CYME software tool does not have the capability to do the time-series simulation which is required for studies of time-varying events such as solar energy

penetration. In order to investigate the solar energy penetration in a the SCE circuit, Open source Distribution System Simulator (OpenDSS) software tool is used which is well-suited for evaluating the impacts of time-varying events on distribution systems. In [19] , an application has been developed to transfer the power system circuit model data (PSCMD) from CYME to OpenDSS in order to conduct this study. After transferring the PSCMD into OpenDSS, the circuit is run and the obtained load flow results are compared with the original results to verify the correctness of the remodeled circuit in OpenDSS.

The rest of this chapter is organized as follows. Section 4.2 discusses the impacts of time-varying solar energy penetration on the power distribution system. In Section 4.3, the necessity of the time-series measurement data and performing time-series simulation in order to investigate the intermittency of the solar energy generation is explained. Moreover, the requisite of interpolating and resampling measurement data, which are unequally spaced time-series data, and converting them to equally spaced time-series data as well as the effect of resampling time-interval on the amount of interpolation error are discussed in Section 4.4. Two applications are developed in Matlab to do interpolation and resampling, and calculate the amount of interpolation error for different resampling time-intervals to find the proper resampling time-interval. In Section 4.5, considerations regarding validation of circuit model are discussed and approaches to validate the model components including line/cable, load and solar energy generation are presented. Moreover, an approach based on the cumulative distribution, regarding the length for lines/cables types and the power rating for loads, is presented to prioritize which loads, lines and cables the meters should be installed at to have the most effect on model

validation. The number of required meters as a function of percentage of whole circuit to be validated is illustrated. In Section 4.6, the time-series simulation results using the actual measurement data are provided to validate the circuit model. Furthermore, the impacts of high-variability points of solar energy generation on the operation of capacitor banks and voltage regulator are discussed in Section 4.7. Finally, Section 4.8 concludes the observations and studies.

4.2. Impact of Time-Varying Solar Energy Penetration

The penetration of large-scale solar energy to distribution systems, which have traditionally been designed to operate in a radial fashion, may result in potential impacts that need to be studied and planned for [18], [20], [21]. Since the integration of solar energy is expected to grow through the next decade and beyond, it is critical to understand its associated effects on distribution system planning and operation. Depending on the scale of solar energy deployment, impacts can be local (e.g., at individual feeder or substation level) or system-wide (e.g., affecting several feeders and substations across the utility's service territory and including sub-transmission and transmission facilities). The impacts of large-scale solar energy penetration on the distribution system can be categorized as follows:

- Reverse power flow issues: voltage regulation and line losses may be affected since the excess power generation of solar plant flows to upstream on a distribution system which is traditionally designed for one way power flow.
- Protection issues: overcurrent protection for electric power systems depends on the

coordinated operation of many devices, including circuit breakers, various types of fuses, relays, reclosers and sectionalizing switches. The presence of solar plants introduces new sources of fault currents that can change the direction of flow, introduce new fault-current paths, increase fault-current magnitudes, and redirect ground-fault currents in ways that can be problematic for certain types of overcurrent protection schemes.

- Integration issues: If the voltage levels go below the voltage sag threshold due to the high demand conditions, inverters must be disconnected according to IEEE 1547 standards. Since the loads remain connected, the feeder may see an increase in demand causing to deteriorate the situation and increase the chance of a blackout.
- Operation issues: Due to the fast transient of cloud (in the range of couple of seconds), high-variability of solar generation as a result of PV cloud shading leads to voltage fluctuation. Consequently, this can affect the operation of equipment in system such as tap changer, voltage regulator and capacitor bank. Therefore, the appropriate setting of the equipment, especially their timing, and their coordination to operate properly is an important issue.

Consequently, the investigation of large-scale solar energy penetration impacts on the distribution system is necessary for the successful integration of solar plants and operation of power grid. The common concern in investigating the impact of solar energy in power distribution system is inevitable intermittency of the solar irradiation, which is in turn, depends on weather conditions and consequently, solar energy generation varies over time. Another fact is that how intermittency of solar energy generation, especially high-

variability points, might affect other customers as well as interact with grid operations. Therefore following should be considered in the investigation process:

- Development of distribution models to evaluate the impacts of large-scale solar energy penetration.
- Identification and development of the necessary distribution system studies and analysis appropriate for determining the impacts of large-scale solar energy penetration.
- Consideration of the highest variability observed on the measurement data.

The major factors determining the impacts of solar energy penetration are: (1) size and layout of the solar facility; (2) centralized vs. distributed; (3) local weather patterns. In [1], a comprehensive report regarding the impacts of large-scale solar energy penetration, such as reverse power flow, voltage profiles variation, increased operations of substation tap changers, voltage regulators and capacitor banks as well as an increase in losses, on utility feeders is provided.

4.3. Modeling the Intermittency of Solar Energy

4.3.1. Measurement Time-Series Data Used by Model:

The best source of data in order to perform time-series investigation, no matter the analysis considers large-scale centralized solar plant or high penetration of small-scale solar energy, is the high-resolution time-series measurements taken at the plant(s) locate(s). The benefits of using high-resolution data for solar energy penetration analysis

include:

- capturing local cloud patterns as it relates to the solar energy deployment being considered in the analysis
- observation of high-variability points at the output of solar system due to the PV cloud shading
- scalability property to represent large-scale solar energy penetration
- accurate estimations of local solar energy production
- and utilization of solar energy measurement with time-coincident load measurement data

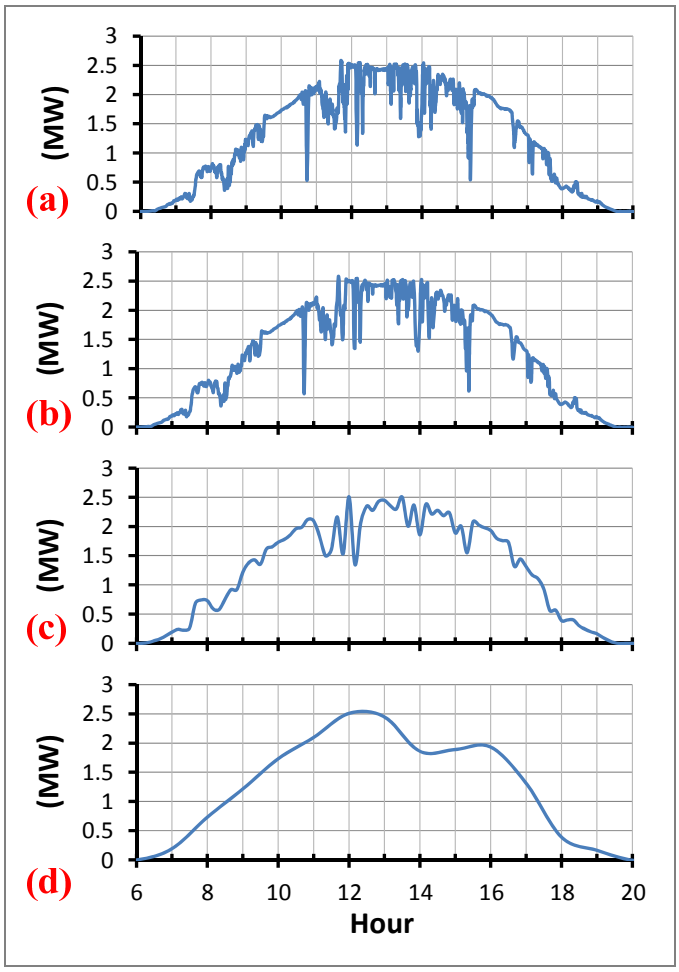

Figure 4.1. The power generation of 3.5MW centralized solar plant: (a) raw measurement data; and interpolated data with resampling time-interval of (b) 60s; (c) 10min; (d) 60min.

In the event local high-resolution data may not be available, other alternatives such as Proxy data or typical meteorological year (TMY) data can be used instead. However, these kinds of data are more suitable to perform long-term simulations at the hourly resolution (for instance for energy calculations) since they don't account for cloud transients that result in solar system output intermittency which would be of concern to utility operations. Another fact is the resolution of measurement data which has significant effect on obtaining the correct insight of system reaction to large-scale solar energy penetration. For example, Figure 4.1(a) depicts 14 hours (from 6:00 to 20:00) raw

measurement data of output power of 3.5MW centralized solar plant integrated to the mentioned SCE circuit. Figure 4.1(b) to (d) show the interpolated data of raw measurement data with different resampling time-interval from 60 seconds to 1 hour. The inverse of the time-interval, which is the time between samples, is the sampling frequency. In practice, in order to reduce the data storage size, the measurement is typically done using variable sampling time-interval. For example, the provided raw measurement data by SCE are sampled whenever the amount of its variation is more than the predefined threshold. This kind of date is not compatible to any simulation software tool since they are typically run the circuit at a fixed sampling time-interval. Thus, it is necessary to interpolate these raw data and resample it at constant sampling time-interval. As it can be seen in Figure 4.1, increasing the resampling time-interval of interpolation affects the data resolution and results in missing the high-variability points, which are of greatest concern, due to PV cloud shading that occurs between 10:00 and 16:00. Therefore, the cloud transients that could result in unacceptable voltage fluctuations and increased operation of tap changer and capacitor bank would be missed and not taken into consideration. Consequently, selection of sampling time-interval is a critical issue and it depends on the type of required analysis. In general, the following sampling time-interval are recommended:

- Energy impacts: hourly
- Voltage fluctuations: seconds – minutes
- Steady-state overvoltage: minutes

This applies for both the underlying time-series measurement data used by the model as well as the simulation time step. In Section V, the proper selection of sampling

time-interval and its effect on the amount of error are discussed in detail. Moreover, the developed application to figure out the best sampling time-interval and keep the amount of error below the specific value is presented.

4.3.2. Time-Series Simulation

The time-series simulation is a sequence of analysis, typically at successive points in time spaced at uniform time intervals. As mentioned previously, the time-varying nature of solar energy is the major challenge in investigation the impact of large-scale solar energy penetration either in terms of voltage regulation, voltage fluctuations, annual energy losses or impact on peak demand or operation of tap changer or capacitor bank. Figure 4.2 shows the power generation of both 1.5MW and 3.5MW centralized solar plants of SCE circuit at three adjacent days from Aug. 2, 2013 to Aug. 4, 2013. As it can be seen, the power generation is very smooth on Aug. 4, 2013 while it varies up to -85% within 60s on Aug. 2, 2013 and Aug. 3, 2013 which shows the significant intermittency of solar energy generation. If a single "snapshot" in time, for example the peak value of solar energy generation, is considered, the obtained results may give the incorrect insight into effects of solar energy intermittency. This issue is also clearly shown in Figure 4.3 illustrating the line active and reactive power losses in the SCE circuit for the three cases of (1) baseline (without solar energy penetration); (2) 30% and (3) 100% of nominal solar energy penetration which is 3.7MW (53% of total load demand). Both Figs. 2 and Figure 4.3 confirm the necessity of the time-series simulation rather than single snapshot simulation.

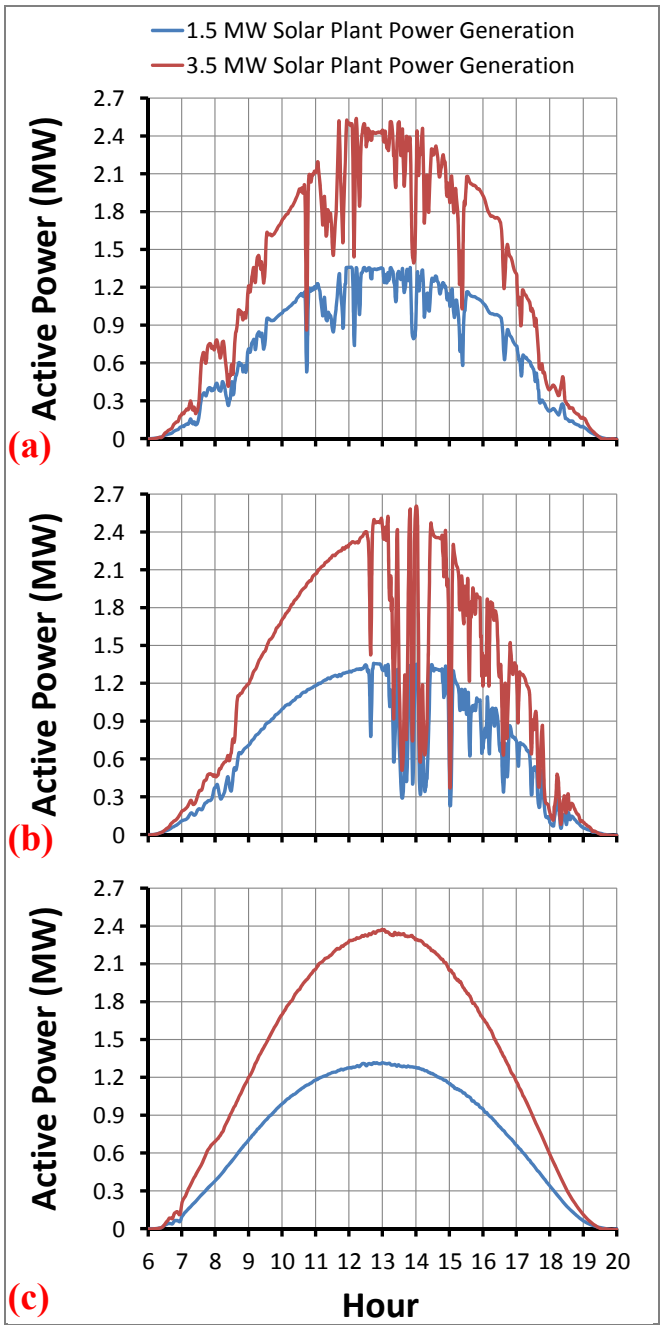

Figure 4.2. The measurement power generation of 1.5MW and 3.5MW solar plants on: (a) Aug. 2, 2013; (b) Aug. 3, 2013; (c) Aug. 4, 2013.

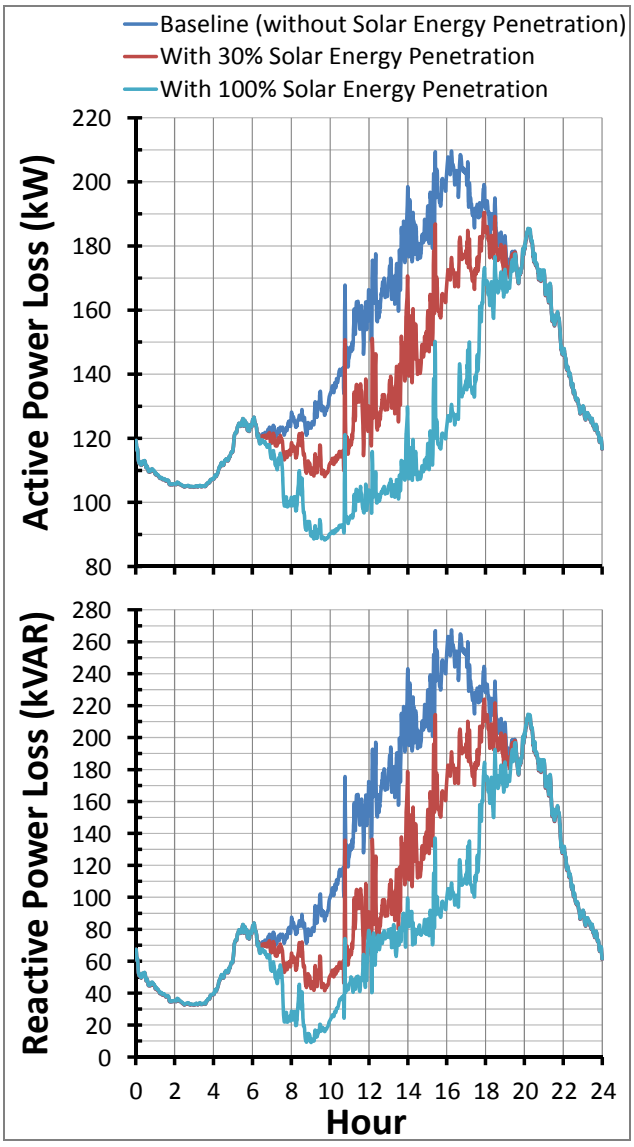

Figure 4.3. The active and reactive power loss of lines and cables obtained from OpenDSS with baseline load demand, and at presence of 30% and 100% solar energy penetration of 3.7MW (53% of measured total load demand).

4.3.3. Circuit Model Used for Time-Series Simulation

In order to investigate the impact of large-scale solar energy penetration on the power distribution system, a full multi-phase representation of the power distribution circuit is required. Distribution system represents the final link between the bulk power

system and the consumers. Typically, positive-sequence models, assuming the system is balanced, are used by software tools such as GE PSLF or Siemens PSS to perform the load flow and stability analyses at power transmission system level. However, this is not suitable for power distribution system modeling since distribution circuits are typically unbalanced systems due to line construction configurations. They have both three-phase and single-phase laterals and loads and have radial or maybe weakly mashed topology. Therefore, most of the software tools to analyze the power distribution system consider full three-phase analysis. On the other hand, most power distribution system simulators such as ETAP or CYME do not have a feature to perform the time-series simulation which is essential in investigation of solar energy penetration due to its time-varying nature. Consequently, it is required to use a software tool with the capability of time-series simulation as like as OpenDSS, GridLAB-D or DEW which have the feature of time-series simulation. In this chapter, the OpenDSS software is used to investigate the SCE circuit. OpenDSS is an open-source electric power Distribution System Simulator (DSS) for supporting distributed resource integration and grid modernization efforts [12], [20], [22]. It performs nearly all frequency domain (steady state) analyses commonly performed on electric utility power distribution systems; however, it does not perform time domain studies [23], [24]. In addition, it supports many new types of analyses that are designed to meet future needs related to smart grid, grid modernization, and renewable energy research [17], [18], [23]. One of the significant features of OpenDSS is time-series simulation to study time-varying events, ranging from sub-seconds to years, of renewable energy resources such as wind or solar in power systems [2], [24]. Examples of time series are the hourly or monthly values of load profile. OpenDSS is a script-based tool where all

components and their parameters and connectivity are assigned in the script-based environment. In other words, it does not have any Graphical User Interface (GUI) to drag and drop a component (e.g., load) from its library and connect it to another component (e.g., cable). Moreover, it does not have any built-in feature yet to import PSCMD from a database, for example spreadsheet or MS Access. Therefore, it will take a long time to create any utility-scale circuit in OpenDSS containing hundreds of lines, cables, loads, etc. In [19], an application was developed in MATLAB to read PSCMD from CYME. This PSCMD transfer application creates a text file containing all lines, cables, loads, transformers, capacitors, circuit breakers, etc., based on the language of OpenDSS. The developed application is used in this chapter to transfer the PSCMD of SCE circuit from CYME to OpenDSS automatically. The obtained load flow results, at a few of nodes, are illustrated in Table 3.3 and 3.4 in previous chapter. As it can be seen, the obtained results match perfectly with results available from CYME which confirms the correctness of the remodeled circuit. Later, the model of SCE circuit created in OpenDSS can be run along with comma-separate value (.csv) files containing the values of time-varying object, such as load profile or solar energy generation, to do time-series simulation.

4.4. Data Conversion from Random Sampling Rate to Constant Sampling Rate

4.4.1. Development of Data Interpolation-Resampling (DIR) Application

Utilities typically sample and record any variable such as voltage, current or power based on dead-band method in which the variable is sampled if its increase/decrease exceeds a preset value. This method has the benefit of data compression; however, it generates "unequally spaced time-series data". A snapshot of the excel file containing actual measurement data of solar plant power generation is shown in Table 4.1, where the data are sampled and stored as an unequally spaced time-series data. Such data is perfectly fine if it is plotted for human to inspect it. In the event when there is a need to import the data into a circuit simulation software, its format will not be compatible to the simulation software since the destination power system simulator software tool, using the time-series data, can only run at fixed time step. In this chapter, a method and its associated application has been developed to resolve this issue by first interpolating the measurement data, which is unequally spaced time-series data, and then resampling it with a fixed sampling time-interval in order to converter it to equally spaced time-series data. Another reason to using this process is to synchronize different type of variables (for instance voltage and power) related to the same circuit. Synchronization means calculating the quantity of all variables at the common time vector with the constant time step as the same as the simulation time step in destination power system simulator software tool which uses time-series data of two or more type of variables to run the simulation.

The mentioned application, called data interpolation and resampling (DIR)

application, is developed in Matlab to read unequally spaced time-series data (i.e., measurement data) from an excel file, interpolate and resample them based on the user defined sampling time-interval and generate equally spaced time-series data. The general scheme of the developed DIR application is depicted in Figure 4.4. As the first step, developed DIR application reads the unequally spaced time-series measurement data from an excel file and stores them in cell variable in MATLAB. As the next step, the application read data from the cell variable, interpolate and resample them based on user defined sampling time-interval and then, store the generated equally spaced time-series data in a new cell variable. The new cell variable can be exported to another excel file and used as an equally spaced time-series data attached to the circuit modeled in OpenDSS to do time-series simulation. A snapshot of the exported excel file containing equally spaced time-series data with sampling time-interval of 30s is shown in Table 4.2 while the input data is the same as Figure 4.4. As the final step, the developed application produces a graph with four sub-graphs. As an example, Figure 4.5 shows the output graph of developed application for the measurement output power of 3.5MW solar plant on Aug. 2, 2013 with sampling time-interval of 30s. The first sub-graph is the actual measurement data and interpolated one. The second and third sub-graphs are the error between the actual and interpolated data in MW and percentage, respectively. The fourth sub-graph is the error between the actual and interpolated data in percentage of peak value of solar output power in that day (herein, Aug. 2, 2013) which is around 2.5MW in the first sub-graph of Figure 4.5.

TABLE 4.1

ACTUAL MEASUREMENT DATA STORED AS UNEQUALLY SPACED TIME-SERIES DATA

Date	Time	Power (MW)
8/2/2013	11:59:47 AM	2.50500
8/2/2013	12:00:17 PM	2.51200
8/2/2013	12:00:32 PM	2.50500
8/2/2013	12:01:17 PM	2.50200
8/2/2013	12:01:46 PM	5.49800
8/2/2013	12:02:46 PM	2.47600
8/2/2013	12:03:17 PM	2.48000
8/2/2013	12:03:32 PM	2.49400
8/2/2013	12:03:47 PM	2.47600
8/2/2013	12:04:03 PM	2.48000
8/2/2013	12:04:17 PM	2.49100
8/2/2013	12:04:32 PM	2.49400

TABLE 4.2

INTERPOLATED MEASUREMENT DATA WITH SAMPLING TIME-INTERVAL OF 30S.

Date	Time	Power (MW)
8/2/2013	12:00:00 PM	2.50803
8/2/2013	12:00:30 PM	2.50593
8/2/2013	12:01:00 PM	2.50313
8/2/2013	12:01:30 PM	2.50021
8/2/2013	12:02:00 PM	2.49287
8/2/2013	12:02:30 PM	2.48187
8/2/2013	12:03:00 PM	2.47781

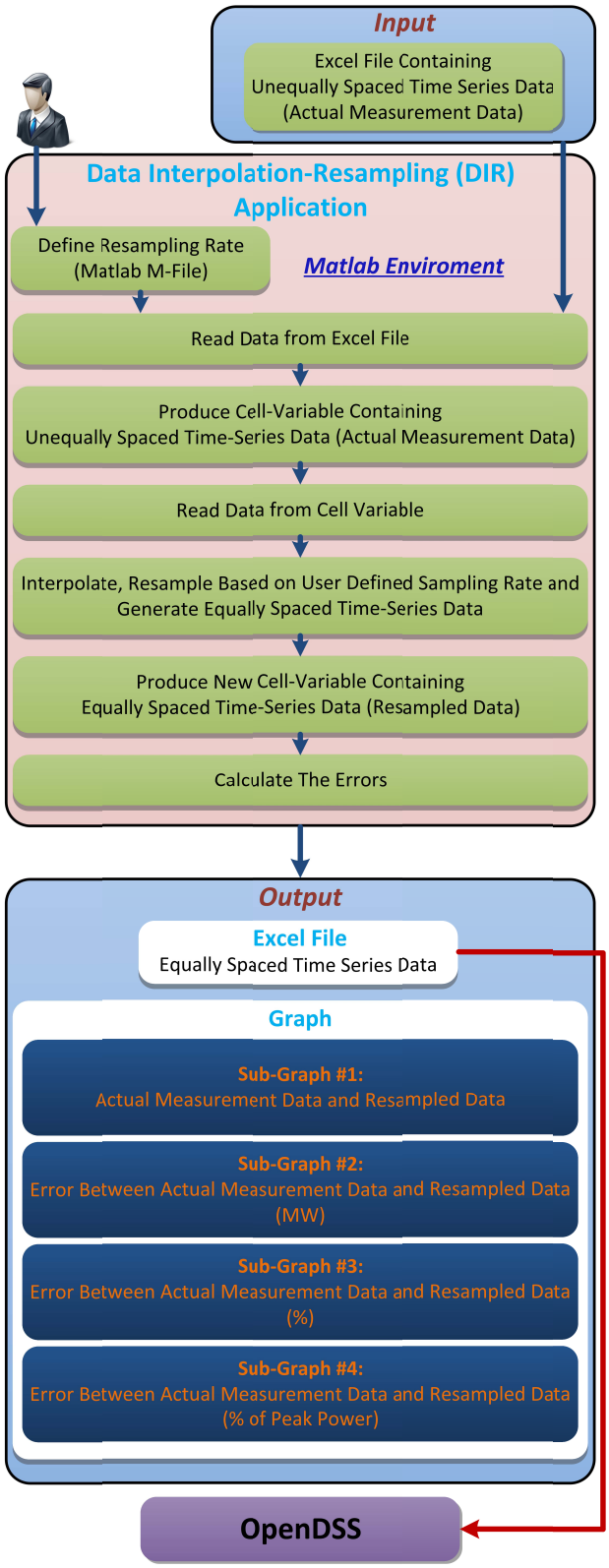

Figure 4.4. General scheme of the developed data interpolation-resampling (DIR) application.

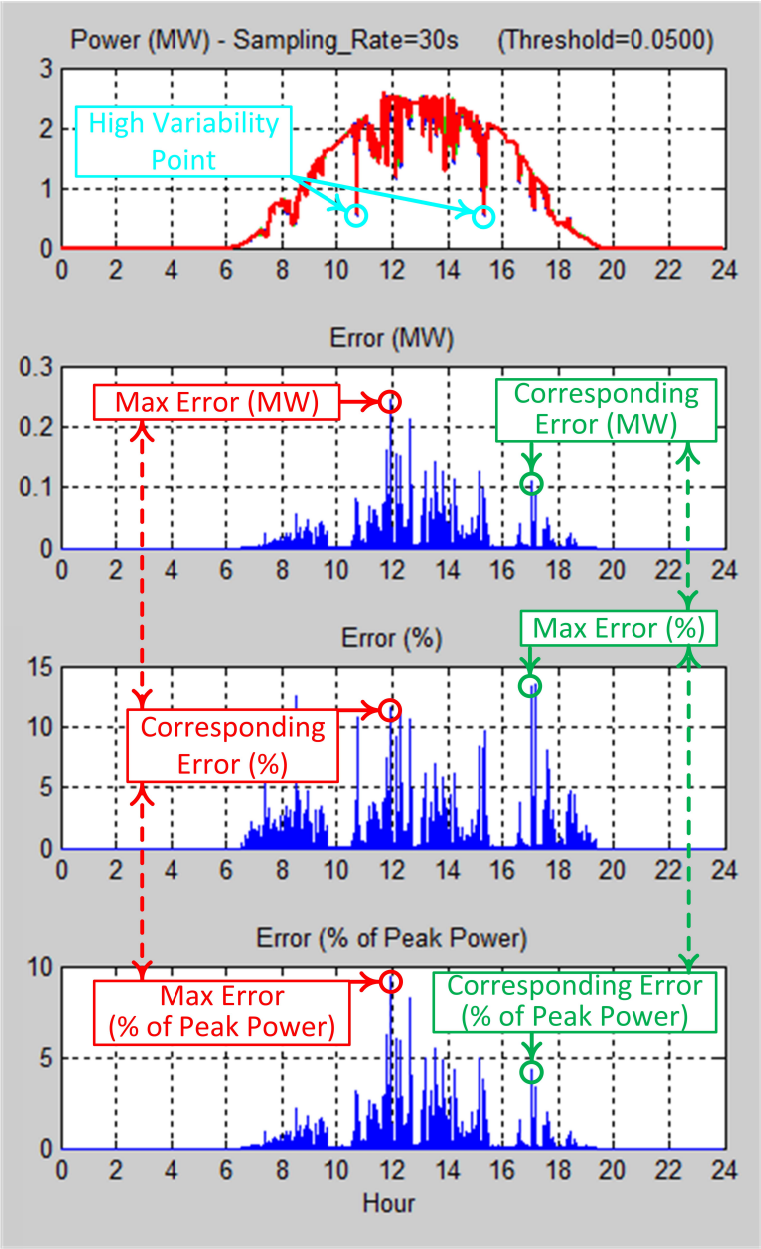

Figure 4.5. Output graph of DIR application depicting the interpolation-resampling error of measurement output power of 3.5MW solar plant on Aug. 2, 2013 resampled at 30s.

4.4.2. Development of Resampling Error Calculation (REC) Application

Although the developed DIR application provides detailed information about the amount of error caused by interpolation and resampling for a specific sampling time-

interval (for instance 30s in Figure 4.5), it is of a great interest that the resampling rate can be optimized for high accuracy and with minimum data storage. The proper selection of the resampling time-interval aims to keep the error between the actual and interpolated data in the acceptable range and the size of data as small as possible. Shorter sampling time-interval results in less error, larger size of data and slowing down the simulation while longer sampling time-interval results in more error, smaller size of data and speeding up the simulation. Therefore, another application called REC is developed in Matlab to read the unequally spaced time-series measurement data from an excel file, interpolate the data and resample with sampling time-interval in the range of T_{min} to T_{max} seconds with time increment of T_{incr} seconds (T_{min}, T_{max} and T_{incr} are user defined) and generates two different graphs (#1 and #2) to show error for each sampling time-interval. It is worth mentioning that due to intermittency of solar generation and greatest concern of high-variability point, it is valuable for user to realize the amount of error produced by interpolation and resampling process for each sampling time-interval and then, select the proper resampling time-interval.

The general scheme of the developed REC application is shown in Figure 4.6 where the application first reads the unequally spaced time-series measurement data from an excel file and stores them in cell variable named CV1 in MATLAB. At the next step, data stored in CV1 are interpolated and resampled with 1s sampling time-interval and new 1s-spaced time-series measurement data are stored in CV1_1s. The reason to generate 1s spaced time-series measurement data will be explained later. At the next step, data stored in CV1 are interpolated and resampled with new sampling time-interval (in the range of

T_{min} to T_{max}) and new generated equally spaced time-series data are stored in CV2. Afterwards, data stored in CV2 are interpolated and resampled with 1s sampling time-interval and new 1s-spaced time-series data are stored in CV2_1s. Subsequently, the data of CV2_1s are compared with data of CV1_1s second by second to calculate the error between the interpolated data and actual data and store the errors at CV_Error. At the next step, the errors stored in CV_Error are analyzed and the maximum and corresponding errors are obtained and stored in CV_Error_Max and CV_Error_Cor, respectively. Afterwards, the sampling time-interval increases with user defined value of T_{incr} and if the new sampling time-interval is within the sweep range (i.e., T_{min} to T_{max}) defined by user, the application will do the same explained loop as shown in Figure 4.6. Otherwise, the application will be ended and generate two graphs explained later.

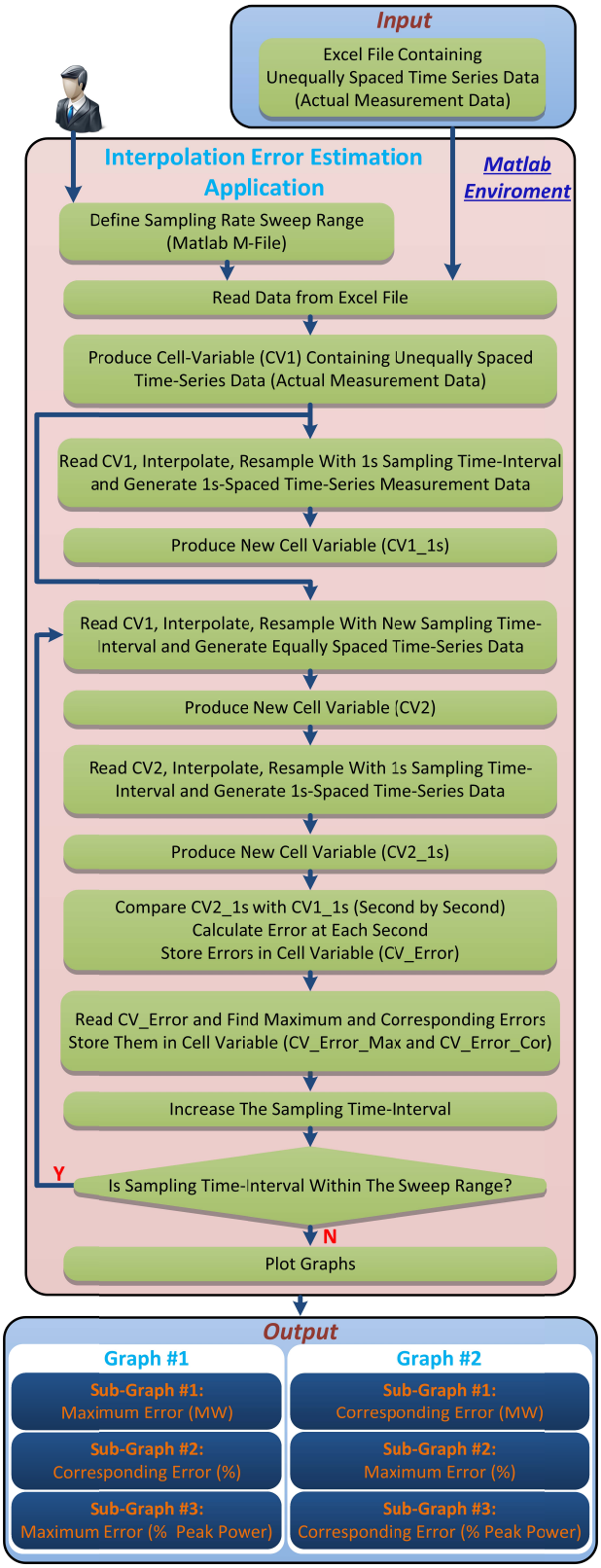

Figure 4.6. General scheme of the developed resampling error calculation (REC) application.

The reason to resample CV1 with 1s sampling time-interval and generate CV1_1s is that in order to compare the actual measurement data and interpolated one, the actual unequally spaced time-series measurement data should be converted to equally spaced time-series data precisely without any error. Otherwise, the comparison between the interpolated data and actual data is not precise. The only solution to have the exact pattern of unequally spaced time-series measurement data but in the format of equally spaced time-series data is to interpolate the actual measurement data with the sampling time-interval equals to greatest common factor of all variable time-intervals of CV1. By doing this, the CV1 containing unequally spaced time-series measurement data can be converted to equally spaced time-series measurement data with no error. However, due to nature of measurement date, the greatest common factor of all time-intervals in CV1 is 1s. Thus, 1s is selected as the sampling time-interval to convert CV1 to 1s-spaced time-series measurement data, called CV1_1s, with no error. In order to precisely compare the CV2 with CV1_1s, it is also required to convert CV2 containing equally spaced time-series data, which is the interpolated measurement data, to 1s-spaced time-series data. This approach is illustrated in Figure 4.7 where the CV2 is obtained by interpolating and resampling the CV1 with sampling time-interval of 5s. As it is seen in Figure 4.7, the maximum error happens at time 22s.

As shown in Figure 4.6, the developed REC application generates two different graphs and each graph has three sub-graphs (numbered 1 to 3). For instance, two generated graphs for the measurement output power of 2.5MW solar plant on Aug. 2, 2013 with sampling time-interval range from 1s to 100s with 1s increment are illustrated in

Figure 4.8. It is worth mentioning that although the moments associate to maximum "Error (MW)" and maximum "Error (% of Peak Power)" are the same, it is not necessarily the same moment associates to maximum "Error (%)". For instance in Figure 4.5, the moment associates to maximum "Error (MW)" and "Error (% of Peak Power)" is around 11:55 while the moment associates to maximum "Error (%)" is around 17:05. This is why the "corresponding" term is used in Figure 4.5 and Figure 4.8 meaning that the corresponding "Error (%)" is amount of "Error (%)" at the moment when the maximum "Error (MW)" happens. On the other hand, the corresponding "Error (MW)" is the amount of "Error (MW)" at the moment when the maximum "Error (%)" happens. This visualization tool is helpful to select the proper sampling time-interval to keep the error below the certain amount. According to Figure 4.8, the 30s resampling time-interval is suitable since the maximum "Error (MW)", maximum "Error (% of Peak Power)" and the corresponding "Error (%)" are 0.24MW, 9% and 12%, respectively. Moreover, maximum "Error (%)" and the corresponding "Error (MW)" and corresponding "Error (% of Peak Power)" are 13%, 0.1MW and 4% respectively. Therefore, the amount of error for 30s resampling time-interval is acceptable for the purpose of this chapter investigating the effect of solar energy penetration. It is worth mentioning that two high-variability points happen around 10:45 and 15:25 and their "Error (MW)", "Error (%)" and "Error (% of Peak Power)" are below 0.1MW, 10% and 5%, respectively. This also confirms that 30s resampling time-interval does not result in missing significant data of two mentioned high-variability points which are of greatest concern.

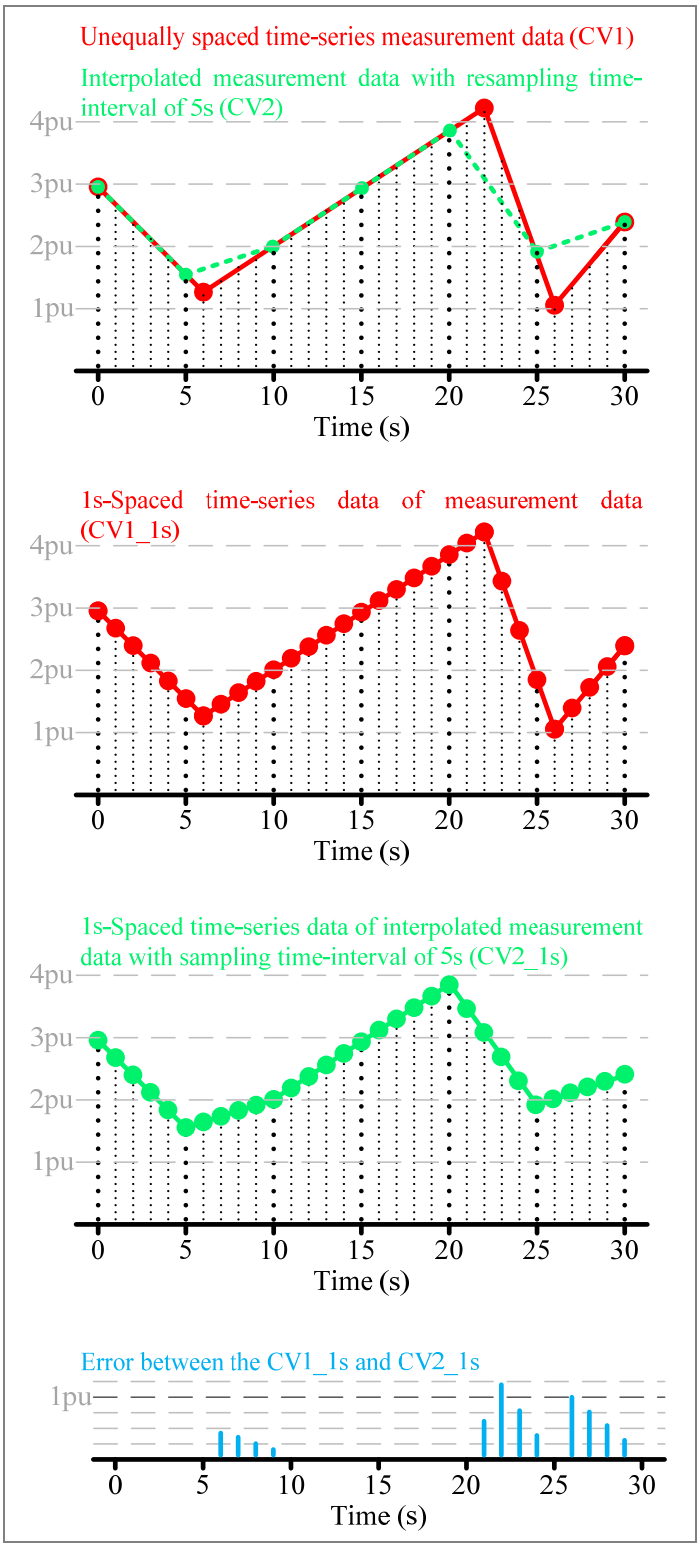

Figure 4.7. The approach of converting both unequally spaced time-series measurement data (CV1) and interpolated measurement data (CV2) to 1s-spaced time-series data (CV1_1s and CV2_1s), comparing them and calculating the error.

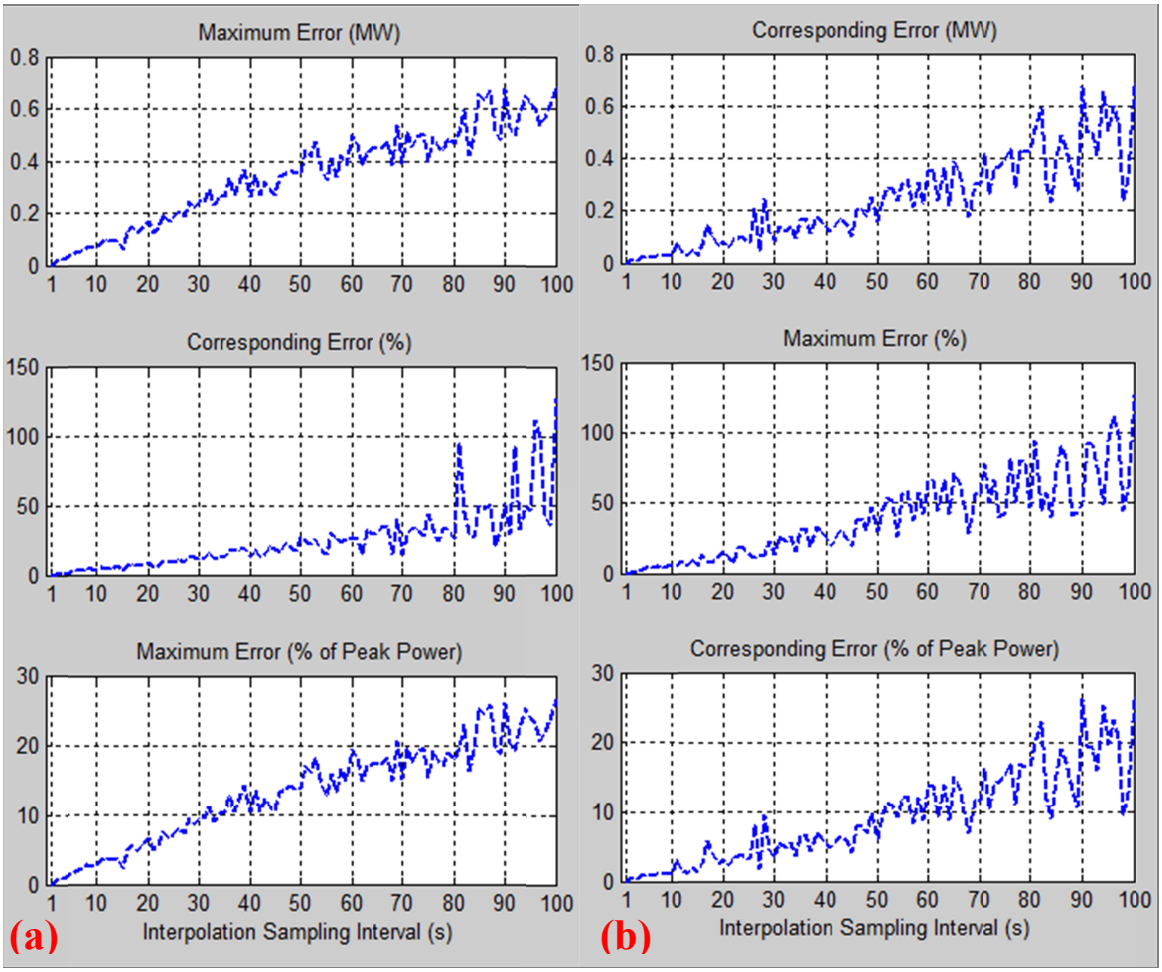

Figure 4.8. The interpolation error of measurement output power of 2.5MW solar plant resampled in the range of 1s to 100s illustrating (a) maximum Error (MW), corresponding Error (%) and maximum Error (% of Peak Power); (b) corresponding Error (MW), maximum Error (%) and corresponding Error (% of Peak Power).

4.5. Model Validation Considerations

Steady-state models of the power system (often called power flow cases) form the foundation of technical studies of the system. Because of this importance, these cases need to be periodically compared (benchmarked) to measured quantities and operational practices of the power system. Such a comparison validates that the power flow case closely resembles actual operating conditions. The comparison also identifies data errors

and parameters that cause mismatch. These can then be corrected or adjusted so that cases more closely match the actual conditions. Herein, three considerations for model validation of line/cable impedance, load and solar generation are provided.

4.5.1. Line/Cable Modeling

Line/cable impedances after being calculated using a model or obtained from measurement are used in power flow and short circuit studies. Calculating these impedances can be complex and their accuracy is often unknown.. An approach is provided here which can be helpful to validate the line/cable model. Figure 4.9 shows the general scheme of the unbalanced distribution line/cable considering the self resistance (R_{xx}), self-inductance (L_{xx}), mutual impedance (Z_{xy}), self admittance (Y_{xx}) and mutual admittance (Y_{xy}). It is worth mentioning that PI model is considered so half of the self and mutual admittance which are only susceptance due to self and mutual capacitance are placed at the beginning of the line/cable and another half at the end of the line/cable.

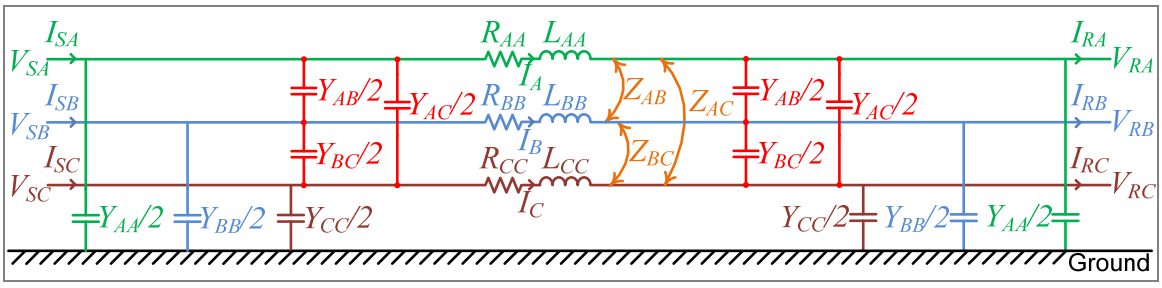

Figure 4.9. General scheme of the unbalanced distribution line/cable.

The first step of model validation for a given line/cable segment is to obtain the self and mutual admittance for that particular line/cable segment as follows:

$$\begin{bmatrix} I_{SA} \\ I_{SB} \\ I_{SC} \end{bmatrix} - \begin{bmatrix} I_{RA} \\ I_{RB} \\ I_{RC} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} Y_{AA}+Y_{AB}+Y_{AC} & -Y_{AB} & -Y_{AC} \\ -Y_{AB} & Y_{BB}+Y_{AB}+Y_{BC} & -Y_{BC} \\ -Y_{AC} & -Y_{BC} & Y_{CC}+Y_{AC}+Y_{BC} \end{bmatrix} \cdot \begin{bmatrix} V_{SA} \\ V_{SB} \\ V_{SC} \end{bmatrix}$$

$$+\frac{1}{2}\begin{bmatrix} Y_{AA}+Y_{AB}+Y_{AC} & -Y_{AB} & -Y_{AC} \\ -Y_{AB} & Y_{BB}+Y_{AB}+Y_{BC} & -Y_{BC} \\ -Y_{AC} & -Y_{BC} & Y_{CC}+Y_{AC}+Y_{BC} \end{bmatrix} \cdot \begin{bmatrix} V_{RA} \\ V_{RB} \\ V_{RC} \end{bmatrix} \quad \text{Eq. 4.1}$$

$$\begin{bmatrix} I_{SA} \\ I_{SB} \\ I_{SC} \end{bmatrix} - \begin{bmatrix} I_{RA} \\ I_{RB} \\ I_{RC} \end{bmatrix} = \begin{bmatrix} Y_{AA}+Y_{AB}+Y_{AC} & -Y_{AB} & -Y_{AC} \\ -Y_{AB} & Y_{BB}+Y_{AB}+Y_{BC} & -Y_{BC} \\ -Y_{AC} & -Y_{BC} & Y_{CC}+Y_{AC}+Y_{BC} \end{bmatrix} \cdot \begin{bmatrix} V_{SA}+V_{RA} \\ V_{SB}+V_{RB} \\ V_{SC}+V_{RC} \end{bmatrix} \quad \text{Eq. 4.2}$$

$$Y_{xx} = jB_{xx} \quad , \quad x = A, B, C \quad \text{Eq. 4.3}$$

$$Y_{xy} = jB_{xy} \quad , \quad x, y = A, B, C \quad \text{Eq. 4.4}$$

where, B_{xx} as the self susceptance of the phase x equals $C_{xx}\omega$ and B_{xy} as the mutual susceptance between phase x and y equals $C_{xy}\omega$. After obtaining the matrix of self and mutual admittance, the current flowing through the series impedance of each phase can be calculated as follows:

$$\begin{bmatrix} I_{A} \\ I_{B} \\ I_{C} \end{bmatrix} = \begin{bmatrix} I_{RA} \\ I_{RB} \\ I_{RC} \end{bmatrix} + \frac{1}{2}\begin{bmatrix} Y_{AA}+Y_{AB}+Y_{AC} & -Y_{AB} & -Y_{AC} \\ -Y_{AB} & Y_{BB}+Y_{AB}+Y_{BC} & -Y_{BC} \\ -Y_{AC} & -Y_{BC} & Y_{CC}+Y_{AC}+Y_{BC} \end{bmatrix} \cdot \begin{bmatrix} V_{RA} \\ V_{RB} \\ V_{RC} \end{bmatrix} \quad \text{Eq. 4.5}$$

Afterwards, the voltage drop for the same line/cable segment is expressed as follows:

$$\begin{bmatrix} V_{SA} \\ V_{SB} \\ V_{SC} \end{bmatrix} - \begin{bmatrix} V_{RA} \\ V_{RB} \\ V_{RC} \end{bmatrix} = \begin{bmatrix} R_{AA} + jL_{AA}\omega & R_{AB} + jL_{AB}\omega & R_{AC} + jL_{AC}\omega \\ R_{AB} + jL_{AB}\omega & R_{BB} + jL_{BB}\omega & R_{BC} + jL_{BC}\omega \\ R_{AC} + jL_{AC}\omega & R_{BC} + jL_{BC}\omega & R_{CC} + jL_{CC}\omega \end{bmatrix} \cdot \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \quad \text{Eq. 4.6}$$

It is worth mentioning that Eq. 4.2 has six variables of $Y_{AA}, Y_{BB}, Y_{CC}, Y_{AB}, Y_{AC}, Y_{BC}$ which need to be calculated. However, it seems to be impossible at the first glance since Eq. 4.2 has three algebraic expressions after substituting voltages and currents values which are obtained through measurement. However, each algebraic expression is a complex expression which has one real and one imaginary expression. Therefore, Eq. 4.2 has overall six algebraic expressions which can be used to obtain six mentioned variables. On the other hand, Eq. 4.6 has twelve variables of $R_{AA}, R_{BB}, R_{CC}, R_{AB}, R_{AC}, R_{BC}$ and $L_{AA}, L_{BB}, L_{CC}, L_{AB}, L_{AC}, L_{BC}$ which need to be calculated. The same approach explained for Eq. 4.2 needs to be considered for Eq. 4.6 which means that one set of voltages and currents values can be used to calculate six variables. The difference between solving Eq. 4.2 and Eq. 4.6 is that voltages and currents values at two different moments are required to solve Eq. 4.6 while voltages and currents values only at one moment are required to solve the Eq. 4.2. Since voltages and currents values are the measurement values as said previously, there is not a technical problem to store voltages and currents values at two different moments and use them to solve the required equations.

Although it seems to be difficult and laborious at the first glance to measure the voltage and current at both beginning and ending nodes of each line/cable to validate its impedance parameters, it is not required to do this approach to all of the lines/cables one by one. First of all, they are limited types of lines/cables used in the real circuits. For

instance, the SCE circuit considered in this chapter has around 36 lines and 90 cables whereas there are only 11 types of lines and 11 types of cables. Moreover, it is most likely that the same types of lines/cables are used in other distribution circuits of the same company, herein SCE, since in practice there are limited types of overhead line towers and underground cables. Therefore, the presented approach to validate the line/cable models is practically possible and beneficial. Considering the fact that some types of lines/cables are utilized in the circuit more than the others regarding the overall length; for instance, Figure 4.10 illustrates overall length of each type of line/cable used in the SCE circuit as well as the number of lines/cables of each type. Thus, this fact can be used to prioritize which types of line/cable should be validated since the type of line/cable which has more overall length has more effect on the circuit voltage profile. For example in Figure 4.10, 86% (regarding overall length of lines/cables in the studied circuit) of whole circuit's lines and cables impedances can be validated by conducting the presented approach for the cable types of G to K and line types of I' to K', totally 9 lines and cables. Moreover, the cumulative distribution of the line/cable types in the SCE studied circuit is shown in Figure 4.11. As it can be seen, three types (I' to K') of line constitute 18% of overall lines and cables length while the other 8 types constitute only 3% (=21-18) of overall lines and cables length in the studied circuit. Furthermore, five types (G to K) of cable constitute 68% of overall lines and cables length while the other 6 types constitute only 11% (=79-68) of overall lines and cables length in the studied circuit.

In light of above discussion, model validation for lines and cables can be carried out for a percentage of the circuit depending on the budget. The approach will be to install

meter at both beginning and ending points of each selected types of lines and cables to measure their voltage and current in order to identify their impedances.

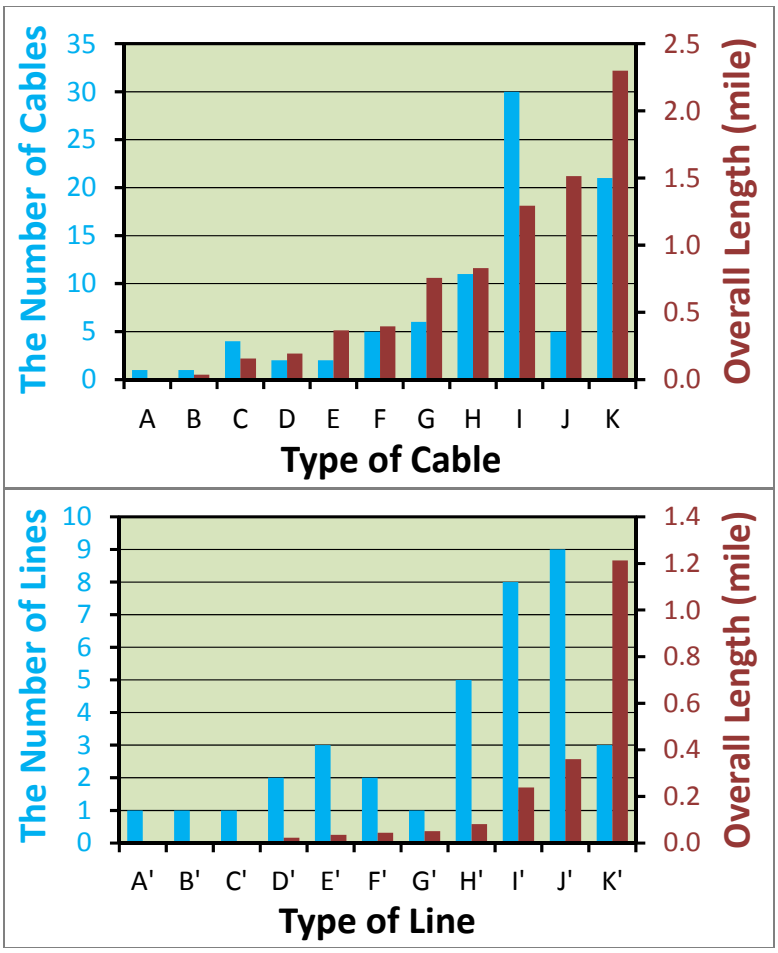

Figure 4.10. The number of lines and cables of each type and overall length of each type of line/cable used in the SCE studied circuit.

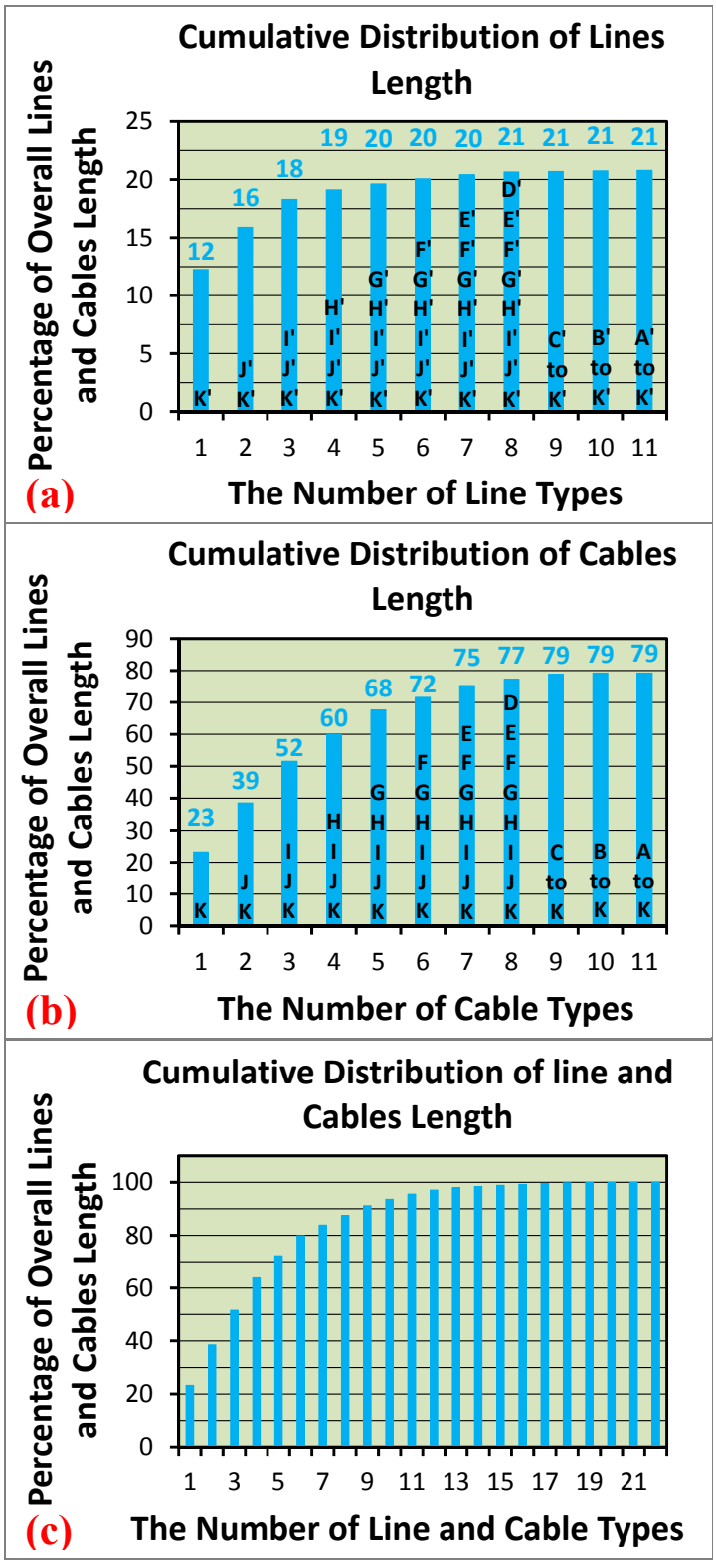

Figure 4.11. Cumulative distribution of line/cable types in the SCE studied circuit: (a) line; (b) cable; (c) both line and cable.

4.5.2. Load Modeling

The general assumption in the power system modeling is that the majority of the loads in the power system are predominantly constant power. But this is not the case in reality. As presented in literature [25]–[31], laboratory experiments on different appliances and pieces of equipment have been conducted and the results show that no load is entirely constant-power, constant-impedance, nor a constant-current.. Each appliance or piece of equipment in the system has its own P-V and Q-V characteristics, which can be represented by its ZIP coefficients. The polynomial expression known as the ZIP coefficients model represents the variation (with voltage) of a load as a composition of three types of constant loads: constant impedance (Z), constant current (I), and constant power (P). The ZIP coefficients can be obtained by applying a least-square fitting on the test data obtained from laboratory experiments or the field measurement [29]–[31].

The P-V and Q-V curves for a particular service class depend on the load composition of customers in such class, for example, type of loads, rating of loads, duty cycle, and use factor [27], [29], [30]. With all of this information, one can generate the ZIP coefficients of each load and consequently, an equivalent ZIP model for each class depending on the percentage contribution of each load to the total load of the class. Taking into account the percent load of users of each class in specific networks, a network-equivalent ZIP model can be obtained. In general, the ZIP coefficients model can be written with the following quadratic expressions:

$$P = P_0\left[Z_p\left(\frac{V}{V_0}\right)^2 + I_p\frac{V}{V_0} + P_p \right] \quad \text{Eq. 4.7}$$

$$Q = Q_0\left[Z_q\left(\frac{V}{V_0}\right)^2 + I_q\frac{V}{V_0} + P_q \right] \quad \text{Eq. 4.8}$$

As an example, the ZIP coefficients of different customer classes presented in [30] are listed in Table II. The SCE circuit with all loads considered as PQ loads is utilized in this conducted study.

TABLE 4.3

ACTIVE AND REACTIVE ZIP COEFICIENTS FOR EACH CUSTOMER CLASS [30].

Customer Class		Z_p	I_p	P_p	Z_q	I_q	P_q
Residential	**Stratum A**	1.5	-2.31	1.81	7.41	-11.97	5.55
	Stratum B	1.57	-2.48	1.91	9.28	-15.29	7.01
	Stratum C	1.56	-2.49	1.93	10.1	-16.75	7.65
	Stratum D	1.31	-1.94	1.63	9.2	-15.27	7.07
	Stratum E	0.96	-1.17	1.21	6.28	-10.16	4.88
	Stratum F	1.18	-1.64	1.47	8.29	-13.67	6.38
Small Commercial	**Duane Reade**	0.27	-0.66	1.06	5.48	-9.7	5.22
	5Guys Burger	0.69	0.04	0.27	1.82	-2.24	1.43
	Laundromat	0.77	-0.84	1.07	8.09	-13.65	6.56
	Optics	0.55	0.24	0.21	0.55	-0.09	0.54
Large Commercial	**School**	0.4	-0.41	1.01	4.43	-7.98	4.56
	Hotel	0.76	-0.52	0.76	6.92	-11.75	5.83
Industrial		1.21	-1.61	1.41	4.35	-7.08	3.72

Another helpful fact in model validation is the times-series power profile of the loads. In this conducted study, power profiles of individual loads are not available to be attached to each load in time-series simulation studies. The only available measurements are start-of-circuit power measurement as well as the output power measurement of 1.5MW and 3.5MW solar plants. By adding the solar plants output power to start-of-circuit power measurement, the loads' native time-series power profile can be obtained which is used as scaling factor for all loads. Therefore, all loads are assumed to operate with the same time-series power profile. However, this is not true in practice since the loads may have different time-series power profiles and dynamics. In order to have more precise modeling of the circuit, it is needed to consider the loads with their individual times-series power profiles in the studies. This requires measuring the time-series power profile of the loads one by one at the first glance which is not a simple task. However, all of the loads generally do not have the same power rating and consequently, they do not have the same effect on the circuit voltage profile. Therefore, as with the lines and cables, the way to validate the loads is to first sort the loads regarding their power rating and then, prioritize the loads whose time-series power profile should be measured. For instance, Figure 4.12 illustrates the cumulative distribution of loads power rating in the SCE studied circuit where 13 out of 39 loads constitute 79% of overall load regarding the power rating. This means that measuring only 13 loads (one third of all loads) time-series power profile results in having the exact times–series power profile of almost 80% of whole circuit loads. Therefore, cumulative distribution of loads power rating is a good indicator which can be utilized in selecting the loads whose time-series power profile should be measured.

In light of above discussion, model validation for loads can be carried out for a percentage of the circuit's loads depending on the budget. The approach will be to have one meter for each selected load to measure voltage and current in order to identify the associated time-series power profile as well as the ZIP coefficient of load model.

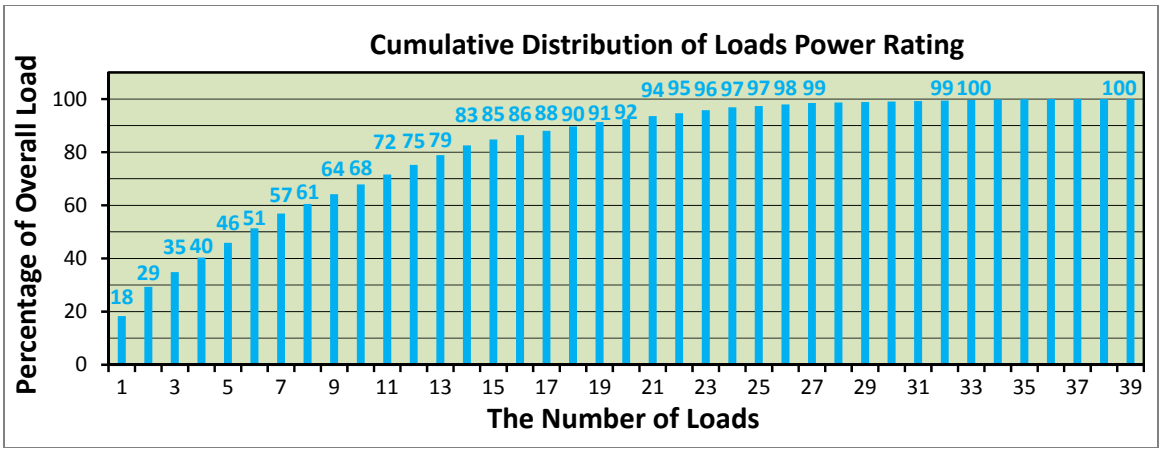

Figure 4.12. Cumulative distribution of loads power rating in the SCE studied circuit.

4.5.3. Solar Generation Modeling

Intermittency, or discontinuity of output power, is one of the inherent traits of solar energy that imposes barrier to distributed energy resources (DER) penetration in a utility system. Solar energy generation is based on solar irradiance, which is the amount of incident electromagnetic power received per unit area of a given surface, usually in units of W/m^2. Insolation is the total amount of solar irradiance received on a given surface area during a given time expressed in units such as Wh/m^2 [32]. Generally, PV panels are rated in peak watts which is the power generated at a reference insolation level of $1000 W/m^2$. A 1 kW panel will produce that much power if perpendicular to the sun's rays at peak insolation periods. Insolation levels need to be gathered at the location where the PV will

be installed to best approximate insolation profiles. They can be obtained from a variety of resources such as TMY2 (Typical Meteorological Year), NREL PVWatts, and NSRDB (National Solar Radiation Database). Insolation levels at the panels vary based on their angle and tracking method if used. This needs to be known when analyzing the data since the PV panels may have been oriented differently. A review of the specifications, spacing, and orientation of the PV arrays is needed to most accurately model the nature of its power output characteristics and intermittencies. In order to obtain the most accurate model of distributed solar energy penetration, it is needed to measure the time-series output power of each solar inverter [33]. Although this kind of approach is feasible for large-scale solar plants, it is a challenging problem, due to budget burden of utilities, for distributed generation at millions of homes throughout the grid. With lack of time-series output power of each solar energy generation in distributed configuration, an alternative is to use nearby time-series solar irradiance profile and assume all distributed solar energy generation operates with the same time-series solar irradiance profile. This can be also done by installing the solar irradiance sensors in couple of places throughout the circuit instead of one location. However, the SCE studied circuit in this chapter does not have distributed solar energy generation and as mentioned before, it has two 1.5MW and 3.5MW solar plants whose time-series output power profiles are available individually.

4.6. SCE Circuit Model Validation

A power distribution circuit from SCE is considered in this chapter as an example to investigate the impact of large-scale solar energy penetration. The circuit contains 39

loads with total rating of 7MW and 4.8MVAR, four 1800kVAR capacitor banks, 291 nodes, 90 cables, 36 overhead lines, and 10 step-up transformers (0.21/12 kV) to connect the solar plants inverters to power grid. The distance from start-of-circuit to end-of-circuit is about 28000 ft. A single-line diagram of the circuit is shown in Figure 4.13. In the mentioned circuit, two solar plants with rating of 3.5MW and 1.5MW are available which represents a substantial solar energy penetration. Table III illustrates the location of four capacitor banks and two solar plants in the SCE circuit. Both three-phase and single-phase loads are represented by spot loads distributed throughout the circuit. Each spot load size was based on its kW and PF values from the original CYME model. This is considered as base load at every load point in the circuit, which would be scaled at each time step of time-series simulation to match the measurement. Figure 4.14 illustrates the start-of-circuit raw measured current of all three phases at the period of 11 days from July 25, 2013 to August 4, 2013. This shows that the circuit has the well-balanced loading in all three phases.

TABLE 4.4

LOCATION OF CAPACITOR BANKS, SOLAR PLANTS AND REGULATOR IN THE SCE CIRCUIT

Component	Distance from start-of-circuit (ft)
capacitor bank #1	10201
capacitor bank #2	11283
capacitor bank #3	23465
capacitor bank #4	24776
1.5MW solar plant	12392
3.5MW solar plant	12066
Regulator	15092

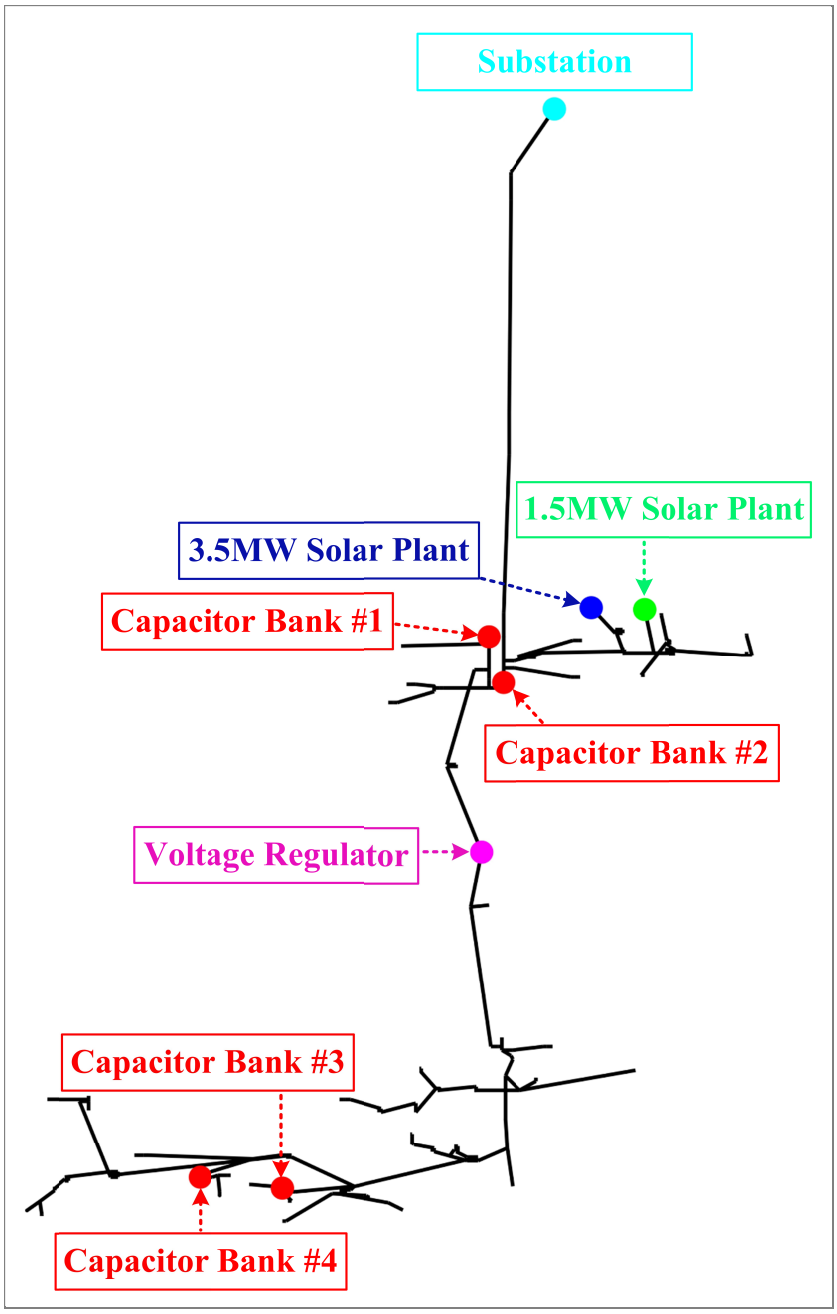

Figure 4.13. Single-line diagram of the studied SCE power distribution circuit.

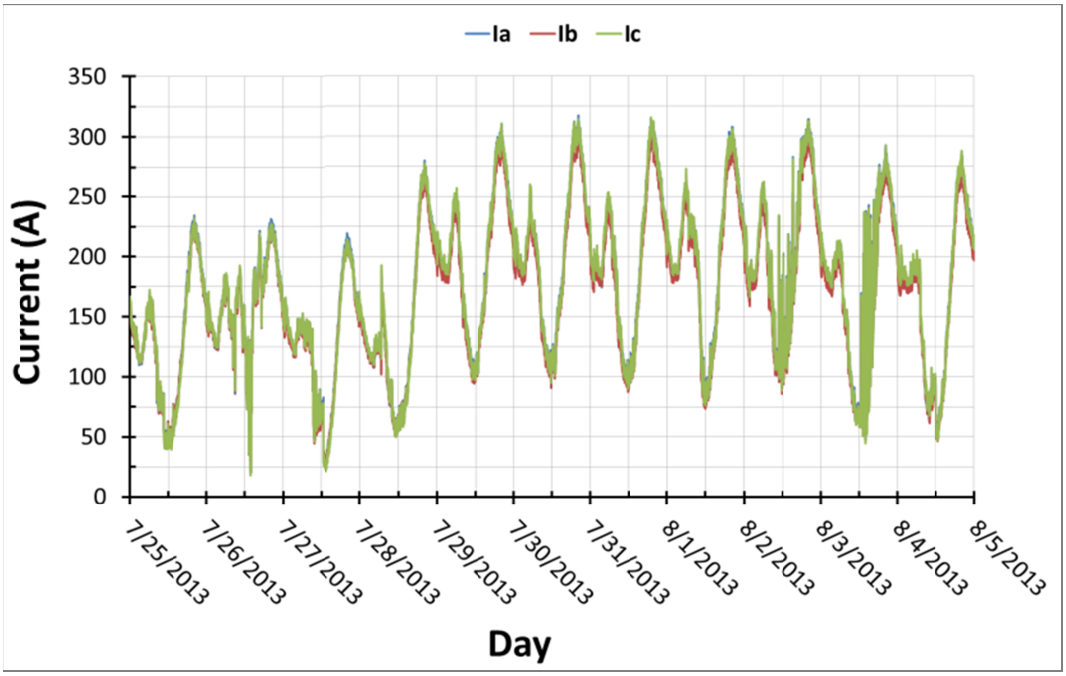

Figure 4.14. The start-of-circuit raw measured current of all three phases.

As mentioned before, studied SCE circuit has 11 types of lines and 11 types of cables (overall 22 types of lines/cables), and 39 individual loads. In order to completely (100%) validate the studied SCE circuit, it is required to install 48 pairs (voltage and current) of meters at each beginning and ending points of all 22 types of lines/cables. Moreover, 39 pairs (voltage and power) of meters are required to be installed to validate all loads. However, this amount of meters could be beyond the budget and is needed to be optimized. The relationship between the number of required meters for loads and lines/cables and the percentage of validation in the studied SCE circuit is illustrated in Table 4.5 and Table 4.6.

TABLE 4.5

THE NUMBER OF REQUIRED LINE/CABLE METERS TO VALIDATE THE SPECIFIC PERCENTAGE OF WHOLE CIRCUIT IMPEDANCES

Percentage of whole circuit's line/cable impedance validation	The number of required line/cable meters in pair (voltage and current)
100	22
95	11
91	9
84	7
80	6
72	5
63	4
51	3
38	2

TABLE 4.6

THE NUMBER OF LOAD METERS TO VALIDATE THE SPECIFIC PERCENTAGE OF WHOLE CIRCUIT LOAD

Percentage of whole circuit's load validation	The number of required meters in pair (voltage and current)
100	39
95	22
90	18
79	13
68	10
61	8
51	6
40	4
29	2

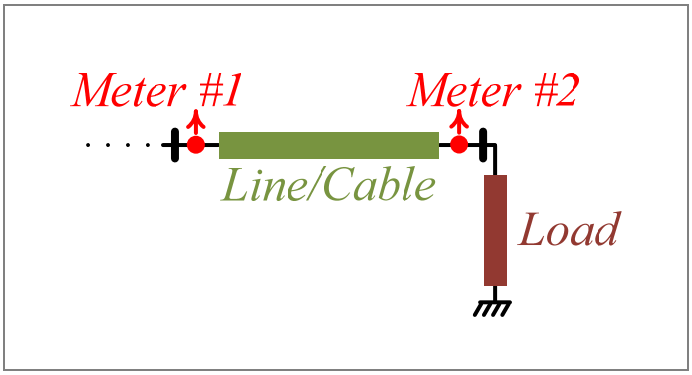

Figure 4.15. Model validation for the combination of the load and cable/line.

TABLE 4.7

THE TYPES OF CABLES FEEDING THE LOADS #1 TO #10 SORTED IN DESCENDING ORDER OF POWER

Load number presented in Figure 4.12	Type of Cable
Load 1	G
Load 2	I
Load 3	K
Load 4	H
Load 5	I
Load 6	I
Load 7	I
Load 8	G
Load 9	H
Load 10	I

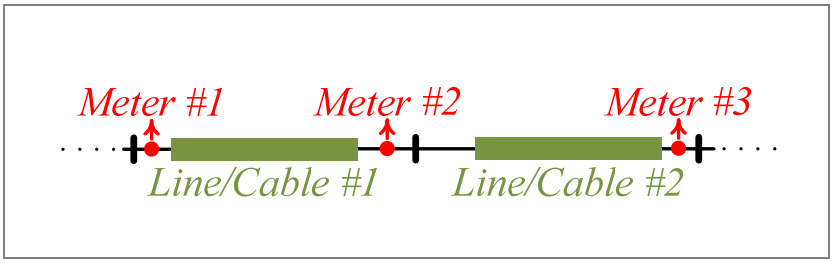

Figure 4.16. Model validation for the case where two lines/cables are connected in series.

TABLE 4.8

LOCATION OF METERS TO VALIDATE 69% OF WHOLE CIRCUIT LINE/CABLE IMPEDANCES AND 40% OF WHOLE CIRCUIT LOADS

Node	Location of Node	Line/Cable Type
PME4895-3_02658_1	starting point of cable #83	G
36992863_02658	ending point of cable #83	
PME5193-1_02658_1	starting point of cable #42	I
48202287_02658	ending point of cable #42	
ND48204276_02658	starting point of cable #30	K
P5427192-1_02658	ending point of cable #30	
ND108471303_02658	starting point of cable #44	H
P5451042-1_02658	ending point of cable #44	
ND151952667_02658	starting point of line #21	K’

For the given SCE circuit, three meters are available, one at the substation and one at each of 1.5MW and 3.5MW solar plants. The output power measurements of 1.5MW and 3.5MW solar plants are combined with the start-of-circuit measurements with the time-coincident to determine the native load profile of the feeder. All the time-series simulations in this study are performed using these filed measurement data to provide scaling factors for the feeder's load allocation and solar generation. As mentioned before, the raw measurment data were uneqaully sapced times-series data; thus, measurement data are interpolated and resampled with sampling time-interval of 30s and are stored in CSV file for importing into OpenDSS to attach to the circuit model.

As the first step of time-series simulation, the measured power generation of both 1.5MW and 3.5MW solar plants along with the native feeder load active power profile of August 2, 2013 are attached to the SCE circuit remodeled in OpenDSS. Figure 4.17 depicts the start-of-circuit (substation) active power obtained from OpenDSS as well as the measurement data. As it can be seen, the obtained result has a great match with the measurement data validating the SCE circuit model for time-series simulation. Hereinafter, all simulation results are obtained for August 2, 2013 and the operation delay time for capacitor bank and regulator is set to 60s.

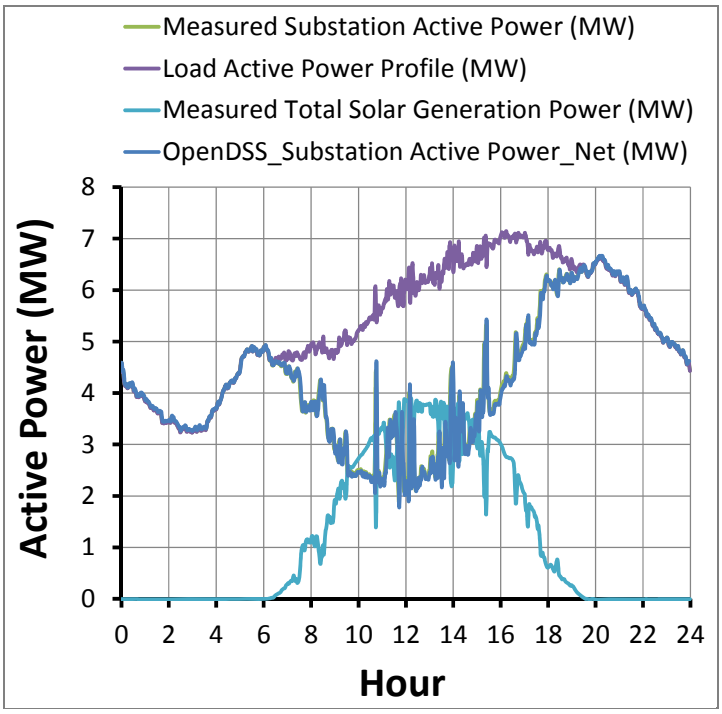

Figure 4.17. The measurement data and obtained simulation result at start-of-circuit.

4.7. Investigation of Solar Penetration Impacts and Simulation Results

As previously mentioned, a power distribution circuit from SCE is considered in this conducted study. Figure 4.18 shows the impact of reactive power on the voltage profile of end-of-circuit. Since the simulated circuit is almost balanced in all phases, the voltage profile of phase A at end-of-circuit is only shown in Figure 4.18 at the following consecutive cases:

- Capacitor bank #3 is disconnected.
- Capacitor bank #3 is connected.
- Capacitor bank #3 is controlled at voltage mode while its turn-off threshold is 1.02pu and its turn-on threshold is 0.99pu.

- Capacitor bank #3 is controlled at voltage mode while its turn-off threshold is 1.02pu and its turn-on threshold is 1pu.

As it is shown, the reactive power injection, especially at controlled mode, can improve the voltage profile. However, the voltage mode control setting is very important issue since it affects the number of operation of capacitor bank. For instance, if the turn-on threshold is set to 0.99pu and 1pu, capacitor bank is switched 4 and 26 times, respectively, while the difference in the number of operation is considerable. This can significantly reduce the life time of switches at capacitor bank. It is obvious that the mentioned frequent operation of capacitor bank is due to the intermittency of penetrated solar energy into power grid and this confirms the necessity to investigate the impact of large-scale solar energy penetration. Figure 4.19 depicts the operation of capacitor bank #3 controlled at voltage mode with turn-on threshold of 0.99pu and 1pu. It should be mentioned that the capacitor operation delay time (from when the control is armed before it sends out the switching command to turn on) and dead time (wait time after capacitor is turned off before it can be turned back on) are set to 60s and 300s, respectively. The power factor at start-of-circuit is shown in Figure 4.20 where the positive and negative values mean the leading and lagging of current phasor regarding the voltage phasor, respectively. It can be concluded that if the capacitor bank is controlled at voltage mode rather than consistently connected, the power factor at start-of-circuit is closer to unity power factor.

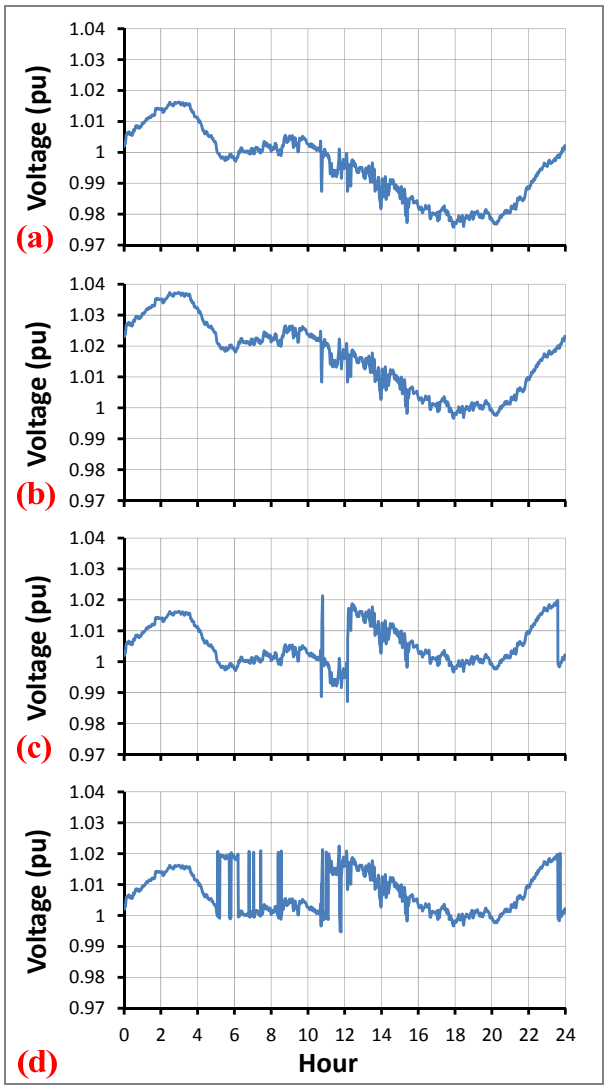

Figure 4.18. Simulation result – voltage of phase A at the end-of-circuit while capacitor #3 is (a) disconnected; (b) connected; (c) controlled with turn-on threshold of 0.99pu; (d) controlled with turn-on threshold of 1pu.

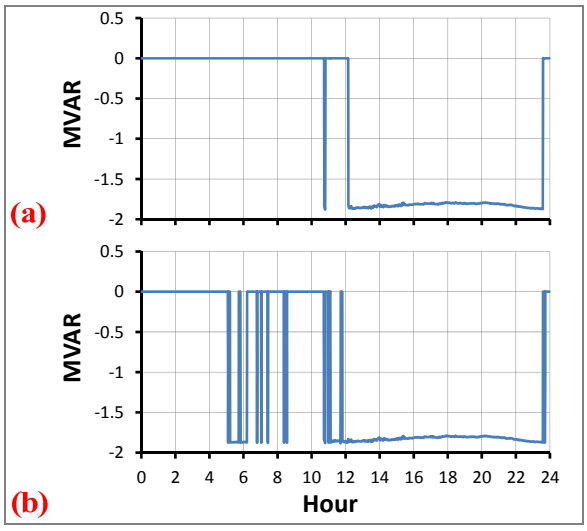

Figure 4.19. Simulation result – capacitor #3 operation at voltage mode control while its turn-on threshold is (a) 0.99pu; (b) 1pu.

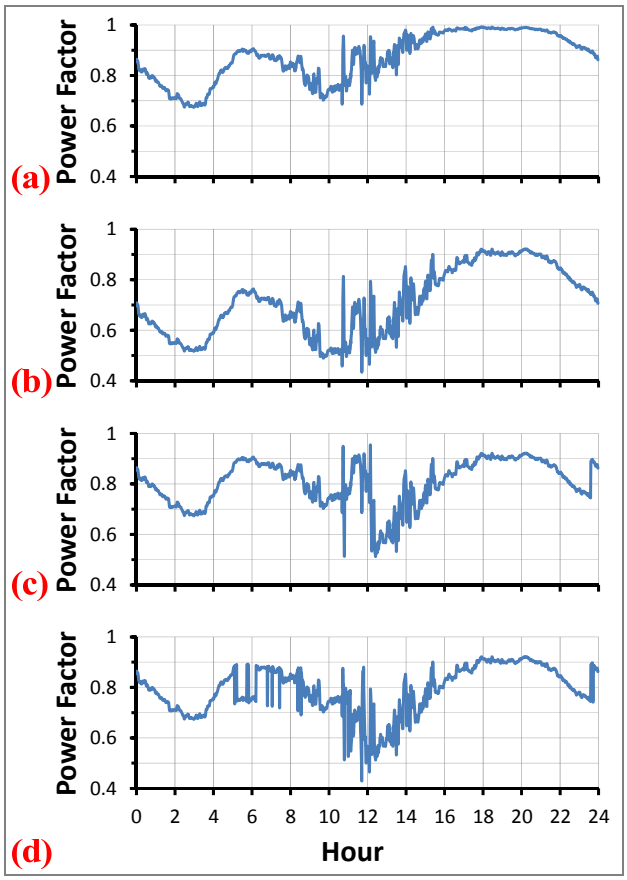

Figure 4.20. Simulation result – power factor of phase A at the end-of-circuit while capacitor #3 is (a) disconnected; (b) connected; (c) controlled with turn-on threshold of 0.99pu; (d) controlled with turn-on threshold of 1pu.

As another case study, the voltage regulator is considered at distance of 15092ft from start-of-circuit, as shown in Figure 4.13. It should be mentioned that in the SCE circuit, there is not any voltage regulator. Herein, the voltage regulator is considered by authors to investigate the possible impact of large-scale solar energy penetration on operation of voltage regulator. The considered voltage regulator has the tap changer varying from 0.9pu to 1.1pu with step change of 0.00625pu and operation delay time of 60s. Figure 4.21(a) shows the voltage profile at the end-of-circuit while both capacitor banks #3 and #4 are turned off to have almost unity power factor at start-of-circuit shown in Figure 4.21(b) while the voltage regulator is not activated yet. Figure 4.22 shows the voltage at primary side of voltage regulator. As it can be seen in Figure 4.22(b) where the voltage regulator is activated, the voltage regulator can adjust the voltage at the defined value of 1.02pu. Consequently, the voltage at furthest point of circuit, i.e., end-of-circuit, is regulated around 1.01pu, as shown in Figure 4.22(d). Figure 4.22(c) depicts the voltage regulator tap position and it can be pointed out that from 10:00 to 19:00 which is almost the period of solar energy penetration, there are couple of unnecessary changes (circled with red color dashed line) occurred due to the intermittency of solar energy. This confirms the impact of solar energy penetration on the number of operation of voltage regulator. In general, the fast transient of clouds (in the range of couple of seconds) causes high-variability of solar generation. This results in frequent voltage fluctuation and consequently, increases the number of operation of voltage regulator and capacitor banks in order to regulate the voltage. This fact affects the life-time of equipment due to frequent operation.

It should be mentioned that under large-scale penetration of solar energy especially at the high-variability points of solar generation, the control actions of the voltage regulator or capacitor bank may fail to mitigate the associated voltage fluctuations. Following can be considered as the remedial actions to improve the system operation:

- Changing the settings of capacitor bank and voltage regulator. Widen the band width of hysteresis comparison decreases the number of operation and vice versa.
- Changing the conductor of distribution lines to decrease their impedance. Although this can be costly at the first glance, this can be considered for the important lines/cables either carrying more power in the circuit or have more voltage drop effect in the circuit.

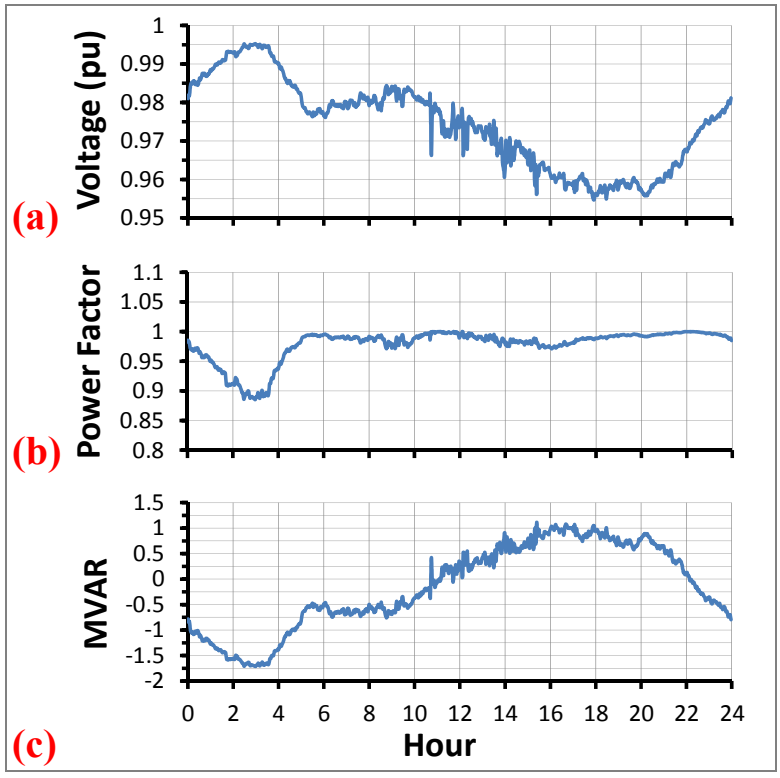

Figure 4.21. Simulation result – (a) voltage profile at end-of-circuit; (b) power factor at start-of-circuit; (c) amount of reactive power at start-of-circuit.

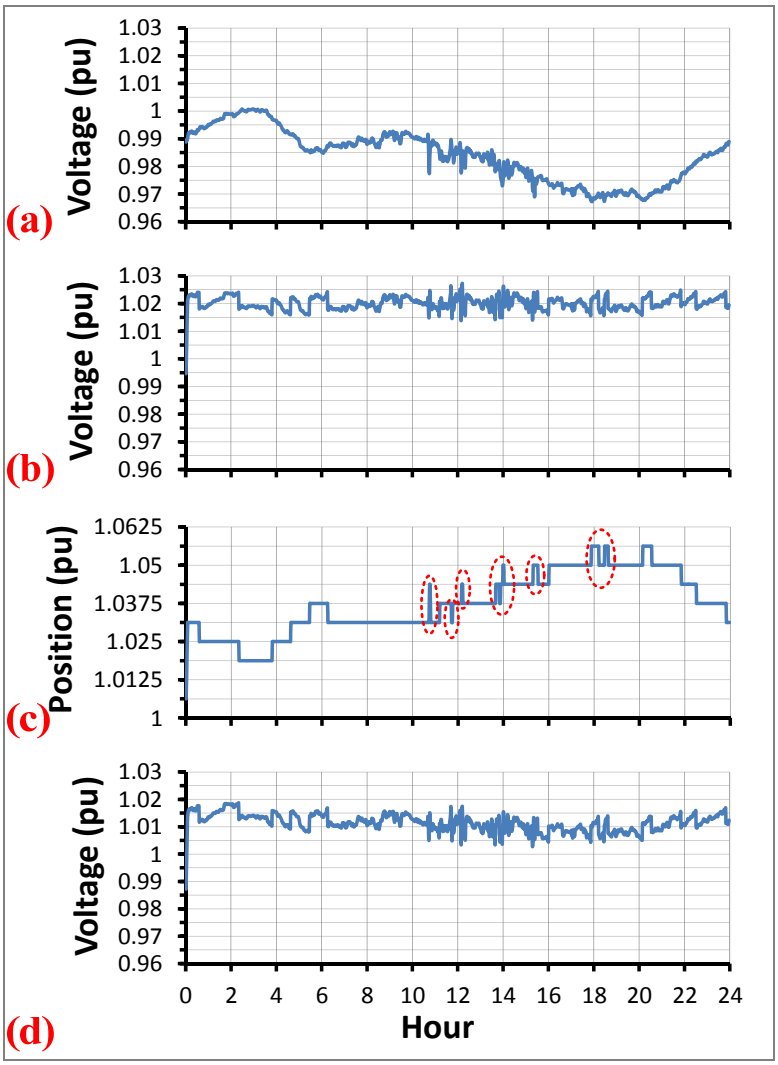

Figure 4.22. Simulation result – (a) voltage at the primary side of regulator; (b) voltage at the secondary side of regulator; (c) regulator tap position; (d) voltage profile of end-of-circuit.

4.8. Conclusion

In this chapter, the time-varying nature of solar-energy is discussed and it has been shown that it is essential to perform the time-series simulation due to this fact. Moreover, impacts of large-scale solar energy penetration in power distribution circuit, such as reverse power flow, protection issues, voltage profile variation, increased operation of

voltage regulator and capacitor bank are explained. In order to do time-series simulation, it is needed to use measurement data which are generally unequally spaced time-series data. Thus, it is required to interpolate, resample them with fixed time-interval and convert them to equally spaced time-series data. An application is developed in this chapter to read the measurement data, interpolate and resample them with fixed time-interval. In addition, it has been shown that the resolution of data used for time-series simulation plays an important role in obtaining correct insight into the impacts of time-varying solar energy penetration. Inadequate resolution may results in missing the high-variability points in the measurement data which are of greatest concern. Therefore, it is essential to find the proper sampling time-interval to avoid missing the high-variability points which have the significant impact on the operation of circuit. In this chapter, an application is developed to show the amount of error for different values of resampling time-interval. Thus, this visualization application can be helpful to select the proper sampling time-interval to keep the error of interpolation below the specified value. Furthermore, approaches to validate the model of line/cable and load are discussed and it has been shown that cumulative distribution of line/cable types regarding their length and loads regarding their power rating can be great indicator to prioritize which line/cable types or loads should be validated due to their significant impacts on the circuit.

A distribution circuit from SCE power utility, which is originally modeled in CYME, is considered in this chapter. Since CYME cannot perform the time-series simulation, an application developed in MATLAB is used to transfer PSCMD from CYME into OpenDSS. The measured power generation of both 1.5MW and 3.5MW solar plants

along with the measured native load profile of the feeder are imported into OpenDSS and its impacts on the line power loss, voltage fluctuation, and capacitor banks and voltage regulator operation are investigated. It has been shown that the intermittency of solar energy penetration can cause the voltage rise/drop and increase the number of operation of capacitor banks and voltage regulator. Moreover, it has been shown that the parameter setting of capacitor banks can affect its operation during the intermittency of solar energy generation.

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