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LOS ANGELES

Vertical Electron Transport Across and Into A Two-Dimensional Material Using Vertical Tunnel Structures and Electron Tunneling Spectroscopy

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Materials Science and Engineering

by

Shin-Hung Tsai

2020

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2020

ABSTRACT OF THE DISSERTATION

Vertical Electron Transport Across and Into A Two-Dimensional Material

Using Vertical Tunnel Structures and Electron Tunneling Spectroscopy

by

Shin-Hung Tsai

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2020

Professor Kang L. Wang, Chair

Over 50 years, Moore's law has successfully predicted the progress of silicon electronics industry. However, Moore's law is approaching to the end recently, and new material and novel device type will be needed for next-generation devices. Two-dimensional (2D) layered material is one of the promising candidates due to its intrinsic desirable features, such as diverse electronic and magnetic properties, carrier mobility protection with deceasing body thickness, and flexibility for wearable applications. Furthermore, hetero-structure comprising of 2D crystals is of growing interest since various combinations are possible for multiple purposes as more and more van der Waals materials have been discovered. In a hetero-structure, electron can propagate not only within 2D in-plane direction but also vertical out-of-plane direction. However, our understanding on the vertical carrier transport is greatly less than that on lateral. Thus, using lateral electron energy band diagrams are still the main vehicle in 2D vertical hetero-structure device analysis, which may not be correct.

In this dissertation, silicon based tunneling devices were fabricated and used to investigate electron transport properties when electrons go into or go across a 2D materials with the measurement of electron tunneling spectroscopy. We firstly examine the role of 2D sheet when electrons propagate perpendicularly across it. Here graphene is used as a platform since it is the earliest discovered one, and it has the most mature development including understanding and growth techniques. Graphene together with its neighboring van de Waals gaps serve as a tunnel barrier and barely has interaction with the vertically tunneling electrons. However, since graphene can still trap a fraction of carriers, we can take advantage of it and control the carrier flux via the adjustment of graphene electrical potential.

In addition to vertically propagating across a graphene sheet, electrons can go into graphene lateral band structure and transport within graphene. In chapter 3, we introduce a new model of the interfacial oscillation states at graphene-silicon hetero-junction, which is found and confirmed for the first time. Because of the present of this discrete interfacial quantum state, Fano-Feshbach resonance is induced by its interaction with graphene's continuum lateral energy diagram. This study provided a further elucidation of interfacial effect in a low-dimension materials based system.

The capability of our silicon based tunneling device along with electron tunneling spectroscopy is not limited to graphene-silicon interface but also able to investigate electron in-plane transport behavior within 2D hetero-structure. Since large-size devices and their macroscopic characteristics would be needed for our everyday applications in the future, the strength of our tunneling device over the conventional scanning tunneling spectroscopy with a sharp tip is its scalable detecting area. Here, a study on graphene/hexagonal boron nitride hetero-stack prepared by chemical vapor deposition and large-area wet transfer techniques shows

multiple secondary Dirac points and the preferred relative rotation angle of ~4° and ~7°. Theoretical calculation was also implemented to support our experimental observation. Raman spectroscopy and scanning tunneling microscope were carried out to confirm the Moiré pattern formation. This study provides a useful way to macroscopically conduct a research on electronic behavior of a van der Waals material, and our finding may be used when graphene/hexagonal boron nitride hetero-structure is pushed to practical applications. Undoubtedly, further careful study is needed for more detailed verification.

The dissertation of Shin-Hung Tsai is approved.

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Mark S. Goorsky

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University of California, Los Angeles

2020

To my family

for their love and tireless dedication to my education

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Acknowledgments

I would like to express my sincere appreciation to my advisor, Professor Kang L. Wang, for his research guidance, his support and his optimistic and positive attitude and encouragement. I have learnt a lot from his experience and profession.

I would also like to thank Prof. Dwight C. Streit and Prof. Mark S. Goorsky in Department of Materials Science and Engineering and Prof. Chee Wei Wong in Department of Electrical and Computer Engineering for their insightful comments, valuable suggestions and their willingness to participate in my PhD dissertation review.

As a member of DRL (Device Research Lab), I am so blessed to have to opportunity to work with these talented and hard-working colleagues. I deeply appreciate their friendship, selfless sharing, and fruitful discussion, especially Dr. Yann-Wen Lan and Dr. Sidong Lei.

I also want to thank all my friends in Los Angeles (too many to name all). During the period of my PhD career, I have been through several unexpected, difficult and tough times. Without all your physical and mental helps, I would not be able to go that far to here.

Last but definitely not least, my parents and my brother. I cannot find any word on the earth to express my greatest gratitude to my family. Their unconditional love, sacrifice and support make me “me” and drive my life over the years.

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Chapter 1 Introduction

1.1 Desires for Novel Materials and Device Concept

For the past fifty years, the prediction of Moore's law successfully matched the development of silicon electronics industry, and silicon (Si) based transistors has become much smaller and faster than fifty years ago, making portable modern electronic devices possible. However, we are now facing the scaling limit of silicon complementary metal-oxide-semiconductor (CMOS) technology, and the gate-length scale has stalled for several years (see **Figure 1-1**).[1] Therefore, novel materials and device concept is eagerly needed for the next-generation information processing.

For conventional metal-oxide-semiconductor field-effect transistors (MOSFETs), short channel effect is one of the most limiting factors that impede the extension of Moore's law. Since the transistor channel length becomes shorter and shorter, the influence of drain-induced barrier lowering (DIBL) on device performance gets more and more severe, as shown in **Figure 1-2**.[1] The consequence of short channel effect is high off-state leakage current. It means that transistor becomes more difficult to be completely turned off as the gate dimension shrinks. As a result, dissipated power density would also be largely increased.[2] Therefore, the control of leakage current is especially important for transistor scaling-down. New device concept should be introduced to solve this problem.[3,4]

This short channel effect is obvious when channel length is comparable to or smaller than five times of the electrostatic length $\lambda = \sqrt{\frac{\varepsilon_S}{\varepsilon_{OX}} t_S t_{OX}}$, where t_S and ε_S is body thickness and

dielectric constant of the channel, and t_{OX} and ε_{OX} is thickness and dielectric constant of the gate dielectric oxide. Through a simple calculation assuming that the applied dielectric oxide is aluminum oxide (Al_2O_3), t_{OX} is 0.8 nm and channel length is 5 nm, the required body thickness should be as thin as around 0.82 nm for Si channel, 0.58 nm for germanium (Ge) channel and 0.74 nm for silicon germanium (SiGe) channel. It is worth noting that they are all less than 1 nm. For current deposition technology, a uniform and defectless 1-nm channel would cost a large amount of money, which is not economically efficient. Furthermore, three-dimensional (3D) materials suffer from another serious problem with thinning body thickness, severe mobility degradation for body thickness of less than 5 nm.[5] With a low carrier mobility, on-state current and operating power would not be enough for driving a high-power end application. Thus, novel materials must be employed for future electronic device development. Two-dimensional (2D) van der Waals (vdW) material is one of the potential candidates to replace Si or other 3D materials.[6–8] First, these 2D layered materials are inherently thin down to 0.3 nm of monolayer graphene and 0.65 nm of single-layer transition metal dichalcogenide (TMD) family members.[9] Second, the decrease in mobility with decreasing thickness in 2D materials is not as significant as 3D crystals. **Figure 1-3** shows the relation between body thickness and carrier mobility.[5] Clearly, 2D materials exhibit its potential for replacing silicon in the future device development.

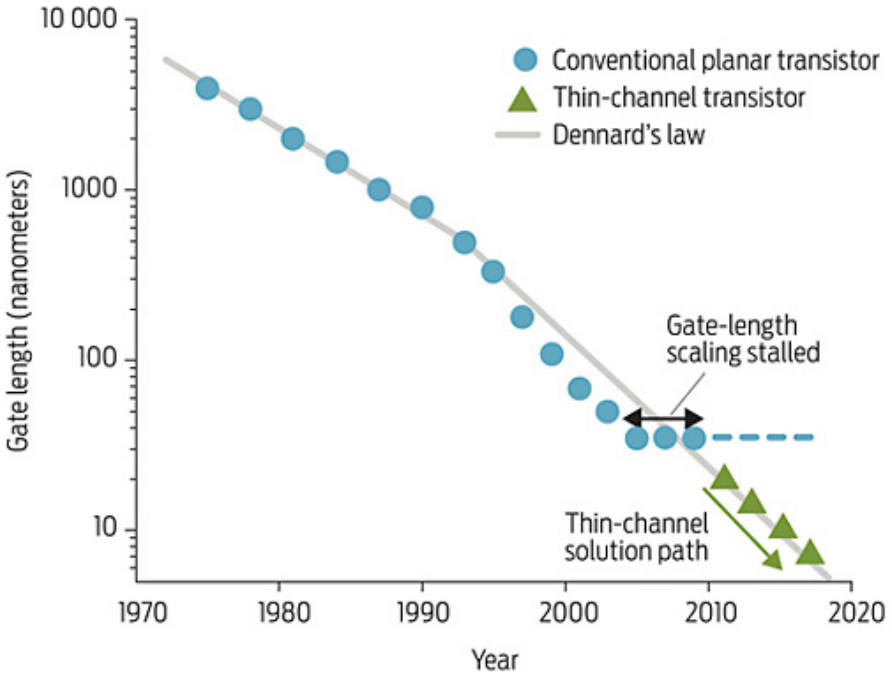
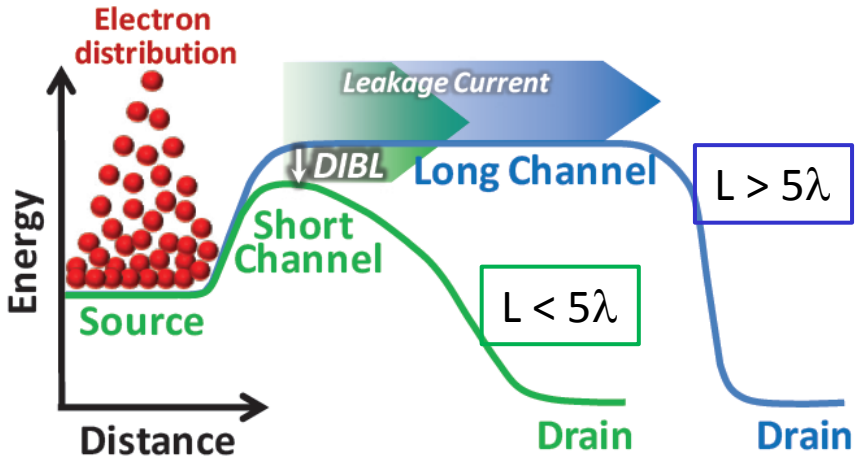


Figure 1-1 Recent development of MOSFET gate length.[1]



DIBL: Drain-Induced Barrier Lowering

Figure 1-2 Illustration of short channel effect (λ is electrostatic length).[1]

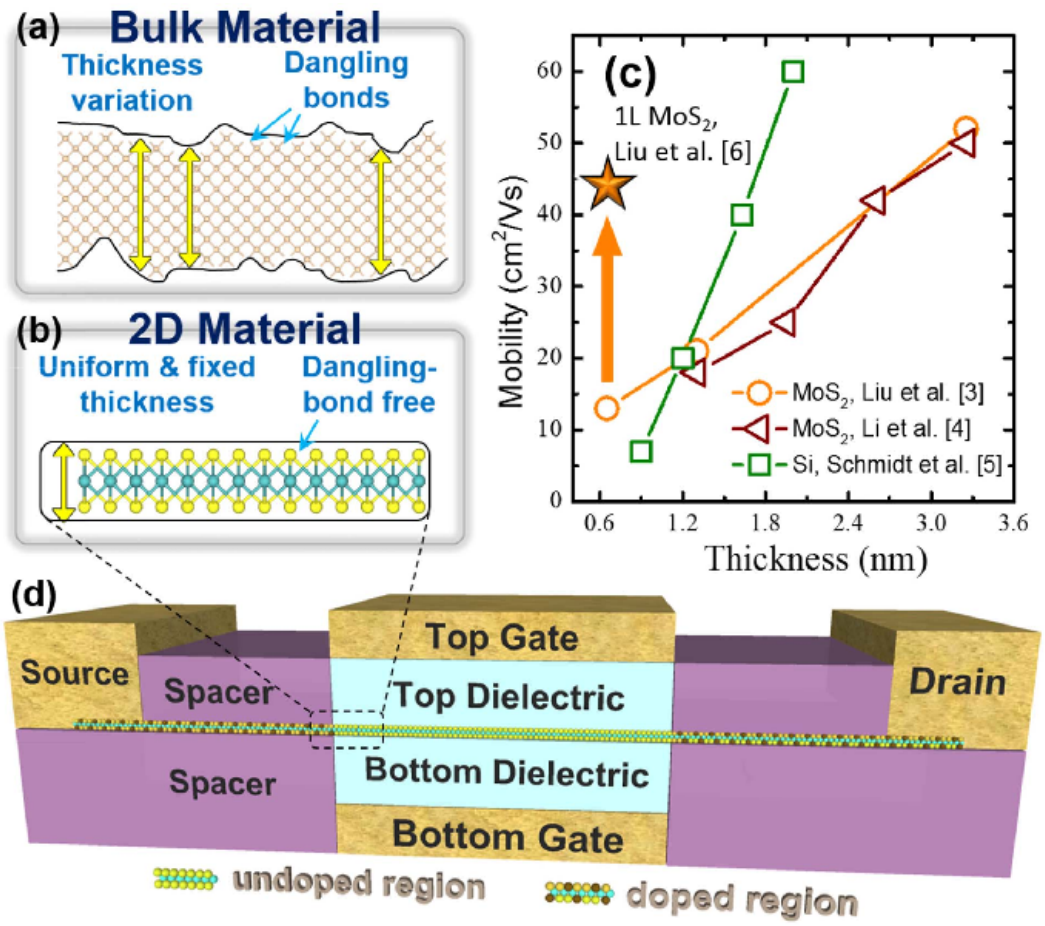


Figure 1-3 (a) Material issues when decreasing a FET based on a bulk material. (b) Advantages of 2D vdW materials over 3D materials. (c) Carrier mobility degradation as a function of reduced body thickness for Si and MoS_2. A work on MoS_2 carrier mobility improvement is also included. (d) Device structure schematic of a 2D FET.[5]

1.2 The Advent of Two-Dimensional Materials

2D vdW materials, such as graphene and TMD family, have been intensively studied for several years since their physical isolation in 2004 and 2005. They are layered crystals, and only a weak vdW interaction between each layer. Therefore, they could be easily exfoliated and stacked together (**Figure 1-4**).[10] Similar to building blocks of unit cell thickness (e.g. reminiscent of atomic-scale Lego blocks), we can form atomic-scale hetero-structures featuring novel optoelectronic phenomena and functionalities. Moreover, 2D vdW crystals cover a broad range of electrical properties from insulating hexagonal boron nitride (h-BN), n-type semiconducting molybdenum disulfide (MoS_2), p-type semiconducting tungsten diselenide (WSe_2), to semi-metallic graphene (Gr).[11,12] Not only do 2D layered materials show diverse electrical properties, but they can also perform magnetism intrinsically[13,14] or through doping[15–17] and proximity effect.[18,19] In addition, since 2D vdW materials are atomically thin, they also possess advantages such as flexibility and light weight. Besides, because of quantum confinement effects, single-layered 2D crystals perform totally different electronic band structure compared to their bulk counterparts.[20,21] This feature could be very useful because 2D materials can fit our device design when we are trying to meet different purposes. Furthermore, owing to the atomic-scale thickness and lack of surface dangling bonds of these 2D vdW materials, custom-design of atomically abrupt and clean hetero-interfaces without the need of epitaxial growth is achievable.[22] Recently, large-scale growth of high-mobility monolayer Gr and TMDs with wafer-size homogeneity has been demonstrated.[23] It means that practical applications based on 2D vdW crystals may be within our reach.

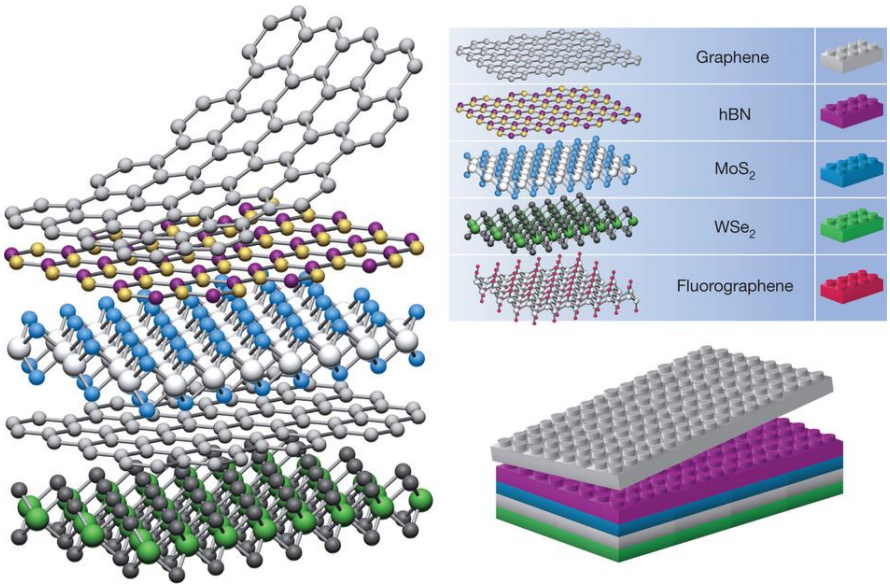


Figure 1-4 Illustration of hetero-junction construction of 2D van der Waals materials.[10]

1.3 Van Der Waals Materials Hetero-structure

1.3.1 Application of 2D Hetero-structure

With the advantages provided in the previous content, pristine 2D materials are promising and gaining a great deal of attentions. Combining different types of 2D materials to create an unprecedented electronic property, magnetic property or a function specific to a certain application is also an appealing idea. Indeed, hetero-structure with various 2D crystal combinations has been intensively studied and offers a platform with a variety of properties, which can be adapted to several areas of applications.

When it comes to 2D materials hetero-structure, these 2D crystals can be fabricated into a monolayer (lateral hetero-structure) or a multilayer stack (vertical hetero-structure). Lateral hetero-structure can be achieved by several methods. The first 2D lateral hetero-structure was based on Gr and h-BN and was demonstrated by M. P. Levendorf et al. in 2012 on *Nature*.[24] CVD-grown Gr sheet was patterned by optical lithography and etched, and synthesis of h-BN film was then carried out via CVD, forming a one-atomic-thin hetero-structure (see **Figure 1-5**). Beyond Gr and h-BN, TMD lateral hetero-structures were heavily studied because of their exceptional potential in the integrated optoelectronic devices,[25,26] as shown in **Figure 1-6**.[26] As for vertically stacked van der Waals hetero-structure, the first demonstration was introduced in 2010 on *Nature Nanotechnology* by C. R. Dean et al. with Gr and h-BN through placing Gr on top of multi-layer h-BN films (See **Figure 1-7**).[27] They showed that Gr exhibits an excellent electronic performance when supported by h-BN substrate. Since then, these types of atomically thin 2D hetero-structure (including Gr, h-BN and other TMD) have drawn extensive attention, and many exciting experimental results have been come out. For both lateral and vertical cases,

2D hetero-structures are generally promising in several areas of application, such as high-mobility electronics,[28] tunneling field effect transistors,[29] memory devices,[30] light-emitting diode,[31,32] photovoltaics,[33] *etc*. Therefore, hetero-structure comprising of vdW materials have been attracting growing interest in the past years.

In the following content and chapters, I will focus on vertically stacked 2D hetero-structure because of its mature device development and easy process steps. Compared to covalent bond formation between atoms at the material-switched junction during lateral hetero-junction synthesis, vertical hetero-structure can be produced via chemical wet transfer, polymer-free wet transfer or exfoliation dry transfer techniques. Combination variety is also an issue for lateral vdW hetero-structure. With creation of covalent bonds between different 2D materials, lattice mismatch must be taken into consideration; on the other hand, the attractive force between vertical layers is vdW force, indicating we can readily stack arbitrary 2D crystals simply by transfer methods.

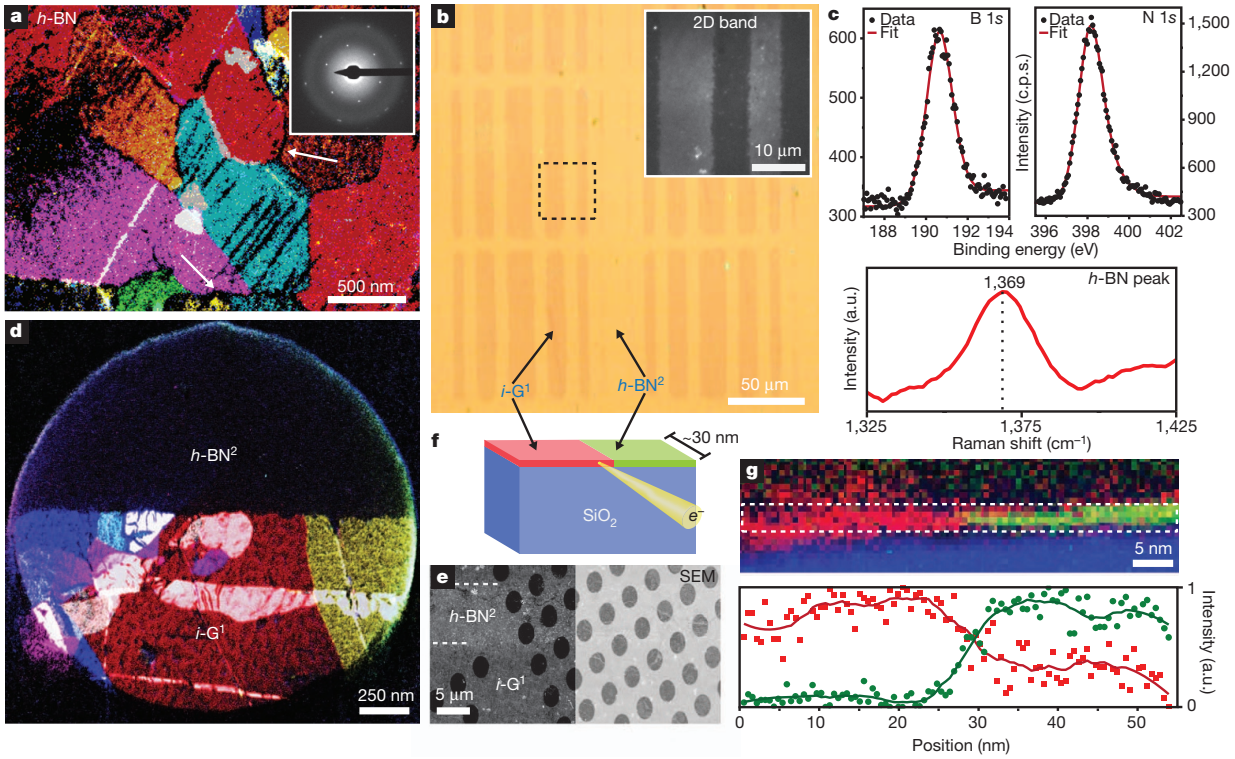


Figure 1-5 Gr/h-BN lateral hetero-structure. **(a)** False-color dark-field transmission electron microscopy image of an h-BN sheet. (Inset) Refraction image of the h-BN structure. **(b)** Optical image of a Gr/h-BN hetero-structure on Si/SiO_2 substrate. **(c)** X-ray photoelectron spectroscopy (upper) and Raman (lower) data on h-BN crystal. **(d)** False-color dark-field transmission electron microscopy image of a suspended Gr/h-BN film. **(e)** Scanning electron microscope image of a suspended Gr/h-BN film. (Left) Gr/h-BN regions (Right) the suspended film. **(f)** Cartoon illustration of cross-section scanning transmission electron microscope and electron energy loss spectroscopy. **(g)** (Upper) Element mapping of a Gr/h-BN junction (Lower) Element intensity profile (Red: carbon, Green: boron, Blue: oxygen).[24]

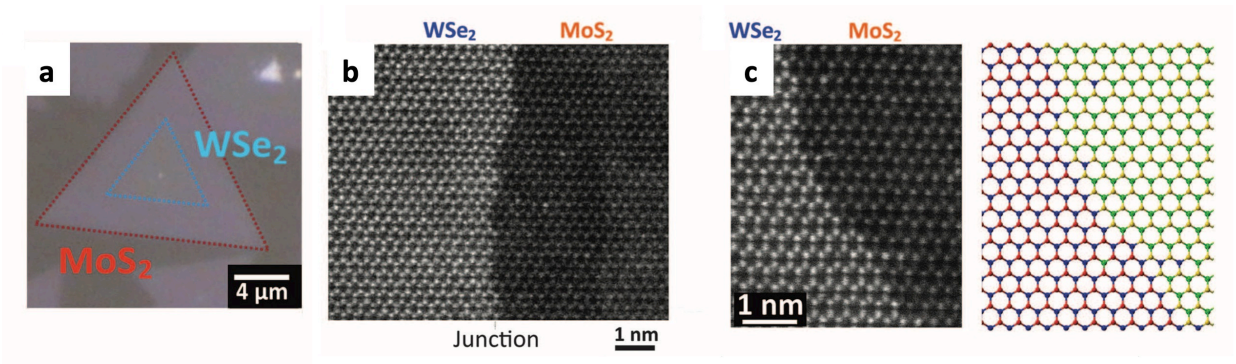


Figure 1-6 Images of WSe_2/MoS_2 in-plane hetero-structure **(a)** Optical image. Lines are added to emphasize the boundaries. **(b and c)** High resolution scanning transmission electron microscope images.[26]

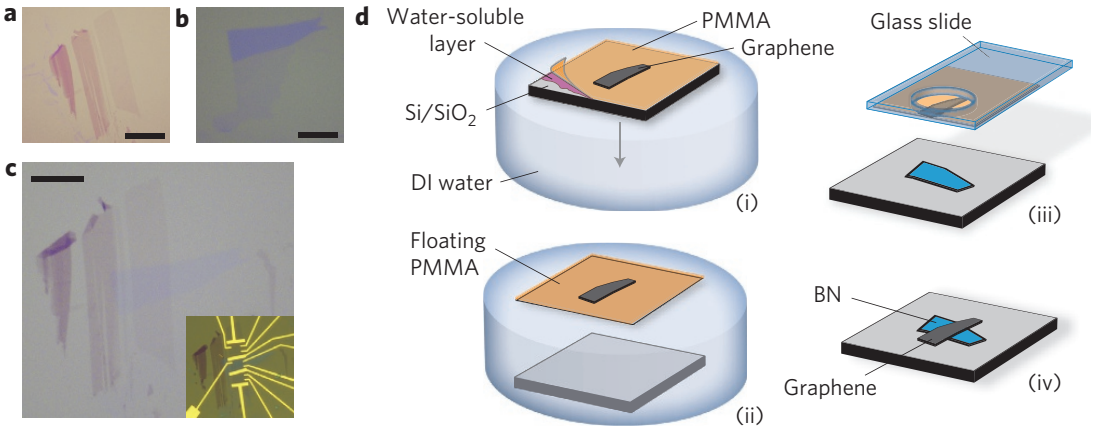


Figure 1-7 (a-c) Optical images of exfoliated Gr, h-BN and Gr/h-BN hetero-structure **(d)** Schematics of the transfer process.[27]

1.3.2 Model of Electron Vertical Transport in 2D Hetero-structure and Their Issues

The unique features and promising capabilities of vdW materials and their vertical hetero-structure have been introduced in the previous content. Not only does the carrier lateral transport in a vertically stacked 2D hetero-structure gain focus, but also the carrier out-of-plane transport via quantum tunneling effect has been extensively experimented. This has rapidly emerged as one of the most interesting topics in the low dimensional material research field, and led to the realization of novel electronic devices, including resonant tunneling diodes,[34,35] tunnel field effect transistors (TFET),[7] hot electron transistors (HET),[36–39] optoelectronic devices,[33,40] as well as spintronic applications.[41,42] However, the physics when electron vertically propagating across the dangling-bond free surface still remains unclear and mysterious. The major vehicle to investigate it is lateral transport measurement, and lateral band diagrams of the stacked 2D crystals are used to analyze the electron transport in normal direction.[7,21,32,40] This might not be correct, or even misleading, since the lack of a periodic crystal structure along the out-of-plane direction of a layered material would lead to a dramatically different transport mechanism from that in the lateral. Therefore, a deep understanding of role of 2D material, interaction between carrier and elements, and interfacial states and exchange interaction in electron vertical transport across 2D layers is essential.

Here in this dissertation, in order to examine electron vertical transport, a silicon-based vertical tunneling device was used. For carefully and attentively focusing on our goal of electron out-of-plane transport across a vdW sheet, the structure of our tunneling devices are purposely simplified down to only one or two types of 2D sheets to avoid any unnecessary concern and interruption, and highly doped silicon was used as an electrode ejecting electrons vertically by an applied voltage difference. With a tunneling device, carrier perpendicular transport property

would be explicitly captured by the first-order electron tunneling spectroscopy (first-order current derivative), which is proportional to density of states of the material. More detailed description of electron tunneling spectroscopy will be discussed in the following content. In addition, principle of quantum tunneling effect, the relation between density of states and first order current derivative, as well as our silicon based tunneling device fabrication flow will be covered later in chapter 1.

1.4 Silicon Based Vertical Tunneling Devices

1.4.1 Device Structure

The schematic illustration (cross-section) of our silicon based vertical tunneling device is shown in **Figure 1-8a**. The degenerately doped n-type silicon (n^{++}-Si) is used as an electrode to eject electrons vertically via an electrical potential drop between it and Gr. Two chromium/gold (Cr/Au) contacts are connected to Gr with side-contact technique to avoid the contact resistance issue. The field oxide is around 500 nm thick to make sure electrons can only eject from the defined area. A DC+AC voltage source is utilized for lock-in amplifier detection. **Figure 1-8b** is the top-view optical image, and the red dashed line indicates the position where the cross-section present in **Figure 1-8a**.

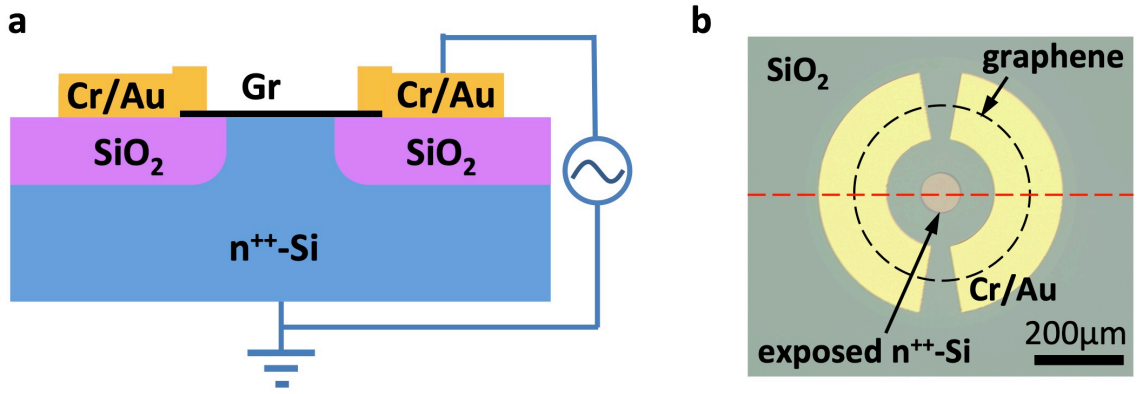


Figure 1-8 (a) Illustration of cross-section view of a silicon based vertical tunneling device. **(b)** top-view optical image of a silicon based vertical tunneling device (a circular exposed n^{++}-Si working area with a diameter of around 90 μm).

1.4.2 Fabrication of Silicon Based Vertical Tunneling Devices

The complete process flow is described as follows:

1. Growth of Buffer Oxide

   First, we prepared 4-inch degenerately doped n-type silicon <100> wafer (dopant concentration of ~$1x10^{19}$ cm^{-3}), and used Piranha (H_2SO_4:H_2O_2) and hydrofluoric acid (HF) to thoroughly clean the surface. The wafers were then placed into Tystar oxidation furnace order to grow a silicon dioxide (SiO_2) of ~50 nm. This buffer oxide will serve as a stress-relieving layer between silicon substrate and the to-be-deposited silicon nitride (Si_3N_4) because the viscosity of SiO_2 decreases at high temperature. Illustration after growth of SiO_2 buffer layer can be seen in **Figure 1-9**.

2. Fabrication of Si_3N_4 Hard Mask and etch of SiO_2 Buffer Layer

   This step involves defining the area on the silicon wafer in which the Si-SiO_2 interface resides at a lower position than the rest of the silicon surface. After cleaning the buffer oxide surface with heated Piranha and DI water, we used a STS-MESC PECVD (Plasma Enhanced Chemical Vapor Deposition) Multiplax system from Surface Technology Systems to deposit a Si_3N_4 layer of ~225 nm across the entire wafer surface. Photolithography was then performed to define the various arrays of circular disks of photoresist on Si_3N_4 layer. We then used a STS-MESC Multiplex AOE (Advanced Oxide Etcher) from Surface Technology Systems to dry etch the Si_3N_4 and SiO_2 which is not covered by photoresist disks and expose silicon. See **Figure 1-10** for the illustration.

3. Growth of Field Oxide

   This step is to have thick field oxide (SiO_2) formed between tunneling device in order to electrically isolate them from each other. Again, to remove any organic residues on the Si_3N_4 and/or SiO_2 surface, cleaning with heated Piranha and DI water is needed. Subsequently, we placed the wafers into the Tystar thermal oxidation furnace to grow field oxide with thickness of ~650 nm. **Figure 1-11** shows the cartoon cross-section and top-view.

4. Selective Wet Etch of Si_3N_4 Mask

   The function of the Si_3N_4 layer is to act as a mask for field oxide growth. Here we need remove the Si_3N_4 disks to expose the active area. During the previous thermal oxidation step, SiO_2 might also grow on top of Si_3N_4; therefore, we firstly dip the wafer into buffered oxide etchant [HF:HN_4OH] BOE (6:1) for a short time in order to remove the SiO_2 on Si_3N_4. Afterwards, for selectively etching Si_3N_4, hot phosphoric acid (H_3PO_4) at 160°C − 165°C was used for ~2 hours. See **Figure 1-12** for the illustration.

5. Formation of Graphene-Silicon Junction

   After removing Si_3N_4 mask, circular active areas are without Si_3N_4 but still covered by a thin SiO_2, which is the buffer oxide layer we grew in step 1. Therefore, we performed a BOE etching for ~60s to expose the silicon surface. A single layer of Gr was then transferred onto the silicon exposed active area to form a Gr-Si junction. After polymer/Gr stack was attached to the silicon surface, we move it into a dry nitrogen filled glove box to prevent the formation of SiO_2 in between. After removing the polymer carrier, a thermal annealing at 300°C under H_2/Ar environment was performed

to thoroughly clean the Gr surface. See **Figure 1-13** for the illustration in which the Gr edges are highlighted by dash lines for clarification.

6. Grapehen Patterning and Deposition of Cr/Au Contact

   We proceeded with optical lithography technique in order to define circular disc regions of photoresist with a diameter larger than silicon working areas to mask and protect the underlying Gr. Afterwards, the samples were placed into a Tegal PlasmaLine 515 Photoresist Asher and dry etch the Gr which is protected by photoresist. We then used acetone to strip the photoresist.

   Subsequently, another photolithography was applied to open a window for contact metal deposition. CHA Mark 40 E-beam Evaporator Metal Deposition system was used to grow a 10nm/100nm chromium/gold film as an ohmic contact material to Gr. We then used acetone to strip the photoresist. See **Figure 1-14** for the illustration.

7. Evaporation of Aluminum Oxide Protection Layer

   Finally, we placed our device into a CHA Mark 40 E-beam Evaporator Metal Deposition chamber to deposit a 3.5 nm thick aluminum film with a low rate of 0.1 Å/s for uniformity. After exposed to air, the aluminum would be converted into aluminum oxide to protect the entire device. **Figure 1-15** shows the complete device configuration.

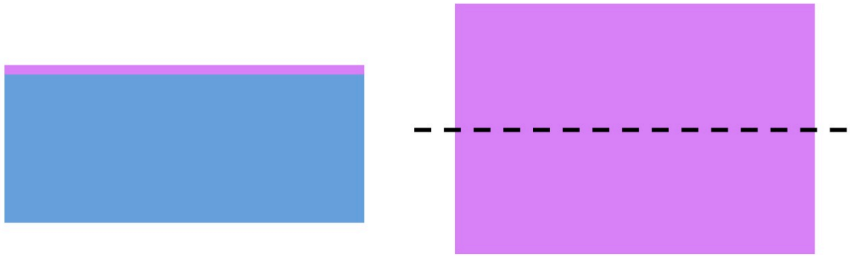


Figure 1-9 (Left) Cross-section and (Right) top-view illustration after the process step of buffer oxide growth.

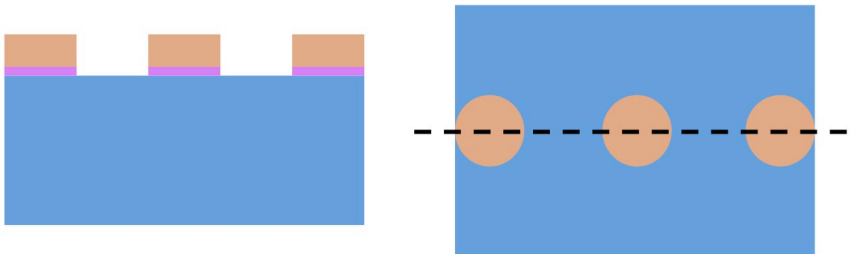


Figure 1-10 (Left) Cross-section and (Right) top-view illustration after the process step of Si_3N_4 hard mask fabrication and SiO_2 buffer layer etch.

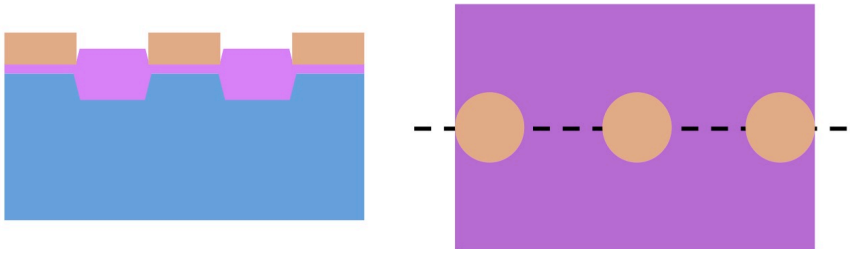


Figure 1-11 (Left) Cross-section and (Right) top-view illustration after the process step of thick field oxide growth.

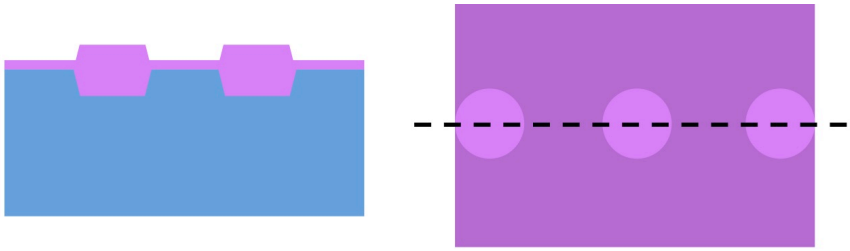


Figure 1-12 (Left) Cross-section and (Right) top-view illustration after the process step of Si_3N_4 selective wet etch.

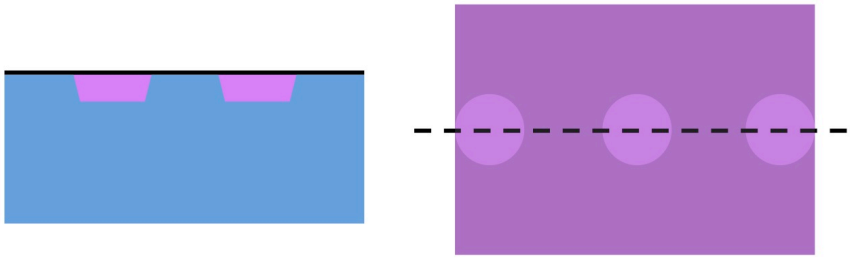


Figure 1-13 (Left) Cross-section and (Right) top-view illustration after the process steps of graphene transfer technique and graphene-silicon formation.

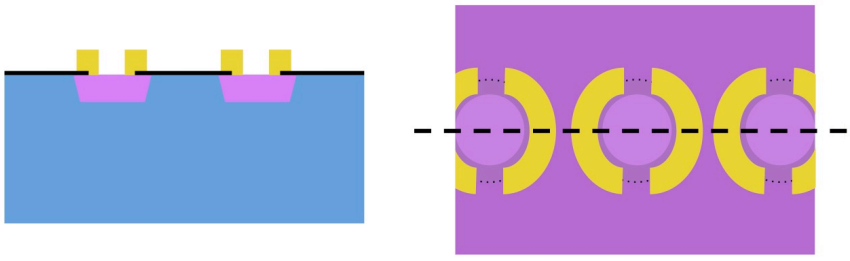


Figure 1-14 (Left) Cross-section and (Right) top-view illustration after the process step of graphene patterning and Cr/Au contact deposition.

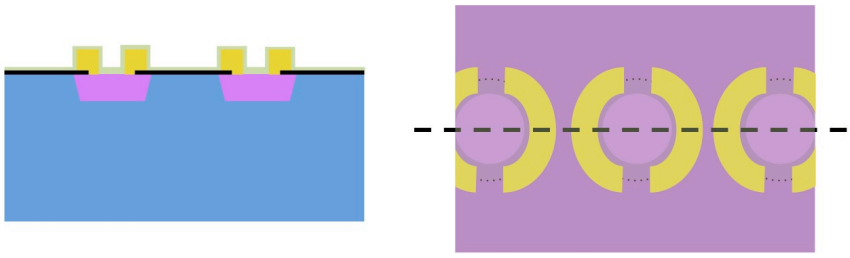


Figure 1-15 (Left) Cross-section and (Right) top-view illustration after the process step of formation of aluminum oxide protection layer.

1.5 Tunneling Devices and Electron Tunneling Spectroscopy

1.5.1 Quantum Tunneling Behavior

Tunneling is one of the breakthroughs in quantum physics from classical physics. In quantum physic, wave-particle duality of matter was introduced, which, along with Heisenburg uncertainty principle, successfully clarifies several phenomena that cannot be adequately explained by classical mechanics.

Classical mechanics considers matters as particles, so if the particles do not have sufficient energy to classically surmount or penetrate an energy barrier, the other side of the barrier is not accessible to them. However, in quantum mechanics, with the wave-like property, these particles are able to tunnel through the barrier with finite transmission probability.

From Schrödinger equation with the assumption of infinite z-direction,

$$\widehat{H}|\Psi(z,t)\rangle = i\hbar\frac{\partial}{\partial t}|\Psi(z,t)\rangle \tag{1.1}$$

wavefunction at other side of the barrier is not zero as depicted in **Fig. 1-16**, in which V is the energy barrier height and E is the particle energy (E<V). It is worthy to note that the transmission probability T is independent of temperature.

$$T \propto exp\left(-\frac{2L}{\hbar}\sqrt{2m(V-E)}\right), \tag{1.2}$$

where L is barrier width, $\hbar = \frac{h}{2\pi}$, and h is Plank constant.

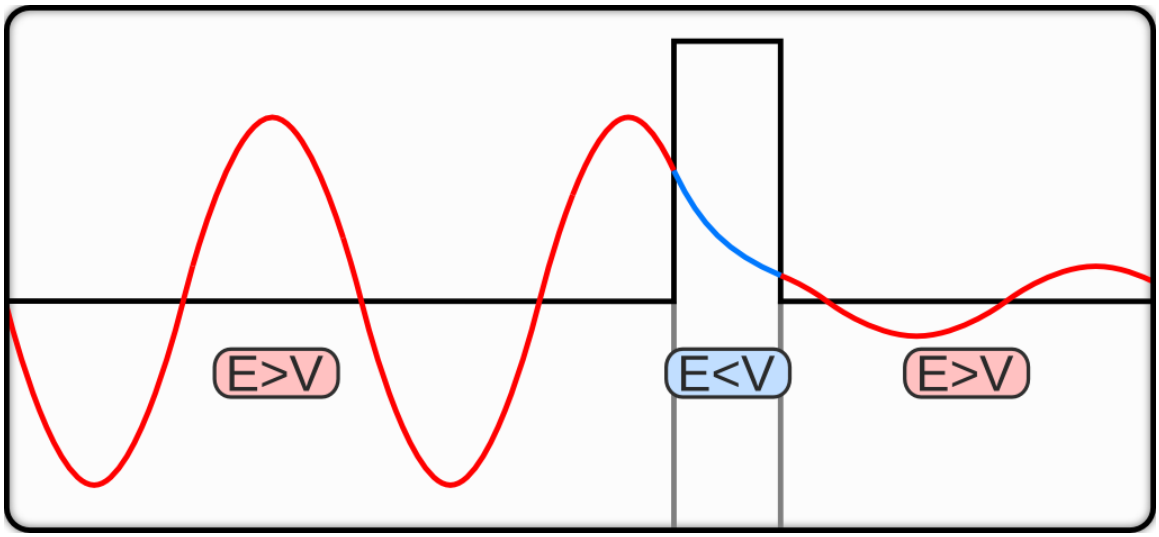


Figure 1-16 The wavefunction under a tunneling process. (Ψ: wavefunction; V: energy barrier height; E: energy of the particle).

1.5.2 Electron Tunneling Spectroscopy

Electron tunneling spectroscopy is used to provide information about the density of states of electrons in a sample as a function of electron energy. An electrode (in our case, it is degenerately doped silicon) is placed closely next to the target material (here we are using Gr or Gr/h-BN as a platform in this dissertation), and an external electrical voltage difference is applied to the electrode and the material. With the distance between the electrode and the sample fixed, the electron tunneling current is then measured as a function of electron energy by varying the applied electrical potential. The change of measured current with the electrode-sample bias (i.e. the electron energy) can be obtained and recorded. That is usually called I-V curve. However, as shown below, the slope of I-V curve, which is dI/dV curve, is more fundamental and important to us since the tunneling conductance (i.e. dI/dV) corresponds to the electron density of states of the target sample. It is noteworthy that electron tunneling spectroscopy is similar to scanning tunneling spectroscopy, which uses a tiny and sharp metal tip instead of an areal electrode. Scanning tunneling spectroscopy is used to determine "local" density of states at the tip position; however, electron tunneling spectroscopy is determining the overall electron density of states of the sample.

Here we will have explanation as well as derivation for showing the relationship between carrier density of states and tunneling conductance, which can be collected by electron tunneling spectroscopy. In the previous content, we introduced the fundamentals of quantum tunneling phenomenon because electron tunneling spectroscopy is relying on tunneling effect and measurement of tunneling current or its derivative. With treating tunneling as a perturbation to the system, Bardeen transfer Hamiltonian method can be modified, and the tunneling current is found to be

$$I = \frac{4\pi e}{\hbar}\int_{-\infty}^{\infty}\left[f(E_F - eV + \varepsilon) - f(E_F + \varepsilon)\right]\rho_S(E_F - eV + \varepsilon)\rho_E(E_F + \varepsilon)\left|M_{\mu\nu}\right|^2 d\varepsilon\,, \tag{1.3}$$

where $f(E) = \dfrac{1}{1 + \exp(\dfrac{E - E_F}{k_B T})}$ is the Fermi-Dirac distribution function, ρ_S and ρ_E are the electron density of states in the sample and the electrode, and $M_{\mu\nu}$ is the element in tunneling matrix between the modified wavefunctions of the sample and the electrode. Note that the energy lowering due to the interaction between the two involved states is captured in the tunneling matrix element, as shown below:

$$M_{\mu\nu} = -\frac{\hbar^2}{2m}\int_{\Sigma}\left(\chi_\nu^*\vec{\nabla}\psi_\mu - \chi_\mu^*\vec{\nabla}\psi_\nu\right)\cdot d\vec{S}\,, \tag{1.4}$$

where χ and ψ are the sample wavefunction modified by electrode potential and electrode wavefunction modified by sample potential, respectively.

In order to simplify the current equation, we assume a low-temperature environment and constant tunneling matrix element. Thus, equation (1.3) can be reduced to

$$I \propto \int_{-\infty}^{\infty}\rho_S(E_F - eV + \varepsilon)\rho_E(E_F + \varepsilon)\,d\varepsilon\,. \tag{1.5}$$

Under the gross condition that the electrode density of states is constant, equation (1.5) implies that

$$\frac{dI}{dV} \propto \rho_S(E_F - eV)\,. \tag{1.6}$$

With these ideal assumptions, the tunneling conductance is directly proportional to the sample density of states.

In our case, we used highly doped silicon as the electron, and graphene is our 2D material platform to investigate electron vertical transport property and interaction with 2D materials.

1.6 Synopsis

2D layered van der Waals materials came with the hope to overcome the obstacle of shrinking transistor size and doubling transistor density in a simple chip. The concept of hetero-structure further makes device type and applicable area more flexible and diverse. However, carrier vertical transport across or into a 2D crystal still remains mysterious and unclear since the lateral energy band diagrams and the propagating properties within 2D materials may not be useful, or even incorrect, for carrier out-of-plane transport. The objective of this dissertation is to discover and study the role of layered materials in electron perpendicular transport and to investigate the interaction between carrier and 2D crystal when electron propagating vertically across or into a 2D material. Additionally, targeting at future scalable practical applications, we take advantage of the areal detectable Si electrode in our tunneling device structure to investigate the macroscopic transport property in Gr/h-BN hetero-stack.

Chapter 2 presents the fundamental understanding of the role of a monolayer 2D material (here we use a single-layer Gr as a platform for 2D material due to its mature growth technique) in electron vertical transport across a vdW material. Although performing like a conductor in its lateral lattice plane, Gr also act as part of a tunneling barrier in electron vertical transport. In other words, the vertically propagating electrons would NOT interact with it due to its atomic thickness and the transverse momenta mismatch between the ejected electrons and the Gr band structure. Meanwhile, Gr as a lateral conductor is able to accumulate charges and control the carrier flux, indicating that potential across this structure can be tuned. A new model on the vertical tunneling is developed to elucidate the possible tunneling process modulation through this transparent and two-dimensional Gr grid based on the quantum capacitance's effect.

Chapter 3, with the same device structure, describes interfacial exchange process at the Gr-Si junction. This is the first time that a novel interfacial quantum state, which is specific to the 3D-2D interface, was proposed and confirmed. In addition, the interaction between this interfacial state (discrete energy spectrum) and the Gr lateral band structure (continuous energy spectrum) would result in Fano-Feshbach resonance. This funding may be useful to realize an all solid-state and scalable quantum interfereometer.

Chapter 4 introduces the Moiré-modulated conductance found in a scalable Gr/h-BN stack via vertical tunneling spectroscopy measurement. Here, instead of Gr-Si junction we used in the previous studies, a stack of Gr/h-BN/Si was fabricated with a large-size tunnel working area. Two dips were observed in our electron tunneling spectroscopy result, indicating two minimums in electronic density of states. They may be attributed to secondary Dirac points stemming from the generated Gr/h-BN Moiré superlattice. Scanning tunneling microscope was performed to verify the formation of Moiré patterns and determine the rotation angles between Gr and h-BN. The result suggests that several Moiré domains maybe formed in the Gr/h-BN stack, and two of them are most commonly found. This study may be used when Gr/h-BN hetero-structure is pushed to everyday applications.

Finally, we conclude the dissertation and propose suggested works for further research in this field.

Chapter 2 A Study of Vertical Transport through Graphene toward Control of Quantum Tunneling

(This chapter is based on the publication, *Nano Letters 2018, 18, 682-688*)

Vertical integration of van der Waals materials with atomic precision is an intriguing possibility brought forward by these two-dimensional materials. Essential to the design and analysis of these structures is a fundamental understanding of the vertical transport of charge carriers into and across van der Waals materials, yet little has been done in this area. In this chapter, we explore the important roles of single layer graphene in the vertical tunneling process as a tunneling barrier. Although a semimetal in the lateral lattice plane, graphene together with the van der Waals gap act as a tunneling barrier that is nearly transparent to the vertically tunneling electrons due to its atomic thickness and the transverse momenta mismatch between the injected electrons and the graphene band structure. This is accentuated using electron tunneling spectroscopy showing a lack of features corresponding to the Dirac cone band structure. Meanwhile, the graphene acts as a lateral conductor through which the potential and charge distribution across the tunneling barrier can be tuned. These unique properties make graphene an excellent two-dimensional atomic grid, transparent to charge carriers, and yet can control the carrier flux via the electrical potential. A new model on the quantum capacitance's effect on vertical tunneling is developed to further elucidate the role of graphene in modulating the tunneling process. This work may serve as a general guideline for the design and analysis of van der Waals vertical tunneling devices and hetero-structures, as well as the study of electron/spin injection through and into van der Waals materials.

2.1 Motivation

Quantum tunneling hetero-structures, such as magnetic tunneling junction and Josephson junctions are the fundamental building blocks of modern quantum computing and data storage systems. The emergence of vdW materials has brought the construction of quantum hetero-structures to new frontiers with precise manipulation and control down to the atomic level. vdW materials featuring dangling-bond free surfaces are ideal to be stacked together with well controlled interfaces separated by vdW gaps in between.[10] Electron tunneling through the vdW gap is a process inherent to all vdW devices, and thus it has rapidly emerged as one of the most interesting topics in the vdW material research field. This process has led to the realization of novel electronic devices, including resonant tunneling diodes,[35,43] tunnel field effect transistors,[7,44] hot electron transistors,[36–39] optoelectronic devices,[33,40,45] as well as spintronic applications.[41,42,46]

So far, the majority of research on the role of vdW materials in tunneling processes still focuses on vdW materials that are insulating in the lateral direction (such as h-BN). Meanwhile, conductive vdW materials are commonly used as the electrodes,[47–51] where the carriers are collected by the vdW materials and transported laterally along the 2D plane. Therefore, the band structure of these vdW materials as well as the carrier interaction with elementary excitations can be applied to describe the physical process, and the vertical transport process is ignored. However, the lack of a periodic crystal structure in the normal direction leads to a dramatically different transport mechanism in the vertical direction from that in the lateral. One striking example is that although Gr is typically treated as a semimetal or zero-gap semiconductor, it behaves as an insulating tunneling barrier for vertical spin injection.[42] A clear description of this

vertical transport is essential because, in many emerging device applications, charge or spin carriers travel perpendicularly through the vdW materials with limited lateral transport,[37,37,38,43,52] such as Gr's role as the base material in hot electron transistors,[37,39,53] and as the tunneling barrier for spin injection.[41,42,54–57]

Here in this chapter, by the fabrication of Gr vertical tunneling devices, we study the vertical transport process through the Gr layer together with the vdW gaps. By purposely excluding the effect of lateral transport from the structure, we provide insight into the vertical transport in single-layer Gr and identify the effects from both quantum and classical transport. Because of the transverse momentum mismatch and the atomic thinness of Gr, the vertical tunneling electrons are unable to interact significantly with the lateral Gr 2D band structure. Meanwhile, the Gr, being a semimetal in the lateral direction, can store charges and effectively tune the profile of the tunneling barrier via its quantum capacitance, thus imposing an electrical field to control the electrons in a more classical manner. A theoretical model to quantitatively explain the experimental observations and elucidate the role of Gr in vertical tunneling is established. Moreover, our model not only applies to Gr but is universally applicable for other 2D systems. This result provides a new insight on the out-of-plane transport behavior and can act as an important guideline for both experimental and theoretical efforts to the design and analysis of vdW vertical hetero-structure devices.

2.2 Result and Discussion

2.2.1 Electrical Characterization of Electron Tunneling into Graphene

The vertical tunneling device is designed to be composed of vertically stacked n^{++}-Si, Gr and a top Cr/Au electrode with the optical image and schematic diagram given in **Figure 2-1a and 2-1b**, respectively. The ⟨100⟩ n^{++}-Si is chosen as the substrate and bottom electrode due to its low surface roughness immediately after treatment of HF, to avoid puncture of the atomically thin Gr. In this configuration, the top Cr/Au contact is aligned to the n^{++}-Si injection area, so that the electrons are directly collected by the top Cr/Au electrode without lateral transport, and the Gr serves only as a tunneling medium. During the experiment, the n^{++}-Si was grounded and the voltage was applied via the top contact. As a control experiment, we also fabricated a "side contact" device (see **Figures 2-2a and 2-2b**), in which lateral propagation is included, and the Gr serves as the counter electrode with the vdW gap acting as the tunneling barrier. In this structure, the electrons are injected into the Gr from the n^{++}-Si bottom electrode and captured by Gr. Subsequently the electrons propagate laterally within the Gr sheet before they are collected by the side Cr/Au electrode. **Figure 2-2c** shows the current density−voltage (J−V) characteristics at different temperatures for this "side contact" device. **The inset of Figure 2-2c** plots the current density at $V_S = 0.5V$ versus temperature, showing little temperature dependence of J−V characteristics. Meanwhile, except for some nonlinearity, the curves do not show significant rectification. Considering these two features, it can be concluded that the interface between the Gr and the silicon is neither Ohmic nor Schottky, but of tunneling nature, and a tunneling current on the order of 0.1 A/cm^2 is observed. In this scenario, the electrons relax to the eigenstates of Gr instead of vertically passing through Gr, shown explicitly by the Dirac cone feature in the first

order electron tunneling spectroscopy (ETS). This is similar to results from previous works using scanning tunneling spectroscopy to inject charge carriers from a metal tip through a vacuum gap into Gr, and the charge carriers are collected by a side contact after propagating laterally through the Gr.[49,50] This indicates that the vdW gap at the Gr/n^{++}-Si interface acts effectively as a nanometer vacuum gap.

To identify the presence of the Gr induced vdW gap, as well as to characterize the various interfaces of the vertical tunneling structure, a cross-section transmission electron microscopy (TEM) analysis was performed. In this case, a platinum (Pt) film was deposited on top of the vertical structure to act as a protection layer for the focused ion beam milling process in the sample preparation. The high-angle annular dark field (HAADF) scanning TEM (STEM) image of the sample is shown in **Figure 2-1c**. A spatially resolved energy-dispersive X-ray spectroscopy (EDS) mapping of Si, C, Cr, and Au (**Figure 2-1d**) confirmed the layer components of the vertical structure. The Gr is visible in **Figure 2-1d** as a thin line adjacent to the Si substrate. The result of the high resolution STEM (HRSTEM) is shown in **Figure 2-1e** for the interfaces between Si/Gr and Gr/Cr. The intensity profile for the cross section of **Figure 2-1e** is shown in **Figure 2-1f**, in which the three distinct material regions can be identified. The monolayer Gr (plus the vdW gap) appears as a nanometer scale gap on top of the atomically flat Si substrate and is responsible for the observed direct tunneling behavior to be discussed in detail in the following paragraphs. However, no van der Waals gap can be distinguished from the TEM study. Unlike the H-passivated silicon, the fresh metal surface may have strong interaction with the π-orbital of Gr and form bond, thus no fully preserved vdW gap is anticipated to form.

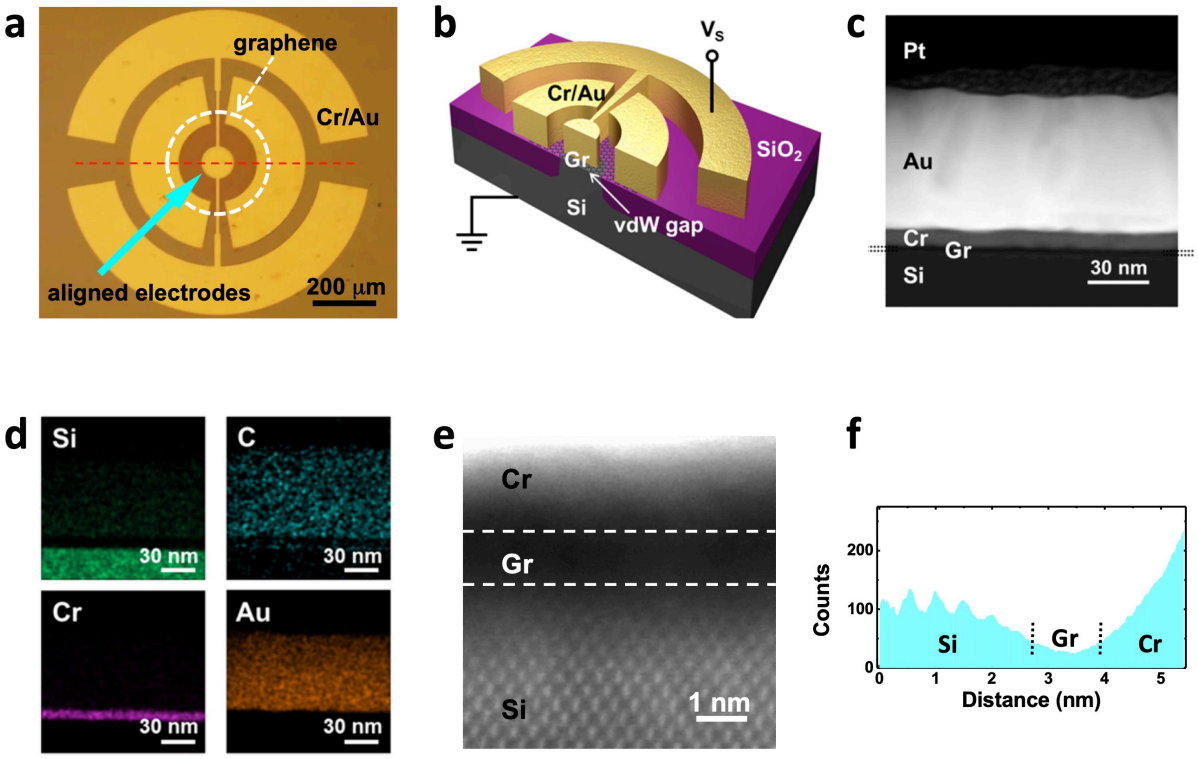


Figure 2-1 Device structure and cross-section TEM of the Gr tunneling structure. **(a)** Optical image of the fabricated device with the Gr region outlined by the white dash line. **(b)** Schematic diagram showing the device structure of the vertical tunneling device. The cross section is cut along the red dash line in (a). **(c)** Low-magnification HAADF STEM image showing the cross section of the vertical tunneling structure. The monolayer Gr and the van der Waals gap are visible as a dark line located between Si and Cr, which is outlined by the black dotted line. **(d)** Spatially resolved EDS analysis indicating the distribution of Si, C, Cr, and Au. **(e)** HRSTEM image of the Si/Gr/Cr interface revealing the existence of a gap-like feature as outlined by the white dashed lines. **(f)** Height profile from a section of the HRSTEM image in (e).

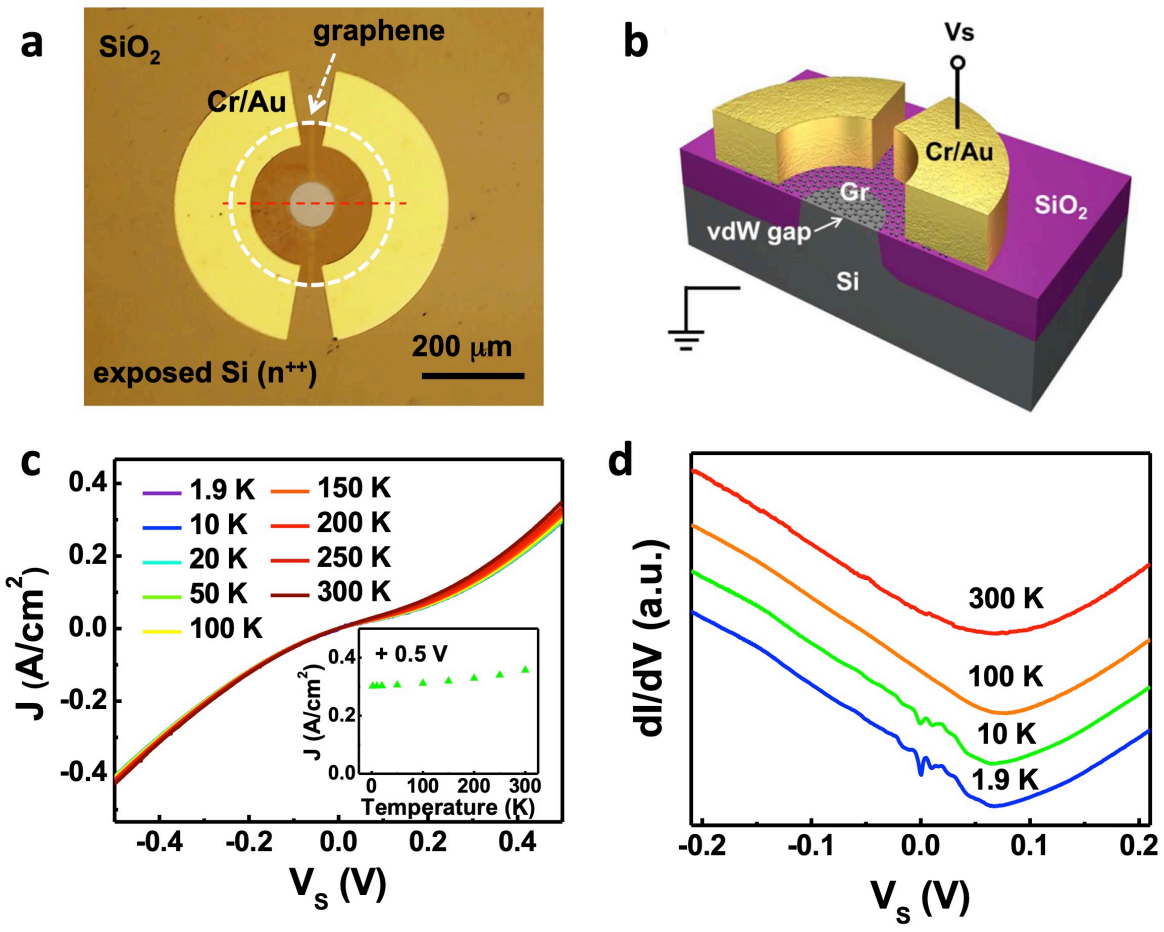


Figure 2-2 "Side-contact" device acting as a control device for studying the vertical tunneling across Gr. **(a)** Optical image of the fabricated "side contact" device. The Gr region is indicated by the white dashed circle. **(b)** Schematic diagram showing the cross section of the "side contact" structure along the direction indicated by the red dashed line in (a) **(c)** J-V characteristics at various temperatures showing little temperature dependence. Inset plots J as a function of temperature at $V_S = 0.5V$. **(d)** 1st order ETS spectrum at various temperatures.

2.2.2 Electrical Characterization of Electron Tunneling across Graphene

The current density−voltage (J−V) characteristics across the Gr vertical structure are shown in **Figure 2-3a** for various temperatures. The curves show some nonlinearity but do not show significant rectification. Thus, the vertical transport across Gr and the accompanying vdW gaps is neither Ohmic nor Schottky but of a tunneling nature. There is a slight asymmetry, a direct consequence of a non-uniform voltage drop across the barrier originating from the electron trapping and quantum capacitance of the Gr layer, as to be discussed in detail later. Note the tunneling current density is 1 order of magnitude larger than that of the "side contact" device. This fact indicates that Gr is almost transparent to electrons and only a small portion of the electrons are reflected or absorbed by the single layer Gr. This is consistent with quantum simulation results of semiconductor−Gr−semiconductor hetero-structures showing that Gr can be treated as a transport barrier with a transmission coefficient dependent on the selected semiconductor material.[58,59] The temperature dependence of the current density is slightly stronger in the vertical tunneling device but the trend is still significantly different from that of thermally activated processes such as transport through Schottky junctions as shown in **Figure 2-3b**. It is found that the current density $J \propto T^2$, characteristic of direct tunneling processes for typical metal−insulator−metal structures.[60,61] Note the sub-nanometer roughness of the Si substrate may slightly increase the barrier thickness; however, it will not affect this discussion significantly. A control sample with Cr/Au directly in contact with the n^{++}-Si was fabricated simultaneously, which yields an Ohmic behavior, further confirming Gr as the origin of the observed tunneling characteristic as shown in **Figure 2-3c**.

Consistent with a direct tunneling process, the first ETS of the vertical structure (**Figure 2-3d**) does not show a clear Dirac cone fingerprint, which is dramatically different from that of the "side contact" device (for the structure, see **Figure 2-1d**), as well as previous studies with vdW materials acting as the counter electrodes.[47–50] Instead, the first ETS shows a consistent minimum dI/dV at zero bias but no other significant feature. There are some weak kinks and bumps, which are barely visible from the second ETS shown in **Figure 2-4**. This observation underscores the fact that the electrons do not interact with the band structure of the Gr significantly during the tunneling process across the Gr, which only acts as a thin tunneling barrier. This is a result of the atomic thickness of Gr, as well as the large momentum mismatch between injected electrons and the Gr band structure, as shown in **Figure 2-3e**, in which the Fermi surface of Si, Gr, and the Au electrode is schematically shown. The momentum of the electrons injected from the valleys near the X point is around 0.98×10^8 cm^{-1}, while Gr exhibits a Fermi momentum of 1.7×10^8 cm^{-1}, and thus a large momentum mismatch (red arrow) is present. The same argument applies to electrons injected from the Cr/Au electrode, which has a transverse momentum ranging from zero to the Fermi momentum of the metal (1.2×10^8 cm^{-1} for Au). As a result, little interaction occurs as the emitted electrons pass through the Gr and are collected by the Cr/Au electrodes; and the collected electrons relax to the available states of the electrodes.

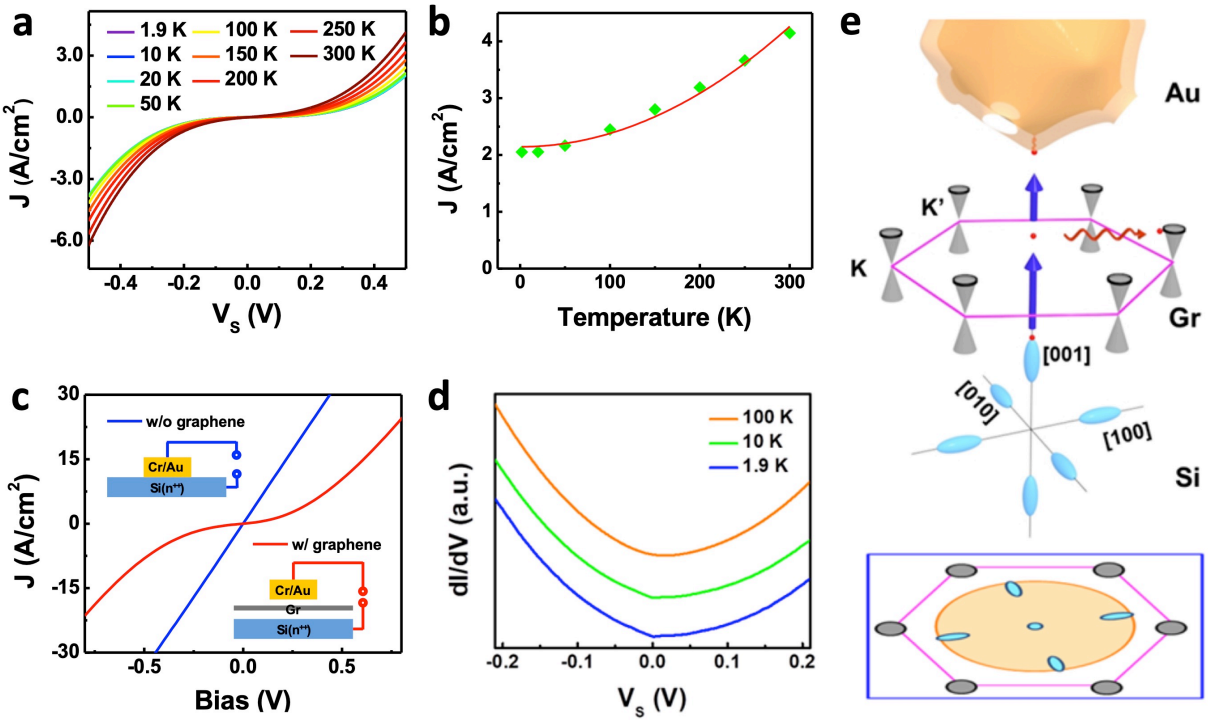


Figure 2-3 Tunneling characteristic through Gr acting as the tunnel medium. **(a)** J−V characteristics at various temperatures. **(b)** J as a function of temperature at $V_S = 0.5V$. Red line shows that fitted result to a metal−insulator−metal tunneling parabolic function. **(c)** Comparison between the J−V characteristics of vertical structure with (red) and without (blue) Gr in the middle. Insets show schematic diagrams of the corresponding structures. **(d)** First order ETS spectrum at various temperatures. **(e)** Schematic diagram showing the Fermi surface of Si (blue ellipses), Gr (black rings in the middle), and the Au electrode of the vertical Gr tunneling structure. Red arrow denote electrons tunneling into Gr with phonon-assistant process.

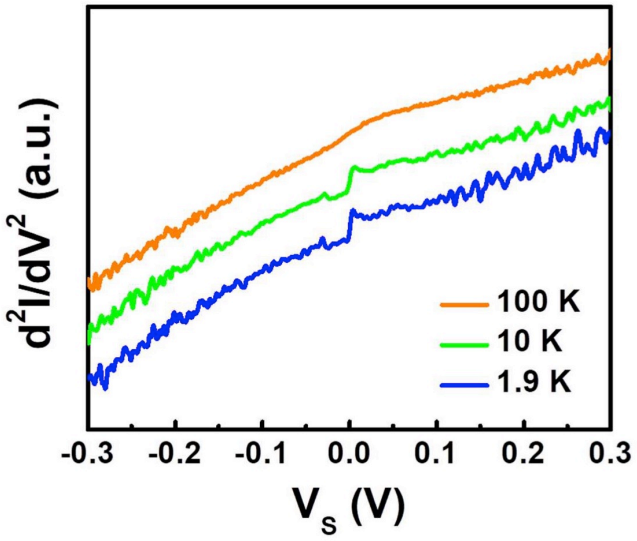


Figure 2-4 2nd order ETS of Gr vertical tunneling structure showing oscillations as a function of bias at various temperatures.

2.2.3 Capacitance Model for Graphene Vertical Tunneling Junction

Although the momentum and energy mismatch prevent quantum interaction between the tunneling electrons and the Gr band structure, the Gr layer can still trap fractions of the tunneling electrons. Because of the low density of states in Gr, the electrical potential of Gr will dramatically change (i.e., the quantum capacitance effect[62,63]) and modify the electrical field configuration across the van der Waals gap. Therefore, the vdW gap serves as the tunneling barrier between silicon and Gr, so a capacitance measurement as a function of voltage will shed light on the modification of Gr on the tunneling process.

The impedance spectroscopy was performed to study this effect in which the frequency response of the resistance and reactance across the gap was measured as shown in **Figure 2-5a**. At low frequencies, the resistance Z′ saturates while the reactance −Z″ tends to zero. As the oscillation frequency is increased, Z′ is reduced toward zero, and a single peak of −Z″ emerges. The Nyquist plot exhibits a single semicircle that passes through the origin of the plot at the high frequency limit (**Figure 2-5b**). This behavior can be readily described by an equivalent circuit consisting of a resistor and a capacitor in parallel (solid curves) and the equivalent circuit is plotted in the **inset of Figure 2-5b**, where C_{Gr} and R_{Gr} represent the capacitance and resistance of the tunneling junction respectively, and C_{Pad} accounts for the capacitance from the surrounding metal contact pads for external circuit connection. The value of R_{Gr} and $C_{total} = C_{Gr} + C_{Pad}$ can be obtained by fitting the frequency response of the reactance for different biases, and the results are given in **Table 2-1**. The decrease of the R_{Gr} with increasing bias is expected for the tunneling dominated (as opposed to leakage dominated) transport behavior. The capacitance of the contact pads, C_{Pad}, can be experimentally extracted by measuring devices

having different areas of the tunnel junction, as shown in **Figure 2-6** and is determined to be 86 pF. It is also found that C_{Pad} is independent of the applied bias in the pad voltage range investigated (**inset of Figure 2-6**). Deducting this contribution from C_{total}, C_{Gr} can be determined. Finally the experimental determined C_{Gr} as a function of the sample bias (V_S) is shown in **Figure 2-5c**.

Distinct from a typical parallel plate capacitor, the capacitance of the Gr vertical tunneling structure is a sensitive function of the bias due to the quantum capacitance. As a result of the atomic thickness of Gr, the quantum capacitance cannot be treated simply as a capacitance in series or parallel connection to the tunneling barrier capacitance. Previous simulation works on Gr base hot electron transistors have taken into account the quantum capacitance of Gr in these vertical devices through the Dirac density of states[64,65] an analytical expression of the influence of the Gr quantum capacitance on the vertical tunneling process is still not readily available. Herein, we construct a new model to describe the capacitance−voltage characteristic of the Gr and the vdW gap in the vertical direction, which takes into account the atomic thickness and linear density of states of Gr, as well as the asymmetrical interfaces on the two sides of Gr. The schematic energy diagram is shown in **Figure 2-5d** for a positive bias. The slight shift of the Fermi level relative to the Dirac point is ignored for simplicity. With V_S, a potential drop, ψ_{gap}, results across the fully preserved vdW gap between the n^{++}-Si interface and the Gr, and charge is induced in the Gr sheet. The limited density of states in the Gr will result in a downward shift of the Gr Fermi level relative to the Dirac point (ψ_{Gr}); this shift is also equal to the voltage drop across the Gr/Cr interface. This is because the Fermi levels of the Gr and Cr are aligned as a result of the orbital hybridization between the two materials,[66] because of the strong interaction

between Gr and chromium, a fully preserved van der Waals gap is not expected to form in between, thus the two materials are expected to share the same Fermi Level due to the strong physical contact and electronic correlation. Another way of looking at the distribution of the voltage drop across the two interfaces is to consider the charge and electric field distributions, as depicted in **Figure 2-5e**. The induced charge is only partially located at the Gr (σ_1), due to its linear density of states, with the rest at the Cr/Au electrode (σ_2), and the sum of which equals the induced charge on the Si electrode ($\sigma = \sigma_1 + \sigma_2$). Thus, the effective electric field at the two interfaces can be defined using the Gauss's Law as

$$E_1 = \frac{\sigma}{\varepsilon_1};\ E_2 = \frac{\sigma}{\varepsilon_2}, \tag{2.1}$$

and the applied sample bias is given by

$$V = \psi_{gap} + \psi_{Gr} = E_1 d_1 + E_1 d_2. \tag{2.2}$$

Taking into account that the charge stored at the Gr sheet is related to ψ_{Gr} through[62]

$$\sigma_1 = e\int_0^{e\psi_{Gr}} f(\varepsilon)\rho_{Gr}(\varepsilon)d\varepsilon, \tag{2.3}$$

in which $f(\varepsilon)$ is the Fermi−Dirac distribution and $\rho_{Gr}(\varepsilon)$ is the density of states of the graphene (per area), C_{Gr} as a function of the sample bias can be obtained by taking the bias dependent potential of Gr into consideration (with the detailed derivation provided in section 2.2.4)

$$C_{Gr} = \frac{d\sigma}{dV} = \frac{\left(\frac{1}{C_1}+\frac{1}{C_2}\right)C_1+1}{\sqrt{\left(\frac{1}{C_1}+\frac{1}{C_2}\right)^2-2\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\times\frac{\xi|V|}{C_1C_2}-\frac{2\xi|V|}{{C_1}^2C_2}}} - C_1, \tag{2.4}$$

where

$$\xi = e^2 \frac{2}{\pi} \frac{e}{(\hbar v_F)^2}, \tag{2.5}$$

in which $C_1 = {}^{\varepsilon_1}/_{d_1}$ and $C_2 = {}^{\varepsilon_2}/_{d_2}$ are the effective geometric capacitances of the Si/Gr and the Gr/Cr interfaces, respectively. The experimental data in **Figure 2-5c** can be readily fitted to this expression, shown as the red curve, except for discrepancies near the zero bias, which has been observed and attributed to charge impurities in the Gr sheet by previous works.[63,67,68] The fitted C_1 is found to be significantly smaller than C_1, characteristic of a full vdW gap at the Si/graphene interface and an almost disappearing vdW gap at the Cr/graphene interface, respectively. This asymmetry in the two interfaces, together with the quantum capacitance of the Gr, is the physical origin of the asymmetric nature of the tunneling J−V characteristic discussed earlier. This is the first model, to the best of our knowledge, which provides the influences of quantum capacitance on the vertical transport across Gr in an analytical expression, which simultaneously takes into account the atomic thickness of Gr and the Gr-metal/semiconductor interface.

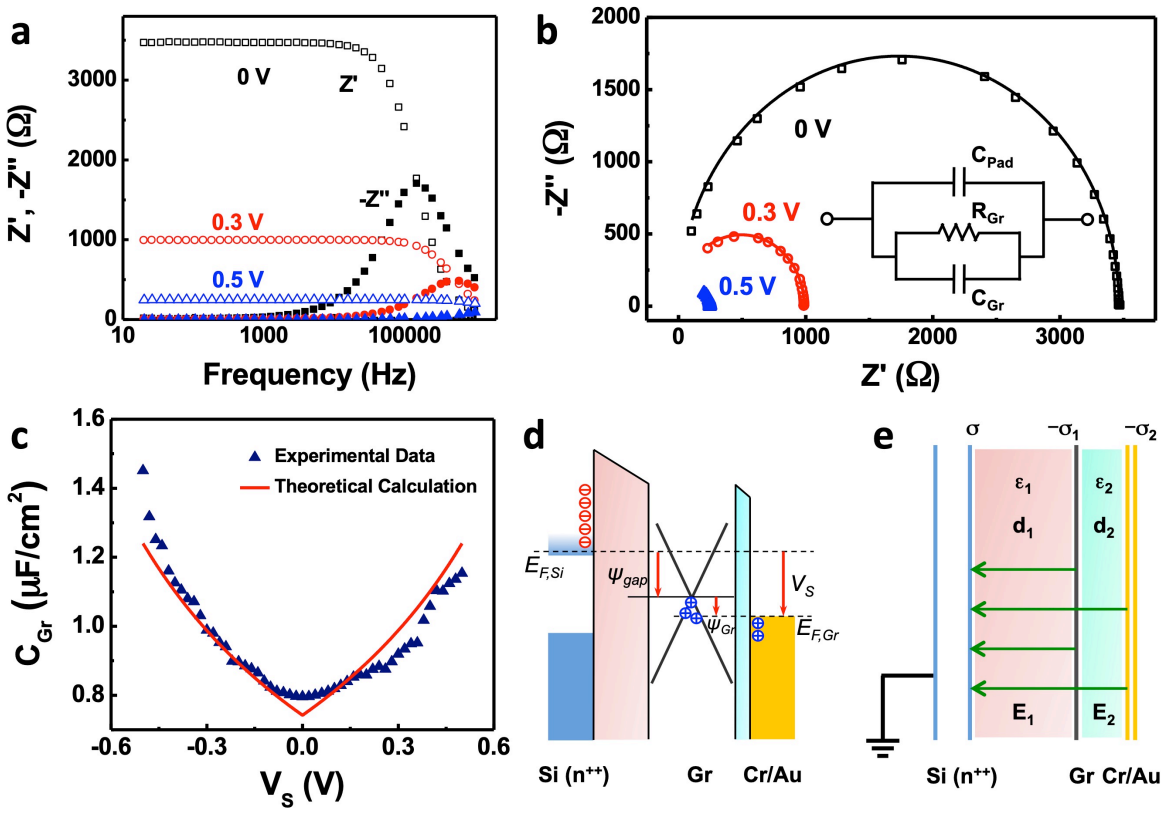


Figure 2-5 Capacitance measurement of the Gr vertical structure. **(a)** Resistance (Z') and reactance ($-Z''$) as a function of frequency for various applied sample biases. **(b)** Nyquist plot showing $-Z''$ versus Z' for various applied sample biases. Inset shows the proposed equivalent circuit of the Gr vertical structure, in which a resistor, R_{Gr}, and a capacitor, C_{Gr}, connected in parallel are used to describe the tunnel junction, while C_{Pad} accounts for the capacitance of the contact pads. **(c)** Experimental data of C_{Gr} as a function of the applied sample bias (blue triangles) plotted alongside with the theoretically calculated curve (red solid line). **(d)** Schematics of the band diagram of the Gr vertical structure, depicting the effect of Gr's limited density of states. **(e)** Schematic diagram of the Gr vertical tunneling junction showing the charge stored on the Si electrode (σ), the graphene single layer (σ_1) as well as on the Cr electrode (σ_2). The green arrows represent electric field lines.

Applied Bias (V)	R_{Gr} (Ω)	C_{total} (pF)	C_{Gr} (pF)
0	3428	306	220
0.3	968.4	317	231
0.5	219.0	385	299

Table 2-1 Summary of the values of R_{Gr}, C_{total} and C_{Gr} at various sample biases for a tunnel junction area of 1.2×10^{-4} cm^2.

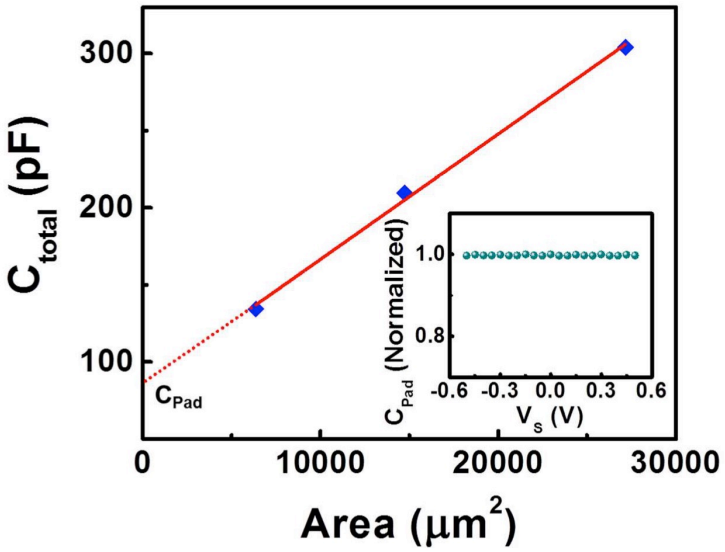


Figure 2-6 The measured parallel capacitance ($C_{total} = C_{Gr} + C_{Pad}$) as a function of the area of the graphene tunnel junction. Inset shows normalized C_{Pad} as a function of the applied DC bias.

2.2.4 Theoretical Calculation for Graphene Vertical Tunneling Structure

When a bias voltage V is applied across the Gr vertical tunneling structure, charges are accumulated on the n^{++}-Si electrode, Gr, as well as the Cr/Au electrode, and the charge area densities are denoted by σ, σ_1 and σ_2 respectively. Charge neutrality requires that $\sigma = \sigma_1 + \sigma_2$. The electric field across the gap between n^{++}-Si and Gr can be determined using the Gauss's Law, and the voltage drop, ψ_{gap} can be subsequently obtained as:

$$\psi_{gap} = E_1 d_1 = \frac{\sigma}{\varepsilon_1} d_1, \tag{2.6}$$

in which d_1 and ε_1 represent the effective thickness and permittivity of the vdW gap between n^{++}-Si and Gr. The interface between Gr and the Cr/Au electrode can be similarly described, with the voltage drop equals to:

$$\psi_{Gr} = E_2 d_2 = \frac{\sigma_2}{\varepsilon_2} d_2 = \frac{(\sigma - \sigma_1)}{\varepsilon_2} d_2 \tag{2.7}$$

with d_2 and ε_2 representing the effective thickness and permittivity of the hybridized Gr/Cr interface. The charge area density on Gr, σ_1, can be obtained by integrating the density of states of graphene over the range of 0 to $e\psi_{Gr}$:

$$\sigma_1 = e \int_0^{e\psi_{Gr}} f(\varepsilon) \rho_{Gr}(\varepsilon) d\varepsilon = \frac{1}{2} \xi {\psi_{Gr}}^2, \tag{2.8}$$

where

$$\xi = e^2 \frac{2}{\pi} \frac{e}{(\hbar v_F)^2}. \tag{2.9}$$

Note that several approximations are made in obtaining this expression. First, the inherent p-doping of Gr is ignored since the Dirac point has been experimentally determined to be very close to the Fermi level of the Gr. Secondly, the Fermi levels of the Gr and the Cr electrode line up because of the hybridization between the two materials. Finally, a step-like Fermi-Dirac distribution is assumed. In this expression, $\hbar$ is the reduced plank constant, v_F is the Fermi velocity of the Gr, and ψ_{Gr} is the Fermi level change in Gr relative to the Dirac point.

The applied voltage equals the voltage drop across the Si/Gr interface plus that across the Gr/Cr interface:

$$|V| = \psi_{gap} + \psi_{Gr} = \frac{\sigma d_1}{\varepsilon_1} + \frac{\sigma d_2}{\varepsilon_2} - \frac{\xi d_2}{2\varepsilon_2}\left(|V| - \frac{\sigma d_1}{\varepsilon_1}\right)^2 \tag{2.10}$$

$$= \frac{\sigma}{C_1} + \frac{\sigma}{C_2} - \frac{\xi}{2C_2}\left(|V| - \frac{\sigma}{C_1}\right)^2 \tag{2.11}$$

C_1 and C_2 are introduced to simplify our expression, and correspond to the effective geometric capacitances of the two interfaces. Solving for $\sigma(V)$ results in:

$$\sigma(V) = \frac{{C_1}^2 C_2}{\beta}\left\{\frac{1}{C_1} + \frac{1}{C_2} - \frac{\xi|V|}{C_1 C_2} + \sqrt{\left(\frac{1}{C_1} + \frac{1}{C_2}\right)^2 - 2\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\frac{\xi|V|}{C_1 C_2} - \frac{2\xi|V|}{{C_1}^2 C_2}}\right\} \tag{2.12}$$

and the expression for the capacitance across the entire Gr vertical tunneling structure can be obtained:

$$C_{Gr} = \frac{d\sigma}{dV} = \frac{\left(\frac{1}{C_1}+\frac{1}{C_2}\right)C_1 + 1}{\sqrt{\left(\frac{1}{C_1}+\frac{1}{C_2}\right)^2 - 2\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\frac{\xi|V|}{C_1 C_2} - \frac{2\xi|V|}{{C_1}^2 C_2}}} - C_1. \tag{2.13}$$

As shown in **Figure 2-5c**, the experimental data can be fitted to this expression using C_1 and C_2 as the fitting parameters, with $C_1 = 0.747\ \mu F/cm^2$ and $C_2 = 107\ \mu F/cm^2$.

2.3 Summary

In summary, we systematically studied the vertical transport into and across vdW materials using Gr as a model system. It is found that when lateral transport was eliminated in a purely vertical transport, the tunneling electrons interacted weakly with the semimetallic Gr plane due to the atomic thickness, as well as the mismatch of the transverse momentum. Instead, the Gr acts as a very thin grid and is transparent to vertically tunneling charge carriers, meanwhile, it can still modulate the potential and charge distribution across the tunneling barrier via the quantum capacitance effect and thus control the tunneling current. Our study highlights, the potential of Gr for use as an electron/spin tunneling barrier for high frequency electronics and spintronics. It can also open new avenues for the design and analysis of 2D material hetero-structures as well as 2D/bulk material hetero-structures.

2.4 Experimental Methods

Monolayer Gr is grown on copper foils using CVD. For both the side contact and the vertical tunneling structures, a ⟨100⟩ n^{++}-Si substrate with a dopant concentration of 10^{19} cm^{-3} is used as the substrate and as the contact electrode, and a 300 nm field oxide is deposited using the Local Oxidation of Silicon (LOCOS) process around each contact region to define the injection area and isolate individual devices. The Si substrate is subsequently treated with HF, immediately followed by the wet transfer of the Gr. The monolayer Gr is etched into many disks with a diameter slightly larger than the contact region using oxygen plasma, followed by photolithography and e-beam evaporation of the side and top contacts (Cr/Au 10/ 100 nm).

The temperature-dependent J−V characteristics and ETS spectra are measured in a physical properties measurement system (PPMS, Quantum Design, Inc.). To directly measure the first and second derivatives of current as a function of the applied voltage, an ac voltage with a dc offset is applied to the device under test using a function generator (Agilent 3250). The amplitude of the ac oscillation is set to 2 mV. The current signal for the device is converted to a voltage signal using a current preamplifier (SR570) and fed into two lock-in amplifiers (SR 830) to measure the first and second derivatives simultaneously. The impedance spectroscopy data is collected in room temperature using an Agilent 4284A Precision LCR meter with the oscillation amplitude set to 10 mV.

Chapter 3 Interfacial States and Fano-Feshbach Resonance in Graphene-Silicon Vertical Junction

(This chapter is based on the publication, *Nano Letters 2019, 19, 6765-6771*)

Interfacial quantum states are drawing tremendous attention recently, because of their importance in design of low-dimensional quantum hetero-structures with desired charge, spin or topological properties. Although most of studies of the interfacial exchange interactions mainly performed across the interface vertically, the lateral transport nowadays is still a major experimental method to probe these interactions indirectly. In this report, we fabricated a graphene and hydrogen passivated silicon interface to study the interfacial exchange processes. For the first time we found and confirmed a novel interfacial quantum state, which is specific to the 2D-3D interface. The vertically propagating electrons from silicon to graphene results in electron oscillation states at the 2D-3D interface. A harmonic oscillator model is used to explain this interfacial state. In addition, the interaction between this interfacial state (discrete energy spectrum) and the lateral band structure of graphene (continuous energy spectrum) result in Fano-Feshbach resonance. Our results show that the conventional description of interfacial interaction in low-dimensional systems is valid only in considering the lateral band structure and its density-of-states and is incomplete for the ease of vertical transport. Our experimental observation and theoretical explanation provide more insightful understanding on various interfacial effects in low-dimensional materials, such as proximity effect, quantum tunneling, etc. More important, the Fano-Feshbach resonance may be used to realize all solid-state and scalable quantum interferometer.

3.1 Motivation

Interfacial states and interactions have a strong influence on intrinsic properties of 2D materials and related quantum materials. For example, substrate selection directly determines the mobility of 2D materials.[27,69,70] Interface proximity effects in the hetero-structures composed of 2D materials, topological insulators and superconductors have been applied to construct various novel quantum states for the applications such as spintronic memory,[71] quantum logic operation,[72] etc. Because of the significant impacts of the interfacial states on material designs and applications in spintronic devices, quantum computing, and high-performance memories, relevant research is receiving a great deal of attention recently. Currently, lateral transport measurements are the major approaches to probe interface interactions, and lateral band structure and transport theories are the main vehicles to analyze experimental observations. However, lateral transport studies can only help us to speculate the vertical exchange in an indirect way. Conclusions from lateral transport studies might be incomplete, even misleading. Thus, vertical transport measurements are critical for us to build a solid and clear picture for understanding these interfacial interactions.

Vertical transport devices with tunneling processes through the vdW gap in 2D materials, which are widely used to design novel quantum devices, such as spin filter,[42,73] atomically thin flexible memory,[74,75] Josephson junctions,[76,77] etc. In all cases, vertically distributed quantum states, or interfacial states, may play a more important role than lateral band structure, although they have been generally ignored. Thus, a deep understanding of vertical quantum states and transport in 2D materials are essential for diverse application of reduced dimensional systems.

Targeting at above objectives, in this work, we study the vertical tunneling process through a vdW gap on a Gr-Si (n^{++} doped) interface, and demonstrate a set of new quantum state specific to the 2D-3D interface. These states are featured by a group of evenly distributed peaks in the tunnelling spectra due to quantum oscillation of tunneling electrons. The discrete vertical interfacial quantum oscillation state can also interfere with the lateral Dirac band structure in Gr layer and result in Fano-Feshbach resonance (FFR).[78] Our discovery indicates that the vertical transport in low-dimensional systems, especially in 2D-3D junctions, are dominantly determined by vertical interfacial quantum states, instead of the intrinsic lateral band structure of Gr. This finding may change our conventional intuition that the tunneling spectrum mainly conveys the information on the intrinsic band structure. It also establishes a more completed and insightful picture to understand the interfacial exchange and coupling processes in 2D and quantum materials, for novel quantum device design and fabrication. Furthermore, we observe FFR resulted from the interfacial and lateral states, and this observation may inspire us with a novel architecture to build a scalable solid-state quantum interferometer.

3.2 Result and Discussion

3.2.1 Clue for Silicon-Graphene Interfacial States

The device configuration applied in our study is shown in **Figure 3-1a**. A heavily n-type doped (n^{++}) Si substrate was thermally oxidized to form a SiO_2 layer for insulation. A round Si working area with a diameter of 90 μm was masked to prevent the oxidation. After polish and hydrogen fluoride acid treatment, the Si working area formed a flat and hydrogen terminated surface. A single layer of Gr was then transferred onto this working area to form a Gr-Si tunneling junction, in which the vdW gap between Si and Gr serves as the tunneling barrier. To prevent the formation of native SiO_2 layer on Si, after the polymer/Gr stack was transferred onto the hydrogen passivated Si surface with a standard wet transfer technique, they were immediately moved to a dry inner gas environment. After removing the polymer carrier, the structure was deposited with very thin aluminum layer, which was quickly oxidized into a layer of Al_2O_3 to protect the Si/Gr interface. All these steps promise that the vdW gap instead of SiO_2 serves as the tunneling barrier, and hence the scattering and trap assisted tunneling through SiO_2 was not taken into consideration in our analysis. **Figure 3-1b** shows the top-view of the as-fabricated tunneling structure.

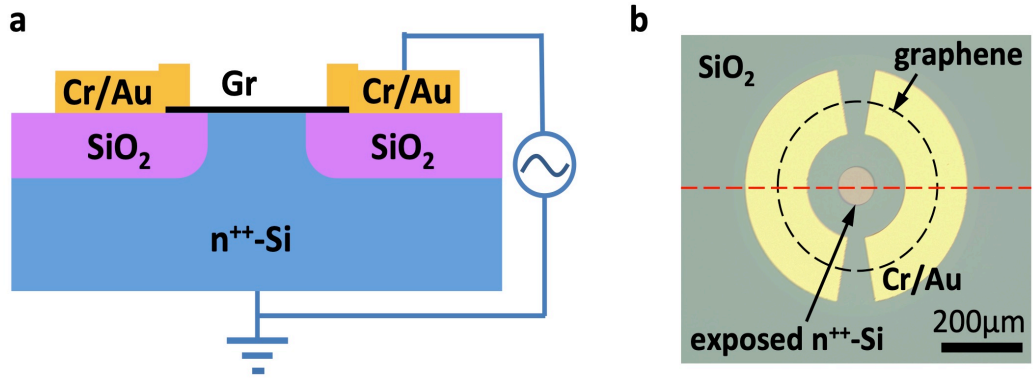


Figure 3-1 Gr-Si tunneling hetero-structure. **(a)** The side-view schematic of the Gr-Si tunneling structure. A modulated signal is applied between silicon and Gr layer to probe IV and tunneling spectroscopy on the Gr-Si junction. **(b)** The top-view of the optical image of the Gr-Si tunneling structure. The black dashed circle labels the area with Gr coverage. The red dashed line indicates the position where the side-view schematic presents.

Temperature-dependent I-V measurements were then performed on the as-fabricated Gr-Si junction, as plotted in **Figure 3-2a**. All the I-V curves show the feature of nonlinearity with little temperature dependence, indicating that the contact on the Gr-Si interface is dominated by tunneling process and that the possibility of forming a Schottky contact is excluded. The I-V curves are not symmetric about zero bias point, because Fermi level of the Gr layer is not exactly at the Dirac point. **Figure 3-2a** lower inset shows the first order derivative of the I-V curve at 150 K, from which the position of the Dirac point is determined to be around 0.03 V above the Fermi level, i.e. the Gr layer is slightly p-doped. **Figure 3-2a** upper inset illustrates the band alignment of the Gr-Si junction at 150K.

In contrast, as the temperature decreases below 80K, the I-V behavior cannot be explained by conventional Dirac cone picture anymore. **Figure 3-2b** shows the zoomed I-V curves around zero bias point, and several plateaus can be clearly distinguished. As discussed in a previous

work,[79] lateral momentum mismatch between Gr and silicon has to be considered in the tunneling process at low temperature, and in this case phonon assisted process, which offers to compensate the lateral momentum mismatch, must be taken into consideration. Nevertheless, under low tunneling bias, the lateral momentum mismatch has to be compensated by phonons with momentum near the boundary of the Brillouin zone, whose modes are hard to be excited at low temperature. As a result, tunneling current near the zero bias point will drop drastically and band structure of Gr cannot be observed. This picture can only explain the "pseudo-gap" feature of the Gr but not the multiple plateaus in our observation.

To further investigate tunneling behavior of the Gr-Si junction, electron tunneling spectroscopy measurement was performed, and the results are plotted in **Figure 3-2c**. As discussed above, the "pseudo-gap" feature due to the lack of phonon momentum compensation is confirmed from the tunneling spectrum at 5 K. Besides, the tunneling spectrum is featured by an additional group of peaks. These peaks are equally separated from each other, as shown in **Figure 3-2d**, which illustrates a linear dependence between the peak order and tunneling bias (Note that the slopes at forward and reverse biases are different due to the asymmetry of this Gr-Si system). This linear dependence feature has similarity to magnetic field induced Landau levels, but with a significant different sign. Due to the effective massless Fermion energy dispersion in Gr, Landau level near the Dirac cone follows the relationship of $E_n = \hbar\omega^{Dirac} sgn(n)\sqrt{|n|}$,[80] where n is index for the nth Landau level, $\omega^{Dirac} = v_F\sqrt{2eB/\hbar}$, and e is electron charge; instead, our observation has a linear dependence ($E_n \propto n$). Therefore, in order to explain this new experimental observation and clarify the physical origin, we construct a 3D-2D system interface model discussed below.

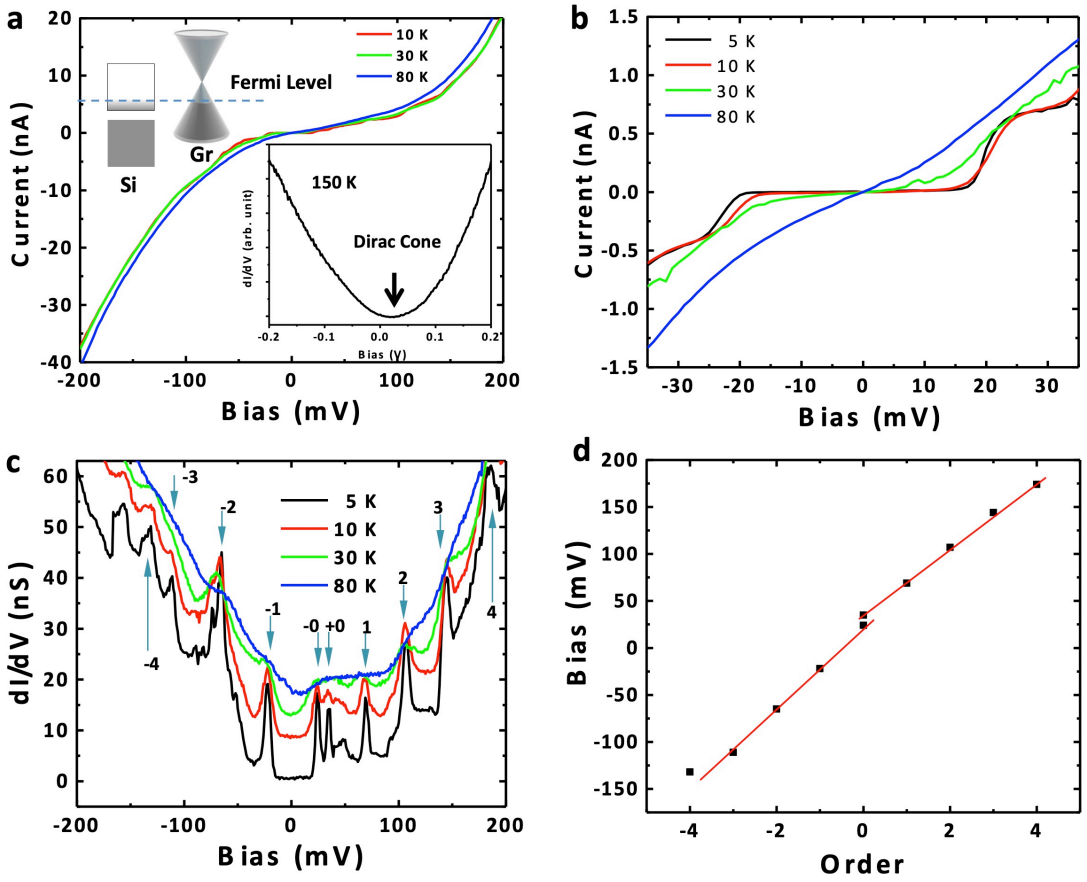


Figure 3-2 Vertical transport and tunneling spectroscopy characterization on the Gr-Si junction. **(a)** The IV curves of the junction at 10 K (red), 30 K (green) and 80 K (blue). Upper inset shows the band alignment between heavily doped n-type silicon and Gr. Lower inset shows the 1st order differentiation of IV curve at 150 K. **(b)** The zoomed-in IV curves around zero bias voltage at 5 K (black), 10 K (red), 30 K (green) and 80 K (blue). **(c)** The 1st order tunneling spectroscopy of the Gr-Si tunneling junction with temperature of 5 K (black), 10 K (red), 30 K (green) and 80 K (blue). **(d)** The linear dependence of the tunneling peak order to the tunneling bias voltage.

3.2.2 Proposed 3D-2D Interface Model

First, driven by the tunneling bias, electrons are emitted from the 3D semiconductor (silicon in our case), and move to the 2D layer. As discussed in our previous work,[79] lateral momentum mismatch makes the 2D atomic layer nearly transparent to the vertically propagating electrons. Thus, in a classical point of view, the electrons will penetrate the 2D layer and keep moving forward. After passing through the 2D layer, electrons will be decelerated and then reflect backward to the 2D layer again. From the viewpoint of quantum mechanics, the tunneling bias will create a potential well at the 3D-2D interface. From our experimental observation, a harmonic oscillator potential is a good initial approximation to describe this interfacial state, as shown in **Figure 3-3a**. The separation between each two neighboring peaks in **Figure 3-2c** and **Figure 3-2d** is 0.04 eV. Then the width of the ground state wave function (Gaussian function) is determined to be 1.2 nm. (Considering the electrons are trapped on the Gr-Si interface, i.e. the van der Waals gap, the free electron mass is used here to simplify the calculation.) This value agrees very well with the intrinsic single layered Gr thickness (~0.7 nm), indicating the sound rational of our interfacial state model. Therefore, due to the large lateral momentum mismatch between Gr and silicon, our model suggests two pathways for tunneling electrons to propagate from silicon to Gr: (1) directly enter into Gr lateral energy band with momentum compensation from phonon scattering; (2) be trapped in the interfacial states and then go into Gr layer (see **Figure 3-3b**).

When it comes to interface states at silicon surface, research on that using metal/oxide/silicon tunneling structure has been intensively studied since around 50 years ago. We can microscopically think of our Gr-Si junction as Gr/vdW gap/Si, and analogize the 2D-3D interfacial trap states we proposed here to those in conventional 3D-3D metal/oxide/silicon

systems.[81,82] The interface states in both cases share a similar function, and are able to serve as intermediate states and assist the carrier in moving from silicon to the conductive materials; the difference we would like to emphasize is in the conductive material side: our 2D Gr and their 3D metals. 3D metal would have more available states with various wavevectors for propagating carriers, while our 2D Gr has only states with in-plane wavevector allowed for tunneling electrons. Besides, as stated in a previous report,[79] majority of vertically tunneling electrons would not go into Gr lateral band through phonon-assisted process. Hence, according to our model, they would enter into the interfacial trap states and then release to Gr.

The other important point deducted from our model is the interference between the interfacial quantum states and Gr lateral band structure. The quantum trap state is a pure interfacial effect in the 2D-3D junction, and the wave function cannot be constructed by the linear combination of the eigenstates of the 3D material or the 2D material. Specific to our case, the trap state wave function cannot be established by the eigenfunctions of the silicon band structure or the Gr Dirac cone, i.e. the interfacial trap states (which are discrete quantum states) are orthogonal to the Gr band structure (which is continuous quantum states). However, the overlap of these quantum states in the energy spectrum will lead to FFR,[78] which is a quantum resonance due to the interference between two possible quantum processes as shown in **Figure 3-3b**. The electrons can directly tunnel into the Gr layer with help from phonon, or get trapped by the interfacial states and then relax to the Gr lateral Dirac band. The interference between these two routes gives the peak profile of the FFR as described by:

$$\sigma_n(\varepsilon) = \frac{(q+\frac{\varepsilon-E_n}{\Gamma})^2}{1+(\frac{\varepsilon-E_n}{\Gamma})^2}, \tag{3.1}$$

where ε is electron energy, E_n is resonance energy of the n^{th} energy level , Γ is resonance peak width, and q is a parameter determines the asymmetry of the resonance peak. It is noteworthy that the reciprocal of Γ is proportional to the lifetime of the interfacial state, and the relation is:

$$\Gamma = \left(\frac{1}{\tau}\right) \cdot \frac{h}{4\pi}, \tag{3.2}$$

where h is Plank constant.[19] From the peak profile delineated in the **Equation (3.1)**, constructive interference corresponds to resonant enhancement of the transmission, whereas destructive interference is related to resonant suppression. In our case, the parameter of q can be approximately expressed as:

$$q \approx \alpha \frac{\tau_i}{\tau_g}, \tag{3.3}$$

where τ_i is tunneling rate through the discrete interfacial states, and τ_g is tunneling rate to the continuous graphene energy band, and α is a constant. Considering that the tunneling rate to the Gr band is proportional to density-of-states of Gr which linearly increases as a function of tunneling bias, the tunnelling spectrum can be simulated and demonstrated in **Fig 3-3c**. The detailed deduction and simulation processes will be presented in the next paragraph.

With the single FFR peak shape provided by **Equation (3.1), (3.2) and (3.3)**, we assume that the tunneling rates to each of the energy levels of the interfacial trap state are the same ($\tau_i = A$), and the tunneling rate to the Gr is proportional to the density-of-states which linear depends on the tunneling bias ($\tau_g = B\varepsilon$), the Equation (6) can be expresses as

$$q \approx \alpha \frac{A}{B\varepsilon} = \frac{\beta}{\varepsilon}, \tag{3.4}$$

where A is a constant with a unit of time representing the tunneling rate through the discrete interfacial states, B is the coefficient for graphene tunneling rate linear dependence, and $\beta \equiv \frac{\alpha A}{B}$. With combining **Equation (3.4)** and **Equation (3.1)**, we get **Equation (3.5)**:

$$\sigma_n(\varepsilon) = \frac{(\frac{\beta}{\varepsilon}+\frac{\varepsilon-E_n}{\Gamma})^2}{1+(\frac{\varepsilon-E_n}{\Gamma})^2}. \tag{3.5}$$

Combining all the resonant peaks corresponding to the discrete energy levels of the interfacial states and the linear baseline due to the direct tunneling to Gr, the entire spectrum can be described as

$$\sigma(\varepsilon) = \sum_n \frac{(\frac{\beta}{\varepsilon}+\frac{\varepsilon-E_n}{\Gamma})^2}{1+(\frac{\varepsilon-E_n}{\Gamma})^2} + \gamma\varepsilon, \tag{3.6}$$

where β, Γ and γ can be determined by fitting the experimental spectrum, and the reciprocal of Γ is proportional to the lifetime of the interfacial state ($\Gamma = \left(\frac{1}{\tau}\right) \cdot \frac{h}{4\pi}$, where h is Plank constant). It is worth noting that we do not consider the lateral momentum mismatch and phonon scattering near zero bias, so the simulation does not show the pseudo-gap feature observed in the experimental tunneling spectra (Compare **Figure 3-3c** and **Figure 3-3d**).

It can be found that the simulation shares two most important features in common with our experimental observations. First, the shape of the resonant peak becomes more and more asymmetric as the tunneling bias increases. This is because the linearly increasing density of states in Gr makes the q factor smaller for higher tunneling biases, resulting in a more asymmetric peak profile. The second feature is the obvious dips next to the tunneling peaks. These two features are both observed in our tunneling spectra, which strongly support our picture

of the interfacial quantum state in 2D-3D junction. By fitting the tunneling peak, the lifetime of the interfacial trap state is determined to be around 1 ps, as shown in **Figure 3-3d**.

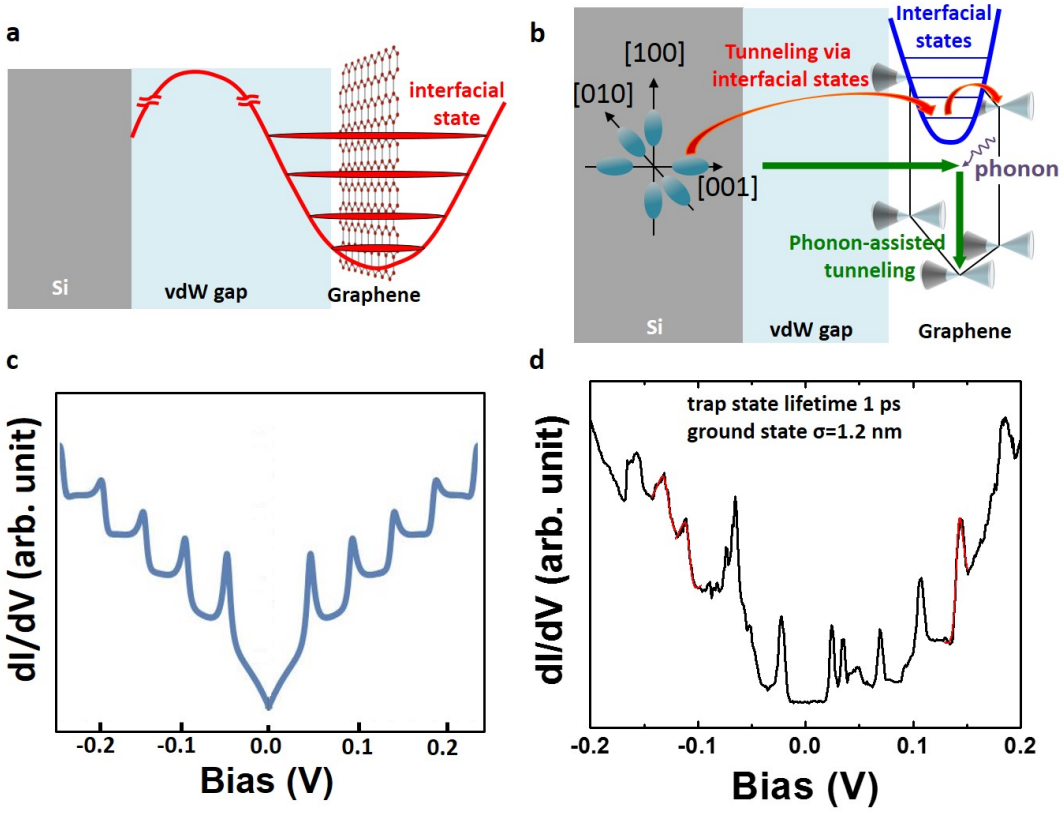


Figure 3-3 The interfacial quantum state and FFR on Gr-Si interface. **(a)** The spatial structure of the Gr-Si tunneling hetero-structure depicting the effect of vdW gap barrier and the illustration of induced interfacial trap states. **(b)** There are two possible tunneling routes between Gr and Si, phonon-assisted tunneling and interfacial state mediated tunneling. The interaction between these two possible routes results in FFR. **(c)** The simulation of the tunneling spectrum considering the FFR, featured by asymmetric peaks and dips. **(d)** The Fano-Feshbach fitting on the experimental observation illustrates a ground state with spatial dimension of 1.2 nm (full width at half maximum (σ) of Gaussian distribution) and a lifetime of 1 ps.

3.2.3 Exclusion of Magnetic Field Induced Discrete Landau Levels

Although we pointed out that the peaks appeared in our tunneling spectrum have linear dependence, which is different from those resulting from Landau levels, it is still necessary to exclude this possibility via more solid experimental evidence. If our observation was due to the Landau levels, there would be two possible origins: (1) the hydrogen-passivated Si surface might result in hydrogen adsorption on Gr surface, which is magnetic;[83] (2) the Si/SiO_2 boundary will build up strain at low-temperatures due to the difference in thermal expansion efficiencies between Si and SiO_2, and this strain may result in pseudo-magnetic field in the Gr.[84–86]

To exclude these possibilities, tunneling spectroscopy was performed under different magnetic fields at temperature of 2.5K. **Figure 3-4a** and **Figure 3-4b** show the 1st order and 2nd tunneling spectra, which show no peak shifting or splitting under different external magnetic fields. If the peaks were resulted from spontaneous magnetization, the superposition between the external magnetic field and intrinsic magnetization would result in peak shifting, which was never observed in our experiment. Shift due to the superposition between the externally applied magnetic field and pseudo-field can be derived and understood from the following considerations.

The Hamiltonians near the K and K' points of Gr under external magnetic field can be expressed as:

$$\begin{cases} H_K = v_F \boldsymbol{\sigma} \cdot (\boldsymbol{p} - e\boldsymbol{A}) \\ H_{K'} = v_F \boldsymbol{\sigma}' \cdot (\boldsymbol{p} - e\boldsymbol{A})' \end{cases} \tag{3.7}$$

where v_F is electron Fermi speed; $\boldsymbol{\sigma}$ and $\boldsymbol{\sigma'}$ are Pauli matrices for the K and K' point respectively; $\boldsymbol{p}$ is electron momentum; $\boldsymbol{A}$ is magnetic vector potential. The Hamiltonians near the K and K' points of graphene with a strain-induced pseudo-field can be expressed as:

$$\begin{cases} H_K = v_F \boldsymbol{\sigma} \cdot (\boldsymbol{p} - \boldsymbol{A_s}) \\ H_{K'} = v_F \boldsymbol{\sigma'} \cdot (\boldsymbol{p} + \boldsymbol{A_s}) \end{cases}, \tag{3.8}$$

where $\boldsymbol{A_s}$ corresponds to magnetic vector gauge field related to pseudo-magnetic field. Then the superposition between the external magnetic field and pseudo-field becomes the following form:

$$\begin{cases} H_K = v_F \boldsymbol{\sigma} \cdot (\boldsymbol{p} - e\boldsymbol{A} - \boldsymbol{A_s}) \\ H_{K'} = v_F \boldsymbol{\sigma'} \cdot (\boldsymbol{p} - e\boldsymbol{A} + \boldsymbol{A_s}) \end{cases}. \tag{3.9}$$

It is obvious that the superposition has opposite effects on K and K' electrons. The external magnetic field will increase the Landau energy spacing for K valley and, meanwhile, reduce the separation for K' valley, i.e. the pseudo-field induced Landau levels should experience splitting with external field applied. However, this effect is not observed in our experiment, indicating that the peaks observed under finite fields do not correspond to pure Dirac Fermions. Specifically, in **Figure 3-4a**, the peak energy separation in zero external field is corresponding to a pseudo-magnetic field of ~2.1 Tesla, which is smaller than the externally applied fields; hence, the external magnetic fields should have dominated and led to peak splitting. Obviously, none of the peaks associated the tunneling spectra in external fields undergo the splitting.

To further exclude the abovementioned possibility of magnetism induced by hydrogen adsorption, lateral transport measurement and selective area tunneling study were designed and performed respectively. A Hall bar structure was fabricated on a Gr layer transferred onto intrinsic silicon with hydrogen passivation, as shown in **Figure 3-4c** inset. Also in **Figure 3-4c**,

measurement setup is labeled, and the measurement was carried out at low temperature of 2.5K. An alternative current source (I_{ac}) was applied along the long arm, and longitudinal (R_{xx}) and transverse (R_{xy}) resistances were obtained through the longitudinal and transverse voltage read by voltmeters, V_{xx} and V_{xy}, and transformation by dividing I_{ac}. Thus, we can probe the possibility of spontaneous magnetization originating from the interface, e.g. hydrogen adsorption. The magneto-resistance curve (black) of the as-fabricated Hall bar shown in **Figure 3-4c** has no hysteresis feature, and, in the meantime, no anomalous Hall effect is observed in the Hall measurement (red). Both of these observations exclude the possibility of spontaneous magnetization.

A selective area tunneling device including a top contact in Si region and a side contact in SiO_2 region was fabricated to study the possibility of pseudo-field induced Landau levels. As discussed above, the strain built on the Si/SiO_2 boundary during the cooling process can result in pseudo-field in Gr layer. Thus, by comparing the tunneling spectrum in Si region to that from side contact in SiO_2 region, more insightful information on the origin of the peaks is provided. **Figure 3-4d** inset illustrates the schematic and optical image of a selective area tunneling device, and **Figure 3-5** shows a clearer top-view picture and a cartoon cross-section illustration. **Figure 3-4d** shows the tunneling spectra collected from the inner electrode (black) and outer electrode (blue), and the tunneling spectrum collected from the inner electrode shows a stronger peak feature than that from the outer electrode, indicating that the Si/SiO_2 boundary and the strain built on it is not the origin of the tunneling peaks, since only the electrons passing through the Si/SiO_2 boundary and being collected by the outer electrodes would experience the boundary strain but not the inner one.

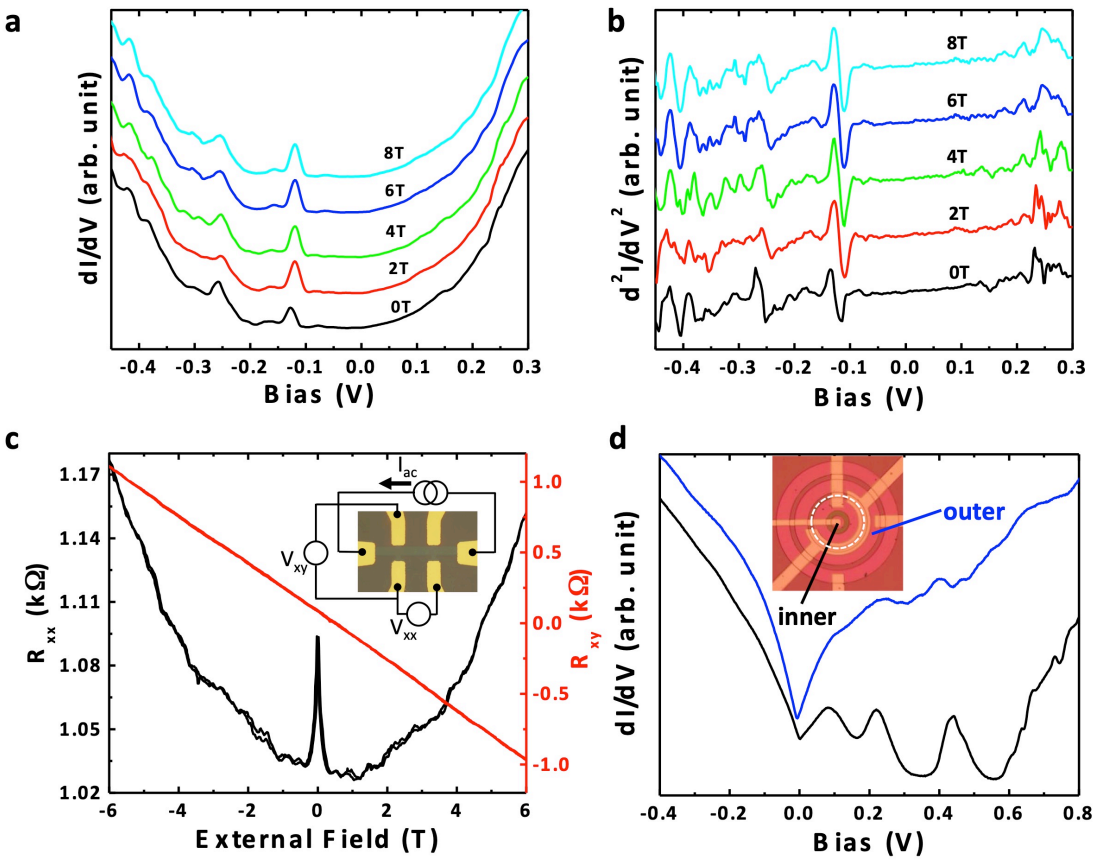


Figure 3-4 Low-temperature (2.5K) experiments excluding the possibilities of Landau levels arising from spontaneous magnetization or strain-induced pseudo-field. **(a)** The 1st order tunneling spectra of the Gr-Si tunneling junction. **(b)** 2nd order tunneling spectra of the Gr-Si tunneling junction. The magnitudes of applied magnetic fields are labeled next to each line. **(c)** The lateral transport measurement on a Hall bar structure fabricated on Gr-Si hetero-structure. Experimental setup is shown in the inset. **(d)** The selected area tunneling spectra collected from the electrode inside the silicon working area (black) and outside the working area (red). The inset shows the device structure, and the white dashed line labels the Si/SiO_2 boundary.

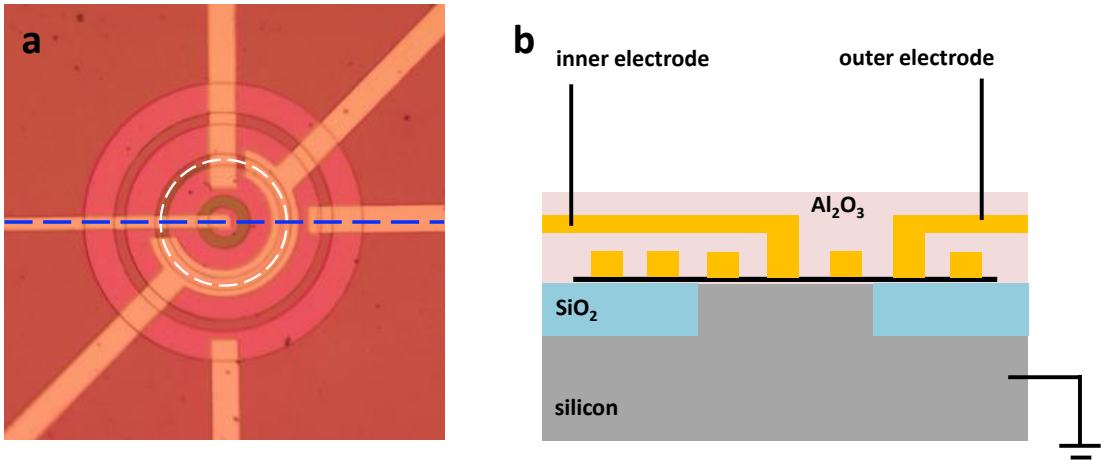


Figure 3-5 (a) The optical image selected area tunneling device, the white dashed line labels the Si/SiO_2 boundary. **(b)** The cross section schematic along the blue dashed line in (a).

Thus, the lateral transport measurements and the selective area tunneling spectra exclude the explanation of the presence of Landau levels from either spontaneous magnetization or pseudo-field. More importantly, the selective area tunneling spectra further indicate the tunneling peaks are mainly contributed by the Gr-Si interface. Therefore, our proposed model at Gr-Si junction is capable of reasonably elucidating the physical origin of the experimentally observed peaks. This harmonic oscillation model may be hypothetical, but it provides readers with a sense to construct a possible picture of electron tunneling process through quantum interfacial states. Undoubtedly, further research is needed to develop a clearer illustration and deeper understanding of these discrete energy levels at Gr-Si interface.

3.3 Summary

In summary, we observed evenly distributed tunneling peaks in the tunneling junction composed with silicon and Gr. The possibility of the presence of Landau levels resulted from either spontaneous magnetization or strain-induced pseudo-field was carefully excluded via lateral transport measurement and selective area tunneling study. Instead, a new interfacial quantum state specific to the 2D-3D junction was observed and confirmed for the first time. The formation of such interfacial state is a result of the transparency of 2D material to vertically propagating electrons and, consequently the electron oscillations occur around the 2D layer. A simple harmonic oscillator model can be applied to explain the experimental observations. This quantum state is a pure interfacial effect and cannot be constructed via the linear combination of the eigenstate of either the 3D or 2D material. The interference between the discrete states and the continuous band structure results in the FFR, and the lifetime of the trap state is estimated to be 1 ps. Our experimental results together with the theoretical explanations demonstrate the interfacial quantum state on 3D-2D junctions, which is not fully discussed and understood before. This new discovery can provide us an insightful understanding about the interfacial exchange processes in 2D materials.

3.4 Experimental Methods

Monolayer gr is grown on copper foils using plasma-enhanced chemical vapor deposition (PECVD).[87] For both the side contact and the vertical tunneling structures, a <100> n^{++} Si substrate with a dopant concentration of 10^{19} cm^{-3} is used as the substrate and as the contact electrode, and a 300 nm field oxide is deposited using the LOCOS process around each contact region to define the injection area and isolate individual devices. The Si substrate is subsequently treated with HF, immediately followed by the wet transfer of the Gr. The monolayer Gr is etched into many disks with a diameter slightly larger than the contact region using oxygen plasma, followed by photo-lithography and e-beam evaporation of the side and top contacts (Cr/Au 10/100 nm).

The temperature dependent and magnetic field dependent IV characteristics and tunneling spectrums are measured in a physical properties measurement system (PPMS, Quantum Design, Inc.). The IV curves are measurement with a Keithley 4200 semiconductor analyzer. The 1^{st} and 2^{nd} order tunneling spectra are collected via SRS 510 lock-in amplifier with an Agilent 3250 function generator. The amplitude of the AC modification is set to 2 mV_{p-p}.

Chapter 4 Moiré-Modulated Conductance in Scalable Silicon-Graphene Vertical Tunneling Devices

Graphene/hexagonal boron nitride hetero-structure holds a great deal of interests because of its mature development, ideal suspending substrate and various applications on electronics devices. A variety of methods to prepare graphene/hexagonal boron nitride hetero-structure have been proposed for different purposes. Although exfoliated stack is well known to be of the highest quality, when it comes to commercial applications, mechanical exfoliation might not be the best choice due to its small device size and difficulty to achieve mass production. The combination of developed chemical vapor deposition growth techniques and transfer skills may be the solution to it. However, very few study focus on the macroscopic transport behavior of grown and transferred graphene/hexagonal boron nitride hetero-structure. In this letter, we fabricated a micro-scale tunneling device as a tool to investigate the electronic transport property of grown and transferred graphene/hexagonal boron nitride hetero-structure. Two dips were observed in our tunneling spectra, which indicate two minimums in electronic density of states. They can be attributed to secondary Dirac points stemming from the generated graphene/hexagonal boron nitride Moiré superlattice. Scanning tunneling microscope was performed to verify the formation of Moiré pattern and determine the rotation angles between graphene and hexagonal boron nitride. Our result suggests that several Moiré domains will be created in our hetero-stack, and two of them are most commonly found. Narrower and upshift graphene Raman 2D peak when being placed on boron nitride than on silicon oxide is another evidence for the formation of Moiré patterns. This study provides a useful way to

macroscopically investigate electronic behavior of a van der Waals materials, and our finding may be used when graphene/hexagonal boron nitride hetero-structure are pushed to everyday applications.

4.1 Motivation

Since the first discovery of single-layer Gr in 2004, 2D materials have attracted a great deal of attention.[88] Until today, a variety of 2D crystals covering a broad range of electronic and magnetic properties have been isolated and studied, and hetero-stacks among them also hold strong interest and open up an exciting field of research.[20,89–91] Because of the high surface-to-volume ratio of these layered materials, their intrinsic properties in hetero-structures are highly sensitive to the environment, including the supporting substrate and encapsulation. Hexagonal boron nitride (h-BN), an insulating vdW crystal, has been found to be a perfect candidate to serve as substrate, encapsulating materials and gate dielectric in 2D materials based devices.[27,92] Gr supported by a h-BN substrate or sandwiched in two h-BN layers shows excellent electronic performance and extended durability compared to Gr on silicon dioxide due to a significant reduction of electron-hole charge fluctuation.[93–96] There are several methods to prepare Gr/h-BN hetero-structure, and most previous Gr/h-BN studies have used mechanically exfoliated Gr and h-BN sheets, in which way the layer number and lateral size are difficult to be intentionally managed.[28,92,97–104] However, in order to make 2D devices applicable and practical in our everyday life, scalability and thickness controllability are two important issues that should be taken into considerations. Therefore, chemical vapor deposition (CVD) family including plasma enhanced CVD (PECVD)[105], low-pressure CVD (LPCVD)[106–108] and ambient pressure CVD (APCVD)[109–111] become useful tools to synthesize Gr and h-BN in which the control of precursor flow rate, growth pressure and growth temperature will give us an amount of room for the size and thickness adjustability of the 2D crystals. Furthermore, with a transfer technique, large-scale CVD-grown layered materials can readily be transferred onto arbitrary substrate without concern of lattice mismatch, and most importantly, their properties are kept remained.[112]

Undoubtedly, exfoliated and CVD-grown samples are different in many aspects. Other than abovementioned size and layer number controllability, the differences are also in their crystallinity, carrier mobility, and surface morphology, and these differences will have huge influence on electronic characteristics of Gr/h-BN stack. Besides, for a real application, a micro-scale device is used, and its overall performance will be inclusive. Nonetheless, to our knowledge, there is no investigation on the Gr's macroscopic electronic properties in a Gr/h-BN system comprising of CVD-grown and transferred Gr and h-BN.

Here we use a large-scale tunneling device as a tool to probe the carrier density of states in Gr sheet and focus on macroscopic transport study in Gr/h-BN hetero-structure prepared by CVD growth and transfer technique. It is found that numerous Moiré superlattice domains may be formed since the CVD-grown Gr and h-BN are both polycrystalline, which dramatically affects the electron transport property in Gr layer. Multiple samples were fabricated and measured, and we observed more than one prevailing secondary Dirac points (SDPs) in our macroscopic tunneling experiment. The morphologies of Moiré patterns were imaged by scanning tunneling microscope (STM), and the most commonly observed rotation angles between Gr and h-BN are ~4° and ~7°, which correspond to our experimentally detected SDP energy positions in our transport results. Theoretical calculation analysis was also implemented to confirm our experimental observations and proposed explanation. Moreover, Raman spectroscopy was implemented to confirm the Gr quality, in which the full width at half maximum (FWHM) of Gr 2D peak indicates the formation of Moiré superlattices.

4.2 Result and discussion

4.2.1 Fabrication of Gr/h-BN Hetero-structure in Vertical Tunneling Device

Figure 4-1a shows the cross-section illustration of our device structure. Degenerately doped n-type silicon (n^{++}-Si) was used as a substrate and electrode, and was thermally oxidized to form thick SiO_2 insulating layer. The defined tunneling area with diameter of 190 μm was masked with silicon nitride (Si_xN_y) to prevent the oxidation. After removing Si_xN_y and hydrogen fluoride acid treatment, a n^{++}-Si tunneling area was exposed. Few-layer h-BN and monolayer Gr were then transferred respectively to form a vertical hetero-structure on top of the n^{++}-Si tunneling area. Note that at each transferring step, annealing treatment at 300°C in H_2:Ar atmosphere was applied to thoroughly remove the organic contamination and clean the surface. Afterwards, a very thin aluminum layer was evaporated, which would be rapidly oxidized into Al_2O_3 layer to protect our Gr/h-BN samples. Conventional optical lithography was then used for electrode and Gr disk shape patterning. **Figure 4-1b** shows the top-view optical image of our tunneling structure with Gr/h-BN etched into circular shape. During the electrical measurement, the Cr/Au electrodes were grounded, and an alternative voltage bias was applied to the highly doped silicon.

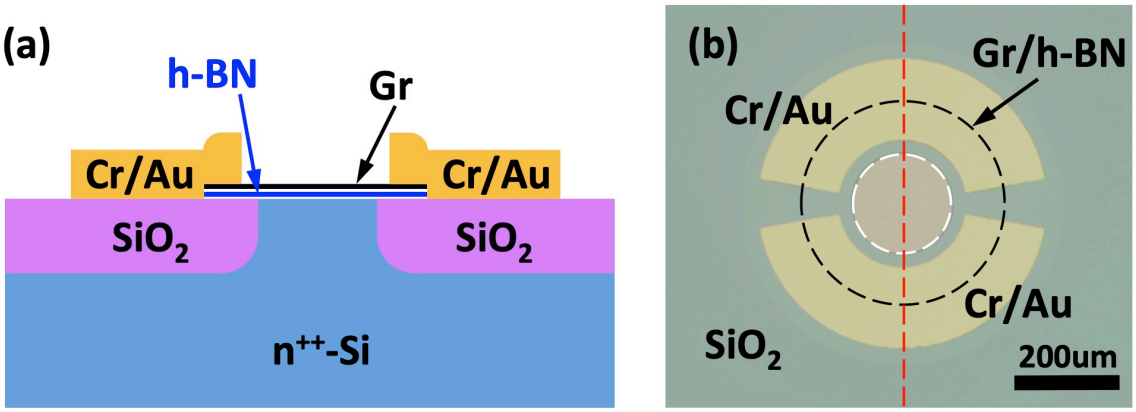


Figure 4-1 Gr/h-BN hetero-structure in our tunneling device. **(a)** The side-view schematic of the tunneling device structure. **(b)** The top-view of the optical image of the tunneling device. The black dashed circle labels the area with graphene coverage. The white dashed line circle delineates the n^{++}-Si exposed tunneling working area. The red dashed line indicates the position where the cross-section presented in (a).

4.2.2 Tunneling Spectroscopy Characterization and Analysis on Gr/h-BN Stack

The tunneling spectroscopy at low temperature (1.9K) was then measured on the as-fabricated tunneling device, and the result was shown in **Figure 4-2a**. Here, two obvious dips are observed in reverse bias region at -0.58 V and -1.06 V (denoted as $V_{M,1}$ and $V_{M,2}$). It is known that derivative current (dI/dV) can represent density-of-states of a material as we derived in Section 1.5.2. These two dI/dV valleys indicate two density-of-states minimums and may result from the SDPs induced by Gr/h-BN Moiré pattern formation.[99] SDP detections have been reported by several works; however, up to date, the SDP observations were all done by scanning tunneling spectroscopies, which are atomic-scale results. Here, our tunneling device is micrometer-size, and n^{++}-Si is used as one of electrodes; thus, our result could be more macroscopic and representing an overall electron transport performance in large-scale CVD-grown Gr when supported by CVD-grown h-BN. Additionally, as described above and shown in **Figure 4-2a insert**, when a reverse voltage is applied, electrons tunnel from n^{++}-Si to Gr, propagate laterally in Gr, and then collected by Cr/Au contacts; on the other hand, with forward bias applied, electrons are moving from Gr to n^{++}-Si, travel inside the heavily doped silicon substrate, and then collected by Cr/Au. It has been reported that electron mean free path in degenerately doped silicon crystal is around 10 nm at low temperature.[113] Consequently, during the travel in silicon, electrons would undergo plenty of inelastic scattering processes and lose their transport information. Therefore, in this chapter, we will focus our discussion on dI/dV signals in reverse bias region.

Multiple tunneling devices were fabricated and measured, and two dI/dV dips around $V_{M,1}$ and $V_{M,2}$ were commonly occurred. We can then correlate these $V_{M,1}$ and $V_{M,2}$ values to

energies of SDPs, $E_{SDP,1}$ and $E_{SDP,2}$ respectively, by multiplying an electron charge, and realize the difference from the primary Dirac point. All $E_{SDP,1}$ and $E_{SDP,2}$ values are extracted from measured tunneling spectra, and their average values (red and blue hollow squares), standard deviation (red and blue boxes) and extreme values (red and blue error bars) are plotted in **Figure 4-2b**. It is reported that, with the superposition of Gr and h-BN layers, the SDP energy and the Moiré wavelength (λ_M) of the created Moire pattern depend on the rotation angle (θ) between the stacked Gr and h-BN as

$$E_{SDP} = \frac{2\pi\hbar v_F}{\sqrt{3}\lambda_M} \tag{4.1}$$

and

$$\lambda_M = \frac{1.018 a_{CC}}{\sqrt{2.036[1-cos(\theta)]+1.018^2}}, \tag{4.2}$$

where $\boldsymbol{a_{CC}}$ is graphene lattice constant (~0.246 nm) and $\boldsymbol{v_F}$ is electron Fermi velocity.[102] It is obvious that $\boldsymbol{E_{SDP}}$, $\boldsymbol{\lambda_M}$ and $\boldsymbol{\theta}$ are entangled to each other, and one of these parameters can delineate the created Moiré supperlattice. **Equation (4.1)** shows that Moiré patterns with specific Moiré wavelengths are generated in our Gr/h-BN hetero-structure, and **Equation (4.2)** is capable of determining the relative rotation angles between our Gr and h-BN layers. As shown in **Figure 4-2b**, the values of $\boldsymbol{V_{M,1}}$ and $\boldsymbol{V_{M,2}}$ are 0.62 ±0.11 V and 1.12 ±0.08 V from our results of tunneling transport experiment, and the two Moiré wavelengths and rotation angles between Gr and h-BN lattices corresponding to these two $\boldsymbol{E_{SDP}}$'s can be calculated through **Equation (4.1)** and **Equation (4.2)**, which are around 3.8 nm and 2.1 nm for Moiré wavelengths and ~3.4° and ~6.5° for rotation angles respectively, as labeled in **Figure 4-2b**.

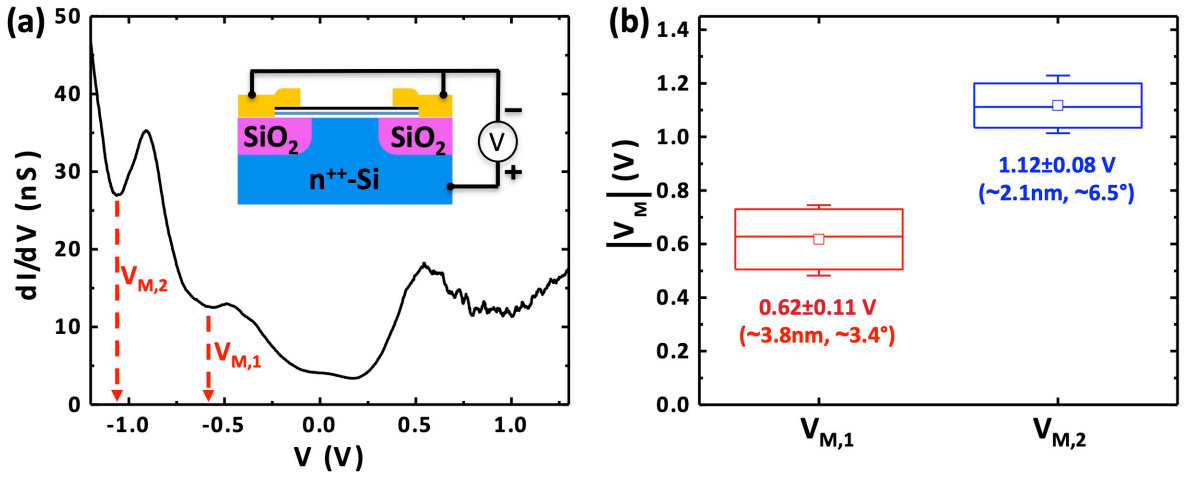


Figure 4-2 Tunneling spectroscopy characterization on the Gr/h-BN in the vertical tunneling device. **(a)** First order tunneling spectroscopy of the Gr/h-BN in a tunneling device at 1.9 K. The two obvious local minimums are labeled as $V_{M,1}$ and $V_{M,2}$ respectively. Inset shows the cross-section device configuration and the measurement setup. **(b)** The summarized $V_{M,1}$ and $V_{M,2}$ positions from multiple devices. Their average values (red and blue hollow squares), standard deviation (red and blue boxes) and extreme values (red and blue error bars) are all plotted. The corresponding Moiré wavelength and rotation angle are calculated by Equation (4.1) and (4.2) and labeled beneath the average and standard deviation values.

4.2.3 Scanning Tunneling Microscope for Moiré Pattern Confirmation

Atomic scale areal Moiré surface morphology of Gr/h-BN hetero-structures was revealed by scanning tunneling microscope (STM) for determining its Moiré wavelengths and further verifying our experimental observation of SDPs. **Figure 4-3a** shows a schematic of the STM configuration for Gr/h-BN hetero-stucture on Au(111)/Mica substrate. The Gr/h-BN hetero-structure for STM measurement was transferred onto Au(111)/Mica substrate via polymer-free transfer method to eliminate the polymer contaminants on top of the surface.[114] **Figure 4-3b and 4-3c** show the representative STM images on transferred Gr/h-BN heterostructure on Au(111)/Mica, and Moiré patterns can clearly be seen in both figures with different Moiré wavelengths. Note that the bright stripes in the STM images are resulting from the Au(111) herringbone reconstruction pattern. The Moiré patterns is formed by the interface between Gr and underlying h-BN/Au(111) substrate, and can be attributed to the lattice mismatch is ~1.8%. Therefore, changing the twisted angle between Gr and h-BN lattice leads to Moiré patterns with different Moiré wavelengths as observed in **Figure 4-3b and 4-3c**. The twisted angle with respect to Gr can be determined by the Fast Fourier transforms (FFT) images of the pattern as shown in the **Figure 4-3e and 4-3f.** Here the outer spots show the Gr reciprocal lattice and the inner spots indicate the Moiré pattern reciprocal lattice. The twisted angle can be determined by the angle between these two reciprocal lattice vector $\overrightarrow{k_g}$ and $\overrightarrow{k_{h-BN}}$ shown in the **Figure 4-3e and 4-3f**. Therefore, the twisted angles of **Figure 4-3b and 4-3c** are found to be ~4° and ~7°. Furthermore, the correlation between the twisted angle and the periodicity of Moiré pattern is given by **Equation (4.2)**. The image in **Figure 4-3b and 4-3c** exhibit their correspondent Moiré wavelengths are ~3.6 nm and ~2.2 nm respectively. The statistical distribution of Moiré pattern twisted angles were plotted in **Figure 4-3d** which shows these two angles are mostly discovered

ones. It has been confirmed that Gr and h-BN sheets are able to rotate themselves to achieve a low-energy state during a thermal treatment.[115] Therefore, these two angles are believed to possess the lowest energies (or local minimums) and be in stable (or meta-stable) states; Gr and h-BN sheets tend to form these angles during annealing process. These STM studies provide us the direct evidence of the formation of Moiré patterns in our Gr/h-BN hetero-structures, and also present the information about the induced Moiré superlattices such as the periodicity and twist angles.

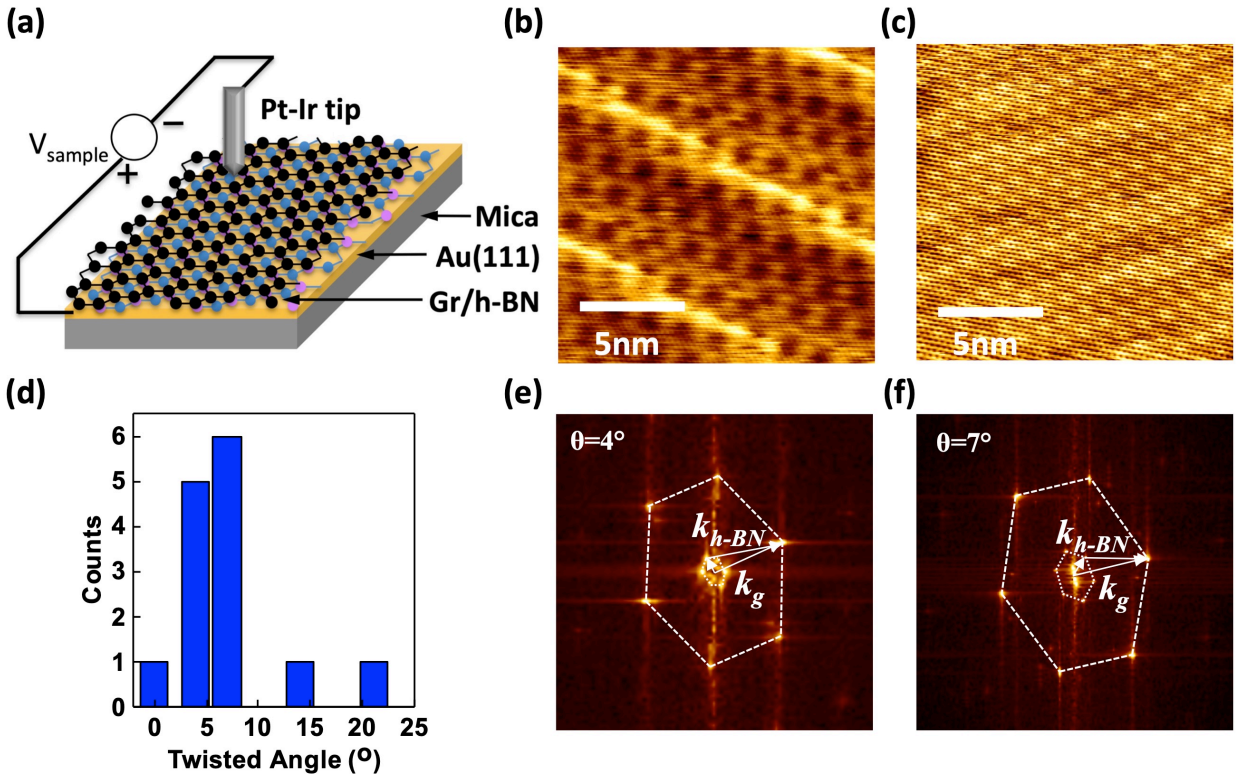


Figure 4-3 (a) Scanning tunnelling microscope measurement schematics on a Gr/h-BN hetero-structure on Au(111)/Mica substrate. **(b)** Topography of a Moiré supperlattice with Moiré wavelength of ~3.6 nm and a ~4° twisted angle. **(c)** Topography of a Moiré supperlattice with Moiré wavelength of ~2.2 nm and a ~7° twisted angle. These images were both acquired with a sample voltage of 0.5 V and a tunnel current of 0.5 nA under a high vacuum atmosphere of 10-11 Torr at room temperature. **(d)** Twisted angle distribution for Gr/h-BN hetero-structure. **(e)** The Fourier transform pattern of the corresponding STM images is shown in the (b). **(f)** The Fourier transform pattern of the corresponding STM images is shown in the (c).

4.2.4 Theoretical Simulation of Gr/h-BN for Stable (or Mata-stable) Rotation States

To further validate our experimental observation and the above explanation, theoretical simulation for energies at each rotation angles was employed. The calculations were performed using the Vienna *ab initio* Simulation Package (VASP)[116] with the Perdew-Burke-Ernzerhof (PBE)[117] functional. Van der Waals corrections are included via the density functional theory Dispersion Correction 3 (DFT-D3)[118] (See Method for simulation details). **Figure 4-4a** shows the modeled Gr/h-BN hetero-structure applied in our theoretical analysis. The interlayer distance was set to 3.8 Å. Balls with different colors are used to denote each element (carbon with black, boron with blue, and nitrogen with pink). The areas of Gr and h-BN layers are fixed and an angle between the two layers is rotated to calculate the system energy. The part of the system energy directly depending on the overlapping area of the two layers is removed in the calculation to simulate the energy change of Moiré superlattice in different rotation angles (see Method for simulation details). The resulted energies relative to the energy of 0°-state (E_0) with rotation angles from 0° to 8° are obtained and plotted in **Figure 4-4b**. Note that the theoretical simulation is for only small angles up to 8° because our tunneling spectroscopy data is in a limited range up to 1.2 V, which is corresponding to ~7°. Obviously, local minimums can be found around two positions, 4° and 6°-6.5°, which means these two twist angles are most energetically stable (or meta-stable) for this Gr/h-BN stack. These are aligned with our electrical tunneling results and the above-presented STM works. The universally monotonic decease in energy with increasing twist angles may result from the decrease in Gr/h-BN overlapped area with the change in angles. Incontrovertibly, there might be other energetically favorable angles larger than 8°, and they might be shown on conductance dips if we further extended the applied

reverse bias range. Nonetheless, our applied voltage across Gr, h-BN and n^{++}-Si was kept lower than 1.2 V to avoid any damages on our tunneling devices.

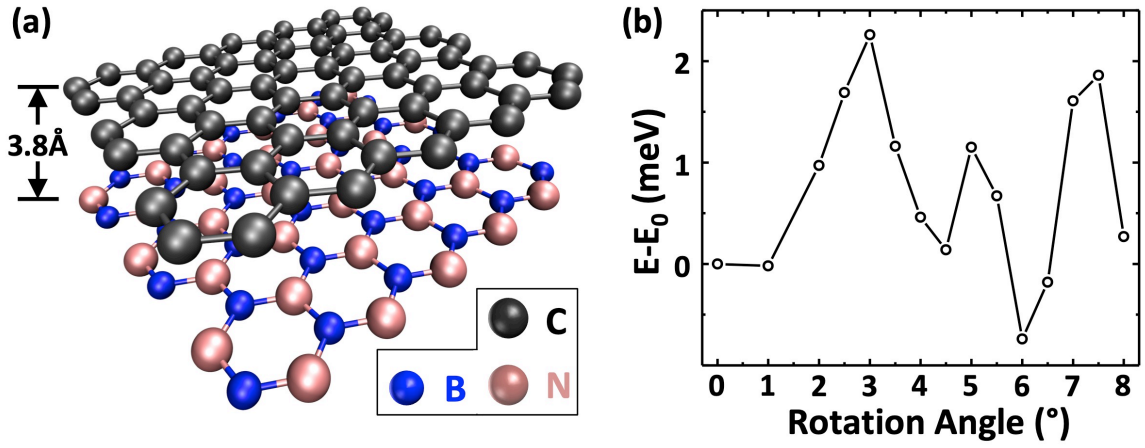


Figure 4-4. **(a)** The atomic model of Gr/h-BN vertical hetero-stack used in our density function theory calculation. Different colors are assigned to each element (black for carbon, blue for boron, and pink for nitrogen). **(b)** Gr/h-BN interaction Energy relative to zero-degree state as a function of rotation angles. E_0 is total energy in the system with rotation angle of 0°.

4.2.5 Raman Analysis for Moiré Pattern Confirmation

To further validate our observation of Moiré patterns in our hetero-stacking system, Raman spectroscopy was employed to ascertain the effect of the Moiré superlattice formation on Raman spectrum. Raman spectroscopy is a fast and nondestructive technique, and it has been reported that FWHM value of Gr 2D Raman peak can be an indicator of Moiré pattern formation probably due to the presence of strain produced by Moiré periodicity.[102] **Figure 4-5a** shows the optical micrograph of a transferred Gr sheet, which is covering entire image region, partially on few-layer h-BN and partially on SiO_2 substrate as labeled. Raman mapping was then scanned on a small rectangular area (red solid line), which contains both Gr/h-BN and Gr/SiO_2 regions, as shown in **Figure 4-5a**. In **Figure 4-5b**, a significant difference in Gr 2D peak FWHM value is obvious: Gr has larger 2D FWHM value on SiO_2 (~49 cm^{-1}) than on h-BN (~23 cm^{-1}). This is consistent with the conclusion in the previous Moiré superlattice Raman research.[102] Additionally, A slight blueshift of Gr 2D peak position can also be observed when placed on h-BN compared to on SiO_2 substrate (see **Figure 4-5c**). As shown in previous work, the dielectric screening on the electronic structure of Gr with an ultra-flat h-BN plays a critical role.[119]

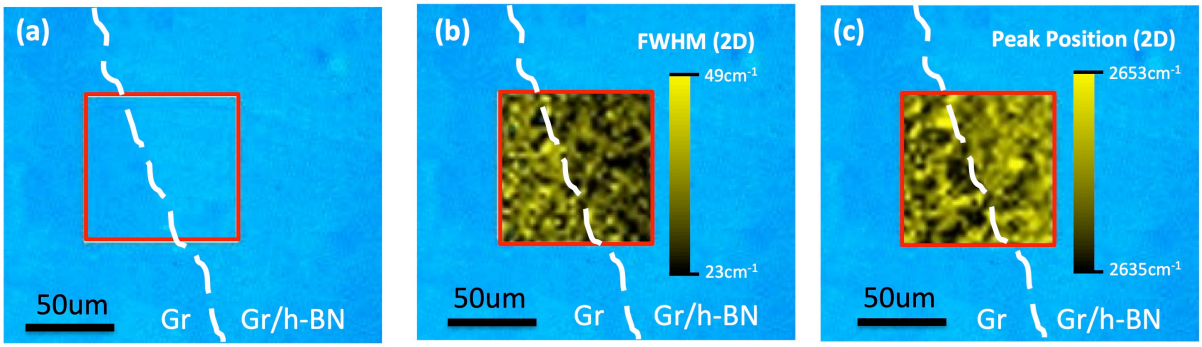


Figure 4-5 Raman spectroscopy mapping on both Gr and Gr/h-BN hetero-structure. **(a)** Optical micrograph of a transferred Gr sheet, which is covering entire image region, partially on few-layer h-BN and partially on SiO_2 substrate. The red solid square frame labels the area where Raman laser is applied. **(b)** Full width of half maximum Raman mapping of Gr 2D peaks inside the red window shown in (a). **(c)** Raman mapping of the 2D peak position inside the red window shown in (a).

4.3 Summary

In summary, we used a micrometer-scale tunneling device to investigate the macroscopic electronic property in a CVD-grown and transferred Gr/h-BN hetero-structure. Our tunneling spectroscopy result shows two additional DOS local minimums other than the primary Dirac point. Several Gr/h-BN stacks are fabricated and measured, and these two local minimums occur repetitively around $0.62 \pm 0.11\ V$ and $1.12 \pm 0.08\ V$, which can be associated to $0.62 \pm 0.11\ eV$ and $1.12 \pm 0.08\ eV$ away from the primary Dirac point, and can be attributed to the generated Gr/h-BN Moiré patterns. With the relationship between Moiré periodicity and SDP energy, which is shown in Equation1, these two values of SDP energies are corresponding to Moiré periodicities of ~3.8 nm and ~2.1 nm and twist angles of ~6.5° and ~3.4°. The topographic morphologies of our Gr/h-BN surface was scanned by STM; indeed, it clearly shows two Moiré superlattices with different Moiré wavelengths of ~3.6 nm and ~2.2 nm, which are consistent with the calculated values from our experimental transport data. In addition, our theoretical calculation reveals that angles around 4° and 6°-6.5° are most energetically stable (or meta-stable), which further verifies the proposed model. In addition, the Gr on h-BN characterizes narrower Raman 2D peaks than on SiO_2, which can serve as an indicator to Moiré pattern formation. This discovery can provide us a deeper understanding about a CVD-grown and transferred scalable Gr/h-BN hetero-structure and be informative when Gr/h-BN devices become commercial and applicable to our everyday life.

4.4 Experimental method

Synthesis of monolayer graphene. Monolayer graphene is grown on copper foils using plasma-enhanced chemical vapor deposition (PECVD).[87] Prior to the graphene synthesis, the copper foils are sonicated in acetone and isopropyl alcohol for 30 minutes then dried by nitrogen gas before insert into the growth chamber. The first step of the graphene synthesis on Cu substrates is preceded by the removal of native copper oxide when the Cu-foils are exposed to H_2 plasma at 40 W power for 1 minutes. The smooth Cu surface ensues simultaneously within 1 minutes after the oxide removal. The growth chamber is subsequently evacuated until the pressure reaches ~ 25 mTorr, and then a mixture of high purity CH_4 (Airgas ,99.999%)and H_2 (Airgas, 99.999%) gases are introduced, where H_2 is used to enhance the dissociation of hydrocarbon. During the initial growth process, graphene nucleates on both the top and bottom sides of the Cu-foils. Continuous exposure of the Cu-foils to plasma at 40 W for 10 minutes in a mixture of CH4 and H2 gases leads to continuing high quality monolayer graphene on the bottom sides. After the growth, the plasma-heated sample is cooled back to room temperature within at least 30 minutes without breaking the vacuum.

Synthesis of multilayer hexagonal boron nitride. The h-BN films were grown using a home-built hybrid CVD setup.[105] Before the whole CVD process, the quartz tube furnace was evacuated with a mechanical pump (P_{base}=1.2 × 10^{-2} torr) and refilled with Ar (99.9997%, O_2 < 0.2 ppm). The pumping and refilling process was repeated three times to eliminate air and moisture, and the tube was finally kept in an Ar environment (flow rate 350 sccm) under atmospheric pressure. The commercial copper foils (HA, 99.9% purity, 35 μm, JX Nippon Mining & Metals) was annealed at 1040°C in Ar environment (flow rate 350 sccm) for 60 min to obtain a smooth surface. After annealing process, the ultrahigh purity hydrogen gas (99.9999%,

O_2 < 0.5ppm, flow rate 15 sccm) was introduced into the system and waited for 5 min to stable the tube environment. The precursor was heated to 130 °C and decomposed to hydrogen gas, monomeric aminoborane, and borazine gas which are carried upstream by a flow of H_2/Ar and delivered to the Cu foils, kept at 1040 °C to start the growth process. The growth continued for certain time duration for 20 minutes to obtained full coverage of the multilayer h-BN film. Finally, the tube furnace was cooled down with the cooling rate ~16°C/min to the room temperature under a 500 sccm of Ar.

Device fabrication. A <100> n^{++}-Si substrate with a dopant concentration of 10^{19} cm^{-3} is used as the substrate, and a 300 nm field oxide is deposited using the LOCOS process around each contact region to define the tunneling area and isolate individual devices. The Si substrate is subsequently treated with buffered oxide etcher (BOE), immediately followed by the wet transfer of the graphene. The monolayer graphene is etched into a disk with a diameter larger than the contact region using oxygen plasma, followed by photo-lithography and e-beam evaporation of the side contacts (Cr/Au 10/100 nm).

Electrical transport measurement. The low-temperature tunneling spectra were measured in an atmosphere created by a physical properties measurement system (PPMS, Quantum Design, Inc.), and collected via SRS510 lock-in amplifier with an Agilent 3250 signal generator. The frequency and peak-to-peak amplitude of the AC modification are set to 10.1 Hz and 10 mV respectively.

Surface Characterization. The Gr/h-BN/Au (111)/mica sample was annealed and sealed in vacuum, and then loaded onto our Omicron VT STM system. The base pressure of the system was 2×10^{-11} torr. Atomically resolved topographic and spectroscopic measurements were carried out on monolayer Gr/h-BN samples at room temperature using a Pt/Ir STM tip. Sample voltage of 0.5 V and tunnel current of 0.5 nA were chosen for mapping data collection.

Raman mapping. The Raman mapping was taken with a Renishaw Model inVia confocal Raman spectrometer system using a laser of 633-nm wavelength. In order for a better signal-to-noise ratio, a 50X objective lens and a grating of 1800 lines/mm were used during our Raman map scanning.

Theoretical Analysis. The calculations are performed using the VASP package[116] with the PBE[117] functional. Van der Waals corrections are included via the DFT-D3 method.[118] The energy convergence value is set as 10^{-6} eV. 1nm × 1nm rectangular graphene and h-BN stacked fragments are adopted to evaluate the interlayer interaction. The stacking order is AA and the interlayer distance is fixed at 3.8 Å. C, N, B atoms are allowed to relax within the atomic plane and all terminated H atoms are allowed to relax until the force on each atom is less than 0.02 eV/Å. Energy cutoff is chosen as 450 eV. At least 10 Å vacuum spacing is set between the adjacent cells. The Brillouin zone is sampled only at the Γ point. With a small rotation angle, the lost in overlapping area is proportional to the angle. Therefore, in order to focus mainly on the Gr/h-BN interaction related to rotation angle, we deducted the monotonic energy decrease by subtracting an energy function proportional to the twist angle.

Chapter 5 Conclusion and Suggested Future Works

5.1 Conclusion

The works presented in this dissertation focused on electron out-of-plane transport across and into Gr as well as macroscopic electronic property in CVD-synthesized and wet-transferred Gr/h-BN hetero-system through a tunneling device and electron tunneling spectroscopy. With this silicon based tunneling structure, we are able to investigate several fundamental electronic phenomena when electrons are vertically propagating across or into Gr. This work help to put a piece of puzzle, gain more insightful understanding and build a more solid picture about electron vertical transport in pure 2D hetero-structure or 3D-2D integrated structure. Our results are highlighted in the following.

First of all, the role of a 2D sheet, Gr in our case, in electron vertical transport across it was carefully studied through electron tunneling spectroscopy with a Gr-Si hetero-junction. Gr together with its neighboring vdW gaps form a tunneling barrier that is nearly transparent to perpendicularly propagating carriers due to its atomic thickness and the transverse momenta mismatch between vertically ejected electrons and Gr lateral band structure. Although having very little influence on electron out-of-plane transport, Gr can still trap a fraction of electrons, act as a 2D atomic grid, and control the carrier flux via the application of an external bias. A new model based on quantum capacitance effect for electron vertical tunneling was proposed to develop an explicit knowledge on electron vertical transport across a van der Waals crystal.

In the following part of this dissertation, we found and confirmed the interfacial oscillation state at 2D-3D interface for the first time. A simple harmonic oscillator model was

used to explain this interfacial trap state. In addition, FFR could be induced by the interaction between this interfacial state (discrete energy spectrum) and Gr lateral band diagram (continuous energy spectrum). Our theoretical calculation result agrees with the experimental observation very well, and lifetime of the ground state of the interfacial state is determined to be ~1 ps. This study provided more insightful understanding of interfacial effect in low-dimensional materials based system.

Lastly, in chapter 4, we presented the macroscopic electron transport property in a hetero-junction comprised of CVD-grown and transferred Gr and h-BN through electron tunneling spectroscopy and DFT theoretical simulation, and the relative rotation angle preferences were found to be ~4° and ~7°. Multiple secondary Dirac points induced conductance local minimums show up, and the creation of Moiré patterns is confirmed by STM measurements. Our result suggests that multiple Moiré domains are formed, and the two with Moiré wavelengths of ~3.6 nm and ~2.2 nm are the most dominant. This study provides a useful way to macroscopically investigate electronic behavior of a vdW material, and our finding may be used when Gr/h-BN hetero-structure is pushed to everyday applications.

5.2 Suggested Future Works

As we presented in the previous chapters, this tunneling device structure was used for investigating both electron vertical transport across and into a 2D material and electron macroscopic transport characteristics within Gr in Gr/h-BN hetero-structure. For all studies, the techniques to prepare 2D crystals are CVD growth. The reason is that for making a practical application in our everyday life, exfoliation is neither an effective (in terms of size and reducibility) nor a thickness-controllable method even though it can provide the best crystalline quality. The method we used to have a particular vdW material on top of the tunneling region is etchant-based wet transfer. However, there is a possibility to create pinholes in the transferred 2D sheet during the cleaning step (rinsing the 2D material with DI water in several different containers). Hence, it will definitely be advantageous to directly grow a target 2D crystal on top of our substrate. In this way, a relatively cleaner and more robust Si-Gr system can be formed for research and application purpose. Nonetheless, there are also many challenges we can expect. The electrical property of the silicon substrate will unquestionably be influenced especially the change in resistivity due to a combination of lattice and impurity scattering.[120] Besides, there is a Si/SiO_2 interface at the boundary of working area, and a growth of 2D material on both regions could be problematic because of their different surface energies, which usually affect growth conditions.

In fact, with the solution based wet transfer technique, we are still able to conduct scientific studies on CVD-growable and interesting 2D materials, e.g. molybdenum ditelluride ($MoTe_2$). $MoTe_2$ is one of the most intriguing layered materials but limited explored. Among the numerous 2D vdW TMD, our experimental setup and device preparation technique are particularly suitable for the fundamental study on $MoTe_2$ since it is the only one which can be

directly synthesized by CVD[121] or PVD[122,123] to be semiconducting 2H, semi-metallic 1T' phases or lateral homo-junction of both the above two owing to its small energy difference between the two phases (~40 mV).[124–126] Additionally, one of the most remarkable features of $MoTe_2$ is its comparable energy band gap with that of silicon (~0.93 eV for bulk and ~1.1 eV for monolayer 2H $MoTe_2$)[127], which is preferential for future silicon-integrated electronic and optoelectronic devices. Therefore, we propose a device configuration similar to ours in chapter 3 but with 2H $MoTe_2$ as the 2D sheet and 1T' $MoTe_2$ as contact (as shown in **Figure 5-1a**) for a photodetector study. Note that the 1T' $MoTe_2$ is used as electron collecting electrodes for forming Ohmic homo-junction and reducing contact resistance.[128] Moreover, another feature that makes 2H $MoTe_2$ attention-grabbing is its large valance band spin-orbit coupling splitting of ~238 meV because of the heavy terminating telluerium atoms.[129] With odd layer number, inversion symmetry breaking together with its large spin-orbit coupling splitting energy may result in long-lasting spin and valley polarization and shed light on the integration of spntronics and valleytronics.[130] Hence, with the same structure, instead of using spectrometer, a polarized laser (could be circularly, linear or any combination) is employed for $MoTe_2$ valley polarization study. Electrons may carry the valley polarization information and show come clues electron tunneling spectroscopy data. Also, if we can use a magnetic metal to replace the electron ejecting part, it may be more interesting since we have one more controllable parameter, electron spin. (see **Figure 5-1b**).

Lastly, judging from chapter 2, the Gr and its neighboring vdW gap are proposed to act as a tunneling barrier,[79] and the Gr sheet is able to further serve as a transparent grid to control the carrier flux via the externally applied voltage. Thus, we propose to utilize the van der Waals gap beneath the Gr as base-collector insulator and the van de Waals gap above the Gr as emitter-base

insulator in a hot electron transistor[131,132] (See the simplified configuration in **Figure 5-2**[131]). This idea may make a high-frequency operation and high common-base current gain come true. Nevertheless, there are still some unknowns about the vdW barriers, such as its thickness, its insulating properties and intrinsic characteristics including dielectric constant. Besides, challenges are also in the device fabrication such as a perfect transferred and uncontaminated Gr sheet and a mild top electrode deposition without any concern about damage in Gr. Undoubtedly, further research and attempt are needed for this project.

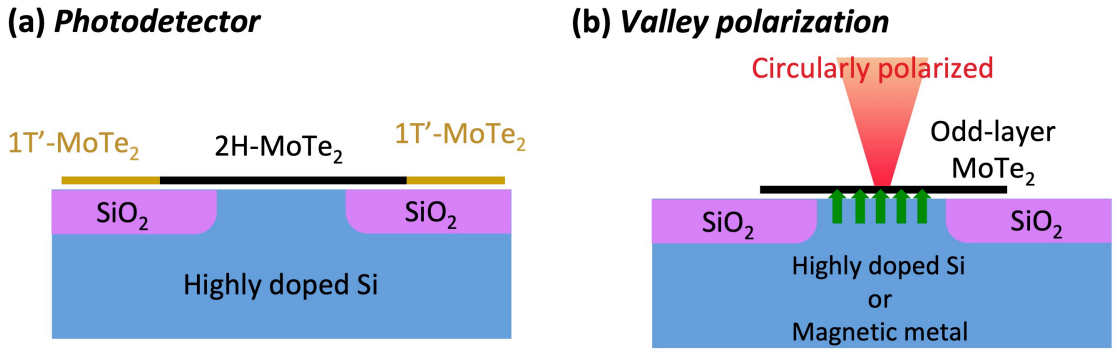


Figure 5-1 (a) Illustration of a proposal of using 2H $MoTe_2$ as an active material and 1T' $MoTe_2$ as a carrier collecting material. **(b)** Illustration of an idea to investigate the valley polarization of $MoTe_2$.

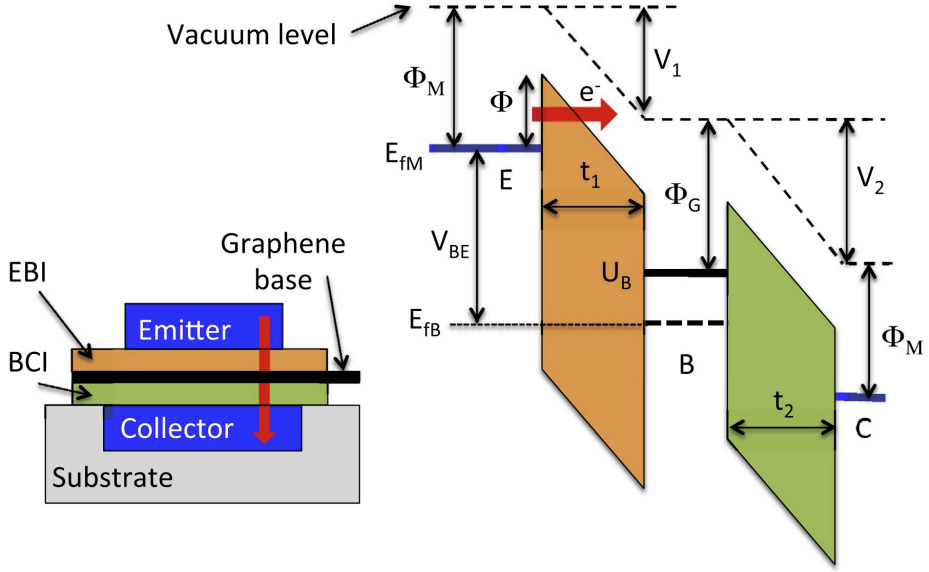


Figure 5-2 Sketch of a Gr based hot electron transistor and corresponding band diagram with bias.[131]

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