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A 40mW/channel Image Sensor Line Driver IC with Independently Tunable Gain and Settling Time

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Abstract—A 16-channel analog front-end integrated circuit (IC) for interfacing an image sensor with single-ended analog output to a differential-input digitizer is presented. The IC is designed for image sensors used in single-electron counting direct detection cameras with applications in cryogenic electron microscopy (cryo-EM), but it's high flexibility allows usage with a variety of sensors. An operational transconductance amplifier (OTA) and a transimpedance amplifier (TIA) replace the traditional instrumentation amplifier, to allow power reduction and decoupling of the gain and bandwidth stages. This allows for a tunable gain in order to exploit the digitizer full-scale range, and an independent bandwidth tuning capability to accommodate a variety of sensors. Additionally, the front-end supports a very wide input common-mode range, and provides offset correction capability as well as frame marker operation. The chip is fabricated in a commercially available 180nm CMOS technology using dual 3.3V/1.8V supply. It achieves more than $\pm 10\%$ gain tunability at 0-1.2V sensor dark-level range, and up to 140MHz operation. Power consumption is measured at 37mW/channel with $155\mu\text{V}$ input-referred noise, at nominal conditions. The chip is a low-power, low-noise, highly optimized solution allowing area and power reduction in camera assemblies.

Keywords—line driver, single-ended-to-differential, image sensors, electron microscopy

I. INTRODUCTION

RECENT advances and continuous scaling of CMOS technology have made CMOS image sensors an increasingly attractive solution for scientific imaging applications. Low cost, high speed, and, more importantly, high integration capability are the key characteristics that have led CMOS image sensors to both improve and surpass charge-coupled devices (CCDs) in many applications, ranging from silicon detectors to electron microscopy and beyond [1]-[2]. Off-chip digitization allows for high pixel density, and use of line drivers to interface the sensor to a high-speed analog-to-digital converter (ADC) is essential in this case.

In this work we present a highly flexible 16-channel line driver to be used in single-electron counting direct detection cameras. The goal is to minimize area for the camera, while simultaneously reducing power in order to control the cooling requirements. The line driver chip takes advantage of an open-loop topology, which is feasible due to the relaxed linearity constraints [3], and adds the capability to independently tune gain and settling time. This allows for the output swing of the line driver to be accurately matched to the ADC fullscale voltage for signal-to-noise ration maximization. The additional operating frequency flexibility enables usage with various sensors and therefore leaves room for future sensor upgrades.

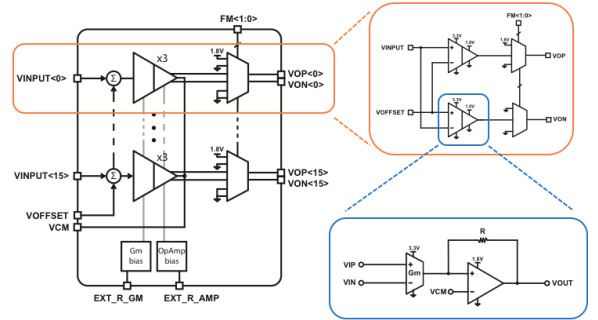


Fig. 1. Block diagram of the chip and sub-blocks. The complete chip block diagram is shown in black outline, the single channel schematic is shown in orange outline, and the instrumentation amplifier is shown in blue outline.

II. LINE DRIVEN DESIGN

Fig. 1 shows a block diagram of the chip and its sub-blocks. Each channel consists of two instrumentation amplifiers connected in a complementary way to implement the singled-ended-to-differential function. The independent offset input V_{OFFSET} is set at $V_{OFFSET} = V_{DARK} - \frac{V_{swing}}{2}$, where V_{DARK} dark-level of the sensor, and can be used for offset correction. Both input and V_{OFFSET} see high impedance loads.

The schematic of the instrumentation amplifier is shown in Figure 2, including the off-chip biasing resistors. The amplifier consists of an OTA which provides the high input impedance, followed by a TIA, which converts back to voltage. The OTA generates a current that is proportional to the difference of its input voltages. Because of the high loop gain of the TIA, this current is forced to flow through the feedback resistor R , generating an output voltage. The gain of the circuit is $A = G_m R_F$, where the G_m is provided by the first stage, and the R is a fixed resistor.

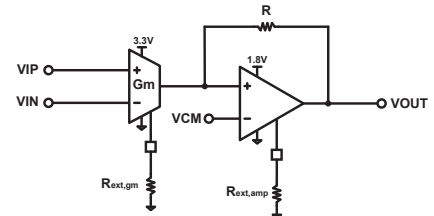


Fig. 2. Schematic of the instrumentation amplifier

The transconductance stage is implemented by a high-

bandwidth folded-cascode amplifier with source degeneration, using a 3.3V supply. A PMOS-input stage is chosen in order to accommodate the required input swing of 0-1.2V. The external resistor $R_{ext,gm}$ controls the bias of the first stage, and therefore directly controls the gain through the G_m . The second stage consists of the folded-cascode amplifier with a class-AB output stage to provide the large current needed to drive the load. The external resistor $R_{ext,amp}$ controls the bias of the second stage. The output stage is designed to dominate the circuit settling performance, which allows for decoupling the gain tuning from the bandwidth tuning. Therefore, the biasing of the first stage does not have a significant effect on settling, and the biasing of the second stage does not have any effect on gain. Finally, a frame marker operation is implemented using analog multiplexers at the output, to allow digital control of the liner driver output for system testing and calibration purposes.

III. EXPERIMENTAL RESULTS

The 16-channel line driver was fabricated in a 180nm CMOS technology. A flip-chip approach was used to allow for further area reduction in the final camera assembly. The bump pads dominate the area. Additional wirebond pads were used in the periphery for initial testing. The die photo is shown in Figure 3.

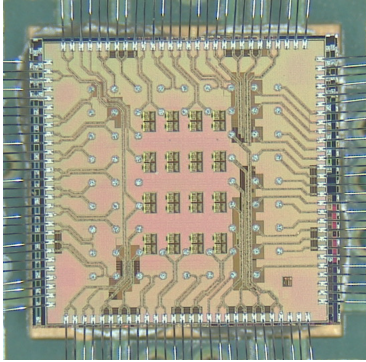


Fig. 3. Die photo of the chip. Chip area is $4\text{mm} \times 4\text{mm}$.

The chip achieves its nominal target, which is gain of 3 and $\geq 75\text{MHz}$ operation, with a measured $155\text{ }\mu\text{V}$ of input-referred noise, and a power consumption of 37mW/channel , while maintaining an excellent linearity of $\leq 0.5\%$ for the entire input range (Figure 4). Figure 5 shows gain tuning by more than $\pm 10\%$, and the corresponding effect on power consumption. Increased gain requires increased power. Figure 6 shows tuning of the worst-case settling time, and the corresponding effect on power consumption. It is shown that 142MHz operation is possible, at a minimal power penalty.

IV. CONCLUSION

A 16-channel line driver chip designed to interface with active pixel image sensors and replace discrete components in direct-detection camera assemblies is presented. The line driver maintains low power and low noise, while offering

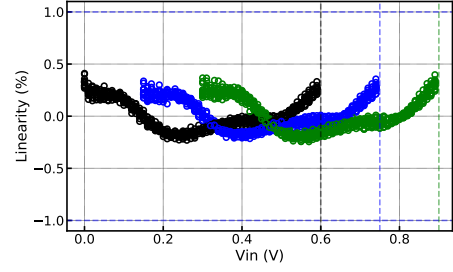


Fig. 4. Measured linearity across all channels for three different V_{DARK} levels. Vertical dashed lines mark the V_{DARK} level, and horizontal dashed lines mark the $\pm 1\%$ limits.

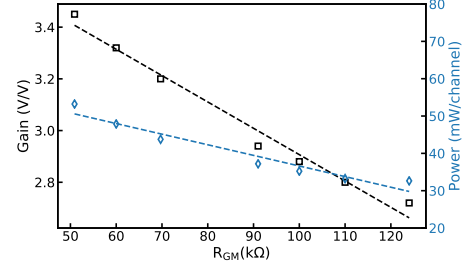


Fig. 5. Gain tuning and corresponding power.

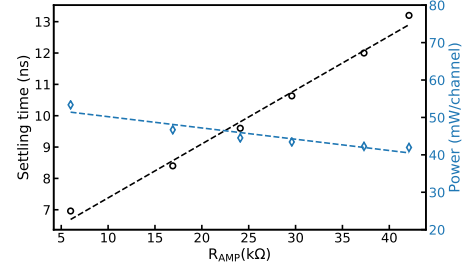


Fig. 6. Settling time tuning and corresponding power.

TABLE I. CHIP PERFORMANCE

	Nominal Value	Tunability range	Units
Technology	180		nm
Gain	3	$\pm 10\%$	V/V
Bandwidth	170		MHz
Large-signal settling time	10	7-13	ns
Input-referred noise	155		μV
Linearity	0.5		%
Power	37	30-50	mW/channel

independently tunable gain and settling time, to maximize signal-to-noise ratio depending on the sensor and application.

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