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The Flying Capacitor LLC Converter: A Hybrid Switched Capacitor Converter with Galvanic Isolation for Large Step-Down Applications

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***Abstract*—In this work, we combine two popular power conversion topologies, the flying capacitor multilevel (FCML) converter and the LLC converter, to arrive at the proposed flying capacitor LLC (FCLLC) solution with advantages of each. The FCLLC comprises a step-down resonant switched-capacitor (ReSC) stage followed by a resonant transformer-based stage which provides soft charging of the flying capacitors, galvanic isolation, and an additional step-down through the transformer. These conversion ratios are multiplied, making the FCLLC especially suited for extreme conversion ratios. An FCLLC prototype capable of direct 400 V to 1 V conversion is fabricated, which demonstrates the potential this topology has for future datacenter applications.**

I. Introduction

Datacenter energy consumption is growing rapidly and projections indicate that it may exceed 10% of worldwide electricity usage by the year 2030 [1]. A significant portion of this energy is lost to heat during power conversion and distribution, leading to intensive cooling challenges and costs. Moreover, any volume taken up by the power electronics is space that would otherwise be used for computing or storage, so the efficiency and power density of these converters is paramount. The modern datacenter power supply architecture is complex, with many cascaded stages to step from the ac grid voltage down to the low operating voltages of CPUs, GPUs and ASICs. Typically, there is an ac to 400 V dc conversion, then a conversion to a distribution voltage of 48 V, another conversion to a 12 V bus, and then a final conversion to point-of-load (PoL) [2]. Fig. 1a demonstrates this approach, which will be referred to as a three-stage design because of its three separate dc-dc conversion stages. Fig. 1b highlights a two-stage design, which is currently gaining popularity, wherein a direct 48 V to PoL conversion occurs [3]–[5]. Fig. 1c illustrates the proposed single-stage approach [6], with direct 400 V to PoL conversion. Multi-stage designs suffer from increased complexity, and also require the use of bus capacitors (C_B) between each stage to ensure that the voltages are held steady. These bus capacitances can be even larger than the converters [7], so eliminating them by performing direct conversion from HVDC to PoL has many benefits for overall system performance.

In this work, we combine two popular power conversion topologies — the flying capacitor multilevel (FCML) converter [8], [9] and LLC converter [10], [11] — to arrive at the proposed flying capacitor LLC (FCLLC) topology, having advantages of each. The FCLLC comprises a step-down switched-capacitor network which resonates with a subsequent transformer-based stage, resulting in complete soft-charging of the flying capacitors [12], [13], galvanic isolation, and an additional step-down through the transformer. As a result of the two inherent cascaded voltage conversions, the FCLLC is especially suited for extreme conversion ratios. An FCLLC prototype capable of direct 400 V to 1 V conversion is fabricated, which demonstrates the potential this topology has for future datacenter applications. Section II introduces the FCLLC and describes its resonant operation. Then, Section III presents the hardware design and experimental results. Finally, Section IV concludes the paper.

II. FCLLC Operation

A. Topology

The FCLLC converter is a merged hybridization of a resonantly operated FCML [14], [15] and a resonant LLC converter, leveraging benefits from both circuit topologies. The FCML converter (Fig. 2a) has demonstrated impressive performance in a variety of applications [9], [16]–[18]. By relying on capacitors for energy storage, with their inherently superior energy density compared to inductors [19], and generating a frequency multiplication effect to shrink the output filter size, it achieves very high power density. Moreover, its multilevel structure allows for the use of lower voltage switches with improved figures of merit (FOM) [20], so it also achieves very high efficiency. Comparatively, the LLC converter (Fig. 2b) and related variants have seen widespread use in both 48 V to PoL and 400 V to 12 V applications [4], [21], [22]). The high-frequency transformer enables a high conversion ratio and provides

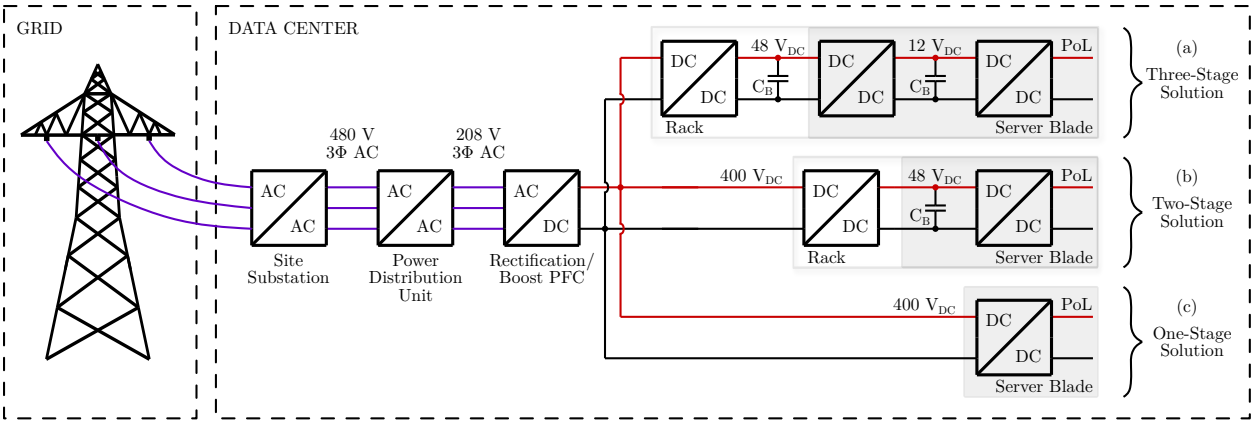

Fig. 1: Simplified illustration of datacenter power delivery architecture from high-voltage ac on the grid to very low voltage dc at the point-of-load. (a) Standard three-stage design, (b) Newer two-stage design with direct 48 V to PoL conversion, (c) Proposed single-stage design with direct 400 V to PoL conversion.

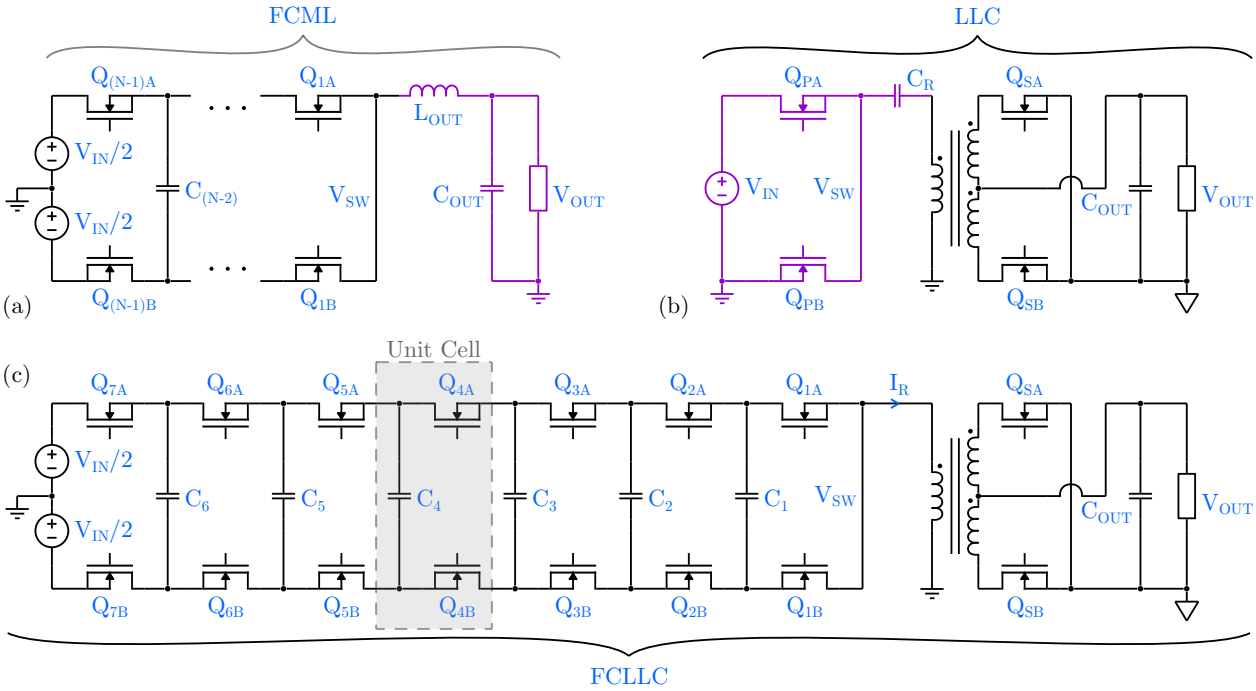

Fig. 2: Labeled schematic for (a) an FCML converter, (b) an LLC converter, and (c) an example 8-level flying capacitor LLC (FCLLC) converter (this work), constructed through the merging of both FCML and LLC structures. Redundant elements of the individual topologies are highlighted in purple.

galvanic isolation to comply with safety considerations, while the resonant operation allows for high switching frequency, and thus small size, while maintaining low losses. The schematic for an FCML is given in Fig. 2a, while the LLC is shown in Fig. 2b. Conventionally, an LLC consists of a primary-side half-bridge (or full-bridge) which generates a square wave voltage driving a resonant capacitor in series with the primary-side leakage inductance of a transformer. Additionally, a switching stage on the secondary side rectifies and filters the high frequency waveform to dc.

For the FCLLC (Fig. 2c), the LLC's primary-side half-bridge and series resonant capacitor are replaced by an N-level FCML stage. This allows for the removal of several components when compared with two independent cascaded FCML and LLC stages (redundant components highlighted in purple in Fig. 2). The output filter of the FCML stage can be completely removed, and the front-end half-bridge and resonant capacitor C_R of the LLC can also be removed. This extends recent work

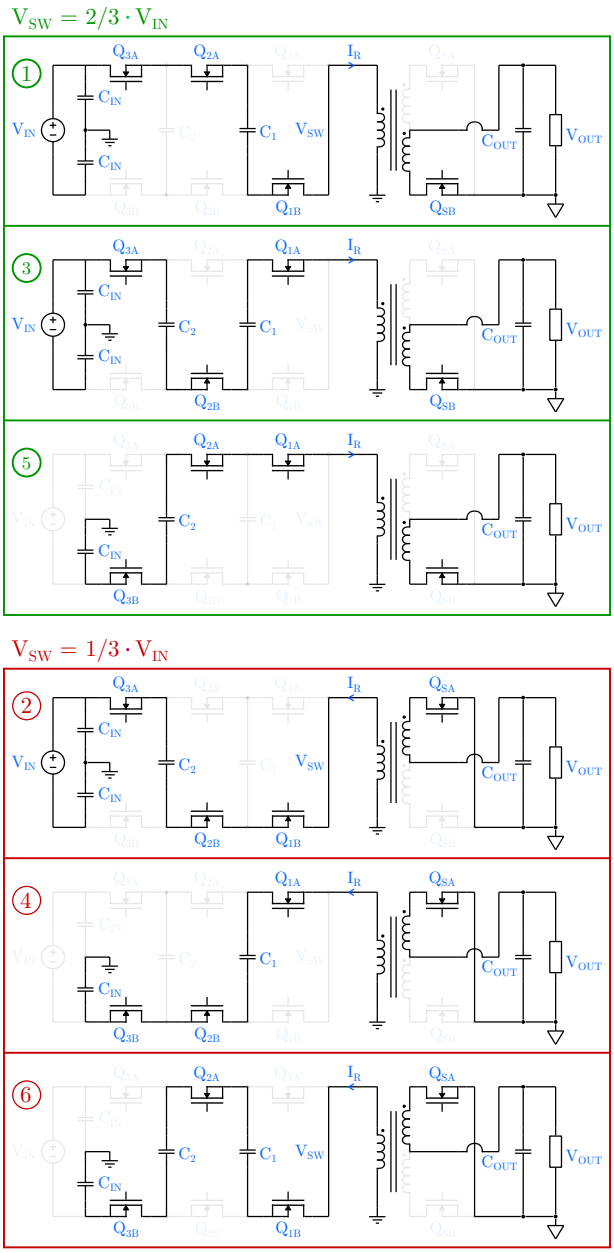

Fig. 3: Equivalent circuits for each state of a 4-level FCLLC. The set of states with resonant conversion ratios of $2/3$ and $1/3$ are highlighted in green and red respectively.

[23], which retains the separate resonant capacitor. In that design, the flying capacitance must be much larger than C_R so that the flying capacitors act as stiff dc voltage sources and do not participate in the resonance. In the proposed work, the flying capacitors themselves are used to resonate with the leakage inductance of the transformer, allowing them to be orders of magnitude smaller than if they have to provide a stiff voltage. Certain states have one capacitor connected in series,

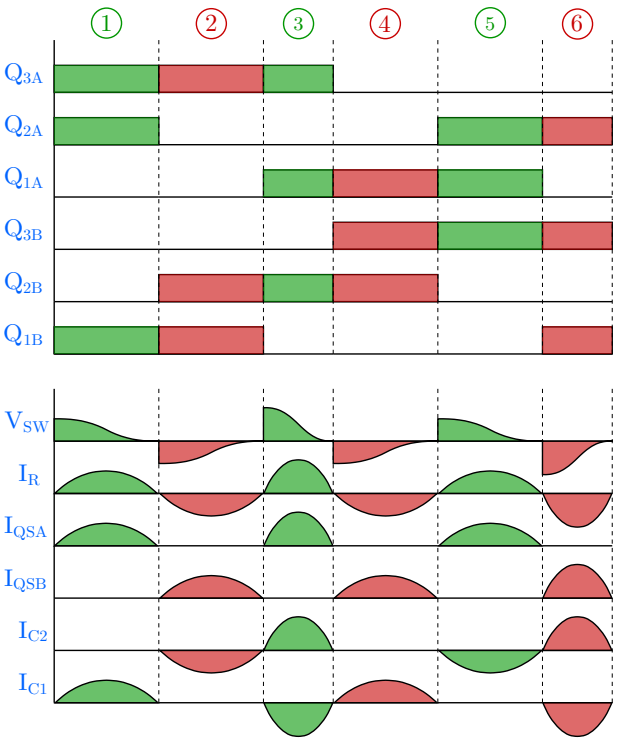

Fig. 4: Key waveforms of proposed topology demonstrating interleaved states and the resultant frequency multiplication effect.

while others have two — thus this is a multi-resonant topology with differing resonant frequencies per phase and an associated increase in control complexity. The FCML and LLC stages are fully merged and so is the operation of this new topology.

B. Modulation

For this subsection only, a 4-level FCLLC is discussed to simplify the diagrams and discussion: operation with any other level count can be extended from this description. Prior work has discussed the modulation and multi-ratio capabilities for a resonant FCML (rFCML) converter [14], [15], [24], [25]. Fig. 3 shows the equivalent circuit for all 6 states of the switched-capacitor network in a 4-level FCLLC. For the 4-level rFCML, switching states 1, 3, and 5 are all necessary for a $2/3$ conversion ratio; and states 2, 4, and 6 are all those necessary for a $1/3$ conversion ratio. During FCLLC operation, these six switching states are interleaved, to provide an ac voltage and current for the transformer primary.

In states 1, 2, 4, and 5, there is a single flying capacitor, C_F, connected in series with the transformer. The duration of these states is $t_1 = \pi\sqrt{L_R C_F}$, where L_R is the leakage inductance of the transformer. In states 3 and 6, there are two flying capacitors connected in series, so these have duration $t_2 = t_1/\sqrt{2}$. The total

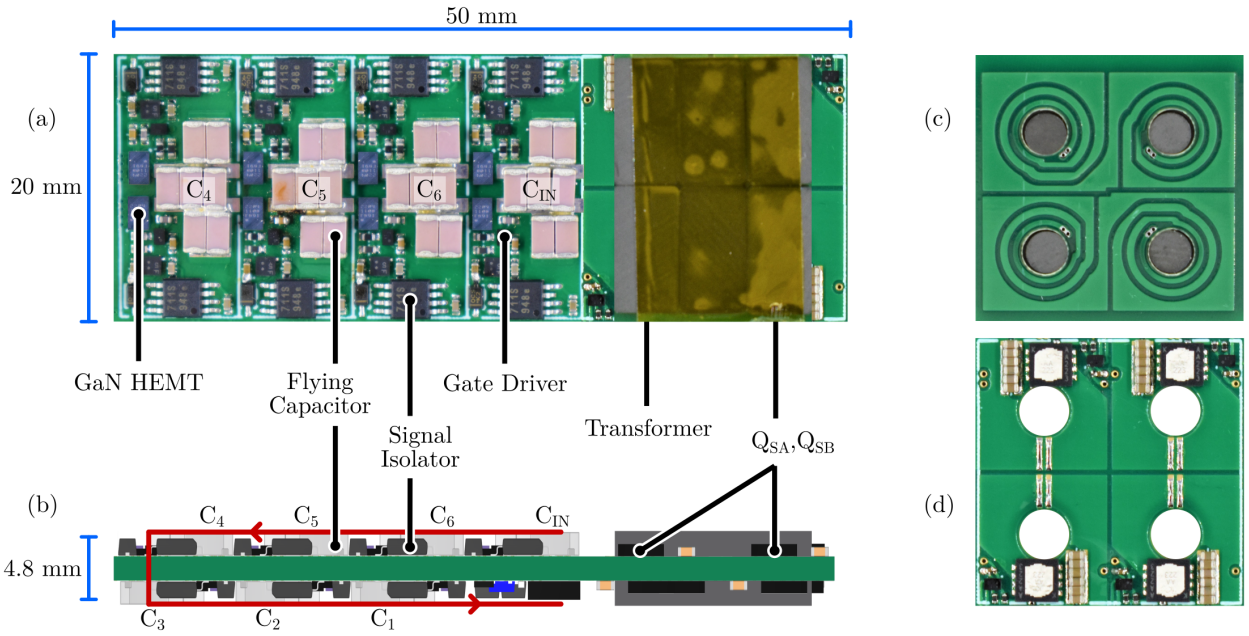

Fig. 5: Hardware photograph of proposed 8-level 400 V to 1 V FCLLC converter with matrix transformer inset to PCB. Key components are annotated, with the power path shown in red. (a) Top view, (b) Side view, (c) Primary windings of transformer, (d) Secondary windings and output rectification.

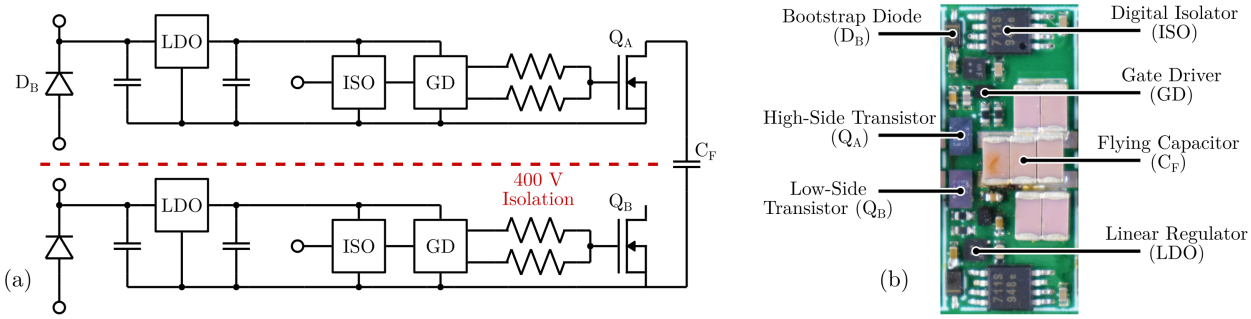

Fig. 6: Cascaded bootstrap gate drive architecture for 8-level FCLLC design. (a) Detailed schematic for unit cell highlighted in Fig. 2c, (b) Layout of unit cell with annotated components. $(N-1)$ of these cells are connected in series to form the primary side of the converter.

number of states is $N_S = 4 + 2(N-3)$, with an overall period $T = 4t_1 + 2(N-3)t_2$. Each primary-side switch commutes only once per period with a duty cycle of 50%. Frequency multiplication occurs, such that the resonant frequency seen by the transformer and output rectification is $(N-1)/T$. Relevant modulation, voltage, and current waveforms are illustrated in Fig. 4, with every flying capacitor successfully achieving net zero charge balance in a full switching cycle. The conversion ratio of this stage is $M_{\text{FCML}} = 1/(2(N-1))$.

In the LLC stage, the voltage conversion ratio is $M_{\text{LLC}} = \lambda/K$, where K is the turns ratio between the primary and secondary windings, and λ is the frequency-dependent gain of the LLC network. The overall voltage conversion ratio of the FCLLC converter is therefore

$$M_{\text{FCLLC}} = M_{\text{FCML}} \cdot M_{\text{LLC}} = \lambda/(2K(N-1)) \quad (1)$$

The FCLLC provides a new degree of freedom and enables the designer to choose how to split the conversion ratio between the level-count of the resonant switched capacitor network and the turn ratio of the transformer.

III. Hardware Validation

A. Hardware Design

To validate the proposed topology and application, a 400 V to 1 V, 8-level FCLLC converter is fabricated ($M_{\text{FCML}} = 1/14$). An annotated hardware photograph is given in Fig. 5. Chip-scale packaged gallium-nitride

Table 1: Hardware Prototype Component List

Component	Part Number	Parameters
Primary Switch	EPC 2204	100 V, 4.4 mΩ
Secondary Switch	ON NTTFS1D2N02P1E	25 V, 0.86 mΩ
Flying Capacitor	TDK CGA5L4C0G2W153J160AA	450 V, 15 nF
Output Capacitor	TDK CL05A226MQ5QUNC	6.3 V, 22 uF
Gate Driver	TI LMG1020	5 V, 7.6 A
Digital Isolator	NVE IL 711S-1E	1000 V
LDO	ON NCP715MX50TBG	5 V, 50 mA

Table 2: Key Converter Parameters

Parameter	Value
Input Voltage	400 V_{DC}
Output Voltage	1.0 V_{DC}
Switching Frequency	100 kHz
Peak Output Power	65 W
Peak Efficiency	81.5 %
Power Density	223 W/in^3

high-electron mobility transistors (GaN HEMTs) are used due to their superior figure-of-merit (FOM) versus silicon transistors at this voltage level [26]. A cascaded bootstrap power supply architecture is used to power all of the floating gate drivers with low dropout regulators (LDOs) ensuring a reliable 5 V supply for the GaN switches [27]. Digital signal isolators provide the level-shifted gate signals. Fig. 6 illustrates the gate drive architecture and details all of the components for each unit cell; the 8-level converter contains $(N-1)=7$ of these cells connected in series.

A planar matrix transformer is utilized to maximize power density and reduce manufacturing complexity, with detailed design guidelines of one such implementation provided in [22]. The transformer is inset to the PCB such that its height is level to rest of the components. A 24-to-1 turns ratio is selected, so $M_{\text{LLC}} = \lambda/24$. The parameter λ is selected such that the overall conversion ratio is $M_{\text{FCLLC}} = 1/400$, i.e. this design choice is suitable for direct 400 V to 1 V conversion when operated slightly above resonance. The power path wraps around the board, beginning at C_{IN} next to the transformer, continuing to the left before going through vias and returning along the bottom of the PCB (illustrated by red arrow in Fig. 5). Relevant components are provided in Table 1, while operating parameters are given in Table 2. The converter box dimensions are 20 mm by 50 mm by 4.8 mm, including all passive components, devices, and gate drive circuitry; the total box volume is 4800 mm^3.

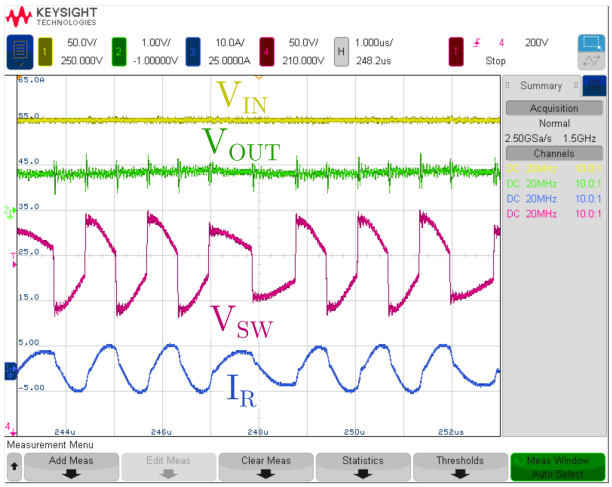

Fig. 7: Measured waveforms for 8-level FCLLC prototype performing 400 V to 1 V conversion at full load.

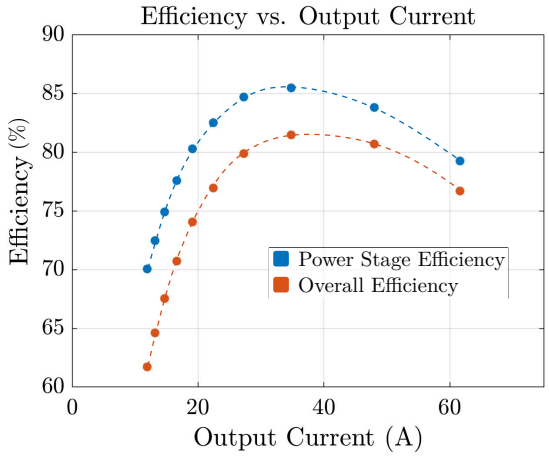

Fig. 8: Efficiency measurements under 400 V to 1 V conversion across load. Power stage efficiency (excluding gate drive loss) and overall efficiency provided.

B. Experimental Results

To demonstrate the converter operation, measurements at 400 V input and 1 V output have been collected, with relevant waveforms shown in Fig. 7. Efficiency measurements were taken with forced air cooling and without heatsinking, as shown in Fig. 8. Peak efficiency is recorded at 85.5% for the power stage and 81.5% including gate drive losses. The full load efficiencies are 74.8% and 72.5%, respectively. The maximum output power of 65.4 W, yields a power density of 223 W/in^3. A comparison to state of the art designs in high conversion ratio datacenter applications is given in Table 3.

IV. Conclusion

This paper has presented a flying capacitor LLC (FCLLC) topology for extreme conversion ratio design.

Table 3: Comparison with State of the Art

Reference	Number of Stages	Stage Conversion Ratios	Stage Efficiencies	Stage Densities (W/in³)	Overall Conversion Ratio	Overall Efficiency	Overall Density (W/in³)
Vicor BCM [28] + Vicor PRM [29] + Vicor VTM [30]	3	384 : 48 48 : 48 48 : 1.2	96% 97.5% 90.4%	1106 1134 531	320	84.6%	272*
CPES LLC [22] + Flex BMR [31]	2	380 : 12 12 : 1	97.6% 90.5%	900 250	380	88.3%	195*
Vicor Mini [32]	1	375:2	74.6%	40	187.5	74.6%	40
Proposed FCLLC	1	400 : 1	81.5%	223	400	81.5%	223

* Power density for multi-stage designs does not include bus capacitors, so system density will be lower

A hardware validation is performed, with measured waveforms and efficiency both demonstrating the potential this topology has for direct 400 V to PoL conversion. A peak overall efficiency of 81.5% was achieved along with a power density of 223 W/in^3.

References

[1] A. S. Andrae and T. Edler, "On global electricity usage of communication technology: trends to 2030," *Challenges*, vol. 6, no. 1, pp. 117–157, 2015.

[2] (2018) Ocp summit 2018: Google 48v update.

[3] J. Baek, Y. Elasser, K. Radhakrishnan, H. Gan, J. P. Douglas, H. K. Krishnamurthy, X. Li, S. Jiang, C. R. Sullivan, and M. Chen, "Vertical stacked lego-pol cpu voltage regulator," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6305–6322, 2022.

[4] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "Single-stage high-efficiency 48/1 v sigma converter with integrated magnetics," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 1, pp. 192–202, 2019.

[5] Y. Zhu, T. Ge, N. M. Ellis, L. Horowitz, and R. C. N. Pilawa-Podgurski, "A 500-a/48-to-1-v switching bus converter: A hybrid switched-capacitor voltage regulator with 94.7*2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1989–1996.

[6] Y. Cui, L. M. Tolbert, D. J. Costinett, F. Wang, and B. J. Blalock, "Direct 400 vdc to 1 vdc power conversion with input series output parallel connection for data center power supplies," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 1554–1560.

[7] Y. Zhu, Z. Ye, and R. C. N. Pilawa-Podgurski, "Modeling and analysis of resonant switched-capacitor converters with finite terminal capacitances," in *2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL)*, 2021, pp. 1–6.

[8] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *PESC'92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*. IEEE, 1992, pp. 397–403.

[9] Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao *et al.*, "A 2-kw single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, 2017.

[10] B. Lu, W. Liu, Y. Liang, F. Lee, and J. van Wyk, "Optimal design methodology for llc resonant converter," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, 2006, pp. 6 pp.–.

[11] (2010) Designing an llc resonant half-bridge power converter. [Online]. Available: https://www.ti.com/seclit/ml/slup263/slup263.pdf

[12] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc–dc converters," *IEEE transactions on power electronics*, vol. 23, no. 2, pp. 841–851, 2008.

[13] R. C. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," in *2008 IEEE Power Electronics Specialists Conference*. IEEE, 2008, pp. 4008–4015.

[14] N. C. Brooks, S. Coday, M. E. Blackwell, R. A. Abramson, N. M. Ellis, and R. C. N. Pilawa-Podgurski, "Operation of flying capacitor multilevel converters at and above resonance," in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1–7.

[15] K. Kesarwani and J. T. Stauth, "Resonant and multi-mode operation of flying capacitor multi-level dc-dc converters," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2015, pp. 1–8.

[16] T. Modeer, N. Pallo, T. Foulkes, C. B. Barth, and R. C. N. Pilawa-Podgurski, "Design of a gan-based interleaved nine-level flying capacitor multilevel inverter for electric aircraft applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12 153–12 165, 2020.

[17] L. Horowitz and R. C. Pilawa-Podgurski, "Modular switching cell design for high-performance flying capacitor multilevel converter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 342–347.

[18] J. S. Rentmeister and J. T. Stauth, "A 48v:2v flying capacitor multilevel converter using current-limit control for flying capacitor balance," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 367–372.

[19] J. Zou, N. C. Brooks, S. Coday, N. M. Ellis, and R. C. Pilawa-Podgurski, "On the size and weight of passive components: Scaling trends for high-density power converter designs," in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1–7.

[20] P. H. McLaughlin, J. S. Rentmeister, M. H. Kiani, and J. T. Stauth, "Analysis and comparison of hybrid-resonant switched-capacitor dc–dc converters with passive component size constraints," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 3111–3125, 2020.

[21] A. T. Russell and E. M. A. Oliveira, "Sine amplitude converters for efficient datacenter power distribution," in *2012 International Conference on Renewable Energy Research and Applications (ICRERA)*, 2012, pp. 1–6.

[22] C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density llc converter with an integrated planar matrix transformer for high-output current applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9072–9082, 2017.

[23] J. Hu, B. Wen, R. Burgos, R. Fernandez-Mattos, and A. Mclean, "Design of a flying-capacitor-based voltage divider llc resonant converter for usb-c pd charger in aircraft applications," *IEEE Transactions on Power Electronics*, pp. 1–17, 2023.

[24] R. A. Abramson, S. Coday, N. C. Brooks, M. E. Blackwell, N. M. Ellis, and R. C. N. Pilawa-Podgurski, "Multi-ratio operation of

flying capacitor multilevel converters at and above resonance," in *2022 IEEE 7th Southern Power Electronics Conference (SPEC)*, 2022, pp. 1–7.

[25] N. M. Ellis, N. Brooks, M. Blackwell, R. Abramson, S. Coday, and R. C. N. Pilawa-Podgurski, "A General Analysis of Resonant Switched Capacitor Converters Using Peak Energy Storage and Switch Stress Including Ripple," *Early Access, IEEE Transactions on Power Electronics*, 2023.

[26] J. Azurza Anderson, G. Zulauf, P. Papamanolis, S. Hobi, S. Mirić, and J. W. Kolar, "Three levels are not enough: Scaling laws for multilevel converters in ac/dc applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 3967–3986, 2021.

[27] Z. Ye, Y. Lei, W.-C. Liu, P. S. Shenoy, and R. C. Pilawa-Podgurski, "Improved bootstrap methods for powering floating gate drivers of flying capacitor multilevel converters and hybrid switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5965–5977, 2019.

[28] (2023) Vicor bcm datasheet. [Online]. Available: https://www.vicorpower.com/documents/datasheets/ds_BCM384x480y325Bzz.pdf

[29] (2023) Vicor prm datasheet. [Online]. Available: https://www.vicorpower.com/documents/datasheets/PRM48JF480T500A00-ds.pdf

[30] (2023) Vicor vtm datasheet. [Online]. Available: https://www.vicorpower.com/documents/datasheets/ds-VTM48EF012T130C01-VICOR.pdf

[31] (2023) Flex bmr467 datasheet. [Online]. Available: https://flexpowermodules.com/resources/fpm-techspec-bmr467

[32] (2023) Vicor mini datasheet. [Online]. Available: https://www.vicorpower.com/documents/datasheets/ds_375vin-mini-family.pdf