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Modeling and Analysis of Resonant Switched-Capacitor Converters with Finite Terminal Capacitances

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***Abstract*—In pre-existing modeling and analysis of resonant switched-capacitor (ReSC) converters, input and output capacitances (C_{in} and C_{out}) have long been assumed to be sufficiently large to ensure ideal input and output behaviors. However, this paper reveals that, in practical applications, finite terminal capacitances can have considerable effects on the output impedance and efficiency of ReSC converters. This paper proposes a general modeling and analysis methodology that can characterize the effects of finite terminal capacitances on the output impedance of ReSC converters. The proposed model is verified by circuit simulations and experimental measurements from a 2-to-1 ReSC converter prototype. It is revealed that the insufficiency in terminal capacitances can result in higher critical switching frequency, and C_{in} has stronger influence on the critical switching frequency than C_{out}.**

I. Introduction

Originating from the conventional pure switched-capacitor (SC) converters [1], [2], resonant switched-capacitor (ReSC) converters can not only leverage the greatly superior energy density of capacitors compared to inductors and transformers but also significantly reduce the inherent capacitor charge sharing loss with soft-charging operation enabled by the augmenting inductor(s) [3]–[5]. Therefore, ReSC converters open up new opportunities for achieving record-breaking high efficiency and high power density, and have recently received increasing attention in various applications [6]–[13].

Although pre-existing models [14]–[16] and analyses [4], [17], [18] of ReSC converters assume input and/or output to be ideal voltage sources as illustrated in Fig. 1(a), practical implementations of ReSC converters involve input and output capacitors (C_{in} and C_{out}) to stabilize the terminal voltages, as illustrated in Fig. 1(b). If the terminal capacitances are much larger than the flying capacitance (i.e. C_{in}, $C_{\text{out}} \geqslant 10C_{\text{fly}}$), the input and output can be regarded as ideal voltage sources. However, in practical applications, the sizes of C_{in} and C_{out} are constrained by space and cost, and thus usually not large enough to ensure ideal input and output behaviors. Fig. 2 illustrates the simulated output impedance of a 2-to-1 ReSC converter with different C_{in} and C_{out}, which shows that the actual output impedance curve can significantly deviate from the ideal scenario when the terminal capacitances are insufficient.

Despite the significant effects of finite terminal capacitances, currently there exists no model that can quantitatively characterize their effects on the performance of ReSC converters. In practice, the sizes of C_{in} and C_{out} are selected mainly based on engineering experiences and through trial and error, indicating the great need for a general method to model and analyze the effects of terminal capacitances.

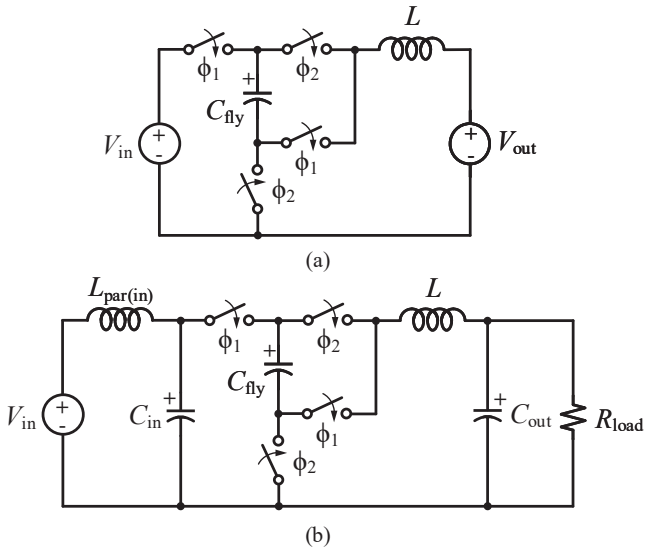

Fig. 1: Schematic of a 2-to-1 ReSC converter. (a) With idealized input and output. (b) With practical input and output. ($L_{\text{par(in)}}$: parasitic source inductance)

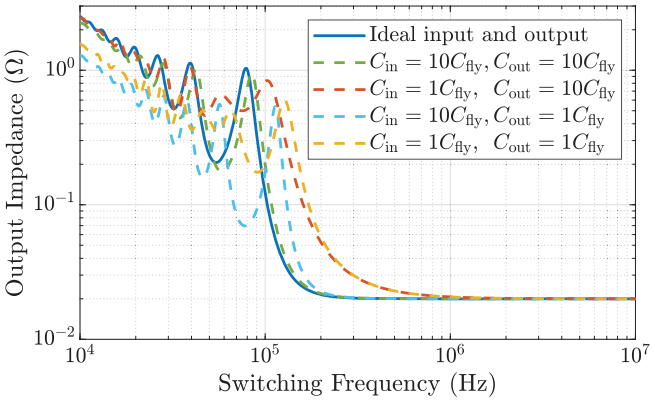

Fig. 2: Output impedance of a 2-to-1 ReSC converter with different C_{in} and C_{out}. ($C_{\text{fly}} = 10$ μF, $L = 0.1$ μH, $R_{\text{ds(on)}} = 10$ mΩ)

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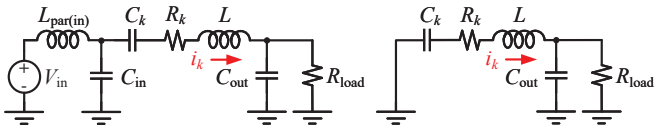


Fig. 3: Complete circuit model of a two-phase ReSC converter with finite terminal capacitances. (a) Case 1 (Phase 1): the input terminal is connected to the source. (b) Case 2 (Phase 2): the input terminal is grounded.

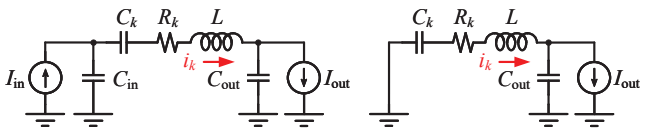


Fig. 4: Simplified circuit model of a two-phase ReSC converter with finite terminal capacitances. (a) Case 1 (Phase 1): the input terminal is connected to the source. (b) Case 2 (Phase 2): the input terminal is grounded.

This paper proposes a general modeling and analysis methodology that can capture the effects of finite terminal capacitances on the output impedance of ReSC converters. With the proposed model derived and verified in Sections II and III, respectively, Section IV reveals the effects of C_{in} and C_{out} based on simulation and experimental results. It is revealed that the insufficiency in terminal capacitances will result in higher critical switching frequency, and C_{in} has stronger influence on critical switching frequency than C_{out}. The set of converters discussed in this paper is limited to two-phase ReSC converters with a single augmenting inductor at the output that can achieve full soft-charging operation.

II. General Output Impedance Model of ReSC Converters With Finite Terminal Capacitances

In a general circuit state (or phase) k, a two-phase ReSC converter can be modeled as the equivalent circuit shown in Fig. 3 consisting of an equivalent resistance R_k, an equivalent capacitance C_k and an augmenting inductor L at the output. Note that this general expression is able to capture any arbitrary ReSC topologies with a single inductor at the output that can achieve full soft-charging operation with (topology-dependent) equivalent R_k and C_k values. With nonideal input, two cases should be considered. Figs. 3(a) and (b) illustrate the equivalent circuits for the cases when the input terminal is connected to the source and when it is grounded, respectively.

Since the complete model shown in Fig. 3 is a third-order circuit that is difficult to handle, it has to be simplified to be practically useful. Due to the existence of the parasitic source inductance $L_{\text{par(in)}}$ (e.g. the parasitic inductance on the source cable) and the high switching frequency of ReSC converters, the input current ripple is typically sufficiently small so that we can regard the the source as an ideal constant current source I_{in}. Similarly, since the output voltage ripple of ReSC converters are typically designed to be small compared to the average DC output voltage, the current through the resistive load can also be viewed as an ideal constant current source I_{out}. In fact, some loads are intrinsically inductive and behave like a constant current source. Therefore, for simplicity (and as conventionally done in topology analysis), the third-order complete circuit model shown in Fig. 3 can be simplified as the second-order model illustrated in Fig. 4. A similar approach [19] has been used to model pure SC converters with finite terminal capacitances.

As explained in [4], ReSC converters are typically designed to be highly underdamped ($\frac{R}{2}\sqrt{\frac{C}{L}} \ll 1$, i.e. with high quality factor Q) so that they can reach the fast switching limit (FSL) impedance at much lower switching frequency compared to pure SC converters with the same R and C parameters. Therefore, in the following analysis, we assume that the ReSC converter is underdamped in both phases. Thus, in phase k of the simplified circuit model shown in Fig. 4, the inductor current i_k can be expressed as

$$i_k(t) = A_k e^{-\alpha_k t}\cos(\omega_k t + \varphi_k) + I_{\text{f}k} \tag{1}$$

where A_k is the amplitude, α_k is the decay rate, ω_k is the angular frequency, φ_k is the initial phase angle, and $I_{\text{f}k}$ is the forced DC component of i_k in phase k, which can be expressed as

$$\begin{aligned} \alpha_k &= \frac{R_k}{2L} \qquad \omega_{0k} = \frac{1}{\sqrt{LC_{k(\text{eff})}}} \\ \omega_k &= \sqrt{\omega_{0k}^2 - \alpha_k^2} \qquad I_{\text{f}k} = p_k I_{\text{out}} \end{aligned} \tag{2}$$

in which $C_{k(\text{eff})}$ is the effective capacitance and p_k is a dimensionless ratio. In the two cases illustrated in Fig. 4, for an m-to-n ReSC converter, $C_{k(\text{eff})}$ and p_k can be given as

$$\begin{aligned} &\text{Case 1 : (Phase 1)} \begin{cases} C_{k(\text{eff})} = 1 \Big/ \left(\frac{1}{C_k} + \frac{1}{C_{\text{in}}} + \frac{1}{C_{\text{out}}}\right) \\ p_k = \frac{C_{k(\text{eff})}}{C_{\text{in}} C_{\text{out}}}\left(C_{\text{in}} + \frac{n}{m} C_{\text{out}}\right) \end{cases} \\ &\text{Case 2 : (Phase 2)} \begin{cases} C_{k(\text{eff})} = 1 \Big/ \left(\frac{1}{C_k} + \frac{1}{C_{\text{out}}}\right) \\ p_k = \frac{C_{k(\text{eff})}}{C_{\text{out}}} \end{cases} . \end{aligned} \tag{3}$$

To find out the unknowns A_k and φ_k in (1), we need two additional conditions. First, since the inductor current i_k must be continuous at every switching instant, the following condition should be satisfied:

$$i_k(0) = i_{\bar{k}}(D_{\bar{k}} T) \tag{4}$$

where T is switching period, D_k is the duty ratio of phase k, and the label $\bar{k}$ is defined as

$$\bar{k} = \begin{cases} 1, & k = 2 \\ 2, & k = 1 \end{cases} . \tag{5}$$

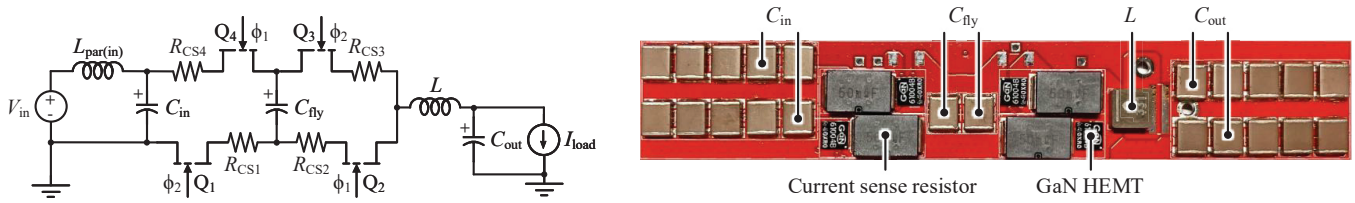


Fig. 5: 2-to-1 ReSC converter prototype. (a) Schematic drawing of the prototype. (b) Photograph of the prototype with key components annotated.

Second, according to the charge balance of the flying capacitors in the periodic steady state, the charge delivered to the output in phase k can be expressed as

$$q_k = a_k q_{\text{out}} \tag{6}$$

where

$$q_k = \int_0^{D_k T} i_k(t) \qquad q_{\text{out}} = I_{\text{out}} T \tag{7}$$

in which a_k is the ratio of the transferred charged in phase k to the total delivered charge in a switching cycle. The definition and calculation of a_k can be found in [2].

Since the resistive output impedance R_{out} accounts for all conduction losses in the ReSC converter, it can be calculated with the average conduction power loss P_{loss} as

$$R_{\text{out}} = \frac{P_{\text{loss}}}{I_{\text{out}}^2}. \tag{8}$$

Note that P_{loss} is the power loss averaged in one switching cycle and thus can be expressed as the summation of the energy losses over all phases:

$$P_{\text{loss}} = f_{\text{sw}} \sum_k E_k \tag{9}$$

where f_{sw} is the switching frequency and E_k represents the conduction energy loss in phase k which can be expressed as

$$E_k = \int_0^{D_k T} R_k i_k^2(t)\, dt. \tag{10}$$

By substituting (1) into (4) and (6), we can find the unknowns A_k and φ_k and thus the explicit expression of i_k. Then, substituting i_k into (8)-(10) yields

$$R_{\text{out}} = \sum_{k=1,\,2} \left[\hat{R}_k + R_k p_k \left(2a_k - D_k p_k\right) \right] \tag{11}$$

where

$$\begin{aligned} \hat{R}_k =& R_k \cdot \frac{\left[\left(a_k - D_k p_k\right)\omega_{0k}\right]^2}{16 f_{\text{sw}}} \cdot \\ & \frac{\left(G_k - H_{k2}\right) T_k^2 + 2H_{k1} T_k + \left(G_k + H_{k2}\right)}{\left(M_{k1} T_k + M_{k2}\right)^2} \end{aligned} \tag{12}$$

and

$$\beta_k = \frac{D_k \alpha_k}{f_{\text{sw}}} \quad \gamma_k = \frac{D_k \omega_k}{f_{\text{sw}}} \quad G_k = \frac{\omega_{0k}^2}{\alpha_k}\left(e^{2\beta_k} - 1\right)$$

$$\begin{cases} M_{k1} = \omega_k \left[\cos(\gamma_k) - e^{\beta_k}\right] + \alpha_k \sin(\gamma_k) \\ M_{k2} = \omega_k \sin(\gamma_k) - \alpha_k \left[\cos(\gamma_k) - e^{\beta_k}\right] \end{cases}$$

$$\begin{cases} H_{k1} = \omega_k \left[\cos(2\gamma_k) - e^{2\beta_k}\right] + \alpha_k \sin(2\gamma_k) \\ H_{k2} = \omega_k \sin(2\gamma_k) - \alpha_k \left[\cos(2\gamma_k) - e^{2\beta_k}\right] \end{cases}$$

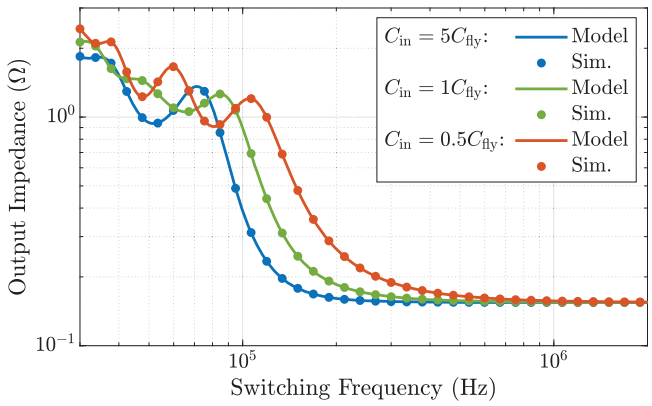
$$\begin{cases} P_{k1} = e^{-\beta_{\bar{k}}} + \left[\dfrac{\alpha_{\bar{k}}}{\omega_{\bar{k}}} \sin(\gamma_{\bar{k}}) - \cos(\gamma_{\bar{k}})\right] \\ P_{k2} = e^{\beta_{\bar{k}}} - \left[\dfrac{\alpha_{\bar{k}}}{\omega_{\bar{k}}} \sin(\gamma_{\bar{k}}) + \cos(\gamma_{\bar{k}})\right] \\ P_{k3} = \dfrac{4\left(p_k - p_{\bar{k}}\right) f_{\text{sw}} \left[\cosh(\beta_{\bar{k}}) - \cos(\gamma_{\bar{k}})\right]}{\left(a_k - D_k p_k\right)\omega_{0k}^2} - \\ \qquad \dfrac{\left(a_{\bar{k}} - D_{\bar{k}} p_{\bar{k}}\right)\omega_{0\bar{k}}^2}{\left(a_k - D_k p_k\right)\omega_{0k}^2} \cdot \dfrac{\sin(\gamma_{\bar{k}})}{\omega_{\bar{k}}} \end{cases} \tag{13}$$

$$T_k = \frac{P_{k1}\cos(\gamma_k) + e^{\beta_k} P_{k2} + P_{k3} M_{k2}}{P_{k1}\sin(\gamma_k) - P_{k3} M_{k1}}.$$

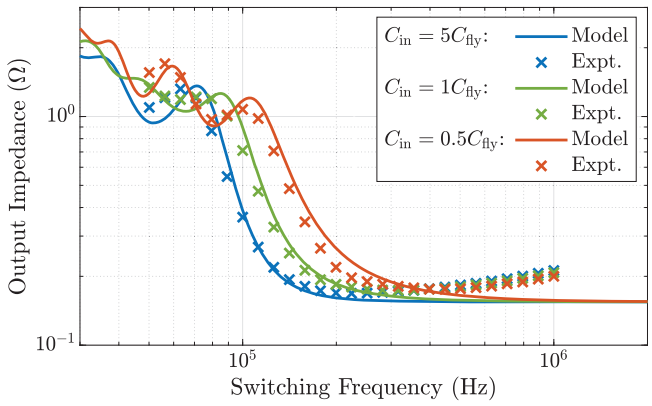
III. Model Verification

To verify the accuracy of the proposed output impedance model, we compare the modeling results with circuit simulations and experimental measurements from a 2-to-1 ReSC converter prototype as shown in Fig. 5 with the flying capacitance $C_{\text{fly}} = 3.76$ μF, effective output inductance $L = 388.9$ nH (including parasitic inductance), GaN HEMT on-state resistance $R_{\text{ds(on)}} = 16$ mΩ, and current sense resistance $R_{\text{CS}} = 50$ mΩ. The high-precision current sense resistors are added to dominate the branch resistance against the variation in the $R_{\text{ds(on)}}$ of the GaN HEMTs [20].

Figs. 6 and 7 present the comparison between the output impedances predicted by the proposed model (Model), simulated with PLECS (Sim.), and measured from the prototype (Expt.) with various C_{in} and C_{out}. As can be seen in Figs. 6 and 7, the modeling results match well with the simulated and experimental results within a wide range of switching frequency, including the oscillating R_{out} curves at low switching frequency. This demonstrates that the proposed model is able to accurately capture the effects of finite terminal capacitances. As the switching frequency increases, the switching loss in

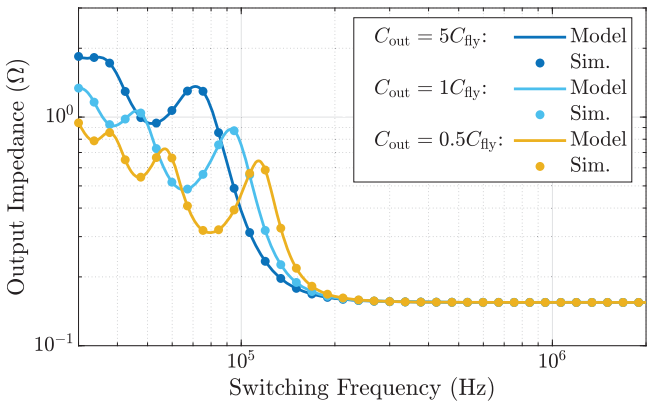


(a)

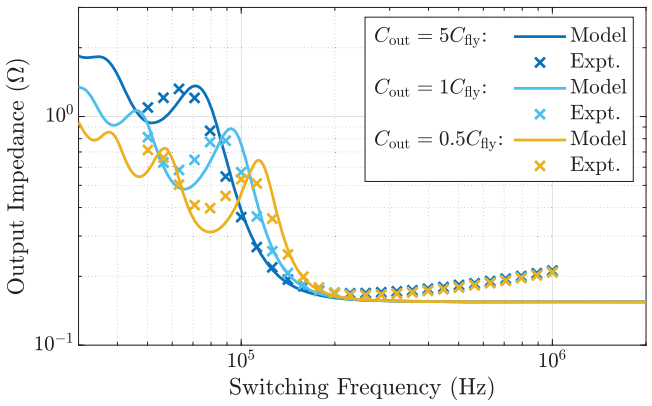


(b)

Fig. 6: Output impedance of the converter with various C_{in}. ($C_{out} = 5C_{fly}$) (a) Comparison between the output impedances predicted by the proposed model (Model) and simulated with PLECS (Sim.). (b) Comparison between the output impedances predicted by the proposed model (Model) and measured from the prototype (Expt.).



(a)



(b)

Fig. 7: Output impedance of the converter with various C_{out}. ($C_{in} = 5C_{fly}$) (a) Comparison between the output impedances predicted by the proposed model (Model) and simulated with PLECS (Sim.). (b) Comparison between the output impedances predicted by the proposed model (Model) and measured from the prototype (Expt.).

the prototype becomes higher and higher. Since the proposed model can capture only conduction loss but no switching loss in the converter, the modeling results will deviate from the experimental results in the high frequency region.

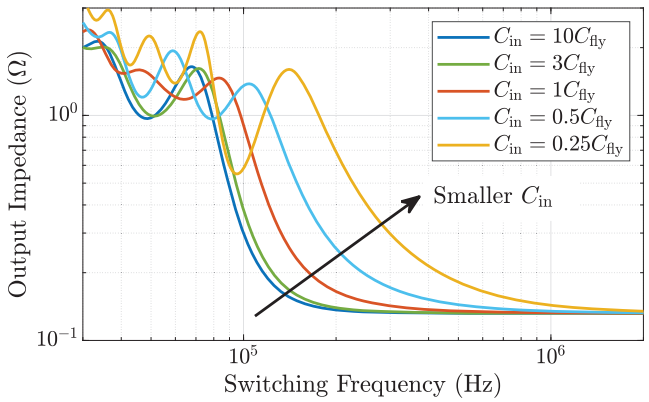
IV. Effect Analysis of Finite Terminal Capacitances

With the general output impedance model derived and verified in Sections II and III, we can now use it to explore the effects of finite terminal capacitances on the output impedance of ReSC converters. In this section, the 2-to-1 ReSC converter mentioned in Section III is used as an example to investigate the effects of C_{in} and C_{out}.

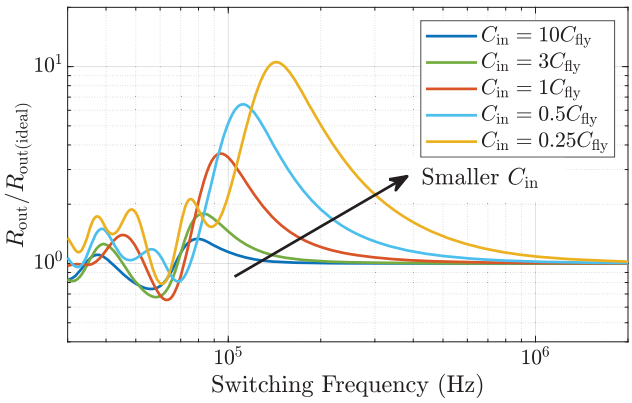
Figs. 8 and 9 show the effects of C_{in} and C_{out} on the output impedance of the 2-to-1 ReSC converter, where Figs. 8(a) and 9(a) present the output impedance curves with various C_{in} and C_{out}, and Figs. 8(b) and 9(b) show how much R_{out} is changed with respect to the output impedance with ideal input and output $R_{out(ideal)}$.

1) Effect of C_{in}. As can be seen in Fig. 8(a), with smaller C_{in}, the knee of the output impedance curve will shift to the right, meaning that the critical switching frequency becomes higher. This indicates that higher switching frequency is required to reach the FSL impedance due to the insufficiency of C_{in}. Since higher switching frequency typically leads to higher switching loss and lower overall efficiency, this effect is undesired and should be avoided in converter design by using sufficient C_{in} to ensure nearly ideal input behavior.

Additionally, we can see that C_{in} has stronger influence on the critical switching frequency than C_{out}. Table I presents a quantitative comparison of the output impedance at the intrinsic critical frequency with different terminal capacitances. Here, we define the intrinsic critical frequency of the 2-to-1 ReSC converter as $f_{crit(int)} = \frac{1}{2\pi\sqrt{LC_{fly}}} = 132$ kHz. It is called *intrinsic* because it is not related to the terminal capacitances and determined only by the primary passive components (i.e. L and C_{fly}). As can be seen in Table I, R_{out}

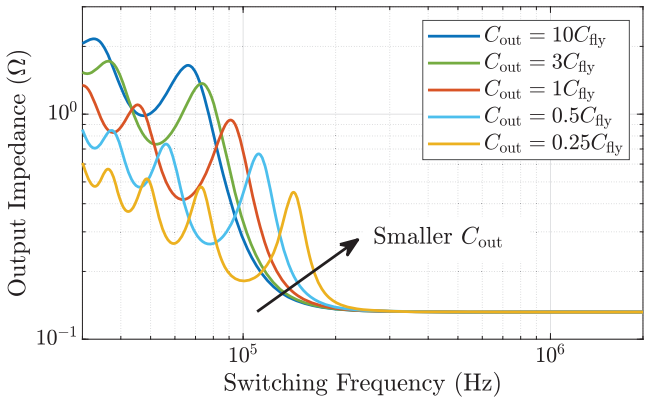


(a)

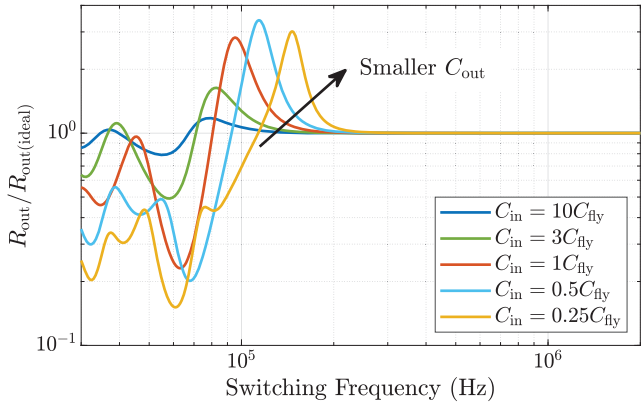


(b)

Fig. 8: Effect of C_{in} on output impedance. ($C_{\text{out}} = 10C_{\text{fly}}$) (a) R_{out} with various C_{in}. (b) Ratio of R_{out} to the output impedance with ideal input and output $R_{\text{out(ideal)}}$.



(a)



(b)

Fig. 9: Effect of C_{out} on input impedance. ($C_{\text{in}} = 10C_{\text{fly}}$) (a) R_{out} with various C_{out}. (b) Ratio of R_{out} to the output impedance with ideal input and output $R_{\text{out(ideal)}}$.

TABLE I: Comparison of the output impedance at the intrinsic critical frequency ($f_{\text{crit(int)}} = 132$ kHz) with different terminal capacitances

No.	$C_{\text{in}}/C_{\text{fly}}$	$C_{\text{out}}/C_{\text{fly}}$	Calculated R_{out} (mΩ)	Measured R_{out} (mΩ)
1)	5	5	201.3	209.5
2)	1	5	326.3	300.3
3)	0.5	5	732.9	621.5
4)	5	1	235.9	238.7
5)	5	0.5	358.9	316.0

will increase by roughly a factor of 3 when C_{in} is reduced from $5C_{\text{fly}}$ to C_{fly}, while R_{out} will increase by only a factor of 1.5 when C_{out} is reduced from $5C_{\text{fly}}$ to C_{fly}.

2) Effect of C_{out}. As we can see in Fig. 9(a), in contrast to C_{in}, C_{out} shows greater influence on the output impedance in the low frequency region, where smaller C_{out} helps reduce output impedance. This should be a favorable feature since decreasing C_{out} will contribute to both higher efficiency and higher power density. However, since the ReSC converters typically operate above resonance, this phenomenon is hard to utilize for performance improvement in practice.

It can also be seen that smaller C_{out} will lead to higher critical switching frequency, meaning that higher switching frequency will be required to reach the FSL impedance if C_{out} becomes smaller, although C_{out}'s effect on the critical switching frequency is quantitatively weaker than that of C_{in}.

To shrink the sizes of terminal capacitors without harming the efficiency of ReSC converters, we can adjust the duty ratio and switching frequency to compensate for the negative effects of finite terminal capacitances [21].

V. Conclusions

This paper proposes a general modeling and analysis methodology to capture the effect of finite terminal capacitances on the output impedance of ReSC converters. A general output impedance model is derived and verified by circuit simulations and experimental measurements from a 2-to-1 ReSC converter prototype. It is revealed that the insufficiency in terminal capacitances will result in higher critical switching frequency, and C_{in} is quantitatively more influential on the critical switching frequency than C_{out}.

References

[1] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," in *Proceedings of PESC '95 - Power Electronics Specialist Conference*, vol. 2, 1995, pp. 1215–1221 vol.2.

[2] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, March 2008.

[3] R. C. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 4008–4015.

[4] Y. Lei and R. C. N. Pilawa-Podgurski, "A General Method for Analyzing Resonant and Soft-Charging Operation of Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650–5664, 2015.

[5] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and Comparison of Passive Component Volume of Hybrid Resonant Switched-Capacitor Converters," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–8.

[6] Y. Yuanmao and K. W. E. Cheng, "Level-Shifting Multiple-Input Switched-Capacitor Voltage Copier," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 828–837, 2012.

[7] Y. Hinago and H. Koizumi, "A Switched-Capacitor Inverter Using Series/Parallel Conversion With Inductive Load," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 878–887, 2012.

[8] Y. Hsieh, J. Chen, T. Liang, and L. Yang, "Novel High Step-Up DC–DC Converter With Coupled-Inductor and Switched-Capacitor Techniques," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 998–1007, 2012.

[9] W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu, "Analysis and Comparison of Medium Voltage High Power DC/DC Converters for Offshore Wind Energy Systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 2014–2023, 2013.

[10] E. Babaei and S. S. Gowgani, "Hybrid Multilevel Inverter Using Switched Capacitor Units," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4614–4621, 2014.

[11] B. Saha and R. Kim, "High Power Density Series Resonant Inverter Using an Auxiliary Switched Capacitor Cell for Induction Heating Applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1909–1918, 2014.

[12] G. Wu, X. Ruan, and Z. Ye, "Nonisolated High Step-Up DC–DC Converters Adopting Switched-Capacitor Cell," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 383–393, 2015.

[13] A. Ajami, H. Ardi, and A. Farakhor, "A Novel High Step-up DC/DC Converter Based on Integrating Coupled Inductor and Switched-Capacitor Techniques for Renewable Energy Applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4255–4263, 2015.

[14] K. Kesarwani and J. T. Stauth, "Resonant and multi-mode operation of flying capacitor multi-level DC-DC converters," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2015, pp. 1–8.

[15] S. R. Pasternak, M. H. Kiani, J. S. Rentmeister, and J. T. Stauth, "Modeling and Performance Limits of Switched-Capacitor DC–DC Converters Capable of Resonant Operation With a Single Inductor," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1746–1760, 2017.

[16] C. Schaef, J. Rentmeister, and J. T. Stauth, "Multimode Operation of Resonant and Hybrid Switched-Capacitor Topologies," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 512–10 523, 2018.

[17] J. S. Rentmeister and J. T. Stauth, "Bypass capacitance and voltage ripple considerations for resonant switched capacitor converters," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2017, pp. 1–8.

[18] Y. Lei, W.-C. Liu, and R. C. N. Pilawa-Podgurski, "An Analytical Method to Evaluate and Design Hybrid Switched-Capacitor and Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2227–2240, 2018.

[19] Y. Zhu, Z. Ye, and R. C. N. Pilawa-Podgurski, "Modeling and Analysis of Switched-Capacitor Converters with Finite Terminal Capacitances," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 178–185.

[20] T. Foulkes, T. Modeer, and R. C. N. Pilawa-Podgurski, "Quantifying Dynamic On-State Resistance of GaN HEMTs for Power Converter Design via a Survey of Low and High Voltage Devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, to be published. doi:10.1109/JESTPE.2020.3024930.

[21] Y. Zhu, Z. Ye, T. Ge, and R. C. N. Pilawa-Podgurski, "Multi-Resonant Compensation Control for Terminal Capacitance Reduction in Resonant Switched-Capacitor Converters," in *2021 IEEE 22nd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2021.