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Oxide Semiconductor Thin-Film Transistors for Sustainable Electronics

A Dissertation submitted in partial satisfaction of the requirements

for the degree of Doctor of Philosophy

in

Electrical Engineering (Nanoscale Devices and Systems)

by

Chi-Hsin Huang

Committee in charge:

Professor Kenji Nomura, Chair
Professor Prabhakar Bandaru
Professor Shadi Dayeh
Professor Eric Fullerton
Professor Oscar Vazquez Mena

2024

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University of California San Diego

2024

DEDICATION

To my family

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PUBLICATIONS

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22. **C.-H. Huang**, Y. Zhang and K. Nomura* Reconfigurable Artificial Synapses with Excitatory and Inhibitory Response Enabled by an Ambipolar Oxide Thin-Film Transistor. *ACS Applied Materials & Interfaces* 14, 22252-22262 (2022).
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FIELD OF STUDY

Major Field: Electrical Engineering (Nanoscale Devices and Systems)

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Professor Kenji Nomura

ABSTRACT OF THE DISSERTATION

Oxide Semiconductor Thin-Film Transistors for Sustainable Electronics

by

Chi-Hsin Huang

Doctor of Philosophy in Electrical Engineering (Nanoscale Devices and Systems)

University of California San Diego, 2024

Professor Kenji Nomura, Chair

The design and development of future electronics must incorporate sustainable design principles throughout the process, including the use of emerging materials, low-power operations, and environmentally friendly manufacturing practices. The objectives of the thesis are to develop oxide semiconductors and devices that pave the way to revolutionize future sustainable electronic applications, including large-area flexible integrated circuits, back-end-

of-line (BEOL) electronics in monolithic 3D integration for CMOS, and emerging computing devices for non-traditional computing platforms.

Amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors have been successfully commercialized in the flat panel display industry. The next significant challenge in oxide semiconductor technology lies in the development of high-performance *p*-channel oxide thin-film transistors, as their absence currently hinders the progress of low-power oxide complementary metal-oxide semiconductor (CMOS) circuits. Overcoming this challenge is crucial for realizing future cost-effective, energy-efficient, and flexible oxide circuit applications. Part I of this dissertation emphasizes the development of high-performance *p*-channel oxide TFTs, including material design, defect termination techniques, and atomically thin oxide semiconductor development. In Chapter 2, we introduce a scalable liquid element treatment technique to address structural defects in *p*-type SnO, particularly oxygen and metal cation vacancies. This technique contributes to enhancing the performance of *p*-channel SnO TFTs. Additionally, leveraging the liquid Bi-Sn eutectic alloy system allows us to control Sn cation treatment at a low temperature of approximately 140°C. This capability facilitates the modulation of hole concentration and a wide range of threshold voltage adjustments for *p*-channel SnO TFTs. In Chapter 3, we develop high-performance *p*-channel oxide TFTs using atomically thin *p*-type tin monoxide (SnO) channels with a thickness of approximately 1 nm, exhibiting extremely low off-current suitable for low-power oxide CMOS circuits.

Exploring new ultra-widegap oxide materials with a bandgap larger than the current commercialized a-IGZO holds promise for reducing TFT off-current and decreasing power

consumption. Part II of this dissertation explores new oxide channel materials for low-temperature processed, high-mobility, and wide-bandgap oxide TFTs. In Chapter 4, we introduced a pressure-assisted liquid-metal printing technique that enables low-temperature crystallization of β -Ga₂O₃ for wide bandgap and high-performance *n*-channel oxide TFTs with a high saturation mobility of $\sim 11 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

Research into new computing devices and systems based on novel computing concepts, rather than traditional digital computers, is an important direction for developing future energy-efficient and sustainable computing. Oxide TFTs also show the potential to be essential building blocks for next-generation analog neuromorphic computing systems. Part III of this dissertation focuses on investigating oxide TFTs as emerging computing devices for non-traditional computing platforms. In Chapter 5, we designed the low-temperature processed ambipolar SnO-based TFT to demonstrate dynamic reconfigurable excitatory and inhibitory synaptic responses in a single synaptic device, emulating complex biological functions in emerging neuromorphic hardware. In Chapter 6, we introduced a novel gate-tunable memristor, referred to as a memtransistor, which utilizes non-layer two-dimensional (2D) oxide semiconductor material, specifically SnO₂. The memtransistor combines memristor and transistor functionalities to advance next-generation nonvolatile computing technology. We successfully demonstrated that the gate-tunable synaptic device dynamically modulated analog switching behavior with good linearity and improved conductance change ratio for high recognition accuracy learning.

Finally, the remaining challenges and opportunities in oxide semiconductors and devices for future advanced electronics are discussed.

Chapter 1 Introduction

1.1 Introduction of Oxide Semiconductors

Metal oxides, abundant constituents of the Earth's crust and key components in traditional ceramics, exhibit remarkable distinctions from conventional inorganic semiconductors like silicon and III–V compounds. These distinctions encompass various aspects, including materials design principles, electronic structures, charge transport mechanisms, defect states, thin-film processing, and optoelectronic characteristics. As a result, metal oxide semiconductors open doors to both conventional and novel functionalities.

Oxide semiconductors have gained significant attention due to their capacity to deliver excellent optical and electrical properties, a wide range of bandgaps, scalability for large-area production, exceptional mechanical flexibility, and adaptability for integration into nanoscale devices. Notably, a key advantage of oxides is that they offer an exceptional and innovative combination of multifunctional properties not achieved by other material classes. The attractiveness of metal oxide electronic materials stems from their versatility, offering a wide array of potential applications that span from thin films to nanostructures. These applications have seen increasing importance in fields such as transparent and flexible electronics, optoelectronics, magnetoelectronics, photonics, spintronics, thermoelectrics, piezoelectrics, power harvesting, and energy storage.

Recent advancements in oxide semiconductors for electronics have yielded significant breakthroughs. These include the discovery and characterization of novel transparent conducting

oxides, the realization of p -type oxide semiconductors along with traditional n -type counterparts for transistors, p - n junctions, and complementary circuits. Additionally, the development of printable and flexible electronics using metal oxides. Most importantly, amorphous oxide semiconductors have been commercialized for flat panel displays.

1.2 Introduction of Oxide Thin-Film Transistors

The commercial use of thin-film transistors (TFTs) in liquid-crystal display applications began over 30 years ago. TFT technology offers several key advantages over traditional silicon complementary metal–oxide–semiconductor (CMOS) transistors. These advantages include the ability to manufacture TFTs on large substrates at a low cost per unit area and at low processing temperatures, allowing for direct integration onto various flexible substrates. Recently, there has been a significant effort to explore new materials and fabrication techniques aimed at enhancing performance, reducing manufacturing costs, and enabling new functionalities.

Currently, the main thin-film transistor (TFT) technologies used in consumer electronics are amorphous silicon (a-Si), low-temperature polycrystalline silicon (LTPS), and amorphous metal-oxide semiconductors, primarily amorphous indium–gallium–zinc–oxide (a-IGZO). Among them, amorphous oxide semiconductors, particularly a-IGZO, have emerged as a promising class of materials for thin-film transistors (TFTs), and they have made remarkable progress, especially in display applications, challenging silicon not only in traditional applications but also opening doors to next-generation applications fields like paper electronics, wearable electronic, flexible ICs. The amorphous oxide semiconductors TFTs can be manufactured at low process temperatures ($<400\text{ }^{\circ}\text{C}$) while still offering charge carrier mobility levels close to or exceeding $10\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ^[1], which is a significant improvement compared to the mobility of a-Si TFTs ($0.5\text{--}1\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$)^[2-3]. LTPS TFTs require higher process temperatures and a more complex manufacturing process, resulting in both *p*-type and *n*-type TFTs with even higher mobilities (ranging from 50 to $100\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$)^[2-3].

These amorphous oxide semiconductors represent a revolutionary idea and offer a compelling combination of high optical transparency, high electron mobility, and amorphous microstructure. Additionally, amorphous oxide semiconductors lack grain boundaries, eliminating a primary limitation of mobility in polycrystalline semiconductors and making them highly advantageous for process integration. One of the most crucial aspects is using low-temperature deposition techniques for oxide semiconductor material growth. These techniques are particularly well-suited for the thermal requirements of various flexible substrates^[4] and the back-end-of-line (BEOL) processes in monolithic CMOS integration^[5]. This new technology is also sustainable, environmentally friendly, and cost-effective, making it an attractive alternative to conventional silicon technology.

1.3 Historical Overview of Oxide Thin-Film Transistors

The history of TFTs spans more than 80 years, establishing it as one of the oldest narratives in the realm of electronic devices. The origins of TFTs can be traced back to 1925, when they were first conceptualized and subsequently patented in 1930 by J.E. Lilienfeld and O. Heil.^[3] It is crucial to emphasize that knowledge about semiconductor materials and the requisite vacuum techniques for thin-film fabrication was limited during this era. As a result, these early reports primarily constituted concept patents, lacking concrete evidence of actual device production. Nevertheless, even within these initial patents, the fundamental concept of controlling current flow within a material through the influence of a transverse electrical field was already present.

Oxide semiconductor TFTs boast a rich history akin to that of Silicon Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs). Notably, in the 1960s, there were pioneering investigations into the field effects governing current modulation in thin films composed of materials such as SnO_2 , In_2O_3 , and ZnO , which serve as representative transparent oxide conductors. After 2000, extensive reexamination of ZnO TFTs occurred, involving multiple research groups. Notably, in 2001, Ohya et al. published a seminal paper on ZnO TFTs, which were fabricated using a non-vacuum process that entailed the application of a chemical solution *via* drop-coating followed by heating in air.^[6] This marked a groundbreaking moment as the first instance of oxide TFTs produced through non-vacuum methods. One distinctive feature of oxide semiconductors lies in their chemical stability when exposed to ambient atmospheres at elevated temperatures, unlike their conventional semiconductor counterparts. This inherent property has since become a cornerstone of ongoing research efforts toward solution-derived oxide TFTs. In addition, numerous papers have been published on ZnO TFTs deposited through techniques like

sputtering or pulsed-laser deposition.^[7] Nevertheless, various challenges have been observed, including poor reproducibility and significant hysteresis, attributed mainly to the intricate characteristics of grain boundaries.

In 1996, a design concept and various examples of amorphous oxide semiconductors with high electron mobility were proposed^[8]. In the realm of TFTs with amorphous oxides, a study conducted by Adkins et al. in 1993 examined field modulation on amorphous InO_x with low current on/off ratio of 2–3.^[9] This low ratio is attributed to a high carrier concentration, and efforts to suppress carrier concentrations and stabilize a low carrier state in amorphous InO_x continue to be a challenge. However, in 2004, high-performance amorphous oxide semiconductor TFTs were reported for IGZO.^[11] Since then, various amorphous oxide semiconductor TFTs have been reported.^[9-10]

The remarkable success of *n*-type oxide semiconductors and their application in TFTs has spurred interest in exploring *p*-type oxide-based semiconductors for TFTs. However, progress in the development of *p*-channel oxide semiconductor TFTs has been slower, and to date, there are no reports of *p*-type oxide TFTs matching the performance of their *n*-type counterparts. Despite numerous reports on *p*-type transparent oxide semiconductors like Cu₂O dating back to 1997^[11], none have exhibited the performance characteristics expected of an ideal TFT.^[12] Until 2008, *p*-channel oxide TFTs were first successfully demonstrated using SnO thin film.^[13] Subsequently, in 2011, complementary metal-oxide semiconductors (CMOSs) were introduced, capitalizing on the ambipolar nature of SnO.^[14] Nonetheless, the performance of SnO TFTs remains inadequate for

practical applications.^[12] The main limitation of *p*-type oxide TFTs lies in the relatively low hole mobilities compared to *n*-type oxide semiconductors.

1.4 Emerging Needs for Oxide Semiconductor Devices

Since the invention of IGZO-based n -channel oxide TFTs, oxide semiconductor device technology has been widely accepted as promising to advance large-area microelectronics from rigid to soft substrates. So far, several state-of-the-art active-matrix flat-panel displays (AMFPDs), such as large-sized and high-resolution liquid crystal displays (AML-CDs) and active-matrix organic light-emitting diodes (AMOLEDs); flexible displays; and micro-LED displays have been successfully developed by adapting IGZO TFT backplanes. Beyond their use in display applications, metal oxide semiconductors are promising choices for developing advanced materials with low-temperature processes that pave the way to revolutionize new electronic applications such as low-power internet-of-thing (IoT) devices, wearable electronic sensors, electronic skin, energy harvesting, and BEOL-compatible transistors for three-dimensional integration.^[2, 13, 15]

1.4.1 Large-Area Flexible Integrated Circuits

Oxide-based integrated circuits have the exciting potential to be fabricated on large, ultrathin, flexible, and stretchable substrates, creating lightweight, flexible, and wearable electronics. These large-area flexible oxide circuits can be folded, rolled, or crumpled without compromising their electronic functionality. As a result of these features, oxide TFTs could be a game-changer for wearable electronics across a variety of applications. A variety of large-area circuits based on oxide TFT technology have already been successfully demonstrated, spanning from radiofrequency identification tags^[16-17], near-field communication tags^[18-19], and analog-to-digital converters^[20] to microprocessors.^[21] These applications have been implemented on both rigid and flexible substrates. Furthermore, innovative device attributes such as transparency,

conformability, biocompatibility, and biodegradability pave the way for an increasing range of applications in diverse technology sectors, including IoT systems, wearable electronic sensors, electronic skin, and medical and healthcare applications.^[4, 15]

Furthermore, the potential to substitute the vacuum processing approach with higher-throughput processes is particularly appealing, especially for large-area and cost-effective applications, including printable displays, electronic sensor systems, and disposable smart labels. In this regard, a fundamental advantage of oxide TFT technologies lies in their compatibility with solution-based processing and additive manufacturing methods like printing, which can potentially reduce overall costs.^[22-24]

1.4.2 Back-End-of-Line Electronics in Monolithic 3D Integration

The semiconductor industry is currently facing huge challenges for further transistor miniaturization due to the physical limitations of Si CMOS technology. Considering the increasingly demanding, incremental, and costly advancements of the technology required to extend Moore's law, it is crucial to consider whether the industry will be able to sustain its growth trajectory. Three-dimensional (3D) monolithic integration technology is being proposed as one of the potential technologies to overcome the issues of power–performance–area–cost and to continue the ever-demanding downscaling of Si CMOS.^[25-27]

To achieve 3D monolithic integration, the top-layer transistors in this architecture must be fabricated at a low temperature ($<400\text{ }^{\circ}\text{C}$).^[27] This is essential to prevent any degradation in the electrical performance of devices in the underlying layers. Consequently, using Si, which requires a high-temperature process to fully achieve its exceptional electrical characteristics, is unsuitable for the BEOL process transistors. As a result, there is a need to explore alternative materials with excellent electrical properties that can be achieved through low-temperature processing.

Oxide semiconductors have recently emerged as promising material systems for BEOL transistors due to their compatibility with conventional CMOS processes, such as sputtering and atomic layer deposition, achievable at low temperatures ($<400\text{ }^{\circ}\text{C}$). Additionally, they exhibit low off-current ($<10^{-18}\text{ A}\mu\text{m}^{-1}$), attributed to their large bandgap ($>3\text{ eV}$), making oxide semiconductors highly appealing for low-power device applications, thus playing a critical role in both memory and Si CMOS applications.^[26-27] However, as technology scales down, numerous unknown aspects of oxide TFTs in scaled dimensions, including carrier transport, electrical contact

properties, and short-channel effects, require extensive research. Moreover, the availability of oxide CMOS TFT technology is crucial for diverse BEOL device applications. Unfortunately, the most challenging obstacle in oxide TFT technology remains the development of *p*-type oxide semiconductors, which must be addressed to expand the potential applications of oxide TFT technology.

1.4.3 Prospects for Oxide Semiconductor Devices

To meet the emerging needs of oxide semiconductor devices, several critical challenges and future research directions must be addressed:

- (a) High-performance *p*-channel oxide TFTs: Developing *p*-type oxide semiconductors with high mobility is a key requirement to enable the creation of oxide complementary circuits with high energy efficiency for various circuit applications. This stands as the most significant challenge in oxide TFT technology, as it is essential to unlock the advantages and potential of oxide semiconductors fully.
- (b) Low-temperature processed, high-mobility, and wide-bandgap oxide TFTs: While amorphous IGZO-TFTs are widely used in flat-panel displays, there is a growing demand for higher mobility oxide TFTs in integrated circuit applications, such as flexible electronics and BEOL devices. Exploring new ultra-widegap oxide materials with a bandgap larger than the current a-IGZO holds promise for reducing TFT off-current and decreasing power consumption. Furthermore, it is crucial to investigate innovative low-temperature semiconductor device fabrication processes that not only cut production costs but also minimize the environmental impact of electronic devices, contributing significantly to the development of sustainable electronics.

(c) Oxide TFTs for new computing technology: Research into new computing devices and systems based on novel computing concepts, rather than traditional digital computers, is an essential direction for developing future energy-efficient and sustainable computing. Oxide TFTs also show the potential to be essential building blocks for next-generation analog neuromorphic computing systems.

1.5 Developing *p*-type Oxide Thin-Film Transistors for Oxide Complementary Circuits

The rapid advances of *n*-type oxide semiconductors such as IGZO, ZTO, ZnO, and In₂O₃ are pushing forward the realization of high-performance oxide TFTs. However, lacking high-performance *p*-type oxide semiconductors limits many potential oxide-based electronic applications. Thus, the next major challenge faced in oxide semiconductor technology is to develop *p*-type oxide semiconductors with similar performance to their *n*-type counterparts to realize the CMOS circuits for future cost-effective, energy-efficient, wearable, and flexible oxide circuit applications. Compared to unipolar transistors, the CMOS circuit holds many advantages, including low power consumption, low waste-heat generation, high noise margin, high logic swing output, high circuit-integration density, and architectural simplicity.

Figure 1.1 illustrates the progress of mobility for oxide TFTs over the years. Since the initial report of a-IGZO-TFTs with mobility of about 6–8 cm²/V¹s⁻¹ in 2004^[1], significant efforts have been made to enhance TFT mobility, primarily through the development of new channel materials using the engineering of the chemical composition. Notable channel materials, such as amorphous In-Sn-Zn-O (a-ITZO), amorphous In-Al-Zn-O (a-IAZO), and amorphous In-Zn-O (a-IZO), have demonstrated higher TFT mobility compared to IGZO TFTs.^[28-29] In Particular, In-rich a-IZO and a-IGZO channels often show excellent TFT mobility comparable to that of LTPS TFTs. In contrast, despite more than a decade passing since the initial report in 2008 of *p*-channel SnO TFTs with a mobility of approximately 1 cm²/V¹s⁻¹,^[13] there has been minimal improvement in TFT mobility over the last ten years in the realm of *p*-channel oxide TFTs. This highlights the most significant challenge in oxide TFT technology: the absence of high-performance *p*-channel TFTs.

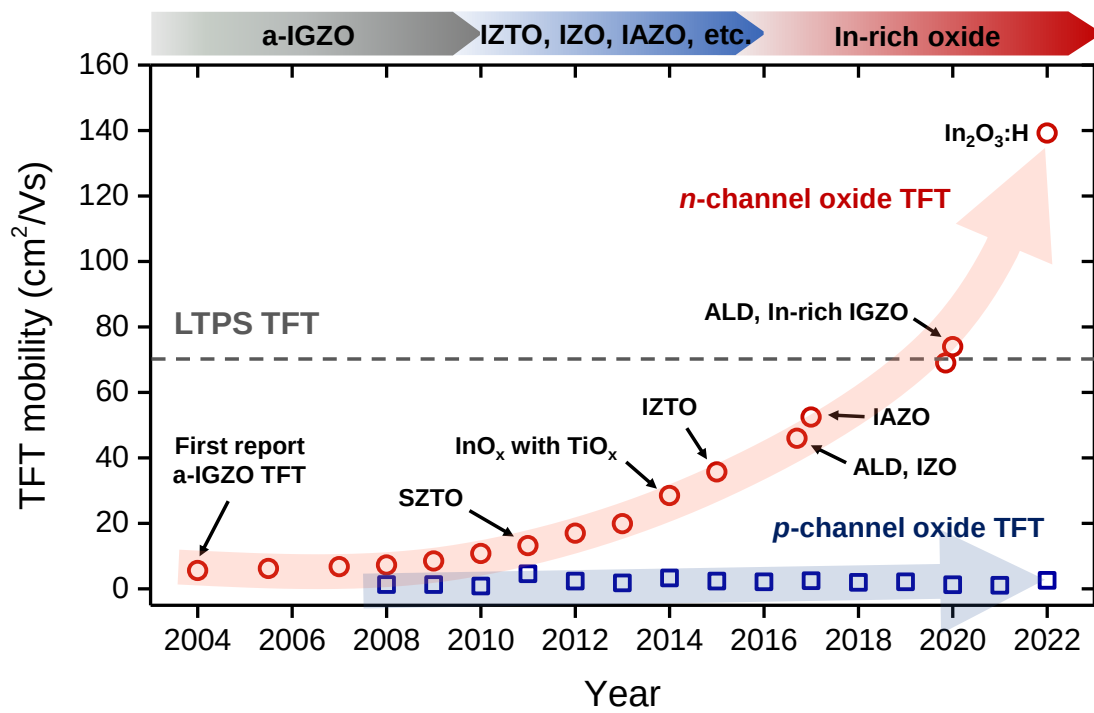


Figure 1.1 Progress of TFT mobility for oxide *n*-channel and *p*-channel oxide TFTs.

1.5.1 Challenge of *p*-type Oxide Thin-Film Transistor Development

The challenge of developing high-performance *p*-channel oxide TFTs stems from the lack of suitable *p*-type oxide semiconductors. This limitation is primarily due to the difficulties in hole doping and hole transport in oxide materials. Several factors contribute to this challenge:

- (a) The valence band maximum (VBM) is primarily composed of oxygen *2p* orbitals, making it challenging to create *p*-type conductivity.
- (b) Acceptor doping is difficult due to the relatively deep VBM energy level from the vacuum level.
- (c) High-density subgap defects, that is, in-gap defects, near the VBM cause the pinning of the Fermi level in a field-effect transistor.
- (d) Unintentional electron doping can occur through hydrogen impurities and other factors.

Additionally, substitutional doping is not yet established for ionic amorphous oxides. Based on the above reasons, hole doping and hole transport in oxide semiconductors present significant challenges, representing a major technological barrier in developing high-performance *p*-channel oxide TFTs.

Figure 1.2 illustrates the electronic structure of oxide semiconductors. In these materials, the electronic configuration is characterized by the spherical metal *ns* orbital, where ‘*n*’ represents the quantum number, contributing to the formation of the CBM. Meanwhile, the VBM predominantly comprises localized and anisotropic oxygen *2p* orbitals.^[8] The spherical nature of metal *ns* orbitals, such as Zn *4s*, In *5s*, and Sn *6s* orbitals, results in high dispersion of the CBM in materials like In₂O₃, ZnO, and SnO₂. This distinctive feature explains why many oxide semiconductors excel as *n*-type materials, offering high electron mobility, even in disordered

structures. In contrast, oxygen $2p$ orbitals do not give rise to a dissipative valence band structure due to their strong directional nature. Instead, they establish a localized pathway for hole transport. Consequently, the effective mass of holes is relatively large due to the non-dispersive VBM structure in oxide materials. Furthermore, hole transport is significantly influenced by bond angle distortions and structural defects, resulting in a susceptibility of the electrical properties to degradation in disordered structures.

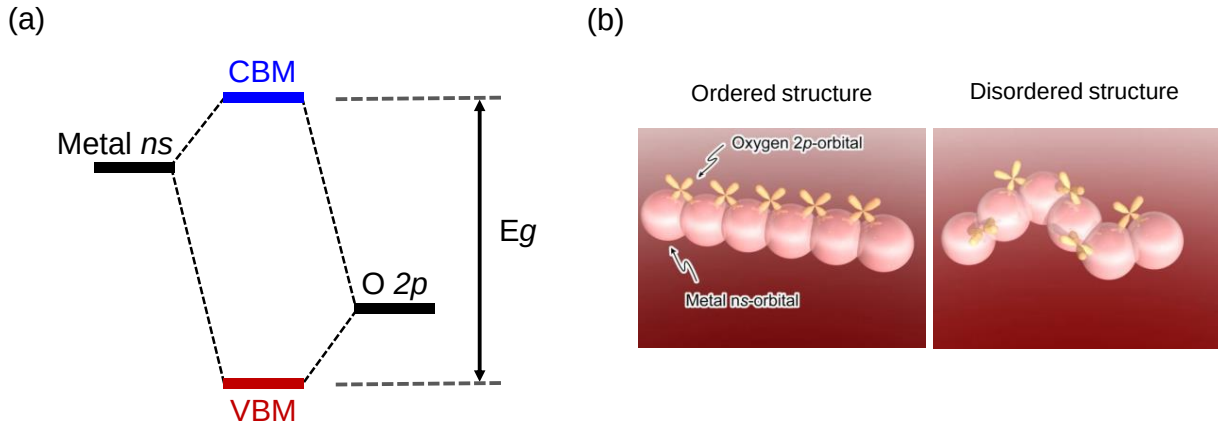


Figure 1.2 Schematic illustration of the (a) electronic structure and (b) carrier pathway for representative ionic oxide semiconductors, such as ZnO, In_2O_3 , and a-IGZO. ^[1]

Figure 1.3 illustrates the band edge energies of CBM and VBM for various semiconductor materials, including Si, Ge, III-V compounds, nitrides, and oxides. In conventional covalent semiconductors like Si, Ge, and GaAs, the CBM and VBM energy levels typically fall within the range of approximately 4–6 eV. This range allows for relatively straightforward control of *p*- and *n*-type polarity through doping. It is a well-established principle that a deep VBM energy level makes hole doping challenging, while semiconductors with shallow CBM levels face greater difficulty in electron doping. Representative oxide semiconductors such as ZnO, SnO₂, and a-IGZO have CBM energy levels around 4–5 eV, making electron doping relatively straightforward. This explains why many oxide semiconductors intrinsically exhibit *n*-type behavior. Conversely, the VBM levels in these oxides typically exceed 7 eV, indicating the difficulty of hole doping in most oxide semiconductors.

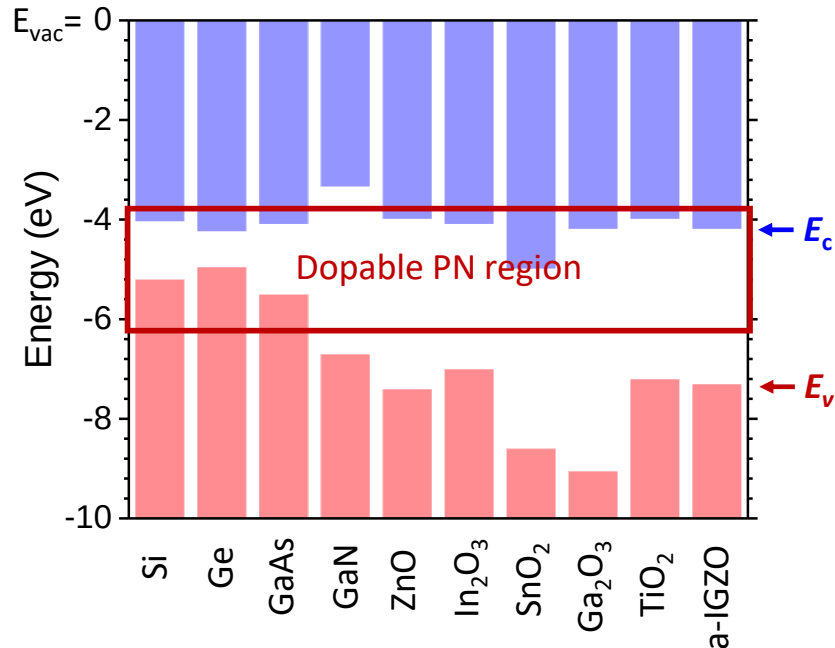


Figure 1.3 Doping energy limits for several semiconductor materials, including Si, Ge, III-V compounds, nitrides, and oxide semiconductors, with reference to the vacuum level.

Beyond the challenges related to the intrinsic electronic structure in oxide semiconductors, subgap defect states present a significant obstacle to developing high-performance *p*-type oxides (**Figure 1.4**). Many oxide semiconductors exhibit a high-density subgap defect state just above the VBM, commonly referred to as the “near-VB state.”^[30] These defect states span a broad range from the VBM to the midgap region, with an estimated density exceeding $\sim 10^{19} \text{ cm}^{-3}$. The high-density near-VB state makes hole doping difficult, resulting in the Fermi-level pinning in field-effect transistors. In such scenarios, the Fermi level in the oxide material channel becomes pinned by the subgap near-VB state, preventing the induction of free holes in the extended valence band states. Although the precise origin of this defect is not yet fully understood, it is likely attributed to factors such as oxygen vacancies and the low valence states of the metal cations in most oxide materials.^[31]

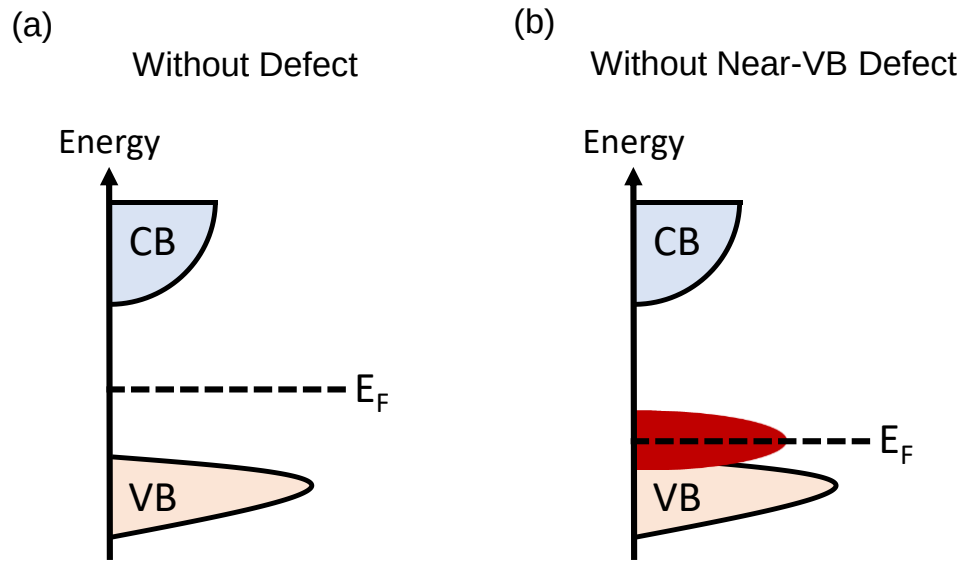


Figure 1.4 Schematics of the Fermi-level pinning caused by a near-valence band defect state.

Another significant challenge arises from the presence of hydrogen impurities, which are often considered electron donors in many oxide materials. As a result, removing impurity hydrogen from the films is crucial to achieve hole doping.^[32] However, this task is challenging because hydrogen is omnipresent, even in vacuum process chambers, and is unintentionally introduced into oxide materials. Furthermore, substitutional doping remains unconfirmed in ionic amorphous oxide semiconductors due to their structural flexibility resulting from strong ionic interactions. This issue also compounds the difficulty of controlling the material polarity of ionic amorphous oxide semiconductors. As of now, the development of *p*-type a-IGZO semiconductors has not been successful. Due to the previously discussed reasons, developing high-performance *p*-type oxide semiconductors for *p*-channel oxide TFTs remains a formidable task. As a result, the current approach in the development of *p*-channel oxide TFTs is to utilize oxide semiconductors that intrinsically exhibit *p*-type behavior, such as cuprous oxide (Cu₂O), tin oxide (SnO), nickel oxide (NiO), and others.

1.5.2 *p*-type Oxide Semiconductors: Cu₂O and SnO

Numerous *p*-type oxide materials have been discovered, including delafossite CuMO₂ (M = Al, Ga, In, Sc, Y, Cr, Fe, etc.),^[11] spinel oxide (ZnM₂O₄ [M = Co, Rh, Ir]),^[33] and perovskite systems.^[34] However, only cuprous oxide (Cu₂O) and tin oxide (SnO) are actively researched as potential channel materials for oxide TFTs.

Cu₂O exhibits a distinctive electronic structure characterized by a closed-shell Cu 3d¹⁰ configuration ((*n*−1)*d*¹⁰*ns*⁰). This compound possesses a cubic crystal structure belonging to the space group (pm3), consisting of two interpenetrating diamond-like networks of oxygen and copper.^[35] In Cu₂O, the valence band maximum (VBM) primarily results from the hybridization of Cu 3d and O 2p orbitals. The energy levels of Cu 3d orbitals are comparable to those of oxygen 2p levels. Consequently, Cu₂O features a less localized hole-transport pathway, resulting in excellent hole-transport properties. The energy levels of the conduction band minimum (CBM) are relatively shallow, and electron doping is feasible. The energy level of VBM in Cu₂O typically falls in the range of 5–6 eV, significantly shallower than the typical energy levels found in *n*-type oxides (>7 eV).

The electronic structure of SnO is characterized by a Sn 5s² configuration ((*n*−1)*d*¹⁰ *ns*²). It possesses a PbO-type structure with a tetragonal litharge structure, which belongs to the space group (P4/nmm). This crystal structure compound comprises a layer structure featuring a pyramid-like arrangement with four oxygen atoms and one tin atom.^[36] The VBM in SnO is formed through the hybridization of oxygen 2p and spherical Sn 5s orbitals. The significant contribution of spherical s orbitals results in a dispersed VBM structure. The VBM energy level for SnO typically

falls within the range of 5–6 eV, which is shallower than the energy levels typically observed in *n*-type oxides (>7 eV). Additionally, SnO has relatively shallow conduction band minimum (CBM) energy levels, allowing for the possibility of electron doping.

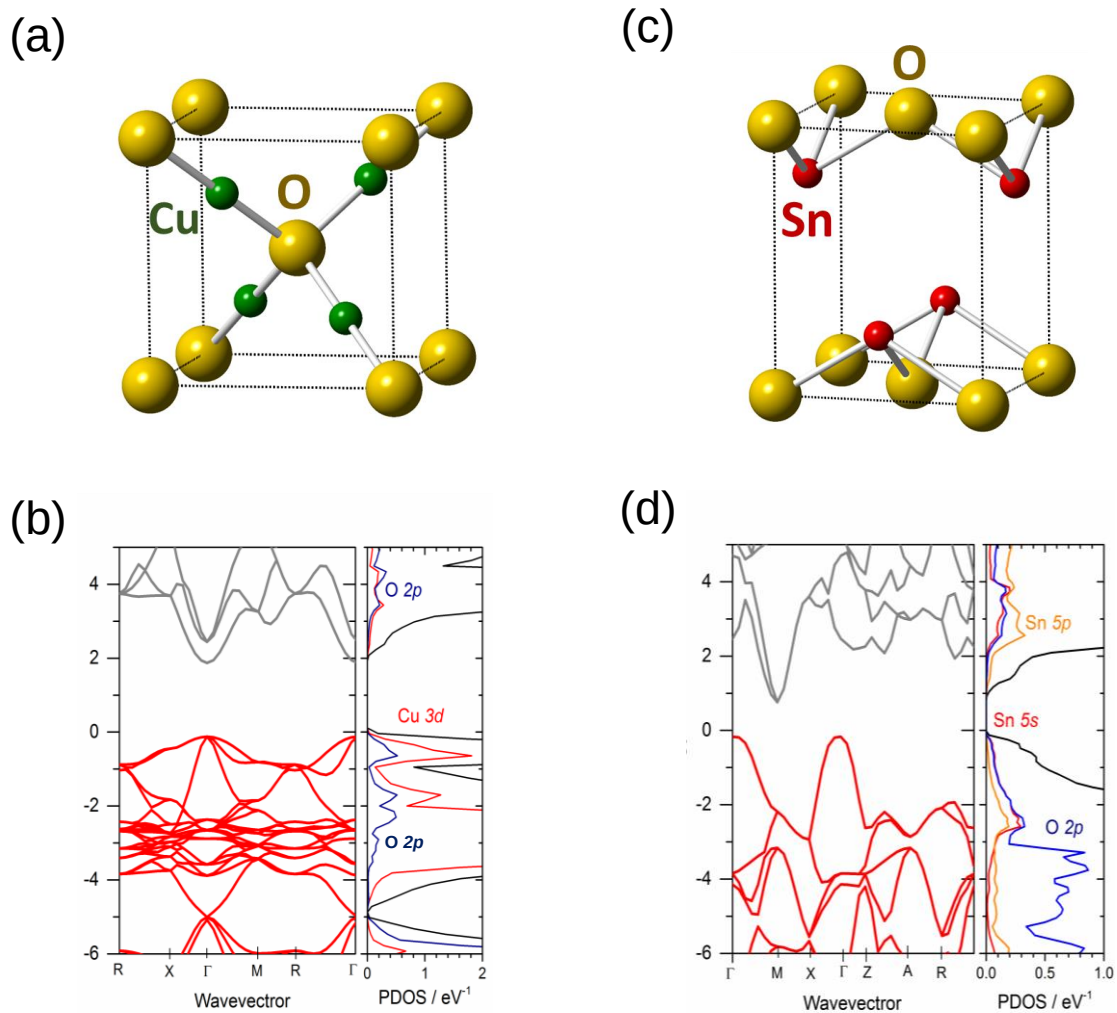


Figure 1.5 (a) Crystal structure and (b) energy band diagram for Cu_2O . (c) Crystal structure and (d) energy band diagram for SnO .

1.6 Oxide Thin-Film Transistors for Synaptic Device Applications

Artificial Intelligence (AI) is revolutionizing technology and expanding its capabilities by learning from vast amounts of data. In recent years, significant advancements in artificial neural networks (ANNs) have emerged, driven by increased computational power, the availability of big data, and breakthroughs in training algorithms. These developments have profoundly impacted various fields, including computer vision, security, robotics, healthcare, and the Internet of Things. However, deploying AI in real-time or mobile applications can be prohibitively expensive due to the substantial costs associated with storage, memory bandwidth, and energy consumption, primarily driven by the size of neural networks and their numerous parameters. To make AI truly ubiquitous, it is essential to develop new electronics that establish the foundations for AI hardware with lower power consumption and thermal requirements.

Despite the significant advancements in Moore's Law over the past few decades, the biological brain continues to exhibit superior cognitive capabilities and energy efficiency when compared to existing computer systems. Conventional von Neumann computing architectures involving data transfers between logic and memory blocks lead to processing bottlenecks and unnecessary power consumption. In response to these challenges, neuromorphic computing systems draw inspiration from the human brain. They aim to enhance cognitive performance and energy efficiency by physically emulating neurons and synapses at a small circuit-to-device level. This approach incorporates the co-location of logic and memory, robustness, and parallel processing.

To fully harness the potential strengths and capabilities of the human brain in neuromorphic computing, it is essential to develop a learning algorithm that relies on information processing between biological synapses and neurons. Additionally, realizing artificial synapses that closely mimic their biological counterparts is crucial. Traditionally, silicon-based CMOS analog circuits were employed to emulate synaptic functions. However, this approach requires a significant number of transistors (~10 transistors per synapse). Moreover, the energy consumption of basic synaptic events in CMOS-based analog circuits can exceed that of biological synapses.

To address the limitations associated with CMOS-based analog circuits, several emerging non-volatile memory (NVM) technologies, including phase-change memory, resistive random-access memory, and spin-torque transfer random-access memory, have been proposed as a foundation for analog neuromorphic computing to implement synaptic functions.^[37-38] While two-terminal artificial synapses, developed using relatively matured NVM technology, offer advantages, such as a simple device structure, small cell size, and low energy consumption, efficiently emulating the complex biological behavior in a two-terminal synaptic device can be challenging. Additionally, two-terminal synaptic devices require supplementary circuit components to select target cells and reduce cell-to-cell interference.

Recently, transistor-based synaptic devices with a three-terminal structure have gained considerable attention due to their ability to efficiently mimic synaptic behavior within a single device. Information transmission and processing occur in biological synapses as the presynaptic pulse is transformed into a current or voltage change in the postsynapse.^[38-39] Synaptic transistors emulate this synaptic behavior by using the gate electrode as the presynapse and the source/drain

electrode as the postsynapse. When a voltage pulse, acting as a stimulus, reaches the presynaptic terminal (gate terminal), the excitatory postsynaptic current is generated in the postsynaptic terminal (drain terminal). Synaptic transistors excel at reliably generating spikes, exhibiting electrical plasticity, and providing precise control over synaptic weight through robust electrical coupling between two or more synaptic spikes. Furthermore, transistor-based synaptic devices offer the potential to replicate multiterminal synaptic behavior, enabling the realization of complex neuromorphic functions using dual- or multi-gate device structures.^[39] Among several emerging materials for synaptic device applications, oxide semiconductors are promising candidates for artificial synaptic transistors because of their high mobility, low power consumption, excellent uniformity, low processing temperature, low cost, and good compatibility with current large-area processing technologies.

Two-terminal memristors necessitate a selector device to program individual memory/synapse nodes in a crossbar array for memory applications and neuromorphic computing. Various solutions have been explored, including the one-transistor-one-memristor (1T1M) configuration, in which the transistor serves as a selector to minimize sneak currents.^[40-41] However, using separate devices for memristors and transistor selectors detrimentally affects integration density and often leads to incompatible processes. Combining the properties of a transistor and a memristor into a single device is highly desirable. Recently, gate-tunable memristors, that is, memtransistors, that combine memory and switching functions into a single device, were proposed to address these issues and offer a new opportunity for memristive circuits and related applications.^[40, 42] Memtransistors integrate the 1T1M architecture within a single

device, achieve bio-realistic heterosynaptic behavior, and provide gate-tunable synaptic and learning functions.

1.7 Objectives and Overview of Thesis

The goal and motivation of the thesis are developing oxide semiconductors and devices that pave the way to revolutionize new electronic applications for large-area flexible integrated circuits, BEOL electronics in monolithic 3D integration for CMOS, and emerging computing devices for non-traditional computing platforms. The thesis is structured into three parts. Part I emphasizes the development of high-performance *p*-channel oxide TFTs (Chapters 2 and 3). Part II explores new oxide channel materials for low-temperature processed, high-mobility, and wide-bandgap oxide TFTs (Chapter 4). Part III delves into the study of oxide TFTs as emerging computing devices for non-traditional computing technology (Chapters 5 and 6).

In Chapter 2, we proposed a scalable liquid element treatment technique to address structural defects in oxide materials, specifically oxygen and metal cation vacancies. To investigate this approach, we conducted experiments using SnO TFTs as our experimental platform. By employing liquid sulfur, we achieved effective anion treatment, resulting in the passivation of oxygen vacancies and a reduction in the density of donor-like defects in SnO materials from 2×10^{18} to $5.5 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$. On the other hand, by leveraging the liquid Bi-Sn eutectic alloy system, we successfully controlled Sn cation treatment at a low temperature of approximately 140°C , allowing us to modulate the hole concentration, reducing it from 9×10^{17} to $5 \times 10^{16} \text{ cm}^{-3} \text{ eV}$ and achieve a wide range of threshold voltage modulation. Furthermore, through the liquid Bi-Sn alloy treatment, we successfully modulated the threshold voltage in SnO TFTs, enabling the development of oxide PMOS inverters. A low-power and high-gain complementary inverter was achieved by integrating *n*-type IGZO TFTs with *p*-type SnO TFTs with the liquid Bi-

Sn eutectic alloy, underscoring the potential of oxide TFTs for power-efficient, large-area CMOS circuitry.

In Chapter 3, we developed high-performance *p*-channel oxide TFTs using atomically thin *p*-type tin monoxide, SnO channel with a thickness of ~ 1 nm. This channel was grown by a vacuum-free, solvent-free, metal-liquid printing process at a temperature as low as 250°C in ambient atmosphere. By performing oxygen vacancy defect terminations for the bulk-channel and back-channel of the SnO channel, the presented *p*-channel SnO TFTs exhibited good performance with a reasonable TFT mobility of $\sim 0.47 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, a high on/off current ratio of $\sim 10^6$, a low-off current ($< 10^{12} \text{ A}$), and a subthreshold swing of $\sim 2.5 \text{ V decade}^{-1}$, which was improved compared to conventional *p*-channel SnO TFTs.

In Chapter 4, we introduced a pressure-assisted liquid-metal printing technique that enables low-temperature crystallization in nanoscale confinement for wide bandgap *n*-channel oxide TFTs. This approach overcomes the thermal limitation of oxide semiconductor materials growth and enables the growth of semiconducting atomically thin $\beta\text{-Ga}_2\text{O}_3$ at the process temperature of less than 150 °C in a non-controlled ambient air atmosphere. The *n*-channel oxide TFTs using the ~ 3 nm-thickness of $\beta\text{-Ga}_2\text{O}_3$ channel exhibited excellent TFT switching properties with a high saturation mobility of $\sim 11.7 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, a large on/off-current ratio of $\sim 10^9$, and a sharp subthreshold slope of $\sim 163 \text{ mV decade}^{-1}$, which were significantly improved from the previously reported $\beta\text{-Ga}_2\text{O}_3$ TFTs. The presented work demonstrates the low-temperature crystallization of device quality $\beta\text{-Ga}_2\text{O}_3$, revealing the high potential of the $\beta\text{-Ga}_2\text{O}_3$ for high-performance *n*-channel oxide TFTs.

In Chapter 5, we demonstrated dynamic reconfigurable excitatory and inhibitory synaptic responses in a single synaptic device using a low-temperature processed ambipolar SnO-based TFT. To develop the well-balanced ambipolarity of SnO TFT, we developed boron-incorporated SnO (SnO:B) as the active channel to suppress the subgap defect in the SnO channel compared to non-doped SnO. By leveraging the carrier trapping/emission and ambipolarity of presented devices, we could dynamically modulate synaptic response through gate bias, emulating excitatory and inhibitory synapse responses. This reconfigurable response is crucial for emulating complex biological functions in emerging neuromorphic hardware.

In Chapter 6, we presented a new type of non-layer two-dimensional (2D) material, oxide semiconductor Tin dioxide, SnO₂ based gate-tunable memristor, that is, memtransistor, an integrated device of memristor and transistor, to advance next-generation normochromic computing technology. Polycrystalline 2D-SnO₂ memristors derived from low-temperature and vacuum-free liquid metal processes offer several interesting resistive switching properties, such as excellent digital/analog resistive switching, multistate storage, and gate-tunability function of resistance switching states. Significantly, the gate tunability function that is not achievable in conventual two-terminal memristors provides the capability to implement heterosynaptic analog switching by regulating gate bias for enabling complex neuromorphic learning. We successfully demonstrated that the gate-tunable synaptic device dynamically modulated the analog switching behavior with good linearity and improved the conductance change ratio for high recognition accuracy learning.

In Chapter 7, I summarize my Ph.D. research work in this dissertation. Additionally, I discuss the challenges and outlook of oxide semiconductor TFT technology for future electronics.

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Chapter 2 Carrier Modulation and Defect Termination of Oxide Semiconductor Enabled by the Liquid Element for *p*-Channel Thin-Film Transistors

2.1 Introduction

Developing high-performance electronic devices that can be processed at near ambient temperatures is highly demanded, realizing various applications such as flexible displays, wearable electronics, sensors, human-machine interfaces, and highly-integrated BEOL-compatible transistors for monolithic three-dimensional (3D) complementary metal-oxide-semiconductor (CMOS) architectures.^[1-4] Oxide semiconductors are as widely accepted as promising materials for developing large-area, cost-effective, and low-temperature processed electronics. However, oxide semiconductors are highly susceptible to intrinsic and extrinsic structural defects, such as cation and oxygen vacancies, which hinder device performance.^[5-6] Thus, it is crucial to develop effective approaches to eliminate these structural defects and enhance the performance of oxide-based electronic devices.

While several *n*-type oxide material systems with high electron mobility, such as *a*-In-Ga-Zn-O (*a*-IGZO),^[7] In₂O₃,^[8] ZnO,^[9] SnO₂,^[10] and others,^[11-12] have been identified, the development of *p*-type counterparts has remained limited despite many years of efforts.^[3, 6, 13] This is known to hinder the realization of energy-efficient oxide CMOS circuits for ultra-low power and low-thermal budget electronics and stands as the most significant technological barrier. Among several *p*-types, tin monoxide (SnO) with α -PbO layered crystal structure is promising for *p*-channel TFT application because of reasonable high hole mobility ($1\text{--}3\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$)^[14-18] and the low-temperature processability as low as 250 °C, enable to develop flexible electronics that have

thermal limitations.^[1, 19-22] In SnO, oxygen vacancies (V_o), and tin vacancy (V_{sn}) are energetically favorable native defects and are considered to contribute to forming donor-like states and acceptor states.^[23-25] So far, it is clear that the V_o defect is located above the valence band minimum (VBM), with a high density of $>10^{19} \text{ cm}^{-3} \text{ eV}^{-1}$, and acts as hole traps, impeding the device performance of *p*-type oxide devices.^[6, 17, 26-27]

Therefore, engineering strategies to terminate such defects are significant for developing high-performance oxide electronic devices. Post-thermal annealing and some oxidization treatments are well-known techniques for reducing V_o defects for oxide semiconductors.^[5] Generally, strong oxidation conditions produced at high temperatures in an oxygen-containing atmosphere are used for V_o defect reduction and high-quality oxide material growth. However, implementing these techniques is challenging for *p*-SnO due to the formation of undesired oxides because of the higher valence states of metal cations; Sn^{4+} is more stable than Sn^{2+} , leading to the conversion of Sn^{2+} to Sn^{4+} at the annealing temperatures above 300°C .^[25-26, 28-30] This limitation restricts post-deposition annealing and treatment conditions, emphasizing the need for defect termination approaches at lower temperatures to fully utilize the potential of *p*-type oxide materials in electronic applications.

Moreover, another significant challenge in *p*-type oxide development is the absence of control of the acceptor density, unlike in the case of *n*-type oxides, where electron density can be controlled through oxygen partial pressure during film deposition. SnO is a highly doped *p*-type semiconductor with a hole density of $\sim 10^{18} - 10^{19} \text{ cm}^{-3}$, regardless of the film fabrication process.^[6, 24, 29-31] Several studies have shown that the V_{sn} forms the shallow double acceptor just above VBM

with low formation energy, causing unintentional self-*p*-doping in SnO.^[23-24] Therefore, most of the previously reported SnO thin-film transistors (TFTs) exhibit depilation mode (*D*-mode) operation with a negative threshold voltage (V_{th}), which hinders the potential of next-generation energy-efficient circuit applications of SnO TFTs. Consequently, it becomes necessary to explore methods for controlling the V_{sn} to modulate the hole density, meet the threshold voltage (V_{th}) requirements for circuit design, and achieve energy-efficient enhancement-type transistor operation.

Here, we report a scalable liquid element treatment technique that can terminate structural defects in oxide materials, specifically oxygen and metal cation vacancies. We developed an anion treatment using liquid sulfur for SnO, demonstrating the effective passivation of V_o with the reduction in the defect density from 2×10^{18} to $5.5 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$. On the other hand, cation treatment using liquid Sn treatment successfully terminated V_{sn} defect and allowed us to modulate the hole concentration. To achieve a wide range of hole concentration modulation, we developed the liquid Bi-Sn eutectic alloy system, enabling Sn cation treatment and modulating the hole concentration from 9×10^{17} to $5 \times 10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$ at a low temperature of $\sim 140^\circ \text{C}$. This method facilitated the modulation of hole density from 9×10^{17} to $5 \times 10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$, offering the opportunity to fabricate SnO-based TFTs operating in the enhancement mode (*E*-mode) with low power consumption. The *E*-mode SnO TFTs exhibited hole saturation mobility (μ_{sat}) of $3.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, ideal turn-on voltage (V_{on}) of 3.9 V, *s*-value of $1.3 \text{ V} \cdot \text{decade}^{-1}$, and on/off current ratio (I_{on}/I_{off}) over 10^4 , enabling the development of oxide PMOS inverters with the same channel width/length as the transistors. By integrating *n*-type IGZO TFTs with *p*-type SnO TFTs using the liquid Bi-Sn

eutectic alloy treatment, the low-power and high-gain complementary inverter is further realized, highlighting the potential of oxide TFTs for energy-efficient, large-area CMOS circuit integration.

2.2 Experimental Section

SnO:B channel deposition

SnO:B channel with a film thickness of ~ 12 nm was deposited by pulsed laser deposition (PLD) at room temperatures (RT) using KrF excimer laser (wavelength of 248 nm, the pulse duration of ~ 20 ns, and the pulse frequency of 10 Hz). The base vacuum of the PLD chamber was $<1.8 \times 10^{-8}$ Torr. The oxygen partial pressure during the deposition was fixed at 2×10^{-4} Pa. A polycrystalline 5 atomic-%-boron-incorporated SnO sintered body target was prepared by conventional solid-state reaction. A laser power density of $\sim 6 \text{ J cm}^{-2}$ at the target surface yielded a film growth rate of ~ 6 nm/min.

SnO:B thin-film transistor fabrication and electrical characterization

The SnO:B thin-film transistors were fabricated with inverted-staggered structures, utilizing bottom-gate and top source/drain contacts. The 150 nm thermal-oxidized SiO_2/n^+ -Si substrates were used as the gate oxide and gate electrode. The channel area was patterned using photolithography and defined by chemical wet-etching with 1 mol/l of diluted HNO_3 solution. Then, the hydrogen thermal annealing was performed for 30 minutes with $\text{N}_2 + \text{H}_2$ (5% hydrogen) at 250 °C. The source and drain electrodes were made of indium tin oxide (ITO), patterned by photolithography and lift-off techniques, and then deposited at room temperature using PLD. The 40 nm-thick ITO layer was deposited with an oxygen partial pressure of 2×10^{-4} Pa at room temperature. The channel width (W) was 300 μm and the length (L) was 50 μm . The electrical characteristics were measured using the semiconductor parameter analyzer at room temperature in the dark.

Liquid sulfur and selenium treatment

The sulfur or selenium powder was melted in a glass container at temperatures slightly above their respective melting points in ambient air (115.2 °C for S and 221 °C for Se), specifically around 125 °C for sulfur and 230 °C for selenium. The molten liquid sulfur or selenium size was larger than the device sample, ensuring complete coverage of all samples.

Prior to treatment, the TFT device sample was pre-heated to the desired process temperature (125 °C for sulfur and 230 °C for selenium). Subsequently, the TFT device sample was inverted and placed onto the liquid sulfur or selenium surface. After the desired treatment process time, the top TFT device sample was vertically lifted, separating it from the liquid sulfur or selenium surface. Any residual sulfur or selenium attached to the surface of the TFT sample could be removed by gently rubbing the SiO₂/Si wafer, which was submerged in ethanol, with a soft wiping tool (such as a cotton bud).

Liquid Sn and Pb treatment

The elemental tin (Sn, 99.99%, Shot Metals) or elemental lead (Pb, 99.99%, Shot Metals) was melted on a glass plate at temperatures around 250 °C and 350 °C, slightly exceeding their respective melting points in ambient air (232 °C for Sn and 327.5 °C for Pb). The size of the molten metal was larger than that of the device sample, ensuring complete coverage of the samples. In this study, the size of the device sample was 10 × 10 mm², and Sn/Pb molten metal was > 30 × 20 mm².

After the Sn/Pb metal was melted, the surface of the liquid Sn/Pb metal would form a surface oxide layer. Before treatment, the pre-existing thick surface oxide layer on the molten Sn/Pb metal was removed, revealing a pristine metal surface. Also, the TFT device sample was pre-heated to the desired process temperature (250 °C for Sn and 350 °C for Pb). Subsequently, the TFT device sample was inverted and placed onto the liquid Sn/Pb metal surface. Following the desired treatment process time, the top TFT device sample was vertically lifted, separating it from the molten Sn/Pb metal. Metal inclusions attached to the surface of the TFT sample could be removed by gently rubbing the SiO₂/Si wafer, which was submerged in ethanol, with a soft wiping tool (cotton bud).

Bi–Sn alloy preparation

The Bi-Sn alloy forms a eutectic alloy with a melting point of ~139 °C, using 43 wt% Sn and 57 wt% Bi. During preparation, elemental bismuth (Bi, 99.99%, Shot Metals) and elemental tin (Sn, 99.99%, Shot Metals) were placed in a glass vial and melted using a hot plate. The samples were heated from room temperature to 300 °C, exceeding the melting points of both Bi (271.4 °C) and Sn (232.0 °C), and were kept at 300 °C for 3 hours. During the first hour, the glass containers with Bi and Sn metals were shaken several times to facilitate mixing to form the Bi-Sn alloy. The samples were then cooled down to room temperature in ambient air.

Liquid Bi–Sn alloy treatment

The prepared Bi–Sn alloy in a glass vial was melted at temperatures that slightly exceeded their respective melting points in ambient air. The eutectic Bi–Sn alloy was melted at a temperature of 150 °C, given that the melting point of the eutectic Bi–Sn alloy is around 139 °C. The size of

the molten metal was larger than that of the device sample, ensuring complete coverage of the samples. In this study, the size of the device sample was $10 \times 10 \text{ mm}^2$, while the liquid Bi–Sn alloy was $> 30 \times 20 \text{ mm}^2$.

After the Bi–Sn alloy was melted in a glass vial, the liquid alloy was poured into a glass container. Before treatment, the pre-existing thick surface oxide layer on the liquid Bi–Sn alloy metal was removed, revealing a pristine metal surface. Also, the TFT device sample was pre-heated to the desired process temperature (150°C for eutectic Bi–Sn alloy). Subsequently, the TFT device sample was inverted and placed onto the liquid Bi–Sn alloy surface. Following the desired treatment process time, the top TFT device sample was vertically lifted, separating it from the liquid Bi–Sn alloy metal. Metal inclusions attached to the surface of the TFT sample could be removed by gently rubbing the SiO_2/Si wafer, which was submerged in ethanol, with a soft wiping tool (cotton bud).

Thin-film material characterization

The SnO:B film was prepared on a glass substrate for material characterization. Film structures were examined by grazing incidence X-ray diffraction with $\text{Cu K } \alpha$ radiation at an acceleration voltage of 50 kV, an emission current of 40 mA, and an incident angle of 0.5° .

Device simulation

Two-dimensional simulations of the TFTs cross-section were conducted using 2D ATLAS TCAD simulator (Silvaco) to gain insight into the electronic and defect structures of TFTs. The

simulations utilized the same configuration and materials as the TFT devices. The parameters used in the simulations are listed in **Table 2.1**.

IGZO Thin-film transistor fabrication

The IGZO thin-film transistors were fabricated with inverted-staggered structures, utilizing bottom-gate and top source/drain contacts. The 150 nm thermal-oxidized SiO_2/n^+ -Si substrates were used as the gate oxide and gate electrode. The a-IGZO films of a thickness of ~ 40 nm were deposited on SiO_2/n^+ -Si substrates by a PLD at room temperature (RT). The atomic composition of IGZO targets used in PLD was In: Ga: Zn = 1:1:1. The channel area was patterned using photolithography and defined by chemical wet-etching with 1 mol/l of diluted HCl solution. Then, the post-thermal annealing in the air atmosphere was performed at 400 °C for one hour. The source and drain electrodes were made of indium tin oxide (ITO). The source and drain electrode patterns were defined by photolithography and lift-off techniques. The 40 nm-thick ITO layer was deposited using PLD with an oxygen partial pressure of 2×10^{-4} Pa at room temperature. The channel width (W) was 300 μm and the length (L) was 600 μm .

2.3 Results and Discussion

Firstly, first-principle calculations based on the density functional theory (DFT) were performed to investigate point defects in SnO and gain insights into its enhanced *p*-type conductivity. **Figure 2.1(a)** shows the formation energies of native defects as a function of the Fermi level (E_F) under the Sn-rich limit. The valence band maximum (VBM) is set at $E_F = 0$ eV. The V_o exhibits defect transition levels of approximately 0.2 eV for ε (0/2+) above the VBM, forming a deep double donor state from the valence band (VB). However, the energy level of this donor state, corresponding to $E_c-0.6$ eV, is too deep to act as an efficient electron donor. Consequently, V_o functions as a donor-like defect, serving as a hole trap state in SnO. Eliminating V_o is crucial to enhance the performance of SnO TFTs. On the other hand, V_{Sn} forms shallow double acceptor states with low formation energy, exhibiting defect transition levels for ε (-/2-) of approximately 0.05 eV just above the VBM. The defect transition level is very close to the acceptor level, leading to V_{Sn} contributing to unintentional self-*p*-doping and facilitating *p*-type conduction in SnO. To control these defects, we develop an atom substitutional method, wherein elements from the same group as O and Sn are used to compensate for anion and cation vacancies, respectively (refer to **Figure 2.1(c)(d)**). To improve the TFT characteristics by eliminating V_o defects, we investigate subgap defect termination employing Group 16 elements, such as sulfur (S) and selenium (Se), to compensate for oxygen vacancies and reduce the defect density. (**Figure 2.1(c)**) Additionally, we utilize Group 14 elements, such as tin (Sn) and lead (Pb), to suppress cation vacancies, effectively acting as hole suppressors to control the hole concentration. (**Figure 2.1(d)**)

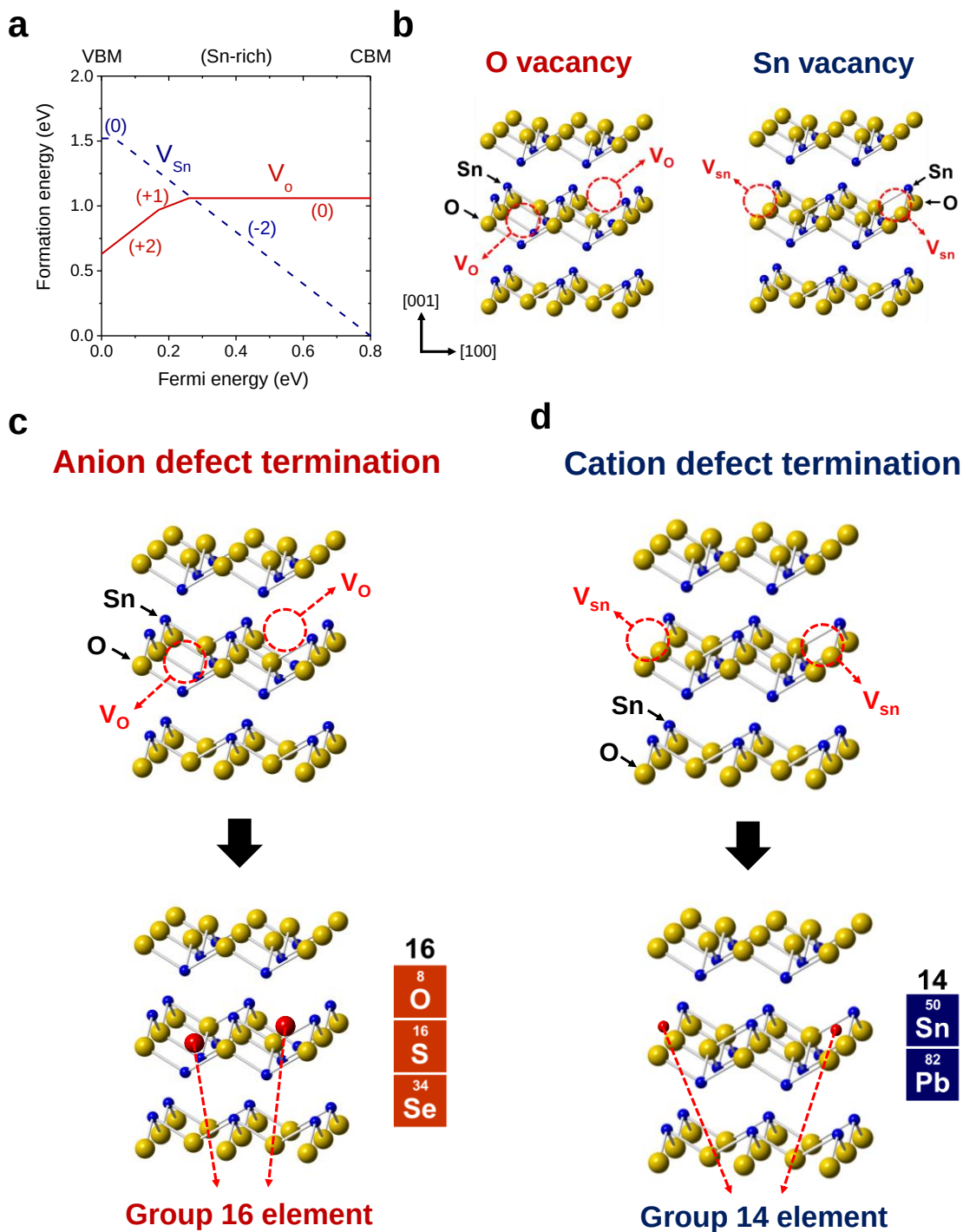


Figure 2.1(a) Formation energies of native defects in SnO as a function of the Fermi level under Sn-rich limit conditions using density functional theory calculations. (b) Schematic illustrations of oxygen vacancies and tin vacancies in the SnO crystal structure. (c) Schematic illustrations of anion defect termination using Group 16 elements, such as sulfur (S) and selenium (Se), to heal the oxygen vacancies in SnO. (d) Schematic illustrations of cation defect termination using Group 14 elements, such as tin (Sn) and lead (Pb), to compensate for cation vacancies in SnO.

Inverted staggered (that is, bottom-gate and top-contact) structure TFT was fabricated using SnO:B channel^[32] with a thickness of ~12 nm on 150 nm-thick thermal-oxidized SiO₂/n⁺-Si substrate, which works as a common gate and a common dielectric layer. (**Figure 2.2 (a)** shows the device structure) The grazing-incident X-ray diffraction (GIXRD) analysis revealed that the 5%-boron incorporation did not affect α -PbO type SnO crystal structure, and the films are polycrystalline without preferred crystal orientation. **Figure 2.2 (a)** also shows the mechanism of anion treatment using liquid sulfur and selenium. **Figure 2.2 (c)** shows the typical transfer characteristic, that is, I_{DS} versus V_{GS} , of the SnO:B TFTs under different anion treatments using liquid sulfur and selenium. The drain currents ($|I_{DS}|$), measured by the source-to-drain voltage (V_{DS}), increase upon applying negative gate bias (V_{GS}), which indicates that the device operates in *p*-channel mode composed of hole conductions. The TFT device characteristics such as saturation mobility (μ_{sat}), subthreshold slope (*s*-value), and threshold voltage (V_{th}) were determined as the following: the μ_{sat} is estimated by the following equation,

$$|I_{DS}| = \mu_{sat} C_{ox}(W/2L(V_{GS} - V_{th})^2) \quad (2.1)$$

, where C_{ox} is the gate insulator capacitance per unit area. The subthreshold slope (*s*-value) is extracted from the slope in the semi-logarithmic plot with $s = (\partial \log I_{DS} / \partial V_{GS})^{-1}$, where I_{DS} and V_{GS} are in the subthreshold region. The V_{th} is determined from the intercept of a straight-line fit of the $(I_{DS})^{1/2}$ - V_{GS} plot. The pristine SnO:B TFT shows the average of μ_{sat} of ~2.8 cm²V⁻¹s⁻¹, on/off current ratio of ~3×10⁴, *s*-value of 2 V decade⁻¹, and V_{th} of 5.7 V, which are comparable with the previously reported SnO TFTs (typical conventional SnO TFT performances; mobility of ~1 cm²V⁻¹s⁻¹, on/off current ratio of ~10⁴, *s*-value of ~5–15 V decade⁻¹)^[15, 29, 33-37]. The trap state density, D_{it} is estimated from the *s*-values using the following relation:

$$s = \frac{\log_e 10 \cdot k_B T}{e} \left[1 + \frac{e D_{it}}{C_{ox}} \right] \quad (2.2)$$

where e is the elementary electric charge, k_B is the Boltzmann constant, T is the temperature, t is the channel thickness, C_{ox} is the gate capacitance per area, and D_{it} is the defect density near the Fermi level. The calculated D_{it} was $\sim 4.7 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, which is also consistent with the previously reported SnO channel with D_{it} of $\sim 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. We performed the subgap defect termination *via* a liquid element approach with sulfur and selenium liquid metals to reduce V_o defects. Since the melting points of sulfur and selenium are $\sim 115.2^\circ \text{C}$ and $\sim 221^\circ \text{C}$, respectively, this process can be performed at low temperatures, which significantly prevents the oxidation from SnO to SnO₂. After performing the low-temperature processed liquid sulfur treatment, we can observe the improvement of the s -value based on the reduction of the D_{it} . In addition, the mobility did not degrade, and V_{th} and on/off current ratio are kept the same. In contrast, we did not improve TFT performances using liquid selenium treatment. This is reasonable because of the larger ionic radius of Se^{2-} (184 pm) than the ionic radius of S^{2-} (170 pm) against O^{2-} (126 pm). Such elements with larger ionic radius could potentially lead to impractical occupation or substitution of oxygen vacancies. The fundamental device parameters (μ_{sat} , s -value, V_{th} , and on/off current ratio) are also summarized in **Figure 2.2 (c)–(f)**. The sulfur-treated SnO:B TFTs exhibited reasonably high μ_{sat} of $\sim 2.7 \pm 0.35 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, improved s -value of $1.1 \pm 0.19 \text{ V decade}^{-1}$, on/off current ratio of $2.5 \pm 1.26 \times 10^4$, and V_{th} of $5 \pm 1.46 \text{ V}$.

We also attempted to utilize another group of elements for liquid cation treatment. Specifically, we investigated the effects of cation treatment using the Group 17 element, liquid iodide (I). Following applying liquid iodide (I) on the back-channel surface of SnO:B TFTs, we observed a degradation in TFT performance despite subsequent post-thermal annealing. We attribute this lack of improvement to the significantly larger ionic radius of I^{-1} (214 pm) compared

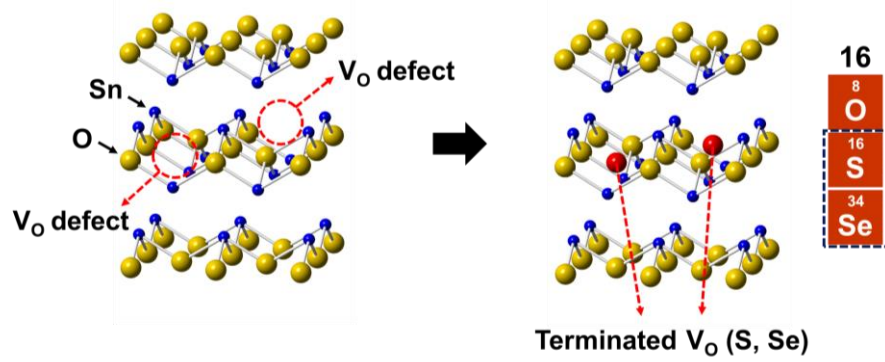
to O²⁻ (126 pm), which could potentially lead to impractical occupancy or substitution of oxygen vacancies.

To gain further insight into the variation of TFT characteristics, we performed a TCAD device simulation to extract the subgap trap state. **Figure 2.2 (g)** shows the measured and simulated transfer curves of sulfur-treated SnO:B TFTs. We found that all the measured curves were reproduced by only optimizing the acceptor-like defect (i.e., electron trap defect) with Gaussian distribution type,

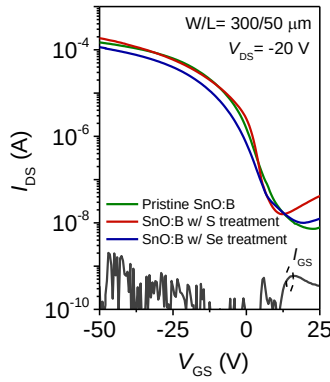
$$g_G(E) = N_{GD} \cdot \exp \left\{ - \left[\frac{(E_c - E_{GA})}{W_{GD}} \right]^2 \right\} \quad (2.3)$$

where N_{GD} is the state densities at the central energy E_{GA} of the Gaussian distribution, E_c the conduction band edge energy for the reference zero point, E_{GA} is the central energy of $g_G(E)$, W_{GD} is the characteristic decay energy. The extracted subgap DOS is shown in **Figure 2.2(h)** (**Table 2.1** provides the parameters of the TFT simulations). The pristine SnO:B TFT exhibited a relatively high density of shallow traps of $2 \times 10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$, resulting from the oxygen vacancies. We found that the liquid sulfur treatment effectively reduced the subgap defect DOS to $5.5 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$, indicating the sulfur incorporation heal defects with the density of $\sim 1.5 \times 10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$ and resulting in better TFT performances with smaller s -value.

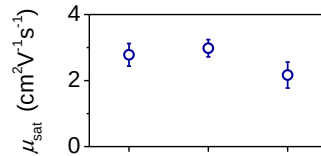
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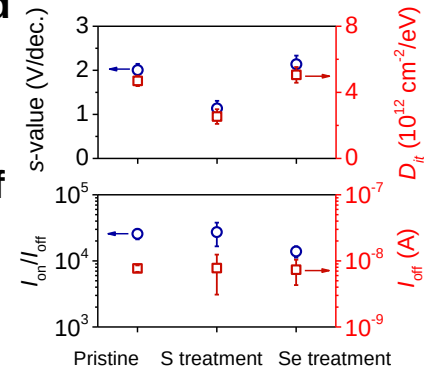
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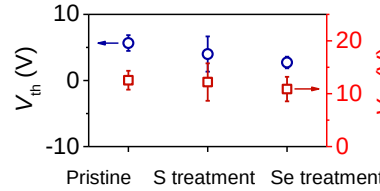
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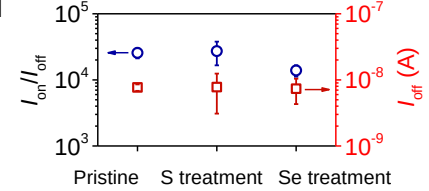
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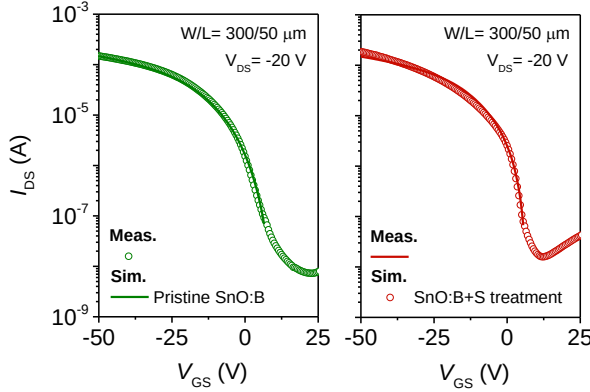
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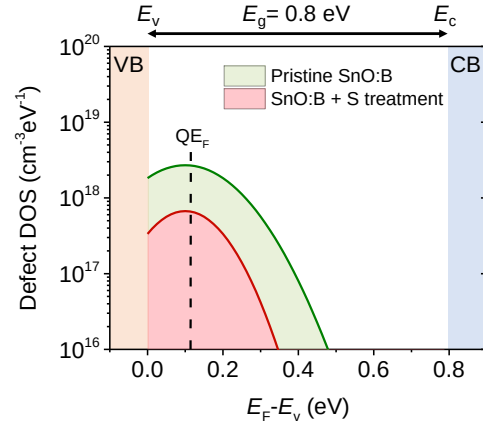


Figure 2.2 (a) Schematic for oxygen vacancies defect termination using liquid sulfur and selenium treatment. (b) Transfer characteristics of SnO:B TFTs under different conditions: pristine TFTs, TFTs with liquid S treatment, and TFTs with liquid Se treatment. The corresponding TFT parameters are plotted: (c) μ_{sat} , (d) s-value and D_{it} , (e) V_{th} and V_{on} , and (f) on/off current ratio and off-current. (g) Comparison of measured (symbols) and simulated (lines) transfer curves with $V_{DS} = -20 V$ of the SnO:B TFTs for pristine TFTs and S-treated TFTs, respectively. (h) Corresponding in-gap density of states of the SnO:B TFTs for pristine TFTs and S-treated TFTs, respectively. Fermi level (E_F) lies at $E_F - E_v = 0.16 eV$.

Table 2.1 TFT simulation parameters for sulfur-treated SnO:B TFT analysis.

Parameter	pristine	sulfur-treated
Band gap (eV)	0.8	4.7
Effective DOS for CB (cm^{-3})	2.41×10^{18}	3.72×10^{18}
Effective DOS for VB (cm^{-3})	9.13×10^{19}	1×10^{19}
Dielectric constant of SnO	10	10
Electron mobility ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	2.6	0.9
N_e electron density (cm^{-3})	9.0×10^{17}	9.0×10^{17}
N_{GD} (cm^{-3})	2.7×10^{18}	6.7×10^{17}
E_{GD} (eV)	0.1	0.1
W_{GD} (eV)	0.16	0.12

It is well-known that SnO exhibits unique ambipolar transport, primarily due to its intrinsic narrow indirect bandgap ranging from 0.7 to 0.9 eV.^[26, 31, 38] This characteristic reveals the potential for developing new circuit applications, such as ambipolar CMOS, for future electronics. Although the defect density of the presented SnO:B channel was reduced to $5.5 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$, the device did not show ambipolar transport characteristics as we discussed in our previous report.^[26, 32] Here, we would like to discuss the reason based on comparing liquid sulfur treatment with Al₂O₃ passivation using ALD, which is used to achieve ambipolar operations by reducing SnO channel defects.^[26, 32, 38] **(Figure 2.3(a)) Figure 2.3(b)** compares these transfer characteristics for the pristine SnO:B, S-treated SnO:B, and ALD-Al₂O₃ passivated SnO:B TFTs. The TFT parameters (μ_{sat} , s -value and D_{it} , V_{th} and V_{on} , and on/off current ratio and I_{off}) for both p - and n - channel operation are also summarized in **Figure 2.3(c),(d)**. The sulfur-treated SnO:B TFTs exhibited reasonably high μ_{sat} of $2.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, s -value of $1.1 \text{ V decade}^{-1}$, on/off current ratio of $\sim 2.5 \times 10^4$, and V_{th} of 10 V for p -channel operation. Meanwhile, the ALD-Al₂O₃ SnO:B TFTs show ambipolar operation, exhibiting μ_{sat} of $1.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, s -value of $2.3 \text{ V decade}^{-1}$, V_{th} of -16 V , and on/off current ratio of $\sim 3 \times 10^4$ for the p -channel mode, and $\sim 0.01 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $4.3 \text{ V decade}^{-1}$, 14 V and $\sim 9 \times 10^2$ for the n -channel mode, respectively. Compared to the pristine SnO:B TFTs, both S treatment and ALD-Al₂O₃ defect termination can effectively improve the s -value by reducing D_{it} . However, only ALD-Al₂O₃ passivated SnO:B TFTs showed ambipolar behavior.

We analyzed the TFT characteristics to evaluate the effective subgap defect density of states (DOS), which corresponded to the trap state density, near the conduction band (CB) and valence band (VB) by the field-effect conductance (FEC) method, which was based on the analysis of the surface potential profile (ψ_s) using the subthreshold region conductance with respect to the

gate bias. Since the surface potential gradient profile is affected by the defect DOS near the conduction/valence band, the effective subgap DOS can be extracted by the following equation:^{[39-}

40]

$$DOS(E_F + \psi_{s,i}) = \frac{\varepsilon_s}{2q} \frac{\partial^2}{\partial \psi_{s,i}^2} \left(\frac{d\psi_{s,i}}{dx} \Big|_S \right)^2 \quad (i = 0, 1, 2, 3 \dots) \quad (2.4)$$

where, E_F is Fermi level, $\psi_{s,i}$ is surface potential, ε_s is permittivity, and i is the sequence beginning from the flat band to the accumulation mode. This method is widely used to analyze a full subgap DOS profile in semiconductor channels.^[41] **Figure 2.3(e)** illustrates the extracted effective subgap defect DOS profiles for the pristine, S-treated, and ALD-Al₂O₃ passivated SnO:B TFTs. A high-density shallow donor-like defect near VB, which acts as a hole trap, is observed in the pristine SnO:B channel, indicating that the high-density donor-like defect hinders the performance of *p*-channel operation. After the S treatment and ALD-Al₂O₃ passivation, the defect density for the SnO:B channel is well suppressed to $\sim 10^{17}$ and $\sim 2 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$, respectively, at $E-E_v$ (E_v : valence band energy) of $\sim 0.1 \text{ eV}$, to improve the *s*-value of the *p*-channel SnO:B TFTs. On the other hand, the S-treated SnO:B channel exhibits high-density acceptor-like defects near CB, which works as an electron trap, of $\sim 3 \times 10^{19} \text{ cm}^{-3} \text{ eV}^{-1}$ at $E-E_v$ of $\sim 0.7 \text{ eV}$, which is the same level as the pristine device. Therefore, the high-density acceptor-like defects near CB hinder the *n*-channel operation and only result in the *p*-channel operation. On the other hand, the ALD-Al₂O₃ passivated device exhibited a lower density of acceptor-like defects near CB, which is well suppressed to 10^{19} cm^{-3} at $E-E_v$ of $\sim 0.7 \text{ eV}$. The acceptor-like defects near CB contribute is critical to enabling the *n*-channel operation to achieve ambipolarity.

Although the origin of acceptor-like defects near the CB has not been clarified yet, based on the SnO crystallinity analysis using grazing incidence X-ray diffraction (GIXRD), we suspect

that the acceptor-like defect is related to structural crystal defects, such as bond angle distortions. **Figure 2.3(f)** plots the GIXRD patterns for the pristine SnO:B films and SnO:B films after S-treatment at 120 °C and SnO:B films after ALD-Al₂O₃ passivation at 300 °C. A series of diffraction peaks appeared at 29.8°, 51.6°, 57.3°, and 62.0° are assigned to (101), (201), (211), and (202) planes for all samples, indicating non-preferred oriented polycrystalline nature of SnO films. The crystallite size of SnO film is improved from 9.64 to 12.58 nm after ALD- Al₂O₃ passivation at 300 °C, suggesting that the crystallinity is improved by the ALD process. **(Figure 2.3(g))** Also, we observe that the crystallite size of SnO film increases from 10.88 to 12.58 nm with the increasing ALD processing temperature from 200°C to 300°C. Based on previous studies, the ALD-Al₂O₃ passivation layer can create a new thermodynamic equilibrium state for SnO and reduce the Gibbs free energy of SnO nucleation.¹⁸ This leads to an improvement in the crystallinity of the SnO film. On the other hand, the S-treatment confirms that it did not change the crystallite size of SnO, indicating the low-temperature processed S-treatment and post-thermal annealing after the sulfur treatment process did not impact the crystallinity.

Figure 2.3(h) summarizes the electronic/defect structure variation by S- treatment and ALD-Al₂O₃ passivation. After the ALD-Al₂O₃ passivation, the crystallinity of SnO:B is improved, resulting in near-VB and near-CB defects being significantly reduced to $\sim 2 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ at $E-E_v$ of $\sim 0.1 \text{ eV}$ and 10^{19} at $E-E_v$ of $\sim 0.7 \text{ eV}$, respectively. In this case, the Fermi level can be smoothly swept toward the conduction band by the applied gate bias because the subgap DOS is more than one order of magnitude smaller than the gate-induced charges. Therefore, the ALD-Al₂O₃ passivated device can exhibit a clear ambipolarity. On the other hand, the liquid sulfur treatment using the sulfur incorporation to compensate for the oxygen vacancies effectively reduced the near-

VB subgap defect DOS to $\sim 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ at $E-E_v$ of $\sim 0.1 \text{ eV}$, resulting in better TFT performances with smaller s -value. However, high-density acceptor-like defects near CB still hinder the n -channel operation and suppress the off-current for the p -channel mode. In this way, sulfur incorporation to compensate for the oxygen vacancies is the effective approach to eliminating the defect density near VB to improve the TFT performance, also avoiding the ambipolarity that leads to high off-current with high power consumption.

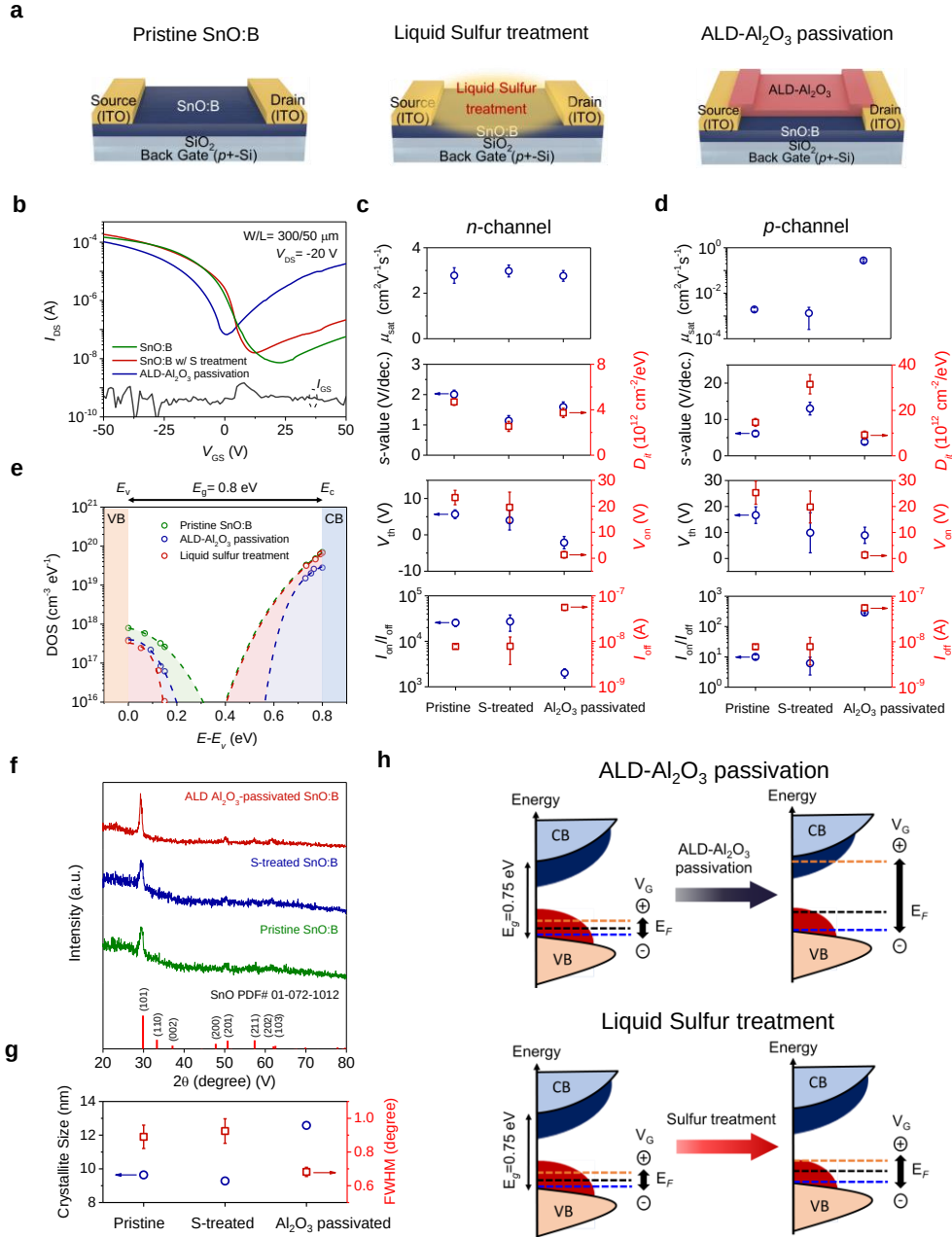
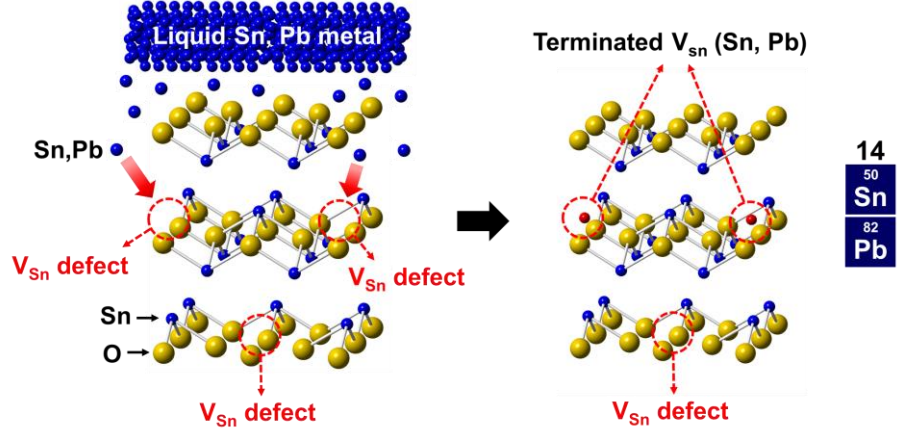


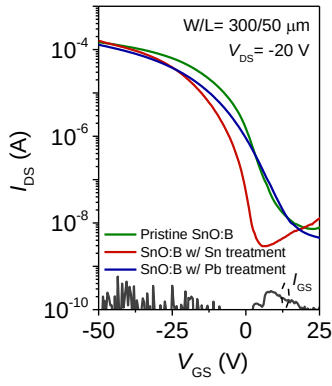
Figure 2.3 (a) Transfer characteristics of SnO:B TFTs under different conditions: pristine TFTs, liquid S treatment, and ALD Al₂O₃ passivation. The corresponding TFT parameters are plotted: μ_{sat} , s -value and D_{it} , V_{th} and V_{on} and on/off current ratio and off-current for (b) p -channel mode and (c) n -channel mode. (d) Corresponding effective subgap DOS extracted from field-effect conductance analysis for the pristine TFTs (red), TFTs with liquid S treatment (blue), and TFTs with ALD Al₂O₃ passivation (black). (e) XRD analysis for SnO thin film under different conditions: pristine film, SnO film with liquid S treatment, and SnO film with ALD Al₂O₃ passivation. (f) Corresponding crystallite size for the pristine film, SnO film with liquid S treatment, and SnO film with ALD Al₂O₃ passivation calculated from the XRD. (g) Schematic energy diagrams to explain the variation of TFT operation modes: SnO film with ALD Al₂O₃ passivation (ambipolar mode), and SnO film with ALD Al₂O₃ passivation (p -channel mode).

Next, we discuss a liquid metal treatment for cation vacancy, V_{Sn} for SnO, which causes unintentional self-*p*-doping with high hole concentrations exceeding 10^{18} cm^{-3} . Liquid element treatment using group 14 elements such as Sn and Pb were examined. Since the melting points of Sn and Pb are approximately 232°C and 327.5°C, respectively, we can directly perform cation treatment using liquid Sn and Pb on the back-channel surface for the SnO TFTs. **(Figure 2.4(a))** After the low-temperature liquid Sn treatment, the negative shift of the V_{on} from 23.4 to 6.3 V and the suppression of the off current was observed, as shown in **Figure 2.4(b)**. Moreover, the average *s*-value also improves from 2 to 1.2 V decade⁻¹, originating from the reduction of the D_{it} . On the other hand, the mobility is slightly degraded due to thermal effects during the liquid Sn treatment but still keeps $\sim 2 \text{ cm}^2/\text{Vs}$. To avoid thermal damage, the treatment time for the liquid Sn treatment should be within 30 seconds. In the case of liquid Pb treatment, further degradation of the *s*-value was observed after the liquid treatment. This is due to the relatively high process temperature, limited by the melting point of Pb (327.5 °C), resulting in the undesired formation of SnO₂ from SnO.

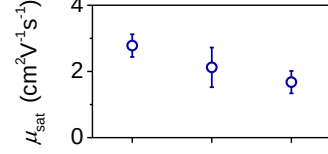
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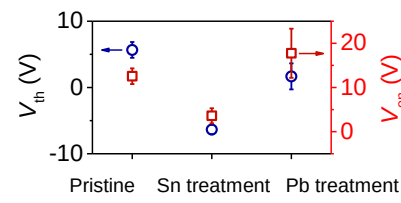
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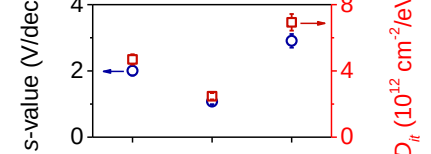
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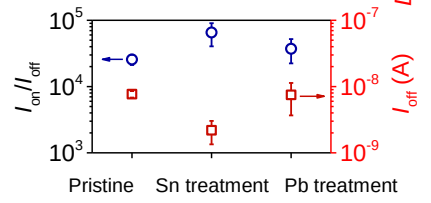


Figure 2.4 (a) Schematic for Sn vacancies passivation using liquid Sn treatment to control the carrier concentration. (b) Transfer characteristics of SnO:B TFTs under different conditions: pristine TFTs, TFTs with liquid Sn treatment, and TFTs with liquid Pb treatment. The corresponding TFT parameters are plotted: (c) μ_{sat} , (d) s -value and D_{it} , (e) V_{th} and V_{on} , and (f) on/off current ratio and off-current.

Since alloying of different metals leads to a decrease in both melting and freezing temperatures, we proposed liquid element treatment using binary metal alloys, bismuth–tin (Bi–Sn) alloy system to achieve a wide range of carrier concentrations and V_{th} modulation. The temperature drop becomes most significant at a specific mixing ratio, known as the eutectic state. Furthermore, in liquid metal alloy systems, individual elements naturally compete to appear on the surface based on their thermodynamic properties. This offers an efficient elemental-level filter for cation treatment based on the concepts we proposed. Bi–Sn alloys with varying ratios can be created, with some alloys having melting points lower than the melting points of both elements (Sn and Bi have melting points of 231.9 °C and 271.4 °C, respectively). When combined with Bi at 43 wt% Sn and 57 wt% Bi, the Bi–Sn alloy forms a eutectic alloy with a melting point of approximately 139 °C.^[42] **(Figure 2.5(a))** According to the Bi–Sn–O phase diagram, SnO selectively forms on the surface of the bulk eutectic Bi–Sn alloy in an air atmosphere, that is, at low O₂ concentrations.^[43–44] Based on this, we suspect a higher concentration of Sn than Bi near the surface of the liquid Bi–Sn alloy,^[43–44] allowing Sn metal to diffuse into the SnO materials and compensate for Sn vacancies during the treatment process. **(Figure 2.5(b))**

After the low-temperature liquid Bi–Sn eutectic alloy treatment, we observe a negative shift in V_{on} to approximately 3.9 V and an improvement in the s -value without any degradation of TFT parameters. **(Figure 2.5(c))** The low melting point of the Bi–Sn eutectic alloy enables a longer treatment process time, resulting in a wide range of V_{th} modulation from 23.4V to 3.9V. At a treatment time of 120 seconds, the device exhibits an average μ_{sat} of 3.1 cm²V⁻¹s⁻¹, an on/off current ratio of 2×10⁴, an s -value of 1.3 V decade⁻¹, and a V_{on} of 3.9 V, realizing E -mode operated TFTs. **(Figure 2.5(d)-(g))** Notably, this is the first report to achieve E -mode SnO TFTs with the

V_{on} close to 0 V, which is highly desirable for low-power consumption applications because it requires minimal gate voltage to turn on or turn off the transistors. The improvement of the s -value from 2 to 1.3 V decade⁻¹ is probably due to the increase in the Fermi level with lower hole density, moving it further away from the peak density of the donor defect state above the valence band. TCAD device simulation indicates that all the measured curves were reproduced by optimizing only the carrier concentration with the same Gaussian-type acceptor-like defect, suggesting that the liquid Bi–Sn eutectic alloy treatment only affects the hole concentration without impacting the defect states of SnO. (**Figure 2.5(h)**, **Table 2.2** provides the parameters of the TFT simulations.) The hole concentration can be suppressed from 9×10^{17} to 5×10^{16} cm⁻³eV⁻¹ using this approach. This is the first reported method to control carrier concentrations with a post-processing treatment in SnO materials. (**Figure 2.5(i)**)

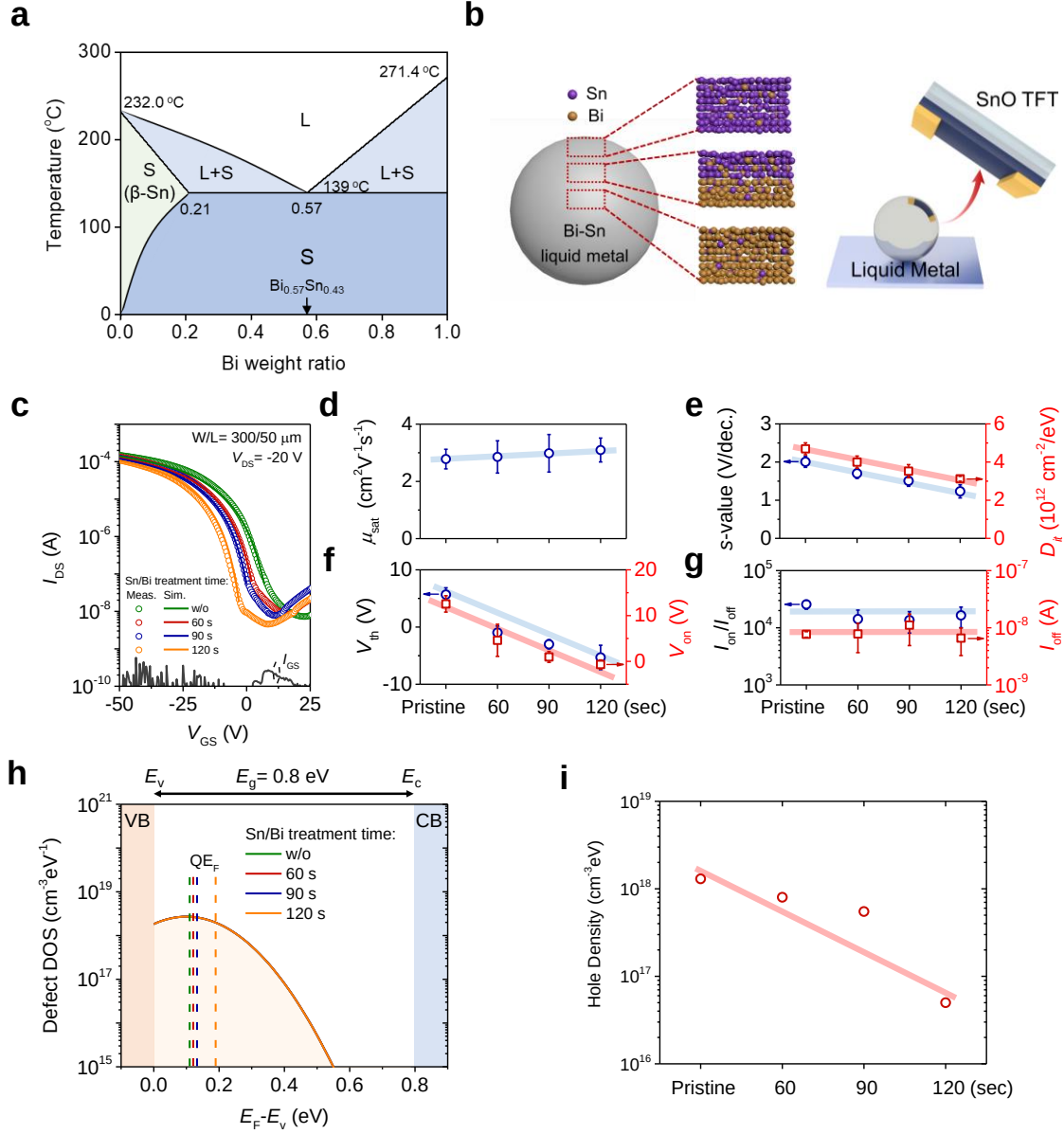


Figure 2.5 (a) Bi–Sn binary alloy phase diagram. (adapted from ref.^[42]) (L: liquid phase; S: solid phase) (b) Left: Schematic illustration of Sn and Bi atoms distribution within a liquid Bi–Sn alloy droplet. Sn atoms exhibit a stronger tendency to migrate from the core of the liquid metal towards the surface, resulting in Sn atoms predominantly occupying the surface layer of the alloy droplet. Right: Schematic of using liquid Bi–Sn binary alloy treatment to perform Sn vacancies passivation for SnO:B TFTs. (c) Transfer characteristics of SnO:B TFTs under different conditions: pristine TFTs and TFTs with liquid Bi–Sn alloy treatment with different treatment times of 60, 90, and 120 seconds, respectively. The corresponding TFT parameters are plotted: (d) μ_{sat} , (e) s-value and D_{it} , (f) V_{th} and V_{on} , and (g) on/off current ratio and off-current. (h) Measured (symbols) and simulated (lines) transfer curves with $V_{DS} = -20 V$ of the SnO:B TFTs for pristine TFTs and TFTs with liquid Bi–Sn alloy treatment under different treatment times of 60, 90, and 120 sec, respectively. (i) Dependence of hole concentration on different liquid Bi–Sn alloy treatment times.

Table 2.2 TFT simulation parameters for liquid Bi–Sn alloy-treated SnO:B TFT analysis.

Parameter	pristine	60 sec	90 sec	120 sec
Band gap (eV)	0.8	0.8	0.8	0.8
Effective DOS for CB (cm ⁻³)	2.41×10 ¹⁸	2.41×10 ¹⁸	2.41×10 ¹⁸	2.41×10 ¹⁸
Effective DOS for VB (cm ⁻³)	9.13×10 ¹⁹	9.13×10 ¹⁹	9.13×10 ¹⁹	9.13×10 ¹⁹
Dielectric constant of SnO	10	10	10	10
Electron mobility (cm ² V ⁻¹ s ⁻¹)	2.6	2.6	2.6	2.6
N _e electron density (cm ⁻³)	9.0×10 ¹⁷	8.0×10 ¹⁷	5.5×10 ¹⁷	5.0×10 ¹⁶
N _{GD} (cm ⁻³)	2.7×10 ¹⁸	2.7×10 ¹⁸	2.7×10 ¹⁸	2.7×10 ¹⁸
E _{GD} (eV)	0.1	0.1	0.1	0.1
W _{GD} (eV)	0.16	0.16	0.16	0.16

The liquid Sn treatment can enable the modulation of the V_{th} of SnO TFTs, allowing us to develop the oxide PMOS inverter with the same channel width/length. Here, we first demonstrated the oxide-based zero- V_{GS} PMOS inverter, consisting of the enhancement and depletion-mode TFTs as the driver and load, respectively. **Figure 2.6(a)** shows the typical transfer characteristics for the enhancement and depletion-mode TFTs in the PMOS inverter. The enhancement-mode TFTs were fabricated by performing liquid Bi–Sn eutectic alloy treatment after 120 seconds, showing the μ_{sat} of were $2.7 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, s -value of 1.5 Vdecade^{-1} , V_{th} of -1.8 V , and on/off current ratio of $\sim 10^4$. The pristine SnO:B TFT is as the depletion-mode TFTs for the load of the inverter with the μ_{sat} of $3.7 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, s -value of $1.3 \text{ V decade}^{-1}$, V_{th} of -8 V , and on/off current ratio of $\sim 10^4$. **Figure 2.6(b)** shows a typical voltage transfer characteristic (VTC) of the PMOS inverter, which is the V_{out} as a function of the V_{in} with V_{DD} . The inset illustrates the equivalent circuit diagram of the zero- V_{GS} -load PMOS inverter. The output voltage switches from high to low, confirming a clear inverting action with the full-voltage swing. The voltage gain of inverters, which is defined as $-dV_{out}/dV_{in}$ were estimated as 2.8, 8.7, 34.1, 104.4, and 205.7 at V_{DD} from -10 to -50 V , respectively. The maximum voltage gain was 205.7 at $V_{DD} = -50 \text{ V}$, indicating that the performance of oxide PMOS is comparable with the reported oxide-NMOS inverters.^[45-48] The top of **Figure 2.6(c)** also shows the corresponding supply currents (I_{DD}) as functions of V_{in} . The static currents ($V_{in} = 0 \text{ V}$ or $V_{in} = V_{DD}$) are lower than $\sim 2.4 \text{ }\mu\text{A}$, and the static power dissipation, which is defined by $P_{static} = V_{DD} (I_{static_low} + I_{static_high})/2$, is $\sim 122 \text{ }\mu\text{W}$ per logic gate at V_{DD} of 50 V . The P_{out} is estimated as $< 187 \text{ }\mu\text{W}$ per logic gate at V_{DD} of -50 V . (the bottom of **Figure 2.6(c)**) The noise margin (NM) is estimated using the maximum equal criterion method and obtained $\sim 23.2 \%$ of the ideal value ($V_{DD}/2$) at V_{DD} of -30 V . This indicates the device has sufficient NM for most static logic applications.

The goal of developing *p*-channel oxide TFTs is to integrate them with commercialized *n*-channel IGZO TFTs to achieve energy-efficient CMOS inverters. Herein, CMOS inverter circuits were fabricated using *n*-type IGZO TFTs and *p*-type SnO:B TFTs with liquid Bi–Sn eutectic alloy treatment after 120 seconds. The typical transfer characteristics of both the *p*-channel SnO:B TFT and *n*-channel IGZO TFT used in the oxide-TFT-based CMOS inverter are shown in **Figure 2.6(d)**. The *n*-channel IGZO TFT exhibits the μ_{sat} of $15 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, *s*-value of $0.12 \text{ V decade}^{-1}$, V_{th} of 2.5 V, and on/off current ratio of $\sim 10^8$. The corresponding TFT performances for *p*-channel SnO:B TFT are the μ_{sat} of $3.7 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, *s*-value of $1.3 \text{ V decade}^{-1}$, V_{th} of -8 V , and the on/off current ratio of $\sim 10^4$, respectively. The inset of **Figure 2.6(e)** illustrates the schematic circuit diagram of the CMOS inverters. **Figure 2.6(f)** presents the typical voltage transfer characteristic of the CMOS inverter, where the output voltage switches from high to low, confirming a clear inverting action with the full-voltage swing. The voltage gain of the inverters was estimated as 22.9, 55.7, 125.2, 203.8, 266.7, and 304.3 at V_{DD} from 5 to 30 V, respectively, which is comparable to the best values for oxide-based CMOS inverters.^[18, 48-51] The high inverter gain can be attributed to the improved device performance of the SnO:B TFT, particularly its steeper subthreshold slope. The I_{DD} of the ultrathin *p*-SnO:B/*n*-IGZO TFT-based CMOS inverter as a function of V_{in} is shown at the top of **Figure 2.6(f)**. The static currents are lower than $\sim 43 \text{ nA}$, leading to the low static power dissipation is $\sim 1.3 \text{ }\mu\text{W}$ per logic gate at V_{DD} of 30 V. The P_{out} is smaller than 48 nW at $V_{DD}=20 \text{ V}$ per logic gate, which indicates that this CMOS inverter can be operated by the nanowatt power source. (the bottom of **Figure 2.6(f)**) This demonstrates the potential of oxide-TFT-based inverter circuits for next-generation energy-efficient electronics.

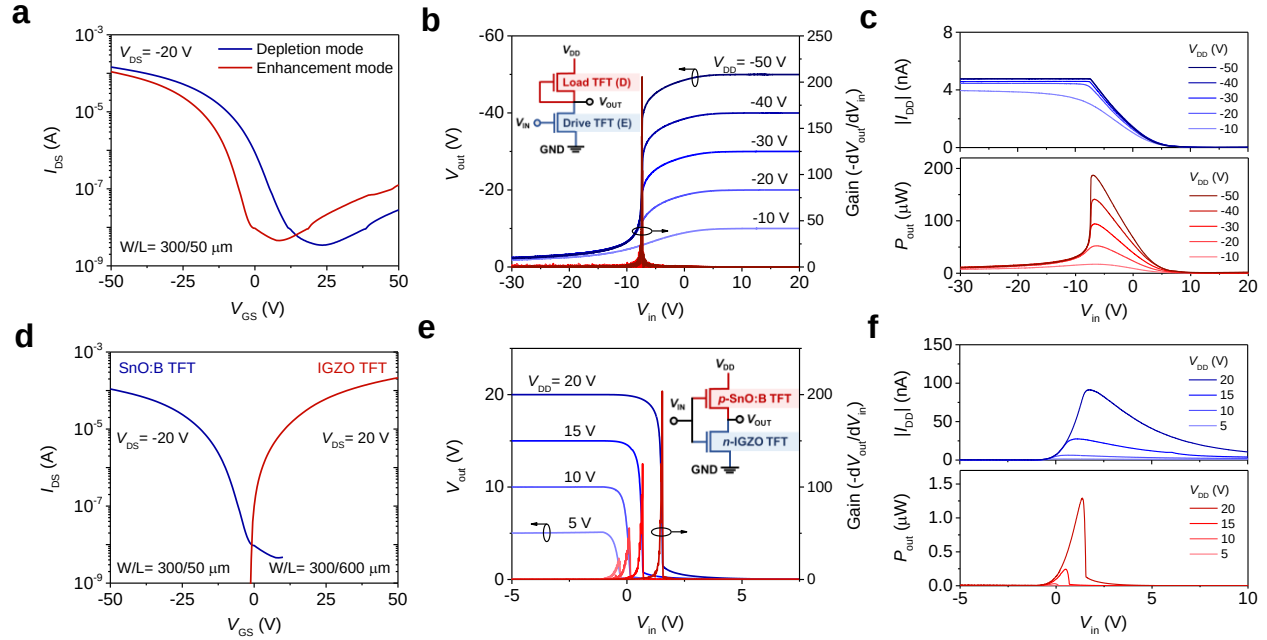


Figure 2.6 (a) Typical transfer characteristics for the depletion-mode and enhancement-mode SnO TFTs. (b) Voltage transfer characteristic and corresponding voltage gains of the SnO:B TFT-based PMOS inverter. Inset: schematic circuit diagram of the zero- V_{GS} -load PMOS inverter composed of enhancement/depletion-mode SnO TFTs. (c) Top: supply currents (I_{DD}). Bottom: output-power consumption (P_{out}) for the SnO:B TFT-based PMOS inverter. (d) Typical transfer characteristics of the p -channel SnO TFT and n -channel a-IGZO TFTs. (e) Voltage transfer characteristic and corresponding voltage gains for the p -SnO:B/ n -a-IGZO TFT-based CMOS inverter. Inset: schematic circuit diagram of the oxide-TFT-based CMOS inverter. (f) Top: I_{DD} . Bottom: the P_{out} for p -SnO/ n -a-IGZO TFT-based CMOS inverter.

2.4 Conclusions

This report introduces a scalable liquid element treatment technique to address structural defects in oxide materials, specifically oxygen and metal cation vacancies. To investigate this approach, we conducted experiments using a SnO oxide thin-film transistor as our experimental platform. By employing liquid sulfur, we achieved effective anion treatment, resulting in the passivation of oxygen vacancies and a reduction in the density of donor-like defects in SnO materials from 2×10^{18} to $5.5 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$. On the other hand, by leveraging the liquid Bi-Sn eutectic alloy system, we successfully controlled Sn cation treatment at a low temperature of approximately 140°C , allowing us to modulate the hole concentration and achieve a wide range of V_{on} modulation from 23.4 to 3.9V. By utilizing this method, we were able to finely tune the hole density, reducing it from 9×10^{17} to $5 \times 10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$. This significant modulation opens up possibilities for the fabrication of SnO-based TFTs that operate in enhancement mode with energy-efficient operation. The *E*-mode SnO TFTs exhibit hole μ_{sat} of $3.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, ideal V_{on} of 3.9 V, *s*-value of 1.3 Vdecade^{-1} , and $I_{\text{on}}/I_{\text{off}}$ over 10^4 . Furthermore, through the liquid Bi-Sn alloy treatment, we successfully modulated the V_{th} in SnO TFTs, enabling the development of oxide PMOS inverters. A low-power and high-gain complementary inverter was achieved by integrating *n*-type IGZO TFTs with *p*-type SnO TFTs with the liquid Bi-Sn eutectic alloy, underscoring the potential of oxide TFTs for power-efficient, large-area CMOS circuitry. It is worth noting that this liquid element defect termination technique holds promise for application in other oxide materials and material systems, including transition metal dichalcogenides.

Chapter 2, in part is currently being prepared for submission for publication of the material. Chi-Hsin Huang and Kenji Nomura. The dissertation author was the primary author of this chapter.

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Chapter 3 Atomically Thin SnO-based *p*-Channel Thin-Film Transistor and Low-Power Complementary Inverter

3.1 Introduction

The discovery of two-dimensional (2D) semiconductors has stimulated significant research attention, building new low-dimensional device applications for a wide electronics area owing to excellent features such as atomic-level thickness, high surface-to-volume ratio, tunable physics, chemical material properties, and extraordinary mechanical flexibility.^[1-2] Several 2D semiconductors, including transition metal dichalcogenide (TMD) monolayers,^[3-4] *h*-BN,^[5] silicene,^[6] have already been developed for next-generation electronics. Furthermore, 2D metal oxide materials such as TiO₂,^[7] ZnO,^[8] MoO₃,^[9] and perovskite-type oxides,^[10-11] have attracted much attention as the new family of 2D semiconductors because oxide has several advantages over others due to its wide-bandgap nature, environmental stability, high mass productivity. Nevertheless, the development of the 2D oxide semiconductor device is still behind that of other 2D materials. Moreover, the majority of conventional 2D materials are *n*-type^[12]. Exploring *p*-type 2D semiconductor materials is essential to developing a complementary metal-oxide-semiconductor (CMOS) inverter, the fundamental building block in digital/analog circuits in modern electronics.

Tin monoxide, SnO with α -PbO layered crystal structure is a well-known *p*-type oxide semiconductor and promising material for *p*-channel oxide-TFT due to its reasonable high hole mobility ($1\text{-}2\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$).^[13-17] **(Figure 3.1(a))** Moreover, the low-temperature processability as low as 270 °C allows fabricating of flexible device applications.^[14, 18-20] Numerous efforts to

advance *p*-channel SnO-TFT have been made and demonstrated for all-oxide-TFT-based CMOS inverters with *n*-channel oxide-TFT, such as amorphous-In-Ga-Zn-O (a-IGZO).^[18, 21-25] However, the device performance of the oxide-CMOS inverter is still not satisfied yet, mainly due to the inferior TFT performances such as a high off-current level as high as ~1 nA, small on/off current ratio <10⁴, and large subthreshold swing (s-value) of *p*-channel SnO-TFTs.^[14, 26-32] Since the off-current characteristics of TFT components in CMOS inverters directly impact the leakage current and easily degrade the voltage transfer characteristic (VTC), the high off-current characteristic is widely recognized as a severe disadvantage of SnO-TFT for oxide-TFT-CMOS technology.

These insufficient device characteristics are mainly attributed to both the high acceptor density (N_A) of > 10¹⁸ cm⁻³ and the high density of the subgap defect state of >10¹⁹ cm⁻³ near the valence band maximum (VBM) in the SnO channel.^[16, 33-34] Thus, all the reported SnO channels are highly conductive, and the TFT device operates in depletion mode, in which the conductive channel is controlled by the field-effect-induced depletion layer. Therefore, it is indispensable to develop thin channel to meet full-depletion conditions, achieving the low-off current for ultralow-power CMOS.^[13-14, 30, 35-36]

Figure 3.1(b) shows the ideal full-depletion conditions for the SnO channel, which can be found by the intersection of the depletion width (W) and field-induced charge (Q) in the SnO channel. The W and Q are determined by

$$W = \sqrt{\frac{2\varepsilon}{qN_e} \times \frac{k_B T}{q} \ln\left(\frac{N_e}{N_i}\right)} \text{ and } Q = C_{ox} V_{gs}, \text{ respectively} \quad (3.1)$$

where ε is permittivity, q is the elementary charge, N_e is donor density, N_i is the intrinsic carrier density, C_{ox} is capacitance, and V_{gs} is gate bias. Q was calculated using 150-nm-

thickness-SiO₂ (permittivity = 3.9) gate oxide with a gate bias of 50 V. It reveals that a full-depletion condition can be achieved if the SnO-channel thickness is less than 6-7 nm. **Figure 3.1(c)** also displays the variation of transfer curves by the SnO channel thickness by TFT device simulation for inverted-staggered SnO TFT (the inset of **Figure 3.1(c)** shows the device model for the TFT simulation) with the N_A of 10^{18} cm⁻³. We confirmed strong channel thickness dependence of TFT characteristics in depletion mode and found that an ultrathin SnO channel less than ~5 nm is required to attain the completely cut-off state with the low off-current for developing a high-performance oxide-based CMOS logic gate.

However, the channel thickness in the reported SnO TFTs is limited to 7-20 nm because SnO is generally grown by conventional physical vapor deposition (PVD) such as sputtering and pulsed-laser deposition (PLD)^{[14-15] [26, 36]}, in which the electrically inactive incubation layer with a few nm-thickness is grown due to the nature of three-dimensions (island) film growth. Recently, liquid-metal printing processes have been developed as a new strategy for growing ultrathin oxide materials.^[37-41], which is transferred from the molten metal to the substrate surface in an ambient atmosphere. Although the method is limited to low melting point low-melting-point metals (e.g. <300 °C) due to the difficulty of handling liquid metals under ordinary circumstances, a wide variety of material systems such as SnO₂, Ga₂O₃, and ZnO have been successfully fabricated so far. Particularly, ultrathin van der Waals layered materials such as SnS and PbO are relatively easily grown and transferred to substrates because of their weaker interlayer forces than the attractive forces between the oxide skin surfaces and substrates.^[42-43] Since the SnO involves the van der Waals gap originating from the lone-pair interaction of Sn 5s electrons, it can be recognized as van der Waals-type layered oxide with the interlayer spacing of ~0.252 nm along

[001] direction.^[44-45] (**Figure 3.1(d)**). Therefore, atomically thin *p*-type SnO channels can be fabricated by the liquid-metal printing process to develop high-performance *p*-channel TFT and oxide-TFT-based CMOS inverters.

This chapter reports the growth of an atomically ultrathin SnO channel by liquid metal printing and the development of *p*-channel SnO-TFTs for ultralow-power oxide-CMOS inverters. The ~1 nm-thick polycrystalline SnO channel with an atomically flat surface was prepared by the liquid-metal printing approach at 230 °C in the non-controlled ambient atmosphere. By reducing the bulk-channel and back-channel defects, the ultrathin SnO-TFT exhibited good TFT switching properties with a low-off current of <1 pA, large on/off current ratio of ~10⁶, TFT mobility of ~0.47 cm²V⁻¹s⁻¹, and *s*-value of ~2.5 V decade⁻¹. Moreover, we also fabricated *n*-channel oxide-TFTs using ultrathin *n*-type SnO₂ and In₂O₃ channels by the liquid metal printing methods and successfully demonstrated printed-oxide-TFTs-based CMOS inverter circuits exhibiting full voltage swing characteristics, high voltage-gain, and low-power operation.

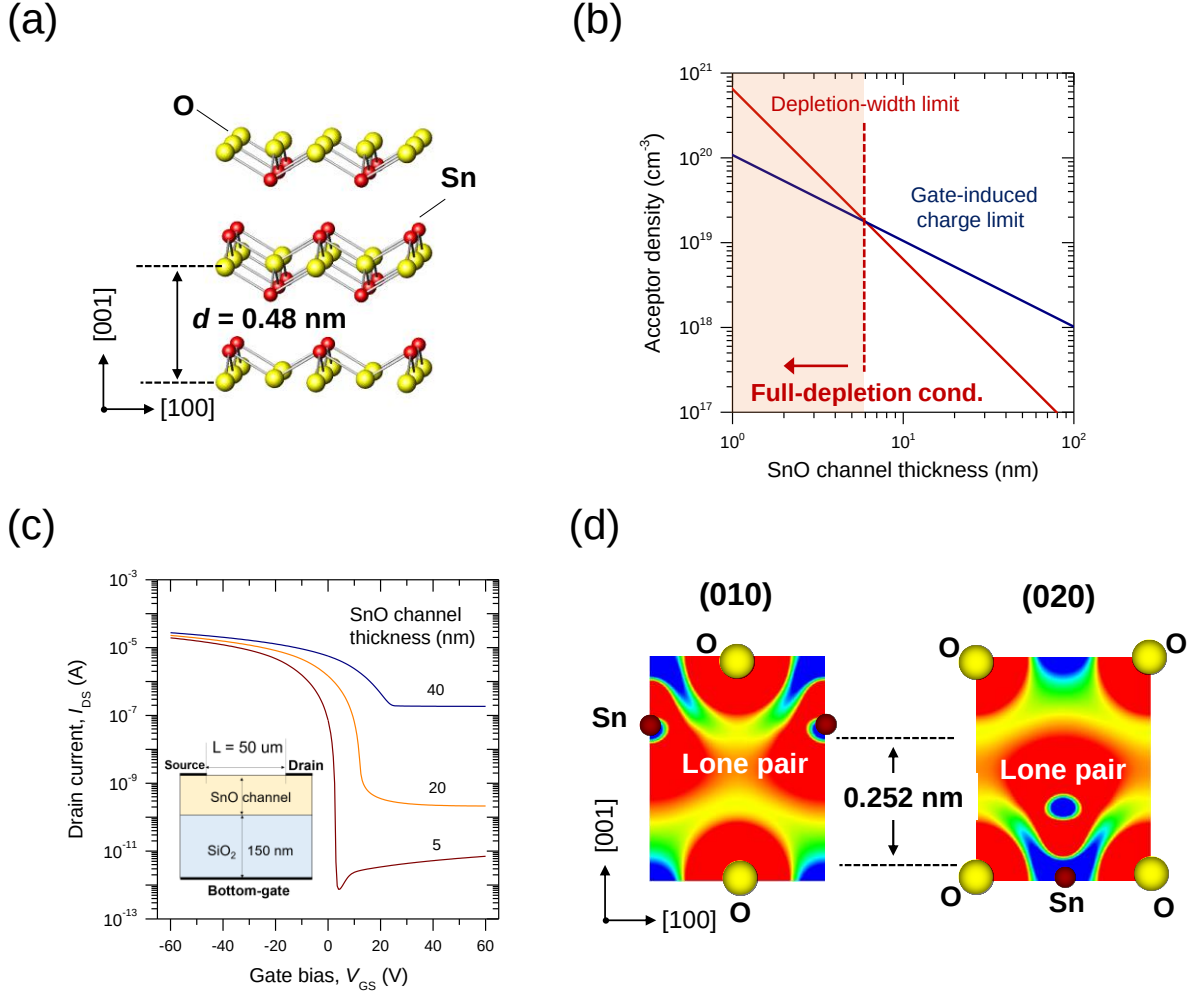


Figure 3.1 (a) The crystal structure of PbO-type SnO projected by [010] direction. The lattice constant (d) for the c-axis is 0.48 nm. (b) Ideal full-depletion condition for SnO channel with 150 nm-thick-SiO₂ gates with gate bias of 40 V. The red and blue lines indicate the depletion-width limits and gate-induced charge density limits. The intercept meets the full-depletion condition for the SnO channel. (c) The variation of transfer characteristics of *p*-channel SnO-TFT by different channel thicknesses from 40 to 5 nm was calculated by TFT device simulation. The inset shows the TFT structure models with a mesh width of 200 μm for the simulation. The acceptor density and the bandgap of SnO were set to 10^{18} cm^{-3} and 0.8 eV, respectively. (d) Different charge density isosurface plots at (010) and (020) planes in SnO unit-cell obtained by density functional theory calculation with VASP code using projected augmented wave (PAW) pseudopotentials and Perdew-Burke-Ernzerhof generalized gradient approximation (GGA-PBE) exchange-correlation functional. Sn 5s electrons do not contribute to the formation of chemical bonding and exist as lone pairs on Sn atom, which contributes to forming an interlayer gap with ~ 0.252 nm along [001] direction.

3.2 Experimental Section

Fabrication and characterization of atomically ultrathin SnO channel

Ultrathin SnO channel layers were prepared by printing the oxide skin from the liquid tin metal by touching a liquid-metal droplet with the thermally oxidized SiO₂/Si substrate. Elemental tin (Sn) (>99.99%, Shot Metals) was firstly melted on top of the glass substrate at ~230 °C in ambient air. The molten-Sn was then cooled down to 200 °C to avoid the formation of SnO₂. After the pre-existing top oxide layer of the molten-Sn was removed, the SnO layer was transferred from the molten-Sn to the substrate. The film surface structure was characterized by optical microscopy and atomic force microscopy (AFM). The film thickness was evaluated by measuring the edge height of the film using AFM. The film structures were examined by high-resolution transmission electron microscopy (HRTEM) with an acceleration voltage of 200 keV. For TEM analysis, ultrathin SnO nanosheets were directly transferred to the carbon film-coated TEM grid with 200 mesh using the same procedure. The selected area electron diffraction (SAED) pattern was obtained by fast-Fourier-transform (FFT). X-ray photoemission spectroscopy (XPS) measurements were carried out with Al $K\alpha$ ($h\nu = 1486.6$ eV). The samples were transferred into the XPS apparatus without an extra surface cleaning, and the binding energy was corrected by the C 1s core levels.

Defect passivation of SnO channel in TFT

Hydrogen thermal annealing was performed for 30 min in N₂ + H₂ (5% hydrogen) forming gas. The annealing temperature was varied from 150-250 °C. For the back-channel surface passivation, ~5 nm of aluminum oxide (Al₂O₃) passivation layer was deposited by atomic layer

deposition (ALD) with Trimethylaluminum precursor and H₂O at the deposition temperature of 80, 150, and 200 °C.

Fabrication of SnO thin-film by PLD

The SnO channels with a thickness of 7.5 to 16 nm were deposited by pulsed laser deposition (PLD) with a KrF excimer laser (wavelength 248 nm, pulse frequency 10 Hz) at room temperature (RT). A polycrystalline SnO-sintered body was used as a target of PLD. The oxygen partial pressure (PO₂) during the deposition was fixed at 2×10^{-4} Pa. The laser energy density was set to $\sim 1.5 \text{ J cm}^{-2}$. Similarly, the SnO films are subjected to post-hydrogen thermal annealing for 30 min in forming gas.

Thin-film transistor fabrication and electrical characterization

Thin-film transistors with inverted-staggered structures (bottom-gate and top source/drain contacts) were fabricated. The 150 nm-thickness-thermal-oxidized SiO₂ /n⁺-Si substrates were used as the gate oxide and gate electrode, respectively. The channel area was patterned using photolithography and defined by chemical wet-etching with 1 mol/l of diluted HNO₃ solution. Ohmic contact indium tin oxide (ITO) was used as the source and drain electrodes, defined by lift-off processes. The 40-nm thick ITO was deposited by PLD with oxygen partial pressure of 2×10^{-4} Pa at . The channel length (L) and the width (W) were 50 μm and 300 μm, respectively. The electrical characteristics were measured using the semiconductor parameter analyzer at room temperature in the dark.

3.3 Results and Discussion

The ultrathin SnO nanosheet was prepared on thermal oxidized SiO₂/Si substrates by liquid-metal printing under an ambient atmosphere.^[37-38] **Figure 3.2(a)** shows the optical microscope image of the as-synthesized SnO nanosheet, indicating that a large lateral-size SnO channel of > 1mm is easily prepared. **Figure 3.2(b)** also presents the atomic force microscopy (AFM) images of the SnO nanosheet. Polycrystalline surface structure feature composed of small crystal grains is observed, but the film surface was atomically flat with a surface roughness value, R_{RMS} of ~ 0.3 nm. The cross-sectional step-height profile on the edge of the nanosheet revealed that the sheet thickness is ~1 nm, which approximately corresponds to 2-3 monolayers of SnO. **(Figure 3.2(c)).** **Figure 3.2(d), (e)** show the low-magnified high-resolution TEM (HRTEM) images of the SnO nanosheet. The crystal grain boundary structures with different crystal orientations were observed, confirming the polycrystalline structure of SnO. The high-magnified HRTEM image showed a periodic atomic ordering arrangement with an internal spacing of ~0.27 nm, which assigns to (110) crystal plane spacing of SnO. **(Figure 3.2(f))** The corresponding selected area electron diffraction (SAED) pattern obtained by fast Fourier transform (FFT) was also shown as the inset of **Figure 3.2(f)**, confirming all the diffraction spots were assigned to (110) and (200) crystal planes of SnO. These material characterizations indicated that the presented material is an atomically thin poly-SnO channel.

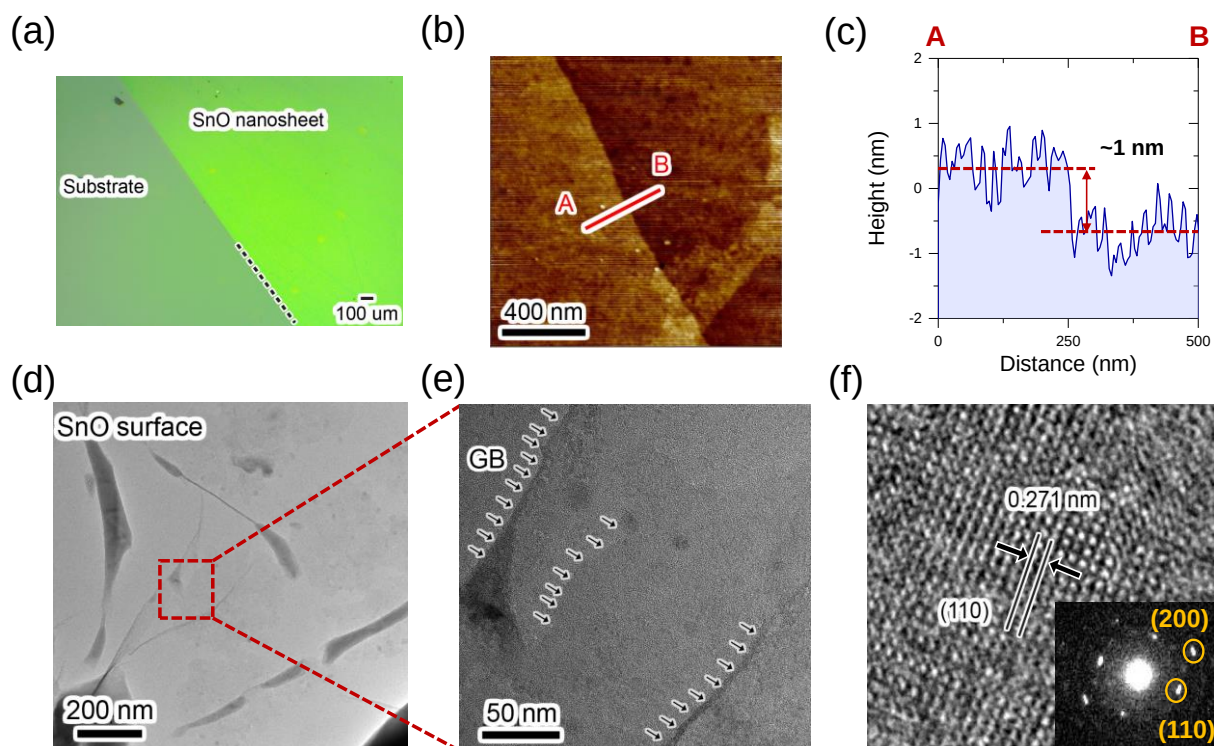


Figure 3.2 (a) Optical microscopy image of the as-synthesized SnO nanosheet prepared by the liquid-metal printing method. (b) AFM surface image of the SnO nanosheet with (c) cross-sectional step-height profile corresponds to the red line (A-B) as indicated. (d, e) The low-magnified HRTEM images of SnO nanosheet with different magnifications. The arrows in (e) point to the grain boundary (GB). (f) High-magnified HRTEM image. The inset shows the corresponding diffraction pattern extracted by fast Fourier transform.

An inverted staggered (i.e., bottom-gate and top-contact) structure TFT was fabricated using a ~1 nm-thick SnO channel on a SiO₂/p⁺-Si substrate. The schematics of the device structure and the optical microscope image of a source/drain configuration with channel width (W)/length (L) of 300/50 μm is also shown in **Figure 3(a), (b)**. **Figure 3(c), (d)** show typical TFT current-voltage (*I-V*) characteristics, i.e., transfer and output characteristics, for the as-synthesized SnO-TFTs. The drain currents ($|I_{DS}|$), measured by the source-to-drain voltage (V_{DS}), increase upon applying a negative gate bias (V_{GS}), which indicates that the device operates in a *p*-channel mode. The output characteristics show ohmic linear-relations at small V_{DS} regions and clear pinch-off behavior with the I_{DS} saturation, confirming the device operation follows the standard MOS-FET model. The important TFT device characteristics (i.e., saturation mobility (μ_{sat}), *s*-value, and threshold voltage (V_{th})) were determined as the following: the μ_{sat} is estimated by the following equation:

$$|I_{DS}| = \mu_{sat} C_{ox} (W/2L (V_{GS} - V_{th})^2) \quad (3.2)$$

where C_{ox} is the gate insulator capacitance per unit area. The *s*-value is extracted from the slope in the semilogistic with $s = (\partial \log I_{DS} / \partial V_{GS})^{-1}$. The V_{th} is determined from the intercept of a straight-line fit of the $(I_{DS})^{1/2} - V_{GS}$ plot. The pristine SnO TFT shows a μ_{sat} of ~3.5 cm²V⁻¹s⁻¹, a on/off current ratio of ~10⁴, an *s*-value of 7.75 V decade⁻¹, and a V_{th} of -2 V. These device performances are almost compatible with the reported SnO-TFTs (typical conventional SnO-TFT performances; mobility of ~1 cm²V⁻¹s⁻¹, on/off current ratio of ~10⁴, *s*-value of ~5-15 V decade⁻¹). HRTEM analysis revealed that the unannealed SnO channel involved a considerable amount of residual β -Sn metal. Therefore, the unexpected high mobility in the unannealed device is considered due to the drain current flow through the residual Sn metal in the SnO.^[14] Trap-state density, D_{it} is estimated from the *s*-values using the following relation:

$$s = \frac{\log_e 10 \cdot k_B T}{e} \left[1 + \frac{e D_{it}}{C_{ox}} \right] \quad (3.3)$$

where e is the elementary electric charge, k_B is Boltzmann constant, T is the temperature, t is the channel thickness, C_{ox} is the gate capacitance per area, D_{it} is the defect density near Fermi level. The calculated D_{it} was $\sim 1.9 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, indicating that the pristine SnO channel involved the high-density defect state.

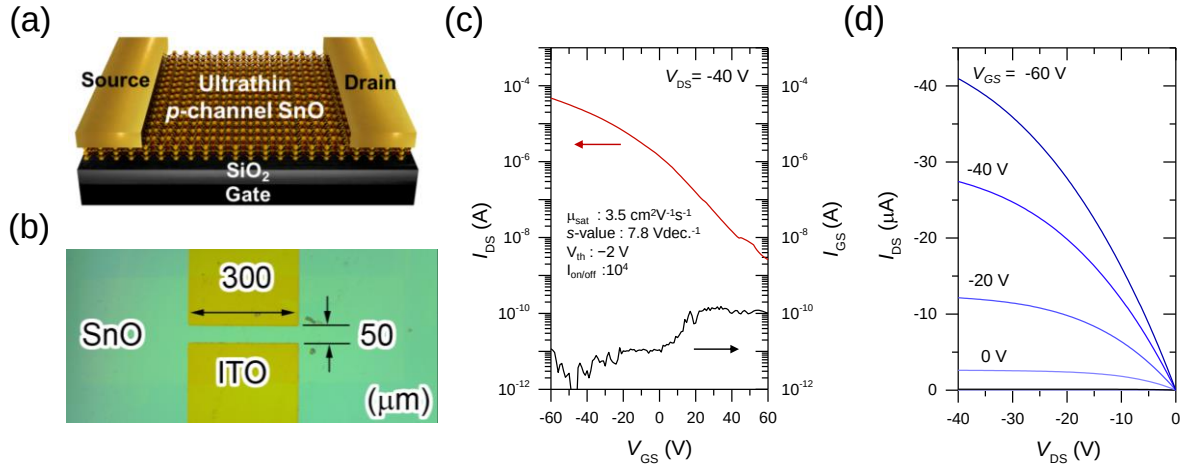


Figure 3.3 (a) Schematics of an inverted-staggered TFT structure for ultrathin SnO TFT. (b) Top-view optical image of source/drain electrode configurations. (c) Typical transfer characteristics with gate leak current (I_{GS}) and (d) output characteristics for ultrathin TFT using the as-synthesized pristine SnO channel.

The origin of the subgap defect state in the SnO channel is mainly considered oxygen-vacancy (Vo) defects, and thus, eliminating the Vo defect is essential to improving the device characteristics. Thus, we performed the subgap defect termination *via* a hydrogenation approach of SnO and atomic layer deposition (ALD)-Al₂O₃ back-channel passivation to improve the TFT performances.^[34, 36] **Figure 3.4(a),(b)** shows the variation of TFT characteristics for the ultrathin SnO TFT by hydrogen annealing at 250 °C and ALD-Al₂O₃ back-channel passivation. The fundamental device parameters (μ_{sat} , *s*-value, V_{th} , and on/off current ratio) are also summarized in **Figure 3.4(c)–(f)**. Significant improvement of the off-current and the *s*-value characteristics by hydrogen annealing was observed, which is consistent with previous reports.^[34, 36] The hydrogenated SnO-TFTs exhibited reasonably high μ_{sat} of $\sim 1.1 \pm 0.19 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, large on/off current ratio of $9 \pm 4.6 \times 10^4$, *s*-value of $4.9 \pm 1.0 \text{ V decade}^{-1}$ and V_{th} of $-2.3 \pm 2.3 \text{ V}$. However, the high off-current of $\sim 10^{-10} \text{ A}$ was retained.

To further improve the device performances, $\sim 5\text{-nm}$ -thick ALD-Al₂O₃ passivation was performed at 150 °C.^[29, 34, 46] The TFT mobility was slightly degraded after the back-channel passivation. However, a significant reduction of off current as low as 10^{-12} A was observed, which nearly corresponds to the measurement limit in our device test system. The passivated device showed the μ_{sat} of $\sim 0.47 \pm 0.18 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, *s*-value of $2.5 \pm 0.39 \text{ V decade}^{-1}$, and on/off current ratio of $5 \pm 4.1 \times 10^5$. The presented SnO-TFT exhibits the best performances in all the reported nonvacuum (i.e., solution)-processed *p*-channel oxide-TFTs. Compared with reported PVD-processed SnO TFTs, the presented SnO TFT showed a significantly improved on/off current ratio originating from the reduction of the off-current

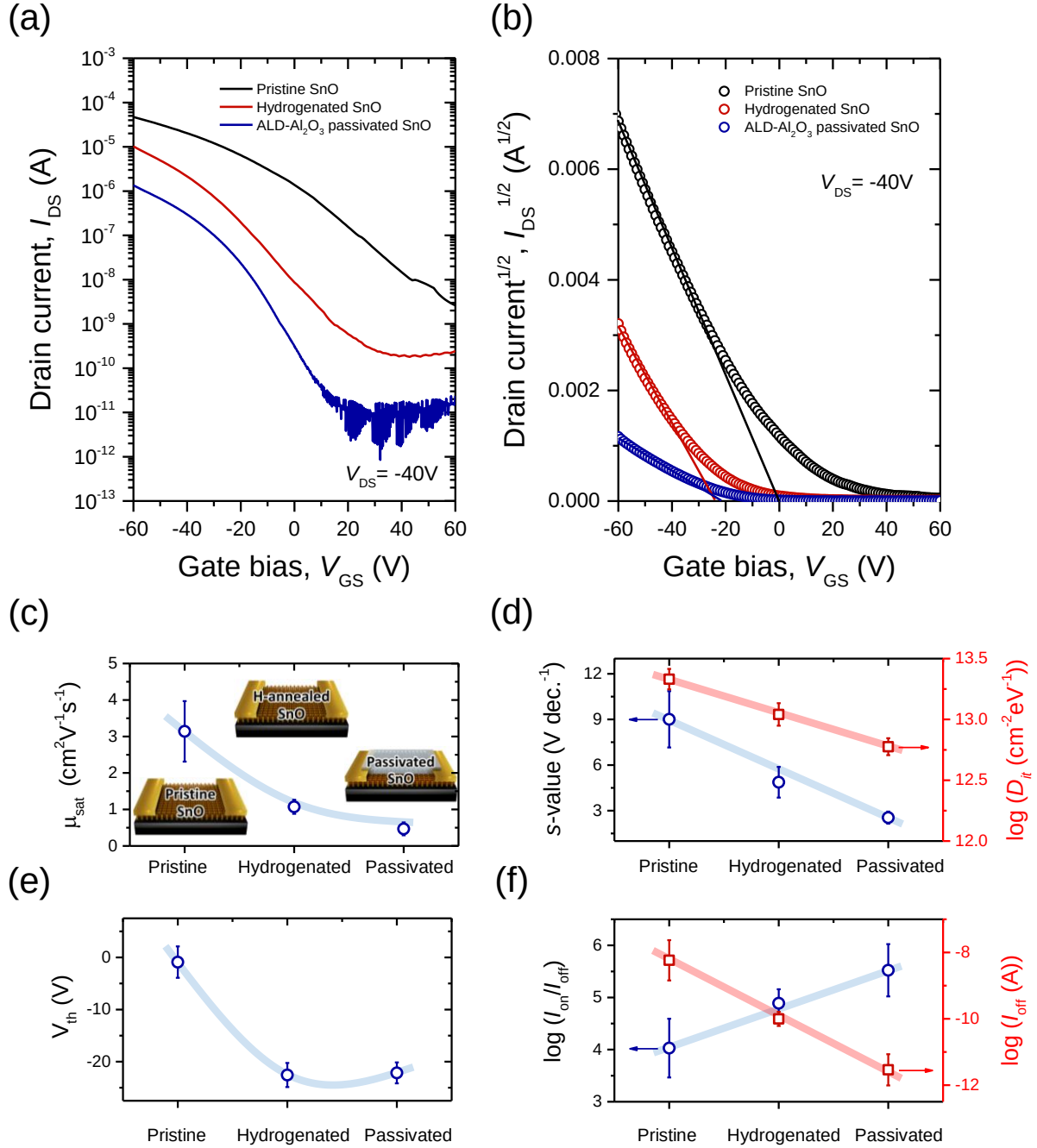


Figure 3.4 (a) Variation of transfer characteristics by defect termination process, including 250°C-hydrogen annealing and ALD- Al_2O_3 passivation for ultrathin SnO-TFTs. The black line shows the transfer curve for the pristine device. (b) Corresponding variation of $I_{DS}^{1/2}$ – V_{DS} characteristics. The corresponding TFT parameters, (c) μ_{sat} , (d) s-value and D_{it} , (e) V_{th} , and (f) on/off current ratio and off-current, were plotted.

Figure 3.5 also plots the TFT parameters as a function of the channel thickness for SnO TFTs. The thicker SnO channel with > 7 nm was prepared by PLD with post-hydrogen annealing at 250 °C for 30 min. We confirmed linear relationships between all the TFT parameters and the channel thickness, which is a reasonable tendency in depletion-operated TFT. The μ_{sat} shows clear channel thickness dependence, and the μ_{sat} of $\sim 1.84 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ is decreased to $\sim 1.1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ by thinning the channel thickness. **(Figure 3.5(a))** Since the SnO channel is polycrystalline, the trend is often observed in SnO TFT due to the effect of crystal grain size, which became smaller in thinner film thickness.^[15] The s -values are also linearly varied from ~ 30.2 to $\sim 4.9 \text{ Vdecade}^{-1}$ as the channel thickness decreases from 16 to 1 nm, indicating that the SnO channel bulk defect is reduced in the ultrathin SnO TFTs. **(Figure 3.5(b))** The total D_{it} calculated from the s -values of transfer curves involves both the interface (D_{it}) and the channel bulk trap density (N_{sg}). It can be separately estimated from the channel thickness dependency of the s -value by replacing D_{it} with $D_{\text{it}} + tN_{\text{sg}}$, which gives the D_{it} of $\sim 2.9 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ and the N_{sg} $\sim 4.4 \times 10^{19} \text{ cm}^{-2}\text{eV}^{-1}$ for the hydrogenated SnO TFTs.

Additionally, we calculated the intrinsic back-channel surface trap density and back-channel interface trap density with the ALD- Al_2O_3 passivation layer based on the induced gap state (IGS) theory.^[47] The intrinsic back-channel surface state density (D_{SS}) was estimated by

$$D_{\text{SS}} = \frac{C_i}{q} \cdot \left(\frac{1}{S_S} - 1 \right) \quad (3.4)$$

where S_S is interface parameter calculated by $[1 + 0.1 (\varepsilon_{\infty\text{SR}} - 1)^2]^{-1}$, C_i is the capacitance density of the surface dipole, $C_i = \varepsilon_{\infty\text{S}}/\delta$, in which $\varepsilon_{\infty\text{SR}}$ is the semiconductor optical relative dielectric constant, $\varepsilon_{\infty\text{S}}$ is the corresponding dielectric constant, δ is the microscopic dipole thickness. The interface state density (D_{IS}) is obtained by

$$D_{IS} = \frac{C_i}{q} \cdot \left(\frac{1}{S_{IS}} - 1 \right) \quad (3.5)$$

where

$$S_{IS} = \left\{ 1 + 0.1 \left[\frac{(\varepsilon_{\infty IR} - 1)^2 (\varepsilon_{\infty SR} - 1)^2}{\left[\frac{(\varepsilon_{\infty IR} - 1)^2 C_{iI}}{(C_{iI} + C_{iS})} + \frac{(\varepsilon_{\infty SR} - 1)^2 C_{iS}}{(C_{iI} + C_{iS})} \right]} \right] \right\}^{-1} \quad (3.6)$$

C_i is the capacitance density of the interface dipole, which is estimated by the following equation:

$$C_i = \frac{C_{iI} C_{iS}}{(C_{iI} + C_{iS})}, C_{iI} = \frac{\varepsilon_{\infty I}}{\delta_I}, C_{iS} = \frac{\varepsilon_{\infty S}}{\delta_S} \quad (3.7)$$

where $\varepsilon_{\infty IR}$ and $\varepsilon_{\infty SR}$ are the insulator and semiconductor optical relative dielectric constants, respectively; $\varepsilon_{\infty I}$ and $\varepsilon_{\infty S}$ are the insulator and semiconductor dielectric constants, respectively. The intrinsic D_{SS} was estimated as $\sim 2.1 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, while $\sim 9.3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ was obtained for the ALD Al_2O_3 -passivated TFT. These values are nearly comparable with the measured D_{it} , and it implies that the back-channel interface defect mainly controls the TFT performances in SnO-TFTs. The analysis also confirms that the ALD Al_2O_3 passivation effectively reduces the back-channel surface defects for the ultrathin SnO channel.

Figure 3.5 (c),(d) also shows the variation of V_{th} and off-current by the channel thickness. The V_{th} was changed from 30.9 V to -22.6 V as the channel thickness reduced from 16 to 1 nm. **(Figure 5(c))** In general, the V_{th} is generally altered by the acceptor density and the charged defects in the channel region. However, the film thickness does not change the acceptor density of SnO film.^[15] Thus, the variation of V_{th} is caused by the reduction of charged defects in the SnO channel. The off current is significantly reduced with a decrease in the channel thickness, leading to the large on/off current ratio of $\sim 10^6$ for an ultrathin channel. **(Figure 5(d))** The result is in good

agreement with the TFT simulations (**Figure 3.1(c)**) and indicates that the ultrathin channel improves the TFT performances of depletion-mode SnO TFTs.

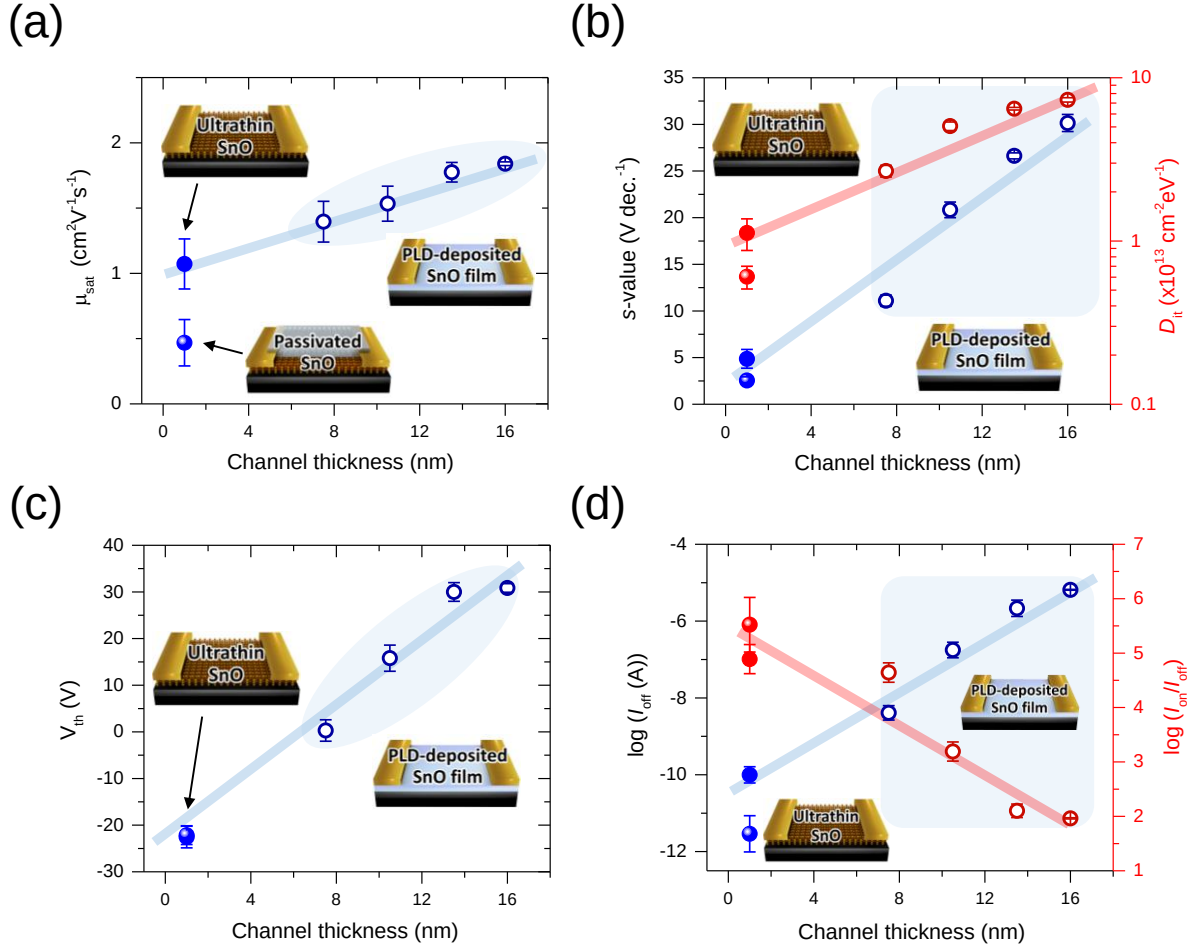


Figure 3.5 Fundamental TFT parameters (a) μ_{sat} , (b) s -value and D_{it} , (c) V_{th} , (d) off current and on/off current ratio) were plotted as a function of the channel thickness for *p*-channel SnO TFT, including the ultrathin channel and PLD-deposited thick channels prepared with hydrogen annealing.

Finally, we fabricated *n*-channel oxide TFTs using ultrathin channels of *n*-type SnO₂ and In₂O₃ by the same liquid-metal printing methods and developed the ultrathin oxide-TFT-based complementary inverter circuits. The typical transfer characteristics for both the ultrathin *p*-channel SnO and *n*-channel SnO₂-TFTs used in the oxide-TFT-CMOS inverter are shown in **Figure 3.6(a)**. The *n*-channel SnO₂-TFT shows a μ_{sat} of $\sim 2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, an *s*-value of $\sim 4.5 \text{ V/decade}$, a V_{th} of $\sim -16.5 \text{ V}$, and an on/off current ratio of $\sim 2 \times 10^4$. The corresponding TFT performances for *p*-channel SnO TFT are a μ_{sat} of $\sim 0.2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, an *s*-value of $\sim 1.9 \text{ V/decade}$, a V_{th} of $\sim -20 \text{ V}$, and an on/off current ratio of $\sim 10^6$, respectively. **Figure 3.6(b)** shows the typical voltage transfer characteristics (VTC), which are the output voltage (V_{out}) as a function of the input voltage (V_{in}) with supply voltage (V_{DD}). The inset illustrates the schematic circuit diagram of the oxide CMOS inverter using ultrathin *n* and *p*-channel oxideTFTs. The output voltage switches from high to low, confirming a clear voltage inversion action with the full voltage swing. The voltage gains of the inverter, which was defined as $-dV_{\text{out}}/dV_{\text{in}}$, were estimated as ~ 3 , ~ 5 , ~ 7 at V_{DD} from 30 to 50V, respectively. (The bottom of **Figure 3.6(b)**) **Figure 3.6(c)** also shows the supply currents (I_{DD}) of the ultrathin *p*-SnO/*n*-SnO₂-TFT-CMOS inverter as functions of V_{in} . The static currents were below $\sim 0.1 \text{ nA}$, and the static power dissipations, which are defined by $P_{\text{static}} = V_{\text{DD}} (I_{\text{static_low}} + I_{\text{static_high}}) / 2$, were less than 4 nW per logic gate. The maximum output-power consumption (P_{out})^[48] was also estimated as $\sim 200 \text{ nW}$ (the bottom of **Figure 3.6 (c)**), which was high due to the insufficient off-state characteristics of ultrathin *n*-SnO₂ TFTs.

We successfully improved the oxide CMOS inverter performances by using ultrathin *n*-channel In₂O₃ TFT with the improved TFT performance metric, including μ_{sat} of $\sim 12.8 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, *s*-value of $\sim 0.43 \text{ V dec.}^{-1}$, V_{th} of $\sim 4 \text{ V}$, and on/off current ratio of $\sim 10^8$. (**Figure 3.6(d)**). **Figure**

3.6(e) shows the VTC for the oxide CMOS inverter composed of ultrathin p -SnO/ n -In₂O₃ TFTs. The VTC exhibited clear signal switching with rail-to-rail output swings and sharper voltage transition between the two states with a high voltage gain of 117 at $V_{DD} = 40$ V (the bottom of **Figure 3.6(e)**). The maximum voltage gain reached ~ 330 at $V_{DD} = 40$ V, which was nearly comparable to the best-recorded values for oxide-TFT-based CMOS inverters.^[49-50] The static I_{DD} was further suppressed to ~ 0.05 nA, leading to lower static power dissipation of less than ~ 2 nW. **(Figure 3.6(f))** The P_{out} value was only ~ 58 nW per logic gate, indicating that the device can be operated by a nanowatt power source. These desirable CMOS characteristics were attributed to the low off-current nature of ultrathin p - and n -channel oxide TFTs.

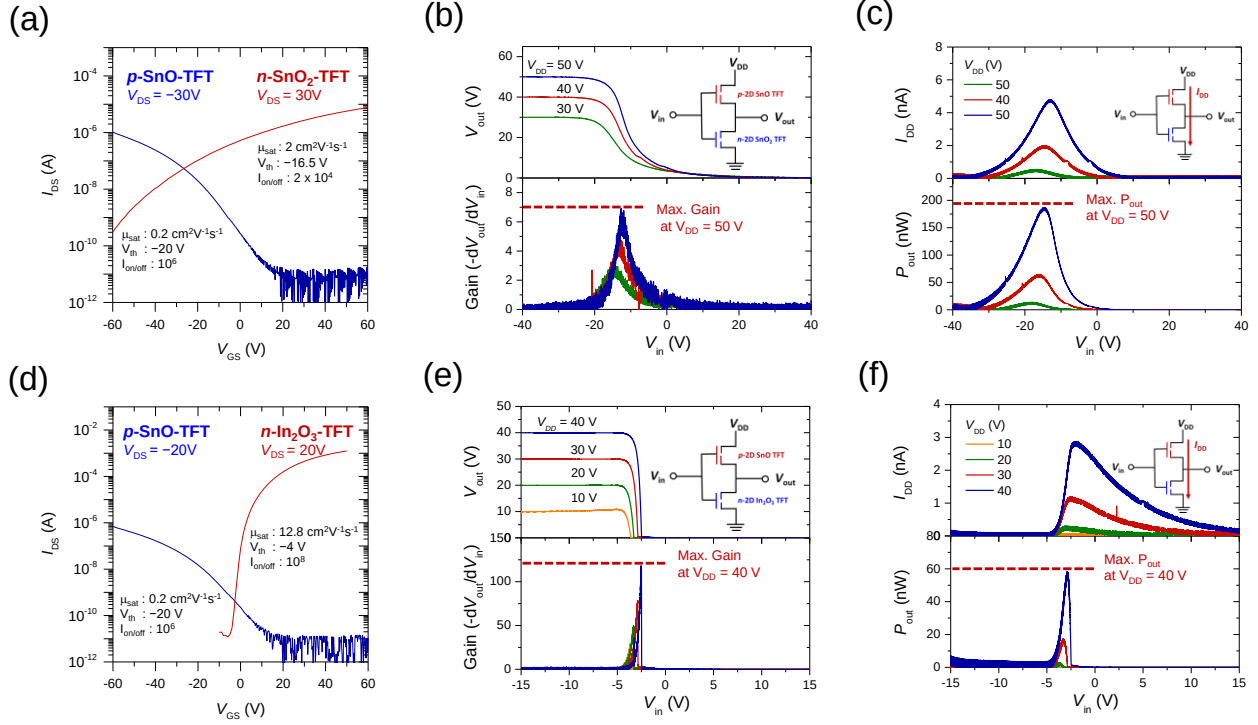


Figure 3.6 (a) Transfer characteristics of ultrathin p -SnO TFT with $V_{DS} = -30$ V and n -SnO₂ TFTs at $V_{DS} = 30$ V. (b) Voltage transfer characteristic (VTC) and the corresponding voltage gains of the p -SnO/ n -SnO₂-TFT-CMOS inverter. Inset: the schematic of the corresponding oxide-TFT-CMOS inverter circuit. (c) Supply currents (I_{DD}) and output-power consumption (P_{out}) for the p -SnO/ n -SnO₂-TFT CMOS inverter. (d) Transfer characteristics of a p -SnO TFT with $V_{DS} = -20$ V and n -In₂O₃ TFT at $V_{DS} = 20$ V. (e) VTC and the corresponding voltage gains of the p -SnO/ n -In₂O₃-TFT-CMOS inverter. Inset: the schematic of the corresponding CMOS inverter circuit. (f) I_{DD} and P_{out} for of p -SnO/ n -In₂O₃-TFT CMOS inverter.

3.4 Conclusions

Atomically thin SnO channels with ~ 1 nm-thickness were developed by a vacuum-free, solvent-free liquid-metal printing method at the maximum process temperature of $250\text{ }^{\circ}\text{C}$ to improve the device performances of fully-depleted-type *p*-channel SnO TFTs. Even the as-synthesized SnO-TFTs showed decent *p*-channel transistor operation with a μ_{sat} of $\sim 3.5\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, an on/off current ratio of $\sim 10^4$, an *s*-value of $\sim 7.75\text{ V decade}^{-1}$ and V_{th} of -2 V . The significant improvement in the off-current characteristics less than $\sim \text{pA}$ was achieved in ultrathin SnO TFTs by performing channel defect terminations. The presented atomically thin *p*-channel SnO-TFT exhibited a μ_{sat} of $\sim 0.5\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, a low off current of $\sim 10^{12}\text{ A}$, an on/off current ratio of $\sim 10^6$, and an *s*-value of $\sim 2.5\text{ V decade}^{-1}$. The low-power oxide-TFT-based CMOS inverter was developed using *n*-channel oxide TFTs with ultrathin *n*-SnO₂ and *n*-In₂O₃ channels, exhibiting a high voltage gain of ~ 120 (Maximum: ~ 380) and the low-power operation of $< 58\text{ nW}$ for *p*-SnO / *n*-In₂O₃-TFTs-based-CMOS inverter. Although this work was performed on small-sized substrates with $10 \times 10\text{ mm}^2$, metal-liquid printing can potentially be used for fabricating large-scale electronics by increasing the liquid-metal area. The presented work demonstrated a high potential of oxide-TFT-based CMOS logic development using atomically ultrathin channel oxide-TFT and promises new opportunities in next-generation energy-efficient, cost-effective oxide TFT technology with vacuum-free, solvent-free, and low-temperature processing.

Chapter 3, in full, is a reprint of the material as it appears in ACS Applied Materials & Interfaces 13, 52783-52792, 2021. Chi-Hsin Huang, Yalun Tang, Tzu-Yi Yang, Yu-Lun Chueh and Kenji Nomura. The dissertation author was the primary investigator and author of this paper.

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Chapter 4 Low-Temperature Crystallization Enabled by Pressure-Assisted Liquid-Metal Printing for β -Ga₂O₃ Thin-Film Transistors

4.1 Introduction

The demand for sustainable high-performance electronic devices and integrated circuits has been on the rise, especially for advanced device applications such as flexible displays^[1], lightweight wearable electronics and sensors^[2-3], electronic skin^[4-5], Internet of Things^[6], and BEOL-compatible transistors for three-dimensional highly-integrated circuits^[7]. To develop these device applications, it is crucial to explore novel low-temperature semiconductor device fabrication processes that not only reduce production costs but also minimize the environmental impact of electronic devices, significantly contributing to the development of sustainable electronics. Therefore, enormous efforts to develop semiconductor materials and device processing have been devoted to paving the way for the realization of environmentally friendly and cost-effective sustainable electronics.^[8-16]

In recent years, a variety of semiconductor materials such as organics and oxide semiconductors have been developed for low-temperature and cost-effective processing such as solution process and ink-jet printing.^[8-15, 17] Among these materials, ionic metal oxide semiconductors, composed of post-transition metals, such as a-In-Ga-Zn-O (a-IGZO), In₂O₃, ZnO, SnO₂ have emerged as promising electronic materials to develop low-temperature processed and cost-effective, ubiquitous electronics. In general, it is well known that structural defects are a common issue in low-temperature material/device processing, causing severe degradation of electrical properties in conventional semiconductors. However, *n*-type oxide semiconductors are

less sensitive to structural defects due to their unique electronic structure nature, and electron transport is not significantly hindered.^[18] This advantage offers a great opportunity to develop low-temperature processed electronic devices.

Currently, there have been significant advancements in the development of solution-processed oxide-based thin-film transistors (oxide TFTs), leading to several high-performance *n*-channel oxide TFTs.^[19-25] However, an additional device fabrication process, such as post-thermal annealing, is generally required to achieve a device-quality semiconducting channel for TFT applications. A post-annealing process for oxides typically involves relatively high temperatures (usually between 300–600 °C) and can potentially negate the advantages of oxide semiconductors for low-temperature processed electronic devices.^[19-22, 24-25] Additionally, precise control of the processing atmosphere is often necessary, even in solution processes.^[25-26] As a result, there is a high demand for oxide-based device processing at low temperatures, vacuum-free, and non-controlled atmospheric circumstances.

β -gallium oxide (β -Ga₂O₃) is a well-known *n*-type wide-bandgap oxide semiconductor with ultra-large wide-bandgap nature of 4.4–4.9 eV and relatively high electron mobility of 100–200 cm²V⁻¹s⁻¹ ^[27-30] for a wide field of device applications such as deep-ultraviolet (DUV) optoelectronics^[31-33], power electronics operated in high-electrical fields (~ MV/cm) and high-temperature devices (250–300 °C). ^[34-36] The wide-bandgap nature of Ga₂O₃ is especially advantageous for designing devices capable of operating in harsh environments, such as extreme environment sensors, space-based applications, and terrestrial applications. Additionally, β -Ga₂O₃ is expected to develop energy-efficient operable transistors with low power consumption due to

the extremely low-channel leakage (i.e., off-current) nature originating from the low intrinsic carrier concentration and wide bandgap. Therefore, Ga₂O₃ holds promise as a semiconductor material for microelectronics, and several demonstrations of high-performance β -Ga₂O₃ transistors have already been achieved. Current research on β -Ga₂O₃ transistors primarily focuses on metal-oxide-semiconductor field-effect transistor (MOSFET) structures using bulk single-crystal wafers for power devices. However, developing β -Ga₂O₃ TFTs remains challenging due to the high-temperature process required for β -Ga₂O₃ film growth in conventional physical vapor deposition (PVD) methods. Nevertheless, low-temperature processes for Ga₂O₃ TFTs show promise for various practical applications, such as low-power switching devices and solar-blind deep-ultraviolet photodetectors, originating from their ultra-wide bandgap nature. (**Figure 4.1**)

To date, high-performance Ga₂O₃ transistors use electron-doped single-crystal β -Ga₂O₃ channels, which are grown at a high temperature of $> 600\text{ }^{\circ}\text{C}$ [34-35, 37-38] and prepared using a mechanical exfoliation process.^[39-41] Recently, amorphous and polycrystalline β -Ga₂O₃ TFTs have also been demonstrated, but achieving good TFT device operations still requires high process temperatures (200–900 $^{\circ}\text{C}$).^[42-45] Moreover, the mobility of the previously reported Ga₂O₃ TFTs is only limited to $< 2\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, which is insufficient for high-performance device applications.^[42-45] Thus, developing a low-temperature process for β -Ga₂O₃ thin film with high mobility is critical to advancing the field of ultra-wide bandgap oxide semiconductor electronic devices. Furthermore, Ga₂O₃ emerges as the next promising channel material in TFT technology to significantly reduce off-current and power consumption compared to the currently commercialized IGZO TFTs.

In this work, we proposed a solvent-free, vacuum-free, pressure-assisted liquid metal printing method called PA-LMP to fabricate high-performance β -Ga₂O₃ TFTs. The LMP method is proposed for forming high-quality crystalline oxide materials with superior electrical properties compared to conventional physical/chemical vapor thin-film deposition, owing to its distinct thermodynamic pathway.^[46-47] Therefore, LMP method has already been demonstrated to develop high-mobility Indium-based *n*-channel oxide TFTs.^[46] Here, the PA-LMP approach, which involves applying external uniaxial pressure during oxide skin formation on liquid metal, is firstly demonstrated to directly form high-quality polycrystalline β -Ga₂O₃ nanosheets at a low temperature of 150°C under a non-controlled ambient air atmosphere, exhibiting excellent transistor operation. The presented *n*-channel β -Ga₂O₃ TFTs exhibited excellent electrical characteristics with a high saturation mobility of 11.7 cm²V⁻¹s⁻¹, on/off-current ratio of $\sim 10^9$, and subthreshold swing of 163 mV·decade⁻¹. Additionally, we successfully demonstrated a zero- V_{GS} -load NMOS inverter composed of enhancement/depletion-mode β -Ga₂O₃ TFTs and an all-oxide-based CMOS inverter using liquid metal printed *p*-channel SnO TFTs. These inverters operated in rail-to-rail full-swing voltage transfer operations with high voltage gain and low static power dissipation.

4.2 Experimental Section

Synthesis of gallium oxide nanosheet

Atomically thin Ga_2O_3 nanosheets were fabricated by printing the oxide skin from the liquid gallium (Ga) metal. The liquid Ga metal was prepared by melting elemental Ga (99.99% purity, Shot Metals) inside a glass vial on a hot plate at 50°C in ambient air.

To fabricate the nanosheets, a liquid droplet of the liquid Ga metal (with a size of ~1 to ~5mm) was placed on a SiO_2/Si substrate using a pipette, and the substrate with liquid metal droplet was heated to the desired process temperature (80–200 °C), which is above the melting point of the liquid Ga metal. The surface of a SiO_2/Si substrate was treated with O_2 plasma (rf power = 70 W for 1 min) and pre-heated to the desired process temperature (80–200 °C) before a liquid Ga droplet was dropped on it. During the printing process, a second substrate (also treated with O_2 plasma and pre-heated to process temperature) was pressed onto the center of the droplet to spread the liquid alloy homogeneously between the two substrates. The two substrates were kept at process temperature (80–200 °C) and under uniaxial vertical pressure for the gallium oxide nanosheet growth for 3 minutes. When the printing process time was too long (>10 min), the channel exhibited insulating behavior, rendering the TFTs inoperative. After the squeezing step with uniaxial vertical pressure, the top substrate was lifted vertically and separated without lateral slippage. Then, homogeneous ultrathin Ga_2O_3 nanosheets were exfoliated onto both substrates. The strong van der Waals bond between the oxide skin and the substrate facilitated the delamination of the oxide.

Metal inclusions attached to the exfoliated nanosheets could be removed by gently rubbing the SiO₂/Si wafer, which was submerged in ethanol, with a soft wiping tool (cotton bud). The Ga₂O₃ nanosheets were found to be firmly attached to the SiO₂ surface due to strong van der Waals adhesion between the nanosheets and the substrate, and they remained intact throughout the cleaning procedure. The large-area atomically thin Ga₂O₃ nanosheets exceeding several centimeters in lateral dimensions could be fabricated efficiently using this method.

TEM sample preparation procedure

First, the TEM grid was placed on top of the glass slide and pre-heated to process temperature (80–200 °C), which is above the melting point of the liquid Ga metal. Note that we did not perform O₂ plasma treatment for the TEM sample, as we did for the Ga₂O₃ nanosheet on the SiO₂/Si substrate.

To fabricate the nanosheets, a liquid droplet of Ga metal (with a size of <1 mm) was pipetted onto a TEM grid, and the TEM grid/glass slide with the liquid metal droplet was kept heated at 50°C to prevent the liquid Ga from solidifying. During the printing process, we used SiO₂/Si as the top substrate (pre-heated to process temperature (80–200 °C)), pressing it onto the center of the droplet to spread the liquid alloy homogeneously between the TEM grid and SiO₂/Si substrates. The TEM grid and SiO₂/Si substrates were kept at process temperature (80–200 °C) under uniaxial vertical pressure for gallium oxide nanosheet growth for 3 minutes.

After the squeezing step with uniaxial vertical pressure, the top SiO₂/Si substrate and TEM grid were carefully separated. We then used a soft wiping tool (cotton bud) to remove Ga liquid

inclusions directly by gentle rubbing. It is important to note that we did not immerse the sample in ethanol, as we did for the Ga₂O₃ nanosheet on the SiO₂/Si substrate. Following the printing process, we observed that most carbon film was broken. During TEM analysis, we looked for nanosheets suspended and connected/supported by the bar of the TEM grid for detailed analysis.

Materials characterization

The surface structure of the nanosheet was analyzed using both optical microscopy and atomic force microscopy (AFM). The nanosheet thickness was determined by measuring the height of the patterned edge using AFM. The detailed crystal structures of the Ga₂O₃ nanosheets were examined using high-resolution transmission electron microscopy (HRTEM) with an acceleration voltage of 200 keV. The selected area electron diffraction (SAED) pattern was obtained using a fast Fourier transform (FFT).

Thin-film transistor fabrication and electrical characterization

Thin-film transistors were fabricated with inverted-staggered structures, i.e. bottom-gate and top source/drain contacts. The 150-nm-thick thermal-oxidized SiO₂/n⁺-Si substrates were used as the gate oxide and gate electrode. The channel area was patterned using photolithography and defined by chemical wet-etching with 1 mol/l of diluted HNO₃ solution. The source and drain electrodes were made of ohmic contact 40 nm-thick indium tin oxide (ITO), which was deposited by pulsed laser deposition (PLD) with an oxygen partial pressure of 2×10⁻⁴ Pa at room temperature. The channel length (*L*) and the width (*W*), which are defined by metal mask processing, were 100 μm, and 300 μm, respectively. The electrical characteristics were measured using the semiconductor parameter analyzer at room temperature in the dark.

Device simulation

Two-dimensional simulations of the TFTs cross-section were conducted using a 2D ATLAS TCAD simulator (Silvaco) to gain insight into the electronic and defect structures of TFTs. The simulations utilized the same configuration and materials as the TFT devices. The parameters used in the simulations are listed in **Table 4.1**.

4.3 Results and Discussion

A family of Ga_2O_3 is known to consist of five crystalline polymorphic forms, namely α , β , γ , δ , and ε phases. The monoclinic β - Ga_2O_3 phase is the most stable, with lattice constants of $a = 1.22$ nm, $b = 0.30$ nm, and $c = 0.58$ nm, and it exhibits excellent thermal stability^[33, 48] (as shown in **Figure 4.1(b)**). **Figure 4.1(b)** summarizes the transformation relationships among the five polymorphic forms of Ga_2O_3 under equilibrium conditions. The α and γ forms are metastable and can be easily formed from GaO hydrate and gel forms and then transform to β -phase. However, to achieve the β - Ga_2O_3 phase from these metastable phases, a high-temperature process of at least 300 °C is required.^[49]

On the other hand, a β - Ga_2O_3 thin film can be directly grown by several physical vapor deposition (PVD) techniques, such as sputtering and pulsed laser deposition. However, high-temperature substrate heating and post-deposition annealing, typically over 500 °C, are required for the thin-film growth process.^[44, 50] These results imply that low-temperature growth of β - Ga_2O_3 is very challenging in conventional thin-film growth approaches. The liquid metal printing approach can form crystalline and highly conductive oxide films upon deposition, avoiding insulating intermediate phases and eliminating the thermodynamic barriers posed by precursor decomposition^[46-47], which is typical in the traditional approach to growing β - Ga_2O_3 . The traditional processes involve the formation of GaO hydrate and gel forms, which then transform into the β -phase during subsequent processing. (**Figure 4.1(b)**) We believe the oxidation process of the liquid metal presents different thermodynamic barriers and pathways for growing oxide materials, potentially making it easier to produce high-quality oxide materials at lower process temperatures. Furthermore, additional energy sources to modify thermodynamic parameters for

crystallization are needed to overcome this issue and lower the growth temperature. It is considered that the external environmental pressure is a typical fundamental thermodynamic parameter and kinetic variable for the free energy change of the materials system defined by $\Delta G_f = \Delta(E + PV) - T\Delta S$, where E is internal energy, P is pressure, V is volume, T is temperature, and S is entropy.^[51] External pressure provides the opportunity to facilitate the crystallization process of oxide materials and lowers the crystallization temperature.^[52] Therefore, we newly developed a novel method for low-temperature growth of β -Ga₂O₃ using external uniaxial pressure-liquid metal printing.

Figure 4.1(c) shows a schematic illustration of the PA-LMP method for fabricating Ga₂O₃ nanosheets under ambient air. The liquid-metal printing process was performed at 150 °C under an external uniaxial pressure of approximately 0.3 kgf/cm². (printing process temperatures (T_p) of 150 °C and process pressure (P_p) of 0.3 kgf/cm²) The process steps are described in detail in Experimental Section. The nanometer-thin surface oxide of liquid Ga is formed by self-limiting Cabrera–Mott oxidation in the ambient air to grow the Ga₂O₃ nanosheets. The optical microscope images and photographs of the Ga₂O₃ grown by previously reported liquid metal printing (LMP)^[53-56] and the proposed PA-LMP method show that these samples exhibit large-scale Ga₂O₃ nanosheets with dimensions of around 1×1 cm². (**Figure 4.1(a), (b)**) The entire laterally large Ga₂O₃ layer is continuous and without significant holes and cracks under optimized synthesis operations. shows additional optical microscope images of the Ga₂O₃ nanosheet fabricated by the different printing process parameters.) **Figure 4.2(a)** displays an atomic force microscopy (AFM) image of nanosheets grown by the previously reported and proposed PA-LMP method. The edge step height profile of these nanosheets found that the thickness was approximately 3.0 nm for both

films. The root-mean-square of surface roughness (R_{RMS}) of the Ga_2O_3 nanosheets grown using LMP and PA-LMP methods were measured to be approximately 1.16 and 0.64 nm, respectively, comparable to the R_{RMS} of SiO_2 surface (approximately 1.0 nm). These results suggest that the surface roughness of the Ga_2O_3 nanosheets is primarily due to the underlying SiO_2/Si substrate. Moreover, the presented Ga_2O_3 nanosheets were homogeneously and conformally grown on the substrates. Therefore, it was also confirmed that the developed pressure-assisted liquid-metal printing enabled the direct printing of large-area oxide materials onto various substrates, including SiO_2/Si , III-V (GaAs), transparent glass, paper, and flexible plastic substrates like PET, allowing the development of versatile applications by integrating diverse functional materials and substrates.

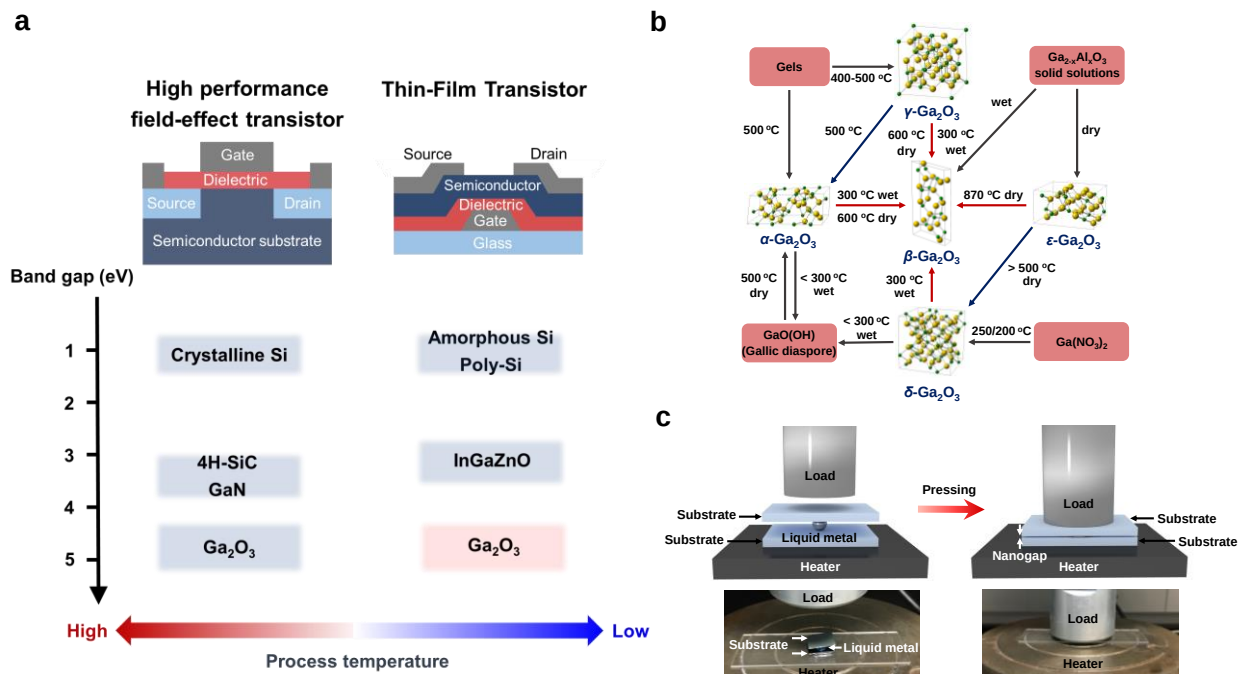


Figure 4.1(a) Motivation and purpose for developing low-temperature processed wide-bandgap Ga₂O₃ thin-film transistors. (b) Phase transformation relationship for Ga₂O₃ polymorphism. (b) Schematic and photographs of the developed pressure-assisted liquid metal printing routes for Ga₂O₃ nanosheet fabrication.

We fabricated inverted-staggered (i.e., bottom-gate and top-contact) structured TFT devices using the Ga₂O₃ nanosheets as a channel layer on thermally-oxidized SiO₂/p⁺-Si substrate (**Figure 4.2(b)**). The SiO₂ served as the gate oxide with a thickness of 150 nm, while the p⁺-Si acted as the gate electrode. The ITO was used as the source/drain electrode for the Ga₂O₃ TFTs to form ohmic contacts.^[57-59] The channel width (*W*) and length (*L*) are 300 μm and 100 μm, respectively. **Figure 4.2(c)** displays the transfer characteristics of the Ga₂O₃ nanosheet TFTs fabricated by the conventional LMP and PA-LMP methods. In the case of the Ga₂O₃ fabricated by conventional LMP, the drain current was comparable to the background current level (~pA) of our device measurement system, and no TFT action was observed. This indicates that the LMP-grown nanosheet is electrically insulating.

In contrast, the PA-LMP-grown Ga₂O₃ channel (*T_p* of 150 °C and *P_p* of 1.3 kgf/cm²) exhibits desirable *n*-channel TFT operation, in which the drain currents ($|I_{DS}|$), measured by the source-to-drain voltage (*V_{DS}*), increase upon applying negative gate bias (*V_{GS}*). The output characteristics show ohmic liner-relations at small *V_{DS}* regions and clear pinch-off behavior with the *I_{DS}* saturation, confirming that the device operation follows the standard MOSFET model (**Figure 4.2(e)**). The key TFT device characteristics (i.e., saturation mobility (μ_{sat}), linear mobility (μ_{lin}), *s*-value, and threshold voltage (*V_{th}*)) were determined as the following: the μ_{sat} , μ_{lin} are estimated by the following equation, $|I_{DS}| = \mu_{sat} C_{ox} (\frac{W}{2L}) (V_{GS} - V_{th})^2$), $|I_{DS}| = \mu_{lin} C_{ox} (\frac{W}{L}) [(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2]$, respectively, where *C_{ox}* is the gate insulator capacitance per unit area. The subthreshold slope (*s*-value) is extracted from the slope in the semi-logarithmic plot with $s = (\partial \log I_{DS} / \partial V_{GS})^{-1}$. A reasonable high μ_{sat} of 11.7 cm² V⁻¹s⁻¹ and μ_{lin} of 10.2 cm² V⁻¹s⁻¹ was obtained for the PA-LMP fabricated TFTs. The *V_{th}* is determined from the intercept of a

straight-line fit of the $(I_{DS})^{1/2}$ – V_{GS} plot and estimated 3.8 V, indicating that the device operates in enhancement mode, the “normally-off” operation, which is preferred for low-power analogs/digital circuits. The device also exhibits a small s -value of $163 \text{ mV} \cdot \text{decade}^{-1}$. Trap-state density (D_{it}) is estimated from the s -values using the following relation: $s = \frac{\log e^{10} \cdot k_B T}{e} \left[1 + \frac{e D_{it}}{C_{ox}} \right]$, where e is the elementary electric charge, k_B is Boltzmann constant, T is the temperature, C_{ox} is the gate capacitance per area. The D_{it} was estimated as $2.53 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, which is a significant improvement over previously reported Ga_2O_3 TFTs with the D_{it} of $\sim 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. Importantly, the presented β - Ga_2O_3 nanosheet TFTs exhibit higher mobility and lower D_{it} with a much lower process temperature compared to reported Ga_2O_3 TFTs fabricated by traditional thin-film processing. These findings demonstrate that the PA-LMP method produces a high-quality Ga_2O_3 semiconductor nanosheet with a low defect density at a low temperature. The average values of μ_{sat} of $5.02 \pm 4.05 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, μ_{lin} of $4.21 \pm 5.87 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, s -values of $0.19 \pm 0.12 \text{ V} \cdot \text{dec}^{-1}$, V_{th} of $3.61 \pm 2.99 \text{ V}$, and $\log(I_{on}/I_{off})$ of 8.09 ± 1.54 were obtained. Furthermore, we observed no significant degradation in the device characteristics of the β - Ga_2O_3 TFTs even after 1 month of storage under a non-controlled ambient atmosphere, confirming the environmental stability of the devices in the air. The photoresponse property of β - Ga_2O_3 TFTs was also evaluated. No photoresponse was observed under green, blue, or UV light illuminations, which can be attributed to the wide-bandgap nature of β - Ga_2O_3 .

From the output characteristics, the output resistance of $1/g_d$, where g_d is the output conductance, was evaluated as $>80 \text{ M}\Omega$. We also calculated the transconductance, g_m , and the $1/g_d$ as a function of V_{GS} . The intrinsic gain, defined as $A_i = g_m/g_d$, was as high as 1,000 at V_{DS} of 30 V, significantly higher than that for other source-gate oxide TFTs (Schottky-barrier oxide TFTs)^[60]

^{62]} and one order of magnitude higher than that for traditional ohmic contact IGZO TFTs. The extremely high gains in the presented β -Ga₂O₃ TFTs guarantee the high potential of amplifier applications with better circuit stability and signal-to-noise ratio in digital/analog circuits. Moreover, good current saturation characteristics are immune to wide-range V_{DS} modulation, making it an excellent candidate for use as a current source in pixel circuits.

We also investigated the effect of post-thermal annealing atmospheres on the ultrathin β -Ga₂O₃ TFTs fabricated by PA-LMP. We observed that the TFT characteristics remain almost unchanged during annealing up to a temperature of 200°C. On the other hand, vacuum annealing ($\sim 10^{-5}$ mTorr) improved the TFT mobility but also exhibited a negative V_{th} shift with the increase of off-current. This observation is attributed to the generation of extra carriers due to oxygen vacancy formation by vacuum annealing.

We analyzed the nanosheet structures grown by the conventional LMP and PA-LMP methods using transmission electron microscopy (TEM). **Figure 4.2(f)** shows TEM image of Ga₂O₃ nanosheet grown by the LMP method. The corresponding high-resolution TEM (HRTEM) image reveals no lattice-ordered structure in the LMP-grown nanosheet. (**Figure 4.2(g)**) The corresponding SAED pattern confirmed a halo pattern (**Figure 4.2(h)**). These observations conclude that the nanosheet prepared by the LMP method is amorphous, which agrees with the previous reports.^[53, 63-65] Since amorphous semiconductor includes high-density tail-state defects^[13], the nanosheet is speculated to involve high-density electron traps. Therefore, the LMP-grown amorphous GaO_x exhibited a high-resistive state. We also attempted to improve the electrical properties of the amorphous GaO_x nanosheets by post-thermal annealing at temperatures

ranging from 200 to 400 °C. However, all devices remained insulative state in the presented annealing conditions. To achieve a crystalline β -Ga₂O₃ phase, high-temperature annealing at temperatures above 500 °C may be required, as reported in previous studies.^[44, 66-67] However, high-temperature annealing may cause serious off-chemical stoichiometry, which can lead to the failure of TFT operations in the presented nanosheet channel.

In contrast, a distinct polycrystalline feature, i.e., ordered atomic alignment, for the PA-LMP grown nanosheet (T_p of 150 °C and P_p of 1.3 kgf/cm²) was observed in the TEM analysis (**Figure 4.2(i)**) for the low-magnified HRTEM images of the Ga₂O₃ nanosheet). The HRTEM image also showed the crystal lattice structure with internal spacings of ~0.362 nm ~0.263 nm, which are assigned to the (201) and (−111) planes, respectively, of the monoclinic β -Ga₂O₃ crystal structure. (**Figure 4.2(j)**) The corresponding selected area electron diffraction (SAED) pattern is shown in **Figure 4.2(k)**, and exhibits spots indexed to the (−111), (201), (−311), and (400) crystal plans. The observation concluded that the presented nanosheet was randomly oriented β -Ga₂O₃ crystals. In addition, we performed TEM analysis for the Ga₂O₃ nanosheet prepared using the PA-LMP approach with different process parameters to confirm the direct growth of β -Ga₂O₃ crystals. The energy-dispersive X-ray spectroscopy (EDX) chemical composition mapping analysis also finds that the Ga/O atomic ratio is ~0.64, which is close to the ideal stoichiometry of Ga₂O₃. The grazing incidence X-ray diffraction (GIXRD) analysis also supported that the Ga₂O₃ nanosheets prepared by the PA-LMP method were polycrystalline β -Ga₂O₃. Furthermore, we conducted a cross-sectional TEM analysis for the Ga₂O₃ nanosheet prepared using the liquid metal printing approach on the Si/SiO₂. The Ga₂O₃ nanosheet was prepared at the T_p of 150 °C, and the P_p of 1.3 kgf/cm², exhibiting a high TFT mobility of 8~10 cm²V^{−1}s^{−1}. The distinct polycrystalline nature of

β -Ga₂O₃ was also observed, providing direct evidence that liquid metal printing can grow crystalline β -Ga₂O₃ on the SiO₂/Si substrate. X-ray photoemission spectroscopy (XPS) analysis also confirmed that this material is Ga₂O₃ with the Ga³⁺ oxidation state. Based on the material characterization discussed above, the developed PA-LMP method directly grows crystalline β -Ga₂O₃ with device quality at less than 150°C.

We believe that the nature of oxidation of the liquid metal has a different thermodynamic barrier and path to grow oxide materials, potentially making it easier to grow high-quality oxide materials at lower process temperatures compared to other material growth approaches.^[46-47] Crystalline β -Ga₂O₃ has been successfully synthesized using liquid metal printing, achieved by scraping off the parent metal layer under stress at a process temperature of 200°C.^[68] Given that the thermodynamic barrier and pathway may lower when employing liquid metal oxidation, the crystallization of the Ga₂O₃ phase could potentially be induced by various factors, such as heat, pressure, and stress, to lower the energy barriers for crystallization. Furthermore, we proposed that the facilitation of low-temperature crystallization for the β -Ga₂O₃ phase can be understood by considering both the effects of nanoscale confinement crystal growth and external pressure. It is well-known that nucleation is the initial critical process for crystallization, so reducing the free energy barriers of the nucleation process is essential. In general, free energy barriers for homogeneous (ΔG_{homo}) and heterogeneous nucleations (ΔG_{hetero}) are defined by

$$\Delta G_{homo} = \frac{16\pi\gamma^3}{3(\Delta G)^2}, \quad \Delta G_{hetero} = \Delta G_{homo} \cdot f(\theta) \quad (4.1)$$

Where γ is the interfacial energy. $f(\theta)$ is a function related to the contact angle θ as

$$f(\theta) = \frac{2-3\cos\theta+\cos^3\theta}{4} \quad (4.2)$$

In the developed PA-LMP method, the contact angle is nearly zero since the liquid metal is confined in the nanogap that two substrates generate. Confined systems are expected to influence crystallization processes significantly. As the volume of the confining space decreases, the role of the surface becomes increasingly important in such constrained systems. To achieve low-temperature growth, crystallization in highly confined nanogap regions (nanoscale confinement) provides the potential approach to lower the energy barrier by reducing the reactive surface area of nuclei, thereby decreasing the surface energy penalty. Additionally, nanoscale confinement can alter the nucleation pathway, further reducing the overall energy barrier.^[69-70]

Moreover, it is widely accepted that external pressure impacts the thermodynamic driving forces for crystal nucleation and growth processes. The pressure (P) on the nucleation activation energy, ΔG^* , can be expressed as^[71]

$$\left[\frac{\partial(\Delta G^*)}{\partial P} \right] = - \frac{32\pi\gamma^3}{3} \cdot \frac{\Delta V}{(\Delta G)^3} \quad (4.3)$$

where $\Delta G = G_c - G_a$, where G_c and G_a are the Gibbs free energies of the crystalline and amorphous phases, respectively, γ is interfacial energy and is not sensitive to pressure, $\Delta V = V_c - V_a$ is the difference in molar volumes between the crystalline phase (V_c) and the amorphous phase (V_a). The amorphous GaO_x film density was determined to be approximately $5.2\text{--}5.4 \text{ g}\cdot\text{cm}^{-3}$, which is lower than that of $\beta\text{-Ga}_2\text{O}_3$ (density $\sim 5.95 \text{ g}\cdot\text{cm}^{-3}$).^[43, 72] In this case, i.e. $\frac{\partial(\Delta G^*)}{\partial P} < 0$, since the smaller molar volume of the crystalline phase compared to the amorphous phase ($\Delta V = V_c - V_a < 0$) and $\Delta G = G_c - G_a < 0$. As a result, we hypothesized that pressure also facilitates crystallization by reducing the nucleation activation energy.

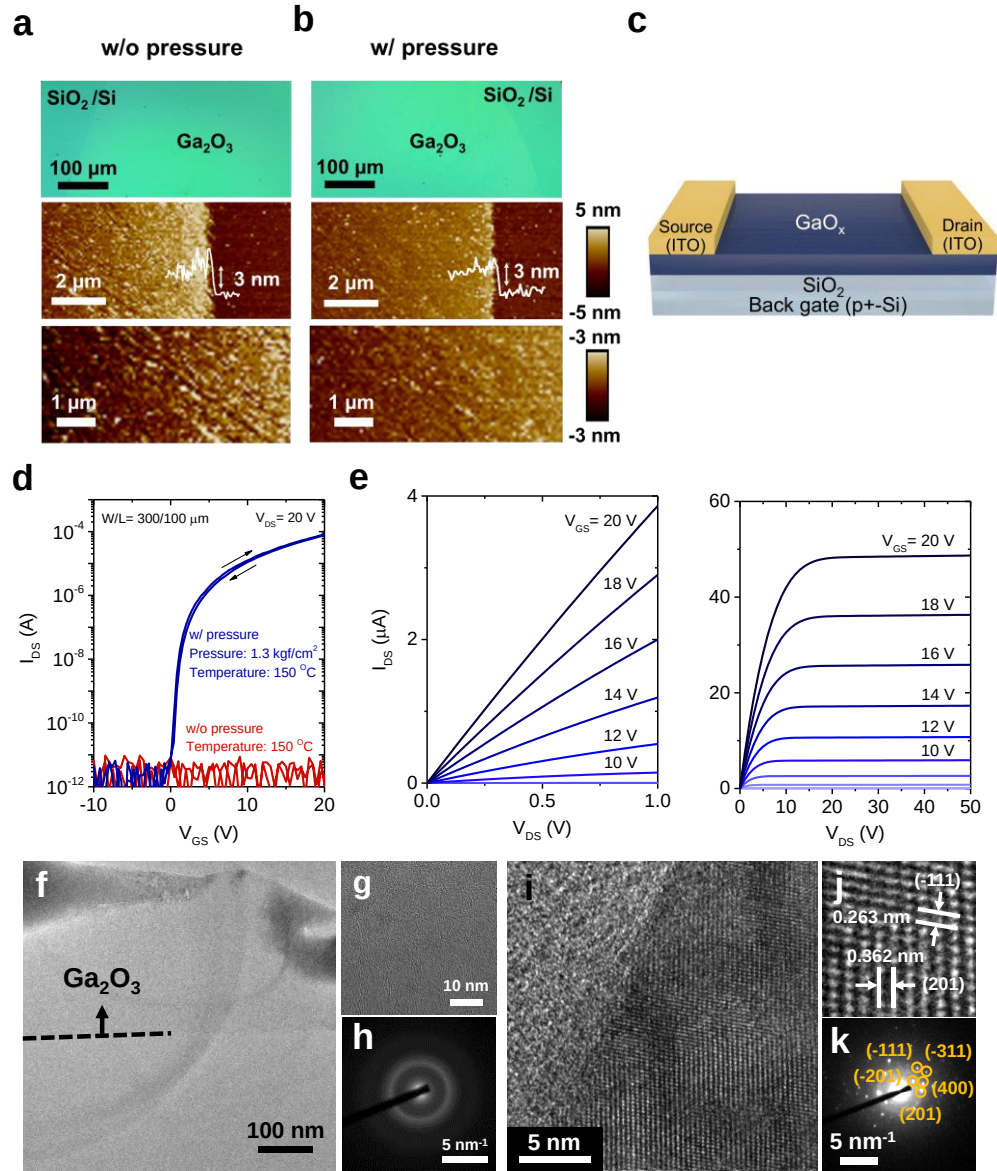


Figure 4.2 Optical microscopy image and AFM image (including cross-sectional step-height profile) for the Ga_2O_3 nanosheet were prepared by (a) conventional LMP (without applied printing process pressure) and (b) PA-LMP methods (applied printing process pressure, T_p of 150 °C and P_p of 1.3 kgf/cm²). (c) Schematics of the device structure of the GaO_x TFTs. (d) Typical transfer characteristics for the Ga_2O_3 TFTs prepared by LMP (T_p of 150 °C and P_p of 0 kgf/cm²) and PA-LMP (T_p of 150 °C and P_p of 1.3 kgf/cm²) methods. (e) Right: typical output characteristics for the Ga_2O_3 TFT. Left: the magnification of the linear regime. (f) Low-magnified HRTEM images of the Ga_2O_3 nanosheet synthesized by the conventional liquid-metal printing route. (without applied printing process pressure) Corresponding (g) high-magnified HRTEM image and (h) selected area electron diffraction pattern. (i) Low-magnified HRTEM images of Ga_2O_3 nanosheet synthesized by the pressure-assisted liquid-metal printing route. (T_p of 150 °C and P_p of 1.3 kgf/cm²) Corresponding (j) high-magnified HRTEM image and (k) selected area electron diffraction pattern.

Figure 4.3(a) illustrates the variation of transfer curves for the ultrathin β -Ga₂O₃ TFTs grown by the PA-LMP under a pressure of 0.3 kgf/cm² at different printing process temperatures. When the device was fabricated at 30 °C, the channel showed highly conducting behavior with an electrical conductivity of 28.3 S·m⁻¹, but the device exhibited negligible field-effect current modulation. Decent TFT actions with an on/off current ratio of 10⁵ were observed when the channels were grown at process temperatures above 80 °C. Furthermore, the TFT mobility was improved by raising the process temperature up to 150 °C. However, a large positive V_{th} shift to 58 V was observed for the device fabricated at a high temperature of 200 °C, indicating that the high-temperature process under a pressure of 0.3 kgf/cm² resulted in poor TFT performances. The fundamental device parameters (μ_{sat} , μ_{lin} , s -value, V_{th} , and on/off current ratio) are also summarized in **Figure 4.3(b)–(e)**. The data are analyzed using 16 representative working devices from different samples.

The temperature at which the gallium oxide skin is formed on the Ga liquid surface metal plays a critical role in the oxidation process. Our observations suggest that the low process temperature of 30 °C may not be sufficient to form Ga₂O₃ phases using the PA-LMP method with printing process pressure of 0.3 kgf/cm², resulting in a high-density Ga metal impurity and highly conductive channels in the as-prepared device. From the TEM characterization, it was also confirmed that Ga-rich GaO_x with embedded Ga metal in nanosheets grown by the printing process at the T_p of 30°C and the P_p of 0.3 kgf/cm². Interestingly, the devices after post-thermal annealing showed p -channel operation with a small on/off current ratio. The origin of the p -type behavior is not yet clear, but we speculate that the p -type behavior may relate to low-valence Ga(I)-based metastable phases formation, such as GaO or Ga₂O, which possibly have the VBM structure

composed of spherical Ga 5s orbital. Further investigation of the origin of *p*-type behavior in gallium oxide is required.

On the other hand, a high-temperature printing process of PA-LMP is sufficient to oxidize gallium metal and form the Ga₂O₃ phase. However, the poor TFT performance observed during the high-temperature process at 200°C under a pressure of 0.3 kgf/cm² (*T_p* of 200 °C and *P_p* of 0.3 kgf/cm²) is primarily caused by (1) the carrier concentration, resulting from oxygen vacancies, can be decreased through compensation by oxygen-containing annealing in the ambient air atmosphere, while (2) excessive oxygen defects, which function as acceptor-like defects, are introduced during oxygen-containing air annealing. Therefore, the optimal process temperature for β-Ga₂O₃ TFTs was found to be between 80–150°C for the PA-LMP. We also fabricated TFTs using the channels prepared by the conventional LMP method at high temperatures of up to 200°C and measured their electrical characteristics. However, no field-effect modulation was observed in any of the devices, indicating that the Ga₂O₃ fabricated LMP is electrically insulating regardless of the process temperature.

Figure 4.3(f) shows the variation in transfer characteristics with different process pressures, with a process temperature of 150°C. The TFT performance was found to improve with increasing the external pressure, with the most significant improvement observed at uniaxial pressure of 1.3 kgf/cm². The most optimized TFT switching properties were achieved under this condition, with high μ_{sat} of 11.7 cm²V⁻¹s⁻¹, large on/off current ratio of ~10⁹, and small subthreshold slope of 137 mV·decade⁻¹, and *V_{th}* of ~4V. The device exhibits clockwise hysteresis originating from electron traps, but the hysteresis window was improved to 0.1V under high-

pressure conditions. The key device parameters (μ_{sat} , μ_{lin} , s -value, V_{th} , and on/off current ratio) are also summarized in **Figure 4.3(g)–(j)**. The data are analyzed using 16 representative working devices from different samples. The average values of μ_{sat} of $8.24 \pm 1.78 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, μ_{lin} of $7.34 \pm 1.96 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, s -values of $125 \pm 23.6 \text{ mV dec}^{-1}$, V_{th} of $4.73 \pm 1.10 \text{ V}$, and $\log(I_{\text{on}}/I_{\text{off}})$ of 9.22 ± 0.43 were obtained under the temperature of 150°C and the pressure of 1.3 kgf/cm^2 . (T_p of 150°C and P_p of 1.3 kgf/cm^2) At high-pressure conditions (2.1 kgf/cm^2), the device operation switched from n -channel to p -channel devices, suggesting the formation of low valance Ga(I) under high-pressure conditions.

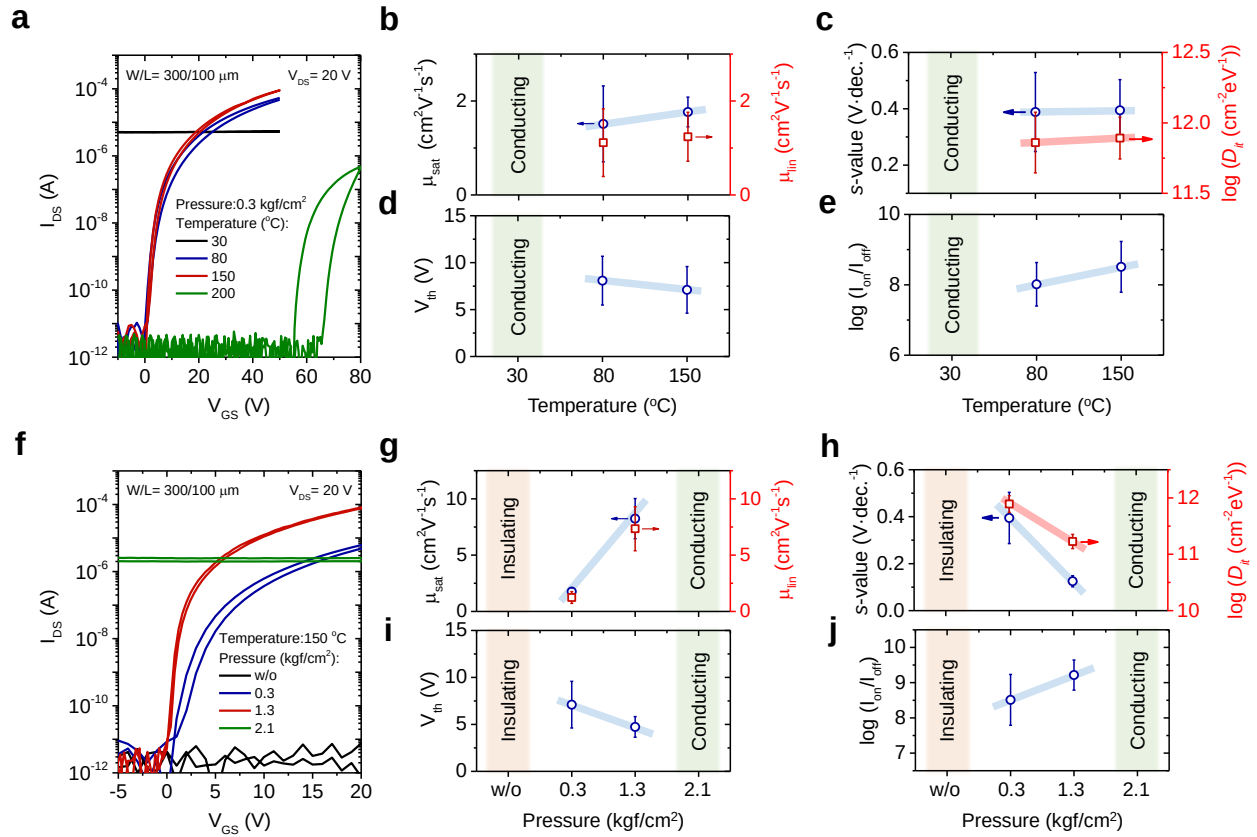


Figure 4.3 (a) Variation of transfer characteristics for the Ga₂O₃ nanosheet TFTs with different printing process temperatures under the uniaxial process pressure of 0.3 kgf/cm². The corresponding TFT parameters (b) μ_{sat} and μ_{lin} , (c) s-value and D_{it} , (d) V_{th} , and (e) on/off current ratio are plotted. (f) Variation of transfer characteristics for the Ga₂O₃ TFTs with different process pressures under the printing process temperature of 150 °C. Corresponding TFT parameters (g) μ_{sat} and μ_{lin} , (h) s-value and D_{it} , (i) V_{th} , and (j) on/off current ratio are plotted.

Figure 4.4 summarizes the TFT operations fabricated by different process pressures and temperature conditions in the PA-LMP route. All The transfer characteristics are presented in **Figure 4.5**. Regardless of the nanosheet growth conditions, conventional LMP-grown nanosheets were electrically insulating amorphous gallium oxide, which was in good agreement with previous reports.^[67, 73] In contrast, the PA-LMP directly synthesized a semiconducting polycrystalline β -Ga₂O₃ channel in the range of the T_p of 80–200 °C with the P_p of 0.3 kgf/cm² and in the range of the T_p 150–200 °C with the P_p of 1.3 kgf/cm². The polycrystalline nature of β -Ga₂O₃ is confirmed by both GIXRD and TEM characterization. The TFT performance degraded with a positive threshold voltage shift during the high-temperature process at 200 °C under pressures of 0.3 and 1.3 kgf/cm², respectively. The reason is suspected to be a decrease in carrier concentration originating from oxygen vacancies, along with the introduction of excessive oxygen defects functioning as acceptor-like defects during annealing in oxygen-containing air. Interestingly, amorphous films grown at high pressure of 2.1 kgf/cm² with the process temperature of 150 and 200 °C exhibited *p*-type behavior. We suspect these materials result from the slight oxidation of Ga metal, leading to off-stoichiometric GaO_x materials. These materials might include low-valence Ga(I)-based metastable phases, possibly with a VBM structure composed of spherical Ga 5s orbitals contributing to the *p*-type behavior. Further study is required to investigate these materials. We notice that there are reports of Ga ultrathin film growth using a similar liquid metal printing method.^[74-75] These results corroborate our findings that liquid metal printing can form off-stoichiometric GaO_x through slight oxidation of Ga metal under an air atmosphere.

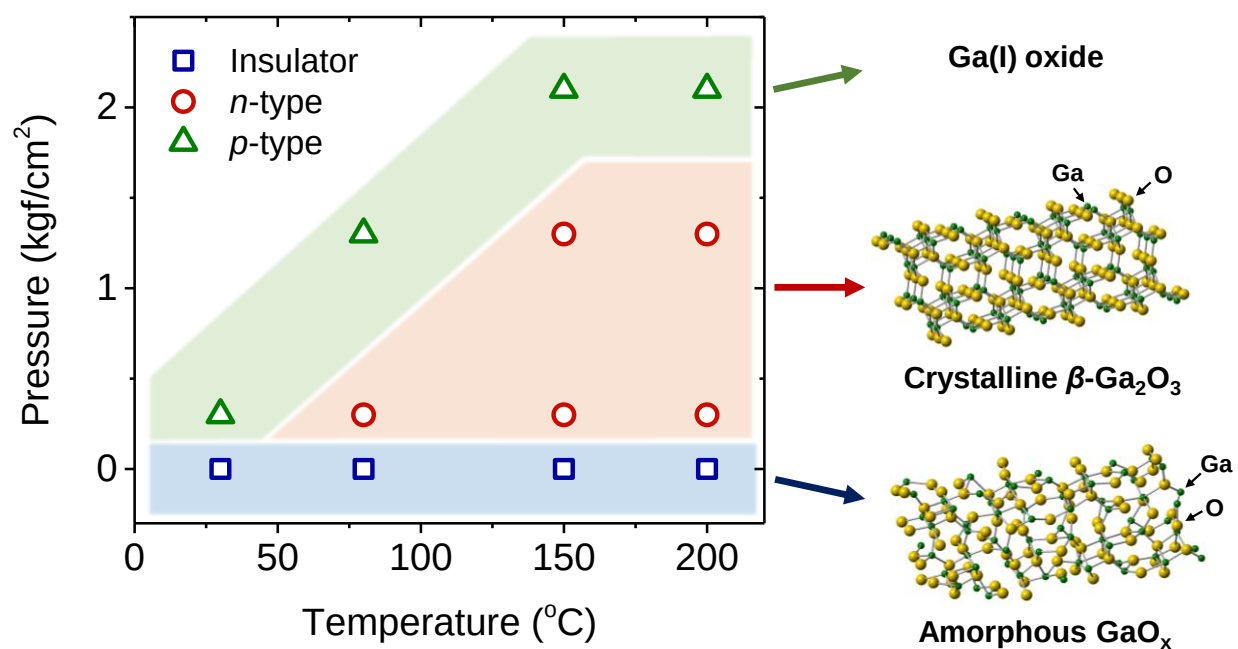


Figure 4.4 Summary of the electrical properties of the gallium oxide nanosheet channel grown using the pressure-assisted liquid-metal route under various printing process conditions of uniaxial pressures and temperatures.

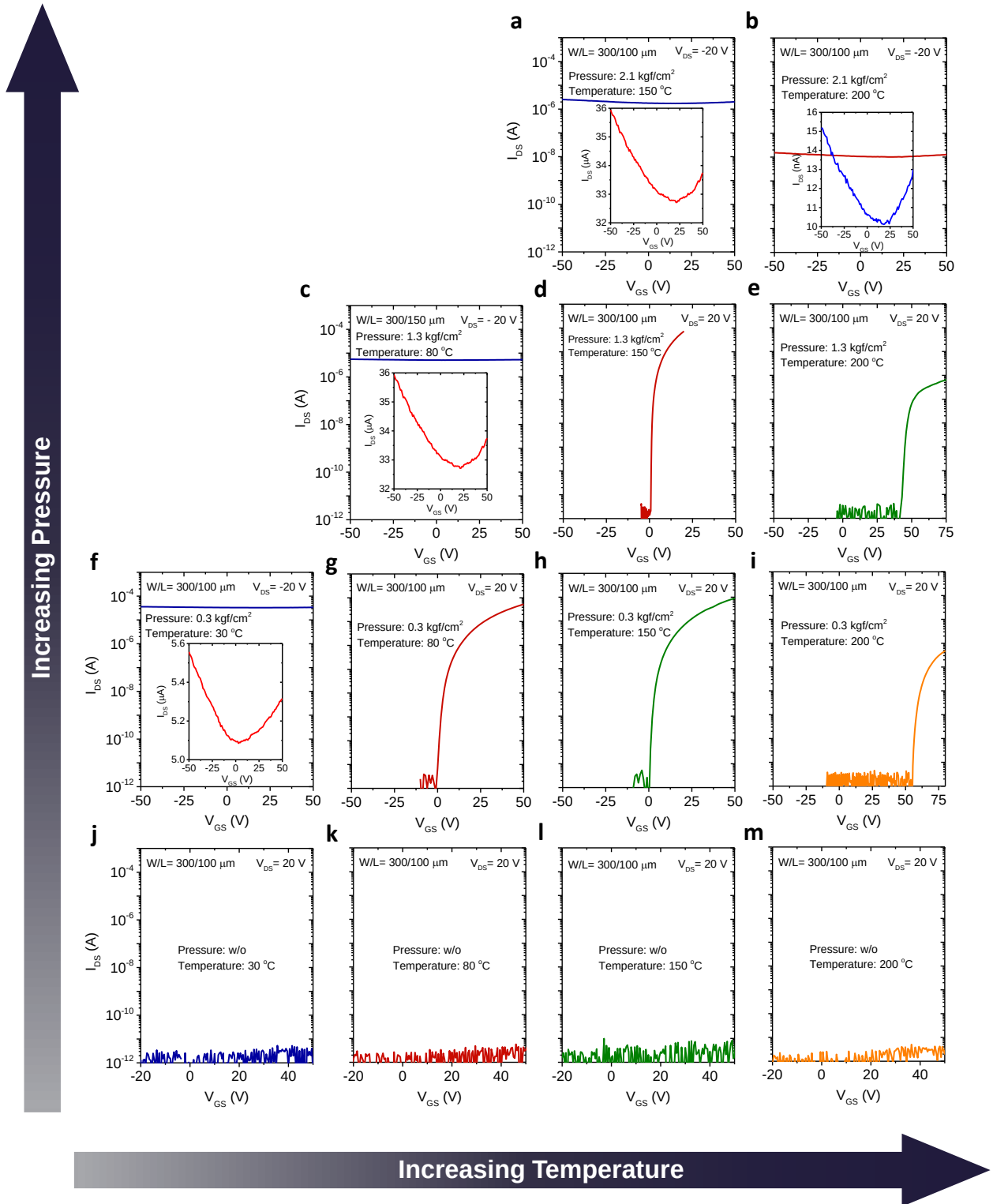


Figure 4.5 Variation of transfer characteristics for the Ga_2O_3 TFTs fabricated by the PA-LMP with different printing temperatures and pressure conditions.

To gain further insight into the variation of TFT characteristics, we performed the Technology Computer-Aided Design (TCAD) device simulation to extract the subgap defect density of state. **Figure 4.6(a)** shows the measured and simulated transfer curves of Ga₂O₃ TFTs with different process conditions. Only parameter optimization for the subgap acceptor-like defect density of state (DOS) can reproduce the measured transfer curves, indicating that the variation in TFT characteristics under different process parameters mainly originates from the change in subgap defect DOS in the Ga₂O₃ channels. The extracted subgap defect DOS near the conduction band (CB) of Ga₂O₃ TFTs under different process conditions are shown in **Figure 4.6(b)**. (**Table 4.1** provides the parameters of the TFT simulations). We found that all the measured *I-V* curves were reproduced by only optimizing the acceptor-like defect (i.e., electron trap defect) with Gaussian distribution type,

$$g_G(E) = N_{GD} \cdot \exp \left\{ - \left[\frac{(E_c - E_{GA})}{W_{GD}} \right]^2 \right\} \quad (4.4)$$

where N_{GD} is the state densities at the central energy E_{GA} of the Gaussian distribution, E_c is the conduction band edge energy for the reference zero point, E_{GA} is the central energy of $g_G(E)$, W_{GD} is the characteristic decay energy. Due to the polycrystalline nature of the Ga₂O₃, we opted not to employ the acceptor-like exponential DOS to fit the measured *I-V* curves that are used for the tail states near the conduction for the amorphous silicon (a-Si:H) and amorphous IGZO.^[76] All the devices show a low carrier concentration of $5.5 \times 10^{14} \text{ cm}^{-3}$ due to the ultra-wide gap nature of Ga₂O₃.

We observed shallow acceptor-like defect states located at 0.15 eV below the conduction band ($E_c - 0.15 \text{ eV}$) in the Ga₂O₃ TFTs. These acceptor-like defect states primarily function as electron traps in the *n*-channel oxide TFT devices. The physical origin of these shallow acceptor-like defect states remains elusive; however, we suspect these defects result from Ga vacancies or weakly

bonded (excess) oxygen defects.^[43, 77-78] The Ga₂O₃ TFT fabricated with the low-pressure condition (T_p of 80 °C, P_p of 0.3 kgf/cm²) exhibited a relatively high density of shallow acceptor-like defect states of $2 \times 10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$ and remained unchanged even in the device fabricated at 150 °C. (150 °C, 0.3 kgf/cm²) On the other hand, we found that the high-pressure condition (150 °C, 1.3 kgf/cm²) effectively reduced the shallow subgap acceptor-like defect DOS to $5 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$, resulting in better TFT performances with higher mobility. This acceptor-like defect reduction makes moving the Fermi level toward the mobility edge easier, achieving band-like conduction and explaining the higher mobilities observed in these TFTs.

We also found that the shallow subgap defect DOS significantly impacts the on-current and s -value but does not affect the turn-on voltage, resulting from the enhancement mode operation. The D_{it} , estimated from the s -values of the experimental transfer characteristics, are $5.37 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ (80 °C, 0.3 kgf/cm²), $4.78 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ (150 °C, 0.3 kgf/cm²) and $1.93 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ (150 °C, 1.3 kgf/cm²) for these three process conditions, respectively. The shallow subgap defect DOS for all these three conditions we attained from the TCAD simulation correspond to area densities of $6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ (80 °C, 0.3 kgf/cm²), $4.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ (150 °C, 0.3 kgf/cm²) and $1.8 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ (150 °C, 1.3 kgf/cm²), respectively, considering the Ga₂O₃ thickness of 3 nm. These values are consistent with those calculated from experimental s -values.

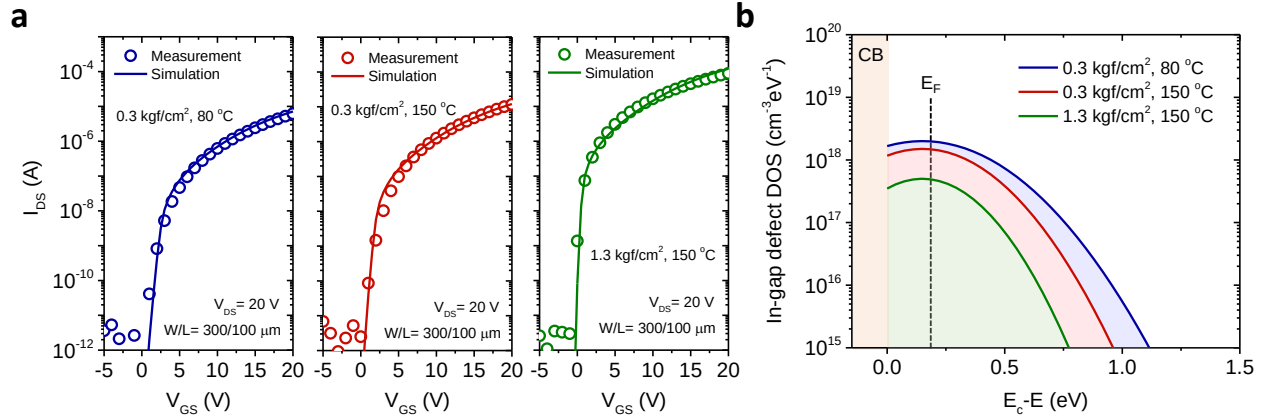


Figure 4.6 (a) Comparison of measured (lines) and simulated (symbols) transfer curves with $V_{DS} = 20 \text{ V}$ for the Ga₂O₃ TFTs with different printing process conditions. (left: T_p of 80°C , P_p of 0.3 kgf/cm^2 , middle: T_p of 150°C , P_p of 0.3 kgf/cm^2 , right: T_p of 150°C , P_p of 1.3 kgf/cm^2) (b) Corresponding in-gap density of states for the Ga₂O₃ nanosheet channels for different printing process conditions. Fermi level (E_F) lies at $E_c - E_F = 0.23 \text{ eV}$.

Table 4.1 TFT simulation parameters for the Ga₂O₃ TFT analysis.

Parameter	80 °C, 0.3 kgf/cm ²	150 °C, 0.3 kgf/cm ²	150 °C, 1.3 kgf/cm ²
Band gap (eV)	4.7	4.7	4.7
Effective DOS for CB (cm ⁻³)	3.72×10 ¹⁸	3.72×10 ¹⁸	3.72×10 ¹⁸
Effective DOS for VB (cm ⁻³)	1×10 ¹⁹	1×10 ¹⁹	1×10 ¹⁹
Dielectric constant of Ga ₂ O ₃	10	10	10
Electron mobility (cm ² V ⁻¹ s ⁻¹)	0.9	1.4	12
N _e electron density (cm ⁻³)	5.5×10 ¹⁴	5.5×10 ¹⁴	5×10 ¹⁴
N _{GA} (cm ⁻³)	2×10 ¹⁸	1.5×10 ¹⁸	5×10 ¹⁷
E _{GA} (eV)	0.15	0.15	0.15
W _{GA} (eV)	0.35	0.3	0.25

Since ultrathin oxide TFT channels improve gate controllability and low-off current characteristics, developing a low-power inverter is highly expected for next-generation energy-efficient oxide electronics. We developed oxide-TFT-based inverter circuits, including NMOS and CMOS circuits, using ultrathin Ga_2O_3 TFTs. The Ga_2O_3 nanosheets used for the NMOS and CMOS circuits demonstration were grown using a T_p of 150°C and P_p of 0.3 kgf/cm^2 . **Figure 4.7(a)** shows the typical transfer characteristics for a zero- V_{GS} NMOS, consisting of the enhancement and depletion-mode TFTs as the driver and load, respectively. The depletion-mode TFTs were fabricated by performing post-thermal annealing under vacuum conditions at 100°C . The depletion-mode TFTs showed the μ_{sat} of $0.8 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, s -value of $1.6 \text{ V}\cdot\text{decade}^{-1}$, V_{th} of -4.5 V , and on/off current ratio of $\sim 10^7$. The corresponding TFT performances for enhancement-mode TFTs show the μ_{sat} of $2.6 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, s -value of $0.28 \text{ mV}\cdot\text{decade}^{-1}$, V_{th} of 6 V , and on/off current ratio of $\sim 10^8$, respectively. **Figure 4.7(b)** shows a typical voltage transfer characteristic (VTC) of the NMOS inverter, which is the V_{out} as a function of the V_{in} with V_{DD} . The inset illustrates the equivalent circuit diagram of the zero- V_{GS} -load NMOS inverter. The output voltage switches from high to low, confirming a clear inverting action with the full-voltage swing. The average voltage gain of the NMOS inverters was 16.9, 45.1, 64.0, 80.5, and 106.4 at V_{DD} from 5 to 25 V, respectively, comparable to the previously reported oxide-NMOS inverters.^[79-81] **Figure 4.7(c)** also shows the corresponding supply currents (I_{DD}) as functions of V_{in} . The static currents ($V_{\text{in}} = 0 \text{ V}$ or $V_{\text{in}} = V_{\text{DD}}$) are lower than 2.4 nA, and the static power dissipation, which is defined by $P_{\text{static}} = V_{\text{DD}} (I_{\text{static_low}} + I_{\text{static_high}})/2$, is 28 nW per logic gate at V_{DD} of 25V. The P_{out} is estimated as $<43 \text{ nW}$ per logic gate, confirming that a nanowatt power source can operate the presented inverter. Since power consumption can be further reduced through scaling, the presented results demonstrate high potential for ultra-low power consumption TFT technology. This is attributed to

the low off-current characteristics originating from the ultra-wide bandgap nature. The noise margin (NM) is estimated using the maximum equal criterion method and obtained 57.2 % of the ideal value ($V_{DD}/2$). This indicates that the device has sufficient NM for most static logic applications (**Figure 4.7(d)**).

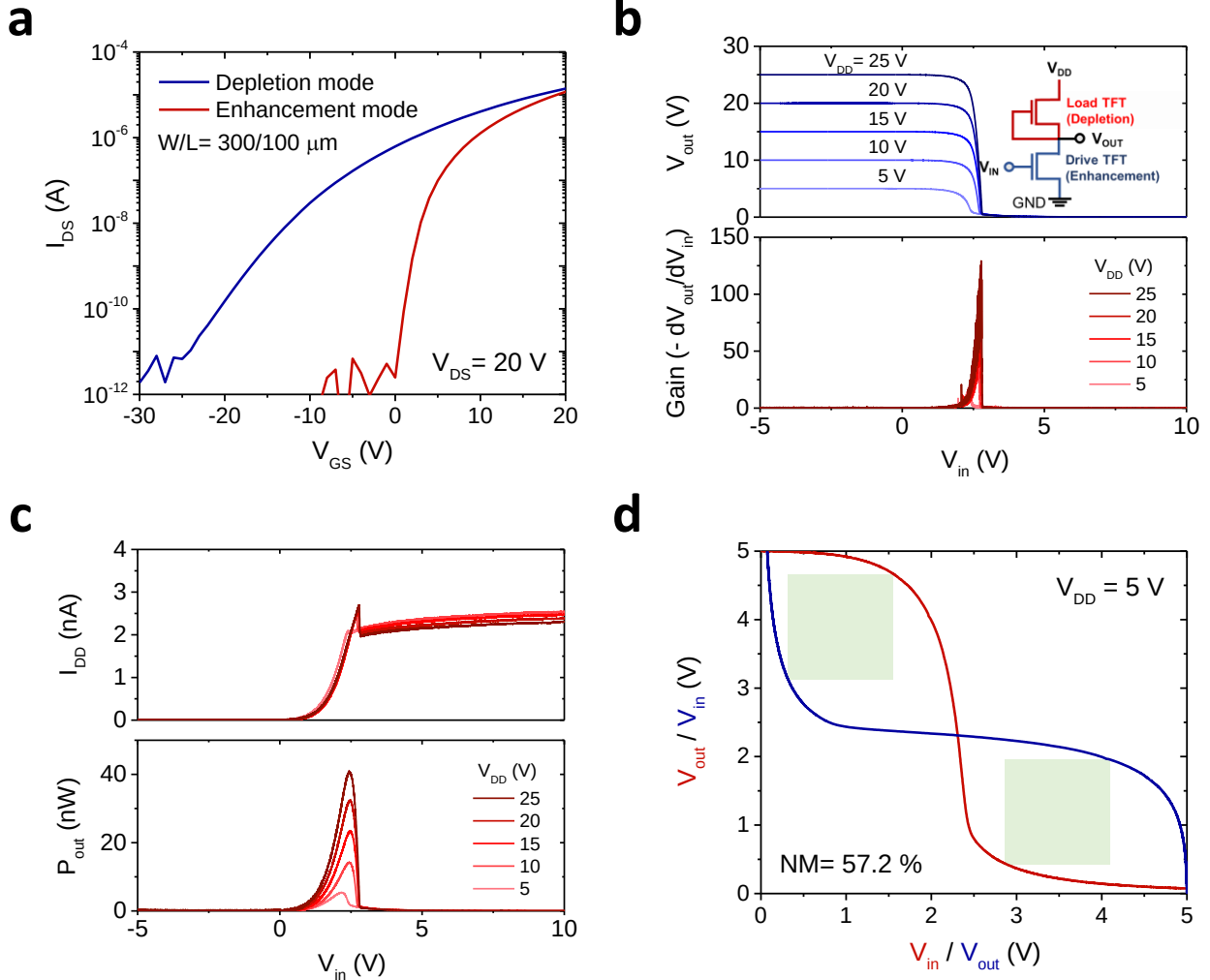


Figure 4.7 (a) Typical transfer characteristics for the depletion-mode and enhancement-mode Ga₂O₃ TFTs. (The Ga₂O₃ nanosheets used for the NMOS circuits demonstration were grown using a T_p of 150 °C, P_p of 0.3 kgf/cm². The depletion-mode TFTs were fabricated by performing post-thermal annealing under vacuum conditions at 100°C.) (b) Top: voltage transfer characteristic (VTC) of the Ga₂O₃ TFT-based NMOS inverter. Bottom: corresponding voltage gains of the Ga₂O₃ TFT-based NMOS inverter. Inset: schematic circuit diagram of the zero- V_{GS} -load NMOS inverter composed of enhancement/depletion-mode Ga₂O₃ TFTs. (c) Top: corresponding supply currents (I_{DD}). Bottom: output-power consumption (P_{out}) for the Ga₂O₃ TFT-based NMOS inverter. (d) Butterfly curves for noise margin (NM) of the Ga₂O₃ TFT-based NMOS inverter.

All-oxide-CMOS inverter circuits were also developed using *n*-type ultrathin Ga₂O₃ TFT and *p*-type ultrathin SnO TFT, which is also fabricated by a liquid-metal printing technique. The detailed fabrication procedure of *p*-channel SnO TFTs can be found in our previous work.^[56] The typical transfer characteristics of both the ultrathin *p*-channel SnO TFT and *n*-channel Ga₂O₃ TFT used in the oxide-TFT-based CMOS inverter are shown in **Figure 4.8(a)**. The *n*-channel Ga₂O₃ TFT exhibits the μ_{sat} of 1.5 cm²V⁻¹s⁻¹, *s*-value of 0.27 V dec.⁻¹, *V*_{th} of 6 V, and on/off current ratio of ~10⁸. The corresponding TFT performances for *p*-channel SnO-TFT are the μ_{sat} of 0.2 cm²V⁻¹s⁻¹, *s*-value of 1.9 V·decade⁻¹, *V*_{th} of -20 V, and the on/off current ratio of ~10⁵, respectively. The inset of **Figure 4.8(b)** is the schematic circuit diagram of the CMOS inverters. **Figure 4.8(b)** presents the typical voltage transfer characteristic of the CMOS inverter, where the output voltage switches from high to low, confirming a clear inverting action with the full-voltage swing. The average voltage gain of the inverter was estimated as 38, 50, 79, 110, and 149 at *V*_{DD} from 10 to 50 V, respectively, which is nearly comparable to the previously reported values for oxide-based CMOS inverters.^[82-85] The *I*_{DD} of the ultrathin *p*-SnO/*n*-Ga₂O₃ TFT-based CMOS inverter as a function of *V*_{in} is shown in **Figure 4.8(c)**. The static currents are lower than 1 nA, leading to the low static power dissipation of 20 nW per logic gate at *V*_{DD} of 50V. (**Figure 4.8(c)**). The *P*_{out} is smaller than 84 nW per logic gate, which indicates that this CMOS inverter can be operated by the nanowatt power source. These results reveal the potential for achieving low-power operation for oxide CMOS circuits using scaled devices. The low-power oxide-CMOS inverter using *p*-SnO/*n*-Ga₂O₃ TFTs is attributed to the ultralow off-current nature for both the *n*- and *p*-channel transistors. This demonstrates the high potential of atomically thin oxide-TFT-based inverter circuits for next-generation energy-efficient electronics.

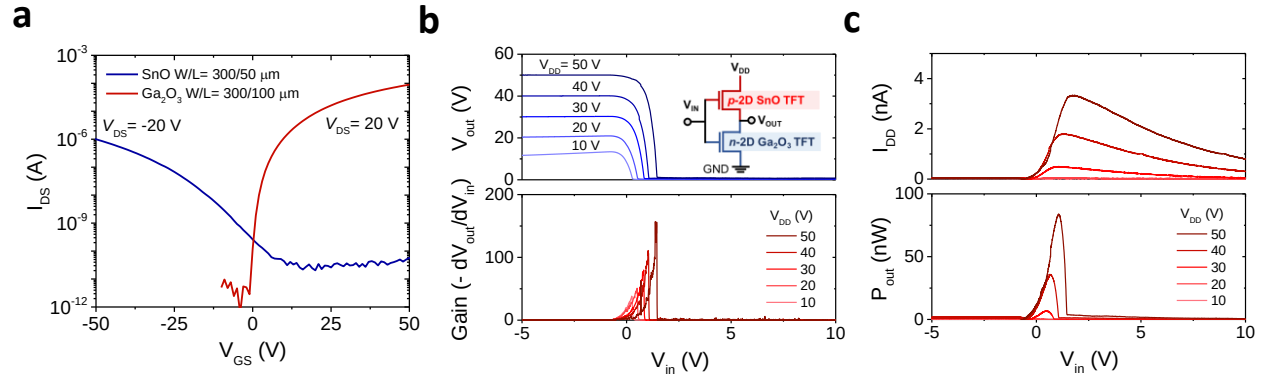


Figure 4.8 (a) Typical transfer characteristics of the ultrathin *p*-channel SnO TFT with $V_{DS} = -20$ V and *n*-channel Ga_2O_3 TFTs at $V_{DS} = 20$ V. (The Ga_2O_3 nanosheets used for the CMOS circuits demonstration were grown using a T_p of 150 $^{\circ}\text{C}$, P_p of 0.3 kgf/cm ^{2} .) (b) Top: voltage transfer characteristic and corresponding voltage gains for the *p*-SnO/*n*- Ga_2O_3 TFT-based CMOS inverter. Inset: schematic of the corresponding oxide-TFT-based CMOS inverter circuit. (c) Top: corresponding supply currents (I_{DD}). Bottom: the output-power consumption (P_{out}) for *p*-SnO/*n*- Ga_2O_3 TFT-based CMOS inverter.

4.4 Conclusions

The uniaxial pressure-assisted liquid-metal printing approach using nanoscale confinement growth was developed for low-temperature processed *n*-channel β -Ga₂O₃ TFTs for energy-efficient and cost-effective next-generation ubiquitous sustainable electronics. The presented growth method successfully fabricated device-quality crystalline β -Ga₂O₃ nanosheet at low temperatures (<150°C) under vacuum-free, solvent-free, and non-controlled ambient air conditions. The *n*-channel TFTs based on β -Ga₂O₃ nanosheet exhibited high performance with a reasonably high mobility of 11.7 cm²V⁻¹s⁻¹, an on/off-current ratio of ~10⁹, and a small subthreshold slope of 163 mV·decade⁻¹, which is the best device performance for low-temperature-processed Ga₂O₃ TFTs to date. We also first observed *p*-channel operation in the off-stoichiometric GaO_x channels fabricated at high-pressure conditions. Toward the oxide-based circuit application, we demonstrated low-power and all-oxide-based zero-*V*_{GS}-load NMOS and CMOS inverters using metal-liquid printing derived Ga₂O₃ nanosheet channel oxide-TFTs. These inverters showed full voltage swing characteristics and high energy-efficient operation with low static power dissipations. Our work demonstrates the high potential of β -Ga₂O₃ for high-performance *n*-channel oxide TFTs and offers a promising approach for the development of sustainable oxide-TFT technology for next-generation electronics.

Chapter 4, in part, has been submitted for publication of the material as it may appear in Nature Communications. Chi-Hsin Huang, Ruei-Hong Cyu, Yu-Lun Chueh and Kenji Nomura. The dissertation author was the primary investigator and author of this paper.

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Chapter 5 Reconfigurable Artificial Synapses with Excitatory and Inhibitory Response Enabled by Ambipolar Oxide Thin-Film Transistor

5.1 Introduction

Artificial intelligence (AI) technology, which is conventionally based on the foundation of von Neumann configurations, currently faces fundamental limitations in processing big data for conventional AI systems. Moreover, developing mobile and truly brain-like systems that are energy-efficient and use low-cost processes is highly demanded beyond conventional AI for ubiquitous AI systems. It is greatly expected that neuromorphic and biomimetic AI can significantly improve performances such as power consumption and data analysis speed compared to those of conventional AI systems, which are digital processing. Since processing and sensing information in neuron networks is critical to the human brain, mimicking such neuromorphic behaviors is the key to neuromorphic device development.

The excitatory and inhibitory postsynaptic potentials are well-known fundamental synaptic responses, yielding the diverse functionalities of the biological nervous systems.^[1-3] Specifically, the excitatory postsynaptic potential activates the postsynaptic neuron to fire an action potential. On the other hand, the inhibitory postsynaptic potential counteracts the excitatory action and makes the postsynaptic neuron less likely to fire. The different synaptic responses, that is, excitatory or inhibitory, are determined by the different neurotransmitters released from the presynaptic neurons to activate the different types of ion channels in a postsynaptic neuron.

Many intelligent behaviors, including learning and perception, are primarily affected by external environmental stimuli in the human nervous system.^[1, 4-5] After these stimuli are detected by receptors and transmitted as electrochemical signals to synapses, the synapse releases diverse excitatory and inhibitory neurotransmitters, leading to the excitatory and inhibitory postsynaptic potentials to process the signals.^[6-7] These synaptic response processes are reconfigured between excitatory and inhibitory postsynaptic responses by modulating signals emitted from the nervous system. Synapses exhibit significantly different responses to even the same external stimuli in the human brain. Therefore, developing artificial synapses with reconfigurable excitatory and inhibitory responses is essential for building advanced AI systems with human-like perceptual capability.

The hardware implementation of an artificial synapse is critical, and it is widely known that conventional neuromorphic systems are based on complementary metal-oxide-semiconductor (CMOS) technology.^[3, 8-10] However, this approach requires tons of transistors to imitate even one synapse and exhibits system complexity and a lack of scalability.^[3, 8-9] Therefore, several types of synaptic devices using emerging memory^[11-18] and transistor-type devices^[19-25] have been developed to realize synaptic functions in a single device. Since these devices operate in unipolar, the capability of synaptic responses is limited, and reconfigurable excitatory and inhibitory responses in a single device is very challenging. Developing a synaptic device exhibiting two different reconfigured synaptic modes is strongly required.

An ambipolar transistor, in which both electron and hole transports contribute to the channel conduction and are controlled by a gate-terminal, is promising to develop a synaptic device

exhibiting both excitatory and inhibitory responses in a single device. Recently, several ambipolar materials such as graphene^[26-27] and black phosphorus^[28] have been proposed for the ambipolar transistor-based synaptic devices. However, these materials still suffer stability and reproductivity, including scalability for practical neuromorphic systems. Ambipolar oxide semiconductor tin monoxide (SnO) has several advantages, such as high material stability and easy channel fabrication processability than conventional ambipolar materials.^[29-33] Moreover, the oxide semiconductor thin-film transistor (TFT) exhibits the electrical hysteresis behavior originating from carrier trapping, which leads to the memory effect and can be utilized for developing charge-trapping transistor-type memory devices.^[18, 34] However, the ambipolarity, an unbalanced hole/electron transport, is not satisfied yet.^[35-36] Since the symmetric current response is essential in excitatory and inhibitory responses, improving the ambipolarity is vital to develop high-performance synaptic devices.

In this study, we developed an artificial synaptic device exhibiting dynamic reconfigurable excitatory and inhibitory synaptic response functions using ambipolar oxide TFTs. Since the balance of ambipolarity is significant, we developed 5 atomic percentage (at. %)-boron (B) incorporated SnO (SnO:B) as a channel material of the ambipolar oxide-TFT to improve the ambipolarity by reducing the subgap defect in the channel. The presented device exhibited well-balanced *p* and *n*-channel mode operations, demonstrating dynamic modulation by the gate terminal to effectively respond to both positive and negative stimulus signals in the excitatory and inhibitory response modes.

5.2 Experimental Section

SnO:B channel deposition

A SnO:B channel with a film thickness of ~ 7 nm was deposited by pulsed laser deposition (PLD) at c using KrF excimer laser (a wavelength of 248 nm, a pulse duration of ~ 20 ns, and a pulse frequency of 10 Hz). The base vacuum of the PLD chamber was $<1.8 \times 10^{-8}$ Torr. The oxygen partial pressure during the deposition was fixed at 2×10^{-4} Pa. A polycrystalline 5 at.-%-boron-incorporated SnO sintered body target was prepared by a conventional solid-state reaction. A laser power density of $\sim 6 \text{ Jcm}^{-2}$ at the target surface yielded a film growth rate of ~ 6 nm/min.

Device fabrication

An inverted-staggered (bottom-gate and top source/drain contact) structure was fabricated. The channel region was patterned by photolithography and defined by chemical wet etching by using 1 mol L^{-1} (M) HNO_3 solution. The source and drain electrodes [indium tin oxide (ITO)] were also patterned by photolithography. The ITO electrode with ~ 40 nm was deposited by PLD at RT. The channel length (L) and the width (W) were 100 and 300 μm , respectively. The hydrogen thermal annealing was performed for 30 minutes with $\text{N}_2 + \text{H}_2$ (5% hydrogen) at 250 $^\circ\text{C}$. The back-channel surface defect was passivated by ~ 5 nm of aluminum oxide (Al_2O_3), which was deposited by atomic layer deposition (ALD) with Trimethylaluminum and a H_2O precursor at the deposition temperature of 250 $^\circ\text{C}$.

Thin-film material characterization

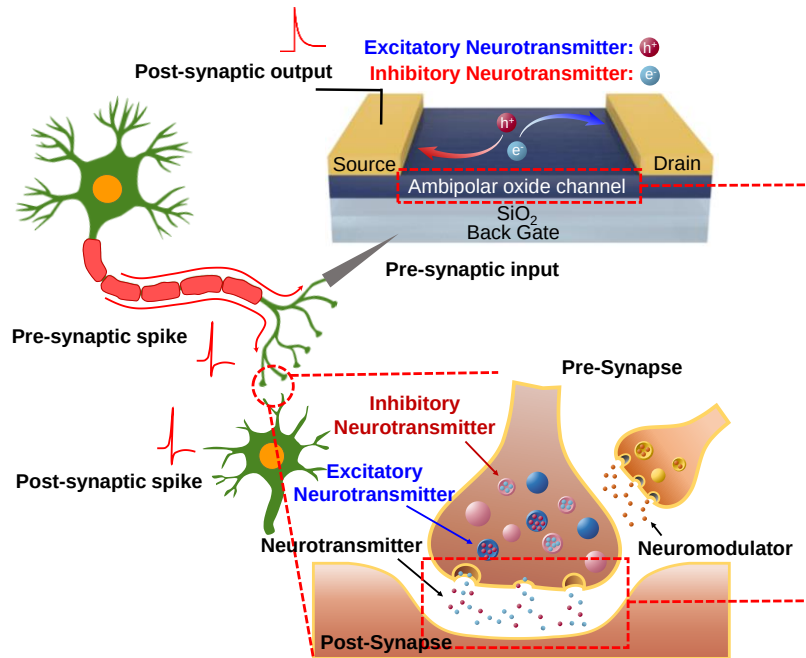
The SnO:B film was prepared on a glass substrate for material characterization. Film structures were examined by grazing incidence X-ray diffraction with Cu K α radiation at an

acceleration voltage of 50 kV, an emission current of 40 mA, and an incident angle of 0.5° . The B concentration of the films was measured by X-ray photoemission spectroscopy (XPS) analysis. The hole density and hole mobility of the films were determined by the AC Hall effect measurement with van der Pauw method at room temperature. The electrical characteristics of the device were measured using a semiconductor parameter analyzer at room temperature in an ambient atmosphere in the dark.

5.3 Results and Discussion

Figure 5.1 explains how to imitate dynamic reconfigurable artificial synaptic devices with excitatory and inhibitory responses by the ambipolar TFT. The biological synapse activity is performed at connecting two neighboring neuron cells, including presynaptic and postsynaptic neurons, and the synaptic cleft.^[1] **Figure 5.1(a)** illustrates the schematic of a biological synapse that releases both excitatory and inhibitory neurotransmitters to induce both excitatory and inhibitory postsynaptic potentials. The release of neuromodulators reconfigures the excitatory and inhibitory synaptic responses. The action potentials from the presynaptic neuron by the external stimulus are transmitted through the synapse to the postsynaptic neuron and generate the postsynaptic current (PSC). In addition, the excitatory and inhibitory synaptic responses can be reconfigured by the release of neuromodulators. **Figure 5.1(b)** also shows a working principle of reconfigurable artificial synapses with an excitatory and inhibitory response by ambipolar-TFT. In charge-trapping transistor-type artificial synapses, hysteresis behavior is the mechanism for emulating the basic biological synaptic responses.^[19, 37-38] When a pulsed signal is inputted by gate-bias (V_{GS}), the drain current (I_{DS}) corresponding to the PSC response to these applied pulses is generated. Ambipolar-TFTs work in both the input signals with different polarities and mimics excitatory and inhibitory responses by using n -channel and p -channel mode operations.

(a)



(b)

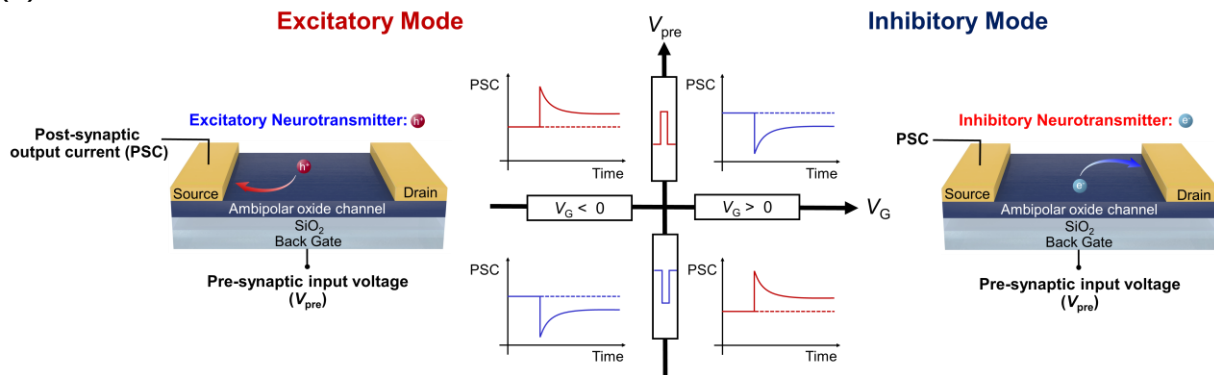


Figure 5.1 (a) Schematic of a biological synapse reconfigured by neuromodulators to release the excitatory and inhibitory neurotransmitters. (b) Working principle of reconfigurable artificial synapses with the excitatory and inhibitory response using an ambipolar oxide transistor.

A dual-mode synaptic device with a bottom-gate and top-contact TFT structure was fabricated using an ambipolar SnO:B channel with a thickness of ~7nm on 150 nm-thick thermal-oxidized SiO₂/n⁺-Si substrate, which works as a common gate and a common dielectric layer. To improve ambipolar characteristics, the back-channel surface defect termination was performed by using atomic layer deposition (ALD)-Al₂O₃.^[30, 35, 39] **(Figure 5.2(a)** for the device structure) The grazing-incident X-ray diffraction (GIXRD) analysis revealed that the 5 at. %-boron incorporation did not affect the α -PbO-type SnO crystal structure, and the films are polycrystalline without a preferred crystal orientation. The X-ray photoemission spectroscopy (XPS) analysis determined that the B concentration was ~ 5.8 at% in the SnO:B films. **Figure 5.2(b)** shows the typical transfer characteristic, that is, I_{DS} versus V_{GS} , of the ambipolar SnO:B TFTs. For comparison, the transfer characteristic for the ambipolar non-doped SnO-TFT with ALD-Al₂O₃ passivation is also shown. The I_{DS} increases by applying both positive/negative polarities of the gate bias, indicating TFTs operate in the ambipolar mode composed of electron (*n*-channel) and hole (*p*-channel) conductions. The TFT device characteristics such as saturation mobility (μ_{sat}), subthreshold slope (*s*-value), and threshold voltage (V_{th})) were determined as follow: the μ_{sat} is estimated by the following equation,

$$|I_{DS}| = \mu_{sat} C_{ox} (W/2L(V_{GS} - V_{th})^2) \quad (5.1)$$

, where C_{ox} is the gate insulator capacitance per unit area. The *s*-value is extracted from the slope in the semi-logarithmic plot with $s = (\partial \log I_{DS} / \partial V_{GS})^{-1}$, where I_{DS} and V_{GS} are in the subthreshold region. The V_{th} is determined from the intercept of a straight-line fit of the $(I_{DS})^{1/2}$ - V_{GS} plot.

The pure SnO-TFT exhibited reasonably high μ_{sat} of ~1.4 cm²V⁻¹s⁻¹, *s*-value of ~2.3 Vdecade⁻¹, V_{th} of -16 V, and on/off current ratio of ~3 × 10⁴ for the *p*-channel mode, and ~0.01

$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, $\sim 4.29 \text{ Vdecade}^{-1}$, 14 V and $\sim 9 \times 10^2$ for the n -channel mode, respectively. The switching voltage (V_{on}), that is, the gate bias that transits between n and p -channel operations in the ambipolar mode, was $\sim +2 \text{ V}$. These observations indicate that n -channel mode is inferior to the p -channel mode for the non-doped SnO TFT. On the other hand, the SnO:B TFT shows a better symmetric ambipolar property with an improved n -channel property and nearly-zero V_{on} . For the p -channel mode, a μ_{sat} of $\sim 1.3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, s -value of $\sim 1.1 \text{ Vdecade}^{-1}$, a V_{th} of -2 V , and an on/off current ratio of $\sim 8 \times 10^3$, while a μ_{sat} of $\sim 0.14 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, an s -value of $\sim 2.2 \text{ Vdecade}^{-1}$, V_{th} of 5 V , and an on/off current ratio of $\sim 1 \times 10^3$ for the n -channel mode. Since the existence of defect states weakens the effective gate control and impedes the drain current increase in the subthreshold region, the s -value exhibits a higher value than the Boltzmann thermionic limit (60 mVdecade^{-1} for room temperature), which is expressed by $s_{\text{limit}} = \ln(10) \cdot k_B T / e$, where k_B is Boltzmann constant, T is the temperature, and e is the elementary electric charge. Therefore, the trap state density (D_{it}) can be extracted from the deviation of the s -value from the Boltzmann thermionic limit using the following relation:

$$s = \frac{\ln 10 \cdot k_B T}{e} \left[1 + \frac{e D_{\text{it}}}{C_{\text{ox}}} \right] \quad (5.2)$$

where k_B is the Boltzmann constant, T is the temperature, e is the elementary electric charge, C_{ox} is the gate insulator capacitance per unit area. The D_{it} was $\sim 5.5 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ for the pure SnO channel device and largely improved to $\sim 2.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for the SnO:B TFTs. On the other hand, the D_{it} for the n -channel mode was evaluated as $\sim 1.0 \times 10^{13}$ and $\sim 7.0 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for the pure SnO and SnO:B-TFTs, respectively. The observations indicate that the subgap channel defect in the SnO channel was reduced by the incorporation of B. The improvement of device performances in the SnO:B channel was also confirmed for the pristine p -channel TFT without the ALD Al_2O_3 back-channel passivation.

We further analyzed the TFT characteristics to evaluate the effective subgap defect density of states (DOS), which corresponded to the trap state density, near the conduction band (CB) and valence band (VB) by the field-effect conductance (FEC) method, which was based on the analysis of the surface potential profile (ψ_s) using the subthreshold region conductance with respect to the gate bias. Since the surface potential gradient profile is affected by the defect DOS near the conduction/valence band, the effective subgap DOS can be extracted by the following equation:^[40-41]

$$DOS(E_F + \psi_{s,i}) = \frac{\varepsilon_s}{2q} \frac{\partial^2}{\partial \psi_{s,i}^2} \left(\frac{d\psi_{s,i}}{dx} \Big|_s \right)^2 \quad (i = 0, 1, 2, 3 \dots) \quad (5.3)$$

where, E_F is Fermi level, $\psi_{s,i}$ is surface potential, ε_s is permittivity, and i is the sequence beginning from the flat band to the accumulation mode. This method is widely used to analyze a full subgap DOS profile in semiconductor channels.^[42] **Figure 5.2(c)** shows the extracted effective subgap defect DOSs for the SnO and SnO:B channels. The p -channel SnO TFT without the ALD Al_2O_3 passivation is also included for comparison. A high-density shallow donor-like defect near VB, which acts as a hole trap, is observed in the p -channel SnO, indicating that the high-density donor-like defect hinders the ambipolar operation and only results in the p -channel operation. On the other hand, these ambipolar devices exhibit a lower density of donor-like near-VB state, and the defect density for the SnO:B channel is well suppressed to $\sim 10^{16} \text{ cm}^{-3}$ at $E - E_v$ (E_v : valence band energy) of $\sim 0.2 \text{ eV}$. Moreover, acceptor-like defects near CB, which works as an electron trap, were characterized in the ambipolar devices. The SnO:B channel exhibits a lower near-CB defect than the SnO channel. The analysis confirmed that the SnO:B channel exhibits lower subgap defect DOS and a better device performance was attributed to the reduction of subgap defect DOS. The presented device involves a higher near-CB-defect than the near-VB-defect, exhibiting slower

dynamic TFT responses of ~2 ms for the *n*-channel operation than the *p*-channel operation (~25 μ s).

The oxygen vacancy (Vo) defect is mainly considered the origin of hole trap states in the SnO channel, and terminating Vo is essential to improve ambipolarity.^[35] It is empirically well-known that incorporating a metal cation with a higher Gibbs free energy (ΔG_f) for oxidation effectively suppress the bulk Vo defect in ionic oxide semiconductors such as amorphous In–Ga–Zn–O.^[43–44] Since the ΔG_f of B₂O₃ is $-1273.5 \text{ KJ mol}^{-1}$, which is larger than that for SnO ($-280.7 \text{ KJ mol}^{-1}$), the boron incorporation reduces a bulk Vo defect in the SnO channel.^[45] We investigated the boron-doped SnO films with a Boron concentration of 5–15 at. % and observed that only 5 at. %-boron-doped film worked as a semiconductor, and all other films with higher B doping concentrations were insulative. This result indicates that the 5 at. % B doping is the optimized condition for TFT operation. The Hall-effect measurement revealed that the hole density and hole mobility for the 5 at. % SnO:B film were $\sim 8.1 \times 10^{17} \text{ cm}^{-3}$ and $1.7 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, respectively, which is nearly comparable to those for the pure SnO-films ($\sim 9.2 \times 10^{17} \text{ cm}^{-3}$ and $1.3 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$). The observation suggests that 5 at% B-doping does not affect the electrical property but effectively suppresses the Vo defect in the SnO channel. Therefore, the SnO:B channel shows an improved device performance at good reproducibility originating from the reduction of the subgap defect in the channel.

Figure 5.2(d) shows the typical hysteresis behavior in the double-sweep transfer characteristics measurement (V_{GS} sweeps from -50 to 50 V , then sweeps back from 50 to -50 V) for the ambipolar SnO:B TFTs. The counter-clockwise hysteresis and clockwise hysteresis were

observed for p -channel mode and n -channel mode, respectively, indicating the existence of both hole and electron trapping in the channel. A large hysteresis window for the n -channel mode indicates the presence of higher electron trap states than hole traps. This is consistent with the defect DOS obtained from the FEC analysis, as shown in **Figure 5.2(c)**. Since these carrier trapping/emission processes are recognized as similar to the neuromorphic transport in biological synapses, the ambipolar SnO:B device can imitate neurotransmitter releases that trigger the potentiation and depression behaviors.

Figure 5.2(e)-(f) also show the sequential double-sweep transfer characteristics measurements for the p and n -channel mode operations. For the p -channel mode, the gate bias swept sequentially from 10V to $V_{G(max)}$ ($-20, -30, -40, -50, -60$, and -70 V), while the gate bias was modulated sequentially from 10V to $V_{G(max)}$ ($30, 40, 50, 60, 70$, and 80 V) for the n -channel mode. The hysteresis window strongly depends on the $V_{G(max)}$, and a high $V_{G(max)}$ generates a large hysteresis window for both the n and p -channel modes. The V_{on} shift and hysteresis window linearly increase with the $V_{G(max)}$. These observations indicate that the carrier trapping-induced hysteresis can be controlled by modulating the gate bias, ensuring the reconfigurable hysteresis $I-V$ curves on both p/n - channel modes by tuning the polarity and amplitude of the gate bias.

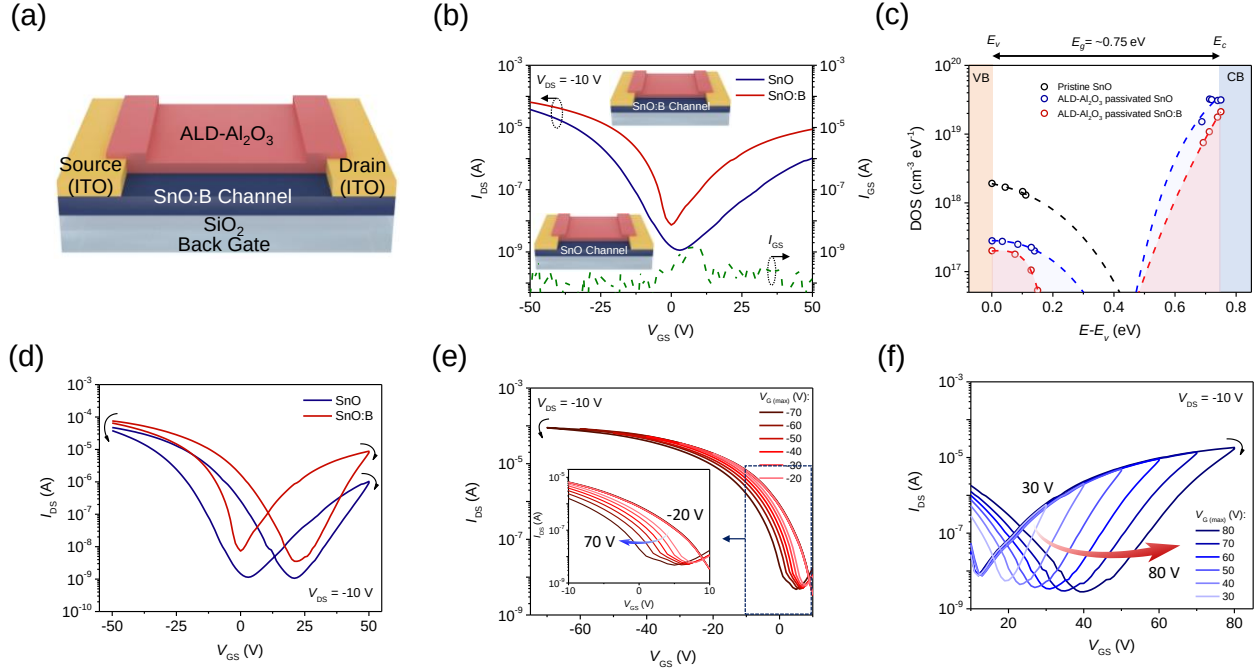


Figure 5.2 (a) Schematics of the device structure of the ambipolar SnO:B TFT with ALD Al₂O₃ back-channel passivation. (b) Typical transfer characteristics of the ambipolar SnO:B and SnO-TFTs at $V_{DS} = -10$ V. (c) Corresponding effective subgap DOS extracted from field-effect conductance (FEC) analysis for the ambipolar SnO:B (red), SnO-TFTs (blue), and p-channel SnO-TFT (black). (d) Typical hysteresis behavior of transfer characteristics. Variations of hysteresis windows for (e) p-channel mode by different gate bias-swept windows from 10V to $V_{G(\text{max})}$ (-20, -30, -40, -50, -60, and -70V) using V_{DS} of -10V, and (f) n-channel mode by different gate bias swept windows from 10V to $V_{G(\text{max})}$ (30, 40, 50, 60, 70, and 80V) using V_{DS} of -10V.

Next, we investigate the fundamental synaptic plasticity for the ambipolar SnO: B TFT-based artificial synapse in the excitatory and inhibitory response modes. (**Figure 5.3**) The presynaptic signal was given by positive and negative spikes (V_{pre}) using gate bias, and the V_{DS} monitored the drain current corresponding to PSC. The excitatory and inhibitory response modes are modulated by the base gate voltage pulse, and the device is operated in the excitatory mode when the negative base gate voltage pulse is applied, while the positive base gate voltage pulse performs the inhibitory mode.

Figure 5.3(a),(b) shows the excitatory response mode using the p -channel mode by applying a negative gate bias. (the base voltage of -10 V) The consecutive 50 pulses (-20 V of pulse voltage, -10 V of base voltage, 10 ms of pulse width, and 50 ms of pulse period) were applied for the initial modulating process to form a positive net charge with a minimum conductance by using hole trapping.

First, the PSCs were measured at five gate bias pulses with a pulse voltage of 10 V, a base voltage of -10 V, a pulse width of 10 ms, and a pulse period of 50 ms. The rapid increase in PSC is observed, confirming the potentiation behavior by the excitation of the presynaptic signal induced by gate bias spikes. (**Figure 5.3(a)**) The behavior emulates the excitatory postsynaptic potentials (i.e., potentiation behavior) by releasing excitatory neurotransmitters in biological synapses. The spike current was clearly observed just after the pulse inputs, indicating the emission process of trapped holes with a decrease in the net positive charge. The PSC gradually decreases after the pulse train due to the trapped hole emission under -10 V of the base reading voltage. The PSC is saturated to ~ 4.59 μ A, which is higher than the initial conductance state. The difference of

the initial and final conductance state is defined as ΔPSC ($\sim 0.23\mu\text{A}$) to represent the potentiation behavior responding to the signal stimulus.

In contrast, when five gate pulses with a pulse voltage of -20 V , a base voltage of -10 , a pulse width of 10 ms , and a pulse period of 50 ms were applied, the PSC decreased due to the effect of hole trapping in the SnO:B channel, indicating the depression behavior under the negative voltage of a presynaptic signal. (**Figure 5.3(b)**) This corresponds to the inhibitory postsynaptic potentials (i.e., depression behavior) caused by releasing inhibitory neurotransmitters. The PSC gradually increased due to the hole emission after the pulse train, and the ΔPSC of $\sim -0.15\mu\text{A}$ was obtained for the depression behavior.

Figure 6.3(c),(d) show the inhibitory response mode using the *n*-channel mode with a positive gate bias. (the base voltage of 20 V) The consecutive 100 pulses (pulse voltage = 30 V , base voltage = 20 V , pulse width = 10 ms , pulse period = 50 ms) are applied for the initial modulating process. In this case, electron trapping forms a negative net charge with a minimum conductance for the *n*-channel mode. The PSC increased under a negative amplitude voltage of -20 V (pulse voltage = 0 V , base voltage = 20 V , pulse width = 10 ms , pulse period = 50 ms), indicating the potentiation behavior stimulated by the inhibitory presynaptic signal. (**Figure 5.3(c)**) While the PSC decreased under the positive amplitude voltage using five positive amplitude gate pulses (pulse voltage = 30 V , base voltage = 20 V , pulse width = 10 ms , pulse period = 50 ms). The results show the depression behavior under a positive voltage of a presynaptic signal. (**Figure 5.3(d)**) These responses in the inhibitory mode are opposite to the responses in the excitatory mode.

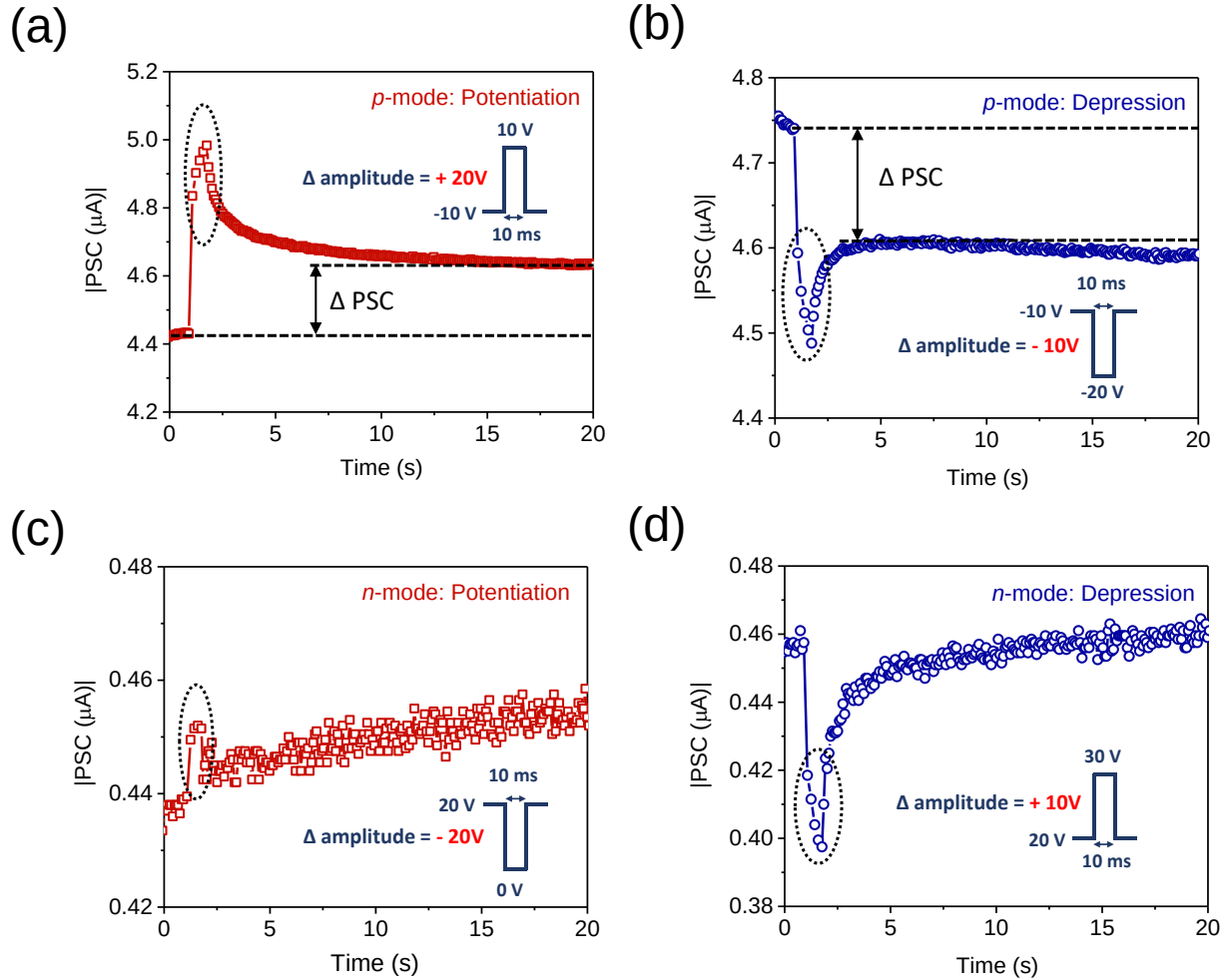


Figure 5.3 (a) Potentiation behavior in the excitatory response mode: a positive ΔPSC caused by a positive presynaptic spike (a pulse voltage of 10 V, a pulse width of 10 ms, and a pulse period of 50 ms). (b) Depression behavior in the excitatory response mode: a negative ΔPSC caused by a negative presynaptic spike (a pulse voltage of -20 V, a pulse width of 10 ms, and a pulse period of 50 ms). (c) Potentiation behavior in the inhibitory response mode: a positive ΔPSC caused by a negative presynaptic spike (a pulse voltage of 0 V, a pulse width of 10 ms, and a pulse period of 50 ms). (d) Depression behavior in the inhibitory response mode: a negative ΔPSC caused by a positive presynaptic spike (a pulse voltage of 30 V, a pulse width of 10 ms, and a pulse period of 50 ms).

We next discuss the fundamental characteristics of biological synapses, including the potentiation, depression, and paired-pulse facilitation (PPF) mimicked in a single device for both the excitatory and inhibitory operation modes. **Figure 5.4(a),(b)** show the repeatable modulation of the synaptic weight for the potentiation and depression behaviors, which are the significant operations in neuromorphic device applications. We first discuss the device operated in the *p*-channel mode for the excitatory response. After the initial process, the 50 positive pulses (pulse voltage = 10V, base voltage = -10 V, pulse width= 10 ms, pulse period= 50 ms) are consecutively applied at the presynaptic input of the device for potentiation, followed by 50 negative pulses for depression. (pulse voltage = -20 V, base voltage = -10 V, pulse width= 10 ms, pulse period= 50 ms) The PSC increases from 1.4 to 2.2 μA with $\sim 37\%$ weight change by a positive V_{GS} pulse sequence, demonstrating a potentiation behavior. While the subsequent negative input pulse sequence leads the PSC to decrease from 2.2 to 1.4 μA , resulting in a depression behavior. (**Figure 5.4(a)**) Since the current increases with the positive input spikes and decreases with the negative input spikes, the *p*-channel mode demonstrates a synaptic excitatory response mode. For the *n*-channel mode, on the other hand, the I_{DS} was measured at the base read pulse of 20V of V_{GS} after applying the training pulses. The PSC increases from 0.44 to 0.53 μA with a $\sim 27\%$ weight change by a negative amplitude V_{GS} pulse sequence, indicating potentiation behavior. Moreover, the subsequent positive amplitude input pulse sequence leads the PSC to decrease from 0.53 to 0.43 μA , performing a depression behavior. (**Figure 5.4(b)**) It reveals that the *n*-channel mode operation can imitate the synaptic inhibitory response mode. We also examined the dual-mode synaptic device performances for the SnO-TFTs. Compared to the non-doped SnO-TFT-based synaptic device, SnO:B TFT offers a well-balanced current response for both the excitatory and inhibitory responses originating from better ambipolarity. We also observed that the PSC response largely

depended on the pulse width and interval. Therefore, this result suggested that the phenomenon was triggered by the carrier trapping/emission process, which was a time-dependent process.

We also performed an endurance test to evaluate the reliability of device operation and confirmed that no apparent degradations were observed after > 5,000 pulse operations. Dynamically reconfigurable modulation between the excitatory and inhibitory modes by switching *n*- and *p*-channel modes is one of the critical advantages of the ambipolar-TFT-based synaptic device. We demonstrated a reconfigurable switching between the excitatory and inhibitory modes using the ambipolar operation in the presented SnO:B-TFTs.

PPF by synaptic facilitation and paired-pulse depression (PPD) by synaptic depression are well-known important characteristics for short-term plasticity and play an essential role in information processing in biological systems.^[46-47] **Figure 5.4(c),(d)** show the PPF/PPD mimicked in a single device for both the excitatory and inhibitory operation modes. When the synapse is stimulated by a paired temporal potential, the postsynaptic current induced by the second pulse is larger than the first one. The presented ambipolar transistor-based synaptic device also emulates the PPF/PPD in response to two consecutive presynaptic pulses separated by a short time duration in the excitatory and inhibitory response modes. The PPF and PPD index ratio is expressed by

$$PPF/PPD = (I_2 - I_1)/I_1 \times 100\% \quad (5.4)$$

where I_1 and I_2 is are channel current induced by the first and second presynaptic spikes, respectively. **Figure 5.4(c)** plots the PPF as a function of the pulse interval (Δt) for the potential and depression in the *p*-channel mode. Similar to the biological synapses, the PPF rapidly decreases with an increase in the pulse intervals. A longer pulse time interval causes less

potentiation and depression behaviors. In the potentiation process, small conductance change is considered a re-trapping effect in large pulse intervals. In contrast, a small pulse interval generates a larger conductance change for the depression because the emission of trapped holes is ignored. Similar behavior was also observed in the n -channel mode operation. **(Figure 5.4(d))** The conductance change related to the spike interval indicates that the previous activity of the synapse is a key factor in changing the ΔPSC . Since the carrier trapping/emission process is a nonlinear process, it is reasonable that the conductance change saturates by longer intervals between the spikes.

Moreover, the PPF/PPD index and the pulse intervals connect with a double-exponential function as the following equation

$$PPF/PPD = A_1 \exp(-\Delta t/\tau_1) + A_2 \exp(-\Delta t/\tau_2) \quad (5.5)$$

where A_1 and A_2 are the constants for the initial facilitation magnitudes of the two phases, and τ_1 and τ_2 are the relaxation times of the rapid and slow phases. For the p -channel mode, the obtained τ_1 and τ_2 for the potentiation are 85.4 and 562.7 ms, and the τ_1 and τ_2 of the depression are 16.1 and 731.0 ms. While the n -channel mode exhibited the τ_1 and τ_2 of 21.9 and 261.2 ms for the potentiation and τ_1 and τ_2 of 16.7 and 1581.5 ms for the depression, respectively. These are nearly comparable to the characteristic relaxation times observed in biological synapses, confirming that the presented device well-mimics the neuromorphic behavior of the biological synapses.^[48]

Moreover, energy consumption is an important metric for a neuromorphic computing system. The power consumption per pulse for the “writing” process was estimated from the gate

leakage current ($\sim 10^{-10}$ A), which was 0.02 ~ 0.03 nJ using the presented pulse operation. On the other hand, the power consumption per pulse for the “reading” process can be evaluated by

$$P = V_{DS} \times \Delta I \times t_p \quad (5.6)$$

where V_{DS} , ΔI , and t_p are the source–drain voltage, the change of PSC, and the pulse width, respectively. The smallest power consumption for the presented device was estimated as < 20 and < 2 nJ per pulse for excitatory and inhibitory operations. These are comparable to previously reported dual-mode 2D material-based synaptic devices. The V_{DS} condition we used in this study is relatively larger than other studies, and the power consumption would be further improved using a smaller V_{DS} .

Figure 5.4(e) also shows the map of the conductance change for 25 devices for the potentiation and the depression in both excitatory/inhibitory modes. All the measured synaptic devices showed comparable conductance change in the potentiation and depression for both modes with a good spatial uniformity. The spatial deviation of the conductance change for the potentiation and the depression are evaluated as 8.9% and 9.9% for the excitatory synaptic response mode and 9.9% and 8.1% for the inhibitory synaptic response mode, respectively. The small spatial variation of the conductance change is due to the good uniformity of the transfer characteristics of SnO:B TFTs. The batch-to-batch deviations of the conductance change were ~3.6% and ~4.9% for the excitatory synaptic response mode and ~4.0% and ~2.1% for the inhibitory synaptic response mode, respectively, indicating good reproducibility. Moreover, no significant degradation of device performances was observed even after 3 months-storage under a non-controlled ambient atmosphere. These results originated from high device yield, a good spatial and batch-to-batch

uniformity of the stable SnO:B channel, promising that the presented device has a high potential for practical neuromorphic applications with good scalability and reliability.

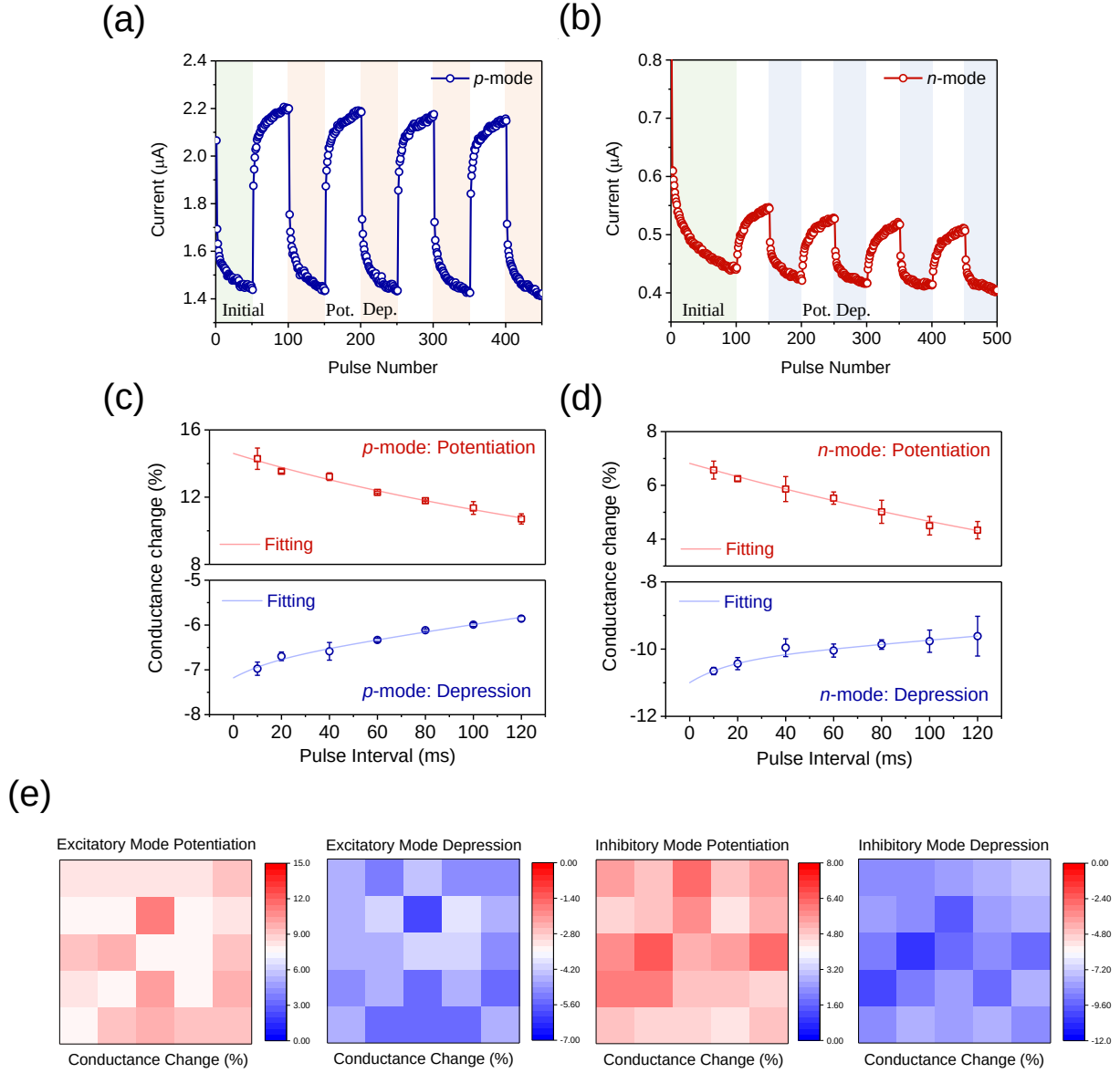


Figure 5.4 (a) Potentiation and depression properties in the excitatory response mode under consecutive training pulses, demonstrating the analog switching characteristic. (b) Potentiation and depression properties in the inhibitory response mode under consecutive training pulses demonstrate the analog switching characteristics. (c) Pulse interval dependence of potentiation and depression properties in the excitatory response mode. (d) Pulse interval dependence of potentiation and depression properties in the inhibitory response mode. (e) Map of the conductance change of 25 devices for potentiation and depression in both excitatory/inhibitory modes.

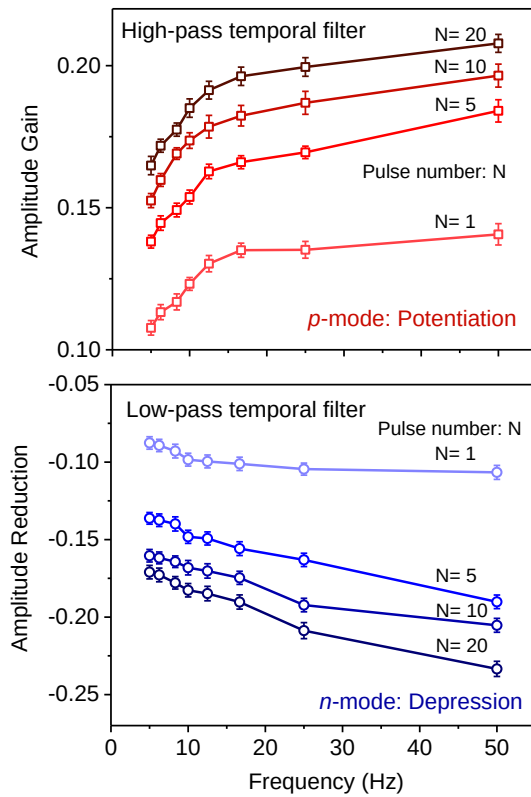
Finally, we demonstrated a high-pass/low-pass temporal filter for signal processing like brain functions using the presented SnO:B-TFT, which exhibited a high stimulus frequency dependence of the plasticity process. A short-term synaptic facilitation contributes to high-pass temporal filtering, while synaptic depression results in low-pass temporal filtering. **Figure 5.5(a),(b)** show the conductance amplitude gain (potentiation) and reduction (depression) as a function of frequency under different pulse numbers for positive/negative amplitude spikes. The conductance amplitude gain/reduction, defined as $(I_n - I_1)/I_1 \times 100\%$, is used as the indicator of the filtering property of the device, where I_1 and I_n represent the conductance amplitude of the first and last spikes, respectively. For p -channel mode operation, the amplitude gain increases gradually with a higher stimulation frequency under the positive amplitude spikes, indicating that it can be used as a high-pass temporal filter. (**Figure 5.5(a)**). The conductance amplitude reduction also increases with a higher frequency, suggesting the low-pass temporal filter characteristics for the negative amplitude input signals (**Figure 5.5(b)**). Similarly, the n -channel mode operation demonstrates high-pass and low-pass temporal filter properties for the negative and positive amplitude pulses. These results indicate that the ambipolar SnO:B TFT synaptic devices can screen input positive/negative amplitude signals with different stimulus frequencies, enabling complex information processing.

The coexistence of the excitatory and inhibitory modes in a single device provides more freedom to design neuromorphic computation and systems. The dual-mode property provides a function to regulate the frequency-dependent synaptic plasticity to frequency-independent plasticity, enabling versatile applications. It is well known that the interaural time difference (ITD) and interaural level difference (ILD) are two major mechanisms for sound localization in the

human auditory system. Since frequency-selective signals produced by excitatory and inhibitory synapses cannot be processed, it is vital to encode only ITD information with a frequency-independent synaptic response for sound localization. We observed that frequency dependence response can be compensated by mixing the response of excitatory and inhibitory modes to achieve a frequency-independent output signal amplitude by two dual-mode synaptic devices.

(a)

Positive amplitude spike



(b)

Negative amplitude spike

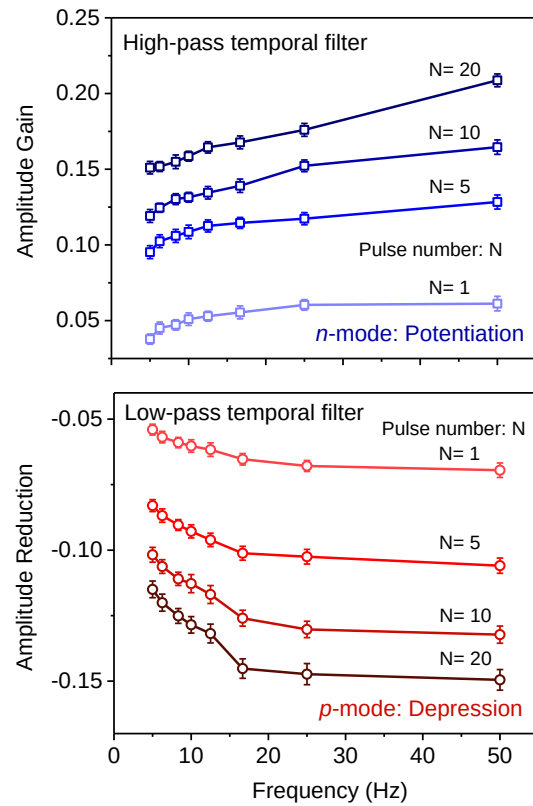


Figure 5.5 (a) Conductance amplitude gain (p -mode) and reduction (n -mode) as a function of frequency under different pulse numbers by positive amplitude spikes. (b) Conductance amplitude gain (n -mode) and reduction (p -mode) as a function of frequency under different pulse numbers by negative amplitude spikes.

5.4 Conclusions

The dynamic reconfigurable excitatory and inhibitory synaptic response in a single synaptic device was demonstrated using a low-temperature processed ambipolar SnO-based TFT. To improve the ambipolarity, that is, *n*- and *p*-channel mode operations, we developed a boron-incorporated SnO (SnO:B) as an active channel for the ambipolar-TFT. The subgap defect in the SnO:B channel was well suppressed as compared with the non-doped SnO channel and was estimated as $\sim 10^{16} \text{ cm}^{-3}$ at $E-E_V$ of $\sim 0.2 \text{ eV}$. The significant improvement of the saturation TFT mobility for *n*-channel mode (the μ_{sat} of $\sim 0.14 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) was achieved in the SnO:B channel and the well-balanced ambipolar TFT characteristics were produced. Beneficial from the carrier trapping/emission effect and the ambipolar property, the synaptic response can be dynamically modulated by the gate bias to emulate both the excitatory and inhibitory synapse responses effectively. Important synaptic characteristics such as potentiation/depression and paired-pulse facilitation/depression for both the excitatory and inhibitory response modes were enabled in a single artificial synapse. The reconfigurable excitatory and inhibitory response is critical to building the emerging neuromorphic hardware to emulate complicated biological functions. Moreover, the dual-mode operation also tunes the frequency-dependent synaptic plasticity to frequency-independent plasticity, enabling versatile applications. Compared to previously reported devices using 2D materials, the oxide semiconductor device presented several advantages such as better conductance update property, low power consumption, an easy fabrication process using a conventional film growth method with good reproductivity, and stable device operation under an ambient atmosphere. A good uniformity of device performances, decent operation reliability, and long-term environmental stability were also confirmed. The low-cost processability

and scalability of oxide semiconductor materials and devices offer an excellent opportunity to develop future AI systems.

Chapter 5, in full, is a reprint of the material as it appears in ACS Applied Materials & Interfaces 14, 22252-22262, 2022. Chi-Hsin Huang, Yong Zhang and Kenji Nomura. The dissertation author was the primary investigator and author of this paper.

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Chapter 6 Artificial Synapse based on Atomically Thin SnO₂ Memtransistor with Dynamically Tunable Analog Switching for Neuromorphic Computing

6.1 Introduction

Memristors are a promising electronic element with digital and analog resistive switching that can store and process information for non-volatile memory, circuit/logic applications, in-memory computing, and neuromorphic computing.^[1-5] Two-terminal memristors require a selector device to program individual memory/synapse nodes in a crossbar array for memory application and neuromorphic computing. Several approaches have been proposed,^[6-11] including the one-transistor-one-memristor (1T1M) configuration.^[12-13] However, the integration of the memristor and transistor limits the circuit density, and the integration process is often complicated. Therefore, the gate-tunable memristor, a so-called memtransistor that combines memory and switching functions into a single device, is expected greatly to address these issues and offer a new opportunity for memristive circuits and related applications.^[14-16]

The gate tunability function that is not compatible with two-terminal memristors leads to a wider tunability of resistive states.^[17-18] Particularly, a memtransistor is greatly promising for artificial synapse due to the additional extra controllability of the synaptic weight, that is, conductance changes in potentiation and depression states by the third modulatory terminal enable to emulate a variety of different synapse functions.^[18-19] Moreover, the conductance responses controlled by the gate bias enable us to tune the linear conductance response for high-performance neuromorphic computing. The natural integration of memristor with transistor functions offers a higher density footprint, multistate storage capability, and complex neuromorphic learning.

Metal oxides are well-recognized as a strong candidate for memristors due to their excellent resistive switching characteristics.^[2, 20-22] Besides, two-dimensional (2D) materials with a controlled atomically ultrathin film thickness can effectively improve the power consumption by reducing the operation and leakage current. Taking advantage of an ultrathin active layer with excellent mechanical properties (e.g., flexibility and light weight), a more advanced, cost-effective, and flexible 2D materials-based memristor can be developed for next-generation electronics. Therefore, developing an atomically ultrathin oxide nanosheet memristor is essential to advance future ubiquitous low-power computing and artificial intelligence systems.^[23]

However, most of the conventional resistive switching metal oxides are non-layered crystalline oxides, which implies that it is challenging to grow 2D nanosheets using conventional growth methods such as mechanical exfoliation and chemical vapor deposition.^[24] Among several oxide materials, tin oxide has a family of several compounds composed of different oxidation states of Sn (i.e., SnO₂, Sn₂O₃, Sn₃O₄, SnO, and Sn).^[25] The multiple oxidation states of tin oxide potentially lead to resistive switching, but the resistive switching is hindered by high carrier conductance due to unintentional electron doping of a conventional SnO₂ thin film. The atomically thin SnO₂ memristor with a lateral two-terminal configuration can address the high carrier conductance and can be used for developing a ReRAM device. Moreover, SnO₂ is a well-known *n*-type semiconductor with high electron mobility. Therefore, the atomically-thin SnO₂ nanosheet is an attractive material for developing a gate-tunable memtransistor with transistor and memristor functions.

Here, we fabricated a large-scale polycrystalline 2D-SnO₂ nanosheet memristor with a film thickness of ~2 nm by using a liquid metal route^[26-27] and developed a 2D oxide memtransistor with a 2D-SnO₂ nanosheet channel for neuromorphic computing. Dynamically gate-tunable analogy switching was demonstrated with near-linear weight updates and an improved conductance ratio. The neural network simulation for pattern recognition with a high recognition accuracy of ~92.25% was achieved in the presented gate-tunable 2D-SnO₂ memristors.

6.2 Experimental Section

Synthesis of 2D SnO₂ nanosheets

Atomically thin SnO₂ nanosheets were prepared on a SiO₂/Si substrate using the liquid metal printing method. Elemental tin (99.99%, Shot Metals) was first melted on a glass substrate at ~250 °C in ambient air. The top pre-existing oxide layer on the molten metal was removed by scrapping off to expose a pristine metal surface. Then, the freshly formed surface oxide layer was transferred from the liquid metal surface to the SiO₂/Si substrate by touching it. The surface of the SiO₂/Si substrate was treated with O₂ plasma (rf power = 70W for 1 min) and pre-heated to ~ 250 °C. The film structure and composition of the nanosheet were analyzed by high-resolution transmission electron microscopy (HRTEM) and scanning transmission electron microscopy (STEM)-energy-dispersive X-ray spectroscopy (EDS). The TEM lamella samples were prepared using a standard procedure using a focused ion beam (FIB). The surface morphology and film thickness were evaluated by atomic force microscopy (AFM).

Device fabrication and electrical characterization of 2D SnO₂ memristor

A gate-tunable 2D SnO₂ memtransistor with a bottom-gate and top source/drain contact structure was fabricated. After the source and drain electrode areas were patterned using the photolithography process, 5 nm-Ti/50 nm-Au was deposited by e-beam evaporation at room temperature. Then, the source and drain electrodes were defined by using the lift-off process. The channel length (L) and width (W) are 50 and 300 μm, respectively. The two-terminal electrical property was characterized using source/drain electrodes using a semiconductor device analyzer at room temperature in ambient air. The three-terminal resistive switching characteristics were studied using SiO₂/p⁺-Si substrates as gate oxide/gate electrodes.

Pattern recognition simulation

The pattern recognition simulation task was performed by using the platform “CrossSim”^[28-31], which was a programming interface to build different algorithms based on crossbar array architectures with experimental synaptic device properties. Two different datasets were used: an 8×8 pixels image version of handwritten digits from the “Optical Recognition of Handwritten Digits” dataset and a 28×28 -pixel version of handwritten digits from the Modified National Institute of Standard and Technology (MNIST) database. For 8×8 pixel images, the simulated artificial neural network has 64 pre-neurons, 300 hidden neurons, and 10 output neurons. After training with 3823 images, the system was used to recognize a separate 1797-image testing set. For 28×28 pixels images, the simulated artificial neural network has 784 pre-neurons, 300 hidden neurons, and 10 output neurons. After training with 60000 images, the system was used to recognize a separate 1000-image testing set.

6.3 Results and Discussion

Figure 6.1(a) shows the atomic force microscopy (AFM) image of tin oxide nanosheets prepared using the liquid Tin (Sn) metal-printing method. The detailed fabrication procedure is described in the Experimental Section. Polycrystal grains with an average size of ~ 65 nm and polycrystalline features were found. As shown in **Figure 6.1(b)**, the step height profile allows for determining the film thickness of the oxide nanosheet. The thinnest thickness was evaluated as ~ 2 nm, which corresponded to ~ 8 monolayers (MLs) of rutile SnO_2 . Significantly, 2D oxide nanosheets with a large area with an average sheet size of >100 μm can be grown. In addition to the low-temperature fabrication process at ~ 250 $^\circ\text{C}$, the process is performed with vacuum-free, solvent-free, and highly friendly wafer-scale technology.

Figure 6.1(c), (d) show the cross-sectional transmission electron microscopy (TEM) image of 2D- SnO_2 , indicating a uniform nanosheet with a thickness of ~ 2.5 nm. The high-resolution TEM (HRTEM) image, as shown in **Figure 6.1(e)**, indicates an ordered atomic lattice arrangement with the internal spacings of 0.21, 0.26, and 0.33 nm, which are assigned to the (120), (101), and (110) crystal planes of the rutile structure of SnO_2 , respectively. We also fabricated SnO_2 nanosheets with a thickness of ~ 10 nm to investigate the crystal structure by selected area electron diffraction (SAED) and confirmed that the synthesized nanosheet was SnO_2 . These observations concluded that the 2nm-thick-nanosheet was polycrystalline SnO_2 with no preferred crystal orientations. The cross-sectional scanning TEM (STEM) image and the corresponding energy-dispersive X-ray spectroscopy (EDS) chemical composition map, as shown in **Figure 6.1(f)-(h)**, also confirms three distinct layers, including a SiO_2 protection layer, ~ 2.5 nm synthesized 2D SnO_2 nanosheet, and a thermal-oxidized SiO_2 layer on the Si wafer.

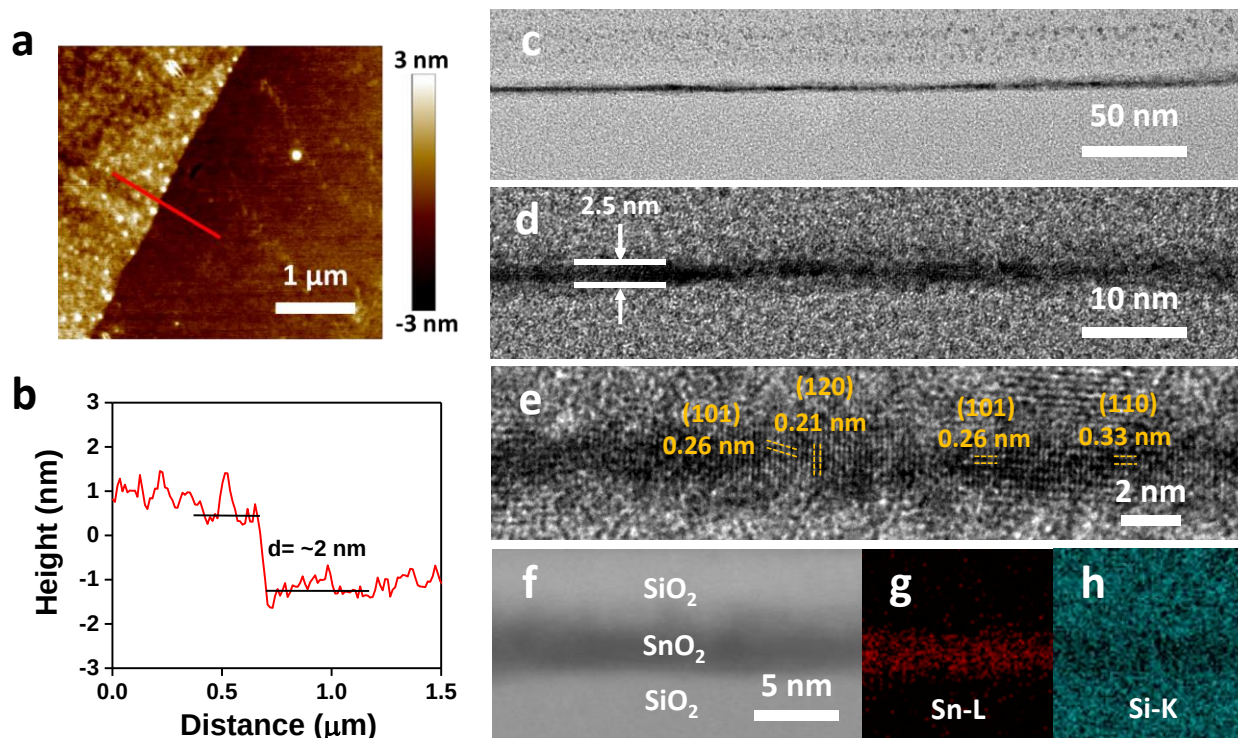


Figure 6.1(a) AFM image for the 2D SnO₂ nanosheet with (b) cross-sectional step height profile corresponds to the red line as indicated. (c)-(e) Cross-sectional TEM images of the 2D SnO₂ nanosheet with different magnifications. (f) Cross-sectional STEM image and the corresponding EDS composition mappings of (g) Sn and (h) Si.

An inverted-staggered type, that is, bottom-gate and top-contact structure, field-effect transistor (FET) was fabricated using the 2D-SnO₂ nanosheet as a channel, as shown in **Figure 6.2(a)**. We first examined the resistive switching characteristics of 2D-SnO₂ using a lateral two-terminal structure with DC voltage sweep. **Figure 6.2(b)** shows the typical resistive switching I – V characteristics of the two-terminal 2D SnO₂ memristor. When the forward DC bias was applied from 0 to 15 V, the resistance gradually decreased and transited from a high-resistance state (i.e., HRS/OFF-state) to a low-resistance state (LRS/ON-state), which was defined as a “SET” process, and then maintained the LRS during the bias sweep back from 15 V to 0 V. When the reverse DC bias swept from 0 to -15 V, on the other hand, the resistance returned to HRS (i.e., “RESET” process). Therefore, the presented 2D SnO₂ device clearly shows a bipolar resistive switching behavior at room temperature. Unlike conventional conductive filamentary resistive switching devices, the presented memristor does not require any forming process to activate the switching operation. A low SET current of 0.12 μ A at 15 V and a low RESET current of 0.1 μ A at -15 V were observed, indicating the device operated with both low SET power (1.8 μ W) and RESET power (1.5 μ W). The low-power operation is nearly comparable to that of the reported planar 2D material-based memristors such as MoS₂-based memristors (the SET/RESET power = 3~1.36 $\times 10^4$ μ W/30 ~ 2 $\times 10^4$ μ W). The low operating current feature of the presented 2D SnO₂ memristor is mainly attributed to the nature of the ultrathin thickness of the 2D nanosheets, which limits the electron flow with large resistance. **Figure 6.2(c)** shows the endurance test at a reading voltage of 1 V. The resistances of the LRS and HRS are on the order of 10⁸ and 10⁹ Ω , respectively, showing a stable $R_{\text{OFF}}/R_{\text{ON}}$ ratio of ~10. The measured temporal variation, which is defined by the standard deviation (σ) / mean value (μ) of log (R_{HRS}) and log (R_{LRS}), is 1.16 and 1.41%, respectively, indicating the device exhibits uniform resistive switching during ~10³ cycles. The retention

characteristics indicate the device maintains the HRS/LRS over 10^4 s (**Figure 6.2(d)**), comparable to that for the state-of-the-art planar 2D MoS₂-based memristors.^[32-34] The statistical analysis of device-to-device variability showed a log-normal distribution of the $R_{\text{OFF}}/R_{\text{ON}}$ ratio with a mean and variance in $\log(R_{\text{HRS}}/R_{\text{LRS}})$ of 1.05 and 0.63, respectively. **Figure 6.2(e)** shows the double-logarithmic plot of the I - V curves at the SET process, where ohmic conduction (i.e., $I \propto V$) at the low bias region (< 1 V) can be found. In contrast, the current is proportional to the square of the bias voltage (i.e., $I \propto V^2$) in a high applied bias region ($> \sim 1$ V), suggesting that carrier conduction is mainly controlled by trap-associated space-charge-limited current (SCLC).^[35] It implies that the SnO₂ channel involves high-density electron traps. On the other hand, a linear curve with a slope of ~ 1 was observed in the whole region on the LRS, indicating that carrier transport for the LRS obeys ohmic conduction (**Figure 6.2(f)**).

Because the SnO₂ nanosheet has a polycrystal grain structure with a high-density grain boundary, we consider that grain boundary plays an essential role in resistive switching because grain boundary includes high-density oxygen vacancy (V_o) defects, which can act as the electron traps. Moreover, it is well known that grain boundary fluctuates the potential energy of conduction bands and forms a potential barrier in the vicinity of the conduction band minimum (CBM). The height is altered by the variation of charge distribution by electron trapping/de-trapping. The grain boundary-induced potential barrier model can explain the observed I - V characteristics for the presented devices.

Moreover, the I - V characteristics confirmed the presence of a Schottky barrier in Ti/SnO₂ interfaces. The effective Schottky barrier heights (SBH, Φ_B) was determined as ~ 203 meV from

the temperature dependence of the I – V characteristics. Therefore, we proposed the resistive switching mechanism based on SBH modulation by V_o defect migration for the presented 2D-SnO₂. In the proposed model, the unoccupied (V_o^{2+}) and partially occupied (V_o^{1+}) oxygen vacancies near the grain boundary regions migrate and accumulate near the source terminal under positive V_{DS} bias conditions. The accumulation of oxygen vacancies contributes to both the formations of the high-density electron trap state and the conductive non-stoichiometric phases such as SnO_x and Sn, which lower the SBH. Therefore, the resistive switching occurs to the LRS by positive V_{DS} . On the other hand, the negative V_{DS} induces electron de-trapping and removes V_o from the interface. Therefore, the HRS can be achieved.

Figure 6.2(g) shows the drain to source current (I_{DS}) – gate-source voltage (V_{GS}) characteristics, that is, transfer characteristics, for the 2D SnO₂ FETs. The device operates in n -channel mode, confirming that electron transport is dominant. The I_{DS} – drain-source voltage (V_{DS}) characteristics under different gate voltages demonstrate the gate-tunability of resistive switching (**Figure 6.2(h)**). The currents in both HRS and LRS can be modulated by the gate bias with a tunability factor of $>10^2$ when $V_{GS} = \pm 10$ V (**Figure 6.2(i)**). Moreover, a more significant rectifying effect and larger hysteresis were observed in the negative V_{GS} conduction. Similar I – V characteristics have also been observed in the reported MoS₂ memtransistors, and explained by asymmetric Schottky junction barrier modulation.^{15, 32, 33} When the negative V_{GS} is applied (**Figure 6.2(h)**), a larger SBH is formed because the Fermi level near the source terminal goes up, causing larger hysteresis. The gate-tunable memristors have been seldom discussed in the current memristive device, providing a new function for memristive circuits and related applications.

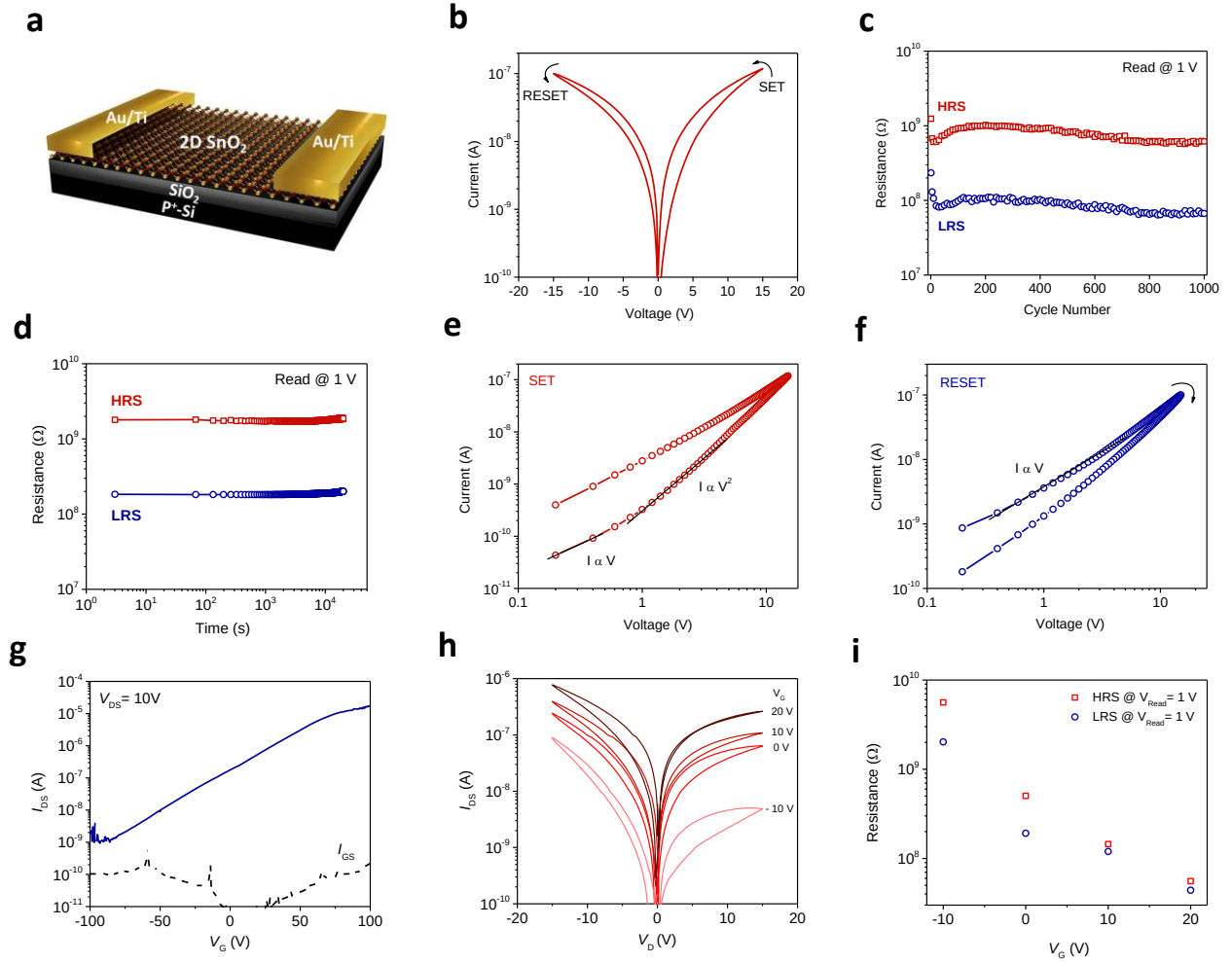


Figure 6.2 (a) Schematic of the inverted-staggered FET structure using the 2D-SnO₂ memristor channel. (b) Typical two-terminal I - V characteristics (no gate bias applied) of the 2D-SnO₂ memristor on the logarithmic scale. (c) Endurance test and (d) retention test in DC mode at a read voltage of 1V. (e)-(f) Double-logarithmic I - V plots for the 2D-SnO₂ memristor at (e) SET and (f) RESET, respectively. (g) I_{DS} - V_{GS} and (h) I_{DS} - V_{DS} characteristics for the gate-tunable 2D-SnO₂ memristor. (i) Variations of HRS and LRS by gate bias.

Next, we examined in detail the analog switching characteristics of the 2D-SnO₂ memristors to emulate the synaptic behavior of biological synapses (**Figure 6.3(a)**). In neuroscience, synaptic plasticity is the ability of synapses to strengthen or weaken over time, which can be regulated by the arrival of an action potential, including short-term and long-term synaptic plasticity.^[36-37] Under the external stimulus, action potentials from the presynaptic neuron can be transmitted through the synapse to the postsynaptic neuron, generating a postsynaptic current (PSC). The amplitudes of PSC determine the synaptic weight. Electronic synapses have been investigated for the building blocks of a brain-like computer, adopting the device conductance to simulate the synaptic weight plasticity.^[3, 38] Sequential voltage pulses are applied to the drain terminal as the presynaptic input, and the I_{DS} is continuously recorded as PSC (**Figure 6.3(b)**). **Figure 6.3(c)** shows analog switching behavior, that is, the conductance versus pulse number, of the two-terminal 2D SnO₂ memristor for potentiation (a 15V amplitude and a 5ms pulse width) and depression (–15 V and 5 ms) training pulses. After applying the training pulses, the conductance was measured at a reading pulse of 1 V and 5 ms. The conductance change of analog switching was observed under both the training pulse conditions, and the increase and decrease of conductance are assigned to the synaptic long-term potentiation (LTP) and long-term depression (LTD) of synaptic weights, respectively. The channel conductance increases from 4.05 to 5.65 nS with a weight change of ~39.5% by the positive V_{DS} pulse sequence, demonstrating the potentiation behavior. The subsequent negative V_{DS} pulse sequence leads the channel conductance to decrease from 5.65 to 4.05 nS, resulting in the depression behavior.

Linearity and the maximum/minimum conductance ratio (G_{max}/G_{min}) of LTP/LTD are crucial parameters for implementing electronic synaptic devices for neuromorphic computing, such

as the training accuracy of artificial neural networks.^[38-39] To evaluate the linearity of potentiation and depression, the change in conductance with the number of pulses is described as ^[39-40]

$$G_p = G_{min} + G_o(1 - e^{-\nu p}) \quad (6.1)$$

$$G_d = G_{max} - G_o[1 - e^{\nu(p-1)}] \quad (6.2)$$

$$G_o = \frac{G_{max} - G_{min}}{1 - e^{-\nu}} \quad (6.3)$$

where G_p and G_d are the fitting conductance for LTP and LTD, respectively. G_{min} and G_{max} are the maximum conductance and minimum conductance, respectively. ν is the nonlinearity (NL) factor, which is the indicator that shows the nonlinear behavior of the weight update of G_p and G_d . p is the normalized number of pulses and is expressed by $p = P/P_{max}$. (P and P_{max} are the pulse number and the maximum pulse number required to switch the device between G_{min} and G_{max}). The 2D SnO₂ memristors exhibited the G_{max}/G_{min} ratio of ~ 1.4 , a NL_p of 1.08 for potentiation, a NL_d of -2.56 for depression and an asymmetry ($|NL_p - NL_d|$)^[41] of ~ 3.64 .

The conductance response of an electronic synaptic device strongly depends on the pulse width, pulse amplitude, and pulse number. **Figure 6.3(d)** shows the analog switching of potentiation and depression under consecutive pulse sequences with different pulse widths of 5 – 100 msec. Obviously, the conductance change is increased with the increase in pulse width, and the wide pulse width leads to the fast potentiation and depression process of the PSC. The conductance change (ΔG) after 50 sets of the pulse sequence for both potentiation and depression increases from 0.45 to 4.1 and 0.4 to 4.5 nS, respectively, by a wide pulse width (**Figure 6.3(e)**). The narrowest pulse width for analog switching is ~ 5 ms, comparable to that of reported planar 2D MoS₂ that operates at milliseconds. Because the diffusivity/mobility of the carrier limits the operation speed, shortening the channel length will improve the operation speed for the presented devices. We

observed that the *NLs* for both potentiation and depression were degraded by increasing the pulse width (**Figure 6.3(f)**). This phenomenon is probably because a wide pulse width provides a long time interval for charge trapping to reach the trap capacity saturation for potentiation and de-trapping of the trapped charge for depression, even in fewer pulse numbers.

Figure 6.3(g) shows the analog switching under consecutive pulse sequences at different pulse amplitudes. Larger pulse amplitude conditions induce a large and faster change in PSC for potentiation and depression because more carrier trapping/de-trapping is involved under larger pulse amplitude conditions. We also confirmed that synaptic weight change strongly depends on pulse amplitude; the conductance changes for potentiation and depression are increased with the increase of pulse amplitudes (**Figure 6.3(h)**). The phenomenon demonstrates the spike-amplitude-dependent plasticity (SADP) function^[18] in the 2D SnO₂ memristors. The large pulse amplitude promotes the conductance change more rapidly at the beginning, resulting in a worse linear weight update for both potentiation and depression (**Figure 6.3(i)**). **Figure 6.3(j)** also shows the analog switching behavior measured at different pulse numbers for potentiation and depression. Although the conductance change is amplified by increasing the number of potentiation/depression pulses (**Figure 6.3(k)**), the conductance response for depression shows better linearly and symmetry in fewer pulse number conditions (**Figure 6.3(l)**). These observations indicate the conductance change is enhanced by pulse conditions, that is, the increase of pulse number, amplitude, and width, but the linearity of conductance weight in depression is degraded. From the above results, we consider the carrier trapping/de-trapping mechanisms, including different kinetics of trapping/de-trapping in defects and the effect of trapping/de-trapping capacity saturation, which are responsible for the nonlinear behavior. V_o has three charged states (i.e., V_o^{2+} , V_o^+ , and V_o) depending on the

number of trapped electrons, and exhibits different energy levels with different capture and emission kinetics.^[42-44] Most carriers are probably trapped by the shallow V_o^{2+} state, but the long-pulsed condition enables the capture of the electron at the deep V_o^+ state. This may cause the non-linear current response under the pulse training. When the electron trapping meets trapping capacity, moreover, the current is saturated. This also contributes to a non-linear behavior.

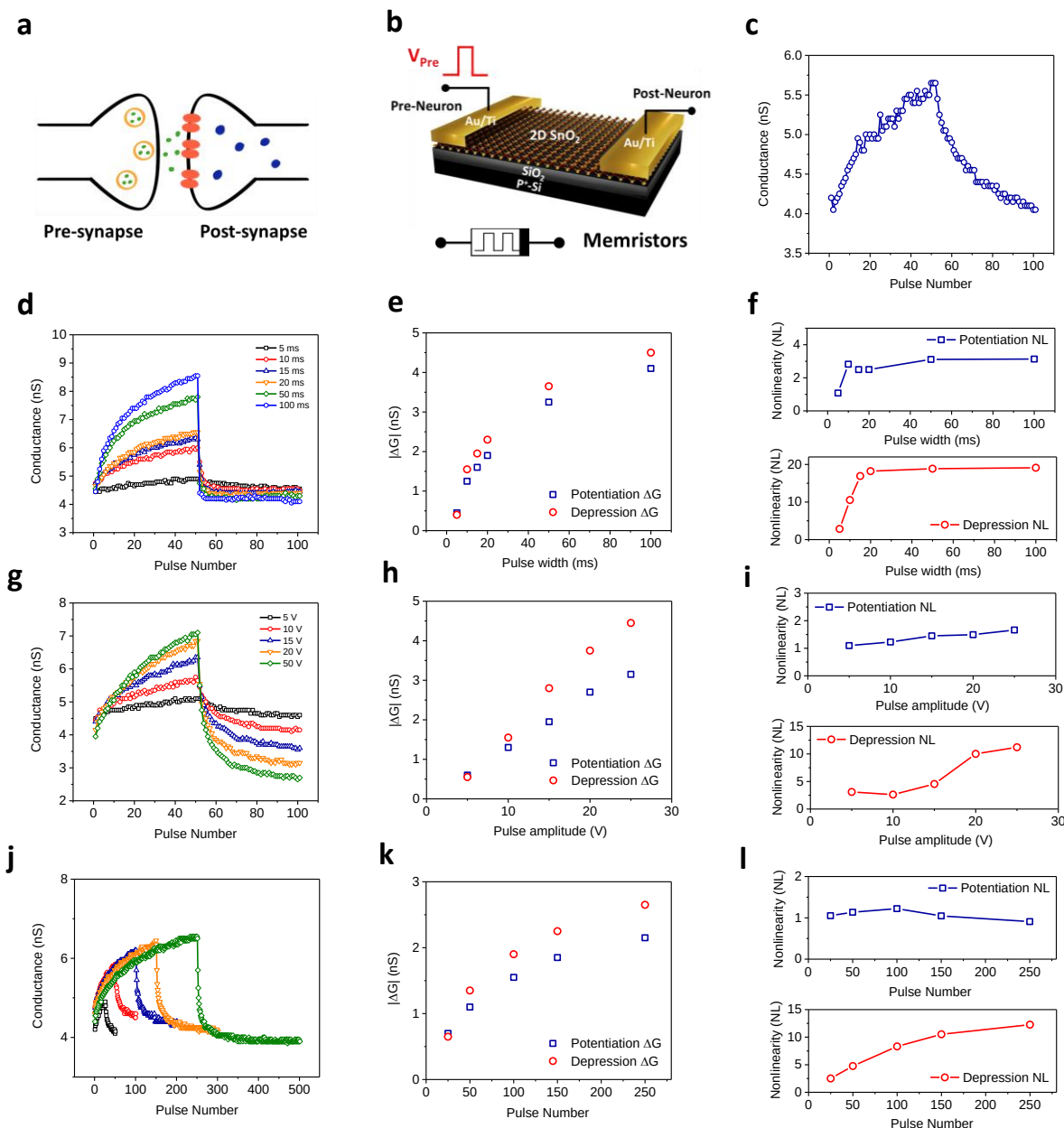


Figure 6.3 Schematic illustrations of (a) biological synapse with homosynaptic plasticity and (b) corresponding circuit diagram of the 2D SnO₂ memristor. (c) Analog switching behavior of the 2D SnO₂ memristor by potentiation (15 V and 5 ms) and depression (-15 V and 5 ms) training pulses. (d) Analog switching behavior, (e) conductance change, and (f) nonlinearity for potentiation and depression with different pulse widths. (g) Analog switching behavior, (h) conductance change, and (i) nonlinearity for potentiation and depression with different pulse amplitudes. (j) Analog switching behavior, (k) conductance change, and (l) nonlinearity for potentiation and depression with different pulse numbers.

It is well known that heterosynaptic plasticity is an essential synaptic synergistically modulated effect tuned by another modulatory interneuron in biology^[45] (**Figure 6.4(a)**). Therefore, the implementation of an artificial synaptic device is significant for developing neuromorphic computing systems. The gate-tunable 2D SnO₂ memristor, the 2D SnO₂ memtransistor, with a three-terminal structure, enables the emulation of heterosynaptic plasticity using the gate as the modulatory terminal (**Figure 6.4(b)**). **Figure 6.4(c)** shows the synaptic potentiation and depression characteristics under different gate modulations (V_G) with training pulses (± 15 V and 5 ms). The conductance change modulation, in which the conductance increases/decreases by positive/negative V_G , respectively, was observed, and the presented device demonstrated a dynamic modulation of synaptic behavior and successfully emulated heterosynaptic plasticity functions.^[46] Moreover, the modulations for the G_{max}/G_{min} ratio and the NL of the synaptic weight update in the potentiation/depression by the V_G is confirmed (**Figure 6.4(d),(e)**). The controlling of the G_{max}/G_{min} ratio by the gate bias offers further improvement of the learning performances. **Figure 6.4(f)** indicates the reproducibility of the potentiation and depression with different gate biases. The slopes of the current update are clearly altered by the gate bias (**Figure 6.4(c)**), indicating that the presented device has a tunable learning rate property that can optimize learning accuracy.^[47] In general, it is known that a learning process involves a fundamental trade-off between learning speed and accuracy. Thus, the ideal training scheme is built up of adopting the fast learning speed in the initial stage to learn input information, followed by the low learning speed to achieve optimal accuracy. Therefore, heterosynaptic plasticity, that is, the control of learning rate characteristics by gate bias, achieved in the presented 2D SnO₂ synaptic devices, is highly promising for neuromorphic systems. The inherently tunable synaptic

kinetics, which is inaccessible in conventional homosynaptic devices, offers new opportunities to design training schemes and learning algorithms with extra degree of freedom.

Moreover, we demonstrated that the conductance and the linearity adjustment can be significantly improved by dynamically controlling the gate bias within pulse training. **Figure 6.4(g)** shows the conductance update using the pulse scheme (+15 V / –15 V, 5 ms) with the dynamical modulation of the V_G from –2 V to 10 V for every 25 pulses in the potentiation and followed by the depression (+15 V / –15 V, 5 ms) with the V_G from 10 V to –2 V for every 25 pulses (**Figure 6.4(h)**). The device exhibited an improved G_{max}/G_{min} ratio of 3.36 and a synaptic weight change of ~236%. The nonlinearity for potentiation and depression are –0.43 and –1.43, respectively, indicating near-linear weight update and a significant improvement from the reported two-terminal resistive switching memory and lateral 2D material memristor-based synaptic devices^[41, 48-51]. The dynamically gate-tunable pulse scheme has a high potential to be implemented in other neuromorphic devices to break through the device limitation of linearity and weight update.

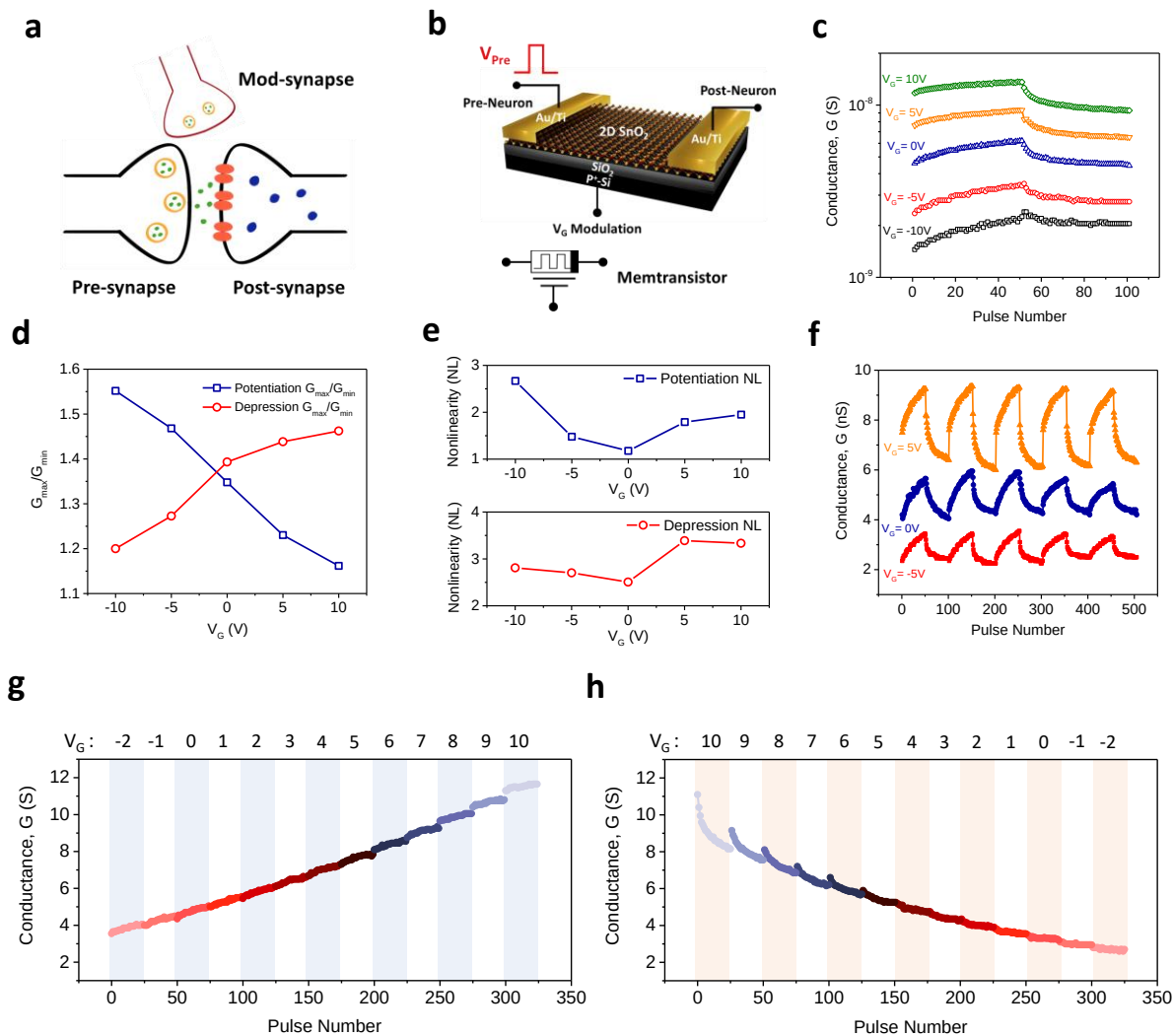


Figure 6.4 Schematic illustrations of (a) heterosynaptic plasticity and (b) corresponding circuit diagram for the gate-tunable 2D SnO₂ memristor (memtransistor). (c) Analog switching behavior of the 2D SnO₂ memristor by potentiation (15V, 5ms) and depression (−15V, 5ms) training pulses under different gate voltages. (d) G_{max}/G_{min} ratio and (e) nonlinearity for potentiation and depression under different gate voltages. (f) Repeatable potentiation and depression behaviors with different gate voltages. (g) Potentiation and (h) depression behaviors with the gate bias modulation.

Finally, we simulated an artificial neural network for pattern recognition using the device parameters for the presented 2D-SnO₂ memristor. The pattern recognition simulation task was performed by the platform “CrossSim” [28-31]. **Figure 6.5(a)** shows the simulated artificial neural network with 8×8 (28×28) pre-neurons, 36 (300) hidden neurons, and 10 output neurons. A three-layer neural network was used to execute supervised learning using a backpropagation algorithm. The 64 and 784 neurons of the input layer correspond to 8 × 8 and 28 × 28 pixels images, respectively, and the 10 neurons of the output layer correspond to 10 classes of digits (0–9). Each of the two layers used by the algorithm requires a crossbar array of a synaptic weight layer, as shown in **Figure 6.5(b)**. Here, the 2D-SnO₂ memristors act as the memory element in the crossbar array, and their channel conductance change was utilized as the weight update for performing the backpropagation algorithm. **Figure 6.5(c),(d)** show the pattern recognition accuracy for the simulated networks using the 2D-SnO₂ memristors. The accuracy in ideal numeric training is 96.88% and 98.23% for 8 × 8 and 28 × 28 pixels images, respectively. On the other hand, the obtained recognition accuracy after 200 training epochs is ~ 85.69 and ~ 84.70 % for 8 × 8 and 28 × 28 pixels images, respectively. The low recognition accuracy is mainly due to a small G_{max}/G_{min} ratio of ~1.4 because the minimum weight that can be mapped to the device conductance is determined by the G_{max}/G_{min} ratio.^[38] Significant improvement of the pattern recognition accuracy is achieved by implanting a dynamic gate-tunable function. By applying V_G from –2 V to 10 V for potentiation and from 10 V to –2 V for depression, the recognition accuracy improves to ~92.25 and ~89.26% after 200 training epochs for 8 × 8 and 28 × 28 pixels images, respectively (**Figure 6.5(e),(f)**). The higher accuracy is attributed to the improvement of the G_{max}/G_{min} ratio and linearity/symmetry by gate bias. The simulated pattern recognition accuracy is largely improved from state-of-the-art two-terminal resistive switching memories (10–70%)^[38].

^{41, 49]} and nearly comparable with those of the three-terminal charge-type synaptic transistor (70–86%)^[52-55] and electrochemical synaptic devices (>95%).^[28-29, 40]

Notably, the presented 2D-SnO₂ memristors exhibit an ultralow conductance (< 10 nS), which is lower than those of most of the reported synaptic devices. Because high operation current often causes misreading and high energy dissipation in crossbar architectures, the ultralow conductance characteristics are an advantage for large-scale neuromorphic systems. Besides, low power consumption in neuromorphic systems during training and learning is a crucial merit compared with von Neumann architectures. The average power consumption ($\bar{W}$) during training can be characterized using the following equation:

$$\bar{W} = (\Delta I \times V \times t) / N_{pulse} \quad (6.4)$$

where ΔI is the change of the channel current after training, V is the training voltage, t is the width of the training pulse, and N_{pulse} is the number of pulses. The power consumption for the presented device during LTP and LTD was estimated as ~4.8 pJ per pulse using 15/–15 V pulse amplitude and 5 ms pulse width as training pulse, which was remarkably lower than that of the conventional CMOS circuit (usually~hundreds pJ)^[28, 48], and comparable with low-power consumption synaptic devices. Because the gate bias modulation does not generate current flow to contribute to power consumption due to a negligible current level between the gate and source terminals, we only consider the channel current flow in the 2D- SnO₂ channel. Therefore, we can use the same equation to discuss the power consumption for the 2D-SnO₂-memristors with gate bias modulation. The power consumption of the memristors with the gate modulation is estimated to be ~1.9 pJ per pulse, which is nearly comparable with that for the device without the gate modulation.

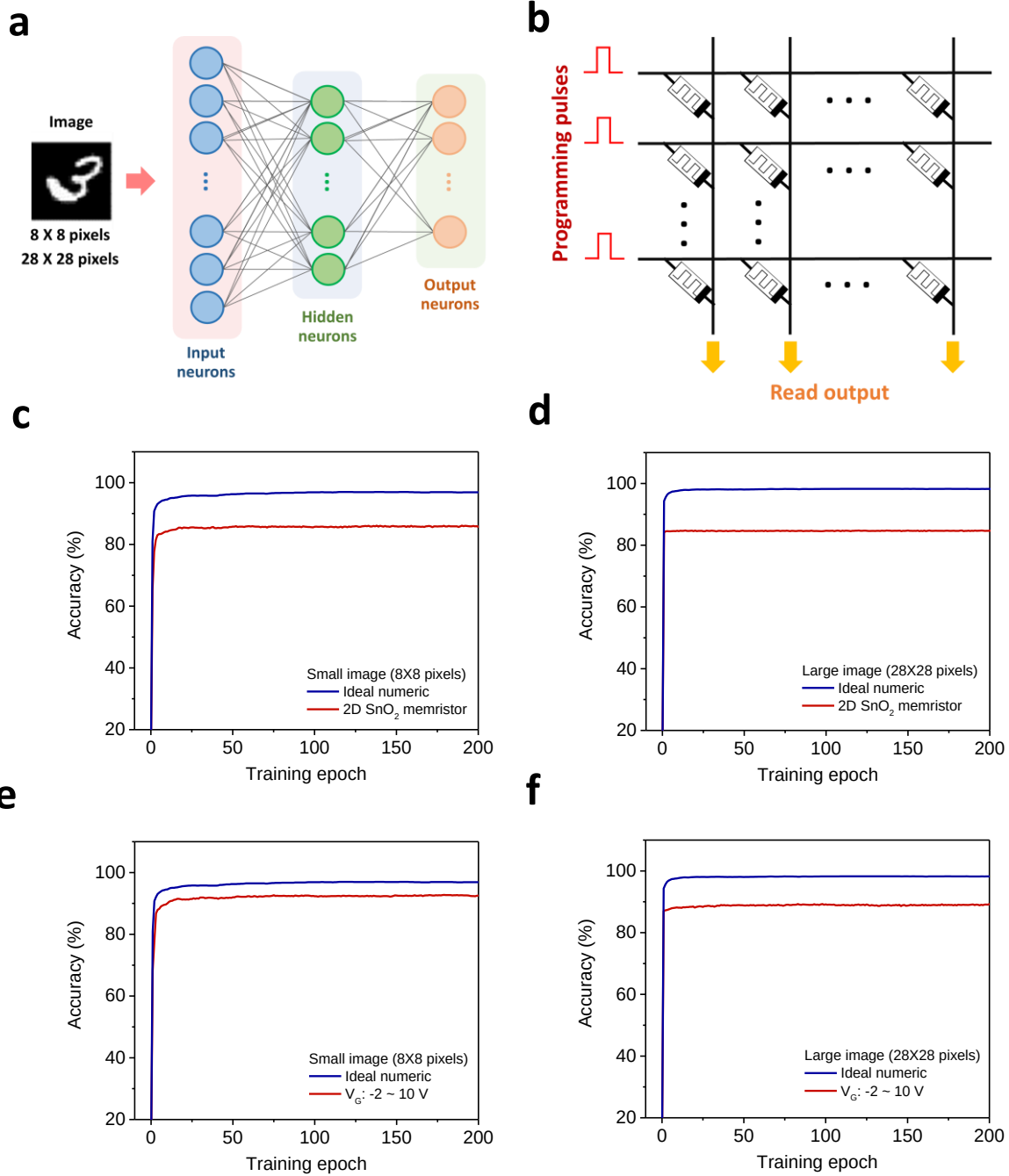


Figure 6.5 Schematic illustrations of (a) three-layer neural network for pattern recognition simulation and (b) synaptic weight layer composed of voltage-programmed crossbar arrays using the 2D SnO₂ memristor. Simulated pattern recognition accuracy of the 2D SnO₂ memristor without a gate bias for (c) 8×8 and (d) 28×28 pixels handwritten digit image datasets. Simulated pattern recognition accuracy of the 2D SnO₂ memristor with gate bias for (e) 8×8 and (f) 28×28 pixels handwritten digit image datasets.

6.4 Conclusions

A gate-tunable oxide memristor using atomically ultrathin-polycrystalline SnO₂ nanosheet with ~2 nm-thickness was developed for next-generation power-efficiency neuromorphic computing applications. The modulation of analog switching by gate bias was presented. Dynamically gate-tunable analog switching was demonstrated with the near-linear weight updates and improved conductance ratio. The artificial neural network simulation for pattern recognition with high recognition accuracy was achieved in the gate-tunable 2D-SnO₂ memristors. In addition, the presented planar 2D-oxide memristors with ultralow conductance offer low-power consumption operation and have a high potential to develop an energy-efficiency biological neural system such as the human brain (~fJ). The gate-tunability function in memristors will improve recognition accuracy and advance the development of neuromorphic devices that can mimic multiple synaptic connections in neurons.

Chapter 6, in full, is a reprint of the material as it appears in ACS Applied Materials & Interfaces 13, 52822-52832 (2021). Chi-Hsin Huang, Hsuan Chang, Tzu-Yi Yang, Yi-Chung Wang, Yu-Lun Chueh and Kenji Nomura. The dissertation author was the primary investigator and author of this paper.

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Chapter 7 Summary and Future Perspectives

In this thesis research, I focus on investigating and developing oxide semiconductors and devices, spanning from material design, growth, and processing to device fabrication and characterization and device modeling applied to circuit applications. Our goal is to contribute to future sustainable and advanced electronic applications, including large-area flexible integrated circuits, BEOL electronics in monolithic 3D integration for CMOS chips, and emerging computing devices for non-traditional computing platforms.

7.1 High-Performance *p*-channel Oxide TFT Development

Part I of this dissertation delves into developing high-performance *p*-channel oxide TFTs, covering material design, defect termination techniques, and the creation of atomically thin oxide semiconductors. We introduced a scalable liquid element treatment method to address structural defects in *p*-type SnO, specifically oxygen and metal cation vacancies, thus enhancing the performance of *p*-channel SnO TFTs. Furthermore, leveraging the liquid Bi-Sn eutectic alloy system enables precise control over Sn cation treatment at a low temperature of approximately 140°C. This capability facilitates hole concentration modulation and a wide range of threshold voltage adjustments for *p*-channel SnO TFTs. Moreover, we achieved high-performance *p*-channel oxide TFTs by utilizing atomically thin *p*-type SnO channels with a thickness of around 1 nm, showcasing extremely low off-current suitable for low-power oxide CMOS circuits. However, the current performance of *p*-channel oxide TFTs does not yet match that of commercialized a-IGZO TFTs. The lack of high performance hinders the potential advancement of oxide semiconductor TFT technology.

Developing high-performance *p*-type oxide TFTs is a crucial and highly challenging task that continues to be an active area of research. Eliminating high-density subgap defects in the bulk and back channels is essential to enhance device characteristics. This requires effective defect termination techniques to be developed. Furthermore, gaining a deeper understanding of material properties, especially carrier transport, electronic structure, and defect structures in *p*-type oxide semiconductors, is necessary to improve device characteristics further and enhance the quality of the channel material.

To achieve a significant technological breakthrough in material and device developments in this field, future directions include:

(1) Exploring new *p*-type oxide materials: Currently, no existing materials meet the expectations for *p*-type oxide transistors as counterparts to IGZO TFTs. Therefore, significant effort is needed to search for and design new *p*-type oxide materials with high mobility and wide bandgaps. It is crucial that these materials are thermodynamically stable and feasible for fabrication. Recently, tellurium oxide has emerged as a potential candidate for *p*-type oxide; however, further research is necessary to fully understand this material and unveil its potential for *p*-type oxide applications.

(2) Innovating low-temperature material growth techniques: Although we have identified potential candidates for *p*-type oxides based on theoretical predictions and bulk material studies, achieving high-quality thin-film growth at low-temperature processing remains challenging. For instance, while Cu₂O exhibits high mobility in bulk materials, fabricating high-mobility Cu₂O thin films using low-temperature deposition is a significant challenge.

(3) Researching other material systems suitable for low-temperature processing with excellent electrical properties and uniformity to integrate with *n*-type oxide devices.

7.2 Low-Temperature Processed and Ultra-Wide-Bandgap Oxide β -Ga₂O₃ TFTs

Exploring novel ultra-widegap oxide materials with a bandgap exceeding that of the currently commercialized a-IGZO holds significant promise for reducing TFT off-current, lowering power consumption, and enabling diverse applications. Ga₂O₃ has emerged as a promising semiconductor material for microelectronics, with several successful demonstrations of high-performance β -Ga₂O₃ transistors already achieved. However, developing an ultra-wide bandgap Ga₂O₃ semiconductor using a low-temperature process remains highly challenging yet promising for various practical applications.

Low-temperature processed Ga₂O₃ has emerged as the next breakthrough channel material in TFT technology, offering substantial reductions in off-current and power consumption for displays and wearable electronics applications. Ga₂O₃ TFTs also facilitate the integration of power devices into large-scale flexible electronic systems, develop robust electronics for harsh environments, and show potential for solar-blind deep-ultraviolet photodetectors. Part II of this dissertation delves into β -Ga₂O₃ as a new oxide channel material for low-temperature processed, high-mobility, and wide-bandgap oxide TFTs. I proposed a pressure-assisted liquid-metal printing technique that enables low-temperature crystallization of β -Ga₂O₃, resulting in high-performance and wide bandgap *n*-channel oxide TFTs with a high saturation mobility of approximately $\sim 11 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

The next phase of this research involves investigating the fabrication of semiconducting polycrystalline/amorphous β -Ga₂O₃ using conventional thin-film deposition methods such as sputtering and atomic layer deposition (ALD) to facilitate the transition from laboratory-scale to

large-scale manufacturing. Furthermore, it is imperative to enhance the performance of β -Ga₂O₃ devices and evaluate their device characteristic in scaled devices and other potential applications.

7.3 Oxide TFTs for Non-Traditional Computing Devices

Embarking on research into novel computing paradigms beyond traditional digital computers is crucial for developing future energy-efficient and sustainable computing systems. Oxide devices hold promise as fundamental building blocks for next-generation analog neuromorphic computing systems. Part III of this dissertation delves into oxide semiconductor devices as emerging computing units for non-traditional computing platforms. We developed low-temperature processed ambipolar SnO-based TFTs to showcase dynamic reconfigurable excitatory and inhibitory synaptic responses in a single synaptic device, mimicking complex biological functions in emerging neuromorphic hardware. Additionally, we introduced a novel gate-tunable memristor, termed a memtransistor, leveraging non-layer 2D oxide semiconductor material, specifically SnO₂. The memtransistor integrates memristor and transistor functionalities, propelling the advancement of next-generation neuromorphic computing technology. Our experiments successfully demonstrated that the gate-tunable synaptic device dynamically modulates analog switching behavior with optimized linearity and a larger conductance change ratio, further enhancing recognition accuracy for pattern recognition tasks.

Throughout this thesis, research has been conducted at both the material and device levels to pioneer analog neuromorphic technology with innovative operational principles. However, challenges persist in achieving desired device performance, analog switching properties, scalability, and reliable production of devices and systems that align with commercially available processors and hardware standards. It is crucial to note that, as of now, no clear winner among neuromorphic materials and devices has been identified to replace CMOS-based electronics for analog neuromorphic systems. Collaborative efforts between academia and industry partners are

essential to identify the materials and devices necessary for future commercialized neuromorphic technology. Addressing the challenges of integrating neuromorphic devices into commercial IC technologies necessitates comprehensive investigations, including device optimization, system-level design, hardware-software codesign, and algorithm-architectural studies.