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A sub-nW 2.4 GHz Transmitter for Low Data-Rate Sensing Applications

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Abstract

This paper presents the design of a narrowband transmitter and antenna system that achieves an average power consumption of 78 pW when operating at a duty-cycled data rate of 1 bps. Fabricated in a 0.18 μm CMOS process, the transmitter employs a direct-RF power oscillator topology where a loop antenna acts as a both a radiative and resonant element. The low-complexity single-stage architecture, in combination with aggressive power gating techniques and sizing optimizations, limited the standby power of the transmitter to only 39.7 pW at 0.8 V. Supporting both OOK and FSK modulations at 2.4 GHz, the transmitter consumed as low as 38 pJ/bit at an active-mode data rate of 5 Mbps. The loop antenna and integrated diodes were also used as part of a wireless power transfer receiver in order to kick-start the system power supply during energy harvesting operation.

Index Terms

Body-sensor networks; energy harvesting; low power electronics; power amplifiers; radio frequency integrated circuits; voltage-controlled oscillators; zero-power electronics

I. Introduction

The ongoing miniaturization of electronics, as modeled by Bell's law [1], has taken solid-state computing platforms from stationary room-sized mainframes to portable platforms such as laptops, smartphones, and smart watches. Although the power consumption and computational performance of such electronic devices have also scaled with Moore's law, the battery technology necessary to power portable devices has not scaled nearly as rapidly. Thus, as Bell's law continues to march on and device sizes continue to scale, it will become necessary to create advances in energy harvesting and near-zero-power electronics in order to overcome limited battery capacities to push into the next generation of ubiquitous sensors and "internet of everything" devices.

Many emerging sensing applications have underlying physical properties that do not vary rapidly with time. For example, sensing of temperature, metabolites, and air quality are but a few examples of applications where sensing front-ends do not require rapid sampling, and therefore can be aggressively duty-cycled into ultra-low-power sleep states. If the majority of the active elements in such a sensing system can follow this duty-cycling paradigm, then the *average* power consumption of the system is not set primarily by the active-mode power, but rather from a combination of active-mode and standby-mode power, with a large percentage coming from standby-mode during deeply duty-cycled operation. Thus, minimizing the standby-mode power is the key to enabling near-zero-power sensing nodes at ultra-low data rates.

In general, miniaturized sensing systems communicate their measured information wirelessly over a short distance (e.g., often only a few meters) in order to minimize the active-mode power of the constituent Radio Frequency (RF) Power Amplifier (PA). Thus, local base stations are typically employed in locations where energy is more abundant - a smartphone within a Body-Area Network (BAN), for example. However, even under low path-loss constraints, RF circuits still often dominate the power consumption of sensor nodes [2], [3]. Thus, there is considerable interest in minimizing the power consumption of RF circuits in such sensing nodes. Many recent publications in the area of energy-efficient RF circuits have described receivers, transmitters, and transceivers with excellent RF performance at efficiencies down to tens-to-hundreds of picojoules per bit [4]-[6]. However, such architectures are typically demonstrated and optimized for efficient performance at data rates exceeding 100 kbps. At such average data rates, leakage and standby power are not critical, and therefore not aggressively optimized. As a result, the average power of such radios do not necessarily scale well down to ultra-low data rates.

In order to enable next generation sensor nodes with near-zero-power for energy-autonomous operation in combination with energy harvesting, this paper presents a 2.4 GHz transmitter that is specifically optimized for standby power in the picowatt regime [7]. To achieve this, a low-complexity, single-stage direct-RF architecture is employed, featuring significant power gating and sizing optimizations for minimized leakage power.

To validate the design, the transmitter is integrated into a system that harvests energy from the Endocochlear Potential (EP) - an electrochemical gradient found naturally in the inner-

ear of mammals - which can only sustain energy extraction of approximately 1 nW [8], [9]. A figure of the EP harvesting system is shown in Fig. 1. Since the EP voltage is low (typically between 70–100 mV), a boost converter is used to process the energy up to a higher voltage (typically between 0.8–1.0 V), which is directly dumped onto capacitor C_{DD}. As more energy is extracted from the cochlea, it is continually buffered onto C_{DD}, forcing its voltage, V_{DD}, and as a result its stored energy, to rise. When sufficient energy has been stored on C_{DD}, the 2.4 GHz radio is enabled to quickly transmit a packet, then return to an ultra-low-power standby mode.

In this system, the boost converter requires 544 pW of quiescent power [10]; leaving approximately 250 pW of transmitter power budget after taking into account the overhead of other peripheral circuits and adding some power budget safety margin. Given the extreme power budget limit, the transmitter is designed and optimized to operate over short transmission distances (1 m) in order to limit the requisite output power. In addition, the transmitter is deeply duty-cycled, for example down to a duty-ratio of 0.00002% by transmitting 64-bit packets once every 80 seconds, with an instantaneous data rate of 5 Mbps, for an average data rate of ≈1 bps in this example (though this can be programmable).

Since the EP in this case is too low to directly start-up CMOS electronics (in particular, the boost converter control circuitry), the transmitter's antenna is shared with a kick-start rectifier [11], used to initialize the charge on C_{DD} at system start-up with little overhead. As an implanted system, kick-starting is performed by placing an external antenna, driven by an RF source, near the surface of the skin just above the implant for transcutaneous wireless energy delivery, similar to traditional inductively-coupled or mid-field powered systems [12], [13].

This paper describe the details of the transmitter, antenna, and kick-start rectifier, while details of the biology and overall system operation can be found in [8], and details of the boost converter can be found in [10].

II. Transmitter Architecture

A. Motivation and Prior Work

The application use-case for this design is to use the endocochlear potential as an energy source to autonomously power a wireless implant. In this case it is not desired (or required) to have a semi-permanent external wireless source powering and interrogating the implant, as is typically done for implantable systems such as cochlear implants. Instead, information can be transmitted directly from the implant to an external device approximately one meter away (e.g., a cell phone or smart watch). This setup permits the design of a functionally autonomous system, with zero patient involvement required (other than a wireless kick-start for system initialization). In addition, it exploits the benefits of a body-area network, where communication complexity is pushed away from the energy-starved implant and towards the energy-rich base station platform.

Since the transmitter will be deeply duty-cycled, its average power consumption is not determined solely by its active or leakage performance, but by a combination of both [14]. More precisely, the average power consumption can be predicted by Equation 1.

$$P_{TX,avg} = P_{TX,leak} + \frac{E_b N}{T_{pkt,int}} \quad (1)$$

Here, $P_{TX,leak}$ is the transmitter leakage power, E_b is the energy required to transmit a single bit, N is the number of bits per packet (programmable from 8–128 bits based on a binary counter), and $T_{pkt,int}$ is the time interval between packets (programmable from 40–360 s based on a counter that is driven by the 12.8 Hz on-chip oscillator found in the boost converter control circuitry [10]). Based on this equation, the transmitter must not only have extremely low leakage power, it also must be very energy efficient during active-mode in order to achieve the necessary overall power goal, otherwise the effective bit rate (i.e. $N/T_{pkt,int}$) will be forced to be extremely low.

There are many examples of very energy efficient transmitter designs in the literature. Previous narrowband transmitters have attained energy efficiencies on the order of 140–2900 pJ/bit for output power ranging from −16 dBm to 0 dBm at instantaneous data rates under 5 Mbps [4], [15]-[20]. However, none of these systems are optimized for ultra-low standby power. On the other hand, narrowband work in references [21], [22] were indeed optimized for low leakage power, consuming 675 pW and 3.3 nW in standby power modes, respectively. However, neither of these results meet the 250 pW power budget required in this work, particularly when their actives transmission modes are taken into account. For example, the two separate chips require 29 nJ/bit and 4.7 nJ/bit, resulting in an average powers of 46 nW and 11 nW, respectively.[1]

Pulse-based Ultra-Wideband (UWB) radios, which communicate using very short duration impulses at RF, also offer promising results in terms of energy efficiency. In particular, the energy efficiency of UWB transmitters using non-coherent signaling can be much lower than their narrowband counterparts, due in part to relaxed frequency tolerances and internationally regulated output power limits [23]-[28]. Although potentially appealing, such efficiency is generally achieved not through active-mode power reduction, but instead through increased instantaneous data rates. In fact, many UWB transmitter implementations require multiple RF stages (even “all-digital” implementations, which often use many cascaded RF inverters as a PA), all of which generally require low-V_t transistors in order to switch sufficiently fast to generate power in the 3.1–10.6 GHz UWB bands. Thus, the high active-mode power, distributed low-V_t blocks can be difficult to effectively power gate down to the requisite levels in this particular application, especially if the I_{on}/I_{off} ratio of power gating switches is limited. Additionally, the high frequencies employed in standard UWB bands suffer from increased losses when transmitting through biological tissue, due primarily to larger conductivity at higher frequencies [29], which would reduce the overall

[1]This is calculated using each radio’s nominal instantaneous data rate scaled to 1 bps.

system radiation efficiency compared to lower-frequency ISM bands, and would thereby require increased active-mode power, increasing the difficulty of effective power gating.

B. Architecture Overview

For the reasons outlined in the preceding section, it is necessary to reduce the overall transmitter complexity by limiting the number of RF blocks while pushing all possible communication complexity to the energy-abundant external base station receiver. Taking the simplified architecture concept to a logical extreme, the transmitter presented in this work radiates information through the use of a direct-RF Power Oscillator (PO) design, inspired by the early days of single-transistor radios and more recent work presented in [15]. A simplified block diagram of the transmitter is shown in Fig. 2.

The transmitter generates RF at a frequency of 2.4 GHz as a compromise between tissue losses, antenna efficiency, and circuit power consumption. A more thorough discussion of this trade-off is found in Section III. A loop antenna is chosen as the radiative element, as it offers sufficient radiation conversion efficiency, has a high quality factor, and is naturally well suited to receive wireless power for system initialization. Due to anatomical size constraints, the physical size of the antenna will be much smaller than its radiating wavelength, resulting in an electrically small design. An electrically small magnetic loop antenna can be modeled as an inductor in series with a resistor, which is well suited to serve as part of the resonant network of the power oscillator. The oscillator itself performs automatic impedance matching, resulting in a very low-complexity, low-area, and energy efficient design. Data modulation can be achieved by turning on or off the entire oscillator for On-Off Keying (OOK) modulation, or the resonant capacitors can be dynamically switched for Frequency-Shift Keying (FSK) modulation.

III. Antenna Design

The design of antennas for implantable applications usually involves a trade-off between radiation efficiency (which increases with antenna size and/or carrier frequency as the wavelength approaches the physical antenna size) and tissue losses (which increase with frequency as the conductivity of tissue increases). In this application, the antenna size is limited to a few millimeters in diameter due to anatomical constraints. At 5 GHz and below, a loop antenna of this size would be considered electrically small, and can thus be modeling as an inductor, L_{ANT}, in series with a resistor, R_{ANT}. Equations predicting the performance of the antenna can be found the in Appendix.

Table I shows simulated results for radiation efficiency, quality factor, and inductance of a representative 3×4 mm^2 antenna in free-space, using 0.2 mm, 2-oz copper traces on a 1.6 mm FR-4 Printed Circuit Board (PCB) substrate in air at various Industrial, Scientific, and Medical (ISM) band frequencies. For completeness, the same antenna is additionally simulated in a realistic implanted environment using both FR-4 and Rogers substrates, while coated with 0.1 mm of bio-compatible parylene and being surrounded on the underside by bone and brain, and on the top side by 3 mm of fat tissue and 2 mm of skin. Antenna electromagnetic simulations were performed in IE3D, a fully 3D method-of-moments simulator [30].

Although the Medical Implant Communication Service (MICS) specification at 402–405 MHz is specifically designated for medical implant communications, the radiation efficiencies are simply too low to be useful for implants with limited antenna sizes. To put this in perspective, a transmitter consuming 1 mW of power could, at its theoretically optimal point, only radiate −44 dBm in air or −64 dBm in an implanted environment at 400 MHz. In contrast, the same antenna operating at 2.4 GHz would ideally radiate −21 dBm in air or −33 dBm in an implanted environment. While operating at an even higher frequencies may be beneficial for many applications with small implanted antennas, the non-inductive antenna reactance may require large (or small and lossy) inductive-based tuning circuits. Additionally, because the loss resistances of the antenna are higher, such an approach may preclude the design of a single-stage power oscillator architecture, as the oscillator load would be substantial, thereby requiring either a separate driver or significantly more static power consumption. On the other hand, Table I indicates that Q peaks at 900 MHz, not 2.4 GHz. However, extremely high Q is not necessarily desirable in this case: a very high Q implies that radiation efficiency is low. What we desire here is finite, positive Q, with maximum radiation efficiency, and a positive reactance for ease of on-chip matching. As a result of these considerations, a frequency of 2.4 GHz was chosen to comply with the simplified architecture philosophy and extreme power gating possibilities. Additionally, this provides an opportunity to communicate in the uncrowded Medical Body-Area Network (MBAN) band at 2360–2395 MHz recently allocated by the United States Federal Communications Commission (FCC) and supported by the recently-passed IEEE 802.15.6 standard [31].

In terms of sizing optimization, the antenna has restrictions not only from anatomy, but also from a resonant frequency perspective. It is known that the radiation resistance of an electrically-small loop antenna increases with the square of the area of the antenna (see Equation 4 in the Appendix), while the loss resistance only increases linearly with area. It would then be beneficial to size the antenna as large as possible given anatomical constraints for maximum radiation efficiency. However, increasing the antenna size also increases its inductance (Equation 2). Since the antenna-chip interface contains fixed parasitic capacitance (bond pads, Electrostatic Discharge (ESD) protection diodes, etc.), the maximum resonant frequency will in fact decrease with increasing antenna size. Figure 3 presents electromagnetic simulation of a rectangular antenna where the antenna height is swept from 2 mm to 7 mm, for a fixed width of 3 mm at 2.45 GHz in air with an FR-4 substrate. The maximum center frequency was calculated based on the simulated inductance, and a layout-extracted parasitic capacitance of 300 fF. As predicted, radiation efficiency does indeed increase with antenna size. However, the maximum parasitic-limited resonant frequency decreases; 2.4GHz resonance is not achievable beyond an antenna height of 4.5 mm. This places a functional upper bound on the antenna size given the requirement to radiate in the 2.4 GHz ISM band. Based on the preceding analysis, an antenna size of 3×4 mm^2 with an inductance of 9.5 nH in air is chosen for this design in order to maximize radiation efficiency given both the anatomical and resonant frequency size constraints.

In the above analysis, the loop antenna was optimized for maximum radiation efficiency. However, it still must also act as a receiver of wireless power for system initialization,

though since kick-starting only happens once, its efficiency is not extremely important. Interestingly, the simulated wireless power transfer gain through 13 mm of tissue was found to be −15.5 dB at an optimal frequency of 1.45 GHz, which is in line with previous work in this area [13]. At 2.4 GHz, the gain falls to −17.5 dB, an acceptable trade-off for not requiring re-tuning.

IV. Circuit Design

A transistor-level schematic of the transmitter and wireless energy receiver architecture is shown in Fig. 4. The following subsections describe the system operation, including details of each individual block.

A. Power Management

The transmitter receives its supply voltage, V_{DD}, from an on-chip boost converter whose details are discussed in [10]. The value of V_{DD} is set by a balance between the amount of energy extracted from the EP and the power of the load circuits. Though no explicit regulation is performed in this initial prototype, the load circuit power consumption increases with V_{DD}, thereby producing a quasi-regulation effect. Future revisions could explicitly introduce feedback regulation by sensing V_{DD} and dynamically modulating the activation frequency, output power, or other load circuit characteristics. During clinical measurements of this prototype, V_{DD} has been shown to vary between 0.8–1.0V [8], which is where the transmitter was optimized to operate. Diode-clamp circuits are employed to ensure V_{DD} does not exceed process safety standards. The boost converter also supplies a boosted power supply voltage, V_{PUMP}, generated by an on-chip charge-pump. Ideally, $V_{PUMP} = 2V_{DD}$, though in practice V_{PUMP} is slightly lower than this as current is drawn from this supply. The dynamics of V_{PUMP} start-up enable a simple Power-On-Reset (POR) scheme, which is discussed, along with the wireless kick-start paradigm, in Section IV-D.

B. Power Oscillator

The core of the transmitter is the power-oscillator, comprising the cross-coupled pair of transistors (M1 and M2), footer power-gating/biasing transistors Mf[5:0], a capacitive tuning DAC (comprising eight parallel instances of transistors Ms 1–3), and the loop antenna. OOK modulation is achieved by dynamically activating footer transistors Mf[5:0], thereby turning on or off the oscillator at the OOK modulation frequency. Similarly, FSK modulation is achieved by dynamically re-configuring the 8-bit capacitive DAC between different center frequency settings. The power-oscillator is biased via a center-tap in the loop antenna that is directly connected to the system power supply, V_{DD}, through an on-board via that connects to a V_{DD} plane below (as shown in Fig. 1).

Since the transmitter draws significant amounts of active-mode power, it is not suited to operate from the on-chip decoupled charge pump supply, V_{PUMP}. As a result, the cross-coupled devices M1 and M2 are implemented using low-Vt devices in order to reduce parasitic drain capacitance by 10X compared to high-V_t devices sized for equivalent on-conduction (from 2.8 pF to 280 fF) at V_{DD}. The reduced capacitance permits a significantly larger antenna as discussed in Section III than if high-V_t devices were instead used. During

OOK modulation, the capacitance at the source terminals of the cross-coupled M1 and M2 devices only switches at the data rate frequency and not at RF. Consequently, the power oscillator can be biased using high-V_t NMOS transistors without any recourse to operational speed. This permits standby-mode leakage currents that are 33X lower for equivalent on-conduction. To further reduce active energy consumed per transmitted bit, the high-V_t NMOS devices are enabled by full-swing signals operating at V_{PUMP}, which decreases the associated gate capacitance (and therefore active OOK switching energy) by 28X for equivalent on-conduction. The biasing circuit specifically consists of six binary weighted devices (Mf[5:0]) with W/L ratios ranging from 16μm/0.35μm to 0.5μm/0.35μm in order to control the amount of on-current for output amplitude swing control, or dynamic pulse shaping in a future implementation. To reiterate, the biasing transistor gates are not driven by an intermediate voltage as set by a current reference, but rather they are driven by full-swing digital signals at V_{PUMP} in order to maximize I_{on} to I_{off} ratios.

Resonant tuning of the antenna inductance within the power oscillator is implemented primarily using a 5-bit binary-weighted Metal-Insulator-Metal (MIM) capacitive DAC, totaling approximately 300 fF. The DAC is dynamically activated using differential switches, which according to the simulation result shown in Fig. 5, reduces the parasitic switch capacitance by 2X for a capacitor quality factor of approximately 50 (or up to 3X for lower quality factors). A separate 3-bit sub-ranging DAC is implemented using custom-designed Metal-Oxide-Metal (MOM) capacitors, where a 3 fF unit-sized MOM cap is placed in series between the main DAC and sub-DAC. Although parasitics can be larger than the sub-DAC unit capacitors, the sub-DAC can still be employed to provide fine frequency control, with 0.25 fF switchable at the least significant bit (LSB) using differential smaller-than unit 0.6 fF MOM capacitors in series with the 3 fF splitting capacitors [32]. The sub-DAC is specifically used to achieve minimal bandwidth FSK modulation. For example, Minimum-Shift Keying (MSK), which uses the theoretically smallest amount of FSK bandwidth for a given data rate, requires approximately 0.5 fF of switchable capacitance at 2.4 GHz when communicating at an instantaneous data rate of 5 Mbps. Although non-linear, the sub-DAC is monotonic, which is sufficient for FSK/MSK purposes. Including the DAC, the resonant circuit achieves a tuning range from 2.1–2.6 GHz, simulated in Cadence using extracted antenna s-parameters from IE3D and extracted circuit models from layout.

C. Ring Oscillator, Modulator, and Control

For this particular prototype, transmitted data comes from off-chip (for example, from a digital sensor interface) or on-chip memory. The modulating frequency that clocks-in this data is generated by an on-chip ring oscillator, shown in Fig. 6. The oscillator is a five-stage current-starved inverter-based design. To minimize active CV^2 switching power, the inverter devices use low-V_t transistors. However, overall current is dictated by 6-bits of NMOS and PMOS degeneration devices, separated into two groups of control: *coarse* and *fine*. Since generating an on-chip current reference would consume excessive static power, current starving devices are instead sized to operate as resistive elements (i.e. in the triode regime) when driven by full-swing input signals (i.e. at V_{DD}). For manufacturing and operational reliability, the ring oscillator is designed to operate from 100 kHz to 10 MHz across process corners and V_{DD} variation. To achieve the high-end frequencies in slow process corners,

low-V_t devices are used for the *coarse*[2] control signal. To achieve low-end frequencies at fast process corners, two-bits of capacitive tuning are included in each inverter delay element. To minimize active CV^2 energy consumption, these extra capacitors should not be activated unless it is necessary to achieve the desired operational frequency. During standby mode, the oscillator is put into a low-leakage state by gating the output and gating all current starving elements.

The data modulator consists of digital logic that is manually designed primarily using low-V_t -based standard cells in order to minimize $CV^2 f$ switching power losses that occur at the data modulation frequency. A schematic of the main data path is shown in Fig. 7. It accepts a digital clock from the ring oscillator (labeled as *osc* in Fig. 7) for simple fully-integrated testing, or can accept externally driven serial data (labeled as *data* in Fig. 7) for benchtop testing or eventual system integration with a separate sensor. Depending on if OOK or FSK modulation modes are enabled (via *enOOK* and *enFSK* signals, respectively), either the power-oscillator biasing transistors (Mf[5:0] in Fig. 4), or the capacitive DAC transistors (Ms 1–3) are activated, respectively. FSK is achieved by switching between two different programming codes (i.e., frequencies), set by *FSK*0[7 : 0] and *FSK*1[7 : 0]. A inverter-transmission gate circuit [6] is used to create phase-matched differential signals to drive a multiplexor selecting one of *FSK*0 or *FSK*1 at a time.

To decrease the standby current of the power oscillator biasing devices (Mf[5:0]) for a given on-current, the modulator output signals are driven from the V_{PUMP} supply. A similar effect is arranged for the capacitive DAC to increase its quality factor. Level-conversion to the higher voltage is achieved using a standard cross-coupled level shifter circuit. Since the output is single-ended, a dummy driver load is installed for edge transition matching purposes. The entire modulator is power gated by PMOS devices MP1 and MP2 whose inputs are driven by *enPGATE* - a signal driven from the V_{PUMP} supply. Power gating saves upwards of 4,000X in leakage power from the V_{DD} supply (MP1), and 20X from the V_{PUMP} supply (MP2). The savings are larger from MP1 since the device enters the super cut-off regime upon application of V_{PUMP} to its gate. The size of power gating devices are annotated in Fig. 7, with MP1 and MP2 having on-resistances of approximately 1.8$k\Omega$ and 600Ω at 15μA and 35μA respectively. The area overhead of power gating here is minimal, occupying the area of approximately six NAND gates in this design.

The output of the ring oscillator also clocks a counter and comparator that are used to set the number of bits transmitted in a single packet. The counter, whose schematic is shown in Fig. 8, uses a ripple-carry frequency divider for the first two registers. The final two counter stages use a synchronous design that is pre-scaled to reduce the critical path, enabling sufficiently fast operation at low voltages using low-leakage devices [33], [34]. Although the counter itself is a 7-bit design, only the final 5-bits are applied to the comparator, as the utility of transmitting 1–4-bit packets is limited. Furthermore, rather than designing a full 5-bit adder to count to arbitrary 5-bit packet lengths, a simple 5-bit power-of-two comparator is used, enabling counting intervals ranging between 8 and 128 in powers of two only. This reduces the gate count by 3.6X, resulting in a low-complexity, low-leakage design. The counter is power gated by a single PMOS device (size: 6μm/0.18μm, or an approximate overhead of 3%), nominally saving 18X in standby power. Since the circuit operates using

the V_{DD} supply, it is possible to gate the PMOS device with the V_{PUMP} supply, forcing the transistor into super cut-off, and saving an additional 2.6X in leakage, or 48X in total. The on-resistance of the PMOS is approximately $1.2k\Omega$ at $10\mu A$.

A start-up logic block is designed to receive an activation signal, nominally generated by the boost converter, which disables the appropriate power gating devices and initializes the ring oscillator and modulator. Since the start-up block itself cannot be power gated, it is designed using almost exclusively high-V_t devices for minimal leakage power consumption.

D. Wireless Energy Receiver and Power-on Reset

The wireless energy receiver circuit design is already included in Fig. 4. In fact, since the antenna can be modeled as an inductor that has a center tap, creating a full bridge rectifier is as simple as placing two diodes between the two ends of the inductor, connected to ground (diodes D1 and D2 in Fig. 4). Interestingly, these diodes are in fact already required for ESD protection. Thus, adding wireless power transfer functionality does not add any additional complexity and, more importantly, does not add any additional parasitic capacitance on the sensitive antenna interface nodes. As described in Section III, reduced parasitics on these nodes permit the design of a larger, more efficient antenna given a resonant frequency requirement of 2.4 GHz. Naturally, diodes D1 and D2 only protect the ground supply; additional diodes are required to protect the positive (i.e. V_{DD}) supply. However, since the antenna is center-tapped and biased at V_{DD}, the power oscillator output RF signals naturally swing symmetrically above and below V_{DD}. If only a single set of diodes were placed to protect V_{DD}, these RF voltage swings would be limited to a single diode drop. The solution here is to instead stack three diodes in series.

Following wireless energy delivery for the purpose of initializing V_{DD}, it is of critical importance to ensure the chip is reset to a known-good state. If, for example, the power oscillator gating switches were somehow enabled after the external wireless energy source was removed, the on-current would be large enough to catastrophically collapse the V_{DD} supply. To avoid such an event, a reliable POR is required. Fortunately, creating a POR signal can be achieved in a very low-complexity, low-leakage manner. Since the charge pump supply, V_{PUMP}, requires 600 ms to initialize following V_{DD} initialization [9], [10], a simple inverter structure can be used to generate the requisite POR signal, as illustrated in Fig. 4. Specifically, an inverter powered from the V_{DD} supply with V_{PUMP} at the input will nominally output a logic high value until V_{PUMP} crosses the inverter threshold (nominally several hundred milliseconds after V_{DD} initialization). The inverter is designed with high-V_t transistors, since there is no opportunity to power-gate the initialization logic. The leakage impact of this inverter is negligible, however, since after the reset signal has been deactivated, the leakage of the inverter is set by the PMOS device which in this case is biased in super cut-off due to the presence of V_{PUMP} as its input.

While the circuit is implanted it is not possible to directly measure kick-start and POR success with immediate feedback. Instead, successful start-up can be confirmed when the radio transmits its first packet.

V. Measurement Results

The transmitter was fabricated in a 0.18 μm process and occupies a core area of 0.035 mm^2. The overall die size is $2.4 \times 2.4 mm^2$ including the DC/DC converter, as shown in Fig. 9; the design is thus severely pad-limited (future revisions can reduce the pad count substantially by providing programming, testing, and calibration functionality through a scan-chain). To minimize packaging parasitics and size, the chip was directly wire-bonded to a PCB using chip-on-board packaging technology. Exposed copper pads on the PCB were finished with 2 μm of soft gold over 6.4 μm of nickel for wirebonding compatibility. The chip was directly bonded to an on-board 3×4 mm^2 antenna. A photograph of the board is shown in Fig. 10. Table II summarizes the transmitter results.

A. RF Performance

Since the antenna is part of the resonant network of the power oscillator, it was not possible to directly test or probe the output power of the transmitter. Instead, wireless testing was performed, unless otherwise specified, by placing the center conductor of a 2.4 GHz, λ/4 whip antenna approximately 5 mm from the loop antenna. Testing the radio transmitter with this setup revealed that the maximum wirelessly received power was −21.9 dBm when operating with V_{DD} = 1.0 V and the maximum current setting in the power oscillator. Figure 11 reveals measurements for additional supply voltages across all power oscillator tuning bits. When placing the whip antenna at a distance of 1 m from the loop antenna, the maximum wirelessly received power was measured to be approximately −60 dBm. These measurements suggest that the maximum output power of the transmitter is approximately −20 dBm. Figure 12 shows the consumed power of the transmitter when in active mode under the same conditions. The power oscillator achieved a phase noise of −105 dBc/Hz at 1 MHz offset.

Figure 13a shows measured OOK spectral results modulated by random externally-derived bits at data rates of 1 Mbps and 10 Mbps. Achieved −3 dB bandwidths and energy per bits for 1 Mbps and 10 Mbps data rates are 620 kHz and 2 MHz, and 191 pJ/bit and 19 pJ/bit, respectively. No explicit filtering is performed here; the attenuated side-lobes may be attributed to antenna filtering and oscillator start-up transient effects. Interestingly, there is no apparent feed-through component found in the spectrum, which is typical for non-phase scrambled OOK transmitters. This implies that the PO start-up is not coherent, and has a certain amount of randomness in its phase. Fortunately, this results in a more desirable spectrum, as OOK is normally use in non-coherent communication systems anyways. Figure 13b shows measured spectra using FSK and near-MSK modulation. The power oscillator achieves a frequency tuning range from 2.1 GHz to 2.54 GHz across the 8-bit capacitive DAC when resonating with the on-board 3×4 mm^2 inductive loop antenna, matching simulated results well.

The transmitter is capable of starting-up in 180 ns, as shown in Fig. 14, enabling rapid and aggressive duty-cycling into low-power sleep states. The start-up time is dictated primarily by the slow, high-V_t logic in the start-up block, which in simulations requires approximately 120 ns to propagate the initialization signal through a D flip-flop and a small number of

logic gates. Note that during this period the PO is not activated, and the overall transmitter power consumption is still dominated by leakage.

B. Ring Oscillator

By tuning the current starving and capacitive loading bits, the ring oscillator was measured to generate clock frequencies from below 100 kHz to at least 100 MHz while consuming between 14 nW and 19 μW across supply voltages ranging from 0.7 V to 1.0 V. This large amount of configurability was required to be able to generate the requisite frequencies across severe PVT variation. To show the effects of current starving versus capacitive tuning, the measured energy required per output cycle, plotted versus achievable frequencies, is illustrated Fig. 15. Here, it is clear to see four distinct zones of energy consumption - a result of the four capacitive loading options, $enC[1:0]$. Although the ring oscillator consumes a small fraction of the total transmitter active energy budget, its energy efficiency is clearly maximized at the lowest capacitive loading setting.

C. Power Consumption

By implementing a low-complexity architecture together with leakage-aware design considerations, the transmitter standby power consumption was measured to be 39.7 pW at a supply voltage of 0.8 V. Table III summarizes the measured transmitter standby power at several different voltages and compares the results to simulated results at 0.8 V. The simulated results matched the measured results with a reasonable amount of accuracy, landing somewhere in between the simulated results in the TT and FF corners (with the exception of the digital supply, which resulted in higher power than the FF corner, though this was a minor component overall). The leakage power from the V_{PUMP} and ring oscillator supplies are the largest since they were not power gated by a transistor in super cut-off (it was simply not possible for V_{PUMP}, while the ring oscillator was designed before the charge pump and not later modified during the design cycle). Total transmitter standby power measured at various supply voltages are shown in Fig. 16. Low-current measurements were performed using a Keithley 6430 sourcemeter together with low-leakage tri-axial cables.

To minimize the energy required to transmit a bit of information during active mode, it is worthwhile to operate the PO at an intermediate back-off point. For example, at V_{DD} = 0.8 V, a data rate of 5 Mbps, and a measured output power of at least −26 dBm or −29 dBm, the transmitter consumed 374 μW or 191 μW for FSK and OOK modulations, respectively. This results in a energy efficiency of 75 pJ/bit or 38 pJ/bit for FSK and OOK, respectively. A power breakdown of these two operating points is shown in Table IV.

Combining this active-mode data point in OOK mode together with leakage power as suggested by Equation 1, results in the total average transmitter power consumption of $P_{TX,avg}$ = 78 pW at an average data rate of 1 bps. In fact, the transmitter can achieve average data rates up to 5X higher while maintaining an average power consumption below the 250 pW power budget specified by the endocochlear potential harvesting applications. Table V summarizes the chip results compared to existing state-of-the-art.

VI. Conclusions

This paper has presented the design of a radio transmitter that was optimized for aggressive duty-cycling between an energy-efficient active mode and an ultra-low-power standby mode for low data rate applications. By employing aggressive power gating, sizing, and architectural strategies, the transmitter consumed 39.7 pW in standby mode. Integrated with an on-board antenna, and employing a direct-RF power oscillator architecture with automatic impedance matching, the transmitter required 38 pJ to transmit a single bit of information. Operating at a duty ratio of 0.00002% and transmitting an average of 1 bps, the transmitter achieved an average power consumption of 78 pW. The transmitter was then used within an energy harvesting platform that extracted energy from the endocochlear potential within the inner-ear, demonstrated the feasibility of sub-nW radio transmitter designs.

Acknowledgments

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Appendix - Antenna Calculations

A circular loop antenna's inductance can be approximated by Equation 2.

$$L_{ANT}=\frac{\mu}{2}D[\ln(8D/d)-2] \quad (2)$$

Here, μ is the permeability of the surrounding environment, *D* is the diameter of the loop, and *d* is the diameter of the constituent wire [35].

The antenna's series resistance, R_{ANT}, is made up of a radiation resistance, R_{RAD}, and a loss resistance, R_{LOSS}-The radiation efficiency, η_{RAD}, can be calculated using:

$$\eta_{RAD}=\frac{R_{RAD}}{R_{RAD}+R_{LOSS}}. \quad (3)$$

The radiation resistance can be approximated by:

$$R_{RAD}=\sqrt{\mu\varepsilon}\frac{8\pi^3}{3}\left(\frac{A}{\lambda^2}\right)^2. \quad (4)$$

Here, ε is permittivity, *A* is the antenna's area in units of m^2, and λ is the operational wavelength. The loss resistor, R_{LOSS} can be calculated in the usual way from metallic conduction properties, taking into account the skin effect. The skin depth, δ_s, is given by Equation 5, and the associated loss resistance, R_{LOSS}, is given by Equation 6.

$$\delta_s=\sqrt{\frac{1}{\pi f\mu\sigma}} \quad (5)$$

$$R_{LOSS} = \frac{d_L}{\sigma d_W \delta_s} \quad (6)$$

Here, σ is the metallic conductance, while d_L and d_W are the length and width of the PCB trace (an appropriate approximation for flat PCB traces).

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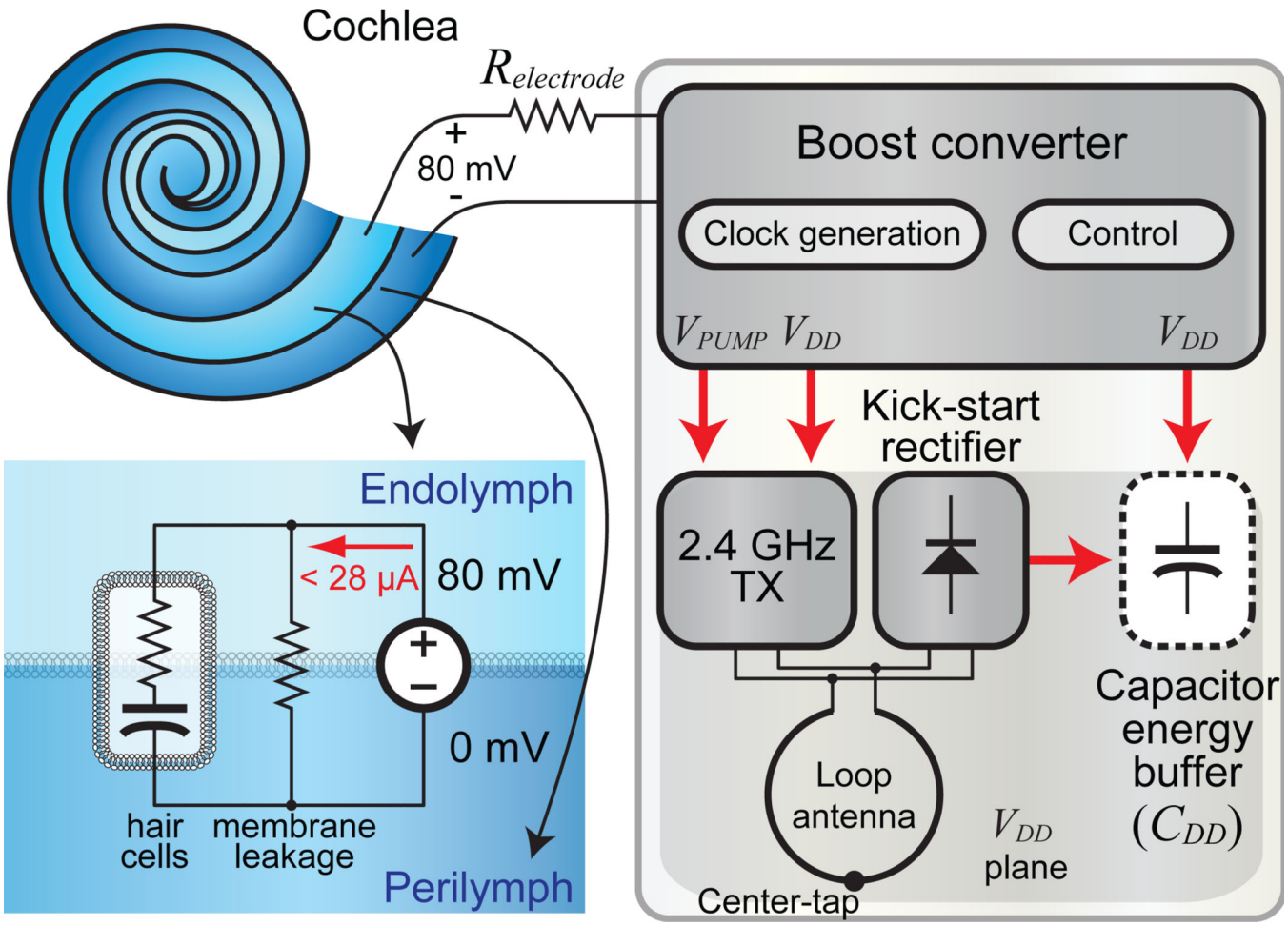


Fig. 1.
Architecture of the endocochlear potential harvesting, sensing, and communicating system.

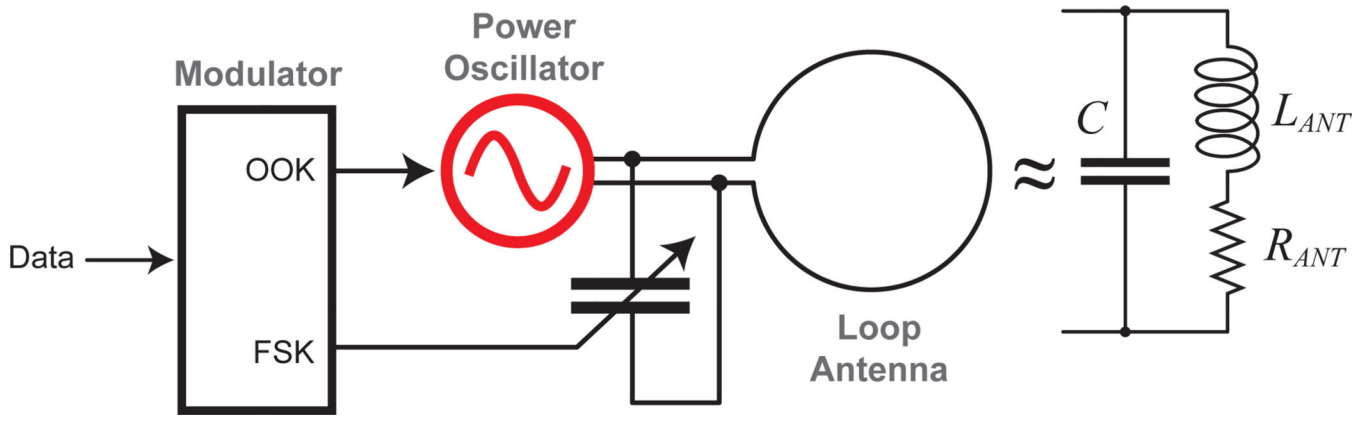


Fig. 2.
Simplified block diagram of the direct-RF power oscillator transmitter.

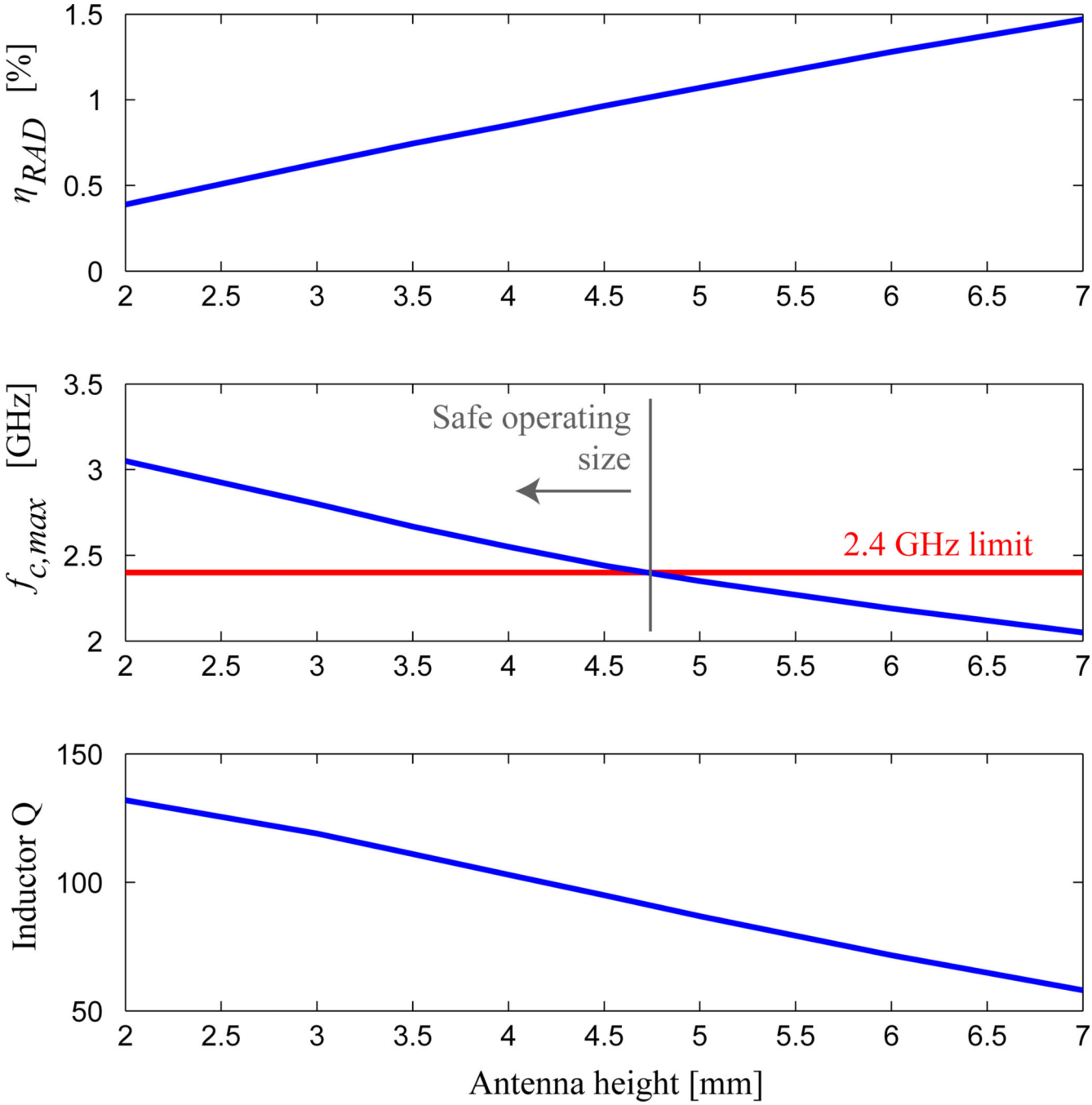


Fig. 3.
Electromagnetic simulation results for varying the antenna height for a fixed, 3 mm antenna width.

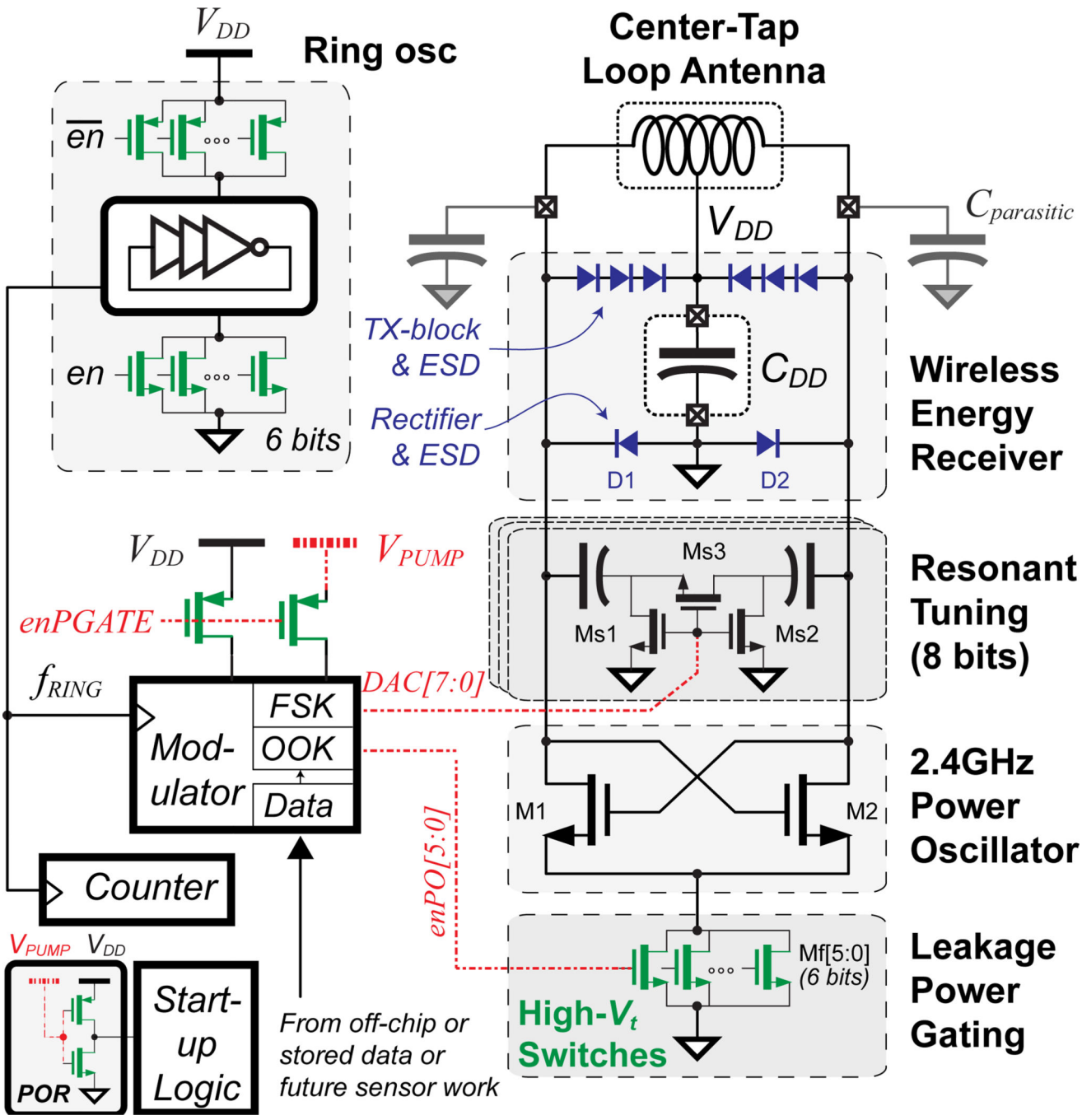


Fig. 4.

Detailed circuit schematic of the 2.4 GHz radio transmitter with integrated wireless energy receiver. High-V_t switches are shown in green, and signals operating from the charge pump supply are shown in red with dash-dot lines.

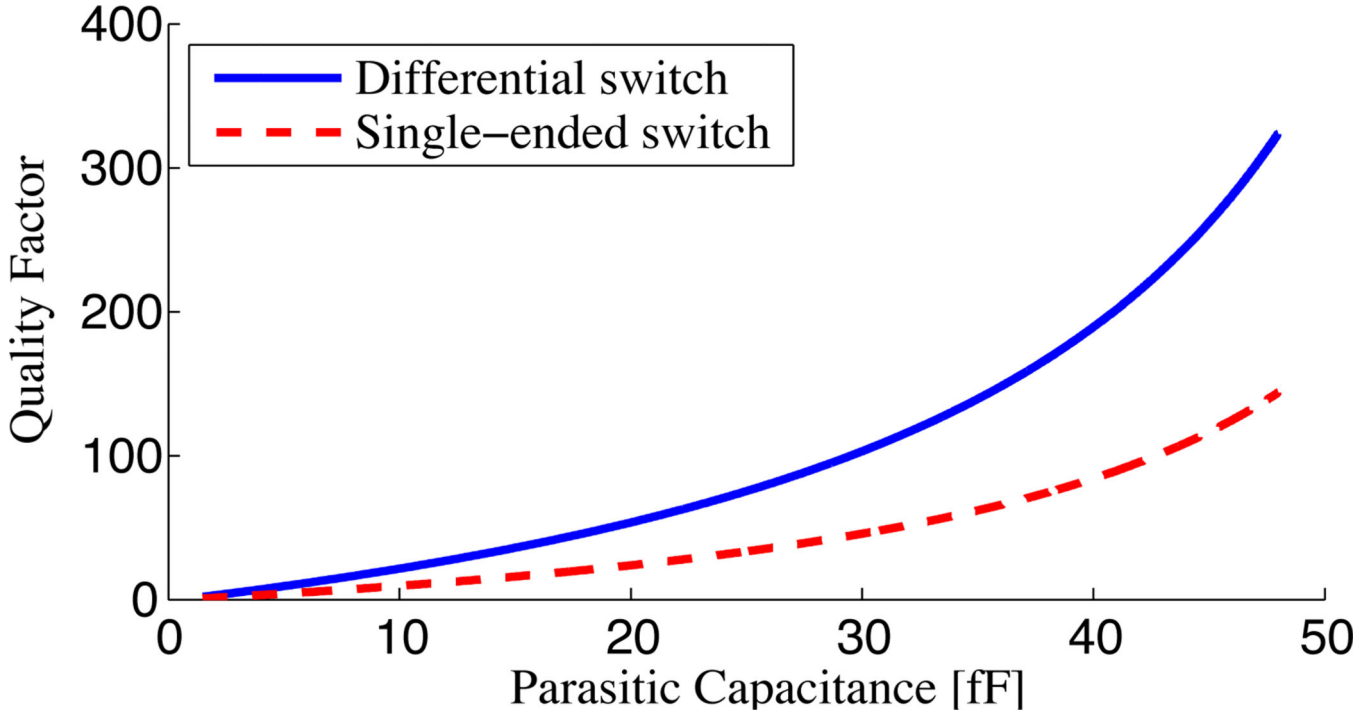


Fig. 5.
Simulated capacitor quality factor versus parasitic switch capacitance for single-ended and differential switches.

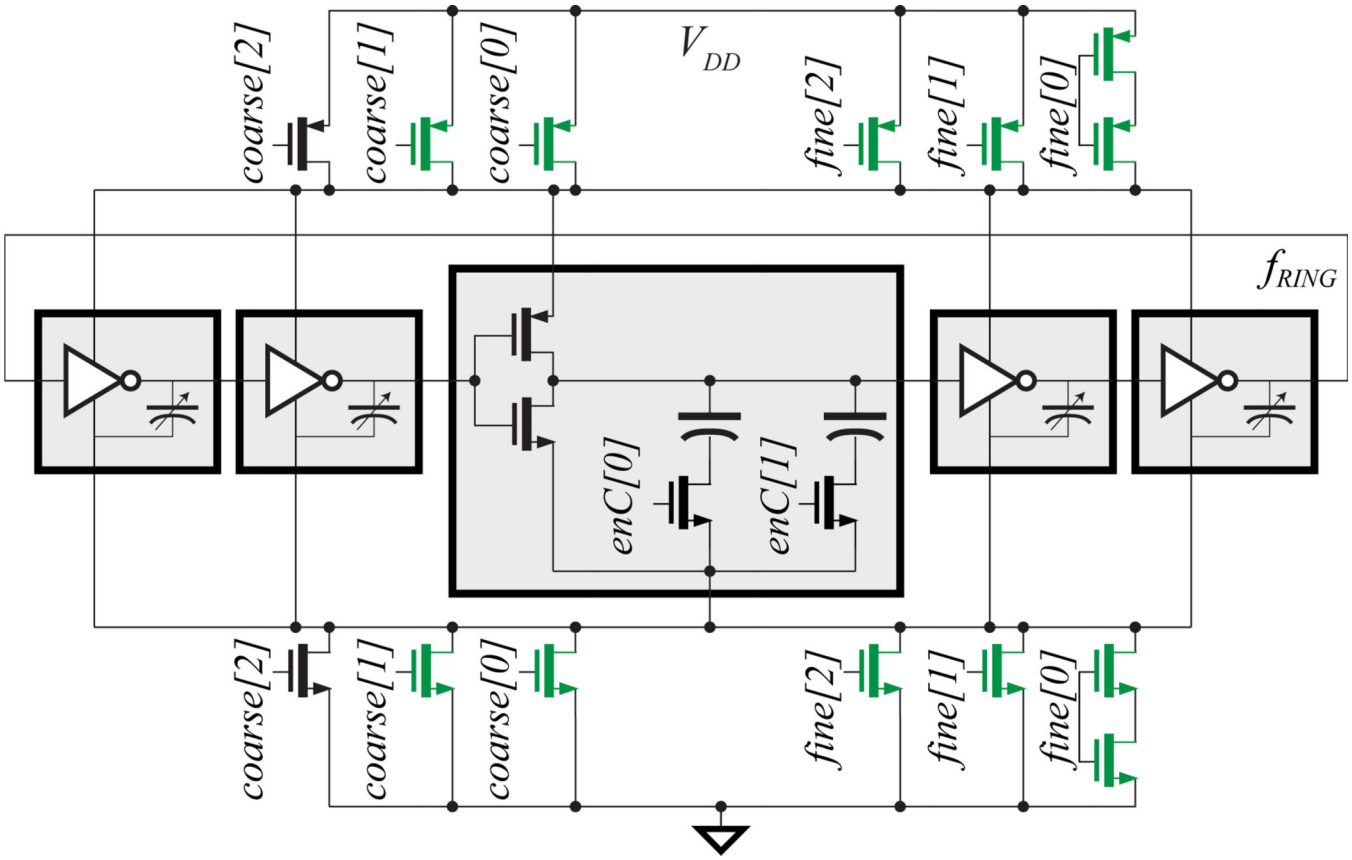


Fig. 6.
Current-starved ring oscillator schematic. High-V_t devices are shown in green.

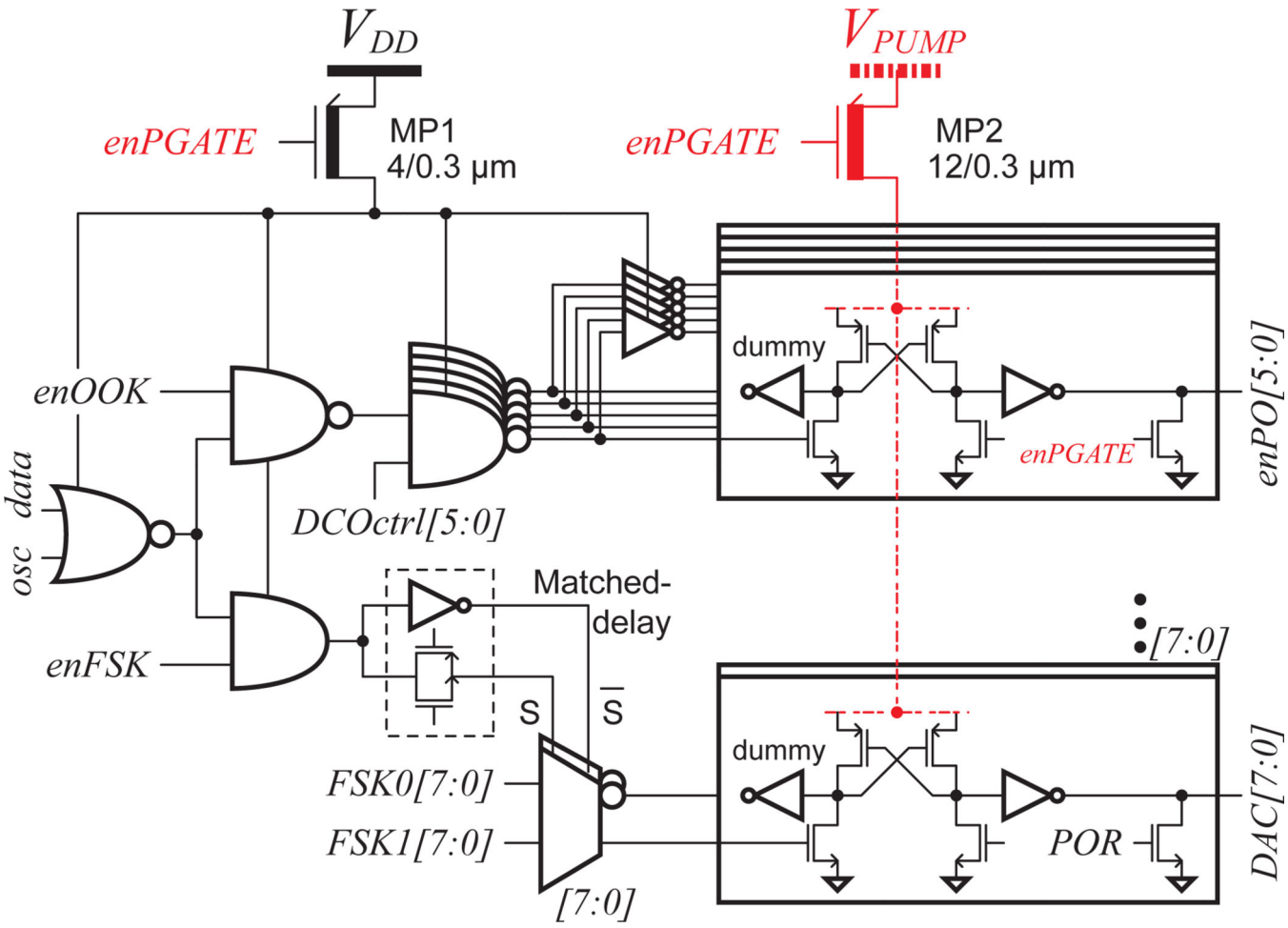


Fig. 7.
Main data path of the modulator.

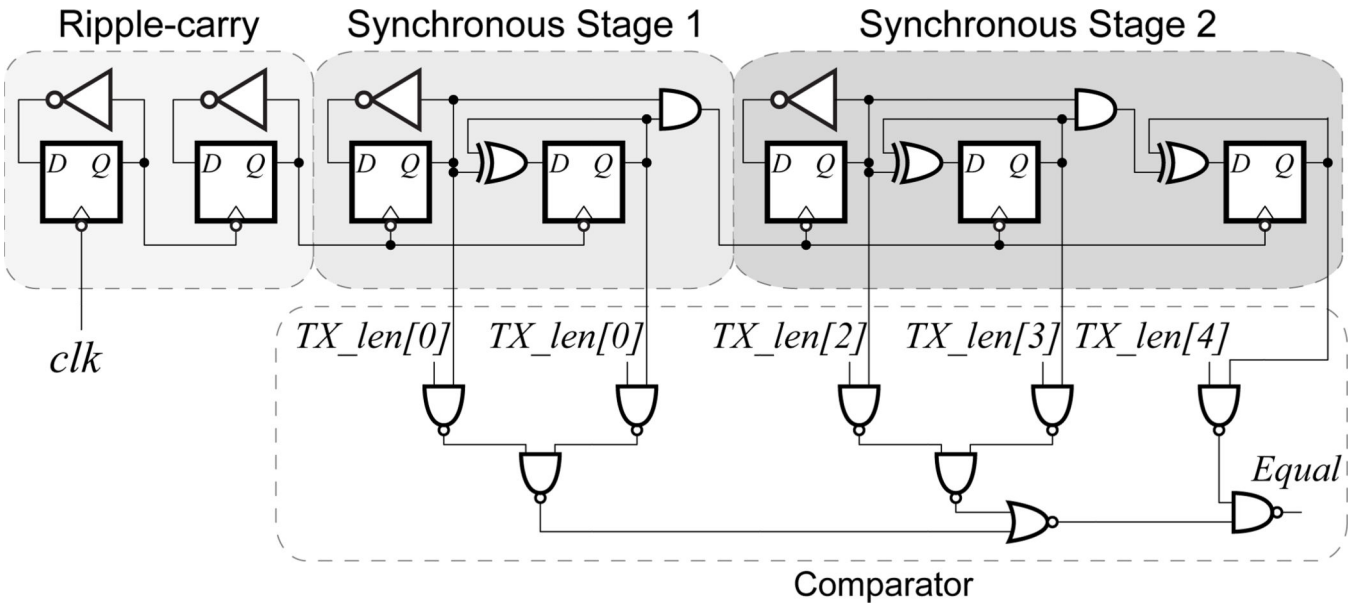


Fig. 8.
Circuit schematic of the 7-bit (5-bit output) counter, with the 5-bit comparator used to set the transmitted packet length.

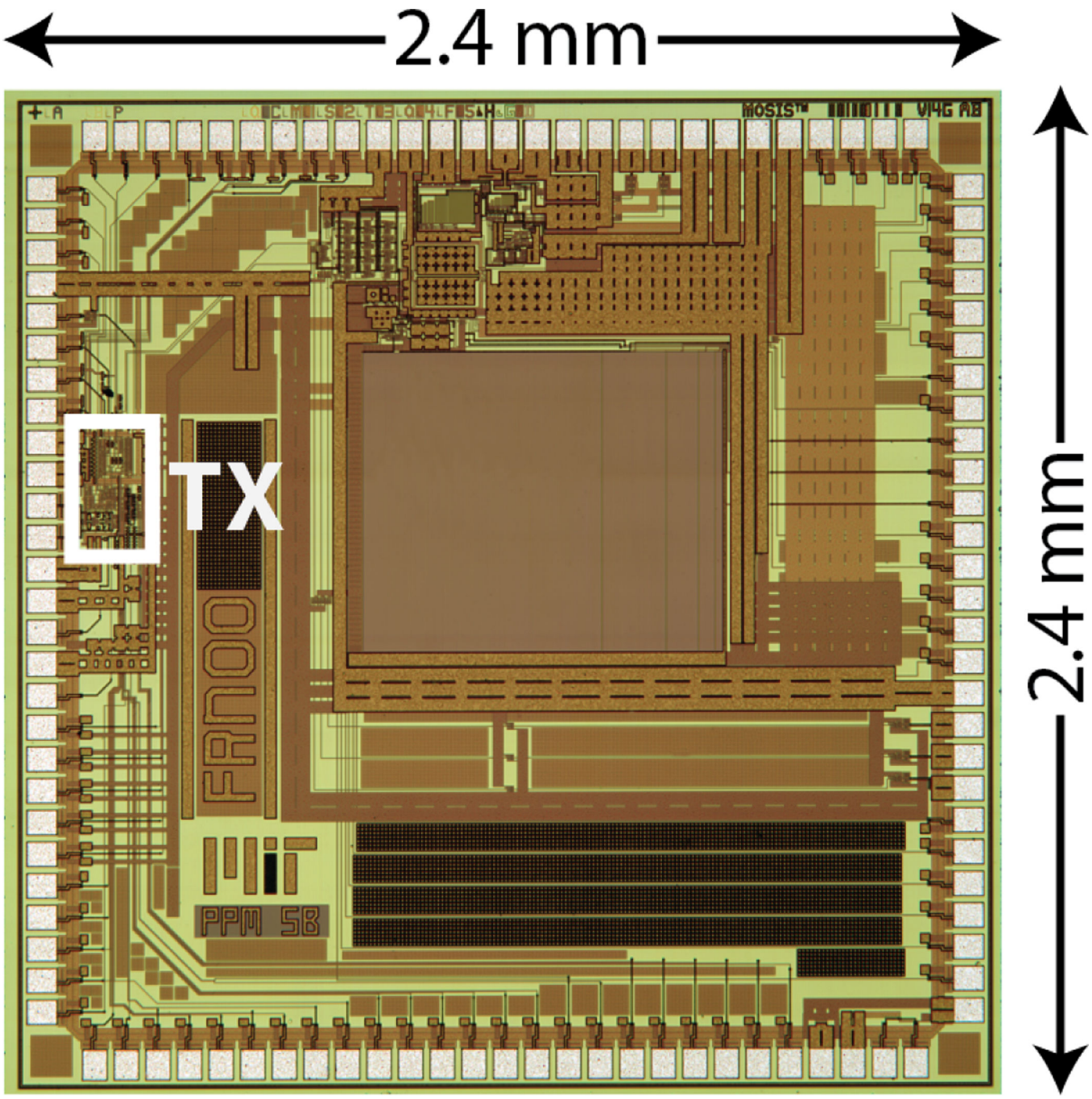


Fig. 9.
Die photograph.

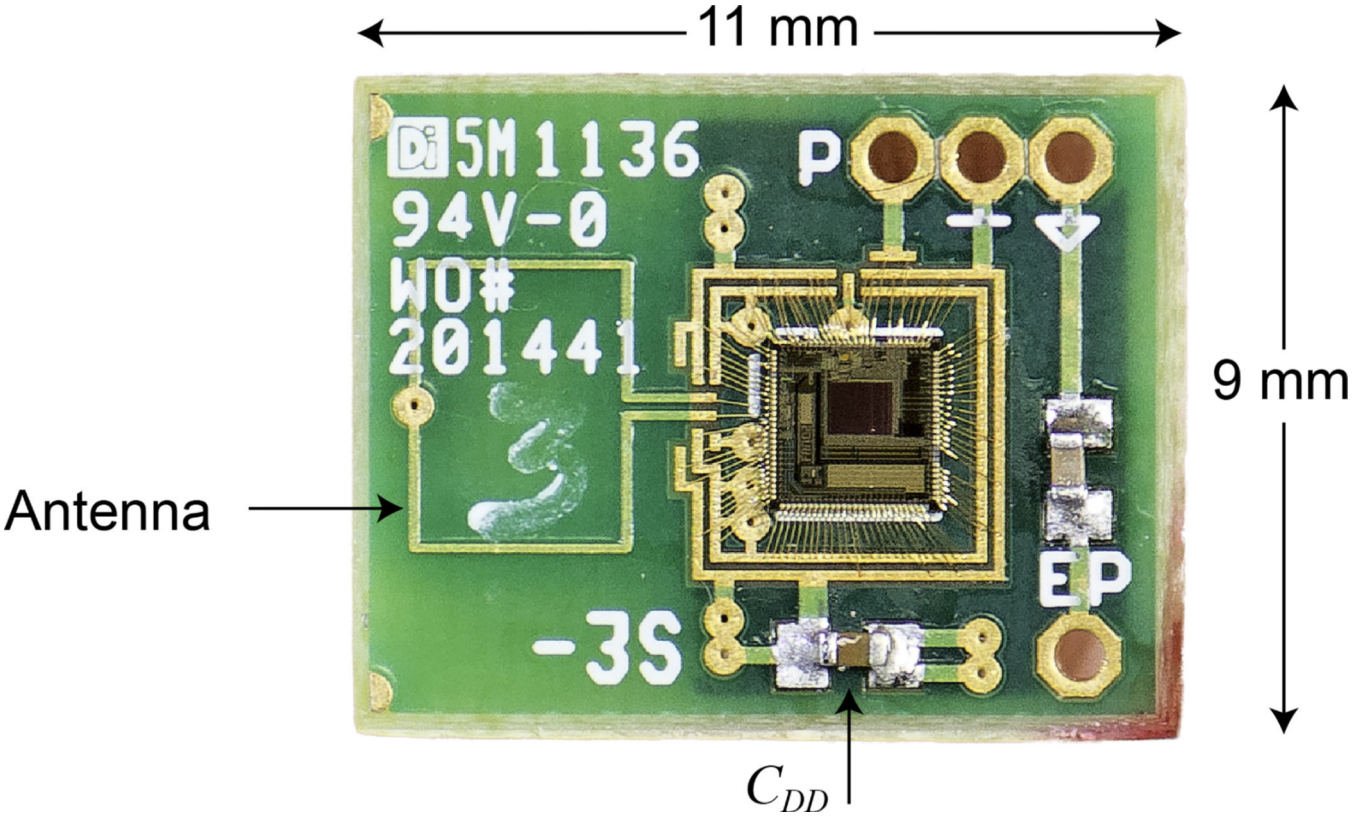


Fig. 10.
Photograph of the chip-on-board package (the protective epoxy covering the chip is not shown for clarity).

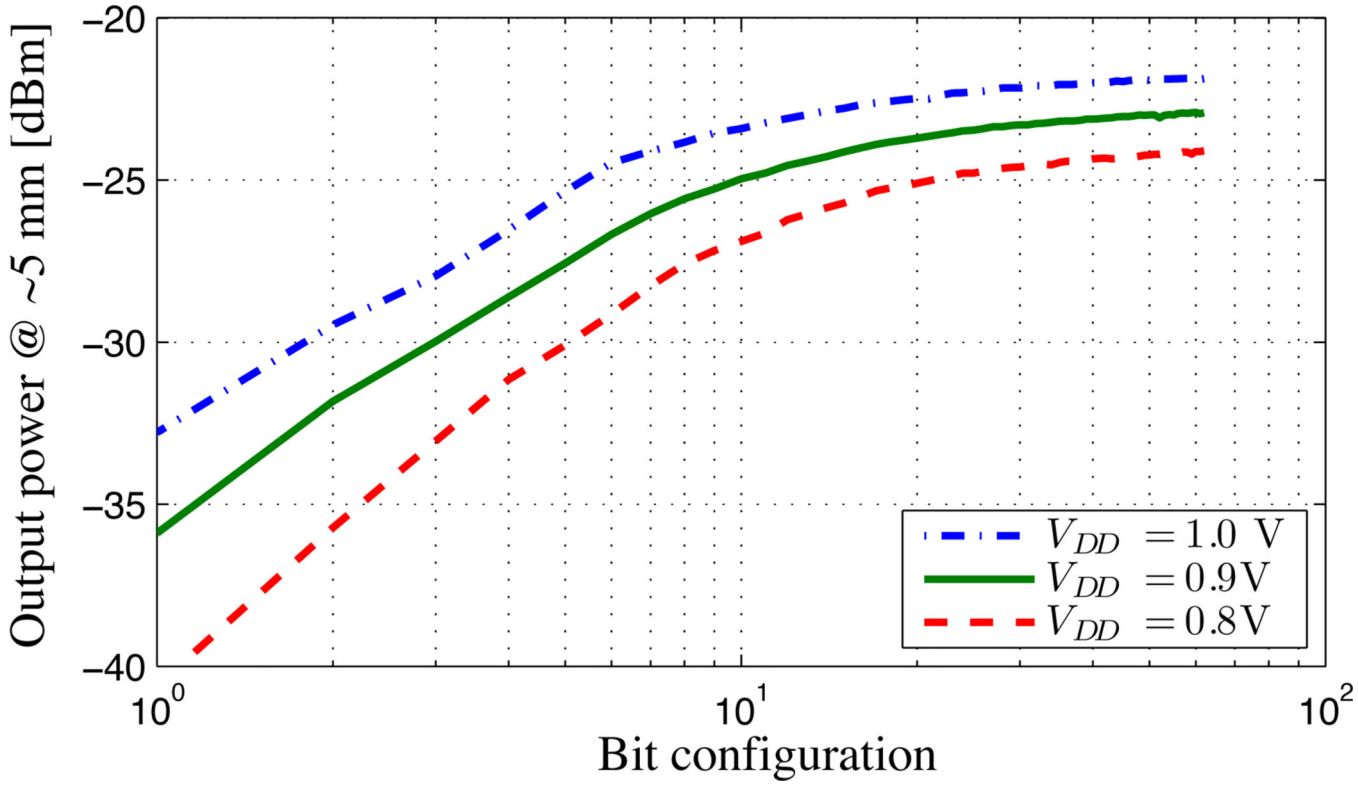


Fig. 11.

Active-mode output power of the radio transmitter measured from approximately 5 mm from the on-board loop antenna, plotted versus power oscillator current configuration settings.

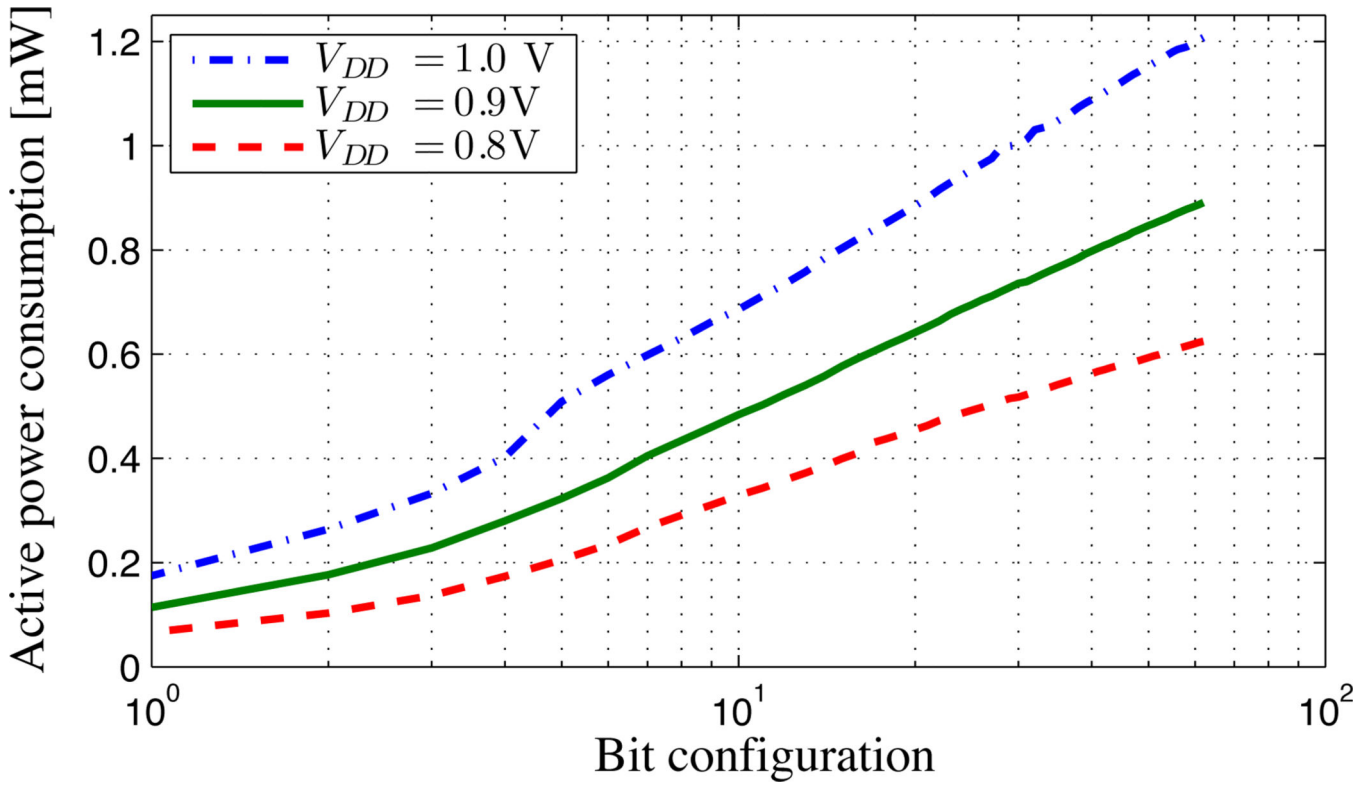
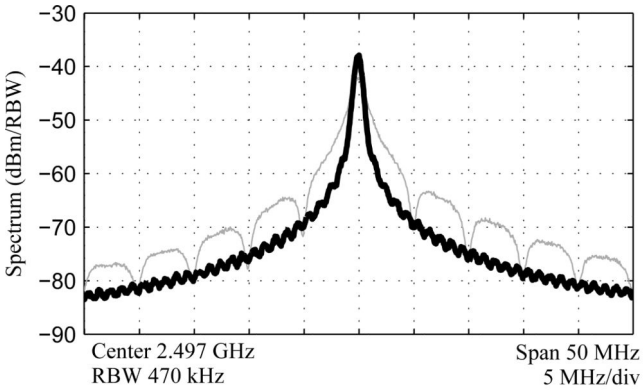
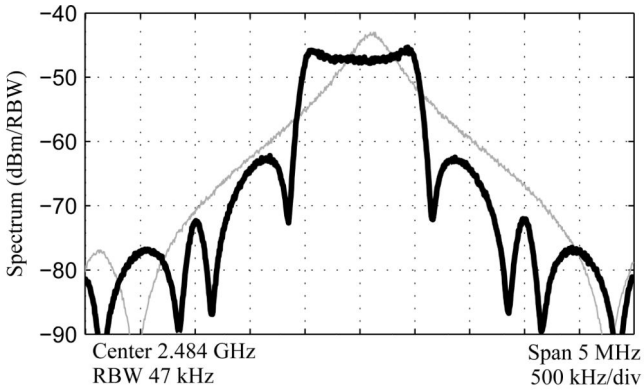


Fig. 12.

Measured active-mode power consumption of the transmitter plotted versus power oscillator current configuration settings.



(a) OOK modulation at 1 Mb/s (dark) and 10 Mb/s (light).



(b) FSK modulation at 1 Mb/s (dark) and near-MSK 2.5 Mb/s (light).

Fig. 13.

Measured spectra taken using a λ/4 whip antenna a few centimeters from the on-board loop antenna.

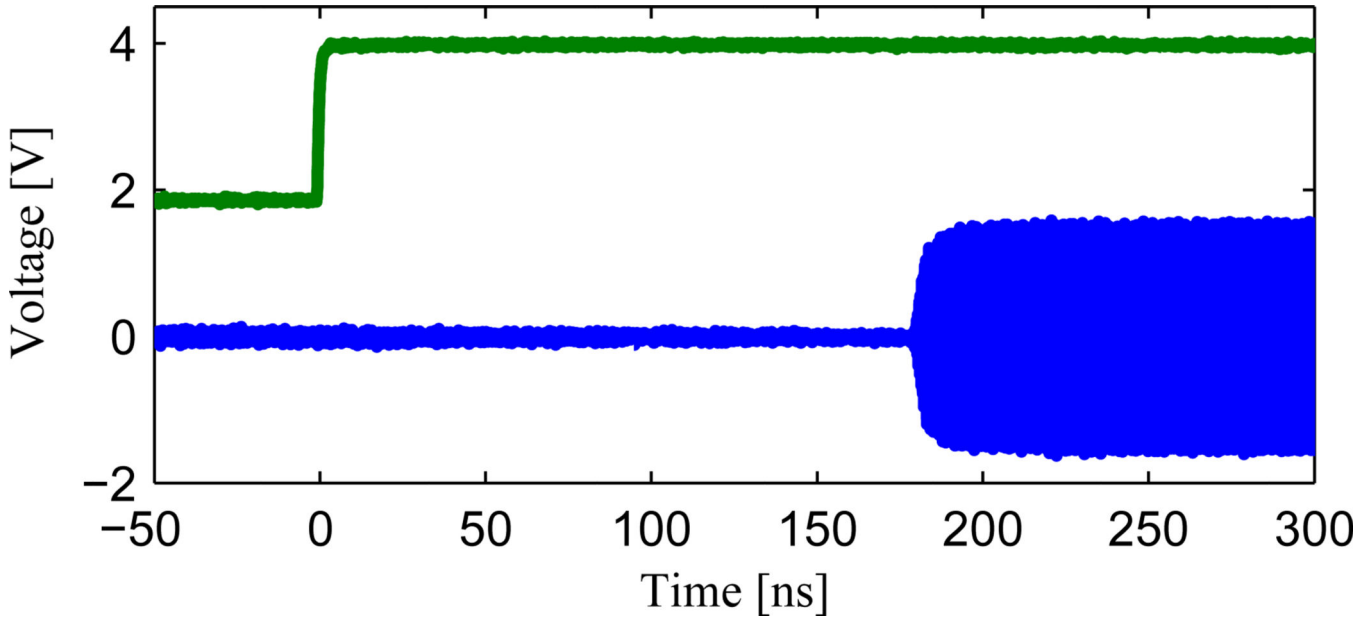


Fig. 14.
Measured transient response, showing a 180 ns startup time between an enable signal and RF output.

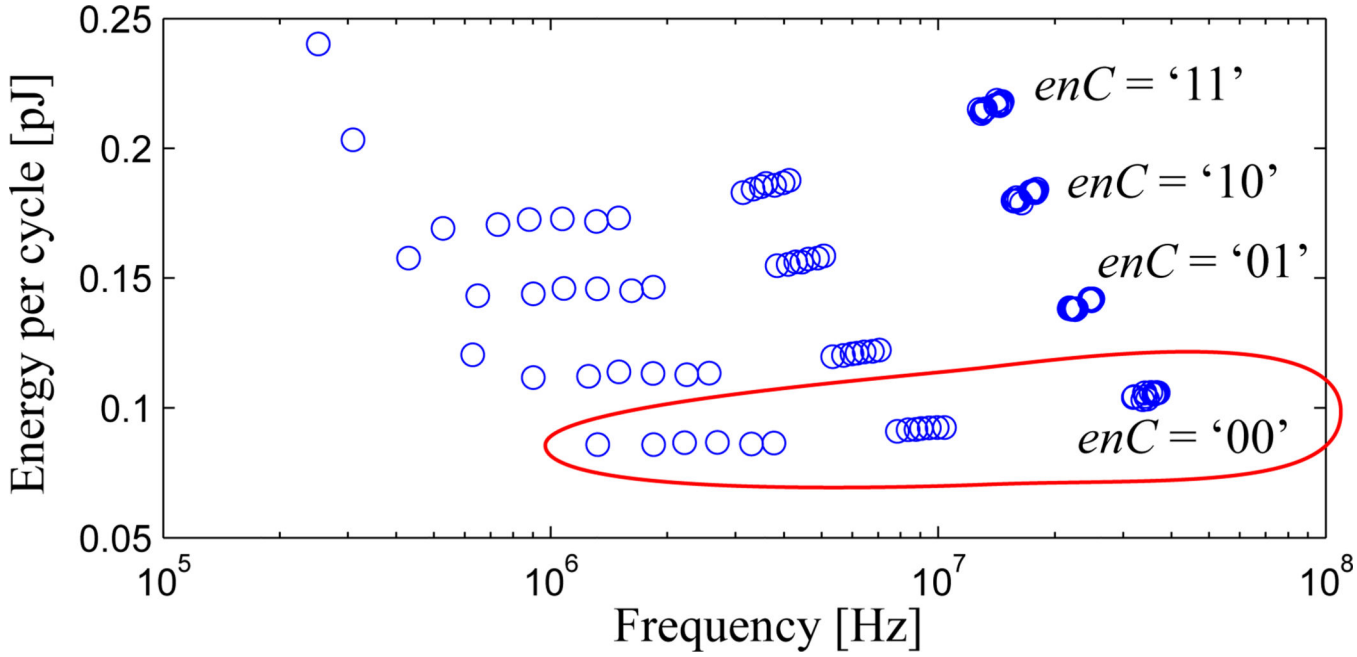


Fig. 15.
Measured energy required for every cycle of the ring oscillator at V_{DD} = 0.8 V.

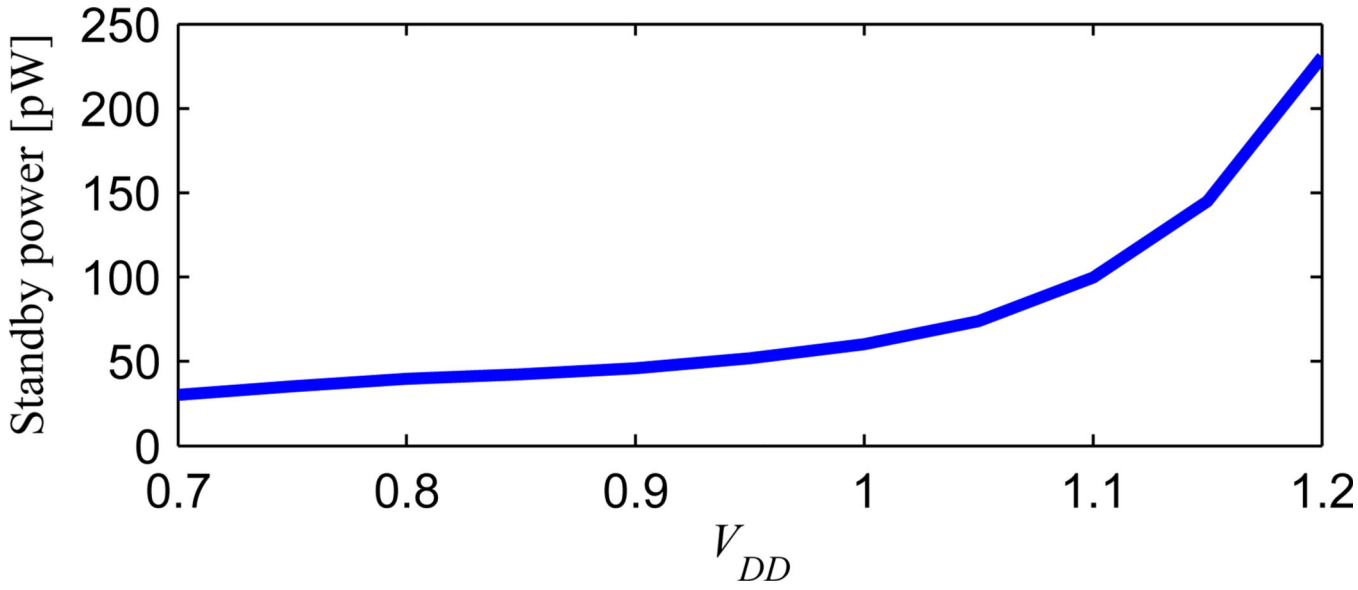


Fig. 16.
Measured standby power of the radio transmitter plotted versus various system supply voltages.

TABLE I

Performance of a 3 × 4 mm^2 loop antenna in free space and biological tissue environments at various ISM bands

	400 MHz			900 MHz			2.4 GHz			5.8 GHz		
	η_{rad}	Q	L [nH]	η_{rad}	Q	L [nH]	η_{rad}	Q	L [nH]	η_{rad}	Q	L [nH]
Simulated (air/FR-4)	0.003%	91	10.5	0.04%	124	10.6	0.8%	105	12.6	6%	No longer	
Simulated (bio/FR-4)	0.00004%	75	10.3	0.006%	90	10.6	0.05%	33	14.6	2%	inductive	
Simulated (bio/Rogers)	0.00004%	76	10.3	0.006%	98	10.5	0.05%	46	13.6	2%		

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TABLE II

Summary of chip results

Technology	0.18 μm	**Standby power** (0.8 V)	39.7 pW
Core area	0.035 mm^2	**Active power** (0.8 V)	191 μW
Supply	0.8–1.0 V	**Active E/bit** (5 Mb/s)	38 pJ/bit
Inst. data rate	1–10 Mb/s	**Average power** (1 b/s)	78 pW
PN @ 1MHz	−105 dBc/Hz	**Max output power** (IV)	−20 dBm

TABLE III

Measured standby-mode power breakdown at various supply voltages compared to simulated results.

	Standby power consumption [pW]				
V_{DD} [V]	PO	Ring Osc.	Digital	V_{PUMP}	Total
0.8 (simulated TT)	0.6	7.8	1.0	9.1	18.7
0.8 (simluated FF)	1.3	27.2	3.3	29.4	61.4
0.8 (measured)	0.7	16.5	4.7	14.8	39.7
0.9 (measured)	0.8	18.8	5.1	17.6	45.8
1.0 (measured)	0.9	21.1	5.9	22.2	60.3

TABLE IV

Measured active-mode power breakdown of the radio transmitter operating at 0.8 V and at a frequency of 2.48 GHz.

		Active-mode power consumption [μW]				
Mod.	**Output Power**	**PO**	**Ring**	**Digital**	V_{PUMP}	**Total**
OOK	> −29 dBm	191	0.1	0.1	0.3	**191**
FSK	> −26 dBm	374	0.1	0.2	0.2	**374**

TABLE V

Comparison of previously published energy efficient and/or low power transmitters.

Reference	Frequency [MHz]	Data rate [Mbps]	P_{out} [dBm]	Energy/bit [pJ]	Standby power [pW]
[5]	900	5	−10	140	–*
[15]	400	0.12	−16	2900	–*
[16]	400	0.8	−4.5	< 14,400	≈20,000
[17]	1900	0.33	0.8	4050	–*
[18]	433	3/10	−12.7	187/52	–*
[19]	900	1	−11.4	3800	–*
[20]	2400	1/10	−10	483/48	–*
[21]	2400	0.042	−45	29,000	< 675
[22]	570/690	10	−10	4700	3,300
[36]	9800	0.03	0.1	747	170
This work	**2400**	**5**	**> −29**	**38**	**39.7**

* Most transmitter publications do not report standby/leakage power.