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ARTICLE

Reconfiguring van der Waals Metal–Semiconductor Contacts via Selenium Intercalation/Deintercalation Post-Treatment

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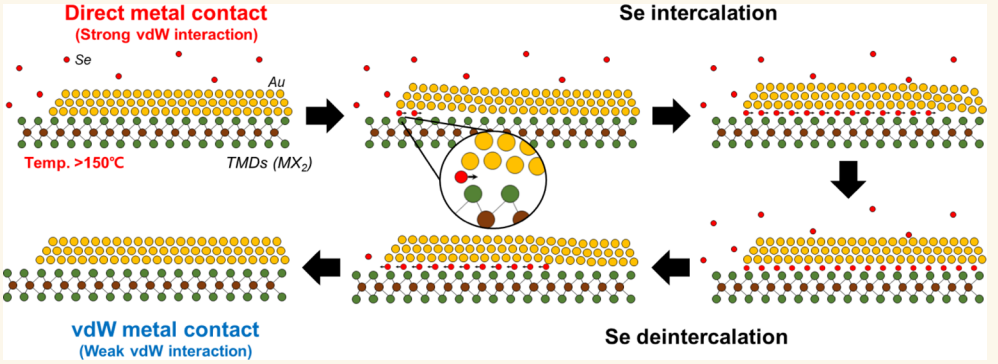

ABSTRACT: To achieve the commercialization of two-dimensional (2D) semiconductors, the identification of an appropriate combination of 2D semiconductors and three-dimensional (3D) metals is crucial. Furthermore, understanding the van der Waals (vdW) interactions between these materials in thin-film semiconductor processes is essential. Optimizing these interactions requires precise control over the properties of the vdW interface through specific pre- or post-treatment methods. This study utilizes Se-environment annealing as a post-treatment technique, which allows for modification of the vdW gap distance and enhancement of the stability of the interfacial structure through the process of Se intercalation and deintercalation at the 2D−3D interface. The depth of Se intercalation and deintercalation is adjusted by varying the temperature and duration of the postannealing process in an Se environment. This precise control over the process enables the effective metallization of 2D semiconductors. The results indicate that expanding the vdW gap and stabilizing the interface structure through this post-treatment significantly improve the metal contact properties in devices such as field-effect transistors and photovoltaic Schottky diodes by minimizing metal-induced gap states, thus reducing Fermi level pinning. The application of Se intercalation and deintercalation techniques achieves an exceptionally low contact resistance of 773 Ω·μm between p-type WSe_2 and Au. Additionally, the integration of doping-free WSe_2 complementary metal-oxide-semiconductor (CMOS) circuits using Se-environment annealing and blocking layers is demonstrated, establishing a promising advancement in semiconductor technology.

KEYWORDS: *van der Waals metal contact, reconfiguration, intercalation/deintercalation, two-dimensional materials, 2D−3D vdW interface, post-treatment*

1. INTRODUCTION

The interaction between two-dimensional (2D) materials and three-dimensional (3D) materials is crucial for the integration of 2D semiconductors, primarily governed by van der Waals (vdW) bonds.[1−4] Understanding these interactions is vital, especially given the predominance of heavy metals and metal oxides with 3D unit cell structures in high-performance device integration.[5−9] These materials often form strong interactions

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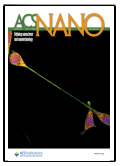

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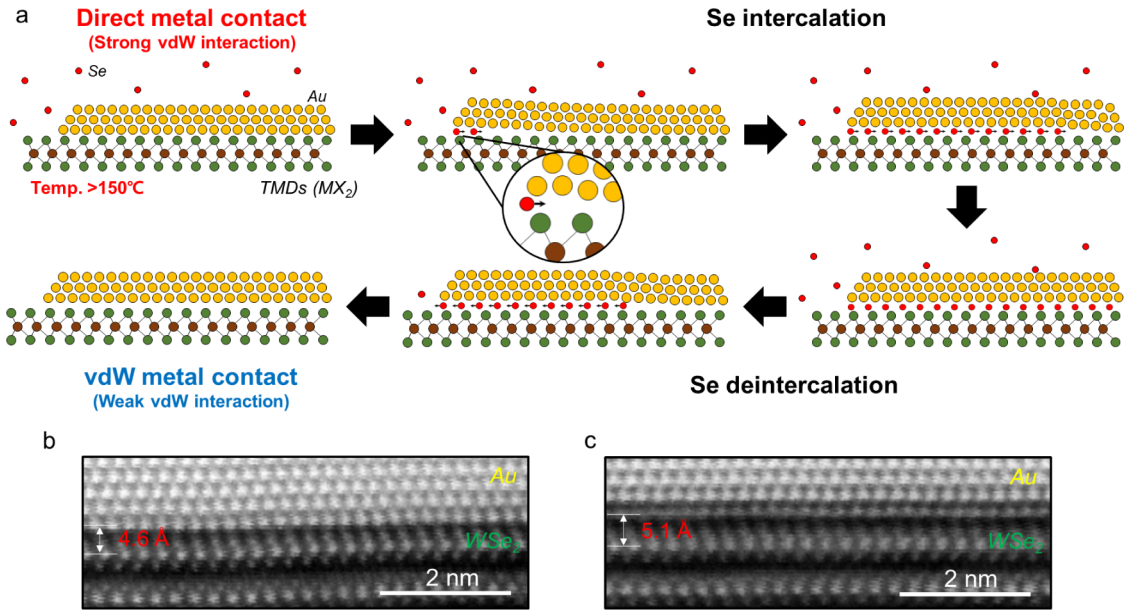

Figure 1. Se intercalation and deintercalation in $WSe_2$and Au via Se-environment annealing. (a) Schematic depicting the Se intercalation and deintercalation process between transition metal dichalcogenides (TMDs) and Au facilitated by Se-environment annealing. (b) Cross-sectional scanning transmission electron microscopy (STEM) image of WSe_2 in direct contact with Au. (c) Cross-sectional STEM image of WSe_2 in direct contact with Au following Se-environment annealing, showing van der Waals (vdW) Au contact.

with 2D vdW materials when metal contacts, gate dielectrics, and substrates are established during the integration process. The effectiveness of these interactions depends on the stability of the vdW state and the distance across the vdW gap. Optimized interfaces typically exhibit weak interactions between the vdW layers and the 3D materials, exemplified by techniques such as transferred metal contacts, the Se buffer layer method, and the oxidation of HfS_2.[5,6,8] Minimizing interfacial defects is imperative to preserve the unique properties of the materials by maintaining a stable vdW state with minimal detrimental interactions at the interface.[5,6,8]

Among the various 2D−3D interactions, metal contact plays a pivotal role in the functionality of all electrical devices. Consequently, precise control of the vdW bonding between 2D semiconductors and 3D metals is essential. Addressing two main issues with metal contact is paramount: reducing contact resistance and eliminating Fermi level pinning (FLP).[5,6,10−13] Notably, a study reported the successful fabrication of an n-type monolayer MoS_2 field-effect transistor (FET) with significantly reduced contact resistance, achieved by using semimetals such as Bi and Sb. These materials are characterized by their low work function and minimal density of state (DOS) near the Fermi level,[14,15] ensuring improved contact efficiency.

The method of growing Sb at optimal substrate temperatures effectively reduces contact resistance by modifying the vdW interactions between MoS_2 and Sb, attributed to alterations in the orientation of Sb's contact surface. Although this technique is effective in reducing contact resistance, it faces challenges in achieving high performance in complementary metal-oxide-semiconductor (CMOS) applications. This limitation stems from its compatibility solely with n-type semiconductors rather than p-type, due to the constraints related to the work functions of Sb metal. For establishing a p-type contact with low resistance in 2D semiconductors, a high-work-function metal is required. However, even high-work-function metals typically exhibit n-type contact characteristics due to FLP, induced by interfacial defects or metal-induced gap states (MIGS) that arise from a narrow vdW gap.[5,6,16]

To reduce FLP, two approaches have been explored: the transferred metal contact and the Se buffer layer method. Both strategies aim to eliminate interface defects and MIGS by shielding the semiconductor from the energetic impacts of impinging metal atoms during deposition.[5,6,17] However, since these pretreatment methods are applied before the formation of the metal−semiconductor junction, there is an urgent need to develop a post-treatment process that can enhance metal contact properties compromised during subsequent metallization steps. The flexible control of metal contact characteristics postmetallization may benefit from a process similar to the forming gas heat treatment, commonly employed in silicon device fabrication.[18]

In this study, the process of Se intercalation and deintercalation was explored, utilizing the unique properties of Se through an annealing process in a Se environment as a postmetallization technique for fabricating 2D semiconductor devices. The phenomenon of Se intercalation has been previously observed at the interface between hexagonal boron nitride (hBN) and metals, even though it is notably limited to specific systems treated via chemical vapor deposition.[19,20] Utilizing the high diffusivity of Se at the interface between 2D materials and 3D metals, this study employed Se for intercalation and deintercalation to modulate MIGS and stabilize the unstable vdW interfaces caused by strong interactions between 2D and 3D materials.

Conventionally, intercalation in 2D materials involves altering the inherent properties of these materials or transforming them into monolayers with new properties by inserting molecules or atoms into the vdW gap. This insertion weakens interlayer interactions and expands the size of the vdW gap.[21−24] Consequently, the intercalation between a 2D semiconductor and metal can attenuate the interactions between them by introducing atoms into the vdW gap. Utilizing both the intercalation and deintercalation effects of Se

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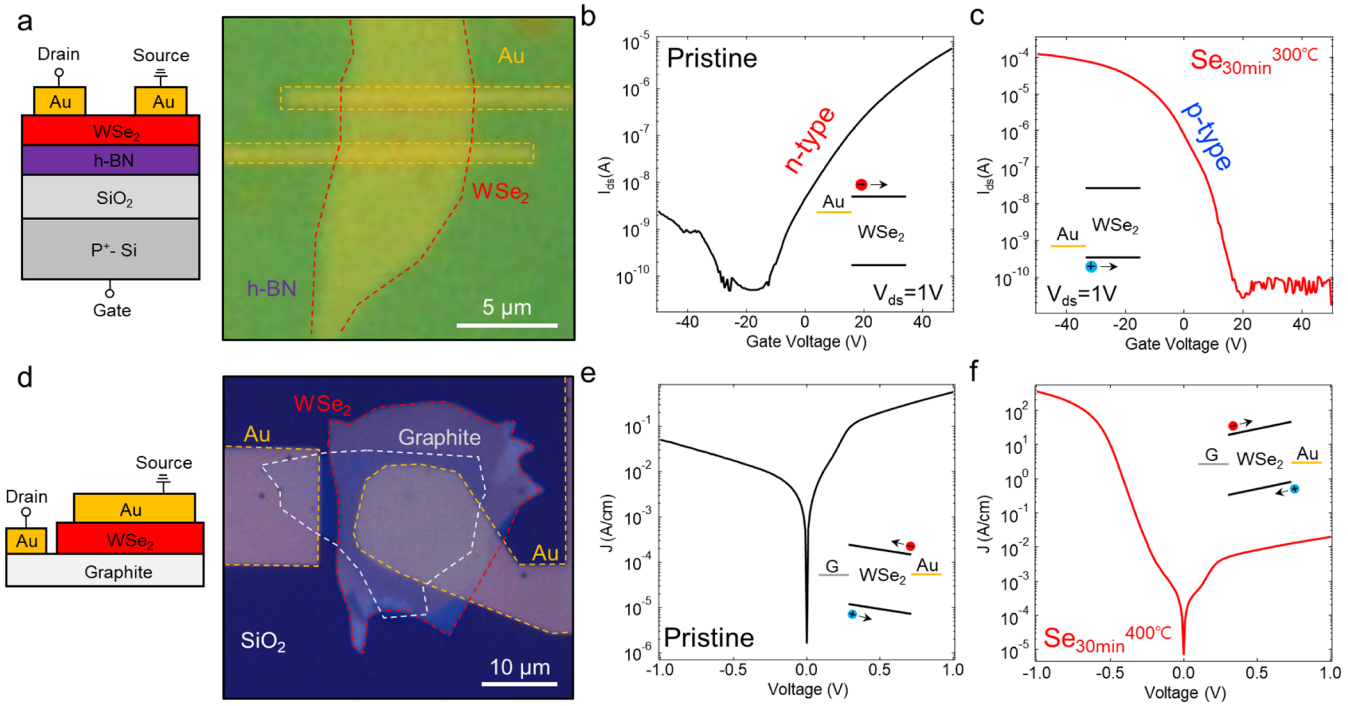

Figure 2. Electrical characteristics of WSe_2 with Au contacts influenced by Se-environment annealing. (a) Schematic and optical images of a WSe_2 field-effect transistor (FET) with Au contacts. (b,c) Transfer curves of the WSe_2 FET with direct Au contact: (b) before Se-environment annealing at 300 °C for 30 min; (c) after the annealing, with channel length $L = 2\ \mu m$ and width $W = 6\ \mu m$. (d) Schematic and optical images of a WSe_2 Schottky diode with graphite and Au contacts. (e,f) $I-V$ curves of the WSe_2 Schottky diode with graphite and direct Au contacts; (e) before Se-environment annealing at 400 °C for 30 min; and (f) after the annealing. The graphite contact was biased, and the Au contact was grounded.

atoms in a 2D semiconductor/metal system facilitates outcomes similar to those of resolving FLP by cyclically inserting and removing Se atoms at the vdW interface between the 3D metal and the 2D semiconductor. Specifically, after the intercalation of Se atoms disrupts the strong interaction between the 2D semiconductor and the 3D metal, the subsequent deintercalation reestablishes a stable vdW gap with an increased distance, effectively minimizing MIGS. Moreover, the intercalated Se atoms contribute to the healing of surface defects during the deintercalation annealing process at the interface between the metal and 2D transition metal dichalcogenides (TMDs), addressing issues such as chalcogen vacancies that arise from deposition damage, electron beam irradiation, and etching processes.[25−27]

2. RESULTS AND DISCUSSION

2.1. Intercalation/Deintercalation of Se into the vdW Gap between WSe_2 and Au. As depicted in Figures 1a and S1a, this study examined changes in the interface state between WSe_2 and Au electrodes under specific conditions. These electrodes typically exhibit a short vdW gap with strong interaction due to the high energy of Au atoms during metal deposition (direct metal contact). The experimental setup involved creating a thermally evaporated Se atmosphere and maintaining a substrate temperature that was high enough to prevent Se deposition on the substrate itself. This setup was designed to enable both the intercalation and deintercalation of Se atoms.

The process was engineered so that Se atoms would penetrate the edge of the patterned Au electrode, traverse the interface between WSe_2 and Au, and then exit. Remarkably, this manipulation led to a noticeable enlargement of the vdW gap at the interface and restoration of vdW properties, indicating the pivotal role of Se atoms in disrupting the strong interaction between WSe_2 and Au. Given that Se possesses an extremely high vapor pressure, it does not deposit at temperatures of 150 °C or higher; instead, it entirely evaporates from the sample[5,28] (as shown in Figure S1b). Additionally, the heat applied to the substrate augments the kinetic energy of the Se atoms within the vdW gap, thereby increasing their penetration length. The extent of Se intercalation through penetration is thus governed by two primary factors: the substrate temperature and the duration of the exposure. In the next step, after the Se supply was stopped and the sample was gradually cooled in a high vacuum, the residual heat within the sample enables complete deintercalation. This process causes the Se atoms previously intercalated in the vdW gap to pass completely through the gap and escape into the vacuum.

To examine the interface dynamics during the Se intercalation−deintercalation process between WSe_2 and Au, cross-sectional transmission electron microscopy (TEM) analyses were conducted on WSe_2/Au samples, both with and without Se intercalation/deintercalation treatment. Also, to prevent amorphization or defects in WSe_2 during the TEM sampling process, we performed FIB at an extremely low power. We used samples with both direct Au contact and vdW Au contact that showed no signs of amorphization or defects in WSe_2 after the FIB process, ensuring reliable data. The Au layer was applied by using electron beam evaporation, and the WSe_2 flakes were prepared via the exfoliation method. As shown in Figure 1b, the direct Au contact without any treatment typically results in a narrow vdW gap characterized by strong interactions due to the high energy of the metal

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atoms. However, as depicted in Figure 1c, the vdW gap between WSe_2 and Au is notably wider in samples undergoing Se intercalation/deintercalation. This process effectively disrupts the strong vdW interactions found in direct Au contacts, maintaining an increased gap distance even after all of the intercalated Se atoms have diffused out from the interface. This suggests that the initial disruption caused by Se intercalation can be stably preserved through the deintercalation process, resulting in a sustained enlargement of the vdW gap. Additionally, as shown in Figure S2, although the Au layer closest to WSe_2 in the vdW Au contact appears faint in the TEM image, adjusting the contrast and brightness reveals that it forms a well-defined FCC gold structure, indicating that it is not a material like Se−Au alloy.

2.2. Characteristics of WSe_2 Electrical Devices According to Se Intercalation/Deintercalation. Furthermore, as illustrated in Figure 2, the electrical transport properties of the WSe_2 FET and Schottky diode were evaluated before and after the Se-environment annealing process. When Au metal electrodes are used on WSe_2, the high work function of Au (5.1−5.3 eV) positions the Fermi level of Au at the valence band edge of WSe_2.[6,29] Consequently, a p-type Ohmic contact is theoretically established between WSe_2 and Au in the absence of FLP, indicating effective contact formation. When FLP occurs at the interface between WSe_2 and Au due to MIGS and defect states, the Fermi level of Au aligns with the edge of the conduction band of WSe_2. This alignment results in an n-type contact, despite the high work function of the metallic contact. As demonstrated in Figure 2b, WSe_2 FETs typically exhibit n-type characteristics attributable to FLP under direct Au contact conditions. Conversely, the application of a 30 min annealing treatment at 300 °C under a Se-rich environment ($Se_{30min}^{300°C}$) significantly alters the contact properties. This treatment expands the vdW gap sufficiently to eliminate FLP, transitioning the characteristics of the WSe_2 FET from n-type to pronounced p-type.

To specifically assess the impact of Se intercalation−deintercalation between Au and WSe_2 on the characteristics of the Au contact alone, a WSe_2 Schottky diode was constructed with graphite as a bottom electrode and Au as a top electrode, as illustrated in Figure 2d−f. Graphite, a 2D vdW material with a low work function, forms an n-type contact with WSe_2 without FLP, owing to the clean 2D−2D vdW interface between graphite and WSe_2, ensuring a stable Schottky barrier height (SBH).[30] Initially, prior to annealing in the Se environment, the WSe_2 Schottky diode with direct Au contact exhibits positive rectification, as the SBH for electrons between WSe_2 and Au is lower than that between WSe_2 and graphite due to FLP. However, the rectification direction of the WSe_2 Schottky diode reverses after the annealing treatment ($Se_{30min}^{400°C}$), which alters the Fermi level positioning of Au from the conduction band edge to the valence band edge of WSe_2 through Se intercalation/deintercalation. To investigate the role of Se in modulating interface properties, we conducted a comparative analysis using WSe_2 FETs, comparing the effects of a simple heat treatment in a vacuum without Se to those in a Se-enriched environment with Se supplementation. As depicted in Figure S3, n-type WSe_2 FETs, induced by FLP, do not undergo a transition to p-type FETs with mere heat treatment in the absence of Se. However, when FETs in direct contact with Au undergo heat treatment in a Se environment, they are converted to the p-type, highlighting the critical role of Se in reconfiguring the vdW interface between WSe_2 and Au. This finding confirms that FLP cannot be eliminated by heat treatment alone.

In cases where stable vdW interfaces were pre-established—either through metal−WSe_2 contact via the Se buffer layer method or through 2D−2D vdW contact using a graphite 2D layer—it was observed that these stable interfaces remained intact upon further annealing in a Se environment, resulting in no alteration to the WSe_2 FET characteristics[5,30,31] (as shown in Figure S4). Additional experiments were conducted, where the WSe_2 channel was annealed in a Se environment prior to the growth of Au metal on top to assess changes in metal contact characteristics. Contrary to expectations, the outcome revealed that the WSe_2 FETs maintained n-type characteristics rather than shifting to p-type, as illustrated in Figure S5. This suggests that annealing in a Se environment does not induce changes on the WSe_2 surface or affects the doping in the contact region with the metal. Both results from Figures S4 and S5 confirm that the annealing treatment in a Se environment does not impact doping at the channel surface of WSe_2 or the contact region with metal. To further explore whether the FLP curing effect by Se-environment annealing is also effective at interfaces with sputter-deposited metal, where interfacial damage is typically greater than in e-beam evaporation deposition, we investigated the changes in electrical properties, and the vdW gap at the interface in WSe_2 FETs is fabricated using sputter-deposited Au.

As demonstrated in Figures S6 and S7, the n-type characteristics of the WSe_2 FET with direct Au contact, achieved using the sputtering method, were altered to p-type following a Se-environment annealing treatment. This process also resulted in an expanded vdW gap, similar to outcomes observed with electron beam evaporation deposition. Notably, as the surface damage in WSe_2 was more extensive when in direct contact with Au electrodes using the sputtering method, the extent of FLP was larger than that using electron beam evaporation, as illustrated in Figure S8.[30,32] Although many interface defects that occur during Au contact formation by sputtering can be somewhat remedied by heat treatment alone (Figure S9), X-ray photoelectron spectroscopy (XPS) and photocurrent measurements (Figures S10 and S11) indicated that the healing of surface defects in 2D semiconductors by sputter-deposited metal atoms is more effectively achieved through Se-environment annealing than by mere thermal treatment. These observations suggest that the surface structure of WSe_2, compromised by sputtering deposition, undergoes a healing process during thermal annealing, contributing to structural ordering. Concurrently, Se-environment annealing also aids in the elimination of MIGS by expanding the interface between WSe_2 and Au into a more stable vdW gap state during the Se-intercalation process.[33] Additionally, as further confirmed by the XPS spectra, the Au deposited via the e-beam did not damage WSe_2 and showed no signs of defect healing from a Se-environment annealing, with only an overall doping effect observed. Consequently, we conclude that the widening of the vdW gap is attributed not to defect healing by Se, but rather to expansion through Se intercalation/deintercalation. As shown in Figure S12, the XPS spectra of the Au islands on WSe_2 before and after Se-environment annealing indicate that no Se−Au alloy was formed.

Further exploring the generalizability of these findings, experiments involving Te-environment annealing were con-

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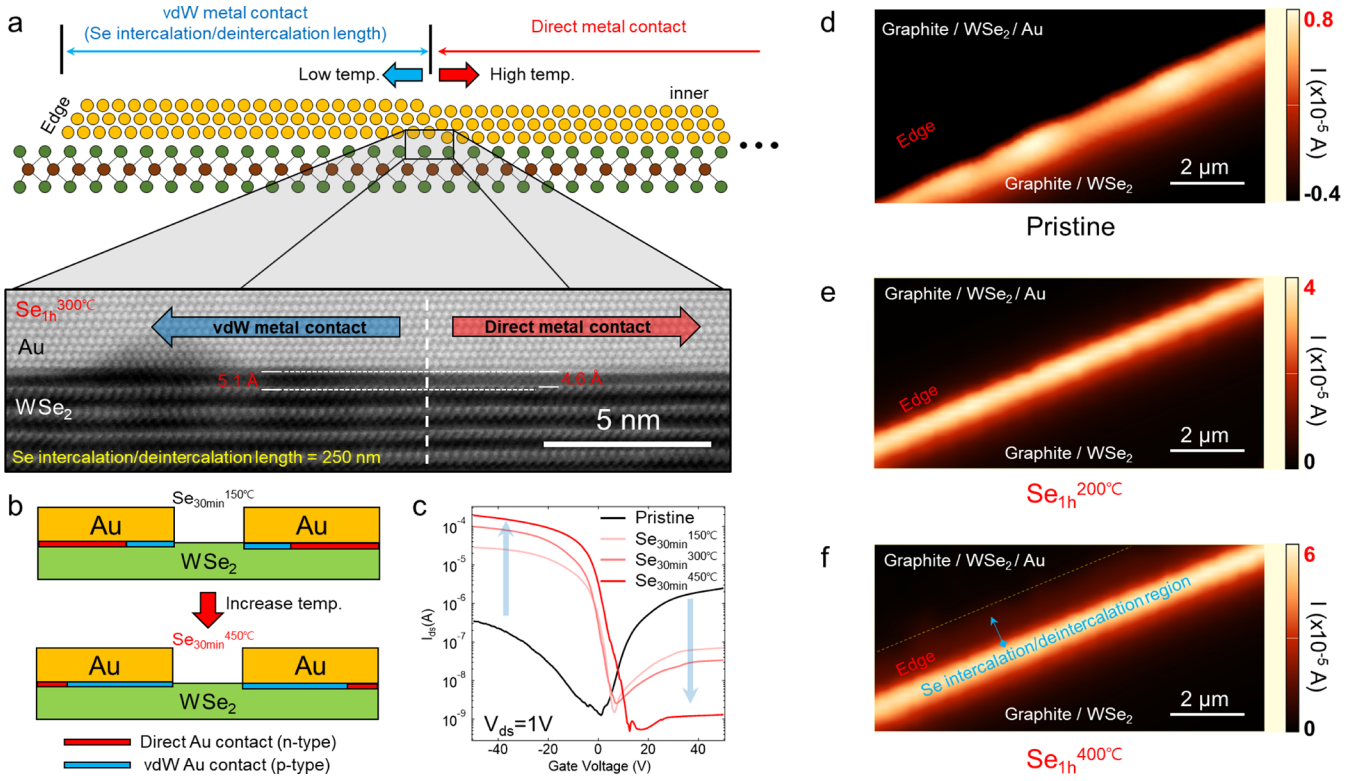

Figure 3. Depth of Se intercalation and deintercalation achieved through Se-environment annealing. (a) Schematic and cross-sectional TEM images showing the boundary of Se intercalation and deintercalation at the interface between WSe_2 and Au post-Se-environment annealing. The vdW gap at the edge region, indicative of the vdW metal contact, is wider than that in the central region with direct metal contact. (b) Schematic illustrating the variation in Se intercalation and deintercalation depth as a function of the annealing temperature in a WSe_2 FET with a Au contact. (c) Transfer curves of the WSe_2 FET with direct Au contact before and after Se-environment annealing at 150 °C, 300 °C, and 450 °C, with channel length L = 2 μm and width W = 8 μm. (d–f) Short-circuit photocurrent mapping of the WSe_2 Schottky diode with Au and graphite contacts; (d) prior to Se-environment annealing; (e) following annealing at 200 °C for 1 h; and (f) after annealing at 400 °C for 1 h. The laser had a wavelength of 532 nm, a power of 0.5 mW, and a spot size of approximately 2 μm. The graphite contact was biased, and the Au contacts were grounded.

ducted on WSe_2 FETs with direct Au contact, as shown in Figure S13. These investigations aimed to assess whether the vdW gap expansion effect through intercalation–deintercalation can be replicated using chalcogen atoms other than Se. The results confirmed that Te-environment annealing does not affect the intercalation/deintercalation process between WSe_2 and Au, indicating no changes in the WSe_2 FET characteristics with direct Au contact under these conditions. In the case of S, similar to Se, the vdW gap expanded, exhibiting p-type characteristics in WSe_2 FET with Au contact after S-environment annealing. (Figure S14)

To evaluate whether Se-environment annealing can be applied across various TMDs, FETs were fabricated with direct Au contacts on semiconductor TMDs and assessed before and after Se-environment treatment. As shown in Figure S15, a transition from n- to p-type characteristics was observed in various TMD FETs with a direct Au contact following Se-environment annealing, suggesting that this treatment can facilitate Se intercalation and deintercalation across a range of TMDs and Au interfaces. Cross-sectional TEM measurements confirmed that vdW gap expansion, due to Se intercalation and deintercalation, was observed between $MoTe_2$ and Au, as depicted in Figure S16. Moreover, similar changes in electrical characteristics and vdW gap expansion were observed in WSe_2 FETs with Pt metal contacts, which possess a large work function, post-Se-environment annealing, confirming that the curing process observed with Au also applies to Pt, as illustrated in Figures S17 and S18. Additionally, although we used 2D flakes with a thickness of approximately 10 to 20 nm, to verify the effectiveness of p-type behavior after Se annealing for different thicknesses, we fabricated WSe_2 FETs with Au contacts of various thicknesses, as shown in Figure S19, and evaluated their electrical properties after Se-environment annealing. As a result, we confirmed that p-type characteristics were consistently stable in all WSe_2 flakes with a thickness of 4 nm or greater.

2.3. Penetration Depth of Se Intercalation/Deintercalation between Metal and 2D Semiconductor. The penetration length of Se intercalation and deintercalation is determined by the diffusion and subsequent escape of Se atoms within the vdW gap during Se-environment and vacuum annealing, respectively.[34] As the annealing temperature increases, the diffusion length of Se atoms also increases, implying that the penetration length of Se intercalation and deintercalation extends further from the edge region. As shown in Figure 3a, cross-sectional TEM was utilized to analyze the penetration length of Se intercalation and deintercalation at the vdW interface between WSe_2 and Au following annealing under $Se_{1h}^{300°C}$. Observations indicated that the vdW gap length between the top metal layer and the bottom WSe_2 layer changed near a point of 250 nm from the edge. This change in the vdW gap, due to the Se intercalation and deintercalation processes, effectively converted direct Au contacts to vdW Au contacts through the Se infiltration process. This clearly

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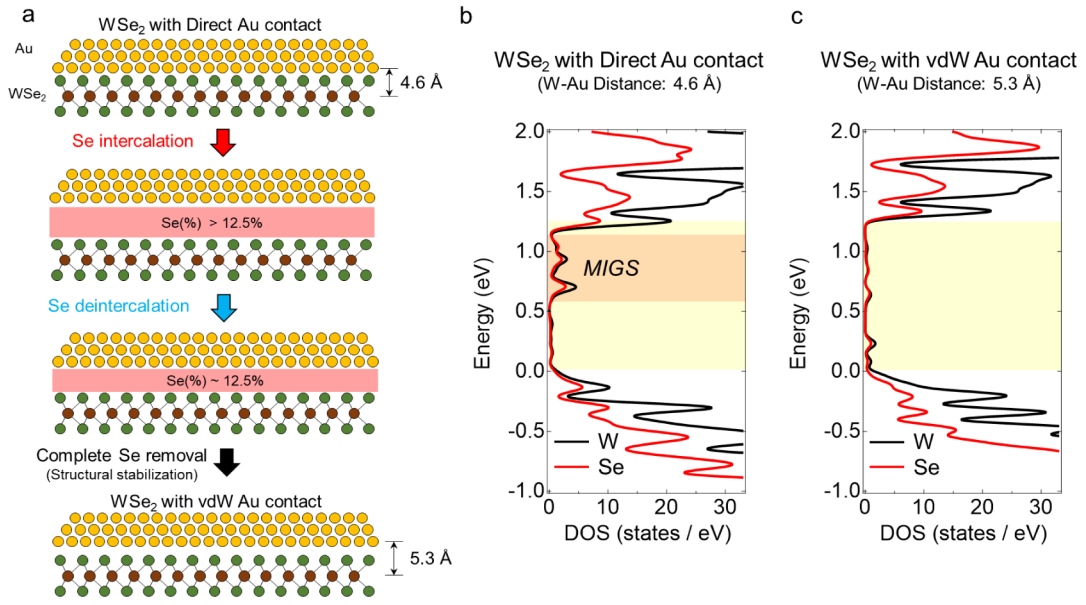

Figure 4. Density of states (DOS) of WSe_2 with direct Au contact before and after Se intercalation/deintercalation. (a) Schematic of the DFT calculation process illustrating Se intercalation and deintercalation between WSe_2 and Au via Se-environment annealing. (b) DOS for each W and Se atom in WSe_2 with direct Au contact before the intercalation/deintercalation process. (c) DOS for each W and Se atom in WSe_2 with direct Au contact after the intercalation−deintercalation process (vdW Au contact), showing the nearest distance between a W atom and a Au atom.

demonstrates the impact of Se, which penetrates up to 250 nm into the interface, expanding the vdW gap distance before it escapes back into the vacuum. Additionally, the deintercalation process was so effective for the high activity of Se that no Se remained at the interface, and the altered vdW gap remained remarkably stable thereafter.

As illustrated in Figure 3b,c, the dependence of the annealing temperature on the Se intercalation/deintercalation length in WSe_2 FETs with direct Au contacts was explored. Increasing the annealing temperature in the Se environment enhanced the transition from n-type to p-type characteristics, corresponding to the increased Se penetration length and a higher proportion of vdW Au contacts than direct Au contacts. As shown in Figures S20 and S21, as the temperature of Se intercalation/deintercalation increased, the saturation current increased and the time required to reach saturation decreased. To further explore the relationship between Se penetration length and FET characteristics, electrical properties were examined in two devices with varying contact lengths. At an annealing temperature of 300 °C for 30 min, WSe_2 FETs with a short Au electrode contact length transitioned from n-type to p-type characteristics. However, devices with longer contact lengths exhibited a predominance of p-type characteristics, albeit with some residual n-type properties (Figure S22). Moreover, as detailed in Figure S23, the effects of Se penetration length during intercalation/deintercalation, influenced by the annealing temperature and time, were investigated more thoroughly. A heat treatment at 300 °C for 15 min altered the characteristics of a WSe_2 FET with a wide Au electrode from n-type to predominantly p-type with some n-type characteristics still present. Extending the annealing time to over 60 min enhanced the p-type characteristics, even though some n-type features persisted in devices with wide electrode lengths. However, increasing the annealing temperature to 450 °C nearly converted the remaining n-type characteristics to p-type, suggesting that the Se penetration length reached nearly the entire length of the device, achieving an optimal p-type FET. Remarkably, as shown in Figure S24, the contact resistance between WSe_2 and Au was measured using the TLM and found to be exceptionally low (R_c = 773 Ω·μm), when most of the Au electrode regions were converted to vdW Au contacts as p-type regions through high-temperature Se-environment annealing ($Se_{1h}^{450°C}$). This result highlights the effective stabilization of vdW Au contacts without FLP. Additionally, the Schottky barrier height between WSe_2 and Au was determined through low-temperature measurements (Figure S25). The results showed a barrier of 150 meV (electron) for the direct Au contact before Se-environment annealing and a significantly lower barrier of 43 meV (hole) for the vdW Au contact after Se-environment annealing. The very low barrier of 43 meV is consistent with the very low contact resistance of 773 Ω·μm.

To meticulously analyze the SBH between WSe_2 and Au across different metal contact areas, photovoltaic mapping was performed on the Schottky diode with Au and graphite contacts following Se-environment annealing, as shown in Figure S26. Unlike electrical measurements such as $I-V$ characterization in FETs or Schottky diodes, which assess electron−hole transport across the entire electrode area, photovoltaic mapping in a Schottky diode enables the measurement of local SBH properties at the interface between WSe_2 and Au. This is achieved through local interfacial activity using a focused laser beam.[30] To examine the changes at the interface between WSe_2 and Au after Se-environment annealing, a short-circuit photocurrent map of the WSe_2 Schottky diode with Au and graphite contacts near the edge of the Au electrode was conducted. As depicted in Figure 3d, prior to Se-environment annealing, the photovoltaic photocurrent of the Schottky diode exhibited a weak negative current, indicating that the Fermi level of Au was closer to the conduction band edge of WSe_2 than to that of graphite due to FLP. A weak positive current was observed in the Au edge

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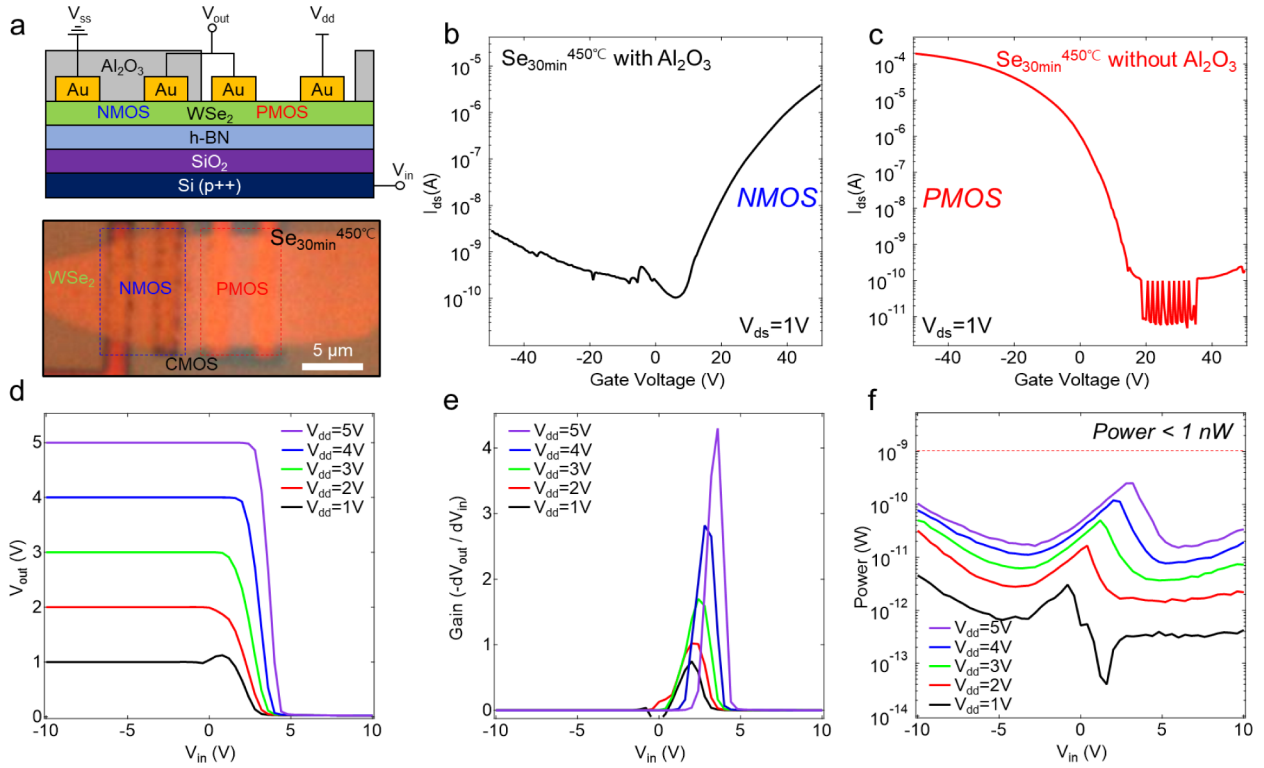

Figure 5. Doping-free WSe_2 CMOS inverter with direct Au contact and patterned Al_2O_3 capping layer to control Se intercalation after Se-environment annealing ($Se_{30min}^{450°C}$). (a) Schematic and optical images of a WSe_2 CMOS featuring direct Au contact with a patterned Al_2O_3 capping layer after Se-environment annealing. (b,c) Transfer curves of the WSe_2 FET with direct Au contact after Se-environment annealing at 450 °C: (b) with the Al_2O_3 capping layer; (c) without the Al_2O_3 capping layer, each with channel length L = 2.5 μm and width W = 10 μm. (d) Voltage transfer characteristics of the WSe_2 CMOS inverter. (e) Voltage gains ($-dV_{out}/dV_{in}$) of the WSe_2 CMOS inverter. (f) Power consumption ($p = I_{dd} \times V_{dd}$) of the WSe_2 CMOS inverter.

region, enhanced by substantial light irradiation onto the WSe_2/graphite interface, contributing to the positive current in that area.[30] After the annealing process at $Se_{1h}^{200°C}$, a strong positive photocurrent was observed near the edge of the Au, as shown in Figure 3e.

This change indicates the formation of a vdW Au contact area from the edge of the Au electrode to the boundary of Se intercalation/deintercalation, which effectively acts as a p-type contact, contributing to a strong positive current. However, the photovoltaic mapping at this annealing condition ($Se_{1h}^{200°C}$) did not clearly reveal the boundary of Se penetration within the WSe_2 Schottky diode, as illustrated in Figure 3e. In contrast, when the annealing temperature was raised to 400 °C, the mapping data distinctly showed a long region of strong positive current extending from the Au edge, as depicted in Figure 3f. This observation confirms that after $Se_{1h}^{400°C}$ annealing, the Se intercalation/deintercalation extends to a region approximately 1 μm from the edge of Au, highlighting the effectiveness of Se-environment annealing in modifying the interfacial characteristics. As shown in Figure S27, in the case of the WSe_2 Schottky diode with a graphite bottom electrode and sputtered Au top electrode, a region exhibiting a strong positive current was observed following Se-environment annealing, similar to the photovoltaic mapping results observed in the WSe_2 Schottky diode with graphite and e-beam deposited Au. Compared with the latter, the photovoltaic current in the sputtered Au sample became positive across a more extensive area than just the edge region. This broader distribution of positive current suggests that the effects observed are due to pure heat treatment rather than solely to Se intercalation/deintercalation at the localized edge area. This explains the changes in the $I-V$ characteristics attributed to heat treatment effects as observed in Figure S9.

2.4. Density Functional Theory Calculation of Se Intercalation/Deintercalation. To further understand the expanding vdW gap between WSe_2 and Au after Se intercalation/deintercalation, density functional theory (DFT) calculations were performed. As illustrated in Figure S28, the investigation into the variation of stability and length of the vdW gap between WSe_2 and Au with increasing amounts of intercalated Se revealed that the stability of the interface improves and the distance between WSe_2 and Au increases when the amount of Se at the interface exceeds 12.5% in a Se-rich environment (μ = 0). This indicates that Se atoms, possessing sufficiently high energy, can readily penetrate the vdW interface between WSe_2 and Au, thereby increasing the vdW gap distance. Subsequent structural stabilization through Se deintercalation results in the formation of a junction state of WSe_2/Au with all Se residues removed. Compared to a W–Au distance of 4.6 Å at the interface without the intercalation process (direct Au contact), it was observed from Figure 4a that the interfacial gap distance at the stable interfacial state after Se intercalation–deintercalation increased to 5.3 Å (vdW Au contact).

Further, Figure 4b,c determines the effect of the Au metal contact on WSe_2 according to the distance between WSe_2 and Au. The DOS of WSe_2 in contact with Au was obtained by performing band structure calculations, providing insights into the electronic interactions at this modified interface. In cases involving the DOS of WSe_2 with direct Au contact (W–Au

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distance = 4.6 Å), metal-induced gap states (MIGS) were observed at the conduction band edge, which contribute to n-type FLP owing to the orbital overlap resulting from the close proximity between WSe_2 and Au. However, in the case of DOS of WSe_2 with vdW Au contact after Se intercalation/deintercalation (W−Au distance = 5.3 Å), no MIGS were detected within the WSe_2 band gap. This absence of MIGS is attributed to the weakened interaction and increased distance between WSe_2 and Au, which effectively alleviates the orbital overlap.[5,35,36] Additionally, as demonstrated in Figure S29, we also explored the influence of Se vacancies on WSe_2 to investigate whether the expansion of the vdW gap post-Se-environment annealing was driven by the curing of Se-vacancy defects or the process of Se intercalation/deintercalation. The vdW gap distance between WSe_2 and Au did not show significant variation with the presence or absence of Se vacancies in WSe_2, indicating that the vdW gap expansion through Se-environment annealing is primarily the result of Se intercalation and deintercalation rather than the curing of Se vacancy defects. This finding aligns with reports showing minimal change in the vdW distance between MoS_2 and Au in relation to S vacancy defects, as determined through DFT calculations.[37]

2.5. Doping-Free CMOS Integration Processes Using Se-Environment Annealing and Blocking Layers. Considering the nature of the Se-environment annealing process, where Se intercalation/deintercalation predominantly occurs at the edge regions of the electrodes, it is feasible to control the electrical type (n- or p-type) of the FET by suppressing the intercalation/deintercalation process by using a blocking layer. As shown in Figure S30, employing Al_2O_3 as a blocking layer preserved the n-type characteristics of a WSe_2 FET with direct Au contact following Se-environment annealing. This demonstrates that during the device fabrication process, using a blocking layer can ensure easy adjustment of FET characteristics based on whether the edge region of the electrodes is exposed, thereby obviating the need for channel doping. Figure 5 illustrates a device that successfully integrates CMOS on WSe_2 without channel doping by employing Se-environment annealing combined with an Al_2O_3 capping layer used as a blocking layer in specific regions. In Figure 5b,c, the devices covered by the Al_2O_3 capping layer retain their n-type FET characteristics due to the original FLP, as the penetration of Se atoms into the vdW gap is effectively blocked during the Se-environment annealing process. Conversely, devices in areas without the capping layer undergo a characteristic transition to p-type FETs facilitated by the Se intercalation/deintercalation process.

Furthermore, the performance of a WSe_2 CMOS inverter fabricated using the patterned Al_2O_3 capping layer and the Se-environment annealing process was evaluated, as shown in Figure 5d−f. Despite featuring a thick stacked gate oxide composed of 300 nm-thick SiO_2 and approximately 30 nm-thick h-BN, the inverter demonstrated robust performance characterized by a substantial voltage gain and distinct on and off states. Notably, since this approach manipulates only the Schottky barrier height between WSe_2 and Au through Se intercalation/deintercalation without altering the channel via doping, there is no threshold voltage shift for each type of FET, and the off−on regions of the n-type and p-type FETs do not overlap. This results in an extremely low leakage current, resulting in a low power consumption (power < 1 nW) CMOS inverter through a doping-free integration process.

Additionally, a metal−semiconductor−metal (MSM) WSe_2 Schottky diode with an ideality factor of 1.5 was demonstrated, employing two types of contacts: a p-type vdW Au contact without an Al_2O_3 capping layer and an n-type direct Au contact with the capping layer, both subjected to the Se-environment annealing process, as depicted in Figure S31. This contact engineering through Se-environment annealing also enables the extraction of intrinsic properties of 2D heterostructures, such as p−n junctions, independent of metal contact influences, potentially leading to a reevaluation of electronic device properties across various 2D vdW materials[38,39] (as shown in Figure S32). Overall, the application of Se-environment annealing, which modifies the contact type without channel doping, is anticipated to simplify the 2D semiconductor process technology and enhances the performance characteristics of various devices.

3. CONCLUSION

By implementing Se-environment annealing, we developed a doping-free post-treatment method that alters the vdW gap between a 2D semiconductor and a 3D metal through Se intercalation and deintercalation. The extent of vdW gap expansion between the 2D semiconductor and the metal can be finely tuned using the Se-environment annealing method, depending on the temperature and duration. This approach holds promise for diverse device applications within 2D semiconductor processing, presenting a substantial shift from conventional 3D semiconductor methods. The modulation of the vdW gap induced by this method has demonstrated significant electrical transformations, highlighting the potential for pioneering new processing techniques exclusive to 2D semiconductors. By utilizing such advanced control over the vdW interface, such as through Se-environment annealing, we anticipate the development of next-generation, high-performance 2D semiconductor devices.

4. EXPERIMENTAL SECTION/METHODS

4.1. Device Fabrication. The sample preparation involved mechanically exfoliated h-BN, TMDs such as WSe_2, WS_2, $MoSe_2$, and MoS_2, and graphite—acquired from HQ Graphene—utilizing the polydimethylsiloxane (PDMS) stamp method, layered onto a cleaned SiO_2 (300 nm) substrate atop heavily p-doped Si. For metal electrode fabrication, poly(methyl methacrylate) (PMMA) was spin-coated onto the graphite/TMDs assembly and then subjected to a soft baking process at 180 °C for 10 min. Subsequently, electron beam lithography was used to pattern the electrodes. The metals (Au, Pt) were then deposited using e-beam evaporation in a high vacuum (>10^{-6} Torr) and sputtering (power, 20 W; Ar, 20 sccm, >10^{-3} Torr). The PMMA was subsequently dissolved in acetone to clean the sample. For the Se-environment annealing, Se was thermally evaporated in an ultrahigh vacuum (<10^{-8} Torr) at a deposition rate of 10 Å/s, with the annealing conducted in the same chamber using a halogen lamp. A 50 nm-thin layer of Al_2O_3 was deposited on the WSe_2 FET at 100 °C as a high-*k* gate insulator and blocking layer using atomic layer deposition (ALD), employing H_2O as a reactant. To selectively remove parts of the Al_2O_3 layer, an AZ MIF 300 developer was employed as an etchant, targeting patterned PMMA areas.

4.2. Transmission Electron Microscopy. The atomic structure of the interface between Au and WSe_2, except for the sample prepared by sputtering (illustrated in Figure S7), was analyzed using transmission electron microscopy (TEM, JEM-ARM200F "NEO ARM," JEOL) at the Yonsei Center for Research Facilities, Yonsei University. TEM and scanning TEM (STEM) observations were conducted at an accelerating voltage of 200 kV. For the sample

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depicted in Figure S7, the atomic structure of the interface between Au and WSe_2 was examined using high-angle annular dark field (HAADF) imaging mode in an aberration-corrected STEM (JEOL JEM-ARM300F) operating at 300 keV, with the equipment housed at the Korea Basic Science Institute.

4.3. Electrical Measurements. Current−voltage (I−V) measurements for all the Schottky diodes were carried out using a 4200-SCS system from Keithley. Transfer curve measurements for the WSe_2 FETs were performed by using a Keithley 6400 system at room temperature.

4.4. Photocurrent Measurement. For the photocurrent mapping, the short-circuit current was recorded using an atomic force microscopy−Raman system (NTEGRA SPECTRA) equipped with a current amplifier at room temperature. The system employed a 100× objective lens, utilizing a laser with a wavelength of 532 nm and a power output of 0.5 mW focused on the sample to a spot size of approximately 2 μm. The photocurrent map was generated by moving the sample stage in a plane, keeping the laser in a fixed position.

For time-dependent photocurrent measurements, the photocurrent was recorded by using a Keithley 2600 system coupled with a current amplifier and a 200 kHz data acquisition system, enabling the measurement of time-resolved photocurrent under ambient conditions. The electrical measurement setups were synchronized using pulsed laser devices, with a laser beam of 532 nm wavelength focused on the sample to a spot size of approximately 10 μm.

4.5. Density Functional Theory Calculation. DFT calculations were conducted using the Vienna Ab initio Simulation Package (VASP). The calculations employed the PBEsol functional along with DFT-D3 vdW correlation and a cutoff energy of 350 eV. Initially, the unit cells of WSe_2 and Au were geometrically optimized until the force on each atom was less than 0.01 eV/Å, using K-point grids of 9 × 9 × 9, 11 × 11 × 11, and 15 × 15 × 15 for their respective optimizations. The model for the Au/WSe_2 interface was constructed with two layers of WSe_2 arranged in 5 × 5 supercells and Au(111) in 3 × 3 supercells, maintaining a lattice mismatch of less than 2.8% with lattice constants a and b both measuring 16.69 Å.

The DFT calculations included bilayer WSe_2 and four layers of Au, focusing on the junction formed at the WSe_2/Au(111) interface. Typically, the coverage of the Se layer was considered to be 100% when a monolayer of Se with a hexagonal structure was fully integrated between the WSe_2 and Au layers.

To evaluate the dependency of formation energy on the interface gap within the WSe_2/Au systems, geometry optimization was carried out and formation energies were calculated for various vdW gap widths, while keeping the distance between the interface Au layer and the interface WSe_2 layer fixed. Additionally, the influence of diffused Se atoms at the interface between Au and WSe_2 was assessed through geometry optimization and calculation of the formation energies for WSe_2/Se/Au systems with differing numbers of Se atoms and interface gaps. The formation energy calculations considered the chemical potential of Se to determine the energy dependency on the vdW gap distance.

Throughout these calculations, geometric optimization was performed until the force on the atoms reached a more relaxed criterion of 0.1 eV/Å using the gamma K-point for simplicity. Finally, the DOS for the interfaces, including those with vdW gaps and hybridization gaps, was calculated using a K-point grid of 2 × 2 × 1 and a cutoff energy of 350 eV to reveal the electronic properties at these modified interfaces.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.4c15117.

Equipment and element for Se-environment annealing, lattice structure of the blurred first layer of Au, annealing effect without Se-environment at WSe_2 FET with Au contact using e-beam evaporation, Se-environment annealing effect in stable vdW contacts, check for Se doping effect at channel region of WSe_2 after Se-environment annealing, electrical properties of WSe_2 FET with direct Au contact using sputtering according to Se-environment annealing, cross-sectional STEM image of interface between WSe_2 and Au using sputtering according to Se-environment annealing, electrical properties of WSe_2 FET with direct Au contact using sputtering and e-beam evaporation, annealing effect without Se-environment at WSe_2 FET with Au contact using sputtering, vdW interface states between WSe_2 and Au using e-beam evaporation and sputtering according to Se-environment annealing through the XPS, time-dependent photocurrent of WSe_2 photocurrent device with direct Au contact according to Se-environment annealing, XPS spectra of Au 4f before and after Se-environment annealing, Te-environment annealing effect of vdW interface between WSe_2 and Au, S-environment annealing effect of the vdW interface between WSe_2 and Au under low vacuum conditions, various TMD FETs with direct Au contact using e-beam evaporation according to Se-environment annealing, cross-sectional STEM image of interface between $MoTe_2$ and Au using e-beam evaporation according to Se-environment annealing, electrical properties of WSe_2 FET with direct Pt contact using sputtering according to Se-environment annealing, cross-sectional STEM image of interface between WSe_2 and Pt using sputtering according to Se-environment annealing, electrical characteristics of WSe_2 FETs with direct Au contact after Se-environment annealing with various thicknesses of WSe_2, electrical characteristics of WSe_2 FET with direct Au contact after Se-environment annealing according to annealing temperature and time, electrical characteristics of WSe_2 FET with direct Au contact after $Se_{30min}^{450°C}$ according to annealing time, electrical properties of WSe_2 FET with direct Au contact using e-beam evaporation according to width of Au electrodes after Se-environment annealing, electrical characteristics of WSe_2 FET with direct Au contact using wide Au electrodes after Se-environment annealing according to annealing time, contact resistance of WSe_2 FET with direct Au contact after $Se_{1h}^{450°C}$ from transmission line measurement (TLM), extraction of Schottky barrier height (SBH) between WSe_2 and Au after and before Se-environment annealing, photocurrent of photovoltaic effect at WSe_2 Schottky diode with Au and graphite contact after Se-environment annealing, photovoltaic of WSe_2 Schottky diode with graphite and direct Au contact using sputtering after Se-environment annealing, DFT calculation of vdW gap distance between WSe_2 and Au versus relative energy graph according to Se concentration of environment and Se intercalation amount, DFT calculation of the distance of the vdW gap between WSe_2 and Au according to Se vacancy, electrical properties of WSe_2 FET with direct Au contact with Al_2O_3 as a capping layer for blocking the Se intercalation according to Se-environment annealing, electrical properties of metal−semiconductor−metal (MSM) WSe_2 Schottky diode with direct Au contact with patterned Al_2O_3 capping layer to block and generate the Se intercalation after Se-environment annealing ($Se_{30min}^{450°C}$), electrical properties of p−n

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junction (WSe_2−MoS_2) with Au contact according to Se-environment annealing (PDF)

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Author Contributions

G.K. conceived the research and designed the experiments with the help of M.-H.C. G.K., H.-S.K., S.O., D.K., W.K., and H.P. contributed to the device fabrication. G.K., S.O., K.J., and S.I. performed the electrical and optical experiments. G.K. and K.J. contributed to DFT calculations and data analyses. The manuscript was written by G.K. and revised by M.-H.C. All experiments and analyses were supervised by M.-H.C.

Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Liu, Y.; et al. Promises and prospects of two-dimensional transistors. *Nature* **2021**, *591*, 43−53.

(2) Liu, Y.; Huang, Y.; Duan, X. Van der Waals integration before and beyond two-dimensional materials. *Nature* **2019**, *567*, 323−333.

(3) Akinwande, D.; et al. Graphene and two-dimensional materials for silicon technology. *Nature* **2019**, *573*, 507−518.

(4) Kang, J. H.; et al. Monolithic 3D integration of 2D materials-based electronics towards ultimate edge computing solutions. *Nat. Mater* **2023**, *22*, 1470−1477.

(5) Kwon, G.; et al. Interaction- and defect-free van der Waals contacts between metals and two-dimensional semiconductors. *Nat. Electron* **2022**, *5*, 241−247.

(6) Liu, Y.; et al. Approaching the Schottky−Mott limit in van der Waals metal−semiconductor junctions. *Nature* **2018**, *557*, 696−700.

(7) Tan, C.; et al. 2D fin field-effect transistors integrated with epitaxial high-k gate oxide. *Nature* **2023**, *616*, 66−72.

(8) Luo, P.; et al. Molybdenum disulfide transistors with enlarged van der Waals gaps at their dielectric interface via oxygen accumulation. *Nat. Electron* **2022**, *5*, 849−858.

(9) Kim, K. S.; et al. Non-epitaxial single-crystal 2D material growth by geometric confinement. *Nature* **2023**, *614*, 88−94.

(10) Allain, A.; Kang, J.; Banerjee, K.; Kis, A.; et al. Electrical contacts to two-dimensional semiconductors. *Nature Mater* **2015**, *14* (12), 1195−1205.

(11) Kim, C.; Moon, I.; Lee, D.; Choi, M. S.; Ahmed, F.; Nam, S.; Cho, Y.; Shin, H.-J.; Park, S.; Yoo, W. J.; et al. Fermi level pinning at electrical metal contacts of monolayer molybdenum dichalcogenides. *ACS Nano* **2017**, *11* (2), 1588−1596.

(12) Wang, Y.; et al. Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature* **2019**, *568*, 70−74.

(13) Wang, L.; Meric, I.; Huang, P. Y.; Gao, Q.; Gao, Y.; Tran, H.; Taniguchi, T.; Watanabe, K.; Campos, L. M.; Muller, D. A.; Guo, J.; et al. One-dimensional electrical contact to a two-dimensional material. *Science* **2013**, *342* (6158), 614−617.

(14) Shen, P.-C.; et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **2021**, *593*, 211−217.

(15) Li, W.; et al. Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature* **2023**, *613*, 274−279.

(16) Yang, Z.; et al. A Fermi-level-pinning-free 1D electrical contact at the intrinsic 2D MoS2−metal junction. *Adv. Mater* **2019**, *31*, 1808231.

(17) Jung, Y.; et al. Transferred via contacts as a platform for ideal two-dimensional transistors. *Nat. Electron* **2019**, *2*, 187−194.

(18) Tsaur, B.-Y.; Mattia, J. P.; Chen, C. K. Hydrogen annealing of PtSi-Si Schottky barrier contacts. *Appl. Phys. Lett* **1990**, *57*, 1111−1113.

(19) Holbrook, M.; Chen, Y.; Kim, H.; Frammolino, L.; Liu, M.; Pan, C.-R.; Chou, M.-Y.; Zhang, C.; Shih, C.-K.; et al. Creating a nanoscale lateral junction in a semiconductor monolayer with a large built-in potential. *ACS Nano* **2023**, *17* (7), 6966−6972.

(20) Dong, A.; Fu, Q.; Wu, H.; Wei, M.; Bao, X.; et al. Factors controlling the CO intercalation of h-BN overlayers on Ru (0001). *Phys. Chem. Chem. Phys* **2016**, *18* (35), 24278−24284.

(21) Wang, C.; He, Q.; Halim, U.; Liu, Y.; Zhu, E.; Lin, Z.; Xiao, H.; Duan, X.; Feng, Z.; Cheng, R.; Weiss, N. O.; et al. Monolayer atomic crystal molecular superlattices. *Nature* **2018**, *555* (7695), 231−236.

(22) Zhang, H.; et al. Tailored Ising superconductivity in intercalated bulk NbSe2. *Nat. Phys* **2022**, *18*, 1425−1430.

(23) Zhou, B.; et al. A chemical-dedoping strategy to tailor electron density in molecular-intercalated bulk monolayer MoS2. *Nat. Synth* **2024**, *3*, 67−75.
(24) Zhou, J.; et al. Layered intercalation materials. *Adv. Mater* **2021**, *33*, 2004557.
(25) Wu, X.; et al. Electron irradiation-induced defects for reliability improvement in monolayer MoS2-based conductive-point memory devices. *npj 2D Mater Appl* **2022**, *6*, 31.
(26) Sun, S.; et al. Defect-rich monolayer MoS2 as a universally enhanced substrate for surface-enhanced Raman scattering. *Nanomaterials* **2022**, *12*, 896.
(27) Zhang, X.; et al. Molecule-Upgraded van der Waals contacts for Schottky-barrier-free electronics. *Adv. Mater* **2021**, *33*, 2104935.
(28) Mattox, D. M. *The Foundations of Vacuum Coating Technology*; Springer, 2003.
(29) Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J.; et al. High performance multilayer MoS2 transistors with scandium contacts. *Nano Lett* **2013**, *13* (1), 100−105.
(30) Kwon, G.; et al. Forming stable van der Waals contacts between metals and 2D semiconductors. *Small Methods* **2023**, *7*, 2300376.
(31) Liu, Y.; Wu, H.; Cheng, H.-C.; Yang, S.; Zhu, E.; He, Q.; Ding, M.; Li, D.; Guo, J.; Weiss, N. O.; Huang, Y.; et al. Toward barrier free contact to molybdenum disulfide using graphene electrodes. *Nano Lett* **2015**, *15* (5), 3030−3034.
(32) Matsui, H.; Toyoda, H.; Sugai, H. High-energy ions and atoms sputtered and reflected from a magnetron source for deposition of magnetic thin films. *J. Vac. Sci. Technol., A* **2005**, *23*, 671−675.
(33) Vilá, R. A.; et al. In situ crystallization kinetics of two-dimensional MoS2. *2D Mater* **2018**, *5*, 011009.
(34) Hennighausen, Z.; Hudak, B. M.; Phillips, M.; Moon, J.; McCreary, K. M.; Chuang, H.-J.; Rosenberger, M. R.; Jonker, B. T.; Li, C. H.; Stroud, R. M.; van't Erve, O. M. J.; et al. Room-temperature oxygen transport in nanothin Bi x O y Se z enables precision modulation of 2D materials. *ACS Nano* **2022**, *16* (9), 13969−13981.
(35) Chen, Y.-H.; et al. Oxidized-monolayer tunneling barrier for strong Fermi-level depinning in layered InSe transistors. npj 2D Mater. *Appl* **2019**, *3*, 49.
(36) Cui, X.; Shih, E.-M.; Jauregui, L. A.; Chae, S. H.; Kim, Y. D.; Li, B.; Seo, D.; Pistunova, K.; Yin, J.; Park, J.-H.; Choi, H.-J.; et al. Low-temperature ohmic contact to monolayer MoS2 by van der Waals bonded Co/h-BN electrodes. *Nano Lett* **2017**, *17* (8), 4781−4786.
(37) Qiu, X.; Wang, Y.; Jiang, Y. First-principles study of vacancy defects at interfaces between monolayer MoS 2 and Au. *RSC Adv* **2020**, *10* (48), 28725−28730.
(38) Chen, P.; Atallah, T. L.; Lin, Z.; Wang, P.; Lee, S.-J.; Xu, J.; Huang, Z.; Duan, X.; Ping, Y.; Huang, Y.; Caram, J. R.; et al. Approaching the intrinsic exciton physics limit in two-dimensional semiconductor diodes. *Nature* **2021**, *599* (7885), 404−410.
(39) Went, C. M.; Wong, J.; Jahelka, P. R.; Kelzenberg, M.; Biswas, S.; Hunt, M. S.; Carbone, A.; Atwater, H. A.; et al. A new metal transfer process for van der Waals contacts to vertical Schottky-junction transition metal dichalcogenide photovoltaics. *Sci. Adv* **2019**, *5* (12), No. eaax6061.

https://doi.org/10.1021/acsnano.4c15117
ACS Nano 2025, 19, 1619−1629