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Los Angeles

Physics Based Reliability Analysis of the Silicon Interconnect Fabric

A dissertation submitted in partial satisfaction

of the requirements for the degree

Doctor of Philosophy

in Materials Science and Engineering

by

Niloofar Shakoorzadeh Chase

2021

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2021

ABSTRACT OF THE DISSERTATION

Physics Based Reliability Analysis of the Silicon Interconnect Fabric

by

Niloofar Shakoorzadeh Chase

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2021

Professor Subramanian Srikantes Iyer, Co-Chair

Professor Dwight Christopher Streit, Co-Chair

Advanced packaging is being driven by the need for computing power, thus, the reliability of these systems needs to be addressed. The wide range of organic and inorganic materials used in these systems results in large coefficient of thermal expansion (CTE) mismatch and ultimately high thermomechanical stresses. Moreover, failure due to moisture ingress in harsh environments and challenges of developing novel encapsulations with high step coverage, high throughput and robust barrier properties is another issue that is receiving a lot of emphasis.

To improve the performance of the integration platforms, we have developed silicon interconnect fabric (Si-IF) and have shown the advantages of Si-IF compared to conventional platforms in terms of performance, power consumption and heat dissipation. In case of the reliability, Si-IF has many

advantages due to the elimination of solder from the platform and the limited number of materials used. All these improvements result in low thermomechanical stresses and elimination of intermetallic compound formation during operation and fabrication in Si-IF.

However, the inability to use conventional passivation in Si-IF, leads to a need for a novel passivation to protect any exposed copper that resulted from misalignment from degradation due moisture ingress. In this work, the use of atomic layer deposition (ALD) to deposit Al_2O_3 thin films for passivation of bonded Si-IF samples was investigated and the effectiveness of this passivation has been verified through experimental testing of fully assembled Si-IF samples for 564 hours under 85%RH and 85 °C testing condition. The change in the electrical resistance of the daisy chains in the samples was less than 3%, showing that this thin film passivation is effective in protecting copper from oxidation.

Moreover, we are developing a sophisticated wafer scale system where Si-IF is at the heart of the platform and is connected to state-of-the-art thermal management unit and power platform, moreover flexible connectors are used to make the connection between Si-IF and the outside world. We investigated use of elastomer buffer layer as stress relaxer to improve the reliability of large wafer scale systems under thermomechanical stress. Finite element analysis (FEA) was used to model the wafer scale assembly where Si-IF is bonded to segmented printed circuit board (PCB) and embedded in Polydimethylsiloxane (PDMS) during temperature cycling between +125 °C/-40 °C. Plastic strain within the solder joints were extracted and lifetime prediction of the assembly was performed using Engelmaier model [1]. These analyses show that addition of the PDMS helps reducing thermomechanical stress and strain levels in solder joints and increase the number of cycles to failure of the assembly.

Moreover, FEA simulation was used to investigate the effectiveness of PDMS buffer layer in damping the input random vibration. The analysis shows that addition of PDMS to the system effectively damps the input random acceleration and consequently, reduces the stresses that the solder joints experience and improves the lifetime of the system. Damping of the input vibration is due to the low natural frequency of the system when PDMS is utilized as the substrate, moreover; PDMS as an elastomer has a higher damping characteristic due to its hyper elasticity properties as compared to PCB.

The dissertation of Niloofar Shakoorzadeh Chase is approved.

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2021

DEDICATION

To my family…

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Unit Process		Material	Process	Process Challenges
Patterning		Positive or negative photoresist	KrF or i-line	Thick resist handling, metrology, die edge exposure
Etch		SF_6, C_4F_8, Ar	Wet etch, silicon DRIE, laser drilling, etc.	Sidewall scallop, top entrance undercut, depth uniformity, etc.
Dielectric liner deposition		SiO_2, SiN_x, polymers, airgap, etc.	SACVD, PECVD, ALD, spin coating, etc.	Step coverage, dielectric breakdown performance
Metallization	Barrier layer	Ta, TaN, Ti, TiN, etc.	PVD, ALD	Step coverage
	Seed layer	Cu, NiB, Co, etc.	PVD, ALD, ELD	Step coverage
	Metal fill	W, Cu, etc.	CVD, ECD	Top underfill, pinch-off voids
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SELECTED PUBLICATIONS

1. **N. Shakoorzadeh**, R. Irwin, Y.T. Yang, H. Ren, S. S. Iyer, "Reliability Considerations for Wafer Scale Systems." 2021 IEEE 71st Electronic Components and Technology Conference (ECTC)
2. Yu-Tao Yang, Chaowei Hu, Peng Zhang, **Niloofar Shakoorzadeh**, Ni Ni, Kang L. Wang, and Subramanian S. Iyer, "Nb-based Superconducting Silicon Interconnect Fabric for cryogenic electronics," Quantum Science and Technology, vol. 6, no. 2, pp. 1-14, 2021.
3. Krutikesh Sahoo, **Niloofar Shakoorzadeh**, Saptadeep Pal, Puneet Gupta, Subramanian S. Iyer, "Copper to Gold Thermal Compression Bonding in Heterogenous Wafer-Scale Systems", 2021 IEEE 71st Electronic Components and Technology Conference (ECTC).
4. **Niloofar Shakoorzadeh**, Subramanian S. Iyer, "Atomic Layer Deposited Al_2O_3 for Encapsulation of the Silicon Interconnect Fabric ", 2020 Semiconductor Research Corporation Technical Conference (SRC TechCon).
5. Y. Yang, C. Hu, J. Green, P. Zhang, **N. Shakoorzadeh**, P. Ambhore, U. Mogera, N. Ni, K. L. Wang, and S. S. Iyer, "Demonstration of Superconducting Interconnects on the Silicon

Interconnect Fabric Using Thermocompression Bonding," 2020 IEEE 70th Electronic Components and Technology Conference (ECTC).

6. **Niloofar Shakoorzadeh**, S. Jangam, P. Ambhore, H. Chien, A. Hanna, S. S. Iyer, "Reliability Studies of Si Interconnect Fabric (Si-IF)", 2019 IEEE 69th Electronic Components and Technology Conference (ECTC).

1. Introduction

1.1 Conventional Packaging

In the advanced packaging and system level integration schemes, such as system-in-package (SiP), interposers and 3-D stacking technologies are primarily focused on improving the form factor and electrical and thermal performance of the system [2]. However, as the packaging and system integration are becoming more complex, the emphasis is on performance and enhancing the reliability of system-level packaging rather than the individually packaged components [2]. Moreover, the increasing complexity of the structures (such as addition of interposers, 3D stacking, etc.) combined with increasing power consumption and higher bandwidth requirements, result in a significant increase in the reliability challenges of the package. Figure 1.1 is a schematic of today's state-of-the-art packaging scheme showing large hierarchy and high complexity.

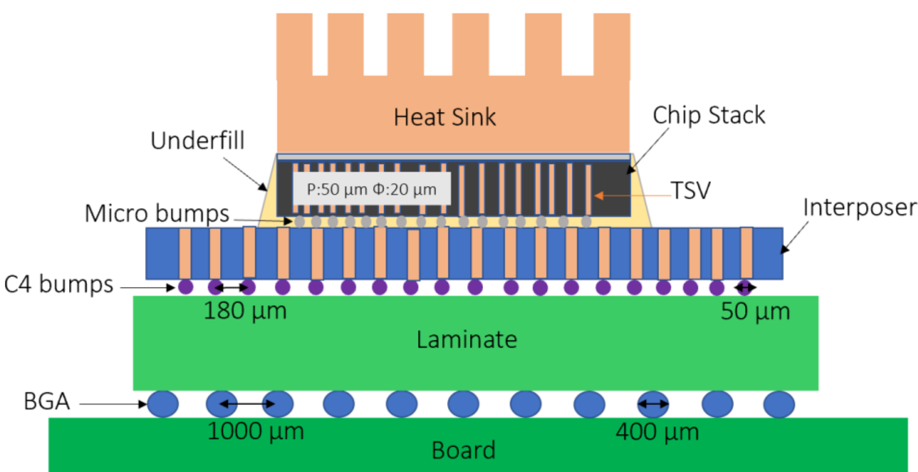

Figure 1.1 a schematic of today's packaging scheme. Due to the need for increasing density and finer pitches, packaging platforms are becoming more complex, introducing new reliability challenges [2].

Due to increasing requirement for higher speed and number of I/Os, solder joints in the packaging platforms are shrinking in size. However, scaling of the solder bump pitch lags CMOS nodes that follow Moore's law [3]. As Figure 1.2 illustrates, device nodes scaled almost 1000X since 1960s however, bump pitch scaling for the same time is roughly 5X.

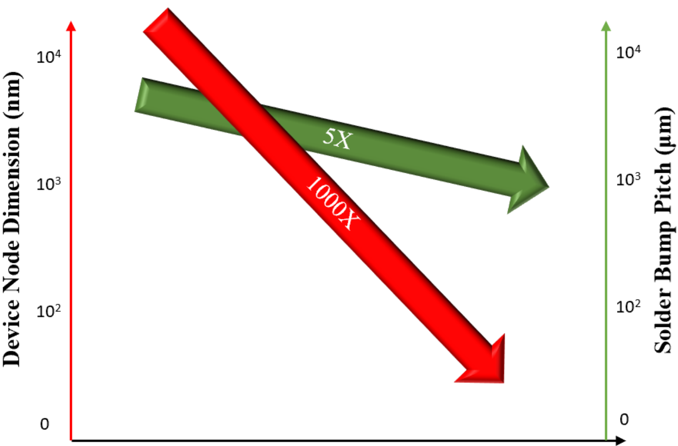

Figure 1.2 device node scaling and solder bump pitch over time. In the late sixties, node sizes were about 15 µm , and bump pitch was about 400 µm . Currently, these numbers are 5 nm and 50 µm respectively [3].

This gap between scaling of Si feature and bump pitch and overall packaging feature size has resulted in numerous mitigations to accommodate the I/O and power requirements. Which in turn has resulted in complex assemblies with various materials of vastly different and/or anisotropic properties. Moreover, solder ball joint scaling introduces new reliability challenges in board level packaging as well as system level packaging due to the fact that the volume fraction of intermetallic compound (IMC) that forms during operation and fabrication increases. Furthermore, addition of low-k dielectric to reduce cross talk and interline capacitance, leads to mechanical stability challenges in the assembly [4], high thermomechanical stresses in the package may transfer to low-k/Cu in the chip and result in chip package integration (CPI). CPI is one of the biggest challenges in the today's conventional packaging.

Also, with increase in the overall size of the 3D assemblies, the thermomechanical stresses in the corner solder joints increases significantly. That is another major challenge in thermomechanical reliability of the solder joints.

1.2 Silicon Interconnect Fabric

To simplify the packaging hierarchy, we have developed a new packaging platform known as the silicon interconnect fabric (Si-IF) [5]. In this integration platform, we have eliminated the laminate and replaced the PCB with a Si wafer. Unpackaged dies are integrated directly on this prefabricated Si wafer using solderless Cu-Cu thermal compression bonding (TCB) [5]. The Si-IF enables the integration of different types of dielets and fine interconnect/interpillar pitch (≤10μm) and small inter-dielet spacing (≤30μm). These fine pitches are not attainable with conventional controlled collapse chip connection (C4 bumps). Moreover, the number of materials in the Si-IF assembly is limited and no underfill or overmold is used, thus, the CTE range of the assembly is much tighter than that of the conventional packaging. Also, due to fine pitch interconnects and short inter dielet links in Si-IF, high bandwith communication with low latency and low power consumption is possible [5]. Figure 1.3 shows 371 heterogeneous bonded dies with different sizes. Inter-dielet spacing was measured to be around 100 μm, Si substrate and dies were fabricated at UCLA cleanroom [6].

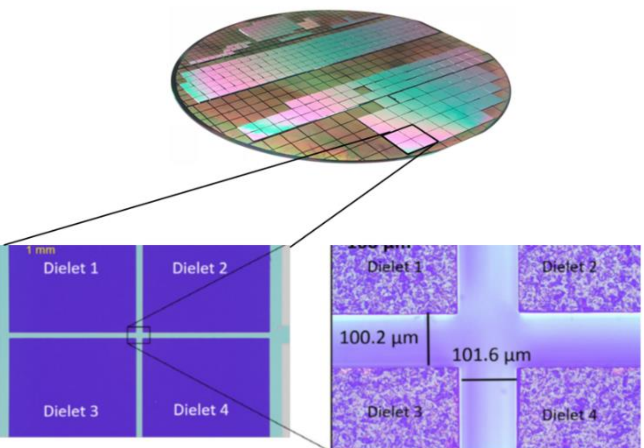

Figure 1.3 assembled dies (1x1 mm^2 to 5x5 mm^2) at ≤100 µm inter-dielet spacing on a 100 mm Si-IF [6]

Si-IF has many advantages over conventional packaging platform, specifically in terms of reliability due to different factors including elimination of solder joints and organic materials, limited number of materials in the system and ability to maintain relatively low temperature during bonding which in turn reduces residual stresses and improves reliability.

1.3 Objective of This Work

As mentioned earlier, Si-IF offers numerous advantages over conventional packaging both in performance and reliability aspects. However, as a novel system, Si-IF reliability and its failure mechanisms need to be investigated and fully understood for lifetime prediction in field use. One example is the degradation of the Cu pillars exposed to humidity since there is no underfill or overmold to protect the Cu from oxidation. Thus, there is a need for a novel passivation with unique requirements since the passivation happens after all the active dies are already integrated into the system. The passivation should have enough step coverage to be able to penetrate through the gap between bonded dielet and substrate and reach the pillars in the center under the dielet. Furthermore, the deposition should be done at low temperature (<200 °C) to prevent degradation of temperature sensitive dielets. Another consideration is the material properties of the passivating

film and its adhesion to Cu and SiO_2. If the CTE mismatch between the passivating film and the other material in the system is very large, that may result in delamination and cracking of the passivation due to thermomechanical stress.

In this work, an extensive study has been performed to select and fabricate a suitable passivation film for bonded Si-IF samples (*i.e.*, Si-IF samples with integrated dies). To understand the robustness of the passivation film, x-ray powder diffraction (XRD) was used to measure oxide formation in blanket Cu samples passivated with different thin films (organic, organic/inorganic multilayer, and inorganic) with various thicknesses following humidity testing. Step coverage of the thin films was investigated using focused ion beam (FIB) cross sectioning. From the FIB cross section images, it was concluded that atomic layer deposition (ALD) process met the step coverage requirement needed for Si-IF assembly. Humidity testing was performed on bonded and passivated samples and change in electrical resistance of the sample during testing was measured. Energy-dispersive X-ray spectroscopy (EDS) was used to study the uniformity of the film under the die and the deposition process was optimize.

Moreover, experimental temperature cycling study was done on passivated and bonded samples to understand the effect of thermomechanical stresses on the Cu pillars. Change in the electrical resistance of the sample was measured during 100 cycles of temperature cycling in accordance with JESD22-A104 [7].

Additionally, finite element analysis was utilized to study the failure mechanisms of Si-IF under random vibration, and the role of the addition of an elastomer on damping the input acceleration into the system. This study is a crucial step to better understand and improve the reliability of Si-IF when it is used as a major part of a wafer scale system.

Thermomechanical analysis of such wafer scale system was done using finite element analysis to identify the effect of the size of the PCB board attached to Si-IF as well as effect of solder joint alloy type of the amount of plastic deformation within the solder joint during temperature cycling. This data was used for lifetime estimation of the system using Coffin Manson equation.

1.4 Organization of the Dissertation

This dissertation is organized as follows: Chapter 2 is a summary of today's packaging and reliability challenges facing each technology as well as the industry outlook and requirements in terms of bump pitch and performance for the next decade. Chapter 3 is a detailed description of the Si-IF and its fabrication process, factors that affect the reliability of the system, and the wafer scale system proposed suing Si-IF at its heart. Chapter 4 is a detailed report on the development of a passivation for the Si-IF. Chapter 5 describes the thermomechanical stresses and experimental results of Si-IF temperature cycling tests. Chapter 6 is dedicated to understanding failures related to vibration and mitigation techniques for damping. Finally, conclusions and a future outlook of this work are given in Chapter 7.

2. Reliability Challenges in Today's Packaging

Electronic packaging consists of several different components that each play a crucial and distinct role. These components are as followed:

1- Integrated circuit (IC) chips (bare dies)

2- The interconnects that can be on chip or off chip for power delivery and signal transmission. These interconnects are usually solder alloys, however, copper interconnects with or without solder cap are also being used.

3- The enclosure or the encapsulation to protect the dies and interconnects from degradation due to moisture ingress and other aggressive ions in the environment. Thermoset polymers such as underfill and overmold are used for encapsulation and passivation.

4- Cooling system for thermal management, usually in the form of a heat sink made from Cu.

5- The power supply and any required shielding from electromagnetic interference [8].

From above description, it is clear that the electronic packaging is a material intensive system. Generally, electronic packaging materials are divided into three categories, metal-based, ceramic-based, and polymer-based materials [8].

Metal-based packaging materials have high thermal conductivity, high strength, and robust reliability. This class of materials is primarily used within electronic packaging for military and aerospace applications. Ceramic-based packaging materials benefit from a low dielectric constant and CTE and similar to metal-based materials, exhibit high mechanical strength and thermal conductivity. Ceramic-based materials are thermally stable and moisture resistant and are mainly used in high frequency applications. Polymer-based packaging materials are composed of polymer

and fillers such as silica, they are very lightweight and cost effective, provide acceptable encapsulation properties, and are easy to process [9].

In this chapter, we review the main types of conventional packages and interconnects, and the associated reliability challenges.

2.1 Timeline

The first IC packaging was invented in mid 1960s at Fairchild consisting of a 14-lead ceramic Dual-in-Line Package (DIP) with two rows of pins [9]. The earliest types of DIP housings were made from ceramic which would provide robust reliability properties. These packages were widely used in aerospace and defense applications. Later, the ceramic encapsulation was replaced by plastic material which reduced the price of packaging and allowed DIP to become more widely used. At the same time, IBM had a different approach for integrating a single chip on to the substrate called solid logic technology (SLT) module [10]. SLT utilized a thick film or paste on an alumina substrate and was primarily used as an inexpensive connection for single device chips to the next level of packaging. Later, monolithic system technology (MST) was introduced, where due to demand for higher density of connections, the interconnect technology was changed to control collapsed chip contact (C4) [10]. The substrate technology remained the same until chip terminal spacing became too small for thick film technology [10]. The next evolution in packaging and integration was the development of metalized ceramic (MC) module by IBM which utilized a composite of Cr/Cu/Cr thin film on a ceramic substrate [9]. Further advancement came in the form of a multi-chip module (MCM) in which multilayer ceramic (MLC) substrate was introduced [9]. Figure 2.1 shows 9-chip MCM in alumina/molybdenum technology [10]. The MLC substrate consisted of twenty-three molybdenum metalized alumina layers with a total thickness of 4 mm.

The top six layers were used for signal lines redistribution from the chip pad grid and would allow for testing and engineering changes. The bottom five layers were typically used for power distribution as well as signal redistribution to pin grid [11]. Moreover, vias were used to connect metal layers to each other within the substrate [12]. Another improvement that happened after the introduction of MCMs was change in the thermal management method. Up until then, heat was conducted through the pins from the chip to the substrate where it would dissipate, with increase in the size of the modules and power consumption, heat dissipation techniques changed to using a heat sink on the backside of the chip. These modules were commonly known as thermally conductive modules (TCM). Table 2-1 is a summary of the earlier packaging technologies with highlighting key features and materials used in each of them [12].

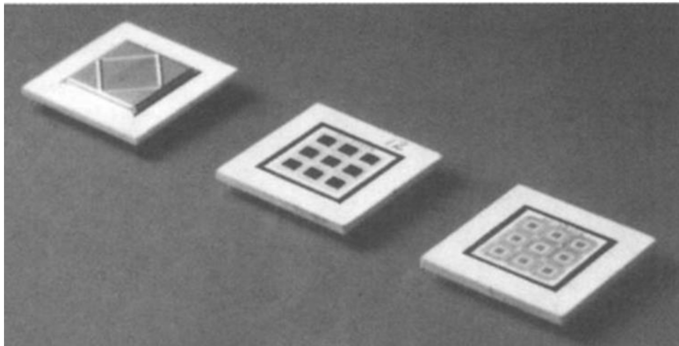

Figure 2.1 9-chip MCM in alumina/molybdenum technology (Adapted with permission from Elsevier) [96].

Table 2-1 *Ceramic Modules Development (IBM system)* [12].

	SLT	MST	MC	MCM	TCM
Starting Year	1964	1970	1975	1979	1980
Ceramic	Pressed 96% Al_2O_3	Pressed 96% Al_2O_3	Pressed 96% Al_2O_3	Doctor Bladed 92% Al_2O_3	Doctor Bladed 92% Al_2O_3
Size	11.6 x 11.6 mm		28 x 28 mm 36 x 36 mm	35 x 35 mm 50 x 50 mm	90 x 90 mm
Metallurgy	Au/Pt Ag/Pd	Au/Pt Ag/Pd	Cr/Cu/Cr Thin Films	Cr/Cu/Cr Thin Films	No Paste Ni/Au Plating
Max. No. of Layers	1-2	1-2	1	23	33
Max. No. of Chips	About 7 (Single Devices)	About 4	About 4	9	133

2.2 Three-Dimensional Integration

To overcome physical, technological, and economic limitations related to planar integrated circuits (ICs), and to further extend Moore's Law, three-dimensional (3D) integration technology was developed [13]. 3D integration refers to stacking of materials, technologies, and other functional nodes vertically with the use of various connections to form a highly integrated system [13]. There are a few major approaches developed to enable 3D integration which include: chip on chip (CoC), chip on wafer (CoW), wafer on wafer (WoW), and system on wafer (SoW). The technologies that enable these approaches include through silicon via (TSV), and wafer thinning and dicing. 3D integration provides numerous advantages over 2D packaging, including increased performance and bandwidth, smaller form factor, and ability for heterogeneous integration. Figure 2.2 shows a comparison of a 3D integration solution and a comparable 2D integration platform for a Samsung memory. 3D integration provides a 35% reduction in package size and a 50% reduction in power consumption, while bandwidth is increased by 8X [14].

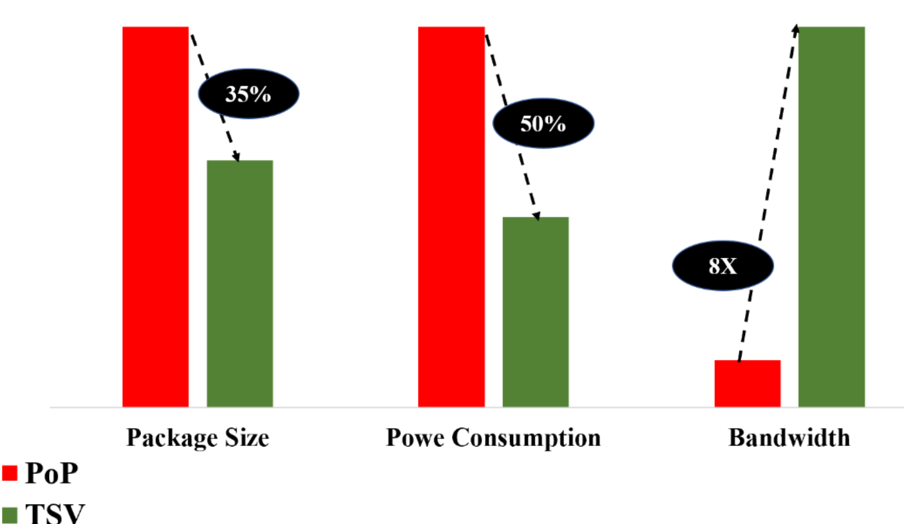

Figure 2.2 Comparison of 3D integration platform vs. a comparable package on package (PoP) [14].

Table 2-2 Comparison of different chip stacking techniques [13]

	CoC	CoW	WoW
Known good dies (KGDs)	Yes	Yes	No
Flexibility	High	High	Low
Throughput	Low	Mid	High

As can be seen from Table 2-2, in the CoC approach, known good dies are used for stacking which results in higher yield, WoW has the highest throughput, and the CoW is in between the other two technologies in terms of throughput [13].

Two types of 3D integration exist, 3D packaging and 3D ICs. In the case of 3D packaging, the process relies on utilization of traditional interconnects such as wire boning or flip chip. However, in 3D IC integration platform, TSVs are used to make the connection between the different layers [13]. Figure 2.3 is a schematic of 3D packaging where wire bonding (a) or ball grid array (BGA) solder balls (b) are used for stacking. Figure 2.4 is a schematic of a 3D IC integration solution developed by Qualcomm and Amkor Technology. Interconnects are micro pilar grid array (MPGA) with a minimum pitch of 40 µm [15].

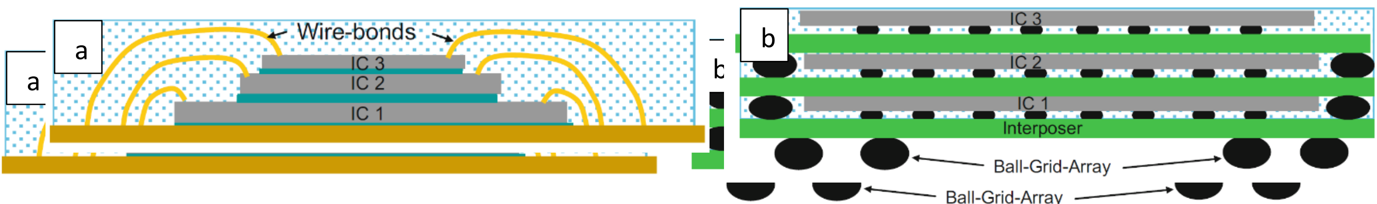

Figure 2.3 3D packaging schemes (a) using wire bonding and (b) BGA solder joints [13].

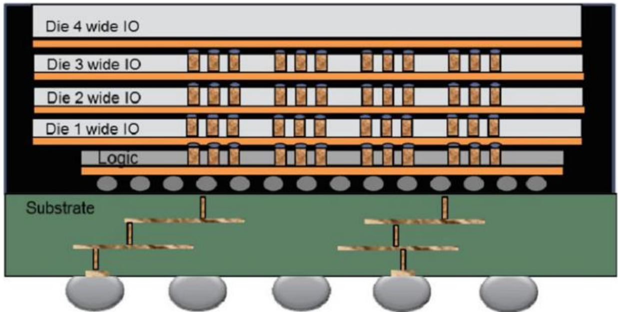

Figure 2.4 schematic diagram of stacked dies in wide IO memory demonstrated by Qualcomm and Amkor Technology [15].

As previously mentioned, process technologies that enabled 3D integration include wafer thinning and dicing, chip stacking, and TSV. To better understand the limitations and reliability challenges associated with 3D integration, it is crucial to fully understand the processes related to each of these technologies. Thus, in the next sections an overview of these processes is presented.

2.2.1 Wafer Thinning and Dicing

Wafer thinning is utilized to expose the TSVs from the backside of the wafer to allow for electrical connection to the substrate. There are different approaches for wafer thinning, one of these approaches is to bond the wafer face down to the base wafer or stack of wafers before thinning, the base wafer(s) are used to support the thinned wafer. This approach is best suited for WoW technologies. The other approach is to thin the wafer containing TSVs before bonding or dicing, this approach is used in CoC and CoW [13]. The limitation of this approach is the susceptibility of the thinned wafer to cracking due to lack of mechanical strength, thus a temporary wafer handler is bonded to the wafer through a temporary adhesive [16]. Decrease in the thickness of the wafer may result in increase in the wafer warpage, thus; some stress relief processes are usually used to reduce the warpage and improve the yield [17]. Figure 2.5 illustrates major processes that are used to relief the stress in the thinned wafers [13]. These processes remove the

damaged layer from backside of the wafer that is remained from fine grinding during thinning process and a mirror polished surface is achieved which improves the wafer strength and helps reduce the wafer warpage [18].

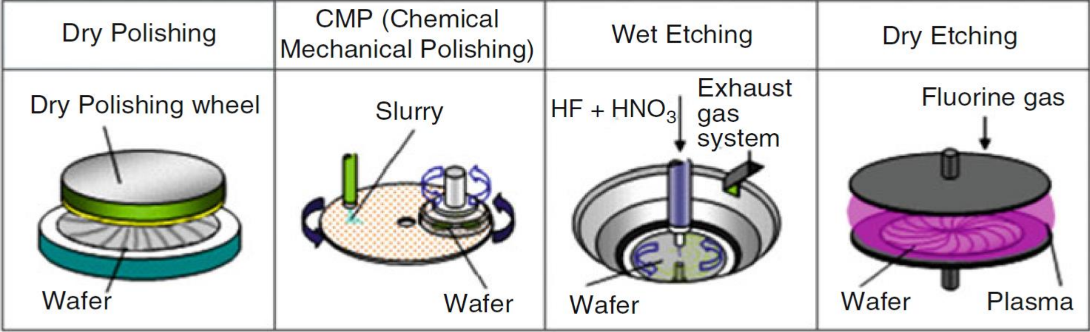

Figure 2.5 major stress relief processes [13].

Wafer dicing is the process of singulation of dies from wafer. There are a few techniques for dicing, including mechanical sawing and scribing. These conventional processes may introduce defects into the dies, thus a more robust technique known as stealth dicing has become a common way for die singulation. Stealth dicing utilizes focused laser beam that is of the wavelength to permeate into the silicon wafer [13]. Stealth dicing provides important advantages over conventional dicing methods, including low kerf loss, high speed dicing, and higher yield [13].

2.2.2 Wafer and Chip Stacking

Wafer and chip stacking are a crucial step to enable 3D integration in the z direction. Stacking is achieved either by CoC or CoW and there are multiple methods for bonding as listed in Table 2-3 [13]. The most common techniques for stacking are the metal-metal methods, even though these methods generally suffer from mechanical stability issues [19]. Underfill is typically used to mitigate mechanical stability issues related to metal-metal stacking. The application of underfill adds to the complexity of the process and introduces further reliability issues such as thermomechanical stresses. Usually, underfill application follows a reflow process for all the dies

at the same time. Underfill resin application relies on capillary flow to reach underneath the dies, scaling of the interconnects, and reduction of the pitches and the gap between the dies (or dies and wafer) hinders the capillary flow for underfill application [20]. Table 2-4 summarizes underfill materials currently in use with their advantages and disadvantages [13]. Wafer level underfill (WLUF) provides key advantages over conventional underfill and allows for finer pitches in stacking to be achieved. Moreover, no flux is required in WLUF process which in turn eliminates the flux cleaning step.

Table 2-3 Different CoC and CoW stacking technologies, advantages, and challenges [13].

Bonding approach	Materials	Advantages	Challenges
Metal–Metal	SnAg (C4)	Direct electrical connection between two wafers	Not suitable for multiple wafer stacking due to thermal budget limits
	Au/Sn	Direct electrical connection, good wetting, etc.	Mechanical stability
	Solid–liquid interdiffusion(SLID) Cu–Sn	Direct electrical connection, good wetting, etc.	Limited thermal stability
	Cu–Cu thermal compression bonding	Direct electrical connection, good for wafer-scale bonding, high bonding energy	Requires accurate alignment and clean metal surface, mechanical stability concern
Hybrid	Cu-ILD/Cu-BCB thermal compression bonding	Direct electrical connection, better mechanical stability	Requires accurate alignment and clean metal surface
SiO_2 or adhesive	SiO_2–SiO_2	Less thermal and mechanical stress, better reliability, and scalability	No direct electrical connection

Table 2-4 Comparison of underfill materials and their pros and cons [13].

Approach	Underfill Materials	Advantages	Challenges
Conventional mass reflow	Capillary underfill (CUF)	High-throughput batch process for mass reflow	Requires cleaning process to remove flux residue
Thermal compression Bonding (pre-applied underfill)	Nonconductive paste (NCP)	No flux, good scalability for fine pitch interconnect	Challenging to achieve 100% electrically and metallurgically good joints and void-free underfill
	Wafer-level underfill (WLUF)	Reduced stress and CPI risk, good throughput wafer-level process, limit creeping issues for thin die	

2.2.3 TSV Integration

TSV can be fabricated at different stages of microelectronic processing. It can be done before or after the front end of the line (FEoL), after back end of the line (BEoL), after wafer thinning, etc. [13]. TSV fabrication after BEoL process, which is also known as via middle, is the most common fabrication process since it has less impact on active devices and provides flexibility for BEoL routing [13].

The most significant challenges for fabrication and reliability of TSVs includes continuity of Cu seed layer, via filling without voids for high aspect ratio vias, and planarization of the Cu and surrounding dielectric film [13]. Table 2-5 lists important process steps and challenges for TSV formation process [13].

Table 2-5 major TSV fabrication steps, materials used and challenges [13].

Unit Process		Material	Process	Process Challenges
Patterning		Positive or negative photoresist	KrF or i-line	Thick resist handling, metrology, die edge exposure
Etch		SF_6, C_4F_8, Ar	Wet etch, silicon DRIE, laser drilling, etc.	Sidewall scallop, top entrance undercut, depth uniformity, etc.
Dielectric liner deposition		SiO_2, SiN_x, polymers, airgap, etc.	SACVD, PECVD, ALD, spin coating, etc.	Step coverage, dielectric breakdown performance
Metallization	Barrier layer	Ta, TaN, Ti, TiN, etc.	PVD, ALD	Step coverage
	Seed layer	Cu, NiB, Co, etc.	PVD, ALD, ELD	Step coverage
	Metal fill	W, Cu, etc.	CVD, ECD	Top underfill, pinch-off voids
Planarization		Cu, Ta, SiO_2, SiN, SiCN, etc.	CMP	Copper erosion and dishing

2.2.4 3D Integration Limitations

Although 3D integration provides the necessary and needed benefits, and the fact that the process challenges related to TSVs and wafer thinning are well understood and mitigated in most cases, there remain limitations which may render 3D integration a complex solution for the ever-scaling platforms. Some of these limitations are as follows [13]:

1. Cost: the cost of 3D integration is not comparable with Moore's law scaling, however; since the largest driver for growth of the semiconductor industry is the mainstream consumer market, it is crucial to account for the associated cost related to TSV formation. Moreover, as integration platforms scale up, the complexity and the cost of the 3D integration solution also increase.

2. Yield and Test: As the number of processing steps increases, the risk of defects increases as well. Yield and testing are related and increasing testing may adversely affect the throughput and increase the cost.

3. Thermal and Power: Stacking of dies in the z direction leads to heat buildup and this heat must be extracted through the stack. Moreover, power delivery could be a challenge in the stacked dies and needs to be managed carefully.

4. Design Complexity: to fully enable 3D integration benefits, sophisticated design tools and techniques are required for thermal management, and routing. Furthermore, mitigation of the thermal and mechanical issues related to solder joints require new materials and techniques which add to the complexity.

2.3 Interconnect

One of the most important parts of any packaging platform is the interconnect, its type, material, and size play a crucial role in the mechanical and electrical reliability of the entire system. To meet increasing demand for pitch scaling and higher bandwidth requirements, the interconnects are changing drastically, thus, it is beneficial to study the current trend and outlook of the interconnect and understand the associated reliability challenges.

Flip chip (FC) is the most widely used interconnect technology and it comes in different bump types, bump material, and package platforms. The flip chip assembly consists of three major steps 1) bumping the dies, 2) attaching the dies face down to the substrate or board, and 3) underfilling.

To mitigate issues such as electromigration, and reliability and to accommodate for fine pitches, interconnects are evolving toward direct Cu-Cu bonding or Cu nano paste [21]. Few factors play a role in selecting the interconnect technology including, bump pitch, power, frequency requirement, and the die size [21]. Table 2-6 is a summary of current FC technologies and Cu/Cu thermal compression bonding process [21].

There exists a need for emerging technologies for pitches below 20 μm that not only satisfy the pitch requirement, but also do not add to the complexity of the integration platforms and do not have adverse effects on the reliability of the system. The interconnect technologies that are under development are summarized in Figure 2.6 with approximate number of input/output (I/O) for each solution [22].

Table 2-6 Summary of the evolution of FC interconnect technologies and outlook for interconnect technology [21].

	C4	C2 (Chip Connect)	TC/LR (Local Reflow)	TC
Schematic Diagram				
Major Bump Pitch Range at Application	> 130 µm	140~ 60 µm	80~ 20 µm	< 30 µm
Bonding Method	Conventional reflow	Reflow with Cu pillar	Thermal compression with Cu pillar	Thermal compression
Bump Metallurgy	Solder (SnAg or SnAgCu)	Cu+ solder (SnAg or Sn)	Cu+ solder (SnAg or Sn) cap	Cu
Bump Collapse	Yes	No	No	No
Underfill Method	- Capillary - No flow	- Capillary - No flow - Wafer level	- No flow - Wafer level	- No flow - Wafer level

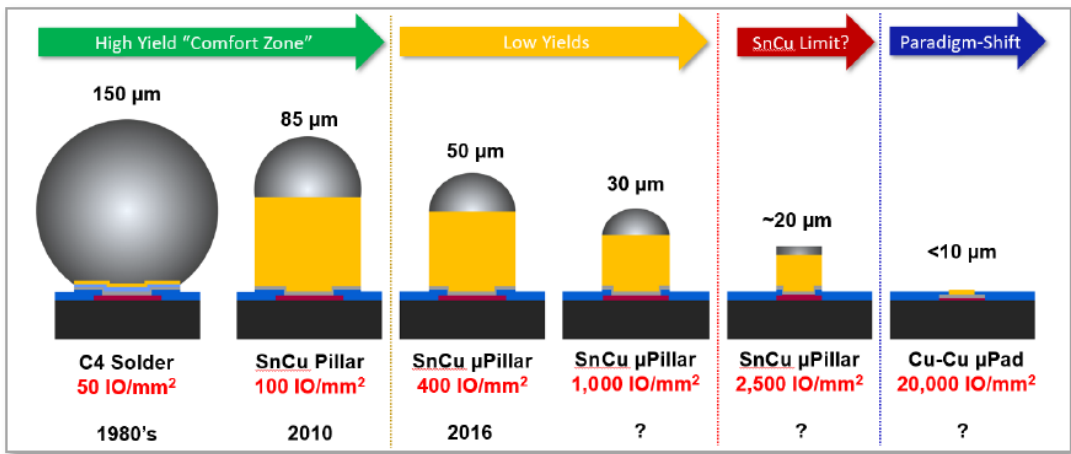

Figure 2.6 trend for interconnect technologies [22].

2.4 Substrates

Substrates are one of the most expensive components in electronic packaging and at the same time, most of the performance limitations of the package arise from the substrate. Ceramic substrates are very expensive but provide higher design freedom in terms of integration of vias, stacking, etc. [13]. The disadvantages of ceramic substrates are related to their high dielectric constant. On the other hand, PCBs have lower dielectric constant and are much cheaper. However, the biggest challenge related to PCB is the large CTE mismatch between them and the Si dies [13].

From the advent of ICs, one of the biggest challenges has been the issue of how to connect the microscopic pins on the dies to the macroscopic I/O terminals. To solve this issue a tiered packaging scheme was utilized which is still in use to this date. The levels of packaging are as follows:

- First level packaging: to connect the terminals of the die to larger terminals on a ceramic carrier or substrate to allow for handling of the dies. Typically dies are sealed hermetically or semi hermetically or protected with a lid.

- Second level packaging: where the substrate wiring is further fanned out by soldering the substrate terminals to plated through holes (PTH) on the printed wiring boards (PWB).

- Third level packaging: where connecters on the PWB side are connected inside to a computer frame or chassis [13].

At the beginning, the role of packaging was to mitigate the challenges related to size transformation. Dies were sitting on ceramic substrate with similar CTEs, the CTE difference between the ceramic substrate and PWB was not a concern due to the small size of the substrates and flexible connection between substrate and PWB through pins. However, as the demand for I/O

and density and subsequently the substrate size increased and pins were replaced by stiffer solder joints, the thermomechanical stresses within the solder joints became a big challenge. These stresses are especially high for the solder joints at the farthest distance from the neutral point (DNP) [13].

Moving from ceramic substrates to organic substrates resulted in the challenge to shift to the DNP of the die and substrate due to the CTE differences. Introduction of underfill mitigated the high levels of thermal stresses by reinforcing the mechanical stability of the solder joints. Thus, the term chip package interaction (CPI) was introduced which recognizes that the effect of material properties is the crucial factor in the reliability of electronic packaging. Table 2-7 is the roadmap for substrate interconnect until 2034, despite the high price and added complexity of 3D integration and interposers, Si-based substrates provide the best scaling option [21].

Table 2-7 interconnect scaling roadmap for organic and Si substrates [21]

Materials	Application	Features (μm)	2020	2021	2022	2025	2028	2031	2034
Organic laminate	FC-BGA	Min. Bump Pitch	100	90	90	80	80	70	70
		Min. Line width/space	9/12	8/8	8/8	5/5	5/5	5/5	5/5
		Min. μVia diameter	50	40	40	30	30	20	20
	Chiplet (Fanout, Organic interposer)	Min. Bump Pitch	50	45	45	40	40	30	30
		Min. Line width/space	2/2	1.5/1.5	1.5/1.5	1/1	1/1	0.5/0.5	0.5/0.5
		Min. μVia diameter	30	20	20	10	10	5	5
Silicon	Chiplet (Si interposer, 3D)	Min. Bump Pitch	40	35	35	30	30	20	20
		Min. Line width/space	0.6/0.6	0.6/0.6	0.6/0.6	0.5/0.5	0.4/0.4	0.3/0.3	0.2/0.2
		Min. μVia diameter	0.6	0.6	0.6	0.5	0.4	0.3	0.2

2.4 Interposers

Interposers were the key enablers of 3D packaging platforms; the main role of the interposer is to redistribute the fine pitch of the micro bumps to the coarser pitches of the C4 bumps. Figure 2.7 is a schematic of a 3D integration platform with main parts labeled, including the interposer. In terms of materials, interposers can be divided into three groups, silicon interposers, glass interposers, and organic interposers. Each class has its own advantages and unique challenges both for processing and reliability.

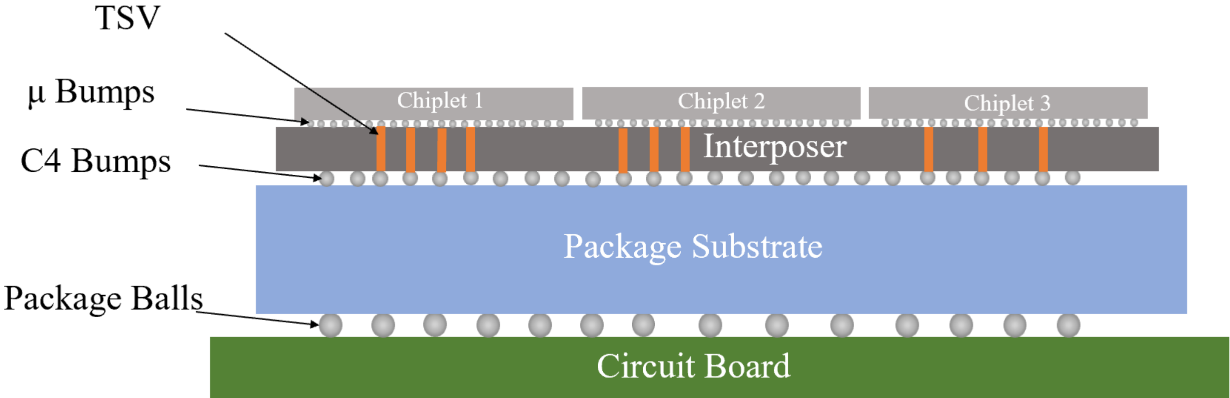

Figure 2.7 schematic of a 3D integration platform.

Silicon interposer allows for high I/O density. However, there are a few limitations to silicon interposers. The first is performance limitation that are related to TSV profiles and changes that have been made in thermal management systems to alleviate thermal stresses [23]. Cost is another limiting factor for Si interposers, as the demand for I/O density increases, Si interposers become more complex and more expensive [23]

Organic interposers are an alternative to Si interposers due to the lower cost associated with them. They are cost effective since their fabrication process is very well stablished and utilizes more traditional processing steps. The challenges in using organic interposers stem from their

mechanical properties and coarser I/O pitch as compared to Si interposers [23]. That's why these interposers are generally used in applications that do not require high I/O density.

Similar to organic interposers, glass interposers are another alternative to Si. Glass interposers provide finer I/O pitch compared to organic interposers and also benefit from lower cost as compared to Si interposers [23]. The cost efficiency of glass interposers is due to lower cost of material as well as their availability in panel form which allows for achieving higher yield [23]. However, the challenges of glass interposers are associated with surface defects that may be introduced during fabrication which may act as stress concentration points and result in crack propagation, difficulty in through glass via (TGV) formation, and material thermal properties of glass with lower thermal conductivity compared to Si [23].

From this short summary about interposers, it is clear that despite the benefits of interposers, specifically ability to significantly increase the I/O density and reduce the interconnect pitch in the first level packaging, each of these interposers introduce a unique challenge to the integration platform and results in complexity of the system.

2.5 Underfill

Underfill is used to alleviate and redistribute thermomechanical stresses within the solder joints that accumulate due to CTE mismatch between the dies and the organic substrate [24]. Thus, it is important to understand the role of underfill in electronic packaging and advances that have been made to mitigate issues associated with it.

The conventional underfill is applied after FC interconnects are fabricated. The underfill materials rely on capillary flow to go through the gap between the die and the substrate, hence they are termed capillary underfill (CUF) [24]. A typical CUF is a mixture of organic resin, inorganic

binder, and a hardener that facilitates cross linking during curing step. Other additives such as latent catalyst might be also added to improve the pot life and reduce the curing time [24]. The inorganic binders are typically micron size silica that help with improving the material properties of the cured underfill including, lower CTE, low moisture uptake, and higher young's modulus [24]. Due to the slow and sometimes incomplete capillary flow, void formation and inhomogeneity of resin/filler system may occur. These issues become a bigger challenge as the size of the die increases and the gap between the die and the substrate decreases [24].

As electronic packaging moved away from lead solder alloys, due to environmental issues, underfill for FC applications had faced new challenges related to compatibility with higher reflow temperature [24]. Higher reflow temperature results in faster degradation of materials due to higher thermal stresses and higher moisture uptake. Thus, it is crucial to improve the mechanical stability, toughness, adhesion to different surfaces, and CTE of the underfill.

One of the most used lead less solder alloys is the Sn/Ag/Cu (SAC) alloy with different Ag and Cu content. SAC alloys have higher young's modulus as compared to PbSn solders; thus, they do not deform plastically as much. Moreover, their creep behavior is quite different from PbSn solders [24] . The creep level of SAC alloys is significantly lower at lower stress levels and significantly higher at higher stress levels, as compared to PbSn solders. Consequently, temperature cycling with a wide temperature range and small dwelling time will induce larger creep deformation in SAC alloys, and thus underfill materials should provide a more robust protection compared to underfills used for PbSn solder alloys [24].

Delamination after higher reflow temperature is another common failure mode which is attributed to materials with lower filler content. Underfills with higher filler content have lower

CTE, higher Young's modulus, and lower moisture uptake and thus, better adhesion to lead free solders [25].

Another challenge is related to introduction of low-k interlayer dielectric (ILD) materials to reduce interconnect delays. Compared to traditional dielectric such as SiO_2, low-k dielectrics have higher CTE, they are brittle, and usually porous. Due to the CTE mismatch between low-k dielectric and Si, large thermomechanical stresses build up at their interface [24]. Thus, the role of the underfill becomes even more important since it should not only protect the solder joints by stress distribution, but also the low-k dielectric and its interface. Optimization of underfill material properties such as glass transition temperature (T_g), CTE, and Young's modulus is crucial to achieve the right underfill for these application [24].

These new challenges have resulted in development of some alternatives to CUFs, even though CUFs are still the most common type of underfill being used. A few of these alternatives are described below.

- No flow underfill (NUF): the idea of an underfill that does not rely on capillary flow was first introduced in 1992 [26]. In this type of underfill, instead of dispensing it after the interconnects between dies and substrates are formed, the underfill is dispensed on the substrate before bonding the die. Subsequently the die is aligned and bonded to the substrate and then the assembly is heated to reflow the solder joints and cure the underfill simultaneously (Figure 2.8) [24]. This type of underfill has few advantages over conventional CUF, it eliminates flux dispensing and cleaning steps, removes the capillary flow for the underfill, and moreover, combines the reflow and curing steps [24]. The two crucial properties required for NUF are latent curing and built-in flux properties. Even though NUF provides advantages both in process simplification and elimination of capillary flow, there are major challenges in developing a good, reliable process. One of the biggest challenges in NUF processing is void formation in the underfill due to outgassing of the underfill, moisture from the board, or voids trapped during the assembly [24].

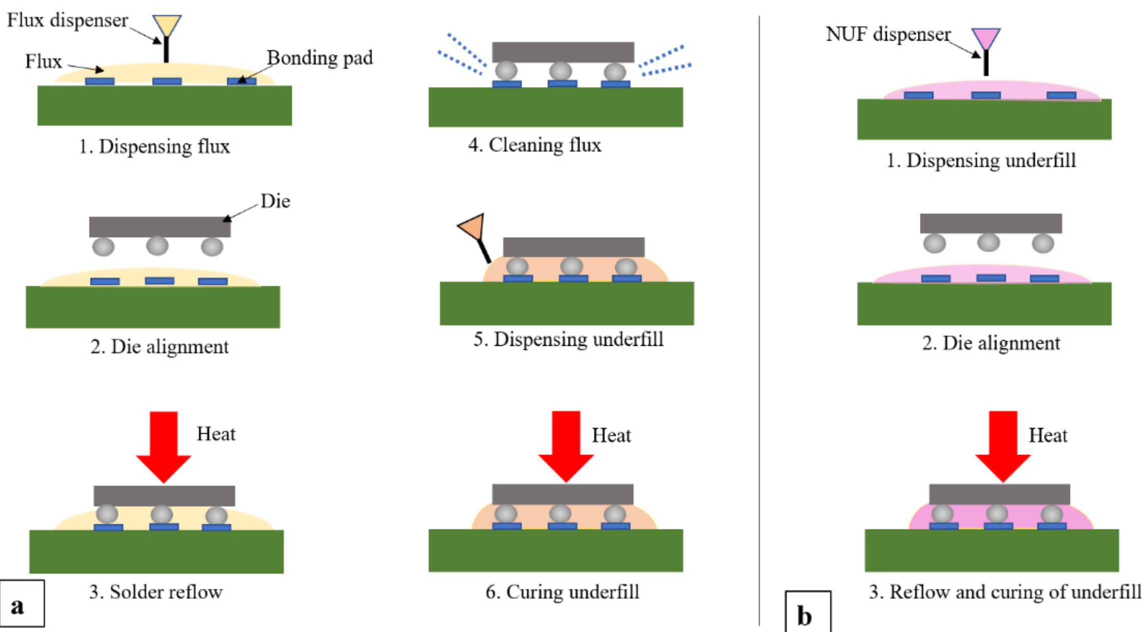

Figure 2.8 comparison of FC process with (a) conventional underfill and (b) no flow underfill [24].

Void formation, especially near the solder joints, may result in early failure due to stress concentration, delamination of the underfill, or solder extrusion [27]. The parameters that affect the underfilling voiding include the interconnect pitch, die placement force, speed, and reflow temperature profile [28]. Void formation becomes a bigger challenge when the assembly complexity increases and there is a temperature gradient across the assembly due to difference in die sizes [28].

The major reliability challenges related to no flow underfill have been studied and the main failure modes are attributed to large CTE mismatch among the solder alloy, underfill, and the board, cracking of the underfill due to low fracture toughness combined with high CTE, and delamination of underfill and passivation [24].

- Wafer level underfill: because of the reliability concerns related to no flow underfill due to high CTE and low fracture toughness, wafer level underfills have been developed as a solution [24]. Wafer level underfill is a surface mount technology (SMT) where the underfill is applied to a bumped or not bumped wafer, subsequently the underfill is partially cured (known as B-staged) before dicing the wafer. After wafer dicing, every die can be placed on the substrate using a conventional SMT process. Figure 2.9 is a schematic of the wafer level underfill application [24]. The advantage of wafer level underfill is the low cost and improved reliability. However, the challenges with this type of underfill are related to uniformity of the underfill film on the wafer, B-staged properties of the underfill, storge of the diced dies, storage life, and wettability of the solder with underfill present [24].

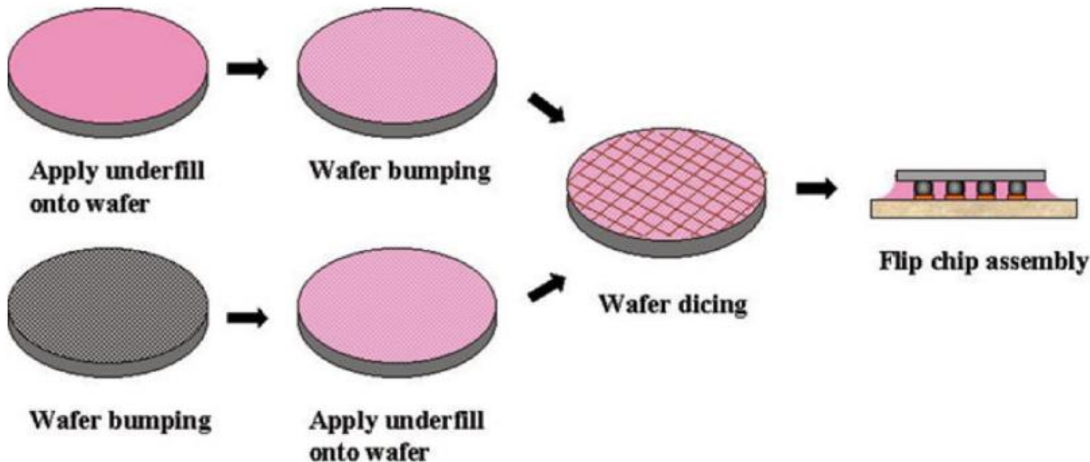

Figure 2.9 Fabrication process for wafer level underfill(© 2003 IEEE) [97]

2.6 Reliability Challenges in Electronic Packaging

Reliability of a system is defined as the probability of the system to function as intended, and failure is the opposite of reliability. To describe the lifetime of a system, a bathtub curve is widely used. A bathtub curve is the plot of instantaneous failure rate h(t) with respect to time [29]. Figure 2.10 is a typical bathtub curve where three distinct regions are observed. These regions are: [29]

1- Early failure (infant mortality): it is the period that the failure rate is decreasing, failures in this region are due to manufacturing flaws and premature failure modes.

2- Useful life (intrinsic failure): this is the region where failure rate is almost constant, and failures occur randomly. The goal of reliability testing is to determine the failure rate in this region.

3- Wear-out stage: Last stage of the system's lifetime where the system starts to break down and wear out resulting in increased failure rate.

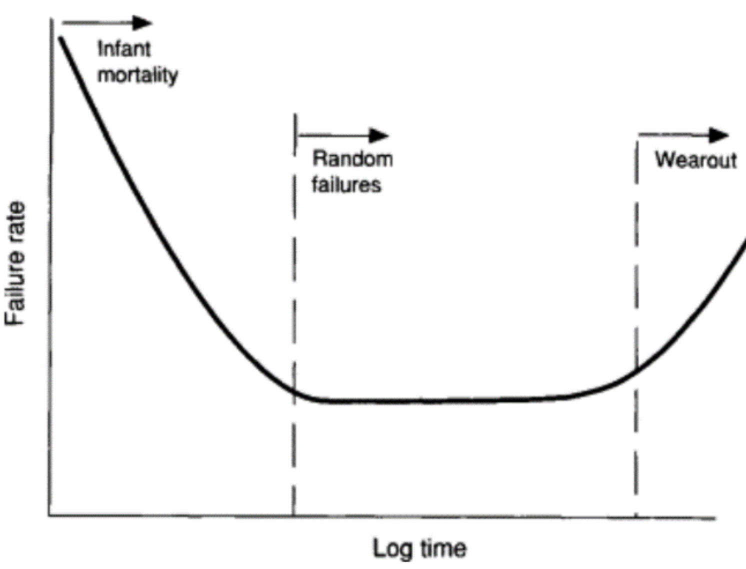

Figure 2.10 A typical bathtub curve highlighting three regions of the curve [29].

During the lifetime of the assembly, various external stresses may result in the failure of the system. In a study of the major failure modes in electronic devices, it was concluded that the largest portion of failures are due to thermomechanical stresses followed by stresses due to vibration and failure due to corrosion (Figure 2.11) [30].

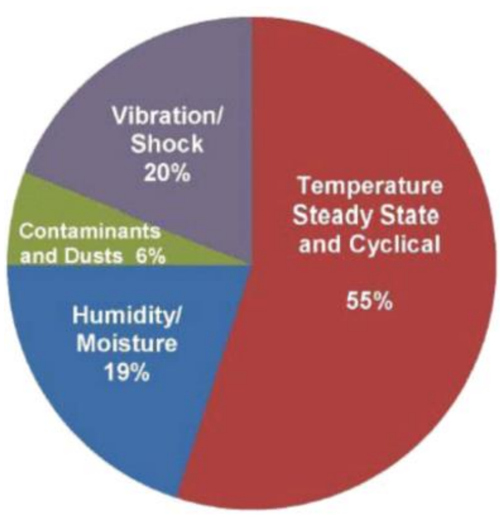

Figure 2.11 distribution of failure mechanisms in electronic devices [30].

Vibration stresses may result in impact or fatigue failures while thermal aging of solder joints results in microstructural changes in the solder alloy and creep failure [31]. Wafer thinning introduces additional reliability concerns to the assembly.

In the next section, the major reliability challenges related to solder joints and other aspects of modern electronic packaging are reviewed.

2.6.1 Reliability Issues of Lead-Free Solder Alloy

There are multiple factors that affect the reliability of the lead-free solder alloys. Following is a summary of these factors:

1- Effect of temperature: Since the melting temperature of lead-free solders is lower than lead-based alloys, elevated temperature affects their microstructure more significantly.

2- Aging: During reflow of the solder alloy to form the joints, IMC forms between the base metal and solder alloy. Subsequently, during the aging process, the volume fraction of the IMC increases and results in stress concentration regions leading to crack initiation, further crack growth, and failure of the joint. Due to the brittleness of the IMC region, mechanical strength of the solder joint diminishes as the volume fracture of IMC increases. Investigated in [32] is the effect of aging on IMC microstructure and growth at the interface of Cu/SAC305 for 360 hours at 150 °C. Figure 2.12 shows the growth of Cu_6Sn_5 within Sn3.0Ag0.5Cu (SAC305) solder alloy during aging process [32]. At 0 hr, Cu_6Sn_5 is finely dispersed in the solder matrix and, in fact, improves the mechanical properties of the alloy through precipitation hardening. However, as the

solder is aged at elevated temperature and the thickness of the IMC region increases, the mechanical properties of the solder joint degrade [32].

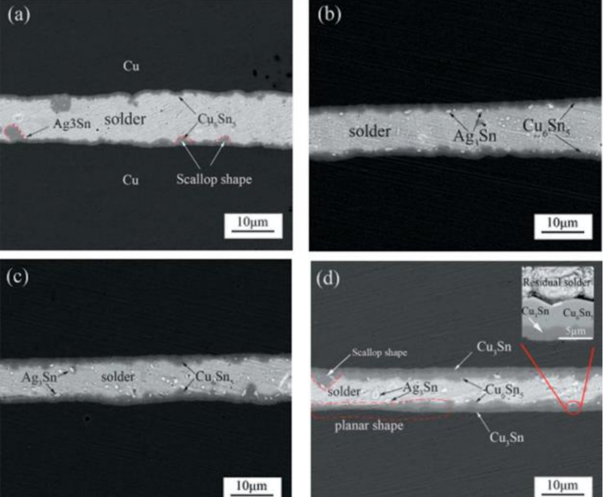

Figure 2.12 IMC growth at the interface of SAC305/Cu at 150 °C for (a) 0 h, (b) 120 h, (c) 240 h and (d) 360 h [32].

3- Tin whiskers: whiskers are formed due to diffusion of metal atoms at or near room temperature. Since Tin has a lower melting temperature (232 °C [33]), diffusion happens faster within the Sn matrix especially when pressure is applied and results in whisker formation in the Sn based solder joints during extended thermal aging or use time where mechanical pressure and temperature are applied [34].

The length of tin whiskers ranges from a few microns to a millimeter and can have diameters in the range of 0.2-5μm and they form different shapes including needle like, columnar, bunched whiskers and others [34]. Figure 2.13 shows different types of Tin whiskers [35]. Since Sn whiskers have high current capacity, they may cause shoring of adjacent solder joints if they bridge the two joints [34]. This shorting may be permanent if the current is below 10mA or intermittent when the current is above 10mA, moreover, these whiskers may cause electric arcs that will damage the device irreversibly [34].

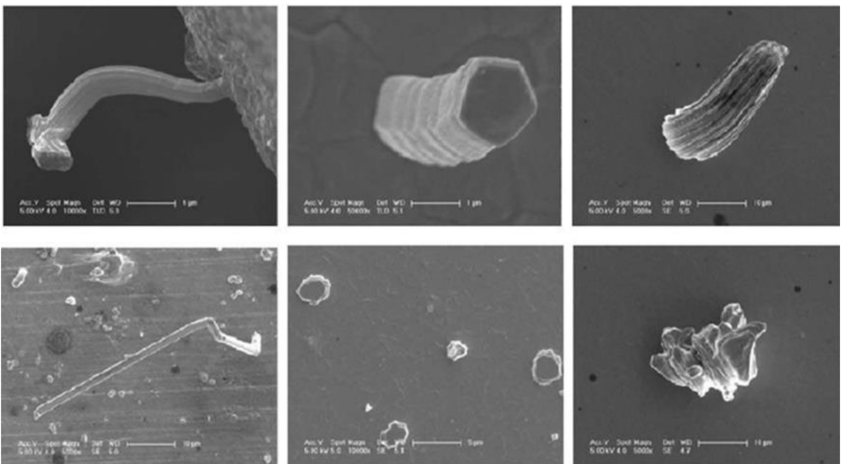

Figure 2.13 Different shapes of tin whiskers [35].

4- Effect of vibration: when electronic assembly is subjected to mechanical load in the form of vibration, PCB board goes through deflection and bending which translates large stress and strain levels on to the solder joints [34]. This transmission of alternating stress from PCB to solder joints results in tensile and compressive stresses in the solder joints which may initiate cracks and/or propagation of cracks within solder joints [34]. Many investigations have been done on the effect of die size, solder alloy material, and underfill on reliability of the solder joints under vibration load. In [36] the effect of underfill on vibration reliability of PBGA solder joints was investigated. It was concluded that the PBGA arrays with full underfill exhibited a significantly better reliability as compared to non-underfill samples. Underfill can reduce the stress and strain levels that the solder joints experience and hence improve the vibration reliability of the solder joints.

The effect of solder alloy on the lifetime of solder joints under vibration has also been investigated. It has been shown that in SnAgCu alloys, with increased Cu content, the reliability of the solder joints is improved through enhancement of the dendrites in the Sn phase and improvement of the Cu_6Sn_5 IMC toughness [37].

In [38] the effect of vibration on fatigue fracture mode of SnAg alloys was investigated. A correlation between frequency and load level and fatigue behavior was identified. It was concluded that increasing the stress ratio and frequency, increases the rate of crack growth. Moreover, the crack propagation behavior changes from cyclic-dependent to time-dependent and fracture mode moves from trans-granular to inter-granular [38].

2.7 Summary

In this chapter, a review of electronic packaging with an emphasis on flip chip technology was presented. In the past few decades, as bandwidth and the number of I/Os increased, significant effort was put into scaling the interconnects and the pitch between them. To further accommodate compact packaging and small form factors, 3D integration solutions were introduced and are widely used in today's industry. 3D integration provides numerous advantaged for scaling, increased bandwidth, and reduced delays, however, the complexity of 3D assemblies especially with addition of TSVs, die thinning, and difficulty of thermal management, add reliability challenges.

Underfill material is used to mitigate large thermomechanical stresses that solder joints experience due to the CTE mismatch between die and PCB. The role of the underfill is to distribute the stresses and reinforce the mechanical stability of the solder joints, it is also effective as passivation to protect solder joints from moisture ingress. Underfill properties can be tuned through additives to achieve underfill with lower CTE and higher toughness, these additives will affect the capillary flow and curing temperature and may hinder complete filling especially if the pitch is small. As the pitch scaling continues and the gap between the die and the board decreases, using conventional underfill becomes more challenging, thus, new underfills that do not rely on

capillary flow have been developed. These types of underfills help with simplification of solder reflow and underfill application however, they introduce other challenges such as incomplete filling, void formation during curing, and possibility of delamination.

Due to all the challenges regarding solder interconnects and continue demand for smaller pitches, the interconnect technology is shifting towards non-solder-based interconnects and Cu bumps and pillars are being studied as possible replacement. Cu interconnects have many advantages over solder joints however, they require unique passivation to protect them from oxidation.

Finally, a summary of major reliability challenges of electronic packages was discussed. The main failure mode in electronic devices is related to temperature, either temperature variation and thermomechanical stresses associated with CTE mismatch, or thermal aging and degradation that happens within the solder joints due to exposure to elevated temperature for extended period of time. IMC formation and growth in solder joints diminishes their mechanical stability and as solder joint dimensions decreases, the volume fraction of IMC increases more rapidly and results in faster degradation of the interconnect, thus sophisticated thermal management system is required to control the temperature.

Other failure modes are related to vibration and humidity. During vibration loading, a large deflection and bending in the PCB exerts alternating stress and strain onto the solder joints, various factors affect the vibration reliability of the packaging including package size, design, solder alloy and underfill.

Failure due to humidity is caused by corrosion in the metal lines and interconnects, galvanic corrosion is also possible. To circumvent degradation due to humidity, passivation and encapsulation are used to protect the assembly from moisture and other ions.

3. Introduction to Silicon Interconnect Fabric

The scaling of package and PCB dimensions is crucial for enabling integration of high-performance systems. At UCLA, we developed the Silicon Interconnect Fabric (Si-IF), which is a platform for heterogeneous integration of unpackaged dies at fine interconnect pitch (≤10 µm) and close inter-dielet spacings (<30 µm). We fabricated 10 µm pitch Cu pillars with 5 µm diameter and 1.5 µm height on the Si-IF. These pillars are bonded to corresponding Cu pads on the die. Both the pillars and pads are fabricated using damascene process [5]. The Si-IF fabrication process is compatible with conventional Si back end of the line (BEOL) processes which makes this platform very attractive in terms of cost and feasibility. The dies are bonded to the Si-IF using a solderless metal-metal thermal compression bonding (TCB). Further, due to the fine-pitch interconnects and short links on the Si-IF, high data-bandwidth with low latency and low power consumption is achievable [5, 3]. In this chapter, a detailed description of Si-IF technology and fabrication process is presented as well as process development for Cu chemical mechanical polishing (CMP) which is a key process step that enables reliable TCB.

3.1 Si-IF Overview

Si-IF is a heterogeneous integration platform that allows fine pitch integration of different die sizes, technology nodes and material on a Si substrate. The Si substrate fabrication process is compatible with Si CMOS back end of the line process. A detailed design manual was prepared to help designers utilize advantages offered by this heterogeneous integration platform [39]. The design manual provides different metallization layers up to four, however there is no fundamental limit on the number of achievable metallization layers. The final layer consists of Cu pillars that are extruding out for about 1.5µm. The only requirement for the dies is to have corresponding

bonding Cu pads, which makes the integration process compatible with unpackaged dies [5]. Figure 3.1 is a cross section of a bonded sample where pillars on the Si-IF side and pads on the side are labeled [40]. In the following section, a summary of the fabrication steps is presented.

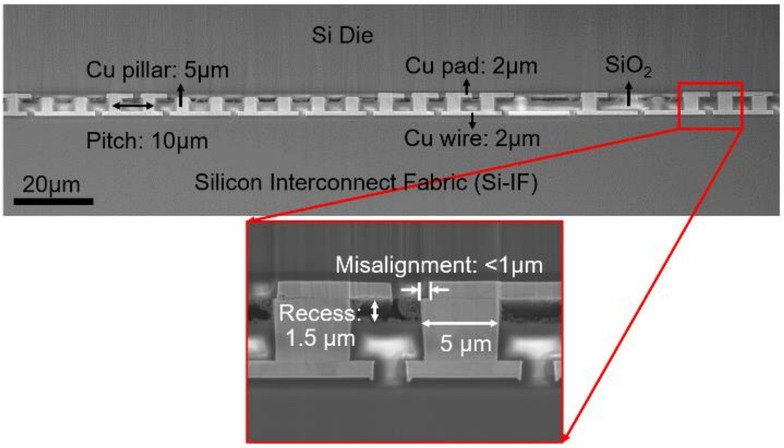

Figure 3.1 Cross section of a bonded Si-IF showing the Cu pillar and pads with misalignment of less than 1 μm [40].

3.2 Si-IF Fabrication Process

Si-IF fabrication process starts with growing thermal oxide on full thickness Si wafer, the step-by-step fabrication process is detailed in Figure 3.2. This figure outlines fabrication steps for one level metallization, but the steps are the same for further metallization levels [39].

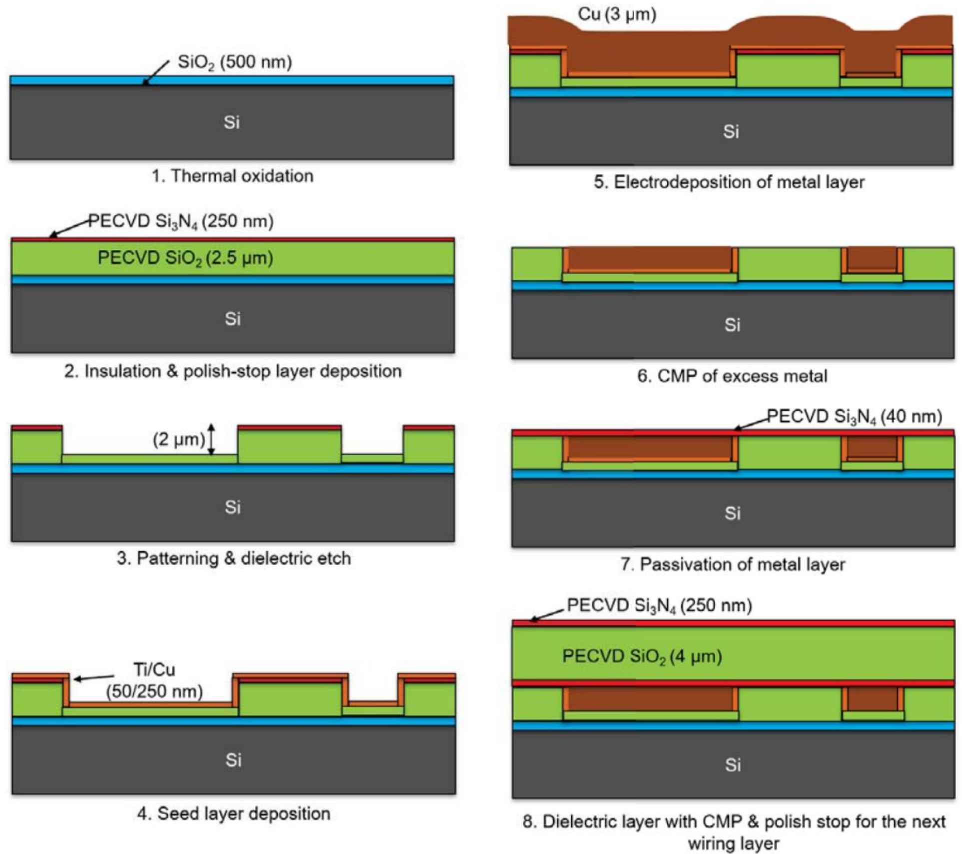

Figure 3.2 wiring level fabrication steps [39].

After finishing all the wiring levels, pillar layer is fabricated. Figure 3.3 is the detailed fabrication steps for pillar layer [39]. These pillars form the interconnects after TCB bonding to the corresponding pads on the die side. The factors affecting the yield of TCB include pads and pillars' surface cleanliness, surface roughness and planarity. Thus, the CMP step in the wiring levels and

pillar level fabrication is significantly important [39]. In the next section, a detailed CMP process development is presented.

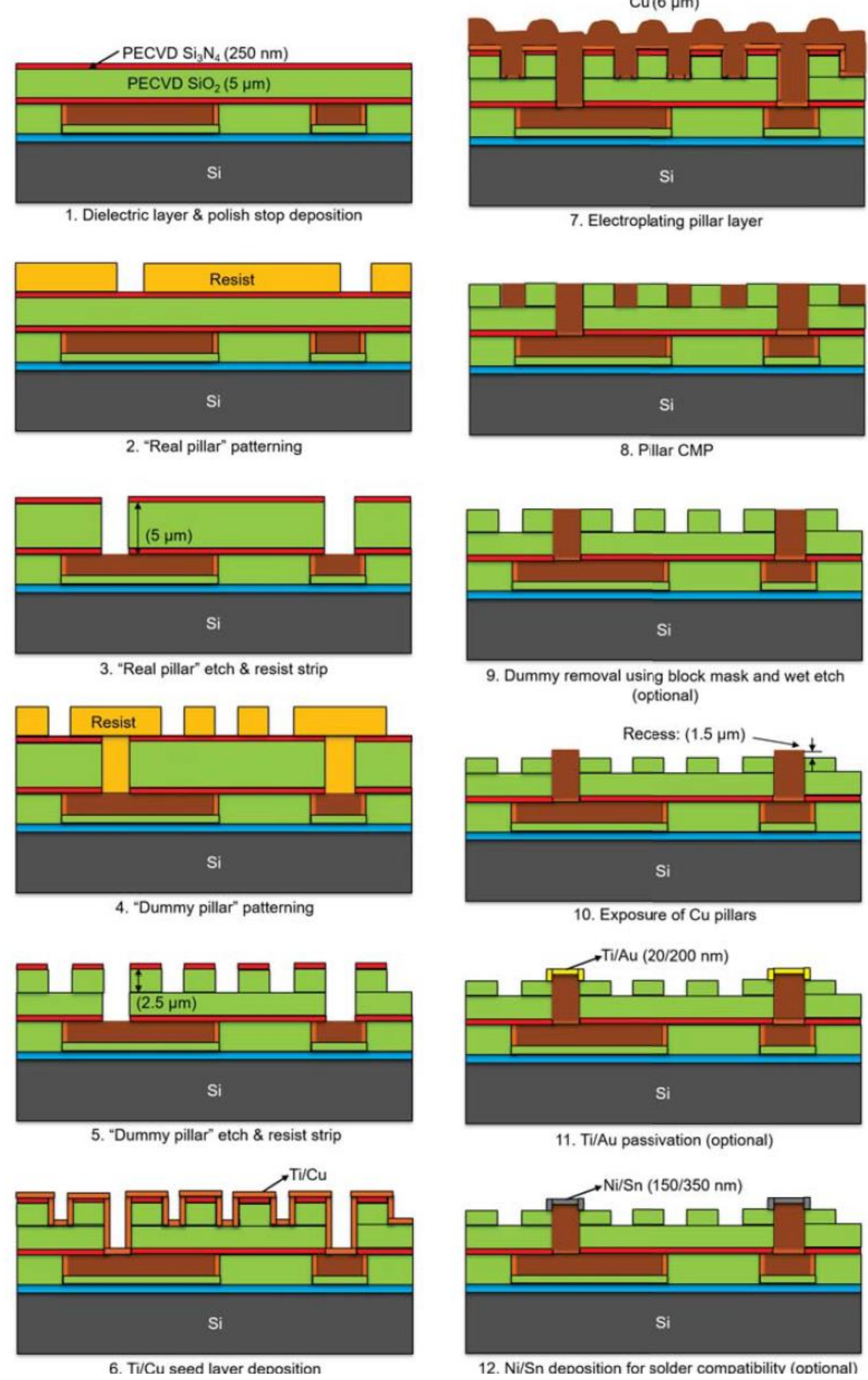

Figure 3.3 pillar layer fabrication step [39].

3.2.1 CMP Process

Chemical mechanical polishing (CMP) is a planarization technique that uses chemical oxidation and mechanical abrasion to remove material and achieve very high levels of planarity. Figure 3.4 is the schematic of the process showing the main parameters and tool components. The primary process control variables [41]:

- down force
- rotation rate
- slurry flowrate

The CMP process can be divided into fluid process, mechanical process, and chemical process.

Figure 3.4 schematic of CMP process showing the main variables (Adapted with permission from Elsevier) [41].

1. Fluid process: The Stribeck curve is a fundamental concept in tribology and is used to describe the nature of the contact of two surfaces in the presence of fluid. It is extensively used in polishing process to identify the optimized polishing environment based on process parameters [42]. The Stribeck curve is plotted by diving dynamic coefficient of friction (CoF) over a dimensionless number associated with film thickness known as Sommerfield number (also known as Hersey number). Sommerfield (So) number is describe in Equation 3-1.

$So = \frac{\eta V}{\delta P}$ *Equation 3-1*

Where η: dynamic viscosity of the fluid, V is the relative velocity between the two surfaces, P is the relative pressure, δ: thickness of the film [42].

The plot consists of three distinct regions as shown in Figure 3.5 [42]. These regions describe the interaction between and the wafer when slurry is present for different CoF and Sommerfield number.

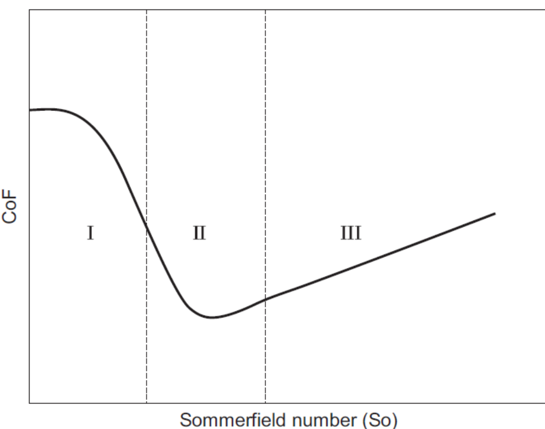

Figure 3.5 Stribeck curve that describes the three different interactions that can happen between pad and wafer in the presence of slurry during CMP process(Adapted with permission form Elsevier) [42]

Region I is known as boundary lubrication where there is an incomplete fluid film between the surfaces. Polishing load is supported by the contact between wafer and pad. In contrast, region III which is known as hydrodynamic lubrication region, describes a situation where the slurry film is continuous, and wafer and pad are hydroplaning. The polishing load is carried by slurry. Region II is known as mixed lubrication region, where the polishing load is partly supported by the pad and wafer and partly by the slurry. CMP process is done in region II or III [42]. An important factor in determining the pad and wafer degree of solid-solid contact is the pad surface roughness. It has been shows that both pad and wafer roughness generally follow a Gaussian distribution [43].

2. Mechanical Process: The earliest model for removal of material from a polished surface mechanically was developed by Preston in 1927 [44]. His theory postulates that the amount of material removed from a surface is proportional to the work done on the surface. The amount of work done is the product of pressure and velocity (Equation 3-2) [42].

$$MRR = K_P \times PV \qquad \textit{Equation 3-2}$$

Where MRR: material removal rate, K_p: Preston's coefficient, P: relative pressure, V: relative velocity.

This equation implies that for a fixed PV, the removal rate is constant, however it has been shown that in the case of CMP, polishing rate in fact changes during the process and decreases as the polishing process continues [42]. This variation is attributed to the surface roughness of both the wafer and the pad. At the beginning of the process, both surfaces are rough, and they do not make complete contact [42]. As the polishing progresses, the wafer surface becomes smoother and the contact area between the pad and the wafer increases and effective pressure decreases until it reaches a constant pressure level due to complete contact between the wafer and the pad [42]. To be able to apply Preston's model to CMP process, modification is done to incorporate "effective pressure" rather than the nominal pressure [42]. Moreover, material is removed from the wafer surface when it is "scratched" by the abrasive particles. To incorporate the mechanism of material removal, more modification is needed to be done on the Preston's equation. Contact mechanics can be used to quantify this mechanism. The volume of the material removed from the surface due to abrasive particle penetrating the wafer surface can be calculated assuming Hertzian contact. Thus, the K_p coefficient is defined only by wafer's Young's modulus (Equation 3-3) [42].

$$MRR = \frac{1}{2E} \times PV \qquad \textit{Equation 3-3}$$

There are a few limitations related to Preston's model and the modified equations. These models do not take into account the effect of the particle size or slurry chemistry on the material removal rate. Furthermore, there is an assumption that the contact is elastic and that the surface contact is always between wafer and abrasive particles, conditions that do not happen in the actual CMP process [42].

2.1. Abrasives: even though the exact role of the abrasive particles in the slurry is not fully understood, they are an integral part of the CMP process. There are different types of abrasive particles depending on the material being polished. For Si and Si based materials, colloidal silica or other metal oxides such as ceria (CeO2) are typically used [42]. For CMP of metals, abrasives such as colloidal silica and alumina are used. The properties of the abrasive particles that affect the material removal rate include, particle size, shape, and concentration [42]. In polishing of hard metals, such as tungsten, there is a logarithmic relationship between size and material removal rate with smaller particles removing materials faster than larger particles [42]. However, the relationship between particle size and removal rate for copper is not very clear [42]. The relationship between the concentration of abrasive particles in the slurry and material removal rate is similar to the particle size. Increasing the concentration increases the material removal rate because higher particle concentration results in more particles available for polishing. However, there is a limit to this effect, after which, increasing the concentration further will not improve the material removal rate [42].

2.2. Particle shape: is another important factor, the abrasive particles are typically assumed to be spherical. There has been some research on the effect of nonspherical, nonsilica particles on the CMP process (Figure 3.6) [45]. Some experimental results suggests that these

particles may improve the material removal rate (Figure 3.7) and CMP selectivity process as well as reducing the introduction of CMP process defects such as scratches [42].

Although mechanical abrasion is an integral part of the CMP process, mechanical abrasion alone does not define the CMP process completely thus it is important to understand the chemical interactions during polishing as well.

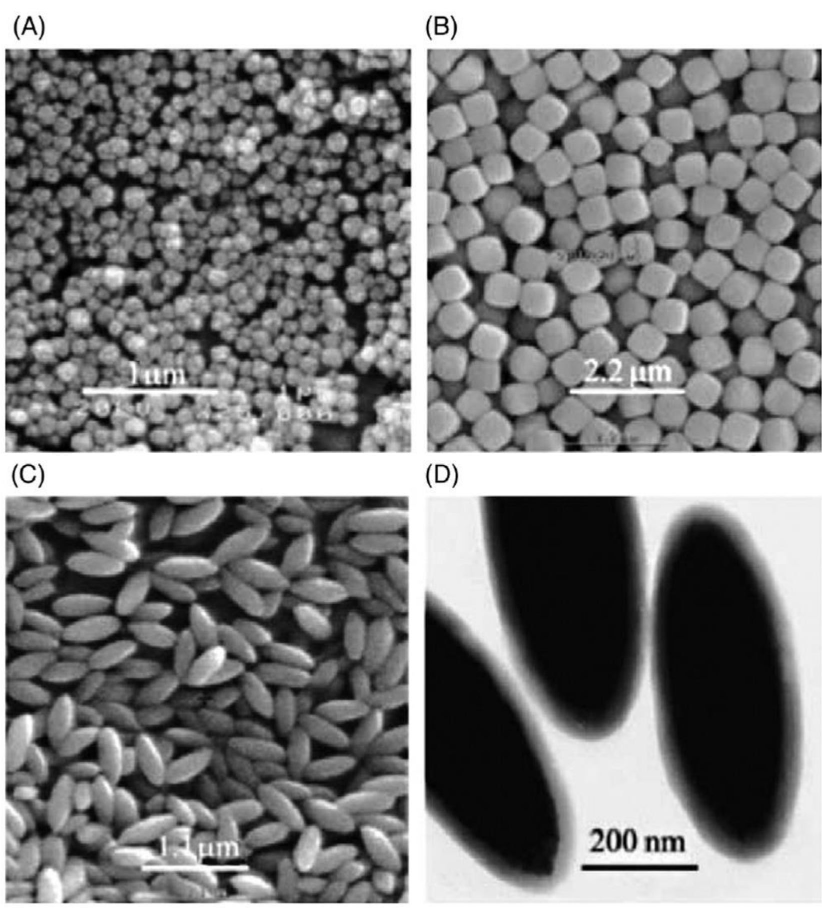

Figure 3.6 SEM images of (A) spherical, (B) cubic, and (C) ellipsoidal hematite, (D) ellipsoidal hematite with a thin silica shell (Adapted with permission form Elsevier) [45].

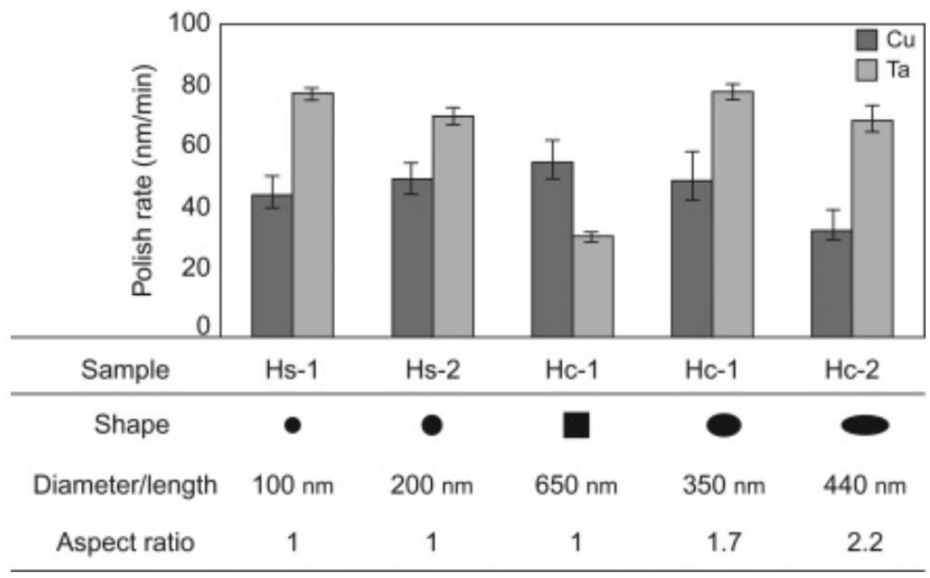

Figure 3.7 comparison of material removal rate of copper and tantalum for particles of varied size and shape (Adapted with permission form Elsevier) [45].

3.Chemical processes: an alternative to mechanical model was proposed by Cook [46]. In this model that is also known as chemical tooth, the abrasive particles in the slurry have the same hardness as the wafer being polished [46]. This assumption removes the mechanical abrasion properties of the particles as well as limiting damaging the wafer [46]. The chemical reaction between the slurry and wafer and particle surfaces hydrolyzes them and results in a bond formation between atoms on the wafer surface and slurry particle surface, these materials are removed through the stream of the slurry. A consideration from this model is that redeposition of the removed material on the wafer surface is possible. A phenomenon that is observed in actual CMP process [47]. The chemical model can effectively consider the effect of the slurry chemistry and abrasive type on material removal rate. However, this model cannot consider the effect of pressure on the MRR [42].

Research in polishing of tungsten resulted in development of another theory that links both chemical and mechanical interactions in CMP process [42]. In this model, the chemical constituent

of the slurry acts as an oxidizer which in case of tungsten, results in formation WO_3 which is softer than tungsten itself and thus is mechanically removed from the surface by abrasion. As oxide is removed from the surface, fresh metal is exposed to the slurry and the chemical-mechanical process is repeated [42].

3.2.1.1 Modeling for Copper CMP

Copper does not form a passivating oxide layer, thus modeling the Cu CMP is complicated. The chemical component of the slurry is very crucial since uncontrolled oxidation results in pitting and etching of the copper surface [42]. Due to these complexities, Preston's equation is widely used to simplify modeling of Cu polishing [42]. However, there are other models that are used to describe Cu polishing mechanism including Plasticity and adhesion model, threshold pressure and real contact area model, and scratch intersection model [42]

3.2.1.2 Slurry Composition for Cu CMP

The constituents of copper slurry are usually the following:

1- Oxidizers: to activate the chemical process of the CMP, there needs to be a condition to facilitate oxidation of the metal being polished. Half reactions for Cu oxidation are as bellow [42]:

$$Cu \rightarrow Cu^{2+} + 2e^{-}$$ *Equation 3-4*

$$2Cu \rightarrow 2Cu^{+} + 2e^{-}$$ *Equation 3-5*

$$\frac{1}{2}O_2 + H_2O + 2e^{-} \rightarrow 2OH^{-}$$ *Equation 3-6*

$$Cu + \frac{1}{2}O_2 + H_2O \rightarrow CuO + 2OH^{-}$$ *Equation 3-7*

$$2Cu + \frac{1}{2}O_2 + H_2O \rightarrow Cu_2O + 2OH^{-}$$ *Equation 3-8*

Above half reactions show that Cu oxidation in the presence of water does not happen spontaneously and there requires to be an oxidizing agent to promote the chemical reaction. The main oxidizing agents used in Cu slurry are nitric acid, ammonium hydroxide, and hydrogen peroxide [42]. Each of these oxidizing agents have their advantages and disadvantages. Nitic acid was one of the first oxidizing agents to be used in copper slurry [42]. It has been shown that nitric acid is effective in oxidizing copper, producing Cu (II) ions instead of Cu(I) ions [42]. However, the presence of H^+ causes copper dissolution and since there is no passivation formation on the copper surface, the copper will etch away [48]. Study of copper CMP with nitric acid containing slurry had shown increased in the surface roughness from 10 Å to 150 Å [49].

To prevent this issue, ammonium hydroxide was introduced as an oxidizing agent [48]. Ammonium oxide provided passivation by in part increasing the pH level of the solution, however, ammonium ions also act as chelating agents which leads to reducing the effectiveness of the passivation formed by copper oxide film and intergranular corrosion happens [48].

In recent years, hydrogen peroxide is the most widely used oxidizing agent in Cu CMP process. Oxidation mechanism of Cu in the presence of H_2O_2 is twofold [42]. Not only H_2O_2 oxidizes Cu, but hydrogen peroxide decomposes to hydroxyl groups as well, this cycle is known as Fenton cycle [50]. The chemical reaction is as follow:

$$Cu^{+} + H_2O_2 \rightarrow Cu^{2+} + OH^{-} + OH^{*}$$ *Equation 3-9*

$$Cu^{2+} + H_2O_2 \rightarrow Cu^{+} + OOH^{*} + H^{+}$$ *Equation 3-10*

The hydroxyl radical is a more efficient oxidizing agent than hydrogen peroxide and as copper ions are formed during the CMP process, this reaction becomes self-catalyzing [42]. Moreover, Chronoamperometric investigation of copper in hydrogen peroxide showed that it can

lead to formation of oxide films without extensive intergranular corrosion that happens when using ammonium hydroxide [42].

2- Corrosion inhibitors: despite the efficiency of H_2O_2 as an oxidizer for copper CMP, it is important to have oxidizing inhibitor agents in the slurry to achieve a good planarization. Corrosion inhibitors stabilize the passivation film, there are various agents used in the slurry but the most commonly inhibitor is Benzotriazole (BTAH) [42].

BTAH results in formation of a CuBTA region, this region is more extensive than the passivation region for copper in water. Increasing the BTAH concentration increases this passivation region up to 0.01 M after which, increasing the BTAH concentration will not have an effect on the passivation region (Figure 3.8) [51].

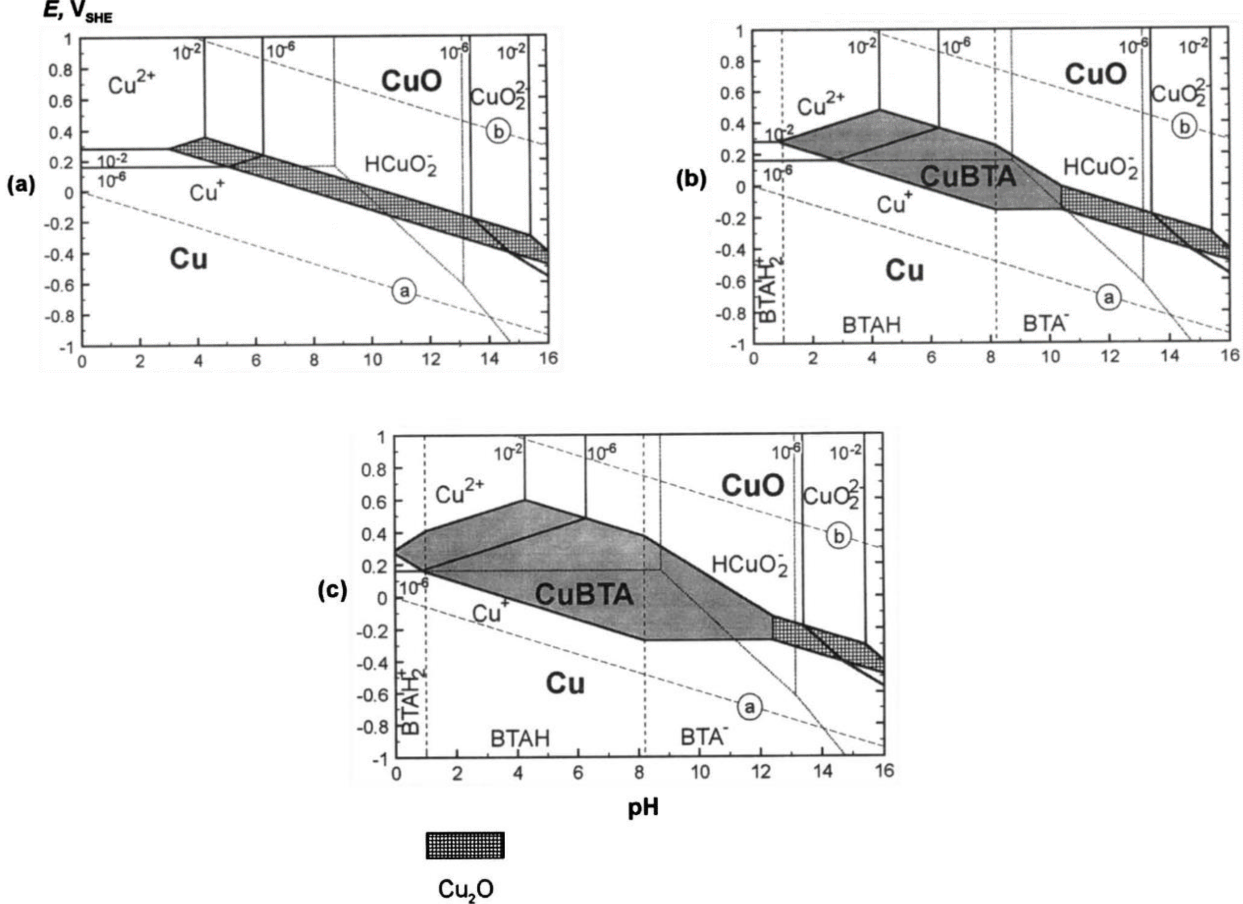

Figure 3.8 E-pH diagrams for the Cu-BTAH-H20 systems; (a) no BTAH, (b) in the presence of 10^{-4} total activity of dissolved BTAH species; and (C) in the presence of 10^{-2} total activity of dissolved BTAH species(Adapted with permission from IOP publishing [51]).

3- Chelating agents: these agents are added to help with removing copper debris from the polished surface and prevent redeposition on the freshly polished surface. Moreover, addition of chelating agents will reduce the occurrence of defects such as scratching with no negative effect on polishing rate. Glycine and citric acid are generally used as chelating agents in the slurry [42].

3.2.1.3 Copper CMP Process Development

The Due to sensitive nature of the CMP process in Si-IF fabrication, a new CMP tool was purchased. POLI 400 from G&P company is a single head CMP tool capable of polishing wafers of different sizes, the polishing head on the current tool is compatible with 4-inch wafers. Figure 3.9 shows the CMP tool and its major components.

Figure 3.9 G&P POLI-400L CMP tool and its major components.

As mentioned in section 3.2, in Si-IF fabrication process copper is electroplated for thicknesses of 3-5 µm, that is the overburden thickness that needs to be polished to form the wiring levels as well as critical step of pillar formation.

To develop an optimized CMP process for Si-IF fabrication, samples with 3µm of electroplated copper were used during trial phase.

In the first CMP trial, a DuPont® IC1000 pad was used (Table 3-1 [52]). CABOT Epoch™ C8902 was used as the base slurry, Table 3-2 is the slurry composition and their role in CMP process [53]. 1% (volume) hydrogen peroxide was used as an oxidizer. Figure 3.10 is the polishing results. Figure 3.10 (a) is after five minutes of CMP, a significant amount of Cu overburden is remained. Figure 3.10 (b) is after removing the rest of the copper. It can be seen that all of the features are oxidized even though oxidizing inhibitor was present in the slurry. The excessive oxidation of the polished copper is related to the type of oxide inhibitor, the inhibitor in this slurry is not as effective as BTAH (Figure 3.11 [54]). Thus, BTA was added to the slurry to improve the oxidation inhabitation. Two different slurry chemistries were used for the second round of process optimization:

- Main polish was performed with C8902 10% ,H2O2 1%, DI water 89%
- Fine polish was done using C8902 10%, H2O2 1%, DI water 89%+ 80 ppm of BTA

*Table 3-1 DuPont® IC1000 polishing pad pr*operties and application [52].

Base Material	Urethane
Compressibility	2.25
Hardness Test (Shore D)	57
Thickness	50
CMP Application	Tungsten, Copper, ILD, STI, and polysilicon

Table 3-2 CABOT Epoch™ C8902 composition and their role [53]

Component	% by Weight	Role
Silica, Amorphous	<3%	Abrasive
3- Amino-1,2,4, Triazole	0.1%	Oxide inhibitor
Proprietary Ingredients	<18%	
DI Water	>79%	

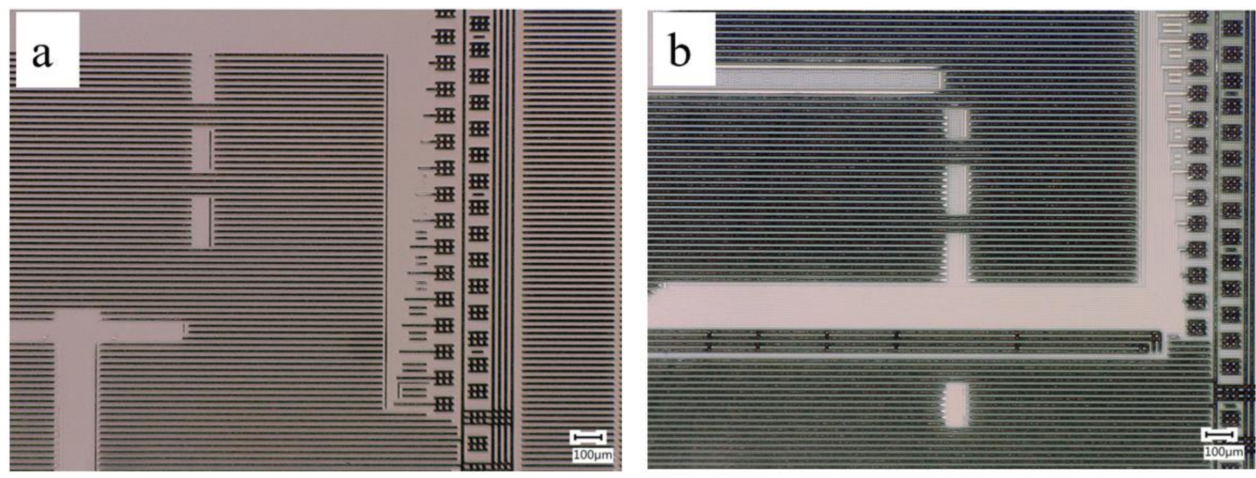

Figure 3.10 optical microscopy image Cu overburden after five minutes of CMP (a), after removing the rest of the overburden, all the previously polished Cu surfaces are oxidized (b).

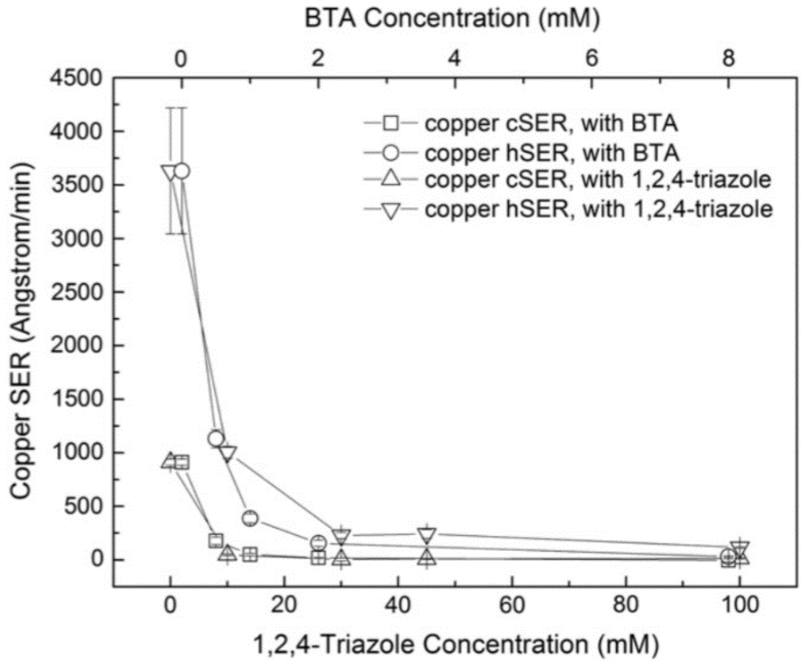

Figure 3.11 Comparison between the inhibition ability of 1,2,4-triazole and BTA [54].

Moreover, the polishing pad was changed to DuPont® IC1000 with K1 concentric grooving.

Figure 3.12 shows the polishing results, even though the excessive oxidation issue is resolved, there are still major challenges including:

1. Long polishing time
2. Nonuniformity resulting in large dishing.
3. Oxidation of larger features

Thus, the slurry was changed to Versum Cu3490. Table 3-3 is the composition of this slurry.

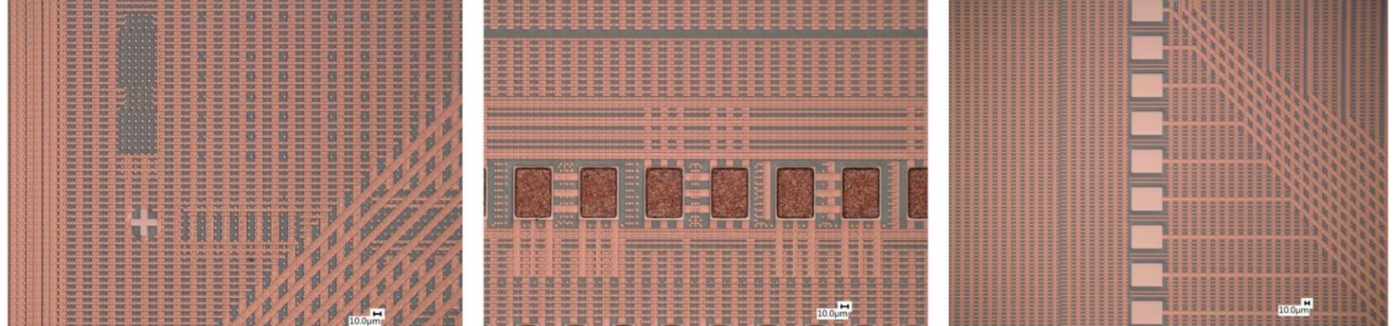

Figure 3.12 optical microscopy image of the polished sample showing all overburden is removed, however; excessive oxidation at the larger feature sites due to long polishing period.

Table 3-3 Versum Cu3490 composition

Component	% by Weight	Role
Glycine	10%-20%	Chelating agent
Amitrole	1%	Oxide inhibitor
DI Water	>80%	

The slurry chemistry used for subsequent polishing was as follow:

- 5600 grams DI water, 1900 grams Versum Cu 3940, 533 grams hydrogen peroxide

- No BTA was added.

One slurry chemistry was used for the entire polishing step. Figure 3.13 is the optical image of the sample after polishing.

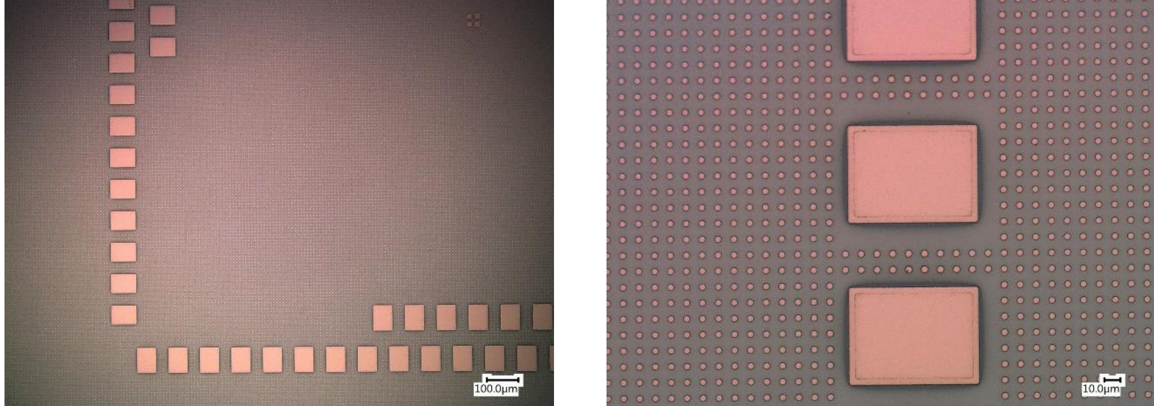

Figure 3.13 optical microscopy images of polished sample showing no signs of oxidation.

From Figure 3.13, it can be seen that this slurry chemistry and CMP polishing parameters are indeed the most optimized for Si-IF processing. These are the process parameters used for conventional Si-IF CMP step for copper wires and pillars (Table 3-4).

Table 3-4 *optimized process parameters for copper CMP step in Si-IF fabrication process*

Wafer pressure (psi)	2
Ring pressure (psi)	2.5
Platen speed (rpm)	50
Head speed (rpm)	57

Figure 3.14 is the atomic force microscopy (AFM) image of a Cu pillar after CMP and dielectric recess. The average roughness of the Cu pillars after CMP is 3.3 nm which is suitable for TCB.

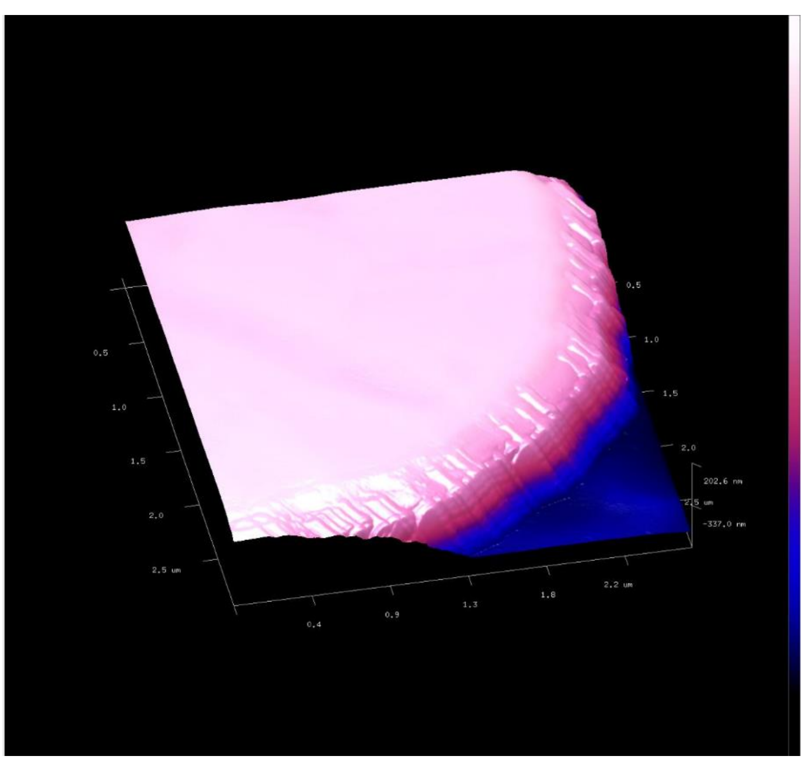

Figure 3.14 AFM image of the pillar, showing the roughness after CMP and the dielectric recess.

3.2.2 Thermal Compression Bonding Process

After Si-IF fabrication, dies (dielets) of different sizes are integrated directly on the Si wafer using thermal compression bonding (TCB). As it was mentioned previously, TCB step is a solderless bonding process where two copper surfaces are brought to contact and through simultaneous application of pressure and temperature, bonding is achieved. The TCB process has been extensively studied and optimized for Si-IF process by Siva et al. [5, 6, 39]. Here is a summary of the process and major challenges related to Cu/Cu TCB process [6]. Figure 3.15 is the schematic of the dielet integration on Si-IF during TCB process [6].

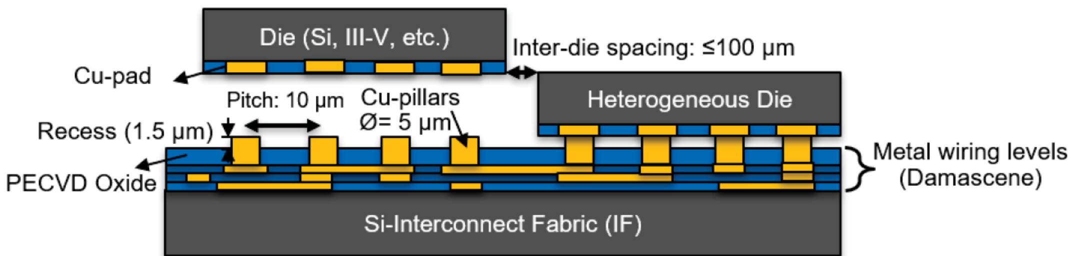

Figure 3.15 schematic of dielet integration on Si-IF [6].

The requirements for a high yield thermal compression bonding include:

1- Planar pad and pillar surface

2- Pristine surface free of any foreign particles

3- Planarity of the wafer and dielet

Copper is very prone to oxidation even at room temperature, and the rate of oxidation increases exponentially with increasing temperature which leads to the requirement that the bonding should be done at low temperature [6]. A more detailed discussion of copper oxidation is presented in next chapter.

To ensure copper oxidation is inhibited during the bonding process, in addition to lower bonding temperature, a reducing atmosphere is needed. To achieve this atmosphere, a formic acid flow was used during the bonding and N_2 gas shield was used throughout the process [6]. Figure 3.16 is a schematic of the bonding tool showing the formic acid supply mechanism and N_2 shield.

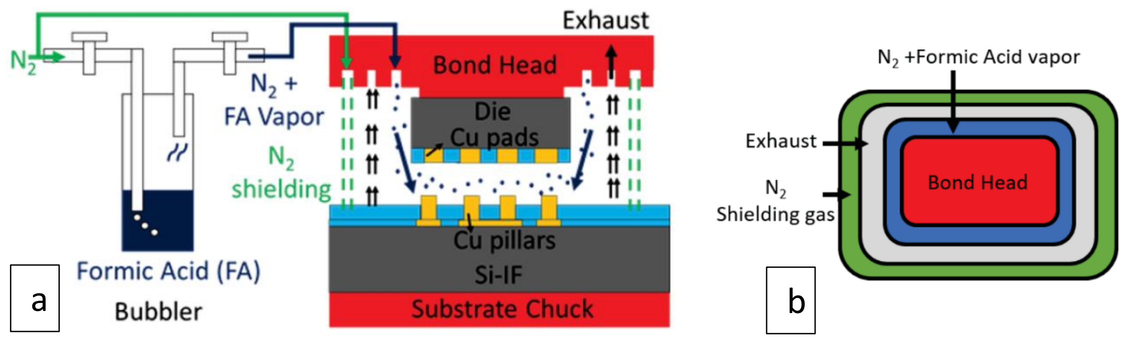

Figure 3.16 schematic of the tool setup showing the formic acid bubbles and bond head (a), top view of the bond-head showing the three channels for shielding N_2 gas, exhaust, and formic acid vapor (b) [6].

Before starting the bonding process, both substrate and dielet are surface treated by Ar plasma to remove any contamination. The bonding tool allows for separate heating of the substrate and dielet [6]. Thus, it is possible to keep the wafer at low temperature (100 °C) to avoid copper pillar oxidation during bonding of multiple dielets across the entire wafer. However, to ensure the surface temperature for both pillars and pads reaches above 200 °C, dielet is heated to a higher temperature and before the bonding step, the dielet is lowered on the substrate to make contact with pillars and locally heat up the copper pillars on the substrate conductively [6]. Below is a summary of the bonding steps [6]:

- Step 1: Dielet and Si-IF are heated up to 100 °C. The alignment between the dielet and Si-IF is done using built in camera.

- Step 2: The formic acid vapor is introduced and dielet is lowered on to the substrate. Dielet temperature is increased to 380 °C. This step ensures the pillar substrate is heated to 200-240 °C and allows for reduction of any copper oxide on the surface.

- Step 3: the bond head is raised to allow for reactants from formic acid reaction be removed - through exhaust.

- Step 4: The dielet is lowered again to form the bond between the pillars and pads through TCB. The pressure is raised to 100-250 MPa.

- Step 5: after bonding the bond head is removed and the assembly is removed from the tool to allow the cooling of the sample.

Figure 3.17 is a sample of the bonding profile process parameters showing the die position, pressure, and temperature of cleaning, purging and bonding steps [6].

Figure 3.18 shows a wafer scale assembly of 371 heterogeneous dielets on a 100 mm Si-IF wafer [6].

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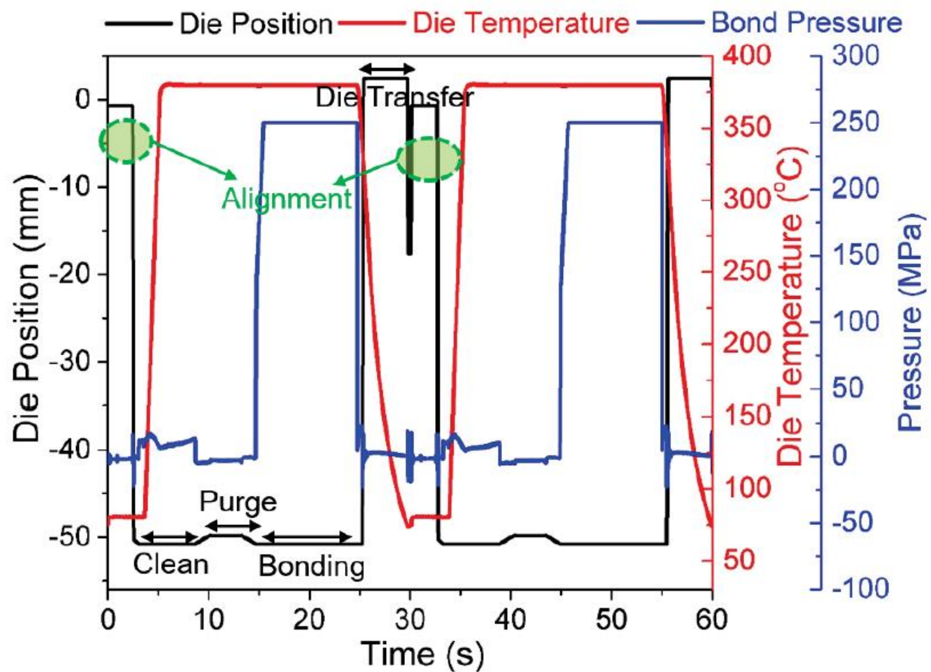


Figure 3.17 process profile parameters in cleaning, purging and bonding steps [6].

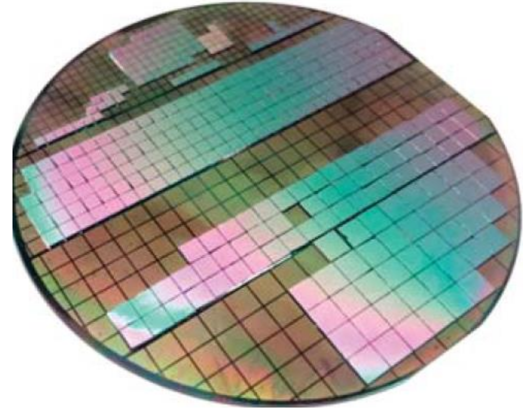


Figure 3.18 371 heterogeneous dielets of different sizes from 1x1 mm² to 5x5 mm² with 100 µm inter-dielet spacing on a 100 mm Si-IF [6].

3.2.3 Si-IF Challenges

Si-IF, similar to any other technologies, has some limitations and challenges in terms of fabrication, integration, and performance. Below is a summary of the major challenges [6]:

- The assembly process is needed to be done at a cleanroom facility to ensure the cleanliness of dielet and substrate and achieve a high yield.

- Solder-based assemblies can be reworked if there is an issue with a chip. However, Cu/Cu TCB interconnects are not reworkable. This hinders the serviceability of the Si-IF. To solve this issue, redundancy of wires around faulty dielets and links are needed. 3D integration and interposer platforms using solder capped micro bumps also have similar limitation.

- Even though Si-IF allows for fine pitch integration of dielets, this integration requires very fine alignment during TCB bonding. This alignment is done through the optical microscope to detect the alignment marks. In the case of solder-based interconnects, the molten solder allows for self-alignment through surface tension. The elimination of solder from interconnects results in the need for very accurate alignment which can be only achieved with sophisticated system equipped with precise optics and isolation from vibration or any other mechanical interference.

- Wafer scale integration that involves large number of dielets present another challenge related to substrate oxidation due to wafer being at elevated temperature for an extended period of time. This issue can be circumvented by temporarily passivating the Cu pillars or progressively increase the formic acid vapor flow rate or duration as bonding process continues.

- Due to elimination of underfill and overmold in Si-IF platform. Exposed Cu in the assembly due to misalignment, is prone to oxidation and degradation during operation. Thus, it is

important to develop a novel passivation to protect exposed Cu from degradation. More detailed discussion about passivation development is presented in Chapter 4.

- Replacing PCB board with Si substrate reduces the vibration reliability of the assembly. PCB is more flexible than Si and is also capable of damping the input mechanical acceleration to a higher extent. Thus, it is important to add insulators to reduce and damp the input vibration to improve the vibration reliability of the assembly. More detailed discussion of vibration analysis of Si-IF is given in Chapter 6.

3.3 Si-IF Based Wafer Scale System

To enable all the advantages that Si-IF offers, a wafer scale system is being developed using Si-IF as the heart of the technology. Figure 3.19 is a schematic of the system. Si-IF is connected to a power platform from the back side through BGA solder joints. A sophisticated two-phase cooling system is attached to the top of the bonded dielets. Data transfer to and from the system can be achieved either through flexible connectors or optical connection.

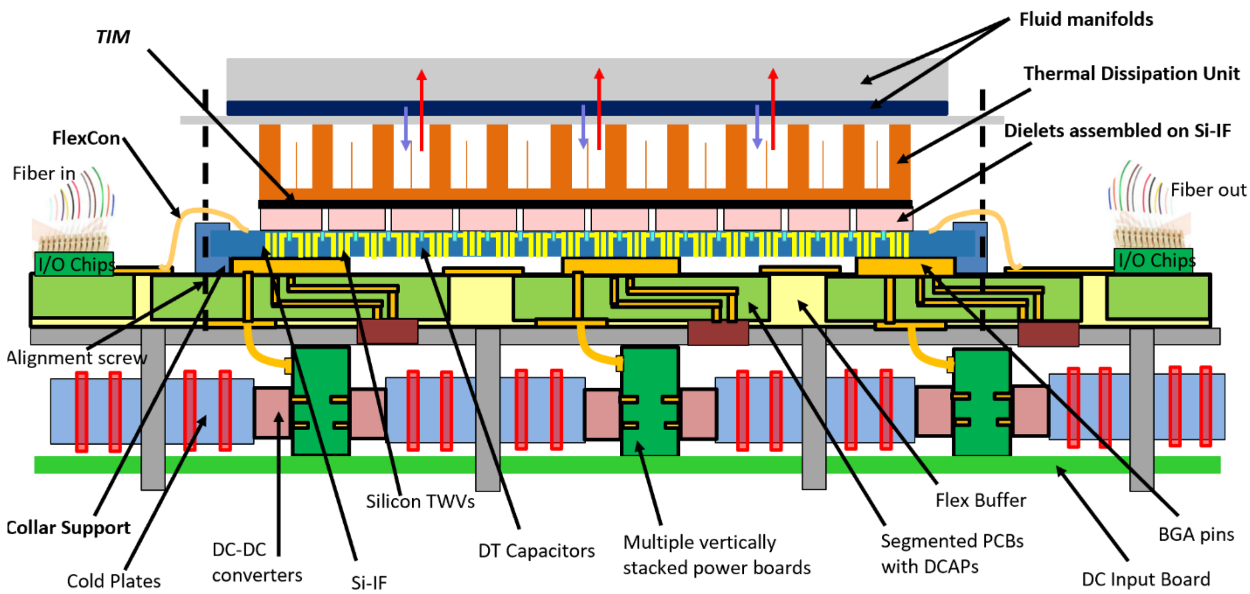


Figure 3.19 schematic of the wafer scale system highlighting different components.

To ensure this large-scale system is capable of withstanding thermomechanical stresses within the solder joints, an elastomer is designed as a buffer between PCB and Si-IF. Two different designs were considered, and the simulation results of both designs are presented in Chapter 5. The effect of solder material and elastomer and PCB size on the reliability of the assembly is also studied in Chapter 5. Moreover, the vibration reliability of the assembly with inclusion of elastomer buffer layer is studied in Chapter 6.

3.4 Summary

An overview of Si-IF was presented in this chapter. The fabrication process of the substrate is compatible with BEoL processes. The interconnect formation is achieved through a solder-less TCB process.

To ensure high yield and reliable bonding during TCB, planarity of the pillars and pads are crucial. This requirement makes the CMP an important step in the fabrication process. A summary of major factors affecting material removal rate and surface roughness was presented. A detailed CMP process development was discussed in this chapter. By utilizing the optimized slurry chemistry, polishing parameters, and pad, a reliable process is developed, and the results were presented. Moreover, an overview of the TCB step with factors affecting a good interconnect are discussed.

Some challenges of the Si-IF platform related to assembly and serviceability were discussed as well as need for a novel passivation to protect the exposed copper in the absence of underfill and overmold.

An introduction to the wafer scale system using Si-IF was presented. This system utilizes back side of the Si-IF for delivering power and top of the dies for assembly of the thermal management unit. Flexible as well as optical connectors can be used for data transfer.

Further discussions related to vibration fatigue and thermomechanical stresses will be presented in Chapter 5 and Chapter 6 respectively.

4. Si-IF Passivation

One of the advantages of Si-IF integration platform is the simplification of the materials in the system by elimination of solder-base joints, underfill, and overmold. However, due to the misalignment that may occur during TCB between pads on the dielet side and pillar on the Si-IF side, some copper may be exposed to the environment. Because the passivation should be applied after integration of all the dies on to Si-IF, it is not possible to use the conventional encapsulation or passivation technologies. Moreover, fine pillar pitch and limitations attributed to the use of underfill, eliminates this passivation as an option as well. Thus, there is a need to develop a novel passivation that not only is effective in protecting copper from oxidation, but also has the step coverage requirement to allow for coating the pillars deep in the middle of the bonded dies.

In this chapter, a review of passivation materials and their properties used in today's packaging are presented. Furthermore, passivation development process for Si-IF, from material selection to experimental testing and results of material as well as electrical characterization are presented. Since passivation is separate from standard Si-IF fabrication process, effect of addition of a new material to the assembly on thermomechanical stresses within the copper pillars was also investigated using finite element analysis and the results are presented.

4.1 Passivation and Encapsulation

Encapsulation in electronic packaging is a crucial step to ensure protection of integrated circuit from degradation due to environmental factors. There are two different types of encapsulations used in electronic packaging, namely, hermetic (metallic or ceramic) and non-hermetic (plastic) [55]. Currently, most of the encapsulation in microelectronics is non-hermetic and a lot of effort has been put into incorporating new polymer-based encapsulations in the recent

years [55]. Numerous material properties must be considered when choosing a new encapsulation. These include CTE, T_g and mechanical properties of the material, its adhesion to the substrate, and conformality of the encapsulation [56]. The following sections are a brief summary of common encapsulation materials and technologies used in electronic packaging.

4.1.1 Hermetic Encapsulation

Hermetic packages are cavity types that protect the electronic devices from moisture and other corrosive gases. As the name suggests, these encapsulations are made of materials that are impermeable to moisture, such as ceramics and metals [55].

Metallic materials include Kovar (29% Ni/17% Co/54% Fe) and Alloy 42 (a nickel-iron alloy). These metal alloys have low CTE and are ideal for sealing between metal and glass or ceramic. Table 4-1 is the mechanical properties of Kovar and 42 Alloy [55].

Table 4-1 mechanical and thermal properties of Kovar and Alloy 42 [55]

	Kovar	Alloy 42
Coefficient of Thermal Expansion (ppm/°C)	30-200°C: 5.5 30-500°C: 6.2 30-900°C: 11.5	30-200°C: 4.5 30-500°C: 8.0 30-900°C: 12.3
Young's Modulus (GPa)	137.89	144.79
Yield Strength (MPa)	344.73	275.79
Ultimate Strength (MPa)	517	510.2

Ceramic encapsulants have limited application in industry due to their high cost, however; they are still widely used in MEMS devices. Ceramic encapsulants provide a wide range of material properties. Their CTE can be matched to Si chips or the CTE of copper. Their dielectric constant can vary from 4 to 10,000. Their thermal conductivity can be tuned to a range of an insulator to higher than Al [55].

4.1.2 Non-Hermetic Encapsulation

Non hermetic (plastic) encapsulations are the most widely used type of encapsulants in electronic packaging. The advantages of plastic encapsulants include low cost of design and manufacturing, smaller form factor and lower weight compared to hermetic encapsulants [55]. Molding compound is the most common type of encapsulation, others of encapsulation techniques include potting, printing, and underfilling [55].

The requirements for an effective molding compound encapsulation include good adhesion to materials in the assembly, mechanical strength, low CTE, electrical resistance, high thermal and chemical stability, and robust moisture barrier properties. The molding compound materials are either thermoplastic or thermosetting polymers, or elastomers. However, the majority of the molding compound materials are thermosetting polymers based on epoxy resins, such as polyurethanes, polyimides, and polyesters [55]. The polyimide films offer high thermal stability, low moisture permeability, and low CTE [55].

Thermoplastic polymers are not used very commonly as an encapsulant material due to high processing temperature and pressure conditions. Moreover, if the operating temperature goes above polymer's melting temperature, irreversible degradation can happen to the electronic devices [55].

Elastomers can be used as encapsulants in flexible electronics due to their flexibility properties, however they are not conventional encapsulant materials in rigid electronic packaging. Table 4-2 is the comparison between hermetic and non-hermetic encapsulants [55].

Table 4-2 comparison of hermetic and non-hermetic encapsulants [55].

	Hermetic vs. Non-hermetic
Size & Weight	Hermetic encapsulants are about twice as heavy as non-hermetic types. The non-hermetic encapsulant size can be smaller than hermetic types
Performance	Ceramic encapsulants have higher dielectric constant than plastic types, thus signal propagation delay is higher in ceramics than plastics. Consequently, the plastic encapsulants provide better performance.
Cost	Plastic encapsulants are cheaper than ceramic types

4.1.3 Passivation Requirements for Si-IF

Si-IF has some unique requirements when it comes to the passivation system. These requirements are as follow:

1- Since passivation is done after all the dielets are integrated into the system, the deposition process should be low temperature to protect temperature sensitive devices from degradation.

2- The passivating material should have a good adhesion to the material in the system including SiO_2, SiN_x, Si, and Cu and should retain its adhesion at elevated temperature and humidity level.

3- Passivating material should have a CTE close to other materials already in the system.

4- The deposition method should provide the necessary step coverage and penetration to allow for coating of the exposed copper under the dies.

From the above requirements, the material systems that are suitable for Si-IF passivation can be narrowed down. The materials that were studied in this research were :

1- Parylene C

2- Multilayer Parylene C and PECVD SiN_x

3- Atomic layer deposition of Al_2O_3

Next sections detail copper oxidation mechanism and experimental testing that can be done to measure robustness of a moisture barrier, experimental results for above three thin film systems, and finite element analysis of the thermomechanical stresses within copper pillars with and without passivation.

4.2 Kinetics of Copper Oxidation

Copper oxidation has been studied extensively and its oxidation mechanism is well known. Unlike Al, copper does not form a passivating oxide layer. Copper oxides are porous and thus, the thin film grows as long as the condition is right for Cu oxidation. It is well known that Cu forms two types of stable oxides CuO (cupric oxide) and Cu_2O (cuprous oxide) [57]. The dominant form of oxide depends on the temperature and ambient. However, it is believed that the copper oxidation is dominant by Cu2O over the temperature range of 873–1173 K and the rate determining factor is the diffusion of Cu through Cu_2O. Moreover, the oxide grows due to simultaneous grain and lattice diffusion [57]. The oxidation rate follows a parabolic law in the temperature range of 573-1173K, however the Arrhenius plot of the rate constant of this curve shows a break at around 823K or, 723K and the activation energy for temperature below the breaking point is very different from temperatures above that [57]. Table 4-3 is the list of copper oxidation energy in the temperature range of 573-1173K.

Table 4-3 copper oxidation activation energy in different ambient, there is a break in activation energy in temperature range of 573-1173 [57, 58, 59, 60]

Type of copper	Atmosphere	Temperature Range (K)	Activation Energy Q_a (kJ/mol)	
OFHC	0.1 MPa O_2	573-823	84	[60]
		823-1173	158	
OFHC	Air	573-773	39	[58]
		873-1173	123	
99.999%	0.1 MPa O_2 or Air	623-723	224	[59]
		723-1073	84	
99.999%	0.1 MPa O_2	573-773	40	[57]
		873-1073	111	
	Ar + 1% O_2	573-773	58	
		873-1073	111	

It has been observed that the lower activation energy for lower temperature is related to the morphology of CuO. At lower temperatures, CuO whiskers on top of Cu_2O is finer and is less protective that the top layer Cu_2O at 873K and above [57]. Thus, it is believed that this finer CuO grains increases the grain boundary diffusion at lower temperature and consequently, responsible for lower activation energy for temperature range of 573-773 [57].In [61], copper oxide activation energy at different temperature (100-600 °C) in dry and wet ambient is investigated and the oxide thickness was measured directly through SEM as well as indirectly using spectroscopic ellipsometry and reflectivity. It was concluded that Cu easily oxidizes at temperatures around 100 °C, and that for temperatures below 400 °C the Cu_2O is the predominant oxide whereas CuO is

dominant in temperatures above 500 °C [61]. Table 4-4 lists the activation energy for both ambient conditions [61].

Table 4-4 activation energy for dry and wet oxidation ambient [61].

Ambient Condition	E_a (eV)
Dry O_2	0.43
Wet Ambient (15% $H_2O + O_2$)	0.68

Bajwa et al. [5] also developed an empirical model for copper oxidation in dry ambient showing a time and temperature dependency:

$$L(\text{Å}) = 0.0076e^{(0.022T)}\log{(t)} \qquad \textit{Equation 4-1}$$

Calculated oxide thickness for different time and temperature using [61] and [5] empirical relations are listed in Table 4-5 . From Table 4-5, it is seen that oxidation happen within the first hour of exposure at room temperature and the thickness can reach 2 μm after a month of exposure to highly oxidizing environment at 100 °C.

Table 4-5 estimation of copper oxide thickness in dry ambient for different times and temperature

Temperature (K)	Time (min)	Oxide thickness (nm) (Bajwa et al. [5])	Oxide thickness (nm) (Hu et al. [61])
300	60	1.0	6.9
	43,800	2.6	187.7
	525,600	3.2	650.2
473	60	44.7	849.6
	43,800	116.6	22954.0
	525,600	143.7	79515.1
573	60	403.2	3638.5
	43,800	1052.4	98307.8
	525,600	1297.1	340548.2
673	60	3638.7	10113.9
	43,800	9498.0	273263.4
	525,600	11706.4	946612.3

Generally, there are two types of barriers based on the behavior of the material, one is sacrificial barriers such as organic films. This type of barriers slows down the rate of oxidation and degradation by absorbing the water molecules. Another type is the true barriers such as Al_2O_3 and other inorganic films that, in their ideal form, block the passage of water molecules and stop the degradation. Failure of this type of barriers due to cracking or delamination will result in catastrophic failure of the system. In next sections, used of both types of barriers as passivation for Si-IF is investigated.

4.3 Parylene C as Passivation

Poly-(para-xylylene), known as Parylene, is a class of semi crystalline polymers that are deposited through chemical vapor deposition (CVD) process. There are different types of Parylene including Parylene C, N and D. Figure 4.1 is the chemical structure of three types of Parylene [62]. Table 4-6 illustrates barrier properties of Parylene N, D and C. Parylene N is mainly used in applications where high temperature stability is required whereas Parylene C is the most common type encountered in MEMS and has the best moisture barrier property compared to the other types [62].

Figure 4.1 chemical structure of Parylene C, N and D [62].

Table 4-6 barrier properties of Parylene C, Parylene N and Parylene D [62].

Polymer	Gas Permeability at 25°C (cc.mm)/(m^2.day.atm)				WVTR (g.mm)/(m^2.day)
	N_2	O_2	CO_2	H_2	
Parylene C	0.4	2.8	3	43.3	0.08
Parylene N	3	15.4	84.3	212.6	0.59
Parylene D	1.8	12.6	5.1	-	0.09

In Parylene C deposition process, the dimer is heated in vacuum to form a gas. Pyrolyzing the gas creates the monomers. These monomers are transferred to the deposition chamber where they sublimate and form a conformal thin film, free of pin holes, at room temperature [63].

Aside from forming a defect free thin film at room temperature, Parylene C has other advantages as an encapsulation material including mechanical flexibility, electrical insulation, and

low intrinsic stress. As a result, it has been used as a water-resistant encapsulation in electronics for the past several decades [62].

To evaluate the robustness of moisture barrier properties of Parylene C, humidity testing was done on blanket Cu samples passivated with 1 and 3 μm. Test coupons were prepared by growing 500 nm of thermal SiO_2 on Si wafers followed by sputtering of 20 nm of Ti as a diffusion barrier and 200 nm of Cu as the seed layer. Then, 1 μm of Cu was electroplated on the samples. These test coupons were then transferred to the deposition chamber and Parylene C was deposited. Humidity test condition was 85 °C and 85% relative humidity (RH). Passivated samples were subjected to above testing conditions for 72 hours and then x-ray powder diffraction scan (XRD) was done on the samples to measure the amount of Cu oxidation. Figure 4.2 shows the schematic of the blanket samples with passivation. Figure 4.3 illustrates the XRD scans for two samples with 1 and 3 μm thick layers of Parylene C after 72 hours of humidity testing. In both the samples, Cu_2O was detected. Scherrer equation (Equation 4-2) was used to estimate average grain size of oxide (Table 4-7).

$$\tau = \frac{k\lambda}{\beta \cos\theta}$$ *Equation 4-2*

where: τ is the mean size of the ordered (crystalline) domains, K is a dimensionless shape factor, with a value close to unity, λ is the X-ray wavelength; β is the line broadening at half the maximum intensity (FWHM), after subtracting the instrumental line broadening, in radians. θ is the Bragg angle.

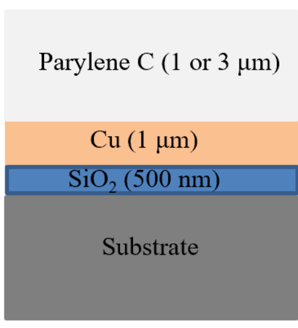


Figure 4.2 schematic cross section of the testing

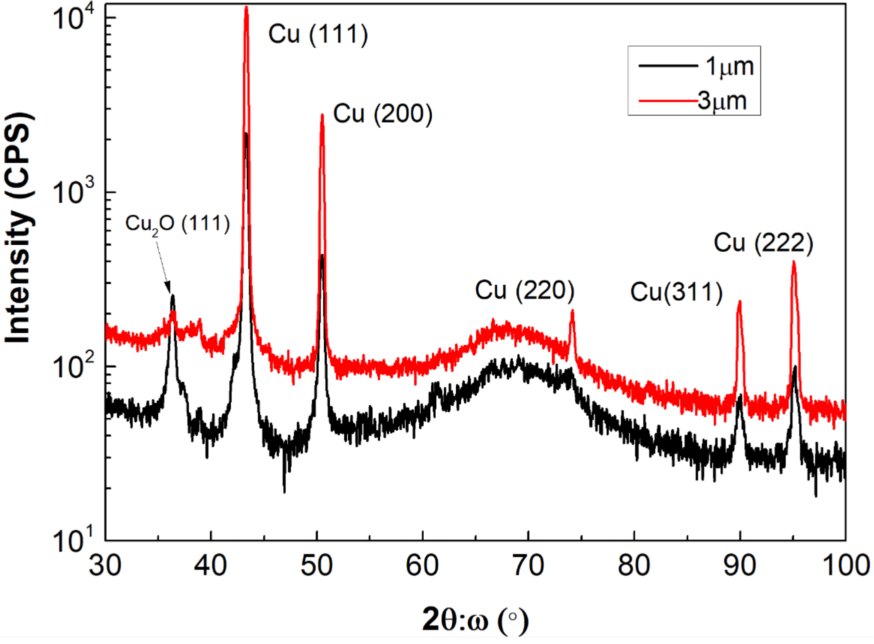


Figure 4.3 XRD scans of samples passivated with 1 µm and 3 µm of Parylene C after 72 hours of humidity testing. copper oxide is present in both samples.

Table 4-7 summary of the average oxide grain size in sample passivated with 1 and 3 µm of Parylene C after 72 hours of humidity testing.

	1µm Parylene C	3µm Parylene C
Cu_2O Average grain size (nm)	15.53	1.5
Cu Average grain size (nm)	22.5	22.5

Figure 4.3 and Table 4-7 show that increasing the thickness of Parylene C reduces the rate of Cu oxidation, however, Parylene C by itself is not a robust passivation film for Si-IF. Thus, a multilayer passivation was studied and the following section is the detailed investigation of this system.

4.4 Multi-Layer encapsulation

A multi-layer thin films consisting of plasma enhanced chemical vapor deposited (PECVD) SiN_x and CVD Parylene C was studied as the next passivating system. SiN_x is a common material in microfabrication that is used as dielectric, polish stop, and as a thin film passivation. SiN_x as an inorganic film has a good barrier property against moisture ingress and water vapor transmission rate (WVTR) as low as 4.39×10^{-4} g.(m^2.day)$^{-1}$ is reported for 480 nm of VHF-PECVD SiN_x [64]. However, due to the inherent defects existing in the PECVD deposited thin films such as pin holes, water molecules can penetrate through the defects and reach the substrate [65]. It has been shown that combining SiN_x and Parylene C as a multi-layer passivation will form an encapsulation system that reduces water molecule penetration rate [66].

Moreover, because Parylene C has poor adhesion to most substrates, especially metals, studies have been done to improve its adhesion using different adhesion promoters including 3 (Trimethoxysilyl) propyl methacrylate (A-174) and molten Parylene C [67, 68].There is a lack of data about the effect of exposure to harsh environment for extended periods of time on adhesion, but it has been reported that using A-174 as an adhesion promoter results in good adhesion of Parylene C to Si and other substrates for up to 20 minutes of exposure to 120 °C [68]. In [67], different techniques for improving Parylene C adhesion to Si was investigated and it was

concluded that utilizing molten Parylene C as adhesion promoter is a suitable replacement to the conventional A-174.

In this work, use of Triacetoxy(vinyl)silane adhesion promoter (DOW AP3000) was investigated. AP3000 is mainly used as an adhesion promoter for Benzocyclobutene (BCB) [69]. AP3000 has three Acetoxy (–OCOCH3) groups and one vinyl (CH=CH2) group. In aqueous solution, Si-(OCOCH3) hydrolyzes and strong Si-O-Si bonds are formed with hydroxyls groups on the surface of the inorganic substrate. AP3000 also reacts with methylene group (=CH2) in Parylene C leading to cross-linking at high temperatures [69]. Thus, annealing at a relatively high temperature plays an important role in improving adhesion, and uniformity of AP3000 [70]. AFM measurement on AP3000 shows unbaked samples have a poor uniformity and as annealing temperature reaches 100 °C, uniformity is significantly improved and annealing at 180 °C results in a uniform thin film [70]. However, since passivation of Si-IF is done on the fully bonded assemblies, there is a temperature restriction on encapsulation process in order to avoid degradation of temperature sensitive dies. Thus, in this work, annealing temperature was kept below 150 °C.

To investigate the effect of AP3000 on improving the adhesion of Parylene C to the substrate, Cu seed layer was sputtered on a Si wafers with 500 nm thermal SiO_2 followed by electroplating of 1 μm Cu. Cu is then coated with 500 nm of PECVD SiN_x. Six blanket samples were then treated with O_2 plasma to clean the surface followed by spin coating of AP3000. Test coupons were annealed at different temperatures for different times. Samples were then transferred to Parylene C CVD chamber where 3 μm of Parylene C was deposited. A "tape test" was then carried out on all samples in accordance with ASTM D3359-17.

This standard is a qualitative measure for ranking film adhesion to the substrate. There are two methods, A and B for different film thicknesses. Method A is used for films with thicknesses above 125 μm whereas method B is generally used for films with lower thickness. For this study, method B was utilized. The test starts with making parallel cuts through the film and another set of the same parallel cuts perpendicular to the first set. Next, a tape is applied to the cut area ensuring no air bubble is trapped between the tape and the film, after waiting for 90 seconds, the tape is removed and the cut area is inspected for the amount of film removed. The adhesion is ranked on a scale of 0 (no film left) to 5 (no material removed). Table 4-8 is a summary of annealing conditions for the samples as well as the tape test result.

Table 4-8 annealing temperature and time for adhesion test samples and their respective tape test result. Increasing annealing time to 5 minutes at 130 °C results in adhesion strength of 5B.

Sample	Annealing Temperature (°C)	Annealing Test (min)	Tape Test Result
b	No annealing	----	0B (more than 65% material removed)
c	0	----	0B (more than 65% material removed)
d	130	3	1-2B (between 15% and 65% material removed)
e	130	5	5B (no material removed)
f	130	10	5B (no material removed)
g	140	5	5B (no material removed)
h	140	10	5B (no material removed)

A test grid before the tape test is shown in Figure 4.4 (a). Tape test results for various surface treatments and annealing times and temperatures, are shown in Figure 4.4 (b-h). Increasing annealing time at 130 °C improved adhesion from 1B (35%-65% material removed) to 5B (0% material removed) The optimal annealing temperature and time were determined to be, 130 °C and 5 minutes, respectively.

Sample	Annealing Temperature (°C)	Annealing Test (min)	Tape Test Result
b	No surface treatment	----	0B (more than 65% material removed)
c	No annealing	----	0B (more than 65% material removed)
d	130	3	1-2B (between 15% and 65% material removed)
e	130	5	5B (no material removed)
f	130	10	5B (no material removed)
g	140	5	5B (no material removed)
h	140	10	5B (no material removed)

Figure 4.4 . (a) sample before tape test. Samples after tape test (b) no surface treatment where all Parylene is removed by the tape,(c) surface treatment and no annealing where more than 65% of the material is removed by tape (0B), d is the sample with surface treatment and 3 minutes of annealing at 130°C, after tape test between 35% to 65% of the material is removed (1B) (e) and (f) Sample with surface treatment and annealing at 130°C for 5and 10 minutes,.(g) and (h) samples with surface treatment and annealing at 140°C for 5 and 10 minutes respectively. It can be seen that increasing annealing time from 3 minutes to 5 minutes at 130°C results in a very good adhesion of Parylene C to the substrate and after tape test no material is removed.

To ensure Parylene C adhesion is not diminished due to exposure to humidity, humidity test was done on similarly fabricated samples that have been annealed for 5 minutes prior to Parylene C deposition. Humidity testing condition was in accordance with “85/85” Steady-State Humidity Life Test and was performed in an ESPEC SH242 benchtop chamber. Initially, samples were subjected to 85 °C for 30 minutes to ensure steady state temperature is reached throughout the sample and then the relative humidity level was increased to the set point of 85% and test duration was initiated. Tape test was performed every 24 hours on samples for up to 144 hours of humidity testing. Characterization of the samples was done using optical imaging before and after the test to evaluate amount of material removed. Optical images of the samples after tape test are shown in Figure 4.5.

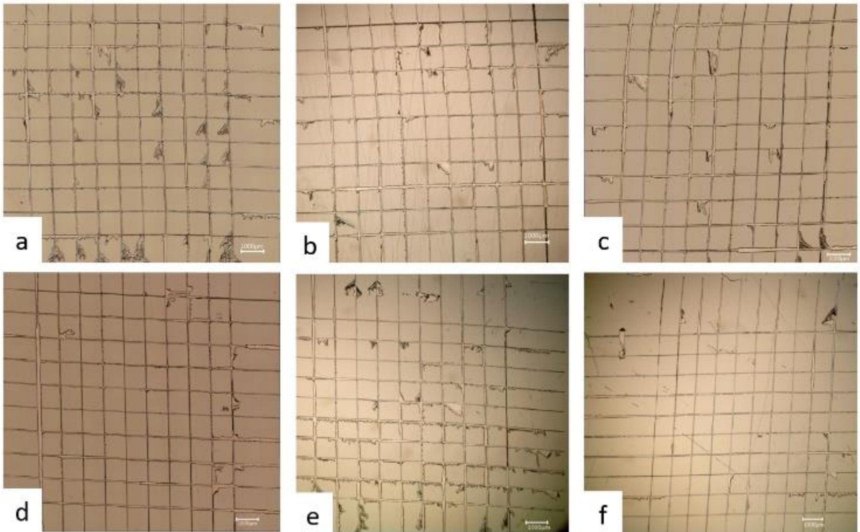


Figure 4.5 tape test result on samples after 24 hours (a), 48 hours (b), 72 hours (c), 96 hours (d), 120 hours (e) and 144 hours (f) of humidity testing. Overall adhesion remains constant and minimal loss of adhesion is observed after 144 hours of stressing.

Adhesion of Parylene to SiN_x substrate remained constant at 4B (less than 5% material removed) up to 144 hours of the humidity testing. The only exception was 120 hours of testing where adhesion degraded from 4B to 3B (between 5% to 15% material removed). That can be the result of insufficient annealing duration of AP3000 leading to insufficient energy for subsequent crosslinking. Tape test results suggest that annealing prior to Parylene C deposition effectively improves adhesion to SiN_x substrate and this improved adhesion remains almost constant after humidity testing.

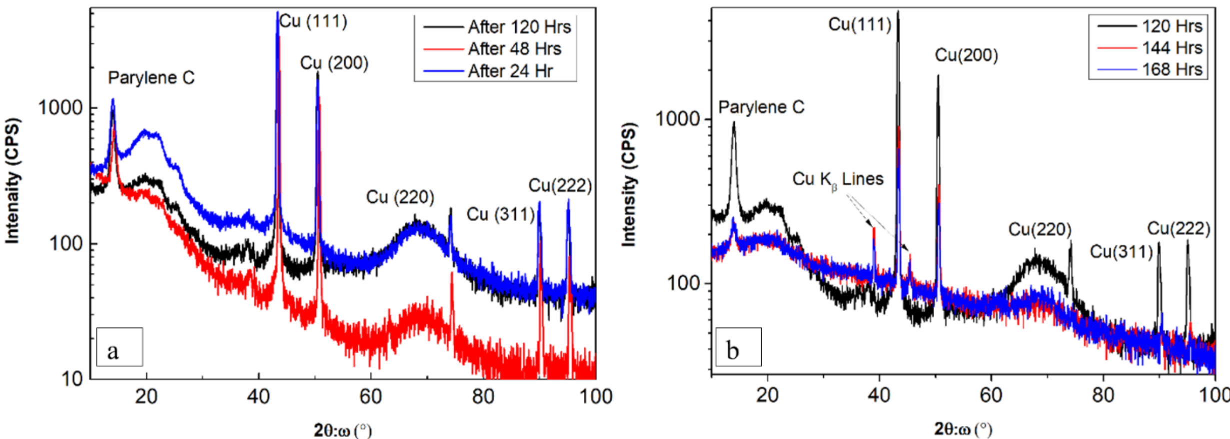


Figure 4.6 XRD scans for samples after 24, 48 and 120 hours of humidity testing (a) and after 120,144 and 168 hours of testing(b). No oxide peaks are detected in the samples.

To evaluate the effectiveness of the multi-layer passivation, humidity testing, similar to the above-mentioned test condition, was performed on passivated Cu blanket samples. Test coupons were fabricated utilizing previously mentioned fabrication process and were passivated with 500 nm of PECVD SiN_x (deposition temperature of 100 °C). Parylene C adhesion promoter was spin coated on the samples and annealed, and then, Parylene C was deposited on test coupons for 3µm and finally, another layer of SiN_x was deposited (300 nm). These test coupons were tested for 168 hours at 85 °C and 85% RH and XRD scan was performed on samples every 24 hours. Figure 4.6 (a) shows the XRD scan of sample after 24, 48 and 120 hours of testing and Figure 4.6 (b) shows the scan for 120, 144 and 168 hours of testing. No Cu oxide peaks were detected in the samples even after 168 hours of humidity testing. Thus, this multilayer passivation is effective in protecting copper from oxidation. To further analyze this passivation system in protecting copper wires from oxidation, sample with wires of different widths (10, 20, 40 and 100 µm) were fabricated using damascene process similar to Si- IF fabrication process. Figure 4.7 shows the process flow for line samples.

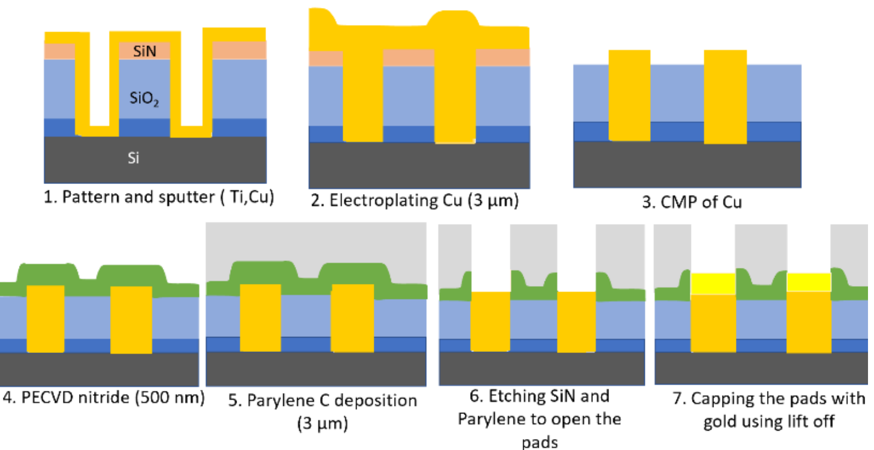


Figure 4.7 fabrication process flow for line samples encapsulated with multilayer thin films to evaluate change in electrical resistance of the Cu lines during 168 hours of humidity testing.

After fabrication, samples were passivated with multilayer encapsulation and humidity testing was performed. Electrical resistance of the lines was measured before start of the test and every 24 hours during humidity testing for 168 hours. Figure 4.8 shows change in the resistance of the lines throughout testing. Since there were 4 lines for each width, average resistance for each width is reported at every measurement point. Moreover, maximum change in the resistance of the lines was less than 3% after 168 hours of testing (Figure 4.8). These results are all very promising for multilayer system and shows the effectiveness of this encapsulation on 2D samples.

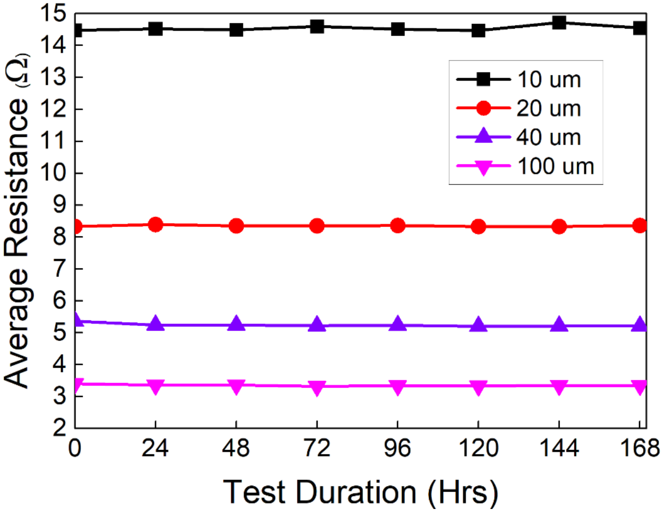


Figure 4.8 line resistance for up to 168 hours of testing, average change in line resistance for all line widths is less than 3%.

4.4.1 Need for Conformality

To effectively passivate bonded Si-IF samples, deposited thin films should have a good step coverage to allow for protection of the exposed Cu under the die. To investigate the step coverage of PECVD SiN_x, focused ion beam (FIB) cross sectioning was utilized on a bonded sample which was coated with 300 nm of SiNx. Figure 4.9 illustrates the change in the thickness of SiN_x from top of the die to the sidewall of the die and the interface of the die/Si-IF. Thickness changes from 283 nm to 44.1 nm. This lack of film thickness uniformity shows that PECVD deposition is not a reliable process for deposition and a more robust deposition process is needed.

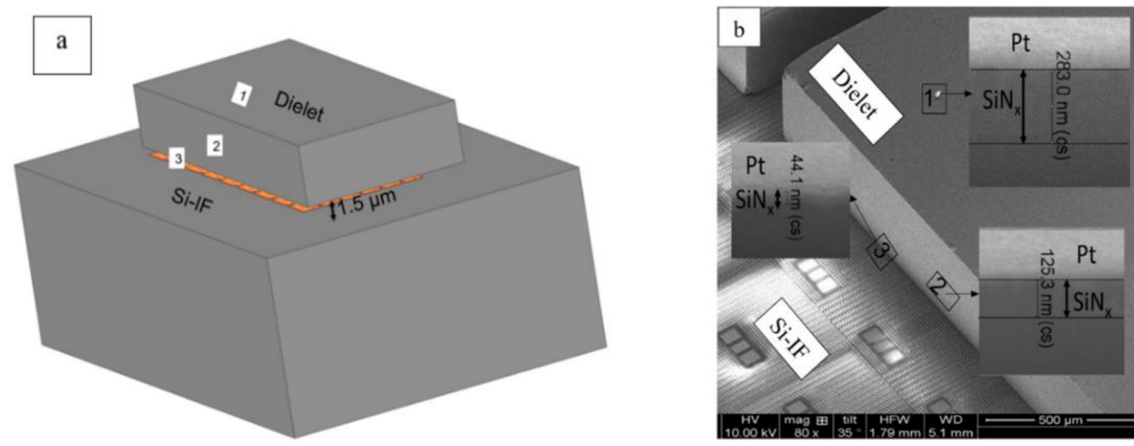


Figure 4.9 a schematic of a bonded sample showing the position of the FIB cross sectioning on top of the die [1], sidewall [2] and the interface of the Si-IF/die (a). SEM image of the bonded sample showing the thickness of SiN_x on top of the die (283 nm), sidewall (125 nm) and at the interface of Si-IF/die (44.1 nm) (b).

4.5 Atomic Layer Deposition Process

Atomic layer deposition (ALD) is a sub-class of CVD process in which thin film deposition is done in two or more sub cycles. Highly reactive precursors are used in each cycle to activate a chemical reaction with active groups on the substrate, residual precursor molecules and reactants are removed from the chamber before introducing the next precursor [71]. Thus, gas phase reaction between different precursors is prevented and thin films with high purity and thickness precision can be grown [71]. ALD is a self-limiting process and allows for precise film thickness control.

One of the most studied ALD film is deposition of Al_2O_3 using trimethyl-aluminum (TMA) precursor. Below equations are the chemical reactions during deposition process of Al_2O_3 using TMA [71]:

$$Al - OH^{*} + Al(CH_3)_3 \rightarrow AL - O - Al(CH_3)_2{}^{*} + CH_4$$ *Equation 4-3*

$$Al - CH_3{}^{*} + H_2O \rightarrow AL - OH^{*} + CH_4$$ *Equation 4-4*

Where asterisk terms are on substrate surface. Alternating between water and TMA results in the growth of Al_2O_3. Typical growth per cycle (GPC) for Al_2O_3 is between 1.1 to 1.2 Å per each full cycle [71].

To achieve a high conformality and uniformity, it is crucial to have a high mean free path to pore size ratio. This gas flow regime is called molecular flow, where molecular transport is dominated by gas-substrate interaction and inter particle reactions can be neglected. If mean free path to pore size ration is not large enough, inter molecular interactions become more significant and gas transport is controlled by viscus flow [72]. Equation 4-5 can be utilized for mean free path calculation in meters.

$$\lambda = \frac{\kappa_B T}{\sqrt{2}\,\pi d^2 P}$$ *Equation 4-5*

Where κ_B is Boltzman constant (J/K), T(K) is temperature, d(m^2) is the molecule's diameter and P (Pa) is pressure [73]. From Figure 4.10, it is apparent that pressure has a more significant effect on the mean free path while temperature and molecule size affect λ to a lower degree.

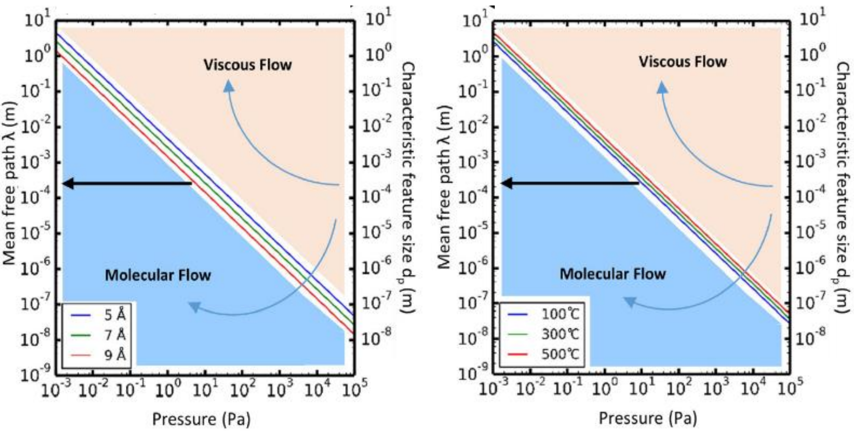


Figure 4.10 mean free path vs pressure, (a) for average molecular size of 5, 7 and 9 Å at 100°C and (b) for average molecular size of 7 Å at 100, 300 and 500°C. Comparison of the mean free path (left axis) with charactiristic feature size (right axis) determines the gas flow regime at a specific pressure [72]. (Adapted with permission from AIP publishing)

Table 4-9 mean free path for TMA molecules (average size 7 Å) at depostion temperture of 100 and 200°C for pressure of 0.01 and 0.001 Torr and mean free path to feature size ratio. Decreaing pressure results in a more signifant increase of the mean free path. For all cases, λ/d_p>>1 which suggests deposition happens in molecular flow region.

T (K)	P (Pa)	λ (m)	d_p (m)	λ/d_p
373	1.33	$1.8x10^{-3}$	$7x10^{-10}$	$2.53x10^{+06}$
	0.13	$1.8x10^{-2}$		2.5310^{+07}
473	1.33	$2.3x10^{-3}$		$3.21x10^{+06}$
	0.13	$2.3x10^{-2}$		$3.21x10^{+07}$

Table 4-9 is the calculated mean free path for TMA precursor for different ALD deposition parameters.

Interaction of copper surface with TMA + O_2 has been studied by A. Gharachorlou et al. [74], they concluded that clean copper surface does not react with TMA. However, TMA readily reacts with native copper oxide that forms on the surface. The chemical reaction happening on the surface of the copper with native copper oxide is as follow:

For the first TMA half cycle, the ratio of the Al:O was approximately 0.46 (the stochiometric of Al_2O_3 ratio is 0.66) this ratio suggests the presence of copper aluminate. Moreover, no long-range order of copper oxide was detected on the surface (Figure 4.11 (a)) during the first few cycles (~ 3 cycles) the TMA reacts with the oxygen within the oxide layer and reduces it to Cu.

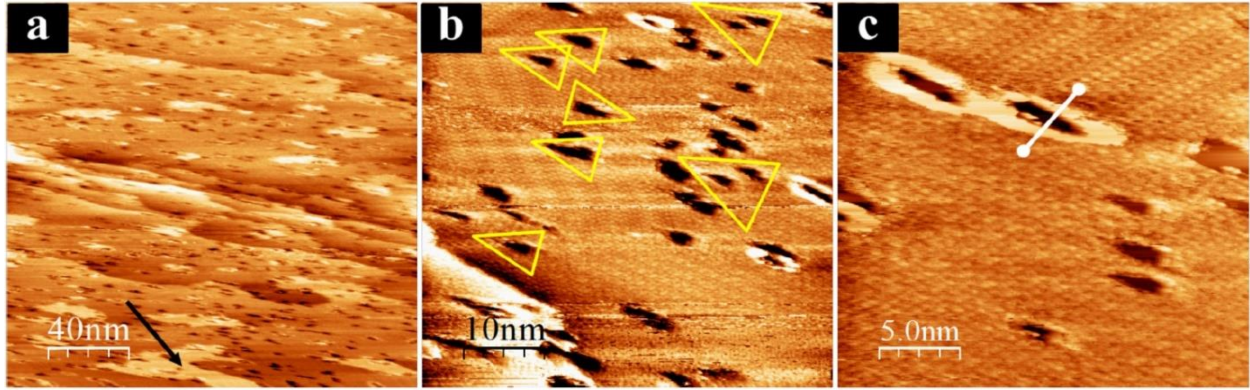


Figure 4.11 aluminum oxide islands that appeared after the first O_2 half-cycle with an average height of 0.17 nm (marked by black arrow in (a), dark regions are high density Al_2O_3 islands (b) Pitting on the surface due to oxygen abstracting Cu from the oxide (these holes work as mines for delivering Cu to the surface) .(Adapted with permission from ACS publishing) [74]

Equation 4-6 is the first half cycle with TMA [74].

$$2Cu_2O + Al(CH_3) \rightarrow CuAlO_2 + 3Cu + 2CH_4 \uparrow + CH_{ads} \qquad \textit{Equation 4-6}$$

Once the substrate is reduced to Cu^0, the surface is inactive for further TMA adsorption and decomposition. Thus, as ALD deposition continues, TMA reacts with the Cu_2O and copper aluminate (Figure 4.11 (b),(c)) and once all the Cu_2O is consumed, TMA continues to react with copper aluminate [74]. Equation 4-7 is the first half cycle with O_2.

$$2Cu + 2CuAlO_2 + 2CH_{ads} + 3\ O_2 \rightarrow 2Cu_2O + Al_2O_3 + 2\ CO_2 \uparrow + 2H_2O \uparrow \qquad \textit{Equation 4-7}$$

Thus, ALD Al_2O_3 has the potential of not only passivating Cu, but also reducing the native oxide on the copper surface.

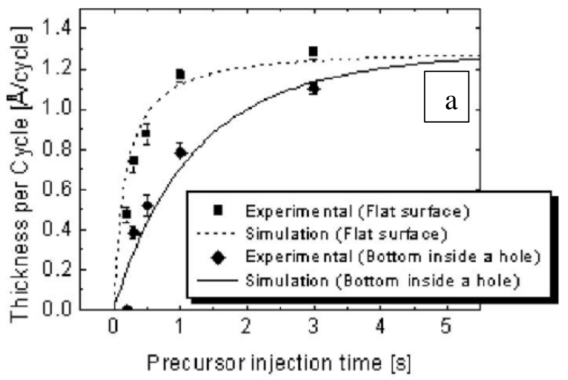
4.5.1 Parameters Effecting ALD Step Coverage

Even though ALD has excellent step coverage, especially when compared to other CVD methods, there are parameters that can improve the step coverage of the ALD film [75]. Equation 4-8 describes the relationship between ALD deposition parameters and film thickness variation on the substrate [75].

$$T^{q}_{f\ or\ h(r,\varphi,z)} = r\left\{1 - exp - \frac{S(0)J^{q}_{f\ or\ h(r,\varphi,z)}}{K_{max}} t_{p.t}\right\} \qquad \textit{Equation 4-8}$$

Where $T^{q}_{f\ or\ h(r,\varphi,z)}$ is thickness of the ALD film at qth cycle at position $h(r,\varphi,z)$ or on a flat surface, $S(0)$ is initial sticking probability, $J^{q}_{f\ or\ h(r,\varphi,z)}$ is precursor flow rate, $t_{p.t}$ is injection time, K_{max} is Max. No. of chemisorbed precursor/ unit area, and r is saturated film thickness per cycle. From Equation 4-8, it can be seen that increasing precursor injection time (t_p) and flux rate ($J^{q}_{f\ or\ h(r,\varphi,z)}$), improves the step coverage of the film given other parameters being constant [75].

Figure 4.12 (a) [75] shows the simulation and experimental results for the relation between precursor injection time and film thickness, with increasing injection time, the thickness of the film on a flat surface and a point in the bottom of a hole converge to similar values [75]. Similae trend is observed for increasing of the precursor flux rate at a constant injection time (Figure 4.12 (b)), increasing the injection time results in film thickness values at a flat surface and a position at the bottom of the hole reach similar values [75].



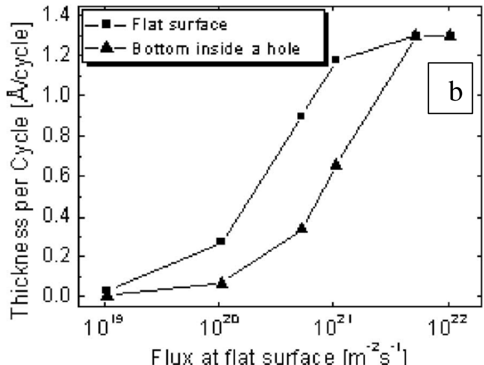


Figure 4.12 dependence of the film thickness per cycle at the flat surface and at the bottom inside a hole on precursor injection time (a), film thickness per cycle at the flat surface and at the bottom inside a hole as a function of J_f^q (b) .(Adapted with permission from AIP publishing) [75]

4.6 ALD Al_2O_3 for Si-IF Passivation

To evaluate the effectiveness of the Al_2O_3 on preventing Cu oxidation, blanket copper samples on Si substrate were prepared. First, SiO_2 was thermally grown on Si (100) wafer for 3 μm and then Ti (20 nm)/Cu (100 nm) seed layer were sputtered following with Cu electroplating for 1 μm. The wafer was diced into sample coupons of 1.5 cm x 1.5 cm, and then each coupon sample was passivated with Al_2O_3 of different thicknesses. Table 4-10 is the process parameters of the ALD process. XRD was used to evaluate samples before humidity testing. Samples were exposed to 85% RH at 85 °C for 216 hours. XRD was performed on the samples post testing to identify any oxide formation.

Table 4-10 ALD process parameters

T(K)	TMA Pulse (s)	TMA Purge (s)	H_2O Pulse (s)	H_2O Purge (s)
473	0.06	10	0.06	10

Figure 4.13 is the XRD scan of the samples passivated with 10,11 and 12 nm of Al_2O_3 after 216 hours of humidity testing and pristine sample passivated with 10 nm of Al_2O_3. No copper oxide peaks were detected in passivated samples after 216 hours of humidity testing which shows that films with thicknesses of 10 nm and above are effective in protecting copper from oxidation. The results are consistent with other studies that studied Al_2O_3 for Cu passivation [76].

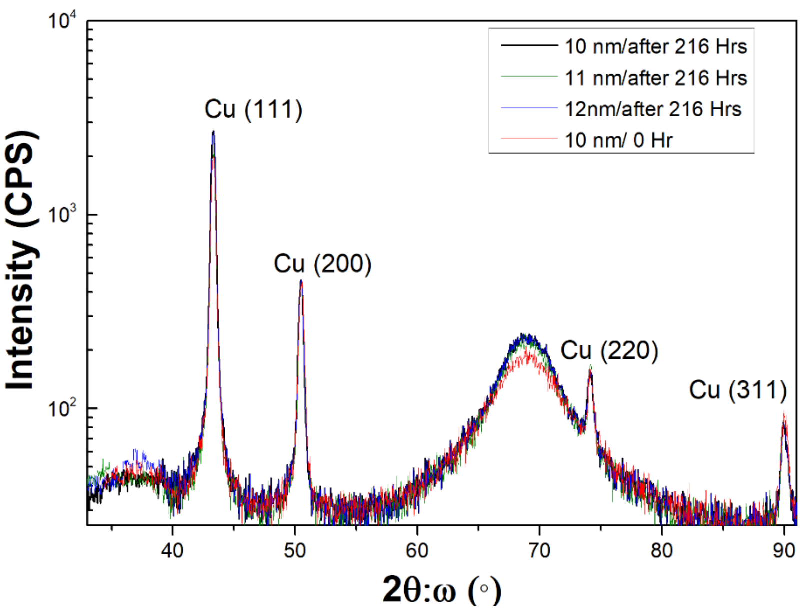


Figure 4.13 XRD scan of the blanket Cu samples passivated with 10,11 and 12 nm of Al_2O_3 after 216 hours of humidity testing in comparison with pristine sample. No oxide peak is detected in passivated samples after testing.

one of the advantages of using ALD is the high uniformity achieved with this deposition process. Thin film growth is not limited with small mean free path and self-limiting nature of the process prohibits the precursor from nonuniform deposition. To study film uniformity of ALD Al_2O_3, bonded Si-IF sample was coated with 40 nm of Al_2O_3, and FIB was used to study the film uniformity across the sample (Figure 4.14). Figure 4.14, illustrates that the thickness of Al_2O_3 film does not change from the top of the die to the interface of the Si-IF and die. This is an important observation which confirms the conformality of the ALD process for a uniform coating of the assembly.

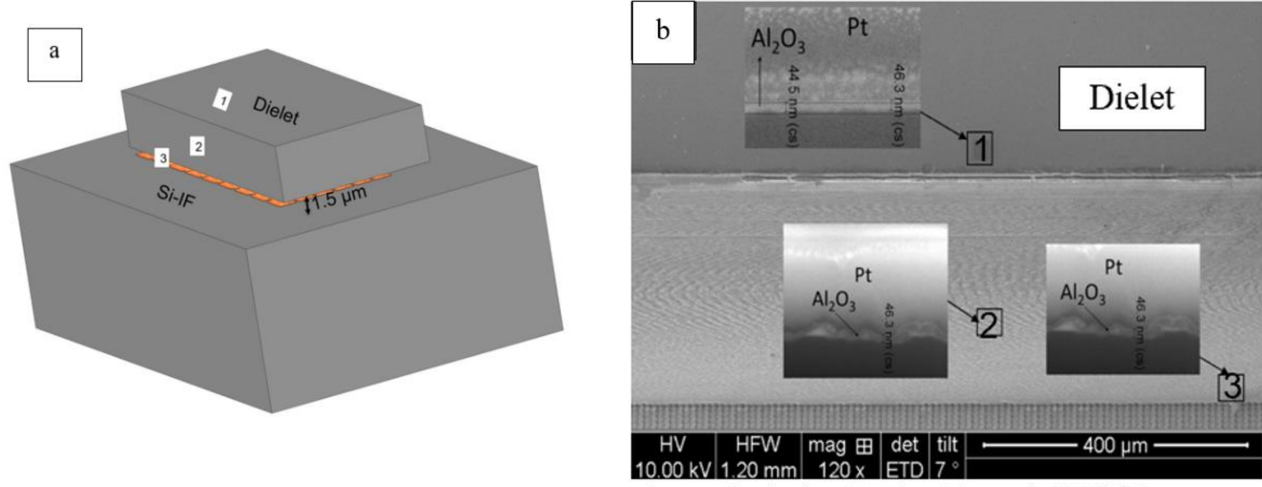


Figure 4.14 a schematic of the bonded Si-IF with measurement points (a), Al_2O_3 thickness remains constant from top of the bonded die ([1]) to sidewall ([2]) and the interface of the die and Si-IF ([3]) at around 46 nm (b).

To evaluate the effectiveness of the ALD Al_2O_3 in protecting exposed Cu in bonded samples from oxidation, bonded samples with daisy chain structures passivated with 17 nm of Al_2O_3 were exposed to humidity testing (85 °C/85% RH) for 216 hours and their electrical resistance before and after humidity were compared. Table 4-11 is the summary of the resistance of the daisy chains which show that the average change in the resistance of the dais chains was less than 5%. Thus, Al_2O_3 was effective in reducing oxidation in exposed Cu in bonded Si-IF samples. However, due to the resistance change observed after humidity testing, more characterization was done to measure the uniformity of the thin film under the die.

Table 4-11 *electrical resistance of the daisy chains before and after 216 hours of humidity testing.*

Pad No.	Resistance before humidity testing (Ω)	Resistance after 216 hours of humidity testing (Ω)
1-2	6.14	6.16
3-4	6.23	6.41
5-6	6.19	6.21
7-8	6.81	6.82
9-10	6.21	6.5

To that end, energy-dispersive X-ray spectroscopy (EDX) was used to measure Al content under a die at different positions from one edge to another. Figure 4.15 (a) is an SEM image of a segment of the sheared die, showing Cu pads and pillars' impressions. EDX measurement was done at multiple points along the width of the die as well as different positions from one edge of the die to another. The percentage of atomic concentration of Al_2O_3 decreases from the edge of the die towards the center and remains constant before reaching the original percentage at the other edge (Figure 4.15 (b)).

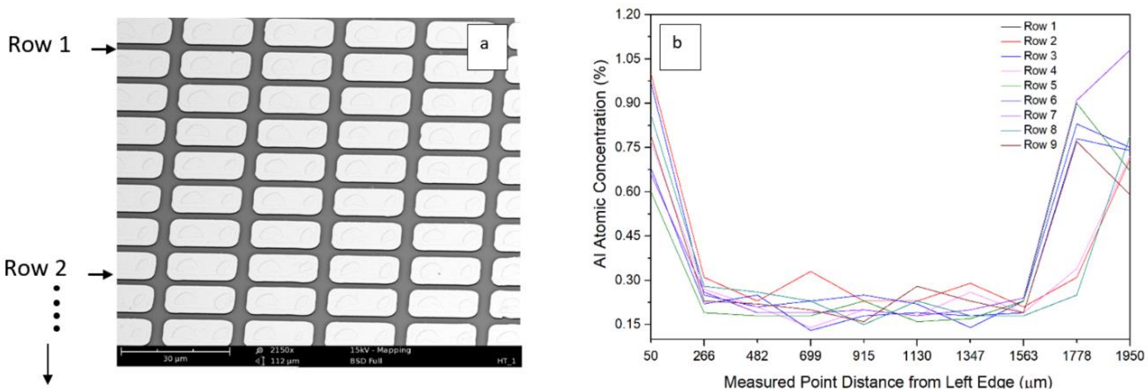


Figure 4.15 a section of the die showing pads and measured points in two rows (a), atomic concentration of Al under a die from one edge to another at different position (b).

This thickness variation can be attributed to the high pillar density under the die that act as scattering points for TMA precursor. Thus, ALD deposition process was optimized to allow for a longer wait time and consequently, allowing TMA molecules to penetrate deeper under the die and achieve the required step coverage.

Knowing the effect of increasing the precursor injection time and flux rate on improving the ALD film step coverage, the TMA injection time was increased from 0.06 s to 0.12 s and the flux rate was increased from 100 sccm to 140 sccm. Al_2O_3 deposition was done on a bonded sample for 200 cycles (thickness of 20 nm) and after deposition, the die was sheared off and this time, the thickness of the Al_2O_3 was directly measured on the pads in the middle of the die and on a pillar

on the substrate side under the die. Figure 4.16 is an SEM image of a segment of the die showing broken pillars and the pads. Figure 4.17 shows the FIB cross section of a pad and Al_2O_3 thickness of 11.4 nm on top of it.

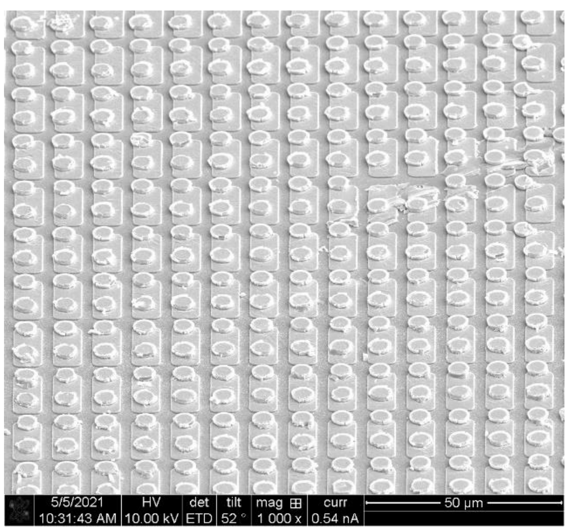


Figure 4.16 SEM image of a segment of the die showing broken pillars and pads.

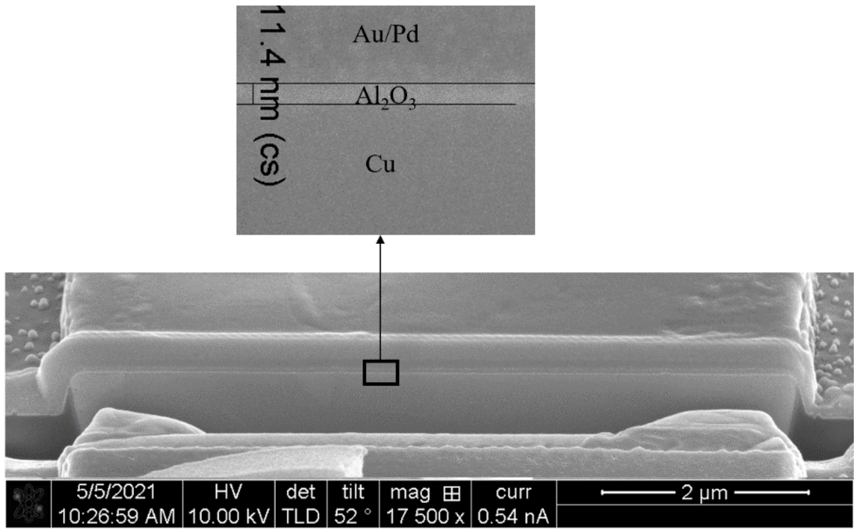


Figure 4.17 Al_2O_3 thickness on an internal pad on the die after shearing off the bonded sample is 11.4 nm which is adequate to protect copper from oxidation.

After ensuring the uniformity of the passivating film is adequate to coat exposed copper under the die. New bonded samples with daisy chain structure (2x2 mm^2 with 180 chains with 180 pillars in each link) were passivated using the modified ALD recipe with 20 nm of Al_2O_3 and were subjected to humidity testing, this time for 564 hours, the electrical resistance of the daisy chains was measured every 94 hours. Figure 4.18 shows the change in the electrical resistance of two daisy chain samples during the humidity testing. Maximum change in electrical resistance was less than 3%. Meanwhile the change in the electrical resistance of a similar sample with no passivation changed from 4.5 Ω to more than 33 Ω during the same period of testing (Figure 4.19).

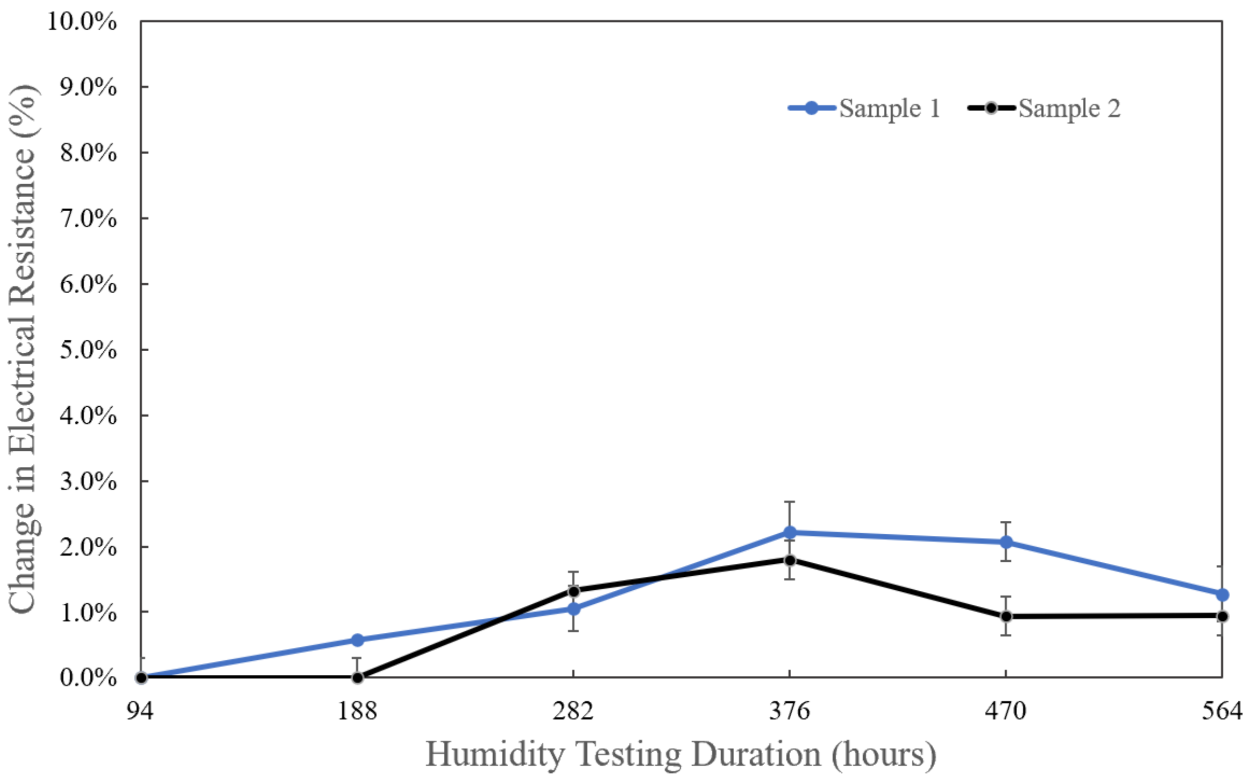


Figure 4.18 percentage of change in electrical resistance of the daisy chain samples in 564 hours of humidity testing.

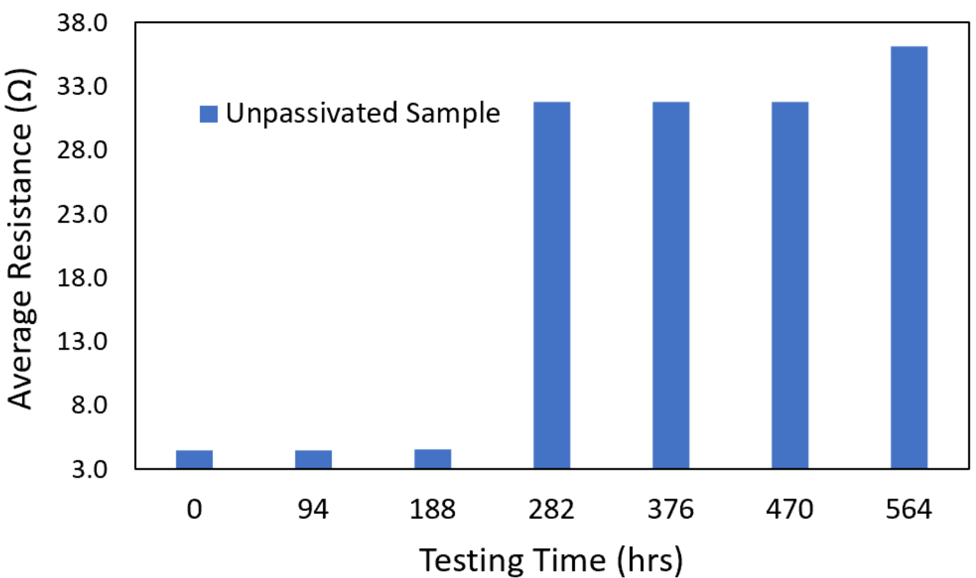


Figure 4.19 percentage of change in electrical resistance of the daisy chain of an unpassivated sample in 564 hours of humidity testing. The electrical resistance changed from 4.5 Ω to more than 33 Ω.

Figure 4.18 and Figure 4.19 show that the modified ALD recipe allows for reliable coating of the exposed copper and protect them from oxidation.

4.7 Effect of Passivation on Thermomechanical Stresses

As mentioned in chapter 3, thermal stresses are one of the major reliability concerns in electronic packaging. Because of CTE mismatch between different materials in the system, thermal residual stresses accumulate. These residual stresses can be the source of failure in the packaging. Since the number of materials in Si-IF are limited, thermal residual stresses are minimal in the system. Table 4-12 is a summary of the coefficient of linear thermal expansion of the materials used in Si-IF at room temperature.

Table 4-12 CTE of the materials used in Si-IF.

Material	Cu	Si	SiO_2	SiN_x	Al_2O_3
CTE (ppm/ °C)	17 [77]	2.64 [78]	0.56 [79]	3.27 [80]	8.1 [81, 82]

The finite element analysis was used to study thermal residual stresses within Cu pillars with and without passivation. Figure 4.20 is the structure set up for ANSYS simulation. A copper pillar with 5 µm diameter and height, bonded to two Cu pads was simulated. Different passivation materials as well as pillar with no passivation were modeled. Mesh size was 0.5 µm for the pads and pillar and 0.1 µm for the passivation thin film. Pads were fixed at top and bottom surface.

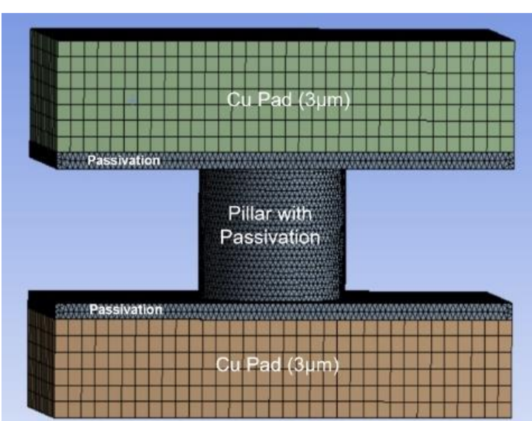


Figure 4.20 meshed structure showing pads (3 µm) and pillar (Ø= 5 µm, h=5 µm) with passivation (0.5 µm).

Figure 4.21 (a) illustrates the thermal residual stresses along a Cu pillar with no passivation when it is cooled down from 200 °C to 22 °C. Stress varies from -48 MPa at the interface of the Cu pads and the pillar to 1.5 MPa in the middle of the pillar.

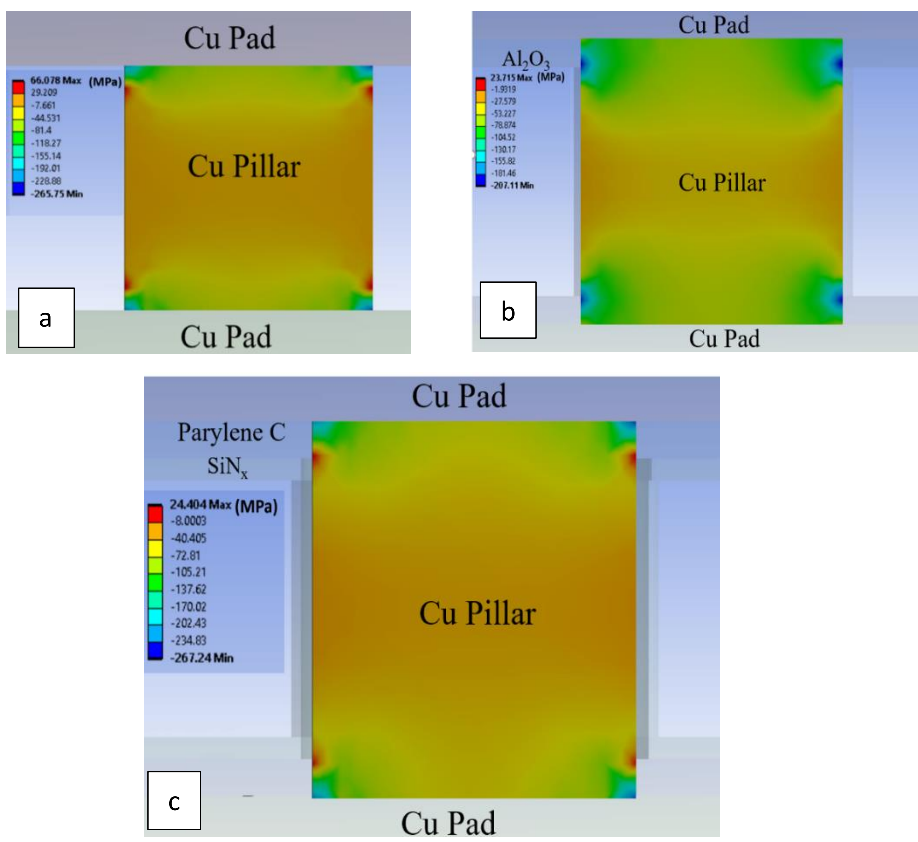


Figure 4.21 residual thermal stresses in the pillar with no passivation (a), with Al_2O_3(b), and bilayer passivation (c).

Addition of 0.5 µm of Al_2O_3 increases the compressive stress within the pillar, the stress distribution profile remains similar to no passivation structure (Figure 4.21 (b)). A bilayer of Parylene C (0.5 µm) and SiN_x (0.2 µm) forms a more compressive stress along pillar compared to no passivation, however; effect of Al_2O_3 in pushing the stresses further into compressive region is more pronounced (Figure 4.21 (c)).

High tensile stresses in the passivation film, especially at the interface of Parylene C and SiN_x, may result in delamination and cracking of the thin films (Figure 4.22 (a) and (b)). Thus, Finite element analysis show that addition of the encapsulation to the Si-IF increases compressive thermal residual stresses along the pillar which is beneficial in increasing the reliability of the bonded samples. However, stress distribution at the interface between Parylene C and SiN_x changes abruptly, which may result in delamination of Parylene C and SiN_x and degradation the passivation.

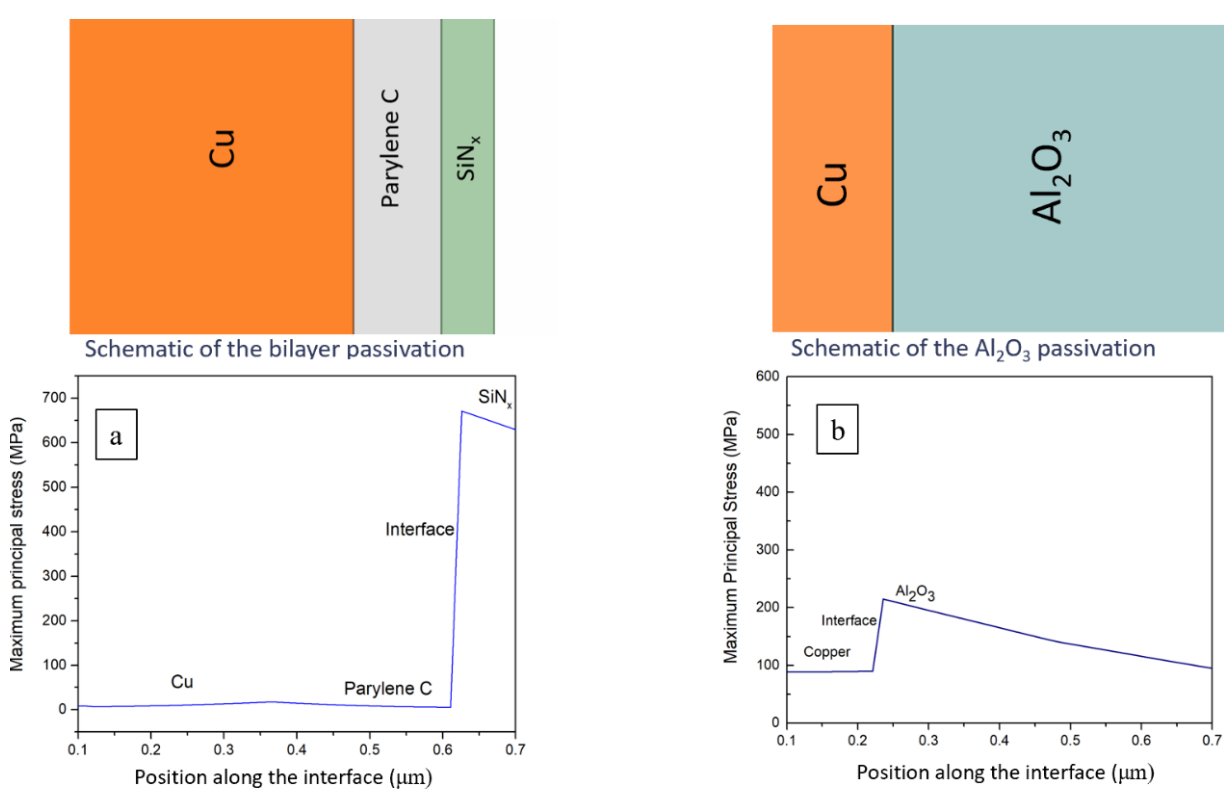


Figure 4.22 stresses at the Parylene C/SiN_x interface (a) and Cu/Al_2O_3 interface (b)

From above results, it is evident that Al_2O_3 in fact an effective passivation for protecting Cu from oxidation within bonded Si-IF samples. One drawback of Al_2O_3 is the low thermal conductivity of the film which may result in limitations in thermal management. Another

alternative to Al_2O_3 is AlN which has all the advantages of Al_2O_3 as well as higher thermal conductivity. A more detailed discussion is given in chapter 7.

4.8 Summary

The passivation of Si-IF was discussed in this chapter. First a detailed discussion of kinetics of copper oxidation was presented. It has been shown that copper readily oxidizes even at room temperature and the activation energy for oxidation decreases in oxidizing environment. The two common types of copper oxides are Cu_2O and CuO.

In Si-IF, there can be some exposed copper under the die due to misalignment that can occur during TCB process, that leaves copper exposed to the environment and in the absence of any passivation, that may lead to excessive oxidation and failure of the interconnects. Thus, it is crucial to develop a novel passivation to protect the exposed Cu from oxidation.

Three different types of passivation were studied. The first study was on the use of Parylene C with two different thicknesses (1 and 3 μm). Parylene C has many advantages including room temperature deposition process and conformality but because it is an organic film, its water vapor transmission rate is much higher than an inorganic film such as SiN_x. Moreover, as an organic material, the CTE of Parylene C is much larger than other materials in the system. Because of these limitations, a multilayer of Parylene C and SiN_x was studied. This passivation system is effective in protecting copper from oxidation. However, Since PECVD process does not have a good step coverage to allow for coating of the exposed copper under the bonded dies, there exist a need for a deposition process with an excellent step coverage.

To achieve this requirement, ALD process was used to deposit Al_2O_3 as passivation. Experimental results of passivating blanket copper samples with different thicknesses of Al_2O_3

and subjecting them to humidity testing (85 °C/85% RH) revealed that Al_2O_3 with thicknesses of 10 nm and above are effective in protecting copper from oxidation. The ALD recipe was modified to allow for longer penetration time for the precursor for a conformal coating of the bonded samples.

Humidity testing of the passivated samples with the modified recipe for 564 hours showed that the maximum change in the electrical resistance in the samples was less than 3% which shows that this passivation is in fact effective in protecting bonded samples from degradation due to moisture ingress.

The finite element analysis of Cu pillar with these three passivation systems shows that residual thermal stresses remain in compressive regime for all three systems, however, there is a large tensile stress at the interface of the Parylene C/SiN_x when the assembly is cooled down from 200 °C to 20 °C which may lead to delamination and degradation of the passivation film. Thus, Al_2O_3 film has another advantage of lower interfacial stresses as compared to the multilayer passivation and is the passivation that is developed and used for Si-IF.

5. Thermomechanical Stresses

Failure due to temperature (steady state or temperature cycling) is one of the major failure modes in electronic packaging. A survey of failure modes in electronic equipment showed that about 55% of failures are thermally induced [30].

These failures can occur due to CTE mismatch in the system, in any electronic packaging there are different organic and inorganic materials with large CTE mismatches and/or anisotropic CTE properties. Thus, when the system goes through temperature variation due to operation or environment, a considerable amount of stress builds up in the system that can lead to crack initiation at stress concentrated regions and subsequent crack growth and failure follows.

In this chapter, the experimental results of temperature cycling of Si-IF is presented. Moreover, the finite element analysis of thermomechanical stresses in a wafer scale system with Si-IF as the building block is presented and the effect of design parameters including substrate thicknesses and material are investigated.

5.1 Temperature Cycling of Si-IF

Si-IF has a robust reliability property, especially in terms of thermomechanical stresses. This is due to smaller CTE difference between materials in the system, since all the organic materials including PCB, underfill, and overmold is removed from the assembly. Moreover, elimination of solder joints removes the complexity of IMC formation and fatigue failure due to temperature induced microstructural changes. These complexities are discussed in more details in next sections.

However, it is important to evaluate effect of temperature cycling on bonded Si-IF samples to verify the robustness of the system experimentally.

To that end, Si-IF bonded samples with ALD Al2O3 passivation was subjected to temperature cycling in accordance with JESD22-A104 [7]. Table 5-1 lists different testing conditions in accordance with JESD22-A104, condition G (-40 °C/+125 °C) was used in for this study. The testing was done in ESPEC SH242 environmental chamber. The sample was tested for 100 cycles and the change in the electrical resistance of the daisy chain was measured every 10 cycles.

Table 5-1 temperature cycling testing conditions (JESD22-A104) [7].

Test Condition	Nominal $T_{s\ (min)}$ (°C)	Nominal $T_{s\ (max)}$ (°C)
A	-55	+85
B	-55	+125
C	-65	+150
G	-40	+125
H	-55	+150
I	-40	+115
J	0	+100
K	0	+125
L	-55	+110
M	-40	+150
N	-40	+85
R	-25	+125
T	-40	+100

Figure 5.1 is the percentage change in electrical resistance in the sample during testing, maximum change in the electrical resistance was less than 8%. The results show that bonded Si-

IF samples have a robust temperature cycling reliability due to limited range of CTE of the materials in the system and lack of organic materials.

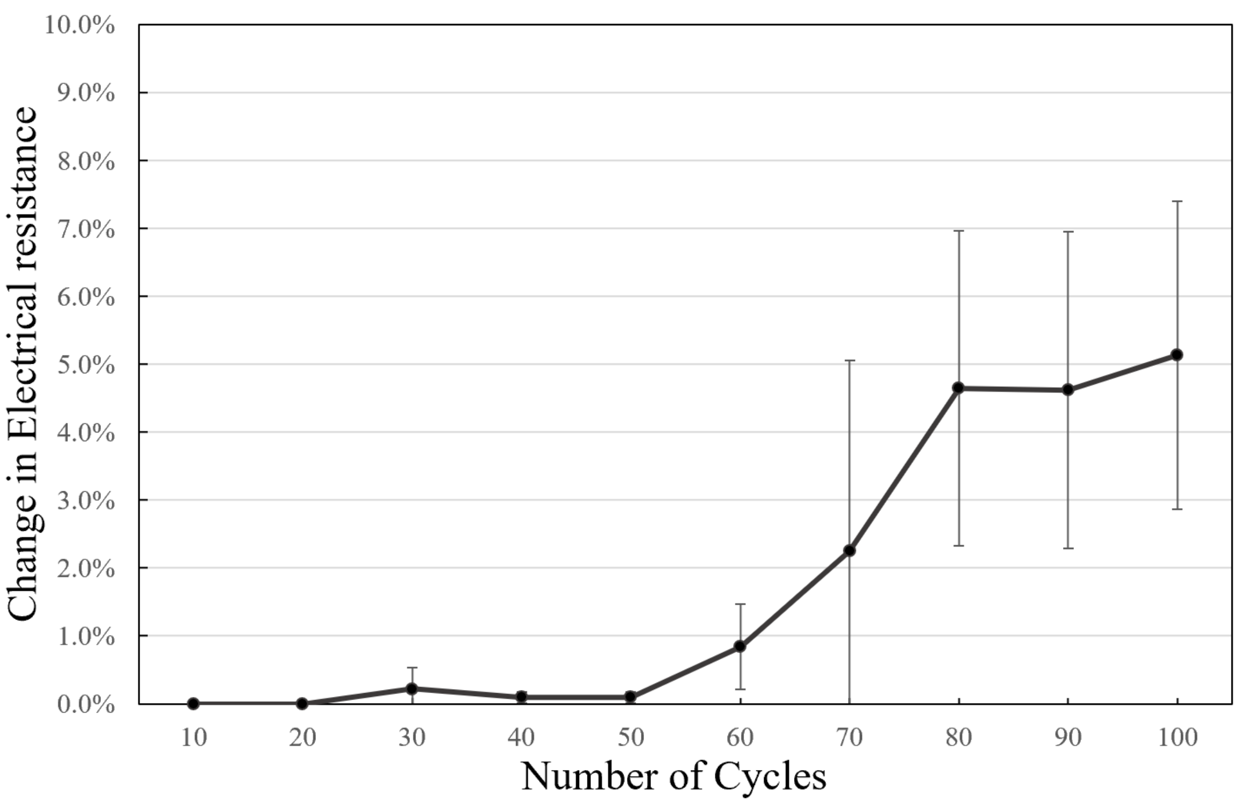


Figure 5.1 change in electrical resistance of the daisy chains over 100 cycles of temperature cycling (+125°C/-40°C). Maximum change in the electrical resistance was less than 6%.

5.2 Thermomechanical Stresses in Wafer Scale System

The thermomechanical stresses are a major issue in wafer scale system due to several factors including:

1- The number of materials in the system including solder alloys, PCB, and other organic materials such as underfill and overmold,

2- Large dimension of the wafer results in larger stress accumulation in corner solder joints. As mentioned in earlier chapters, the corner solders that have the largest DNP, experience higher

stresses and these stresses can reach very high levels and lead to failure in the case of wafer scale systems.

Thus, it is important to address these challenges during the design process.

There has been a lot of efforts to estimate the fatigue life of the system under a specific stress gradient. The Coffin-Manson model (Equation 5-1) is one of the most common models used for mechanical failure material fatigue and material deformation prediction. It establishes the relationship between the cycles to failure and temperature profile [83].

$$AF = \left(\frac{\Delta\gamma_2}{\Delta\gamma_1}\right)^{\beta} \left(\frac{f_1}{f_2}\right)^{\kappa} \left(\frac{G(T_{max})_1}{G(T_{max})_1}\right) \qquad \textit{Equation 5-1}$$

where AF is the acceleration factor, term 1 is the effect of strain, term 2 is the effect of frequency and term 3 is the effect of material composition. In the next sections, the effect of materials composition and microstructure on the temperature cycling properties of solder joints are discussed.

5.2.1 Effect of Solder Composition

SAC solder series are the most commonly used solder alloys out of all the Pb free solder compositions proposed in the last decade or so as shown in Figure 5.2 [84]. The most popular SAC are the near eutectic alloys, which consist of 3.0–4.0% of Ag and 0.5–1.0% of copper [84].

The formation of intermetallic compounds between the primary elements Sn and Ag, and Cu affects all the properties of the alloys, Figure 5.3 (a) and (b) show the binary phase diagrams and possible intermetallic compounds that can be formed: Ag_3Sn due to the reaction between Sn and Ag and Cu_6Sn_5 from the interaction between Sn and. However, if the Cu content is not high enough, Cu_3Sn will not form at the eutectic point unless for the formation at higher temperatures, thus in bulk samples, Cu_3Sn is not present [84].

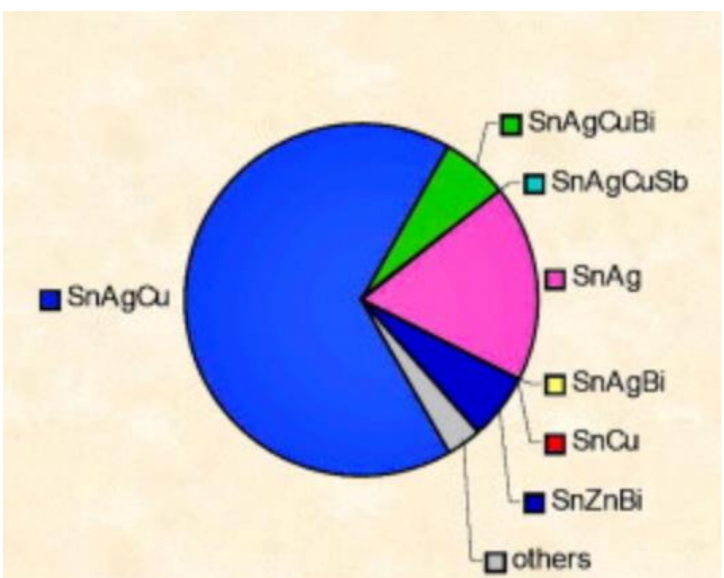


Figure 5.2 market share of different lead-free solders (Adapted with permission from Elsevier Ltd.) [84].

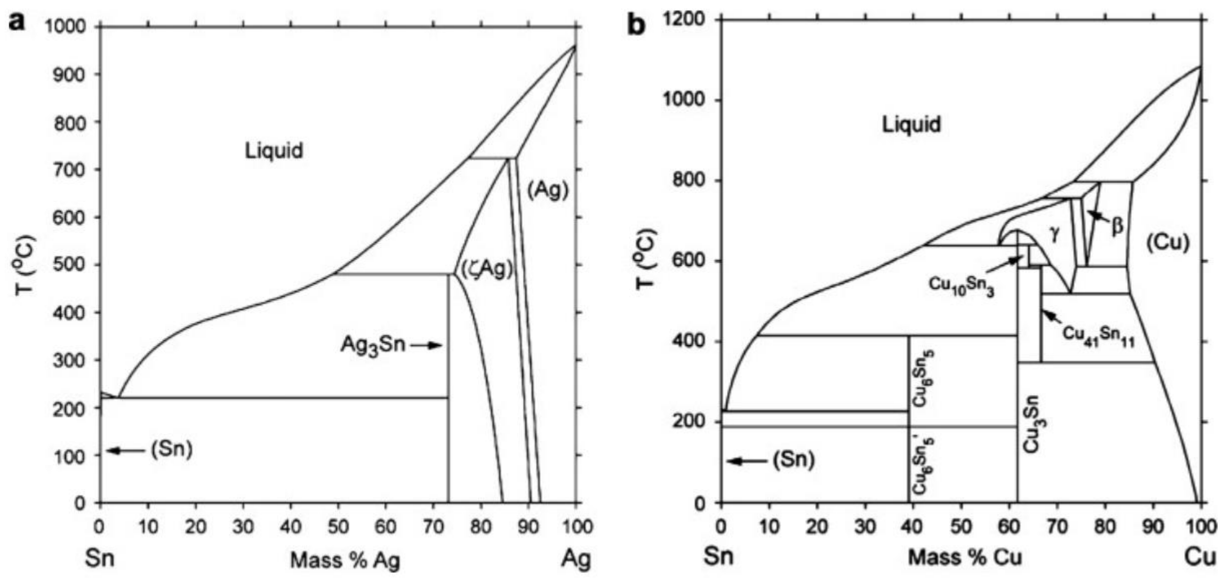


Figure 5.3 binary phase diagram (a) Sn–Ag and (b) Sn–Cu (Adapted with permission from Elsevier Ltd.) [84].

Investigation of the microstructure of the SAC alloys revealed that composition has three main effects on the reliability and mechanical properties of the solder joints [84]:

1. Initial microstructure: increase of Ag increases the Ag_3Sn dispersoids (Figure 5.4). Sn primary grain size decreases with increasing Ag, Ag_3Sn particles strengthen the Sn matrix through precipitation hardening [84].

2. Recrystallization: happens due to thermal strain and elevated temperature, higher Ag content results in suppression of grain growth thus the fatigue reliability of the solder joint is improved with increase of the Ag content (Figure 5.5, Figure 5.6) [84].

Grain orientation: Sn has anisotropic properties, Table 5-2 illustrates mechanical properties of the Sn for different orientations. Thus, number and orientation of Sn grains affect the reliability of the solder joints.

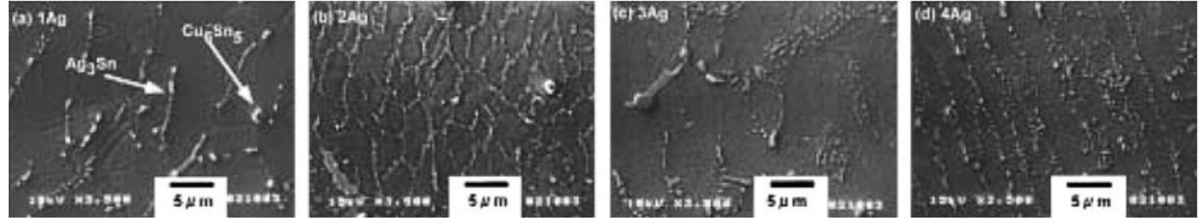


Figure 5.4 microstructure of Sn-xAg-0.5Cu with 1-4% Ag (a-d) before temperature cycling (Adapted with permission from Elsevier Ltd.) [84].

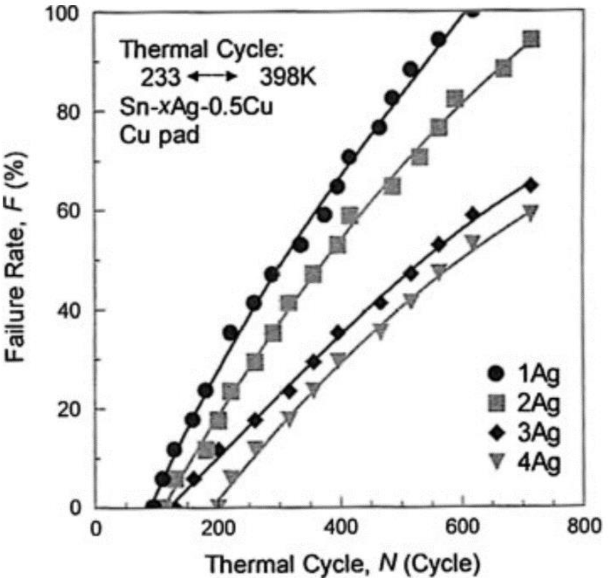


Figure 5.5 temperature cycling reliability of Sn-xAg-0.5Cu for different Ag content (Adapted with permission from Elsevier Ltd.) [84].

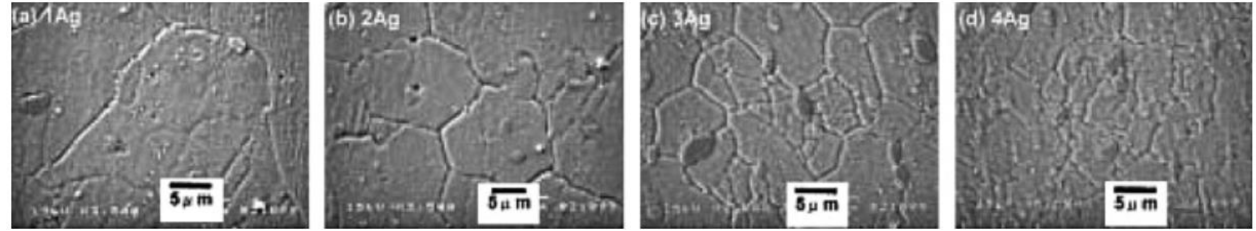


Figure 5.6 microstructure of Sn-xAg-0.5Cu with 1-4% Ag (a-d) after temperature cycling (Adapted with permission from Elsevier Ltd.) [84].

Table 5-2 Sn Properties in different directions [84].

Direction	CTE (ppm/°C)	Young's Modulus (GPa)
[001], [010]	15.4	23
[100]	30.5	70

Thus, it is important to investigate the effect of solder composition on reliability of the solder joints. However, apart from the composition of the solder joints, the microstructure of the solder alloy plays an important role in the reliability and solder alloy lifetime prediction.

5.2.2 Effect of Microstructure on Solder Alloy Constitutive Models

One of the most common constitutive models used for lead-free solder alloys is called Anand model. There are nine parameters in this model.

There are two basic assumptions in the model, the first assumption is that the model does not require an explicit yield condition and that the plastic strain happens at all nonzero values, however, the rate of the plastic flow is very small at low stress levels. Second feature is that the model utilizes a scalar parameter to represent the isotropic resistance to plastic deformation due to internal state of the material [85]. The scalar parameter is denoted by s and is known as the deformation resistance and has the unit of stress. S is proportional to equivalent stress [85]:

$$\sigma = cs \quad c < 1 \qquad \textit{Equation 5-2}$$

$$c = \frac{1}{\xi} sinh^{-1}\left[\left(\frac{\dot{\varepsilon}_p}{A} e^{\frac{Q}{RT}}\right)^m\right] \qquad \textit{Equation 5-3}$$

Where $\dot{\varepsilon}_p$ is the inelastic strain rate, A is material constant, Q is the activation energy, *m* is the strain rate sensitivity, ξ is the stress multiplier, R is the gas constant and T is the absolute temperature. Strain rate is defined as:

$$\dot{\varepsilon}_p = Aexp(-\frac{Q}{RT}) \left[\sinh (\xi \frac{\sigma}{s}\right]^{1/m} \qquad \textit{Equation 5-4}$$

And the evolution equation for the internal variable s is defined as follow:

$$\dot{s} = g(\sigma, s, T)\dot{\varepsilon}_p \qquad \textit{Equation 5-5}$$

Where $g(\sigma, s, T)$ is related to strain hardening and dynamic recovery and can be expanded as follow:

$$\dot{s} = \left\{h_0 \left|1 - \frac{s}{s^*}\right|^a . \mathrm{sign}\ (1 - \frac{s}{s^*})\right\} . \dot{\varepsilon}_p \quad a>1 \qquad \textit{Equation 5-6}$$

Where h_0 is the hardening/softening constant, a is the strain rate, s^* is the saturation value of s. s^* is also defined as:

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon}_p}{A} \exp\ (\frac{Q}{RT})\right]^n \qquad \textit{Equation 5-7}$$

Where $\hat{s}$ is a coefficient and n is the strain rate sensitivity for deformation resistance saturation value [85].

There has been a lot of studies to determine these nine parameters for different solder alloys, and the values of these studies are sometimes very different from one to another for the same type of alloy. One of the reasons for these discrepancies is the differences in sample preparation process that leads to different microstructures and thus the results vary. Moreover, it has been shown that aging of the solder alloy results in grain and phase coarsening ad well as recrystallization. Thus, any preconditioning of the samples before testing will also affect the experimental results. Basit et al. [86] studied the most common lead-free solder alloy with various microstructures, including reflow, water quenched, and aged alloys, Table 5-3 is the summary of the parameters they extracted for SAC 205,305,405 [86]. These parameters were utilized in the finite element analysis studies presented in the following section.

Table 5-3 Anand parameters for SAC 205, 305 and 405 for reflowed (RF) and water quenched (WQ) [86]

Anand parameters	Unit	SAC 205		SAC 305		SAC 405	
		WQ	RF	WQ	RF	WQ	RF
S_0	MPa	27.9	16.5	32.2	21.0	34.35	23.65
Q/R	1/K	9080	9090	9320	9320	9560	9580
A	Sec^{-1}	3200	4300	2800	3501	2650	3175
ζ	-	4	4	4	4	4	4
m	-	0.28	0.238	0.29	0.250	0.3	0.263
h_0	MPa	174,000	169,000	186,000	180,000	192,000	183,000
$\hat{s}$	MPa	43	29	44.67	30.2	45.51	31.3
n	-	0.0115	0.0087	0.0120	0.0100	0.0123	0.011
a	-	1.75	1.84	1.72	1.78	1.7	1.77

5.3 FEA Analysis of Wafer Scale System under Temperature Cycling

Due to a large variation in CTE of different materials in wafer scale systems, large stress levels may accumulate in solder joints during to temperature variations. To prevent excess stresses within the solder joints, addition of a flexible substrate to allow for relaxation of the stresses and improving the reliability of the overall system have been studied utilizing finite element analysis. Three different designs were considered, in the first design , Si-IF is bonded to PCB. In the second design, an elastomer is used as a buffer layer between Si-IF wafer and PCB power board, and the third design is where PCB power board is segmented, and each segment has a 30 mm x 30 mm dimension. These PCB pieces were embedded in the elastomer. The material used as the elastomer is Polydimethylsiloxane (PDMS) which is a mineral-organic polymer that is widely used in MEMS and biomedical applications [87]. It is a thermoset polymer in which its mechanical properties can be tuned by changing the ratio of the elastomer and crosslinking agent. In this study, the material

properties of 10:1 PDMS (10 parts elastomer base and 1 part curing agent) was used. Table 5-4 is the summary of the material properties used in this simulation, finite element analysis was done using ANSYS 2020 R1.

Table 5-4 material properties used in FEA simulation.

Material	Density (Kg/m^3)	CTE (ppm/°C)	Young's Modulus (Pa)	Poisson's ratio
PDMS	1100	300	$5x10^5$	0.48
Si	2339	2.4	$1.4x10^{11}$	0.265
SAC 405	7500	20	$44.\ x10^{10}$	0.35
FR4	1840	X: 12.5 Y: 11.4 Z: 82	X: $2x10^{10}$ Y: $1.8x10^{10}$ Z: $1.5x10^{10}$	XY: 0.11 YZ: 0.09 XZ: 0.14

To save on computing power and increase the accuracy of the simulation, a quarter symmetry design was utilized. Figure 5.7 (a) is the model for the first design showing Si-IF (Si wafer) and PDMS buffer layer and the cross section of the model showing the solder dimension and pitch (Figure 5.7 (b)).

Before starting temperature cycling simulation, mesh dependency analysis was done to ensure that the simulation results are not dependent on the mesh size but rather the boundary conditions of the simulations . Figure 5.8 (a) shows the number of elements vs. mesh size and Figure 5.8 (b) is the change in the stress with changing the mesh size. After concluding the optimum mesh size, temperature cycling simulations were performed using the optimized mesh size value.

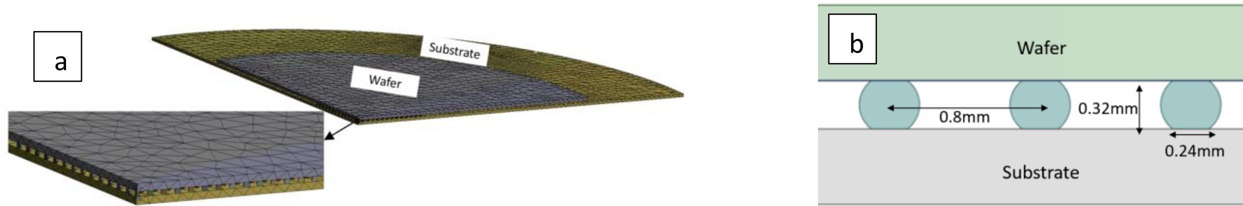


Figure 5.7 FEA model of the simulated system showing substrate, wafer (Si) (a) and cross section of solder joints showing the solder dimension and pitch (b).

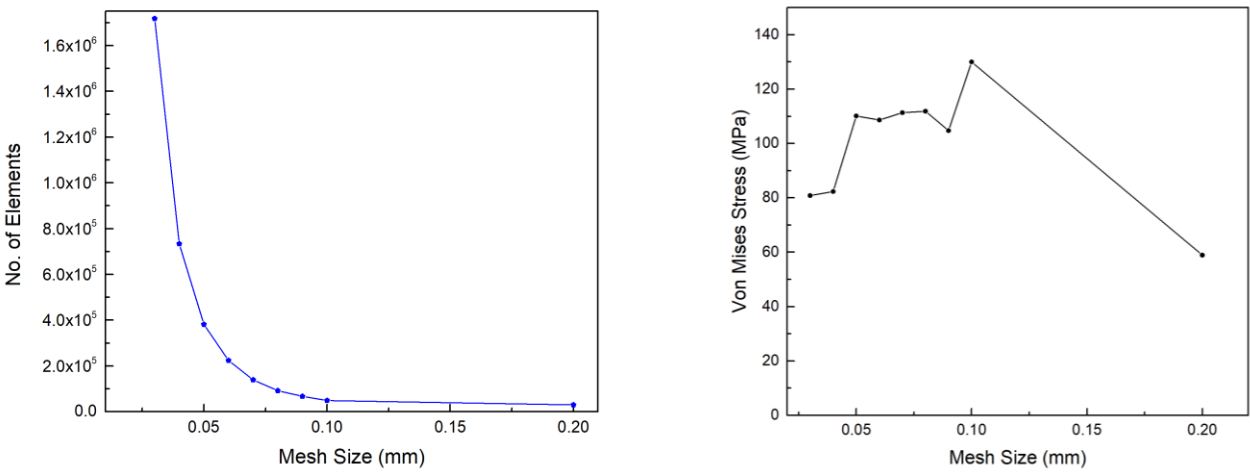


Figure 5.8 No. of elements vs. mesh size (a) and change in Von Mises stress vs. mesh size (b).

Figure 5.9 is the cross section of the first model, where PCB board is directly connected to Si-IF wafer using solder joints. Figure 5.10 is the cross section of the Si-IF attached to PDMS buffer layer and Figure 5.11 is the cross-section design of the PCB embedded in PDMS connected to Si-IF.

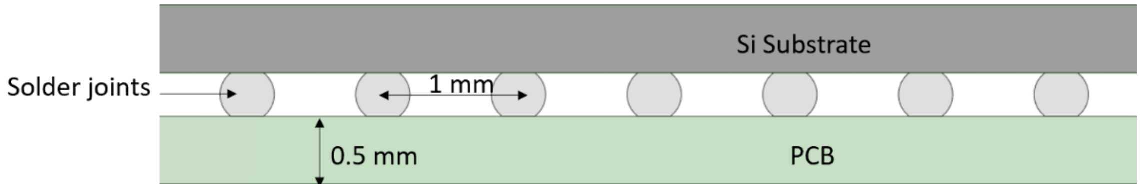


Figure 5.9 cross section of the model showing Si-IF bonded to PCB through solder joints.

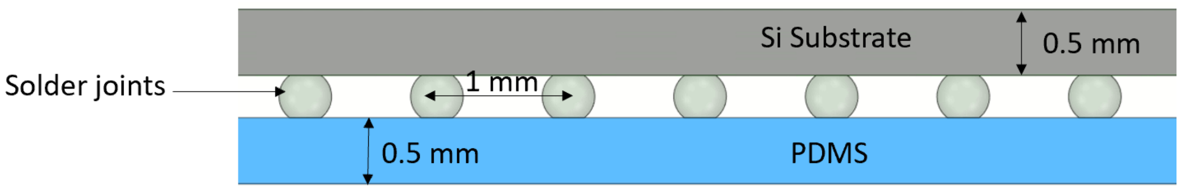


Figure 5.10 cross section of the model showing Si-IF bonded to PDMS buffer layer through solder joints.

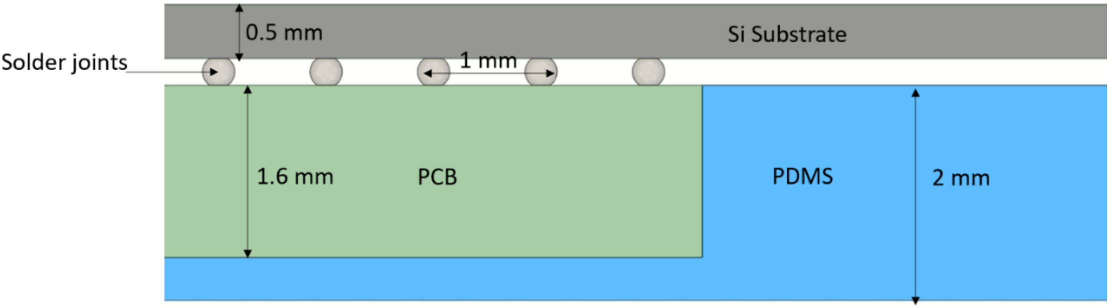


Figure 5.11 cross section of the third model where PCB pieces are embedded in PDMS and attached to Si-IF

Figure 5.12 shows the simulation results for Von Mises stresses within two different proposed structures compared with FR4. The simulation confirms that the stresses in solder joints is the highest when FR4 is attached directly to Si due to the large CTE mismatch between the two entities and lack of flexibility in them. However, addition of PDMS as a buffer layer between Si and FR4, reduces the stress levels. This stress reduction is due to elastomer properties of PDMS that allows for the buffer layer to accommodate for the stress build up due to temperature variation. Embedding PCB pieces in the PDMS helps with reduction of stress levels within the solder joints as well.

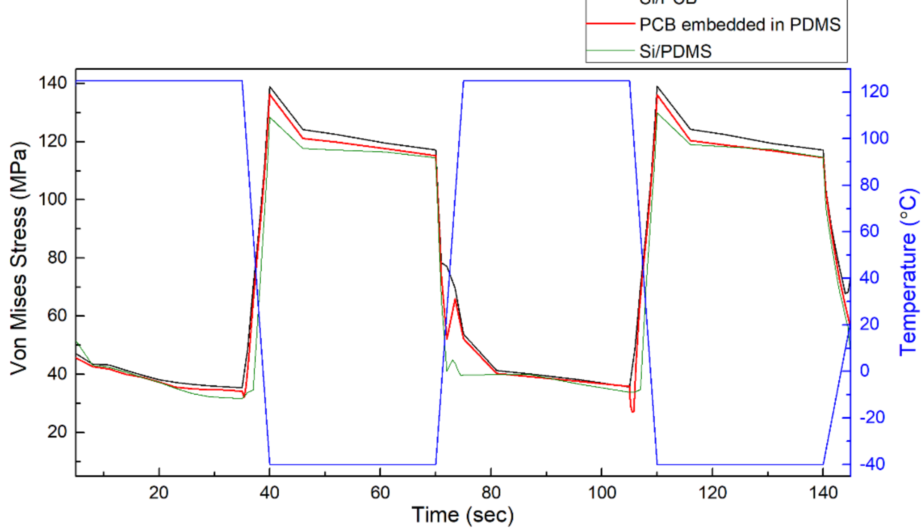


Figure 5.12 Von Mises stresses during temperature cycling simulation for Si wafer is attached to PDMS (green line), Si wafer directly attached to FR4 (grey line), PCB embedded in PDMS attached to Si wafer (red line). The dotted line is the temperature profile.

Moreover, to evaluate the effect of temperature cycling on the lifetime of the simulated structures, the plastic strain within the solder joints were extracted (Figure 5.13).

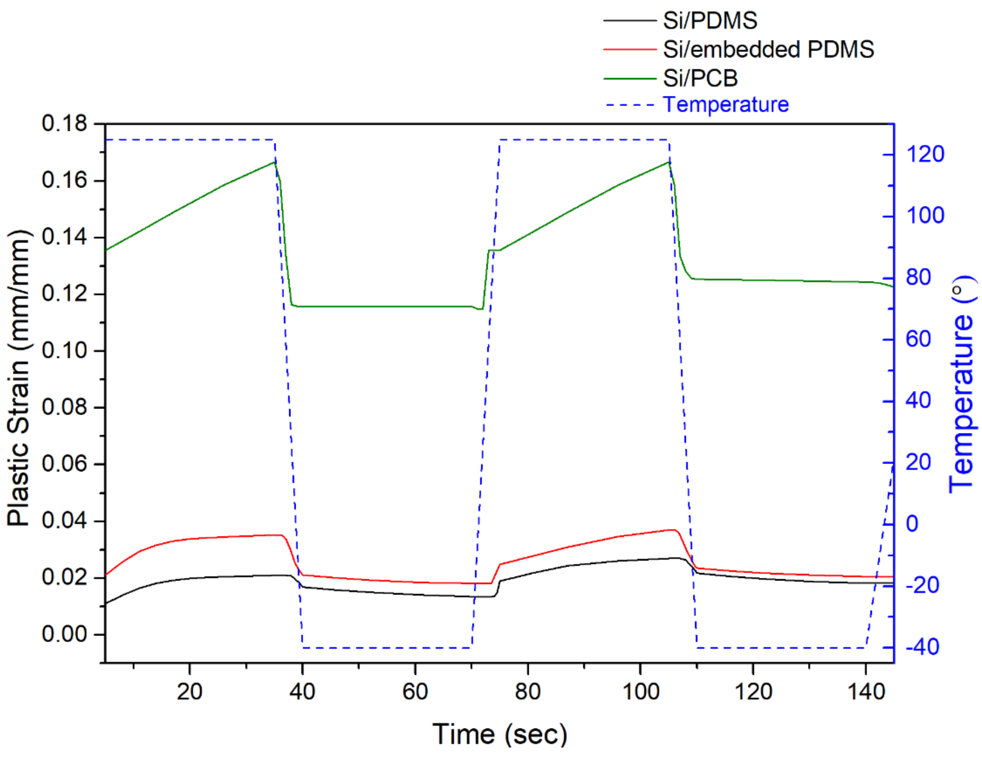


Figure 5.13 plastic strain within the solder joints for when Si-IF is directly bonded to PCB, Si-IF bonded to PDMS, and Si-IF bonded to segmented PCB embedded in PDMS. There strain levels in Si-IF/PCB are much higher than when PDMS is added as a buffer.

Figure 5.13 shows that the plastic strain levels in Si-IF/PCB structure are much higher than the other two structures, this shows addition of PDMS is effective in reducing the strain level in solder joints. Modified Coffin Manson lifetime prediction model known as Engelmaier was used to calculate the number of cycles to failure for each model [1]. Engelmaier model takes into account the effect of frequency (number of temperature cycling per day) and temperature range on the failure of the structure (Equation 5-8) [1].

$$N_f = \frac{1}{2}\left|\frac{\Delta\gamma_T}{2\varepsilon_f'}\right|^{\frac{1}{c}} \qquad \textit{Equation 5-8}$$

Where, N_f is the number of cycles to failure, $\Delta\gamma_T$ is the plastic strain range, ε_f' is fatigue ductility coefficient, and C is the fatigue ductility exponent. It should be noted that fatigue ductility coefficient and exponent are empirical values and are dependent on the solder alloy type, solder, and package shape. Table 5-5 is the summary of the values used in this modeling.

Table 5-5 material properties used in FEA simulation [88].

Material	ε_f'	C	f
SAC 405	0.939 [88]	-0.514595168 [88]	4

Using values in Table 5-5 and extracted plastic strain values, number of cycles to failure was calculated for all three simulated structures (Table 5-6).

Table 5-6 plastic strain range and N_f for all three structures.

Model	Plastic strain range (mm/mm)	N_f
Si/PCB	0.05177	537
Si/PDMS	0.01588	5334
Si/PCB embedded in PDMS	0.01882	3835

From Figure 5.13 and Table 5-6, it can be seen that addition of the PDMS, both in the form of a buffer layer and when PCB is segmented and embedded in the PDMS, reduces the plastic strain range in solder joints and consequently increases the number of cycles to failure in the assembly.

5.4 Summary

In this chapter the effect of temperature on the reliability of Si-IF and wafer scale system was discussed. The temperature variation that happens during operation of the assembly may result in accumulation of stresses in the interconnect due to CTE mismatch between materials in the system. However, due to limited number of materials in Si-IF system and tighter CTE range, the thermomechanical stresses in copper pillars are much smaller than the conventional BGA and C4 bumps. Moreover, because copper has a much higher melting temperature (1084 °C) compared to SAC solder alloys (≈ 220 °C), no fatigue or microstructural changes are expected in copper pillars during temperature cycling.

To verify these hypotheses, a passivated Si-IF assembly was subjected to temperature cycling in accordance with JESD22-A104 condition G (+125 °C/-40 °C) for 100 cycles and the change in electrical resistance of the daisy chains were measured every 10 cycles, maximum change in electrical resistance of the daisy chains was less than 8% which shows that Si-IF has a robust thermomechanical reliability.

However, due to complexity and size of the wafer scale system, high levels of thermomechanical stresses in solder joints connecting the PCB board to Si-IF may result in failure. Thus, there is a need for a stress buffer mechanism in the design of the wafer scale system. To evaluate the effectiveness of a buffer mechanism, FEA was used to simulate thermomechanical stress and strains in solder joints during two temperature cycles between +125 °C and -40 °C for three different models. In the firs model, Si-IF is directly bonded to PCB board, in the second model Si-IF is bonded to PDMS (a buffer layer) and in the third design, the Si-IF is bonded to

segmented PCB pieces embedded in PDMS. The result of the FEA analysis shows that addition of the PDMS reduces the stress and strain levels.

Moreover, lifetime prediction modeling of these three designs based on simulated plastic strain within the solder joints during temperature cycling shows that the number of cycles to failure for the wafer scale system increases from 538 cycles in the case of Si-IF/PCB to more than 3800 cycles in the cased of Si-IF/ PCB segmented and embedded in PDMS.

From above simulation results and lifetime prediction calculation, it is clear that addition of the PDMS is effective in reducing the stresses within the solder joints and improve the reliability of the overall system.

6. Vibration Analysis of Wafer Scale System

Failure due to vibration can occurs during shipment or operation. Excessive deformations and accelerations in PCB lead to damage to mounted components, solder joints and electrical interfaces, as well as the circuit board itself [89]. Some possible mechanical failures due to vibration are:

• Structural fatigue failure

• Solder joint fatigue failure

• Excessive deflection

There are two types of experimental tastings for evaluation failure modes due to vibration in electronic devices. These tests are:

1. **Sine vibration:** which can be a single frequency to selectively excite resonant structures within the device. Or Swept sine in which a vibration sine tone is ramped up and down through a range of frequencies and for a specified rate and duration.

2. **Random vibration:** Comprised of vibration energy at all frequencies over a specified range. The vibration frequency input signal for a random vibration appears on an oscilloscope as random noise.

Table 6-1 summarizes the objective of each of these tests and data that can be derived from them. Due to the fact that random vibration provides a more realistic representation of the stress and acceleration that the system may see, this type of testing is gaining more attention.

Table 6-1 objective of different vibration tests and data that can be collected from each.

Sine Vibration Testing	Random Vibration Testing
Identify the resonant condition of the structure	The most common type of validation and qualification test.
Understand how vibration fatigue propagates through the structure	Most vibration environments are characterized as having mainly random vibration conditions
Helps to stiffen or add damping to improve reliability	Used to study overall response of the system to vibration (not a specific amplitude or frequency)
Used to simulate worst case scenario at resonance	

In this chapter, the failure of the proposed wafer scale system due to random vibration is investigated. First, natural frequencies of Si-IF are extracted using modal analysis and verifying with FEA simulations. Subsequently, the response of the wafer scale system to input vibration was studied for three different scenarios to understand the effectiveness of PDMS in damping the input acceleration.

6.1 Failure Due to Vibration in the Proposed Wafer Scale System

The objective of this analysis is to understand the acceleration and the stresses that critical features see in the structure when subjected to vibration loads. These vibrations are due to the pumps that are integrated in the system for thermal management as well as other components that maybe present. Figure 6.1, is the schematic of the system, in this system following failures may happen due to vibration:

- Flextrate connectors
- Solder joints

- Flextrate buffer connection to Si-IF
- Dielets bonds to Si-IF

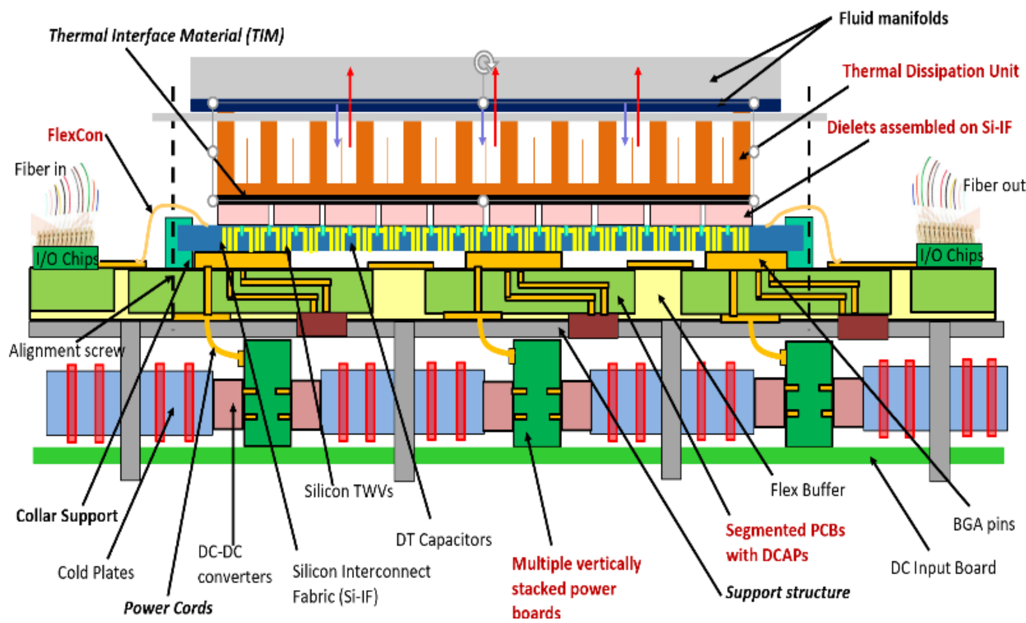


Figure 6.1 schematic cross section of the wafer scale system showing Si-IF, compliant power platform (bottom of Si-IF) and thermal management unit (top of Si-IF).

6.2 Modal Analysis of Si-IF

In order to identify the critical frequencies that may lead to delamination or fatigue failure, it is important to extract the natural frequencies of the model. Modal analysis identifies natural frequencies and mode shapes of the system. Natural frequency and mode shape are described as below:

1.**Natural frequency** (eigenfrequency): The frequency at which a system tends to oscillate in the absence of any driving or damping force.

2.**Mode shape** (eigenvector): is the deformed shape of the structure as it vibrates in the jth mode.

Modal analysis involves solving the equation of the motion for the system to extract eigenfrequency and eigenvector.

Equation 6-1 is the generalized equation of motion for an undamped system.

$$M\ddot{x} + Kx = 0 \qquad \textit{Equation 6-1}$$

Where: x is time dependent displacement, M is mass matrix and K is Stiffness matrix.

To verify the FEA model, modal analysis of a Si die connected to Si-IF was done mathematically using a mass-spring system with 2-degree of freedom (DOF). The mass-spring system is shown in Figure 6.2.

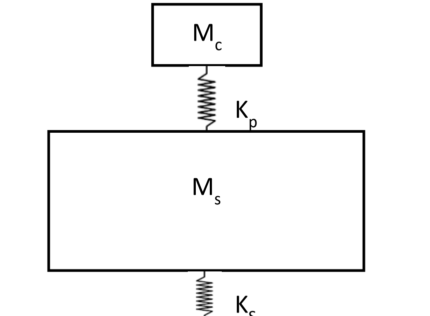


Figure 6.2 mass spring model of the Si-IF

Assuming a simply supported system, natural frequency was calculated for a 1 mm x 1 mm and a 10 mm x 10 mm dies. Table 6-2 summaries the properties of dies, substrate, and pillars. Equation 6-2 and 6-3 are the details of EOM for the model and solution.

Table 6-2 properties of the modeled dies, substrate and Cu pillars

Die size (mm^2)	1x1	10x10
Die mass (Kg)	1.22 $\times 10^{-6}$	122.273 $\times 10^{-6}$
Substrate mass (Kg)	0.0498	0.0498
K_p (N/m)	153 $\times 10^{4}$	153 $\times 10^{4}$
K_s (N/m)	18.859 $\times 10^{3}$	18.859 $\times 10^{3}$

$$\begin{bmatrix} -K_p & K_p \\ K_p & -(K_p + K_s) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} m_c & 0 \\ 0 & m_s \end{bmatrix} \begin{bmatrix} \ddot{x}_1 \\ \ddot{x}_2 \end{bmatrix}$$ *Equation 6-2*

- $x = Xsin(\omega t)$
- $\ddot{x} = -X\omega^2 \sin(\omega t)$

Substitute in (Equation 6-2) and rearranging:

$$\begin{bmatrix} -\omega^2 m_c + K_p & -K_p \\ -K_p & (K_p + K_s) - \omega^2 m_s \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} = 0$$

$$\begin{vmatrix} -\omega^2 m_c + K_p & -K_p \\ -K_p & (K_p + Ks) - \omega^2 m_s \end{vmatrix} = 0$$

$$\omega^4 m_s m_c - \omega^2 (K_p m_s + K_p m_c + K_s m_c) + K_p K_s = 0$$ *Equation 6-3*

Same model was simulated using ANSYS for modal analysis, Figure 6.3 is the simulated model, Table 6-3 summarizes the natural frequencies of the models. The difference between calculated and simulated values is 4.4%, suggesting a good agreement between the two.

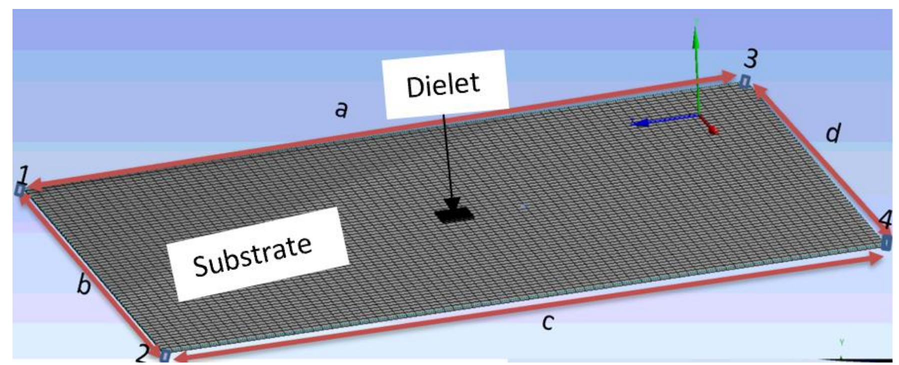


Figure 6.3 FEA model showing the dielet and substrate (boundary condition: $u_{a,b,c,d}(y)=0, u_{1,2}(x)=0$, $u_{3,4}(z)=0$

Table 6-3 calculated and simulated natural frequency of the model.

Die size (mm^2)	Calculated frequency (Hz)	FEA frequency (Hz)
1x1	97.98	102.38
10x10	97.83	102.33

From the modal analysis and FEA simulation, it can be seen that increasing the die size does not change the natural frequency in any significant way, the reason is that the mass of the die is negligible compared to the substrate mass and the natural frequency of the system is dependent on the substrate.

6.3 Damping in Vibration Analysis

PDMS as an elastomer is highly effective in vibration damping in automotive industry [90]. PDMS damping mechanism is hysteretic damping. During material deformation, internal friction causes high energy losses and energy is also stored through elastic deformation [91].

Transmissibility (T) is used as a measure to understand the damping characteristics of the structure. T is the ratio of the input energy (acceleration, displacement, et.) to the output and is defined [90]:

$$T = \left|\frac{A}{A_0}\right| = \sqrt{\frac{1+2\zeta\left(\frac{\omega}{\omega_0}\right)^2}{1-\left(\frac{\omega^2}{\omega_0^2}\right)^2+2\zeta\left(\frac{\omega^2}{\omega_0^2}\right)^2}}$$ *Equation 6-4*

Where: ζ is damping ratio, ω is excitation frequency, and ω_0 is natural frequency.

Equation 6-4 shows that higher damping ratio and lower natural frequency result in lower transmissibility.

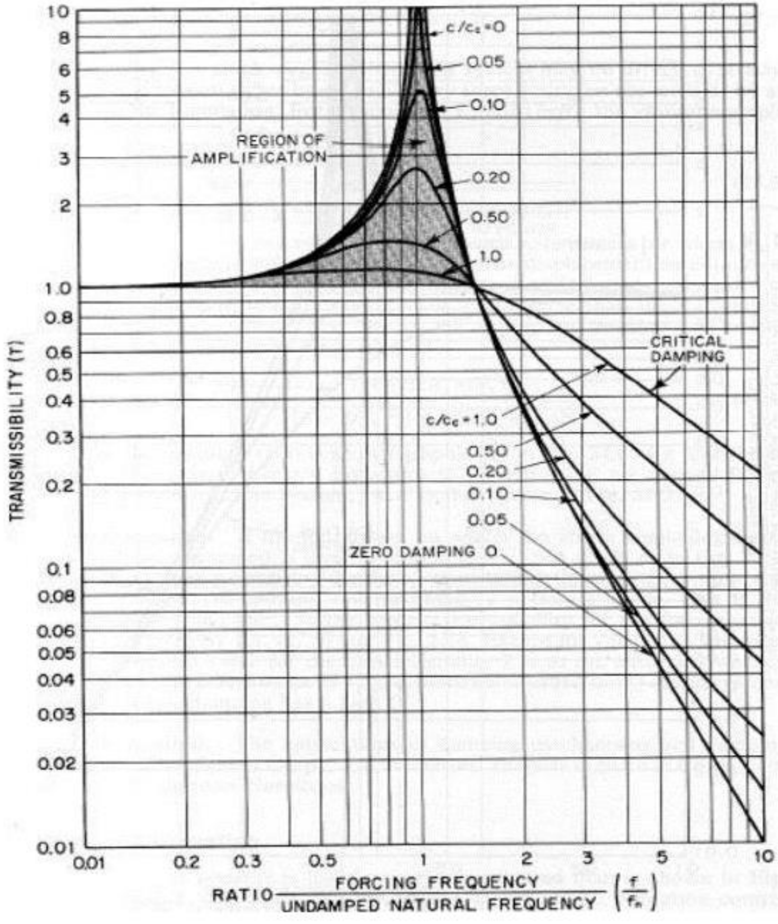


Figure 6.4 transmissibility VS. frequency ratio (f/f_0) for a damped single degree of freedom system [90]

Figure 6.4 is a typical transmissibility vs. frequency ratio curve for different damping ratios for a damped system [90]. Figure 6.4 shows that the transmissibility curve can be divided

into two different areas regardless of damping ratio: region of amplification and region of isolation. In frequency ratios close to natural frequency ($f/f_0=1$) the input force or displacement is amplified and T>1. However, when $f/f_0 \geq 1.4$ system enters the isolation region where T<1. To ensure an effective isolation and damping, it is crucial to select a damping material that possesses low natural frequencies to place the system in the isolation region in the frequency range of interest. PDMS provides extremely low natural frequency and high damping characteristics and thus is effective as a damping material.

6.4 Simulation Results of Random Vibration Analysis

As mentioned before, PDMS buffer layer is expected to considerably damp the input acceleration into the system. To investigate this effect, FEA analysis of a Si die attached to a substrate was performed. However, before performing random vibration simulation, the extract natural frequencies of the structure must be extracted as a prerequisite for the subsequent simulation. Natural frequencies of the structure with PDMS and FR4 as substrate are summarized in Table 6-4 and the simulated model is shown in Figure 6.5.

Table 6-4 shows that PDMS as a substrate has a much lower natural frequency. The frequency range of interest is usually 2-2000 Hz, since PDMS natural frequency is below this range, it is expected that the response of the system must be much lower compared to FR4.

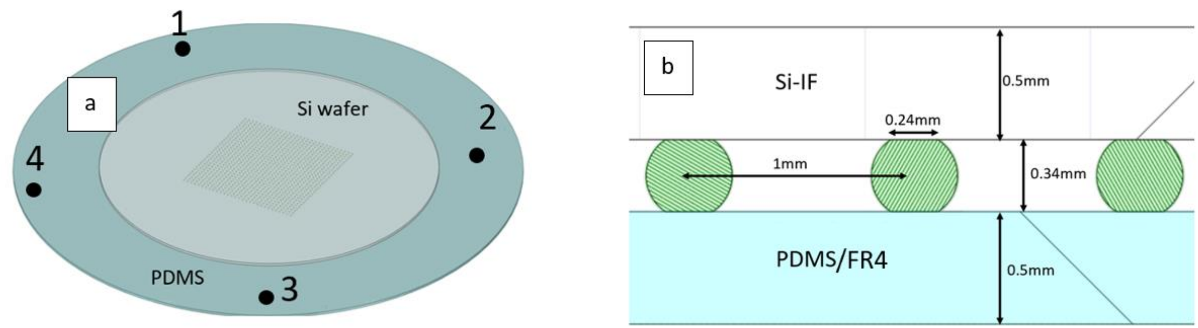


Figure 6.5 simulated model of the substrate, Si wafer and solder joints (a), cross section of the solder joints (b)

Table 6-4 natural frequency of the models for different number of solder joints and substrate material.

PDMS Substrate				FR4 Substrate
Mode #	100 Solder balls frequency [Hz]	400 Solder balls frequency [Hz]	900 Solder balls frequency [Hz]	900 Solder balls frequency [Hz]
1	12.808	2.8894	0.64277	90.449
2	17.858	4.226	1.0103	142.7
3	21.125	4.9873	1.0859	160.22
4	24.279	6.2307	1.4592	199.82
5	32.136	8.3547	1.8798	264.64
6	33.257	8.4022	1.9689	272.25

To validate this hypothesis, random vibration simulation was done on the 900 solder balls system for both FR4 and PDMS. Input G acceleration was taken from JESD 22-B103 [92]. Figure 6.6 illustrates the input and response of three systems, PDMS (high damping), FR4 (medium damping) and Si (low damping) models. Peaks in the responses correspond to natural frequency of each model.

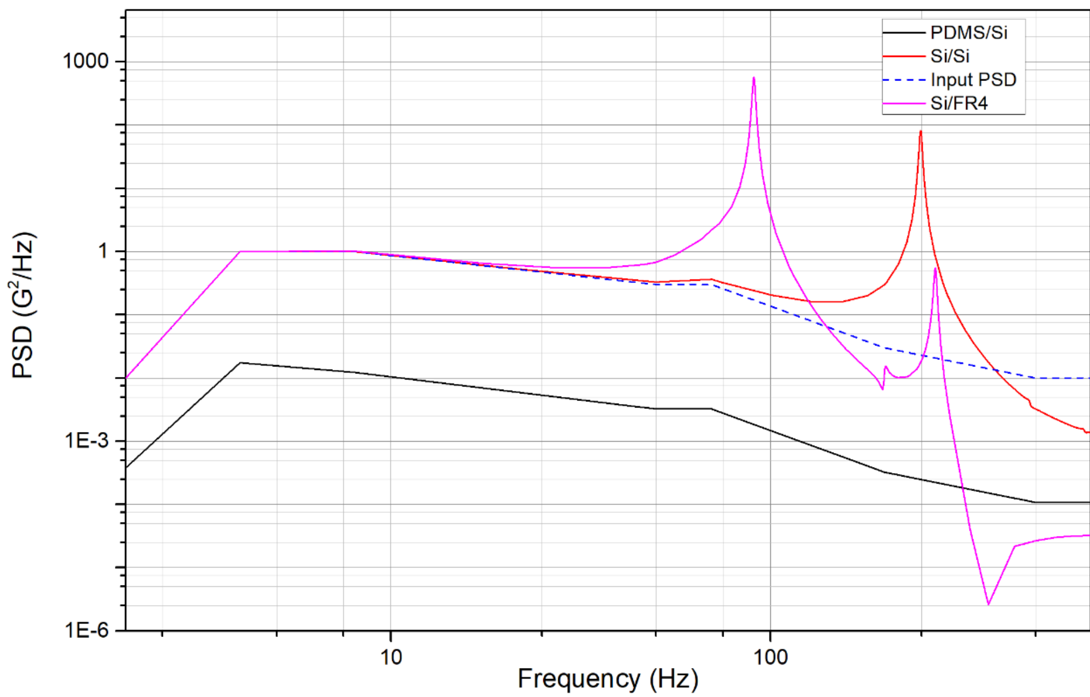


Figure 6.6 comparison of the FEA simulated response of a PDMS/Si, FR4/Si and Si/Si structure.

From Figure 6.6, it is observed that the response of the model with PDMS substrate is much lower than the other two models and in fact, PDMS as an elastomer is an effective damper to the mechanical shocks.

The reason for PDMS behavior is that 1. PDMS natural frequencies are extremely low and outside of the interested range of vibration analysis and 2. hysteresis damping properties of PDMS. Thus, PDMS is effective in damping the input acceleration.

6.5 Summary

In this chapter, the failure due to vibration in wafer scale system was discussed. Failure due to vibration is one of the most common failure modes in electronic devices. The sources of vibration include shipment, cooling pumps and other mechanical tools that are in the vicinity of the device.

In case of the wafer scale system, these vibrations may result in delamination of the flexible connectors, fatigue, and delamination of solder joints and etc.

To evaluate the effect of vibration on failure of the assembly, FEA analysis was used to model the natural frequency of the structure when Si-IF is bonded to PDMS and PCB. The natural frequencies of the assembly with PDMS are much smaller than Si/FR4.

Moreover, the response of the assembly to the input random vibration was measured for three different scenarios, Si-IF bonded to Si, Si-IF bonded to FR4 and Si-IF bonded to PDMS. From the output acceleration results and modal analysis of the assemblies, it is concluded that addition of PDMS is effective in damping the input vibration. The reason for the superior performance of the PDMS is due to its material properties and hysteresis damping characteristics of PDMS as an elastomer as well as its low natural frequency. These two factors result in high transmissibility (T) and thus, when PDMS is used in the system, the assembly is in the isolation region of the transmissibility curve (Figure 6.4).

7. Summary & Outlook

7.1 Summary

In this work, the reliability of a novel heterogeneous integration platform (Si-IF) was investigated. Si-IF platform utilizes direct metal-metal thermal compression bonding for integration of dielets into the assembly. The fabrication process is compatible with BEoL processes, and it allows for integration of dielets regardless of their size, material and technology nodes.

In this platform many of the reliability concerns associated with conventional electronic packaging related to solder alloys are eliminated. These include, formation of intermetallic compound, Kirkendall voiding and solder fatigue. Moreover, due to removal of underfill and overmold, the CTE range of the material in Si-IF is narrow resulting in lower thermal stresses in the interconnect (copper pillars) due to temperature variation. Overall, the chip package interaction is very limited in this platform.

However, there are some reliability challenges attributed to SI-IF that needed to be studied and mitigated. The first challenge is copper oxidation. Since copper is used as the interconnect, during TCB process, some misalignment may happen between the pillar on the Si-IF side and the pd on the die side that leaves copper exposed to the environment. In this dissertation, three different passivation techniques were presented.

First passivation that was studies is Parylene C, this semicrystalline polymer has many advantages including room temperature deposition process, conformality, having low defect density, and water vapor transmission rate. Moreover, it is widely used in MEMS applications. The initial studies of Parylene C with 1 and 3 μm thickness revealed that even though increasing

the thickness reduces the rate of copper oxidation, Parylene C by itself is not sufficient to protect copper from oxidation.

The next passivation that was investigated is a multilayer thin film of PECVD SiN_x and Parylene C. This structure demonstrates sufficient barrier properties to protect copper from oxidation and no copper oxide peaks were detected in passivated blanket copper samples after 168 hours of humidity testing (85%RH/85 °C). The limitation of this passivation is the lack of step coverage, since the exposed copper is under the bonded die and passivation is done after bonding, the deposition process must be conformal enough to allow for coating of the copper that is exposed at under the die.

The final passivation system that was studied is ALD Al_2O_3. This inorganic thin film has many advantages over Parylene C and multilayer passivation. It has a better thermal and chemical stability, and the CTE of Al_2O_3 is closer to other materials already in the platform. Moreover, the ALD process provides an exceptional step coverage. The initial investigation of the passivated blanket copper samples shows that Al_2O_3 with thickness of 10 nm and above is effective in protecting copper from oxidation. After modification of the ALD recipe to allow for longer time for precursor to penetrate through the gap between the die and Si-IF, bonded samples with daisy chain structures were passivated with 20 nm of Al_2O_3 and were subjected to humidity testing for 564 hours and the electrical resistance of the daisy chains were measured every 94 hours. Maximum change in the electrical resistance of the daisy chains were less than 3%, which shows Al_2O_3 is effective in protecting samples from degradation due to moisture ingress.

Another failure mode that was investigated was failure due temperature cycling. Bonded Si-IF sample with daisy chain structure was subjected to 100 cycles of temperature cycling (+125

°C/-40 °C) and the maximum change in electrical resistance of the sample was less than 8%. The experimental results confirms that Si-IF is a robust platform.

A wafer scale system is being developed based on utilizing Si-IF as the integration platform, the power delivery system is designed to be bonded to the bottom of the Si-IF while thermal management unit is design to be placed on top of the dies. Flexible connectors on the periphery are designed for communication between this system and outside.

Due to the large size of the wafer scale system and large CTE difference between Si and PCB, there can be a large thermomechanical stress in the solder joints that may result in failure. To mitigate these stresses, two different designs were considered. One design consists of using a PDMS buffer layer between Si and PCB board and the second design consists of PCB pieces embedded in PDMS. FEA analysis was used to investigate the evolution of thermomechanical stresses in solder joints during temperature cycling. The simulation results show that use of PDMS buffer layer reduces the stress levels significantly compared to when Si-IF is directly attached to PCB. The embedded PCB in PDMS further reduces the stresses.

Finally, the effect of PDMS buffer layer in damping the input vibration into the wafer scale system was investigated. FEA analysis shows that PDMS substrate has a much lower natural frequencies compared to PCB. Moreover, the random vibration analysis of the system shows that PDMS reduces the input acceleration into the system and effectively damp the input vibration.

7.2 Outlook

1- The effectiveness of Al_2O_3 as a passivation has been shown in this dissertation. Al_2O_3 has a lot of favorable material properties including low CTE, low water vapor transmission rate and chemical and thermal stability. However, Al_2O_3 has a low thermal conductivity (30 $Wm^{-1}K^{-1}$ [93]), Even though the passivation thickness is relatively small, this low thermal conductivity may result in lower thermal extraction efficiency through the thermal management unit in the wafer scale system. Thus, it is important to develop a passivation with a higher thermal conductivity that can be deposited using ALD process. Recently, much effort has been put into to developing ALD AlN, AlN all the advantages of Al_2O_3 with the addition advantage of high thermal conductivity (up to 321 for single crystal $Wm^{-1}K^{-1}$ [94]). Thus, it is beneficial to investigate use of AlN as passivation for Si-IF.

2- Thermomechanical analysis of the wafer scale system: in this work, it has been shown that addition of the PDMS buffer layer and segmenting the PCB board reduce the stresses in the solder joints during temperature cycling. Experimental verification is needed to ensure reliability of the wafer scale system when subjected to temperature cycling.

3- It has been shown through FEA simulation that addition of the PDMS is effective in reducing the natural frequency of the system to levels that are below the frequency range of interest. However, natural frequency is very sample dependent, and it is important to perform random vibration testing on the assembly after fabrication to understand potential failure modes and extract lifetime.

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