Title

Optimized Thyristor Random Access Memory (TRAM) for High-Speed Computing

Author

Kwon, Ikhyeon

Publication Date

2024

Peer reviewed|Thesis/dissertation

Optimized Thyristor Random Access Memory (TRAM) for High-Speed Computing

By

IKHYEON KWON
THESIS

Submitted in partial satisfaction of the requirements for the degree of

MASTER OF SCIENCE

in

ELECTRICAL & COMPUTER ENGINEERING

in the

OFFICE OF GRADUATE STUDIES

of the

UNIVERSITY OF CALIFORNIA

DAVIS

Approved:

S. J. Ben Yoo, Chair

Venkatesh Akella

Rajeevan Amirtharajah

Committee in Charge

2024

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to Distinguished Professor S. J. Ben Yoo for his constant support and inspiration. Thanks to his guidance, I have been able to conduct interesting research related to this next-generation memory, and his passion and hard work inspired me a lot.

I would also like to extend my gratitude to Professor Venkatesh Akella and Professor Rajeevan Amirtharajah as a member of my thesis committee members, for providing guidance.

Thanks should also go to everyone in the Next Generation Networking and Computing Systems (NGNCS) group. They are great friends to me both as research colleagues and friends. I also wish to thank my Korean friends, brothers, and sisters.

I am grateful to Hyeonsu Kim who has waited for, supported, and encouraged me during my master's degree.

Finally, I would like to express my deepest appreciation to my family and my parents for their love and support. Many thanks to my brother, Hyosang Kwon who has supported my parents and encouraged me.

ABSTRACT

Various types of memory devices have been investigated for the development of next-generation memory technology with high operating speed, high reliability, and low leakage currents. Thyristor Random Access Memory (TRAM) can be one of the most promising candidates. In this work, we demonstrate the memory operation characteristics of TRAM with measurement and simulation results. The results have shown non-volatile characteristics while holding voltage applied. The holding voltage is required voltage condition to keep charges stored in memory. TRAM also has shown high speed switching operation with device PNPN structure. However, the conventional TRAM with two terminal designs has some disadvantages such as short retention time and large leakage currents. Additionally, the PNPN device structure has shown difficulties in controlling the current flows. Therefore, we propose a Three-Terminal TRAM (3T-TRAM) design and compare the device performance with the conventional Two-Terminal TRAM (2T-TRAM).

The proposed 3T-TRAM has an additional gate contact to control the currents flow, which makes low leakage currents and high retention characteristics. The optimized design with different doping conditions has been investigated. With the optimized design, we can expect that 3T-TRAM can replace current dynamic random-access memory (DRAM) with excellent performance and be applied as a next-generation high speed computing memory.

CONTENTS

LIST OF FIGURES AND TABLES

INTRODUCTION

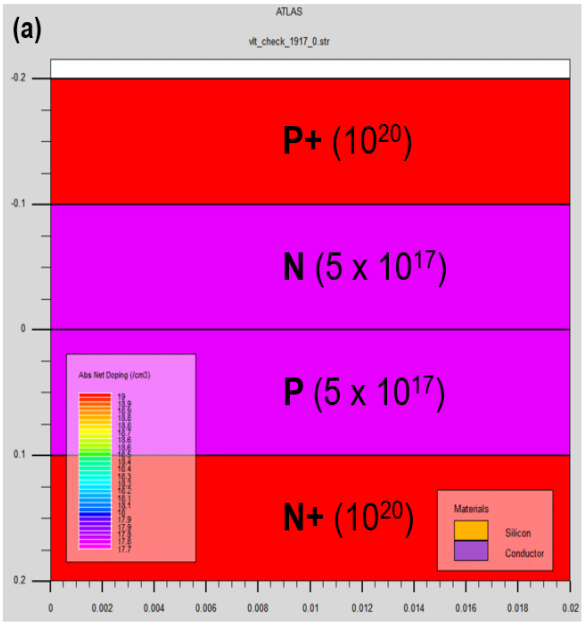
High-performance computing (HPC) is necessary for the innovation and development of modern industry. This plays an essential role in complex problem-solving and data analysis, and large-scale computing in various fields. In the fields such as an artificial intelligence (AI), a big data analysis, and a real-world simulation, the HPC has been attracting researchers' attractions. Also, the amount and variety of data is growing explosively in modern cyberinfrastructures. Examples of the growing large-scale data include sensor data from the Internet of Things (IoT), large-scale user data from active use of social media, and real-time data from advances in industrial automation and robotics. As a result, the requirements for data processing and analysis have gradually increased. In these fields, existing memory systems have difficulty meeting these requirements. Volatile memories such as static random-access memory (SRAM) and dynamic random-access memory (DRAM) provide high performance, but there are still limitations such as cell density, stability, power consumption, and lifespan [1]. In addition to volatile memories, non-volatile flash memory can have small cell sizes. However, it has very slow access times and program/erase times [2].

These technological limitations have led to the growth of ultrafast memory devices with remarkable features such as high speed, large bandwidth, low latency, and low energy consumption [3]. Thyristor Random Access Memory (TRAM) has emerged as a promising ultrafast memory to achieve these requirements. The two-terminal simple structure of the proposed TRAM shows the potentials for low-cost fabrication, high switching speed, low power consumption, and non-volatile characteristics [4]. However, this structure suffers from the significant challenge of crosstalk or memory disturbance between adjacent cells in dense arrays [5].

In this work, we investigated and compared the memory characteristics between two terminal TRAMs and three terminal TRAMs. Sentaurus TCAD and Silvaco TCAD are used to investigate the device characteristics. Additionally, we fabricated three terminal TRAMs, and the results demonstrate that the gate plays an important role in memory characteristics

Chapter 1. Two-Terminal TRAM (2T-TRAM)

i. The Device Structure of Two-Terminal TRAM (2T-TRAM)



(b) Device parameters

Doping concentration (cm^{-3})	10^{20}/5 x 10^{17}/5 x 10^{17}/10^{20}
Width (nm)	20
Length (nm)	100/100/100/100

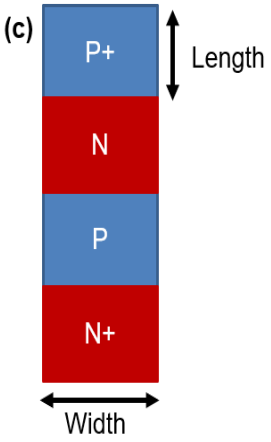


Figure 1. (a) Silvaco 2T-TRAM device structure (b) Device structure parameters (c) Schematic diagram of the optimized 2T-TRAM.

Figure 1 shows the proposed device structure and device parameters of 2T-TRAM. This design has p+/n/p/n+ areas, with doping levels at 10^{20}/ 5 x 10^{17}/ 5 x 10^{17}/ 10^{20} cm^{-3}. The doping concentrations of side p+ and n+ areas should be higher than n/p base areas. The n/p base areas are used for the stable storage of charges. Anode contact is located on the p+ region and the cathode is located at the bottom of the n+ region. For the device size, 20 nm width and 100 nm length are used. 2T-TRAM is designed using Silvaco technology computer-aided design (TCAD). Silvaco TCAD is a simulator to investigate the operation characteristics of electronic devices.

ii. Operation Principle

Unlike traditional electronic devices, the TRAM has unique I-V characteristics. Until a breakdown occurs, ‘off’ current is maintained. This is because TRAM has high energy barriers created by high doping concentration between the anode and the cathode. Due to the high energy barriers, carriers are confined or stored in the n/p base areas and there is no carrier flow in the TRAM device. However, the confined carriers can be excited thermally, which leads to leakage currents. Therefore, the high energy barrier should be generated to prevent leakage currents. The high energy barrier can be observed in Figure 2 (a), and this state is called an ‘off’-state. Figure 3 shows the I-V characteristics of the designed 2T-TRAM device. The forward bias is applied to the p-type anode area. Before a breakdown condition occurs, very low currents are observed. This state is called a forward blocking state.

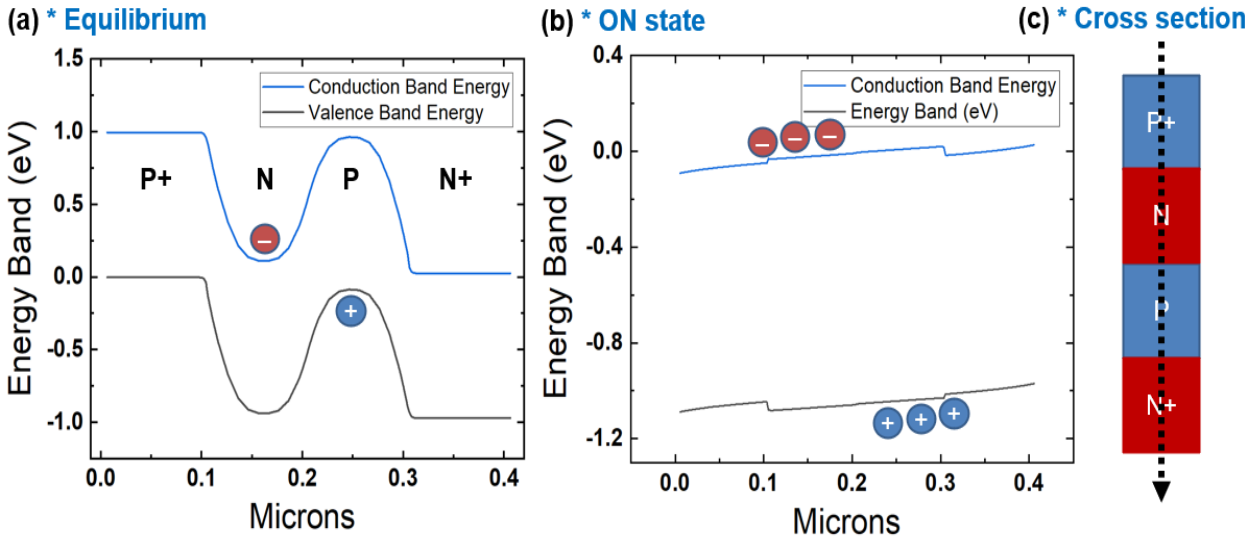


Figure 2. (a) Energy band diagram in the equilibrium state, (b) energy band diagram in the ON state, and (c) the cross section from p+ doped area to n+ doped area.

As the forward bias increases, the breakdown is generated, and the breakdown leads to weakened energy barrier height. The state in which the resistance decreases with weakened energy

barrier is called the ‘transition state’, and the highest current in the transition state is called holding currents (Figure 3). The holding current is an important concept in TRAM for memory operation. The voltage at which the holding current is observed should be applied if we want to maintain the programmed state. This means that the TRAM can have excellent retention characteristics while holding voltage is applied in the device. In other words, the TRAM has non-volatile characteristics. If the TRAM is designed to have a low holding voltage, it can have low energy consumption. However, if the holding voltage is too low, TRAM can be sensitive to memory disturbance in memory array. Therefore, it is important to find an optimized holding voltage.

From the end of transition state, the device current rapidly increases again and device changes to the ON-state (Figure 3). Due to the lower energy barrier between anode and cathode in Figure 2 (b), the confined carriers in Figure 2 (a) can flow easily with lowered resistance. The lowest current in the ON-state is called the latching current. Based on results, we demonstrated that TRAM can have two different states for memory operation using energy band diagram and IV characteristics of 2T-TRAM device. Optimized 2T-TRAM design and device challenges are discussed in chapter 1, section iii of this dissertation.

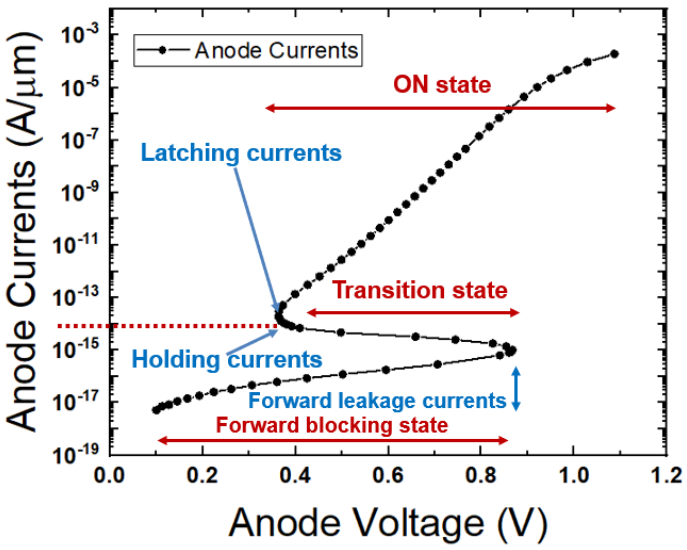
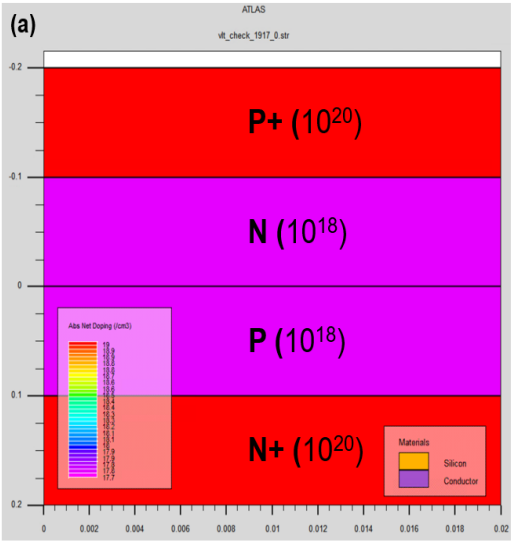


Figure 3. I-V characteristics of the designed 2T-TRAM device. The forward bias is applied to the P-type Anode area.

iii. Device Results

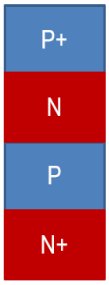
In a 2T-TRAM, the device structure strongly influences both I-V characteristics and memory operation. Since memory does not operate as a single device cell but as multiple devices in an array, it is important to find optimal device conditions. For example, it is desirable to have low power consumption in a single cell, but low power consumption can result in high sensitivity to noise and disturbance in a memory array.

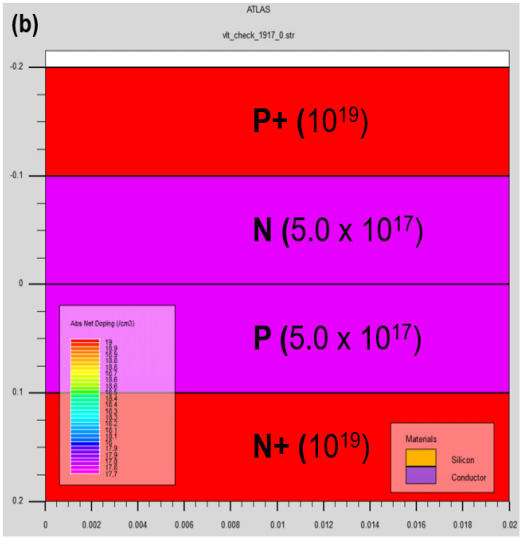
Therefore, we investigated device characteristics of 2T-TRAMs with different doping concentrations and lengths of storage areas. Figure 4 represents the device structure and different structure parameters. In Figure 4 (a), p+/n/p/n+, 10^{20}/ 10^{18}/ 10^{18}/ 10^{20} cm^{-3} structure is investigated with different lengths 100/100/100/100, 100/120/120/100, 100/150/150/100, 100/200/200/100. Also, p+/n/p/n+ (10^{20}/ 5 x 10^{17}/ 5 x 10^{17}/ 10^{20} cm^{-3}) doping concentration with same device size conditions is investigated in Figure 4 (b). Only the structure conditions of storage regions are changed in this work because the carrier flow of device is determined by storage carriers.



Device parameters

Doping concentration (cm^{-3})	$10^{20}/10^{18}/10^{18}/10^{20}$
Width (nm)	20
Lengths (nm)	100/100/100/100 100/120/120/100 100/150/150/100 100/200/200/100





Device parameters

Doping concentration (cm^{-3})	10^{19}/5.0 x 10^{17}/5.0 x 10^{17}/10^{19}
Width (nm)	20
Lengths (nm)	100/100/100/100 100/120/120/100 100/150/150/100 100/200/200/100

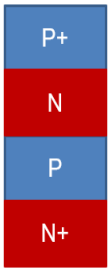


Figure 4. Device schematic diagram with different structure parameters.

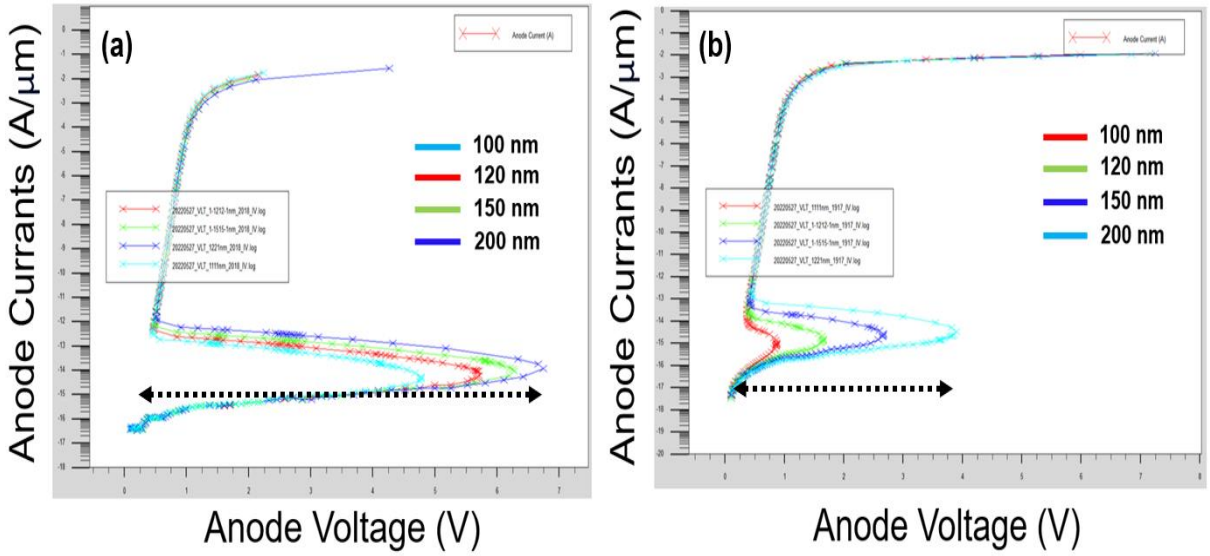


Figure 5. I-V characteristics of the designed 2T-TRAM device. (a) PNPN, doping concentration 10^{20}/ 10^{18}/ 10^{18}/ 10^{20} cm^{-3}, (b) 10^{20}/ 5 x 10^{17}/ 5 x 10^{17}/ 10^{20} cm^{-3} with different lengths of storage regions, 100, 120, 150, and 200 nm.

Figure 5 shows the IV characteristics of the Figure 4 devices. Figure 5(a) 2T-TRAM device has higher doping concentrations of storage regions than Figure 5(b). The high doping concentration of storage regions creates higher barrier height between anode and cathode. Therefore, it is more difficult to generate currents of the confined carriers in storage regions, and Figure 5(a) device condition requires a larger anode voltage to change the state of the device, 0 to

1 for memory operation. This means that devices of Figure 5 (a) require a higher power consumption than those of Figure 5 (b).

Next, we studied the effects of different device lengths. As the length of storage regions increases, the number of confined carriers required to lower the barrier height increases. Additionally, as the device lengths increase, the holding currents required for non-volatile properties increase. This causes higher leakage currents in programmed devices and requires a larger memory size. Based on the results, we proposed the device structure conditions with pnpn 10^{20}/ 5 x 10^{17}/ 5 x 10^{17}/ 10^{20} cm^{-3} doping concentrations and 100/100/100/100 nm device lengths for optimized 2T-TRAM device operation. The I-V characteristic of optimized 2T-TRAM device is shown in Figure 6. It has 0.4 V, holding voltage.

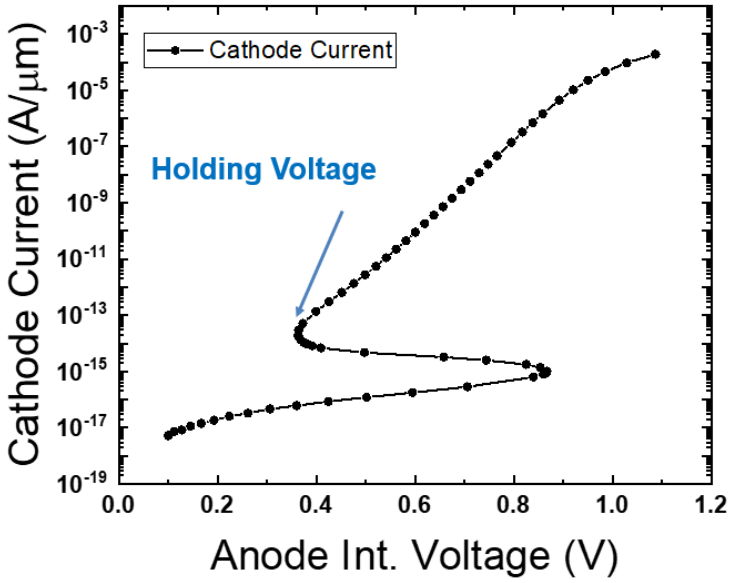


Figure 6. I-V characteristics of the optimized 2T-TRAM device with holding voltage. PNPN, doping concentration 10^{20}/ 5 x 10^{17}/ 5 x 10^{17}/ 10^{20} cm^{-3} and 100/100/100/100 nm.

iv. Memory characteristics

From the previous study, we proposed an optimized device structure that requires a lower power consumption and an excellent memory disturbance characteristic. Another important parameter related to the reliability of memory operation is a retention characteristic. Retention characteristics represent the ability of a memory component to maintain stored data or carriers without significant degradation or loss. In other words, it refers to the period during which data is maintained without being lost even if the power is disconnected or turned off. DRAM, which is currently widely used in the high-speed computing field, has volatile characteristics in which data is lost when power is turned off. On the other hand, 2T-TRAM shows non-volatile characteristics without data degradation. Data stability and continuity are necessary for high-speed computing. In this section, we will determine the program conditions of the proposed 2T-TRAM device in previous work and will investigate its retention characteristics.

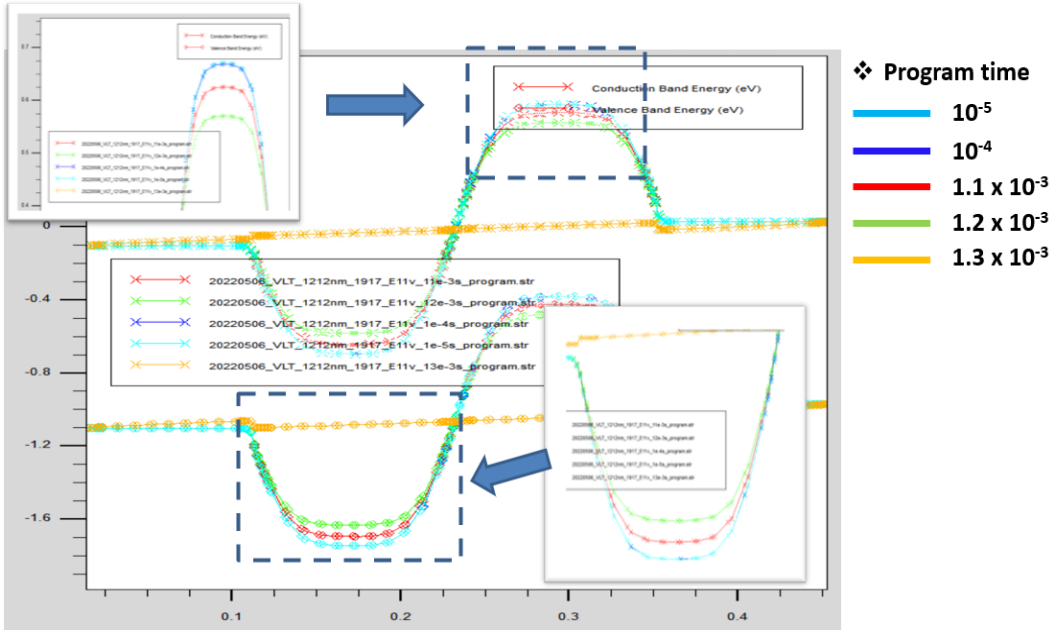


Figure 7. Energy band diagram of proposed 2T-TRAM with different program voltage conditions (Program voltage: anode 1.1 V, Program time: 10^{-5}, 10^{-4}, 1.1 x 10^{-3}, 1.2 x 10^{-3}, 1.3 x 10^{-3} s.

The energy band diagrams of programmed 2T-TRAM devices are extracted by TCAD simulation. Forward bias 1.1 V is applied into an anode contact to write or store data in memory device. We have investigated the programmed data amount with different program time. If the program time is long, the number of carriers stored in the storage region (n/p) increases, so the energy band in the n area and p area increases and decreases, respectively. The dotted square box in Figure 7 shows the energy band change depending on program time 10^{-5}, 10^{-4}, 1.1 x 10^{-3}, 1.1 x 10^{-3}, 1.2 x 10^{-3}, and 1.3 x 10^{-3} s. Based on results Figure 7, we decided the device program condition with 1.1 anode voltage and 10^{-5} s. At 10^{-5} s, the device has the largest number of stored carriers.

After a program or write operation, retention characteristics are investigated at 300 K (Figure 8). In Figure 8, the standby voltages represent applied anode voltage to maintain programmed states.

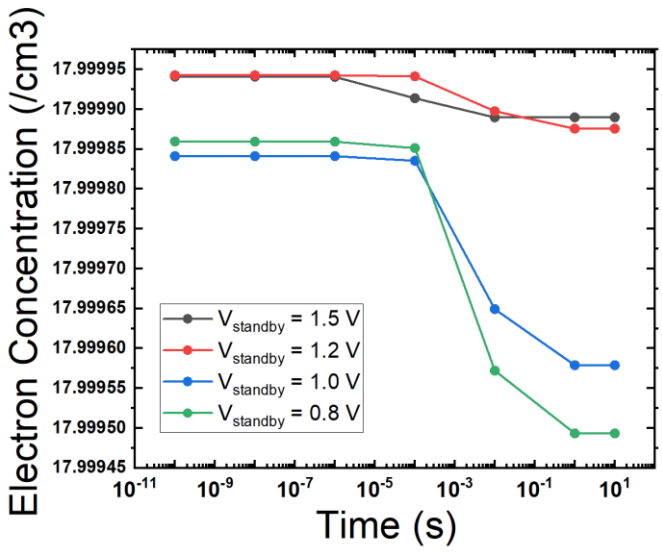


Figure 8. Retention characteristics of proposed 2T-TRAM design. The y-axis represents the electron doping concentration, and the x-axis represents time (s).

Forward voltage, 1.1 V is applied to the anode, and the investigated program times were 10^{-5}, 10^{-4}, 1.1 x 10^{-3}, 1.2 x 10^{-3}, 1.3 x 10^{-3} s, respectively. The Y-axis represents the stored electron concentration, showing that there is almost no loss or degradation of stored carriers while the

holding voltage is applied. In this work, we have demonstrated that most stored carriers (10^{17} cm^{-3}) can be maintained for 10 s.

The barrier height that has the direct influence on the loss of stored carriers was investigated. The holding voltage (0.4 V) of the optimized 2T-TRAM structure was determined in the previous study, Figure 6. If a larger voltage than holding voltage 0.4 V is applied, the barrier height between anode and cathode is rapidly damaged or weakened (Figure 9). This is because the higher standby voltage makes current flows of stored carriers. Therefore, the stored carriers can escape easily due to the lowered barrier.

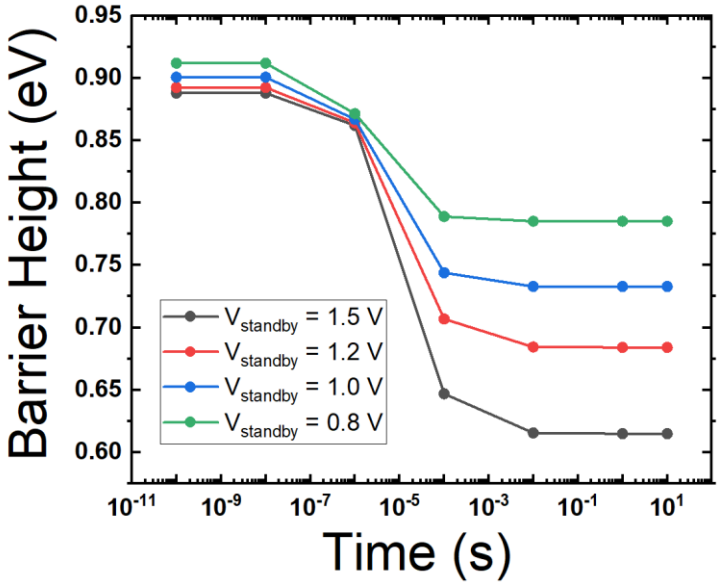


Figure 9. Barrier height of programmed 2T-TRAM device. 0.8, 1.0, 1.2, and 1.5 V are applied for 10 seconds.

2T-TRAM is one of the promising candidates for next-generation memory devices because it has a simple structure and non-volatile characteristics. However, there are some challenges to control the energy bands and carriers with only two terminals. High power consumption with high anode voltage is required for programmed state or retention characteristics. Additionally, in an array structure, pnpn junction areas are directly exposed to other memory cells, which can be vulnerable to memory disturbance. The vertical structure of the proposed 2T-TRAM has excellent

potential in terms of scaling down the memory footprint. However, in a manufacturing perspective, the vertical structure has critical challenges when the implantation process for highly doped areas is performed. To overcome these limitations, we have proposed a 3 terminal-TRAM (3T-TRAM) with an additional gate contact in the following work.

Chapter 2. Three-Terminal TRAM (3T-TRAM)

i. The Device Structure of Three-Terminal TRAM (3T-TRAM)

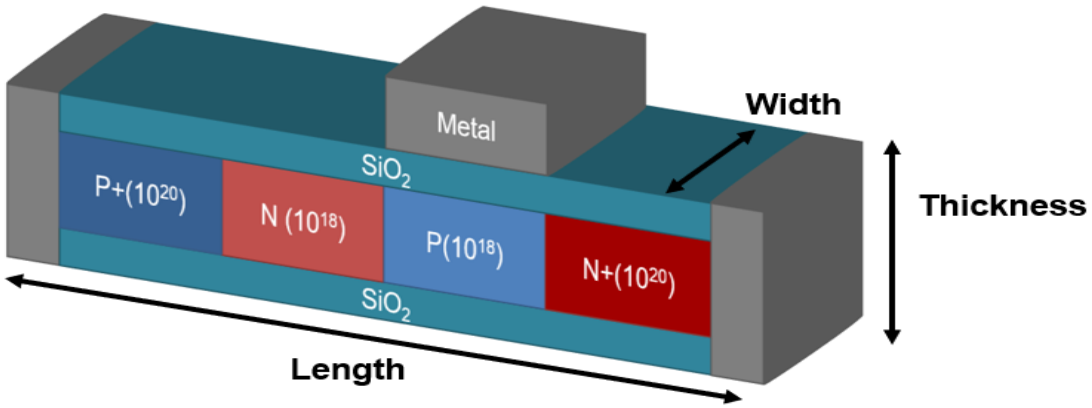
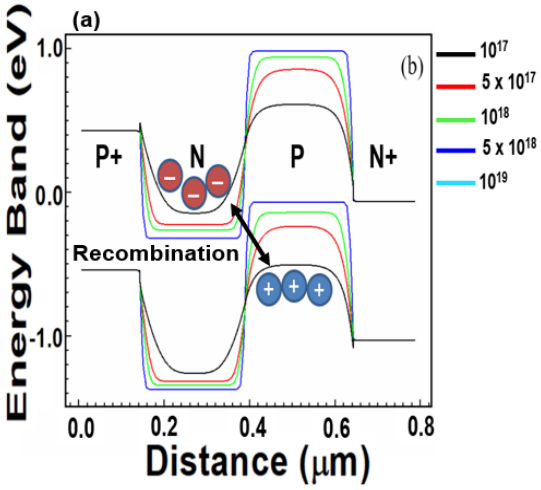


Figure 10. Schematic diagram of 3T-TRAM device structure.

Figure 10 shows the schematic diagram of the optimized 3T-TRAM structure in this work. The optimized structure parameters and operation characteristics are demonstrated by Sentaurus Technology Computer-Aided Design (TCAD) simulator. The 3T-TRAM has been investigated with different storage region lengths, 150, 200, 250 nm and different doping conditions 1 x 10^{17}, 5 x 10^{17}, 1 x 10^{18}, 5 x 10^{18}, and 1 x 10^{19}. In the device, high-doping concentration is used for the stable storage of carriers. Also, the high-doping concentration helps to induce breakdown. The middle area uses a lower doping concentration than the doping concentration of both side regions. Boron dopants are used for P-type doping and Arsenic dopants are used for N-type doping. Figure 11 (b) presents the device parameters, doping concentration, lengths, widths, and thicknesses. Based on these device parameters, Figure 11 (a) displays the different energy band diagrams. The high barrier between p+ and n+ regions formed by high doping concentration prevents the excitation of stored carriers, but it causes recombination of holes and electrons stored in n/p base regions.

Figure 10 shows an additional contact called a gate contact is added on the p-type base region. The gate contact plays an important role in controlling dynamic memory characteristics and non-volatile memory characteristics. The voltage applied to the gate directly affects the p-type area. To enhance the gate control, a SiO_2 gate oxide is used, and the thickness is 5 nm. Also, the silicon thickness of this device is 20 nm. Unlike the previous 2T-TRAM device, which had a vertical structure, this 3T-TRAM device has a horizontal structure because it was manufactured according to the design rule of GlobalFoundries, a manufacturing and design company. However, our ultimate goal is to have a vertical structure, as the vertical structure grown by epitaxial growth achieves excellent carrier control.



(b)	Doping Concentration (cm^{-3})	L / W / T (nm)
	$10^{20}/10^{17}/10^{17}/10^{20}$	150/170/20 200/170/20 250/170/20
	$10^{20}/5 \times 10^{17}/5 \times 10^{17}/10^{20}$	150/170/20 200/170/20 250/170/20
	$10^{20}/10^{18}/10^{18}/10^{20}$	150/170/20 200/170/20 250/170/20
	$10^{20}/5 \times 10^{18}/5 \times 10^{18}/10^{20}$	150/170/20 200/170/20 250/170/20
	$10^{20}/10^{19}/10^{19}/10^{20}$	150/170/20 200/170/20 250/170/20

Figure 11. (a) Energy band diagram of 3T-TRAM devices with different doping concentrations, (b) This table represents 3T-TRAM structure parameters.

ii. Operation Principle

The operation mechanism of 3T-TRAM devices is very similar to that of 2T-TRAM devices. The anode voltage controls the carriers flow using the barrier height formed between anode and cathode regions, but the added gate contact also influences the energy barrier height. Gate contact has a direct effect on the energy barrier under the gate contact region. Therefore, 3T-TRAM can

have higher doping concentration for storage regions than 2T-TRAM because it can easily control the energy band. As the doping concentration of the storage area increases, the retention characteristics of the memory also improve. Additionally, the strong gate control prevents 3T-TRAM devices from memory disturbance of adjacent cells.

iii. Device Results

Through Figure 11 (a), we demonstrated that 3T-TRAM also has a higher barrier height when it has the storage regions with higher doping concentration. However, if the doping concentration becomes too high, the spacing between stored carriers in n/p storage regions also becomes too close. There are two carrier loss mechanisms in n/p storage regions of TRAM. One of the loss mechanisms is caused by the surrounding temperature, and the other is caused by recombination that occurs between confined carriers in the n/p storage regions (Figure 11 (a)). Therefore, in the proposed 3T-TRAM device, the doping concentration in the storage region is determined to be 10^{18} cm^{-3}, considering the recombination loss mechanism of the stored carriers.

Next, we investigated the I-V characteristics with different device lengths. In this work, the difference between the required anode voltage to change the state of the device from 0 to 1 and the holding voltage is defined as the memory window. In memory array, the larger the memory window, the higher the required anode voltage for state change. This means that a large memory window device can have excellent performance against memory disturbance, but it requires a high-power consumption (Figure 12). Therefore, we determined the device length of our 3T-TRAM to be pnpn 200/150/150/200 nm in Figure 12. This device has the lowest holding currents and voltage, 2×10^{-12} A/μm and 0.55 V in Figure 12.

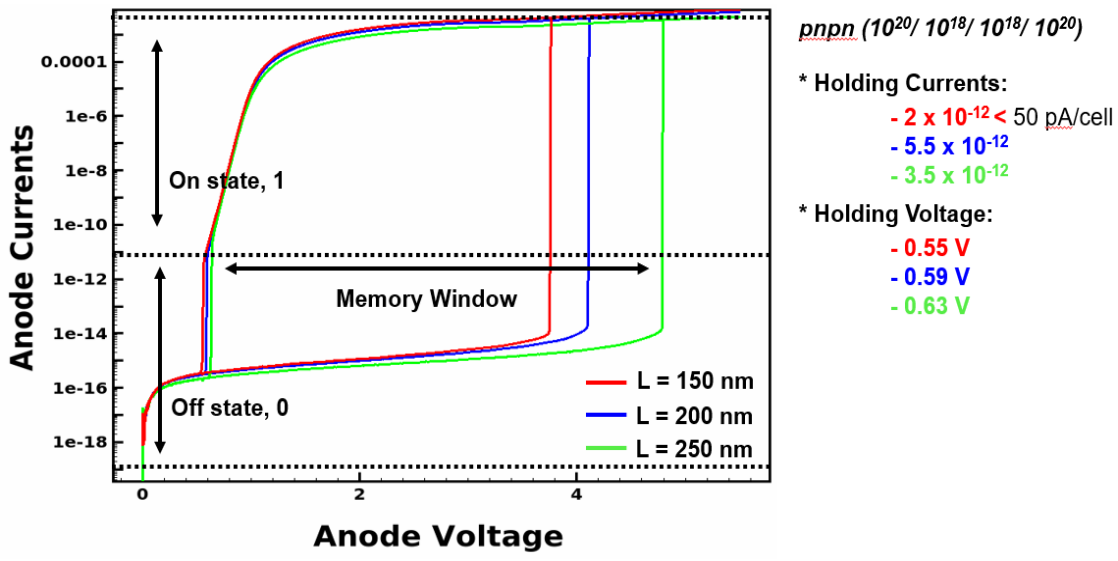


Figure 12. I-V characteristics of the designed 3T-TRAM device with different lengths, L = 150, 200, 250 nm and $10^{20}/10^{18}/10^{18}/10^{20}$ cm^{-3}, pnpn regions.

After determining the device parameters (pnpn $10^{20}/10^{18}/10^{18}/10^{20}$ cm^{-3} doping concentrations and 200/150/150/200 nm lengths), we studied the influence of the additional gate contact in the proposed 3T-TRAM device. Figure 13 shows the I-V characteristics of this proposed device with different gate voltage. Since the gate voltage is applied directly to the p-type region (Figure 10), the energy barrier between the anode and the cathode can be easily controlled by the gate voltage (Figure 10 and 11).

As shown in the results in Figure 13, the gate voltage has a very strong control over the device carriers. Compared to Figure 12, Figure 13 requires a much lower anode voltage to change the device state from 0 to 1. In the same device length condition, L = 150 nm, the required voltage to change to the ON state has decreased from approximately 5 V to 0.85 V. Based on these results, we demonstrate that the voltage conditions of the 3T-TRAM device can be changed easily depending on the required memory operation conditions.

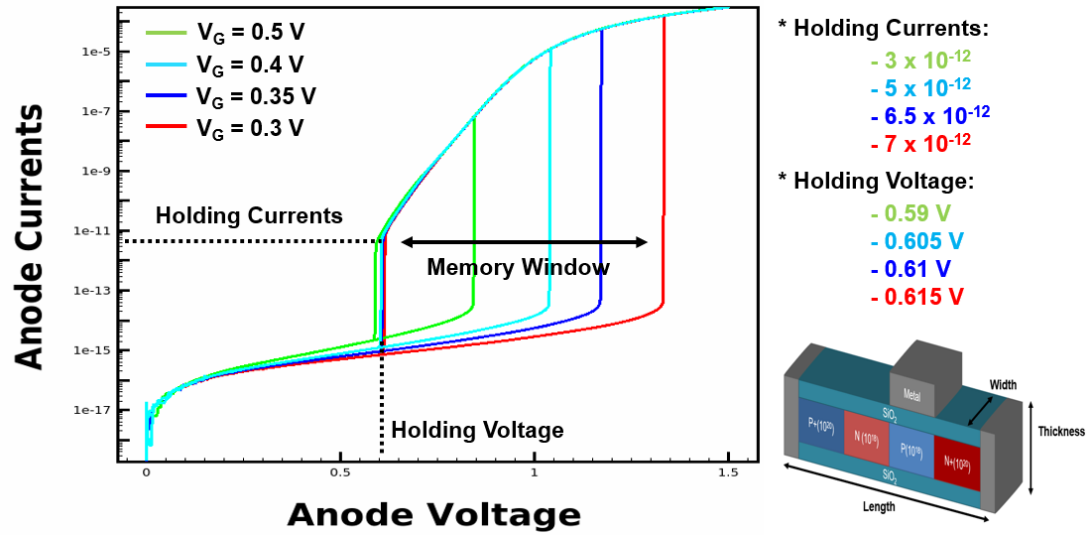


Figure 13. The I-V characteristics of a proposed 3T-TRAM device with different gate voltages from 0.3 V to 0.5 V.

iv. Fabrication Design and Measurement

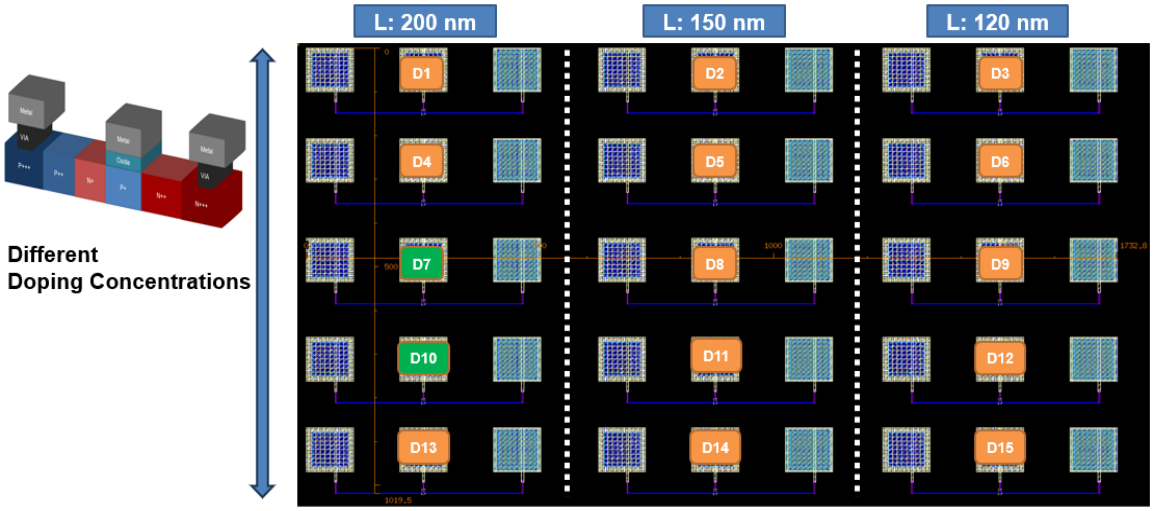


Figure 14. The schematic diagram and device layout of fabricated 3T-TRAM devices by GF. There are 15 different devices, and they have different doping concentrations and device dimensions.

The 15 different 3T-TRAM device designs were manufactured on GlobalFoundries' monolithic silicon CMOS-photonic platform (GF45SPCLO). The devices were manufactured under constrained conditions according to the manufacturer's device design rules (Figure 14). These structures were fabricated as pnpn structures with different lengths, 400/200/200/400 nm,

400/150/150/400 nm, and 400/120/120/400 nm. GF's doping information cannot be disclosed, except for our custom doping concentration below the thin oxide layer was specified as p-type doping 10^{16} cm^{-3}. The storage area located in the center of the device should have a lower doping concentration than the p+ n+ areas at both ends of the side. For the gate oxide, a SiO_2 insulator is used, and it has 5 nm thickness. The thin gate oxide layers can prevent the device from extracting gate leakage currents. Also, aluminum is used for all the three metal contacts, anode, cathode, and gate. Under the anode and cathode contacts, p++ and n++ high doping concentrations are used to create ohmic contacts.

TRAM controls the carrier flow using the barrier height formed between pn-junctions. When anode voltage is increased, carriers are accumulated inside the pn-base regions. These accumulated carriers decrease the barrier height between pn-junctions and generate high currents at a certain voltage. If the accumulated carriers are maintained within the internal energy band of the base area, this is called a programmed state. To maintain the program state, a specific voltage called holding voltage is required. TRAM can continue to maintain the program state while a holding voltage is applied. This means TRAM can have non-volatile characteristics with a holding volage. If the applied voltage is decreased or the accumulated carriers disappear through recombination phenomenon or increased thermal energy, it returns to its original state 0. The states 1 and 0 are distinguished by the currents level. In Figure 16, both the fabricated and simulated devices show sufficiently different current levels to distinguish program states. However, it is difficult to have memory characteristics compared to simulation results since GF devices use the standard doping layers provided by GF that are close to the intrinsic doping concentration.

To have memory characteristics in the fabricated devices, the negative gate voltage is necessary for the low doping devices. The negative gate voltage increases the barrier height

between anode and cathode regions, which generates breakdown phenomenon and memory window (Figure 15 and 16 (b)). Figure 15 shows the energy band diagram of two different devices using a high doped storage area and a low doped storage area, and the increased barrier height by a negative gate voltage.

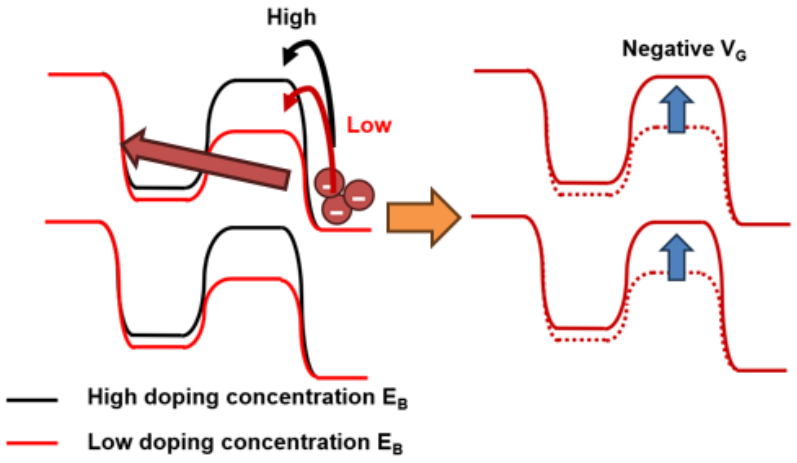


Figure 15. the energy band diagram of two different devices using a high doped storage area and a low doped storage area (left). The right figure represents the energy band diagram of a low doped storage area with a negative gate voltage.

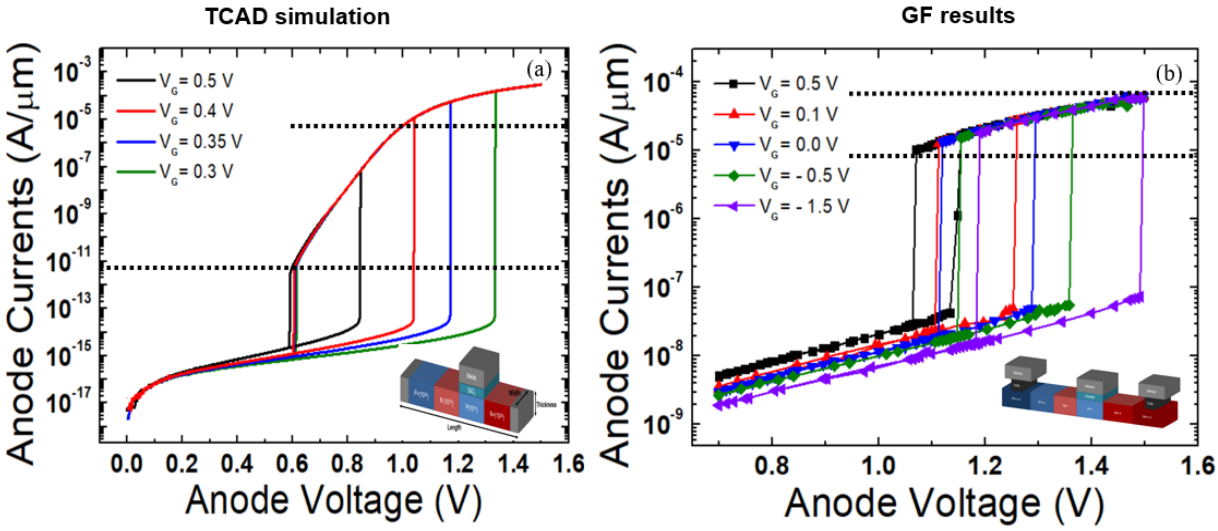


Figure 16. The I-V characteristics of the TCAD simulation devices (left) and the manufactured devices by GF (right).

Our fabricated 3T-TRAM devices are measured by HP 4155A semiconductor parameter analyzer and probe station in Center for Nano-MicroManufacturing (CNM2), University of

California, Davis, California, United States. HP 4155A is an instrument for measuring and analyzing electronic device characteristics. The probe station can be used for general semiconductor parameter testing on up to 4-terminals. To measure the devices, the forward bias is applied onto the anode contact. The applied anode voltage is changed from 0.0 V to 1.6 V and then from 1.6 V to 0.0 V. While the anode voltage is applied, a negative gate voltage is applied into the gate contact as well. Figure 16 (b) shows the measured I-V characteristics and Figure 16 shows the holding voltage and memory window with different gate voltage conditions. The smaller the gate voltage, the higher the holding voltage and memory window are measured.

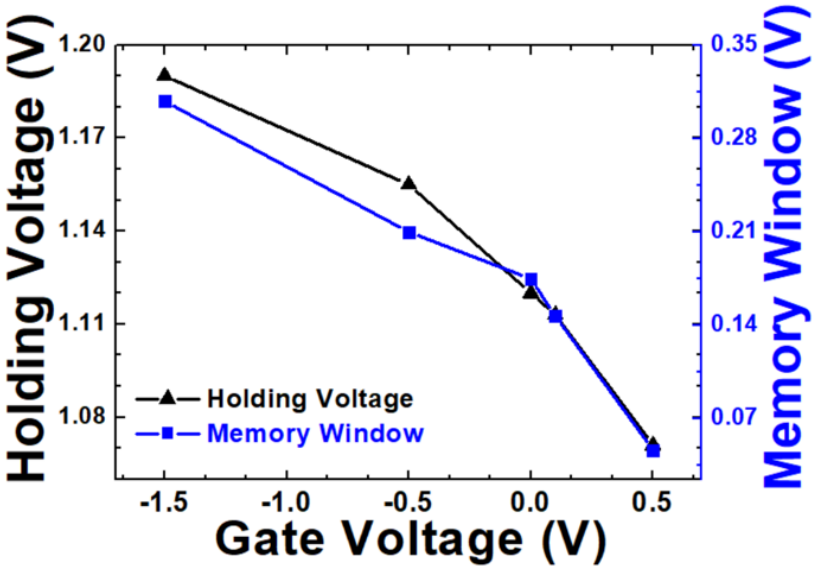


Figure 17. the measured holding voltage and memory window of the manufactured devices with different gate voltage conditions (Figure 15 (b)).

Although the negative gate voltage was used to increase the energy barrier height under the gate contact area and to create wider memory window characteristics, the manufactured devices still have poor memory performance due to the low doping concentration in the storage regions. Compared to the simulation results in Figure 16 (a), a very small ON state area is observed in Figure 16 (b) between the dotted lines. This means that even if the holding voltage is continuously

applied, the GF device still has very poor retention characteristics. This limitation is caused by the small barrier height between anode and cathode (Figure 15). Also, the short channel length with a low doping concentration between high doping concentration areas can lead to fully depleted storage regions. The fully depleted area is generated by diffusion phenomenon from the highly doped area to the lowly doped area. Therefore, the dimension of device and the doping conditions of storage regions should be considered carefully before manufacturing TRAM devices.

v. Dynamic Characteristics of Fabricated Devices

Demonstration of dynamic characteristics of the fabricated TRAM devices utilized KEITHLEY 4200SCS instrument for measurements of AC characteristics (Figure 18). Two pulse generators were used for generating the gate and anode voltage signals, and the cathode contact was connected to ground.

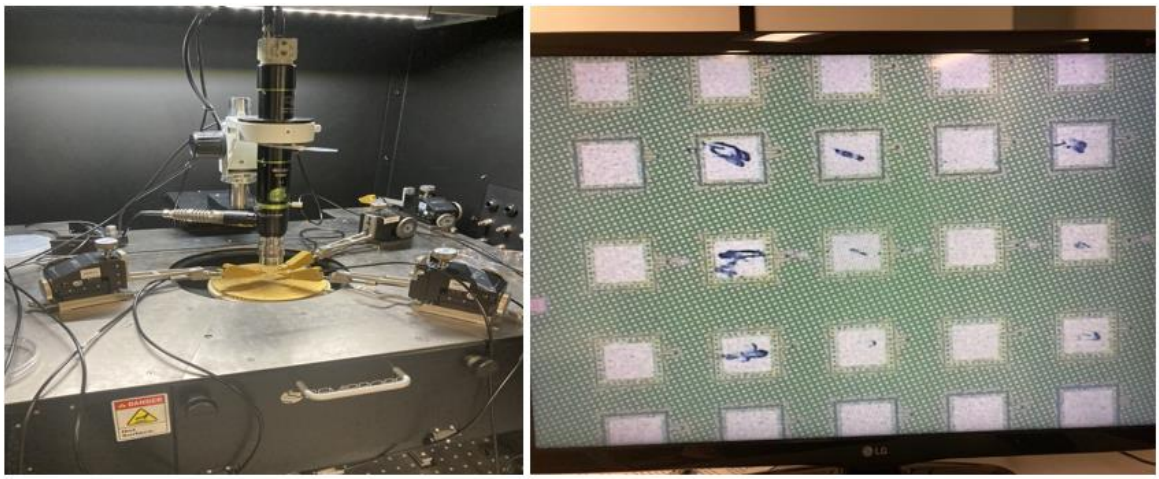


Figure 18. photo of the measurement set up for AC characteristics.

As shown in Figure 19, -0.5 V was applied into the gate voltage, and holding voltage V_A was 1.15 V. For the applied program voltage conditions were V_A = 1.5 V, V_G = -0.5 V, and V_C = GND. The fastest rising time (T_r), pulse width (T_w), and falling time (T_f) are 5 μs, 7 μs and 5 μs

respectively. To measure the retention time of the device, the longest period time of 1.0 s was used in the instrument. These time parameters T_r, T_w, T_f, and period are decided by the probe and KEITHLEY 4200SCS instrument conditions. Therefore, faster device operation could have been demonstrated if faster measurement set up was utilized.

In cycle 1 of Figure 19, low anode currents were measured while the negative gate voltage and the applied positive anode voltage increase to the target voltage level of -0.5 V and 1.5 V respectively. At the target voltage level or around 5 μs, the measured anode current rapidly increases. This is caused by the breakdown phenomenon, and the carriers that have crossed over the barrier from the n+ area, are stored in the n-type storage area between the p-regions. After the pulse width time of 12 μs, the anode current decreases as the anode voltage decreases and as the negative gate voltage approaches zero. However, as shown in the second red box area of cycle 1 (Figure 19), a high anode current level is maintained while a holding voltage of 1.15 V is applied onto the anode contact. Prior to the rising time or the device programming process, there was no current with the same anode voltage of 1.15 V. This result demonstrates that the applied holding voltage can maintain the programmed state and stored carriers of the fabricated 3T-TRAM device.

While applying the holding voltage, we investigated the retention characteristics for 1 second in cycle 2. Even though the holding voltage was continuously applied for 1 second, the anode current, which is the green line in this graph, rapidly decreases to less than 100 nA. This means that all stored carriers in this period have disappeared. This is because the barrier height of the fabricated device is too low to confine the carriers in the storage region for a long time. Therefore, storage regions with higher doping concentrations are necessary for the improvement of these memory reliability issues. Lastly, the same results as the operation characteristics of cycle 1 are repeated from the rising time of cycle 2.

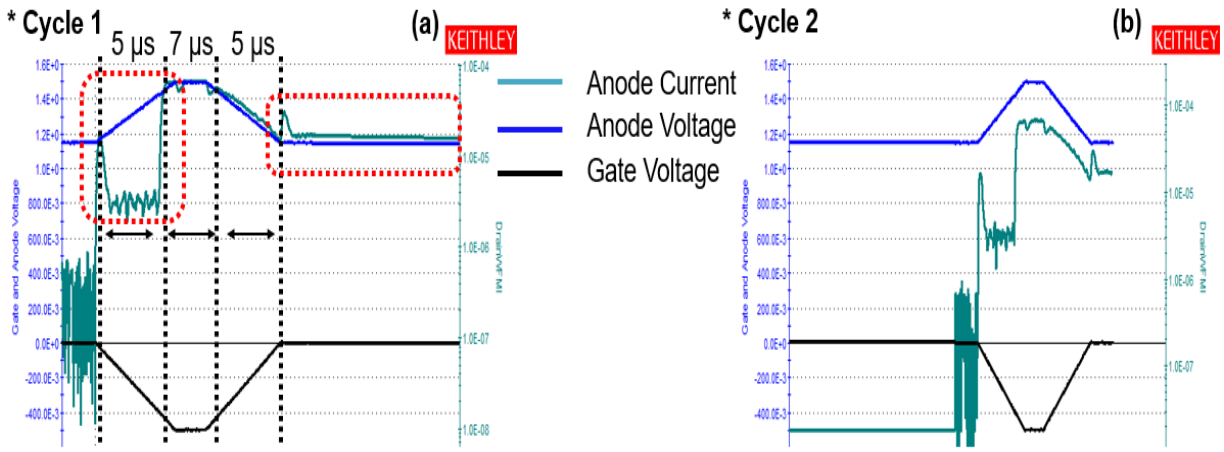


Figure 19. Dynamic characteristics of a fabricated device (Program Voltage (V): V_A = 1.5, V_G = -0.5, V_C = GND, Holding voltage (V): V_A = 1.15).

In summary, based on Figure 16 and 17, the memory operation of the fabricated 3T-TRAM has been demonstrated. Additionally, the AC characteristics of Figure 19 show that TRAM can have non-volatile characteristics while the holding voltage is applied. Due to the instrument limitation, the device could not be measured in faster operation condition. We expect to achieve higher speed operation measurement by employing the probe tip, the probe arm, and the instrumentation compatible with higher bandwidth (>1GHz). The period of testing cannot exceed 1 second in the current instrument. In terms of the device design, the increased doping concentration in the stored region increases the barrier height of the confined or stored carriers. Therefore, excellent retention time and non-volatile characteristics can be expected in 3T-TRAMs with the new design with higher doping concentration.

vi. Compare 2T-TRAM vs 3T-TRAM

In the previous work, we have investigated the 2T-TRAM and 3T-TRAM operation characteristics. 2T-TRAM has a simple structure but has critical limitations in controlling the carrier flow. The commercialized memories are made up of numerous single cells. Memory capacity is determined by the number of single cells, with more cells allowing more data to be stored. Therefore, the simple vertical structure of the proposed 2T-TRAM device can be beneficial for data storage capacity. However, this structure is vulnerable to memory disturbance. Memory disturbance represents a phenomenon in which a read or write operation on a memory cell affects other cells. This phenomenon is common in conventional non-volatile memory devices such as ReRAM (resistive random-access memory), PRAM (Phase-change memory), MRAM (Magnetoresistive random-access memory) and Flash memory. During read or write operation in such memory devices, carriers are transferred to adjacent cells, which can potentially lead to memory degradation or data loss. For example, if a memory disturbance occurs during a read operation, it may affect other cells around the cell being read, which may result in incorrect data being returned. Likewise, if a memory disturbance occurs during a write operation, it may affect other cells except for the write target cell, which leads to reliability issues. Also, although TRAM has non-volatile characteristics, stored carriers can disappear if carrier recombination or diffusion overcome the carrier control of anode voltage. These memory reliability issues must be overcome to realize TRAMs, the next-generation memory for high-speed computing.

As one of the solutions, this dissertation proposes the 3T-TRAM structure with an additional gate contact. Compared to a 2T-TRAM, the 3T-TRAM can easily control the energy barrier height offering its structural advantages. Also, it can reduce the influence of adjacent cells with a strong gate control. These operations by the gate contact were not only investigated with Sentaurus TCAD

in Figure 13, but also demonstrated with devices manufactured by GF. The manufactured 3T-TRAM does not have excellent performance yet. However, this dissertation demonstrated through simulation results that 3T-TRAM performance can be improved with highly doped storage layers. High-speed operation, low leakage current, memory disturbance, and non-volatility characteristics are all sensitive to the doping concentration of the device. The doping concentration dependence of TRAMs can be improved with enhanced gate control.

FUTURE WORK

Table 1. Required performance of target device designs for high-speed computing and replacement of conventional DRAM.

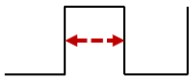
	Design 1	Design 2
Purpose	High-speed computing	Replacement of NVM
Required performance	**High-speed, low-voltage**, but leakage is not important	**Very low leakage current,** but high-speed, low-voltage is not important
Pulse period 	➢ 4Gb/s (250 ps, pulse width) ➢ 100 ps (rise and fall time) **10 us** (**retention**)	➢ 0.5Gb/s (2000 ps) ➢ 1000 ps (rise and fall time) **1 ms** (**retention**)
Peak-to-peak voltage (Gate, Anode)	< 1.4 V (gate, anode) 	< 2.8 V
Leakage current	< 50 pA/cell	< 0.5 pA/cell

Table 1 represents our final design goals in two applications. For the high-speed computing application, high-speed and low operating voltages are necessary. We aim for high-speed memory operation at a few hundred picoseconds. On the other hand, to replace conventional non-volatile memory devices, operating speed and voltages are relatively less important, but very low leakage current and long retention characteristics are desired. To realize both designs for high-performance memory devices, high-quality and high doping concentration processes are necessary. Ion implantation or doped epitaxial growth are methods of incorporating dopants of required concentrations of impurities in the semiconductor devices. These processes are used to place more ions into specific areas of the semiconductor device, decreasing its resistance or controlling certain electrical properties. However, high doping concentration processes have several technical challenges. Precise control of the amount and the depth of the doping is very important. Even small deviations from the designed doping profile can have a significant impact on the electrical properties of memory devices. In ion implantation, a high dosage of ions must be injected from the surface of the target materials towards the bottom. Therefore, advanced equipment and

sophisticated ion implantation technology are required. The current DRAM technologies are not compatible with < 3 nm Gate All Around (GAA) FETs which utilize Si and Ge epitaxial growth methods. Here, TRAM with high doping profiles can be epitaxially incorporated [6].

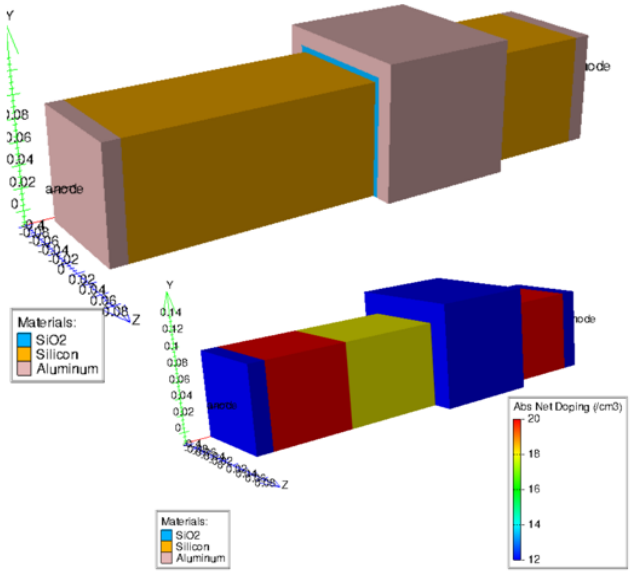


Figure 20. the schematic diagram of Fin-TRAM structure.

For ~12 nm device fabrication technologies, TRAMs with Finfet structures can solve these difficulties due to improved gate control. This multi-gate structure allows for smaller device dimensions and very low leakage currents due to high gate control. This is because the energy barrier height, which is determined by the doping concentration, can be adjusted with an enhanced multi-gate. This structure also shows excellent characteristics in memory operation. The storage area surrounded by multiple gates and oxides suppresses crosstalk from adjacent cells in memory array. Figure 20 shows the Fin-type TRAM structure. The thyristor device with the muti-gate structure is not only very fast and reliable, but also shows the possibility of scaling down [6, 7]. To small dimension at ~12 nm feature sizes, the Fin-type TRAM can be an excellent candidate for reliable high-speed operation memory.

REFERENCES

[1] R. Roy et al., “Thyristor-Based Volatile Memory in Nano-Scale CMOS” ISSCC 2006, 06-09 February 2006.

[2] M.T. Bohr et al., “Nanotechnology goals and challenges for electronic applications,” IEEE Trans Nanotechnol., Vol. 1, no. 1, March 2002. [3] X. Chen et al., “Neuromorphic Photonic Memory Devices Using Ultrafast, Non-Volatile Phase-Change Materials,” Adv. Mater. 2023, 35, 2203909.

[4] Y. Kim et al., “Design and electrical characterization of 2-T thyristor RAM with low power consumption,” IEEE Electron Device Lett 39(3):355–358.

[5] H. Kim et al., “Electrical and data-retention characteristics of two-terminal thyristor random access memory,” IEEE Open J Nanotechno 1:163–169.

[6] Wei-Chen Chen et al., “Highly Pitch-Scalable Capacitor-less 3D DRAM Using Cross-bar Selection with Gate-Controlled Thyristor (GCT) Featuring High Endurance and Free Read-Disturb”, 2023 International Electron Devices Meeting (IEDM), Dec 2023.

[7] Kynghwan Lee et al., “3-STAR : A Super-steep switching, Stackable, and Strongly Reliable Transistor Array RAM for Sub-10nm DRAM and beyond” 2023 International Electron Devices Meeting (IEDM), Dec 2023.