Control of threshold voltages in Si/SiGe quantum devices via optical illumination

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Optical illumination of quantum-dot qubit devices at cryogenic temperatures, while not well studied, is often used to recover operating conditions after undesired shocking events or charge injection. Here, we demonstrate systematic threshold voltage shifts in a dopant-free, Si/SiGe field effect transistor using a near infrared (780 nm) laser diode. We find that illumination under an applied gate voltage can be used to set a specific, stable, and reproducible threshold voltage that, over a wide range in gate bias, is equal to that gate bias. Outside this range, the threshold voltage can still be tuned, although the resulting threshold voltage is no longer equal to the applied gate bias during illumination. We present a simple and intuitive model that provides a mechanism for the tunability in gate bias. The model presented also explains why cryogenic illumination is successful at resetting quantum dot qubit devices after undesired charging events.

I. INTRODUCTION

Gate-defined semiconductor quantum-dots devices provide a platform for a wide variety of solid-state qubits [1–4]. These devices are based on voltage-biased gates fabricated on top of semiconductor heterostructures, either epitaxial or oxide-on-semiconductor, and they provide a highly controllable electrostatic environment for electron and hole-based qubits. However, unlike their classical counterparts, which are substantially uniform across a chip, state-of-the-art quantum-dot devices show variation in operating points between gates even very close together on a chip [5, 6]. Operating points can be manipulated by charge injection [7, 8] and bias cooling [9]. One potential source of variability between devices is at the gate-oxide interface, which hosts charge traps [10] that lead to device instability, electrostatic disorder [11, 12], and charge noise [13, 14]. The latter is a significant source of dephasing for quantum-dot qubit operations [15–17], to the extent that sweet spots [18, 19], symmetric operating points [20–24], and other favorable points in the energy dispersion [25] are used to mitigate its effects.

Threshold voltages for quantum-dot devices are difficult to predict upon cool down, with variations as large as 700 mV possible for nominally identically devices; in part, this variation can arise from trapped charge at the interface. A common experimental technique to reduce this variation is to illuminate the device with light, with a single-photon energy that is larger than the bandgap of the host semiconductor [26–33]. The incident photons generate electron-hole pairs that, evidently, allow for the rearrangement of unwanted charge, which is otherwise locked in place at low temperatures. However, the processes, mechanisms, and limitations of this technique are not well understood.

Here we present a method to systematically tune the threshold voltage of dopantless Si/SiGe devices using optical illumination in the presence of an applied gate voltage. We show that such biased illumination provides precise *in-situ* tuning of threshold voltages over a wide voltage range. We present a model that explains these results in terms of control of the density of trapped charge at the oxide-semiconductor interface. At large positive bias voltages, we argue that this method fills all the available interface states. Under even larger applied gate biases, above 1.5 V in the device studied here, Fowler-Nordheim tunneling results in metastable trapping of even more charge. Unlike measurements at positive gate bias, measurements at large negative bias voltages depend quadratically on light intensity, which suggests a two-photon process may be important in that regime. In addition to providing a tool for tuning threshold voltages, these results enable an understanding of illumination at cryogenic temperatures, which is widely used to provide a consistent reset for Si/SiGe quantum devices.

II. MEASUREMENTS

A. Overview

To introduce the concept, we first demonstrate the ability to reset a Si/SiGe quantum-dot device at cryogenic temperatures using *in-situ* illumination. The inset in Fig. 1(a) shows a scanning electron micrograph (SEM) image of a Si/SiGe quadruple quantum-dot device with two charge sensors, lithographically identical to the device measured in this work. A global turn-on curve, where all gate voltages are swept simultaneously at the same voltage V_{G}, is measured immediately after cooling down the device to 1.2 K with a source-drain bias (V_{SD}) of 50 µV, as shown in Fig. 1(a). We define the threshold voltage (V_{T}) to be the V_{G} that achieves a source-drain current $I_{\mathrm{SD}} = 1$ nA. The blue curve in Fig. 1(a) corresponds to the initial turn-on curve with

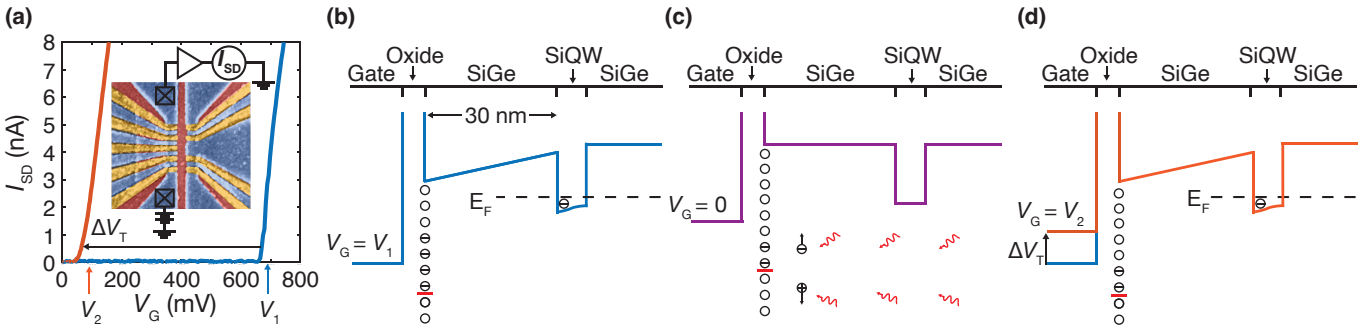

FIG. 1. (a) Global turn-on curve of a quadruple quantum-dot device before (blue) and after (red) illumination. (Inset) A false-color scanning electron microscope (SEM) image of a Si/SiGe quadruple quantum-dot gate-defined device. Different colors denote the three different gate layers of the device, where all gates are treated as one global accumulation gate at voltage V_G. Relevant ohmic contacts and measurement circuit are labeled. (b,c,d) show schematic band diagrams of the device, related to the turn-on curves in (a): (b) before reset (blue), (c) during reset (purple), and (d) after reset (red). V_1 and V_2 are voltages slightly above the threshold V_T needed to accumulate the same charge density in the quantum well, and $V_2 = V_1 + \Delta V_T$

$V_T = 675\,\text{mV}$. After cryogenic illumination with light of wavelength 780 nm from a laser diode (U.S. Lasers Inc D7805I) biased with 15 mA of current, V_T is dramatically reduced by 600 mV to 75 mV (red curve).

Figures 1(b)-(d) present schematic band diagrams of a gated Si/SiGe quantum well device before, during, and after illumination, illustrating how optical illumination can shift the threshold voltage of such devices. In Fig. 1(b), trapped charge (filled circles) initially resides at the semiconductor-oxide interface, which in this case is formed of SiGe/Al_2O_3 (see Appendix A for details of the device fabrication). Here, the short red line indicates mid gap, and filled states above this level trap negative charge at the interface, whereas empty states below midgap trap positive charge (holes) at the interface [34]. This negative charge influences the voltage required to turn on the device, and as shown in Fig. 1(a), the threshold voltage in this case is $V_T = 675\,\text{mV}$. During illumination at $V_G = 0\,\text{mV}$, as shown in Fig. 1(c), photo-generated electron-hole pairs enable charge to accumulate as needed to make the electric field zero in the semiconductor heterostructure, as indicated by the flat bands. In the case shown, the charge density required to screen the electric field from the semiconductor region is negative and of smaller magnitude than the original charge density shown in Fig. 1(b). Following the illumination, a reduced charge density is trapped at the interface, as shown in Fig. 1(d), leading to a lower threshold voltage $V_T = 75\,\text{mV}$ for accumulation. Repeating this reset procedure, i.e., illuminating again with $V_G = 0\,\text{mV}$, causes no further shifts in V_T (see Appendix C for data on repeatability and stability).

In the following we analyze a series of experiments in which a heterostructure field-effect transistor (H-FET), nominally identical to that shown in Fig. 2(a), is illuminated under a wide range of gate bias conditions at a temperature of 3 K. The heterostructure stack for the device is shown in Fig. 2(b). Here, the gate oxide is formed by dry oxidation, and additional details on device fabrication are given in Appendix A. In the following, we observe markedly different results after illumination depending on the sign and magnitude of the bias voltage applied during illumination, which we present below in Secs. B, C, and D.

B. Biased illumination at small gate bias

Figure 2(c) reports the turn-on curves following a series of illuminations at a gate bias of V_B. To ensure a consistent starting condition, before performing each gate-biased illumination we initialize ("reset") the device by illuminating at a V_B of 0 V using a laser diode current of 15 mA for a duration of 30 s. For each curve in Fig. 2(c), we then illuminate with the same laser current and duration and with a non-zero V_B, as indicated by the color bar. We then measure the turn-on curve using a 1 mV source-drain bias. (We note that the data shown Fig. 2 appear unchanged even without the reset step, provided sufficiently long biased-illumination is performed.)

Figure 2(c) shows that the turn-on curves shift dramatically as a function of the applied bias during illumination. The threshold voltage V_T extracted from this data depends linearly on V_B with a slope of 0.94 ± 0.01, a value very close to unity (Fig. 2(d)). We argue here that this behavior arises from mobile, photo-generated electron-hole pairs that, during illumination, move to screen the electric field in the semiconductor. That is, after sufficiently long illumination, carriers of the correct sign accumulate at the oxide-SiGe interface in order to screen the electric field arising from both the applied bias voltage and the work function difference between the top gate and the electrical connection at the quantum well. Evidently these carriers are frozen in place when the light is turned off. With each change in V_B, the amount of

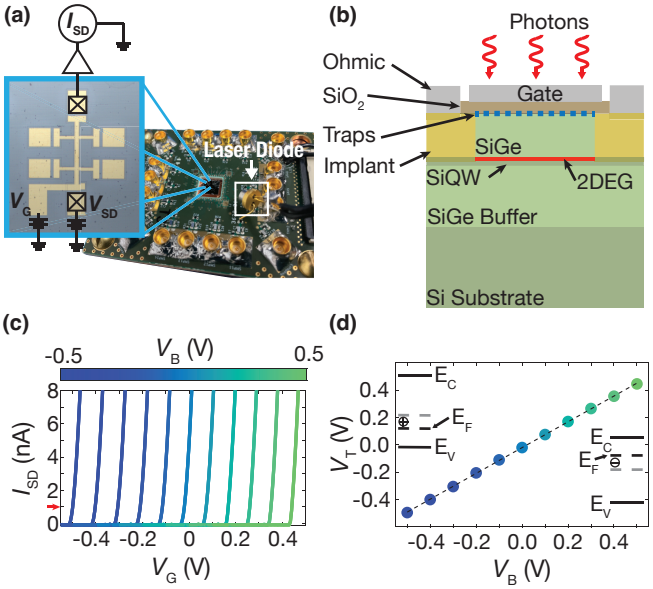

FIG. 2. (a) Image of a typical circuit board and laser diode used for illumination and measurements of a Si/SiGe quantum device. (Inset) Optical micrograph of a H-FET used in the experiment with relevant ohmic contacts connected to the measurement circuit labeled. (b) Schematic illustration of the Si/SiGe H-FET device stack indicating locations of the two-dimensional electron gas (2DEG), trapped interface charge, and incident light radiation. (c) Measured device source-drain current after subsequent gate-biased illuminations for a range of bias voltages. The threshold voltage V_T of each curve is determined at the current value $I_{SD} = 1\,nA$ (red arrow). (d) Extracted V_T as a function of gate voltage. The uncertainty in V_T is smaller than the data points shown. Black dashed line is a linear fit, with a slope of 0.94. (Inset) Diagrams indicating how the position of the Fermi level relative to midgap (dashed gray line) determines the sign of the trapped charge.

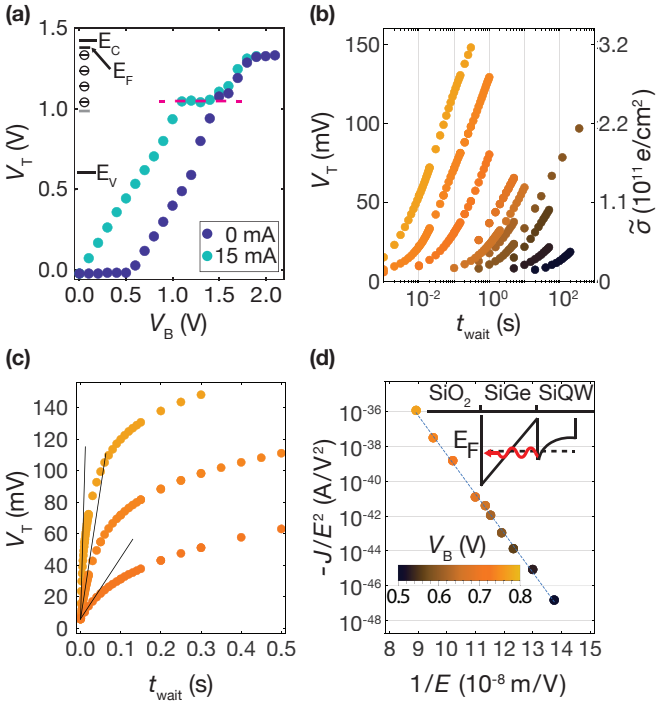

FIG. 3. (a) Measured threshold voltage V_T as a function of bias voltage V_B after a gate-biased 15 mA, 30 s illumination (cyan) and a 30s wait with applied bias but with no illumination (purple). The dashed pink line indicates a plateau in the biased illumination data. (b) Measured device turn-on (left axis) and calculated accumulated charge σ (right axis) as a function of the duration t_{wait} under the 9 different values for the applied V_B. The colors of the data points match the data shown in (d). (c) Three example data sets from (b) plotted on a linear horizontal axis and shown with a linear fit (black lines) to the short-time data points. These fits are used to acquire the Fowler-Nordheim tunneling current density J, which is reported in (d) for all the curves from (b). The inset to (d) shows a schematic band diagram of the Fowler-Nordheim process for this device geometry.

charge needed to screen V_B changes in direct proportion. For this reason, and as derived in Appendix B, the shift in V_T is very close to V_B, and hence the slope in Fig. 2(d) is nearly unity. Depending on the required sign of charge to screen the electric field arising from V_B and the work function difference, either excess electrons (right inset in Fig. 2(d)) or excess holes (left inset in Fig. 2(d)) can be trapped at the interface after illumination.

C. Large positive gate biased illumination

We now explore the effects of biased illumination for larger V_B. As shown in Fig. 3(a), at $V_B = 1.1(1)\,V$, corresponding to $V_T = 1.06(3)\,V$, we observe a plateau in the threshold voltage after illumination, as indicated by the pink dashed line. This suggests an upper limit to the amount of charge that can be trapped at the oxide interface: as charge fills the available interface states, the Fermi energy increases, eventually crossing into the SiGe conduction band, where any additional added charge at the interface is mobile and can escape through the sample ohmic contacts when the light is turned off.

This saturation suggests an average density of interface states $\bar{D}_{it} = 2\sigma_{max}/(eE_G)$, where $E_G = 1.04\,eV$ is the band gap of $Si_{0.7}Ge_{0.3}$ [35], e is the electron charge, and σ_{max} is the maximum density of trapped charge at the interface, which can be negative above mid-gap or positive below mid-gap. We can estimate σ_{max} as follows: the charge density at the oxide interface required to cancel the electric field in the Si/SiGe during illumination is $\sigma = -\frac{\epsilon_1}{d_1}(V_B - V_\phi)$ where ϵ_1 and d_1 are the dielectric constant and thickness of the gate oxide respectively, and $|e|V_\phi = \Phi_{Al} - \chi_{Si} = 0.23\,eV$ is the difference between the work function of polycrystalline aluminum, $\Phi_{Al} = 4.28\,eV$ [36], and the electron affinity of the silicon quantum well, $\chi_{Si} = 4.05\,eV$ [34]. We find $\sigma_{max} = -\frac{\epsilon_1}{d_1}(1.1 - 0.23)V = 1.9 \times 10^{12}\,e/cm^2$,

and the corresponding average density of interface states $\bar{D}_{\rm it} = 3.6 \times 10^{12} {\rm eV}^{-1} {\rm cm}^{-2}$. This value is consistent with the expected magnitude of $\bar{D}_{\rm it}$ at SiO_2-SiGe interfaces fabricated using low-temperature thermal growth [37].

Surprisingly, at even larger $V_{\rm B}$, we observe a transition in $V_{\rm T}$ up and out of this plateau. To understand the origin of this transition, we perform an analogous experiment without illumination during the biasing period: we apply a bias voltage $V_{\rm B}$ for 30 seconds *without* any illumination. As expected and as shown in Fig. 3(a), for small $V_{\rm B}$ there is no change in $V_{\rm T}$. (If there were, the device could not function as an H-FET.) At just above $V_{\rm B} = 0.5\,{\rm V}$, $V_{\rm T}$ begins to shift upward as a function of increasing $V_{\rm B}$, and, further, the measured $V_{\rm T}$ joins up smoothly with the measurements of $V_{\rm T}$ *after* biased illumination. This result strongly suggests that the threshold voltage shifts observed after the plateau shown by the pink dashed horizontal line in Fig. 3(a) are unrelated to illumination. Evidently, at large enough $V_{\rm B}$, a charge density can be trapped in excess of $\sigma_{\rm max}$.

We now present data showing how this charge accumulates. As shown in Fig. 3(b), we find that the measured $V_{\rm T}$ depends on the amount of time $t_{\rm wait}$ spent at $V_{\rm B}$. As with the every measurement of $V_{\rm T}$ with the H-FET, a reset (biased illumination with $V_{\rm B} = 0$) is performed in between the data points of Fig. 3 to erase all history of charge accumulation from the previous measurement. This time dependence suggests that, during application of large enough $V_{\rm B}$, a small current flows that enables charge trapping. We attribute this current to Fowler-Nordheim tunneling, where electrons in the accumulated quantum well tunnel across the SiGe barrier, which becomes triangular in the presence of an applied electric field [38–40].

Interestingly, this process enables shifts in $V_{\rm T}$ above the observed plateau marked by the pink dashed line in Fig. 3(a). We argued above that the plateau arises because the interface states below the band edge have been filled. Electrons that during illumination accumulate at the oxide-semiconductor interface evidently cannot access any additional states during the 30 second illumination. In contrast, electrons accelerated during the Fowler-Nordheim process have non-zero kinetic energy, and we hypothesize that this energy enables injection of charge into the near-interface region of the oxide or into localized states in the thin silicon cap layer [39], either of which would explain how additional charge is trapped beyond that needed to fill the interface trap states up to the band edge.

We now extract the Fowler-Nordheim tunneling current density during the initial stages of the experiment. This current density is given by $J = d\tilde{\sigma}(t)/dt$, where $\tilde{\sigma}(t) = -\frac{\epsilon_1}{d_1} V_{\rm T}(t)$ is the change in the density of trapped charge arising from J, and $\tilde{\sigma}$ is plotted on the right-hand axis of Fig. 3(b). It is important to fit only the first part of the data $V_{\rm T}$ as a function of $t_{\rm wait}$, because the accumulation of charge will screen the electric field in the semiconductor, reducing the Fowler-Nordheim current. Figure 3(c) shows such a linear fit to three example curves from Fig. 3(b). The Fowler-Nordheim current density is given by,

$$J(E) = AE^2 e^{-B/E} \tag{1}$$

where the prefactors A and B depend on sample details [41, 42]. We extract the familiar $\ln\left(J/E^2\right)$ vs. $1/E$ relationship over 11 orders of magnitude, as shown in Fig. 3(d). The extracted fit parameters $A = 1.28 \times 10^{-7}\,{\rm A/V^2}$ and $B = 2.26 \times 10^8\,{\rm V/m}$ predict a minimum bias voltage of 0.52 V to generate sufficient tunneling current to shift the threshold voltage beyond our measurement precision (2 mV), in agreement with the onset of Fowler-Nordheim tunneling in Fig. 3(a).

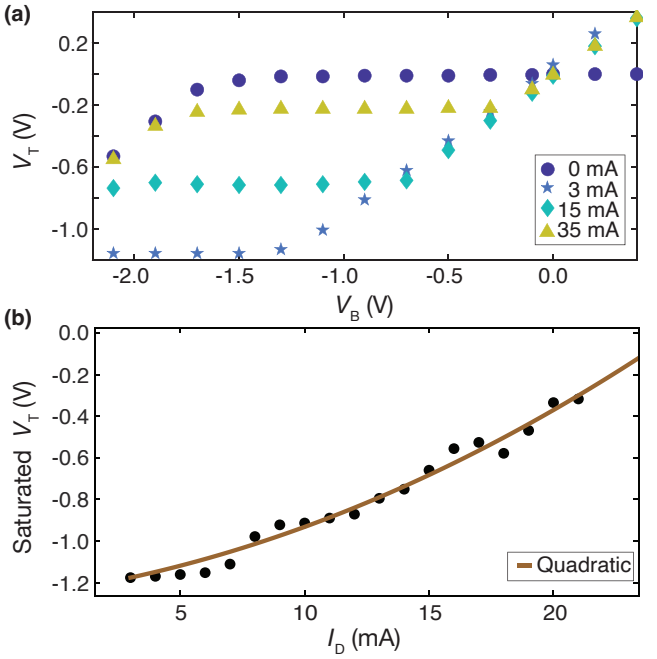

FIG. 4. (a) Measured device threshold $V_{\rm T}$ vs. illumination bias $V_{\rm B}$ for different laser diode pulse heights in the negative-bias regime. The saturation point becomes power dependent for biases $V_{\rm B} < -0.2\,{\rm V}$. (b) Measured device threshold vs. diode pulse height for a fixed pulse time of 30 s. The relationship is found to be quadratic (brown line) with the minimum of the fit at the lasing threshold of 3 mA, suggesting a two-photon process.

D. Large negative gate biased illumination

We now investigate biased illumination for large negative gate voltages. Figure 4(a) shows $V_{\rm T}$ after biased illumination, for three different laser currents all with a 30 s long pulse, and for the case of no illumination. Unlike experiments done at positive $V_{\rm B}$, the threshold voltage for negative bias depends sensitively on laser power.

Furthermore, we observe a saturation point where V_B no longer shifts V_T, and this saturation point is sensitive to the laser power applied during biased illumination.

Figure 4(b) reports the saturation value of the the threshold voltage as a function of the current through the laser diode, which is found to be quadratic with a minimum near the threshold current of the laser diode. The fact that the saturation value depends on laser intensity suggests that there is a competing process that empties trapped charge at the same time that the screening charge is filling trap states from the electron-hole pairs in the SiGe bands, and the quadratic dependence indicates that such a process may involve two photons. At even larger negative voltages (e.g. $V_B < -1.5\,V$ for $I_D = 35\,mA$), Fowler-Nordheim dynamics again take place, as with the positive bias experiments reported above, and as made evident by comparison with the case of no illumination (purple circles).

III. CONCLUSION

We have shown how the threshold voltage of a device at cryogenic temperatures can be tuned *in-situ* using illumination under an applied gate bias. For low bias, these results are consistent with the simple and intuitive hypothesis that illumination generates electron-hole pairs in the bulk semiconductor, enabling charges to fill states at the interface and screen the electric field arising from the bias voltage applied to the gate. These charges are trapped in place after the illumination ends. For larger V_B, we have discussed the important roles of the finite density of available interface states, Fowler-Nordheim tunneling, and two-photon charge liberation. These results and the models presented help explain the effectiveness of the widely-used practice of illumination of Si/SiGe quantum dot qubit devices, and they offer possibilities for expanding the use of such illumination to non-zero gate biases, which would not need to be the same on each gate in a device.

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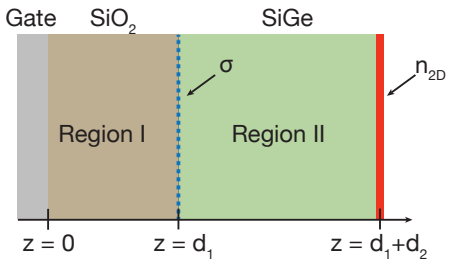

FIG. 5. One-dimensional model for the classical electrostatics inside the Si/SiGe devices used in this work.

APPENDIX A: DEVICE FABRICATION

The quantum-dot device shown in Fig. 1(a) is fabricated on a CVD-grown Si/SiGe heterostructure with a 170 nm $Si_{0.7}Ge_{0.3}$ relaxed buffer layer, 9 nm Si quantum well, 30 nm $Si_{0.7}Ge_{0.3}$ spacer, and a 1 nm Si cap. A 20 nm Al_2O_3 field oxide grown by atomic layer deposition (ALD) isolates the reservoir gates from the implant regions. The gate oxide is grown in the active region of the device where the quantum dots form. This layer consists of 5 nm Al_2O_3, also grown by ALD, to isolate the gate electrodes from the semiconductor. Device bond pads are a 20/160 nm Ti/Pd stack patterned using photolithography. The quantum dot gates consists of three overlapping aluminum gate layers with 35/55/70 nm for the screening, accumulation, and barrier gates respectively, patterned using electron-beam lithography. A $\sim$ 4 nm AlO_x intergate oxide is achieved by a plasma-ash oxide enhancement.

The H-FET measured in this work is fabricated on CVD-grown Si/SiGe heterostructure with a 690 nm $Si_{0.7}Ge_{0.3}$ buffer layer, 12.5 nm Si quantum well, 38 nm $Si_{0.7}Ge_{0.3}$ spacer, and a 3.4 nm Si cap. A gate oxide of thickness approximately 10 nm was grown using a 700 °C dry-oxidation of the Si cap. The 180 nm aluminum top gate is patterned using electron-beam lithography.

APPENDIX B: POISSON EQUATION FOR SI/SIGE WITH TRAPPED CHARGE

We show here that a simple one-dimensional model for the Si/SiGe device predicts a shift in V_T equal to the V_B applied during illumination. As shown in Fig. 5, we calculate the classical electrostatics in two regions: the gate oxide with dielectric constant ϵ_1 and thickness d_1 and the SiGe spacer with dielectric constant ϵ_2 and thickness d_2. Assuming there is no background doping,

and making the simplifying assumption that there is no oxide fixed charge, the electrostatic potential, $\phi_i(z)$, in each region i is linear, and the boundary conditions are

$$\phi_{\mathrm{I}}(z=0) = V_{\mathrm{G}} - V_{\phi} \tag{2a}$$
$$\phi_{\mathrm{I}}(z=d_1) = \phi_{\mathrm{II}}(z=d_1) \tag{2b}$$
$$\epsilon_1 \frac{\partial \phi_{\mathrm{I}}(z)}{\partial z}\Big|_{z=d_1} - \epsilon_2 \frac{\partial \phi_{\mathrm{II}}(z)}{\partial z}\Big|_{z=d_1} = \sigma \tag{2c}$$
$$\phi_{\mathrm{II}}(z=d_1+d_2) = 0 \tag{2d}$$
$$\epsilon_2 \frac{\partial \phi_{\mathrm{II}}(z)}{\partial z}\Big|_{z=d_1+d_2} = n_{2\mathrm{D}} \tag{2e}$$

where V_{G} is the applied gate voltage and $n_{2\mathrm{D}}$ is the density of electrons in the quantum well. Eqs. (2d)-(2e) are consistent with a parallel plate capacitor model where there is no electric field beyond $z > d_1 + d_2$.

This linear system of equations is solved for $\phi_{\mathrm{I}}(z)$, $\phi_{\mathrm{II}}(z)$, and V_{G}, giving

$$\phi_{\mathrm{I}}(z) = V_{\mathrm{G}} - V_{\phi} - \frac{\epsilon_2(V_{\mathrm{G}} - V_{\phi}) - d_2\sigma}{\epsilon_2 d_1 + \epsilon_1 d_2} z \tag{3a}$$
$$\phi_{\mathrm{II}}(z) = \frac{\epsilon_1(V_{\mathrm{G}} - V_{\phi}) - d_1\sigma}{\epsilon_2 d_1 + \epsilon_1 d_2}\big(z - (d_1+d_2)\big) \tag{3b}$$
$$V_{\mathrm{G}} = V_{\phi} - \frac{\epsilon_1 d_2 + \epsilon_2 d_1}{\epsilon_1 \epsilon_2} n_{2\mathrm{D}} - \frac{d_1}{\epsilon_1}\sigma. \tag{3c}$$

V_{T} is the limit of V_{G} as $n_{2\mathrm{D}} \to 0$. As described in the main text, the charge density at the interface is $\sigma = -\frac{\epsilon_1}{d_1}(V_{\mathrm{B}} - V_{\phi})$. By substituting this charge density into Eq. (3c) and taking the limit $n_{2\mathrm{D}} \to 0$, it can be seen that $V_{\mathrm{T}} = V_{\mathrm{B}}$ in this model.

As reported above, the slope of the dashed black line in Fig. 2(d) is 0.94, close but not equal to the unity value predicted by this model. A slope less than unity is consistent with some charge escaping after illumination. It is possible that during illumination some of the charge that screens the electric field from the gate resides in the conduction band rather than in localized states. Such charge presumably can escape when the illumination is terminated, consistent with the physical interpretation described above, in Sec. IIC, of the plateau marked by the pink line in Fig. 3(a).

APPENDIX C: STABILITY AND REPEATABILITY

To demonstrate the level of stability and repeatability of device behavior following illumination, we show in Fig. 6 three turn-on curves, each acquired immediately after 0 V biased illuminations (teal squares, circles, and triangle data points). The blue star data points report a turn-on measurement acquired one month after a 0 V biased illumination. Together, these data sets demonstrate the level of stability and repeatability of the turn-on curves following illumination.

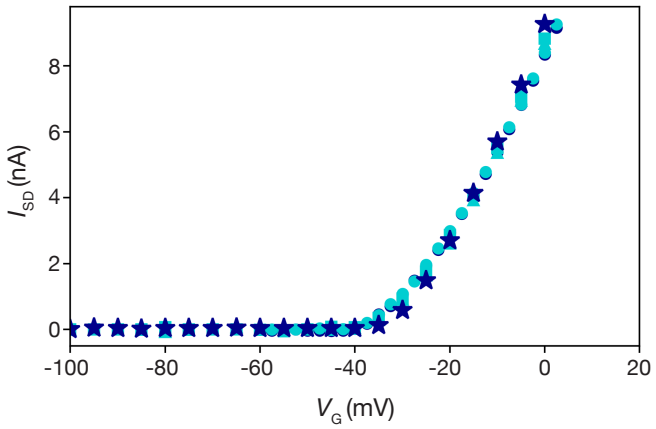

FIG. 6. Turn on measurements of an H-FET device following 0 V biased illuminations. The teal squares, circles, and triangles report three example turn-on measurements—analogous to those shown in Fig. 2(c)—performed immediately after an illumination with a bias voltage of 0 V. Blue stars report a measurement performed one month after a 0 V biased illumination.

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