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Exploring the van der Waals integration for probing and pushing the performance limit of emerging electronic materials

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Chemistry

by

Peiqi Wang

2021

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ABSTRACT OF THE DISSERTATION

Exploring the van der Waals integration for probing and pushing the performance limit of emerging electronic materials

by

Peiqi Wang

Doctor of Philosophy in Chemistry

University of California, Los Angeles, 2021

Professor Xiangfeng Duan, Chair

The continued miniaturization of the silicon-based electronics has been the core of the information technology revolution, but such efforts are quickly approaching the fundamental material limit, which has motivated considerable efforts in exploring a new generation of electronic materials and device architectures. Among many material systems explored, two-dimensional (2D) atomic crystals, wide bandgap semiconductors and halide perovskite have attracted considerable interests for their unique physical geometry or excellent electronic, optoelectronic properties, offering a pathway for further miniaturization of digital devices or diversified function integration for Internet of Things and artificial intelligence. However, to probe the fundamental transport of these materials and capture their intrinsic merits in functional devices is a nontrivial challenge since these materials are usually rather delicate and may readily degrade during the material integration and device fabrication steps. To this end, a physical transfer process exploiting the weak van der Waals (vdW) force to combine disparate materials to form heterojunction interfaces with atomically clean and electronically sharp vdW interfaces, allowing creating high-performance

devices for probing and pushing the limit of these emerging electronic materials. Here in this dissertation, we explore and optimize vdW integration of high-quality and uniquely designed device architectures for creating and investigating high performance devices of emerging electronic materials including 2D atomic crystals, bulk β-Ga_2O_3 and single crystalline lead halide perovskites. We first show the potential of integrating metal contacts with sub-10 nm channel length to 2D materials for probing quantum transport and pushing the on-current for breaking the miniaturization limit of silicon. Then we demonstrated various high-performance vdW heterojunctions based on 3D semiconductors including Schottky diode, p-n diode, metal semiconductor field effect transistors and junction field effect transistors to unlock a rich material library for vdW integration. We also design a feedback gate structure to suppress the threshold voltage roll-off and undesired ambipolar transport in 2D semiconductors, which are crucial for stable device operation for integrated circuits but have seldomly been explored. Finally, we develop a convenient and scalable vdW plug-and-probe technique to integrate top-gate and contact structures on 2D materials and halide perovskite in one step to form ideal transistors for intrinsically probing these novel materials and fabricating high-performance devices. By increasing both complicity of device architectures and the variety of channel material choices while still capturing the merits of these emerging electronic materials, we prove the vdW integration as a universal approach providing prominent opportunities to both fundamental study for novel materials as well as the design of next-generation devices in future semiconductor industry.

The dissertation of Peiqi Wang is approved.

Benjamin Joel Schwartz

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2021

TABLE OF CONTENTS

Chapter 1. Introduction 1

1.1 The potential and challenges of emerging electronic materials 1

1.2 The van der Waals integration approach 4

1.3 Overview of this dissertation 6

1.4 Reference 9

Chapter 2. Chapter 2 Study of ultrashort channel WSe_2 field effect transistors via electromigration 14

2.1 Introduction 14

2.2 Experimental section 16

2.3 Device fabrication and characterization 17

2.4 Conclusion 21

2.5 Reference 22

Chapter 3. Chapter 3 vdW Integrated Devices based on Bulk Materials 24

3.1 Introduction 24

3.2 Experimental Section 26

3.3 Fabrication and performance evaluation of Pt/β-Ga_2O_3 vdW heterojunction 32

3.4 Fabrication and performance evaluation of Si/β-Ga_2O_3 vdW heterojunction 41

3.5 Conclusion 43

3.6 Reference 44

Chapter 4. Suppressed Threshold Voltage Roll-off and Ambipolar Transport in Multilayer Transition Metal Dichalcogenides Feed-back Gate Transistor 51

4.1 Introduction 51

4.2 Experimental section 54

4.3 MoS_2 FBG transistors with suppressed threshold voltage roll-off 55

4.4 WSe_2 FBG transistors with tailored unipolar transport 60

4.5 Conclusion 64

4.6 References 65

Chapter 5. A One-Step Plug-and-Probe Approach for Probing Delicate Semiconductor Materials via van der Waals Integration 69

5.1 Introduction 69

5.2 Experimental section 75

5.3 Transfer whole device structure via graphene sacrificial layer 76
5.4 Performance evaluation of the 2D transistors by vdW plug-and-probe 80
5.5 Performance evaluation of the LHP transistors by vdW plug-and-probe 88
5.6 Conclusion 93
5.7 Reference 94
Chapter 6. Conclusion 102

LIST OF FIGURES

Figure 2.1 Process flow of the ultrashort channel WSe2 device fabrication. 16

Figure 2.2 Feedback controlled electromigration of gold nanowire to generate sub-10 nm nanogap. 18

Figure 2.3 The performance of the sub-10 nm WSe_2 transistor fabricated by feedback controlled electromigration of an evaporated gold nanowire. 20

Figure 2.4 Output curves of sub-10 nm WSe_2 transistors fabricated by feedback controlled electromigration of a vdW integrated gold nanowire. 21

Figure 3.1 Process flow of fabrication of Si strips. 28

Figure 3.2 General model setup to calculate current and density in MESFET/JFET. 28

Figure 3.3 Mobility extraction method from linear region. 30

Figure 3.4 Mobility extraction method from saturation region. 32

Figure 3.5 Schematics of the fabrication flow. 33

Figure 3.6 Characteristics of β-Ga_2O_3 transistor. 34

Figure 3.7 AFM scan on the surface of exfoliated β-Ga_2O_3. 35

Figure 3.8 Schottky barrier diode based on β-Ga_2O_3 and transferred Pt electrodes. 36

Figure 3.9 Temperature-dependent output characteristics of SB diode. 36

Figure 3.10 Transfer curve of MESFET with various backgate voltages and corresponding threshold voltage against backgate voltage. 40

Figure 3.11 AFM image of the MESFET. The thickness of channel material is 122 nm. 41

Figure 3.12 Characterizations of MESFET. 41

Figure 3.13 Characterizations of p-n diode and JFET.. 42

Figure 3.14 Output characteristics of Si (a) and β-Ga_2O_3 (b) transistors used in JFET. 42

Figure 4.1 Competition among different electric fields for a unit volume in the channel. 53

Figure 4.2 Simulation of electron potential energy in the channel region via Finite Element method.. 54

Figure 4.3 Device geometry and DC performance of multilayer MoS_2 transistor. 55

Figure 4.4 Schematics of the normal back gate multilayer MoS_2 transistor. 56

Figure 4.5 Comparison of threshold voltage roll-off and DIBL between the normal back gate transistor and double feedback gate transistor based on multilayer MoS_2. 57

Figure 4.6 Mechanism exploration of the S-FBG multilayer MoS_2 transistor.......... 59

Figure 4.7 Optical image of the D-FBG multilayer WSe_2 transistor. 60

Figure 4.8 Transfer characteristics and operating mechanism of the multilayer WSe_2 D-FBG transistor. 62

Figure 5.1 The vdW plug-and-probe approach enabled by transfer of metal contact and Y_2O_3 gate dielectric. 78

Figure 5.2 Cross-sectional TEM image of the Al_2O_3/MoS_2 interface. 78

Figure 5.3 XPS of the Y_2O_3 film.......... 79

Figure 5.4 TEM image and EDS maps of various elements of the transferred $Au/Ti/Y_2O_3/MoS_2$ interface. 79

Figure 5.5 Transfer Ti as an n-type contact by graphene sacrificial layer. 80

Figure 5.6 Performance of TMD transistors with transferred device architectures. 82

Figure 5.7 Transfer curves of a MoS_2 transistor with 5 nm evaporated and then oxidized Y as top gate. 83

Figure 5.8 C-V and transfer curve of a thick WSe_2 transistor with transferred top-gate and contacts. 84

Figure 5.9 Performance of MoS_2 transistor using CVD graphene as sacrificial substrate.......... 85

Figure 5.10 One-step transfer of Y-shape top-gate/contact architecture.......... 85

Figure 5.11 Double gate performance of vdW integrated WSe_2 top-gate transistor.......... 87

Figure 5.12 CVD MoS_2 transistor array fabricated via vdW plug-and-probe approach.. 88

Figure 5.13 Epitaxial single crystalline $CsPbBr_3$ transistor array fabricated via vdW plug-and-probe approach.......... 89

Figure 5.14 Optical microscopic image of the peeled plug-and-probe electrode array for fabricating perovskite transistors. 90

Figure 5.15 Transfer curve of the perovskite transistor on SiO_2 (300nm) substrate under light illumination. 91

Figure 5.16 P3HT top-gate transistor by vdW plug-and-probe.. 92

Figure 5.17 C8-BTBT top-gate transistor by vdW plug-and-probe.......... 92

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Chapter 1. Introduction

1.1 The potential and challenges of emerging electronic materials

The modern semiconductor industry is entering post-Moore era as the miniaturization of silicon-based complementary metal oxide semiconductors (CMOS) approaches its bottleneck.[1] As the physical size of transistor shrinks in pursuit of denser integration and faster computing, the power density has considerably exceeded the prediction of conventional scaling paradigms, posing an increasing challenge for further miniaturization.[2-3] The rapidly growing leakage power dissipation against size scaling is fundamentally originated from a gradual loss of gate control in silicon transistors with shrinking channel length, referred as the short channel effect (SCE), which leads to degraded subthreshold switching and increased leakage current [4]. Current solutions mainly focus on achieving thinner channel thickness and more effective gating geometry [5], leading to the development of fully-depleted silicon-on-insulator field-effect transistors (FDSOI-FETs) [6], multi-gate structures [7] including fin field-effect transistors (FinFETs) [8] and the upcoming gate-all-around field-effect transistors (GAAFETs) [9-10]. These device architecture engineering strategies have successfully pushed the limit of silicon electronics, but often at the expense of increasing cost and process difficulties [11], and will eventually halt at the physical limit set by fundamental electronic properties of silicon in near future [12]. These fundamental challenges have motivated considerable efforts worldwide to search for new materials that can fuel the continued progress in future electronics.

Alternative to the continued miniaturization towards next-generation digital devices, also known as the strategy of “more Moore”, the International Roadmap for Devices and Systems (IRDS) are also paying close attention to the future direction of “more than Moore” [13], which

focuses more on function diversification including integration of analog devices, power electronics, sensors, optoelectronic functions, and biochips to satisfy the increasing needs of different application domains. To achieve such function diversification is often beyond the reach of the typical silicon electronics and requires to vastly expand the electronic materials with tunable chemical compositions and rich electronic properties [14]. In addition, this route also calls for unconventional computing approaches that surpasses the fundamental limit of Moore's law, such as spintronics [15], neuromorphic computing [16] and quantum computing [17]. These prospects call for the exploration of exotic physical properties in unconventional materials and implementation of unconventional devices such as spin-valves [18] and memristors [19].

In the past two decades, a large variety of novel electronic materials have emerged, particularly including low-dimensional materials including nanowires, carbon nanotubes, graphene and other two-dimensional (2D) atomic crystals for semiconducting channels, dielectrics, interconnects in CMOS, as well as unique functional materials such as quantum dots, molecules and self-assembled monolayers (SAMs), halide perovskite, high-power gallium nitrides and oxides, and topological materials for optoelectronics, non-digital devices and computing beyond CMOS. These emerging electronic materials have the potential to open up many exciting opportunities in both the "more Moore" and "more than Moore" strategies. On the one hand, the atomic-scale dimensions of high-mobility semiconducting nanomaterials could offer the ultimate physical limit for the continued miniaturization of metal-oxide-semiconductor field effect transistors (MOSFETs). For example, 2D semiconductors exhibits natural advantages in overcoming SCE as they could achieve atomically thin channel thickness without performance degradation, which is difficult to achieve with traditional 3D semiconductors [20-21]. On the other hand, the highly variable band structures of many emerging electronic materials bring unprecedented potential in non-digital

functional devices beyond silicon. For instance, halide perovskites are prominent candidates for solar cells [22], light emitting diodes (LEDs) [23] and photodetectors [24], which exhibits low cost and superior power conversion efficiency over silicon optoelectronic devices. The low-dimensional materials with decent electronic performances also feature large surface ratio, ideally suited for sensor applications [25]. Exploiting the exotic physical properties of the novel electronic materials could also lead to entirely new device concepts, such as tunable contact based on graphene with gate-tunable work function [26], spintronic devices based on few-layer transitional metal dichalcogenides (TMDCs) with spin-orbit coupling [27], SAMs with designable tunneling probabilities [28], etc.

Despite many exciting prospects with these emerging electronic materials, to probe the intrinsic electronic properties and to capture such properties in high-performance devices is not straightforward and faces considerable practical challenges. In particular, most emerging electronic materials feature atomic or molecular scale dimensions with highly disparate chemical compositions or lattice structures, and are usually too delicate to maintain their intrinsic properties in the harsh material integration or device fabrication steps, and are thus difficult to integrate with traditional materials to form functional devices with uncompromised performance due to strict lattice matching limitations or processing incompatibilities[29]. In particular, the conventional materials integration methods usually involve aggressive chemical processing and strong chemical bonds at interface, which would inevitably alter the lattice structure of the atomically thin materials and degrade their electronic properties [30-32]. Such incompatibilities have limited our capability to fully capture the intrinsic merits of the novel electronic materials in emerging devices. Careful engineering designs in specific material systems could help alleviate such challenges, but is hardly applicable for the vast library of emerging electronic materials. An alternative of traditional

integration method is highly desired to overcome the lattice matching and process compatibility limits.

1.2 The van der Waals integration approach

To this end, an alternative bond-free integration strategy, in which the pre-synthesized/fabricated material components are physically transferred and assembled together through weak van der Waals (vdW) force, offers a mild "damage-free" integration strategy for highly flexible combination of diverse material components to form diverse heterostructures with atomically clean and electronically sharp interfaces beyond the limits set by lattice matching or processing compatibility requirements. The vdW force is a universal intermolecular force which is generally weaker than typical chemical bonds. The equilibrium distance between interactants is generally considerably larger than atomic or ionic diameter of the elements, where the difference between could be defined as the vdW gap, roughly in the order of 0.2 nm in most materials[29]. The vdW interaction starts to take place when the physical gap between any two materials is reduced to the range of the vdW gap. Although generally perceived as a weak interaction, the vdW force between two fully vdW interacting surfaces is strong enough to overcome gravitational force for most nanoscale and macroscale materials, thus sufficient for creating mechanically stable heterostructures and devices.

The initial efforts of vdW integration may date back to the vdW integration of semiconductor nanowire/nanotube heterojunctions about two decades ago[33], followed by more recent efforts on nanosheets/nanoparticles heterostructures for photodetectors, or nanowire/2D materials heterostructures for *p-n* junctions, high-speed transistors and optoelectronic devices. Later, a wide range of 2D vdW heterostructures[34] with diverse atomic layers has ignited the field and stimulated tremendous interests for both the fundamental studies and new device concepts including some

early examples of BN encapsulated graphene transistors, vertical tunnel transistors, vertical field effect transistors with channel length determined by atomic layer thickness and gate-tunable photodetectors and light emitting diodes. The flexible assembly of diverse 2D/2D heterostructures with widely variable electronic structures and twisting angles while retaining atomically clean interfaces have provided a rich playground for exploring exotic properties, such as unconventional superconductivity, Moiré excitons, and 2D magnetic order, etc. Finally, considering vdW interactions represent a universal force between any two given materials, the vdW integration approach can be broadly expanded to virtually any material systems as long as the interface is flat enough or at least one component is compliant enough to allow the interface to naturally relax to vdW distance to activate the vdW interaction. Such 3D vdW heterostructures are still largely remain unexplored, while has already been proven effective in ideal metal/semiconductor junctions including the delicate 2D materials and halide perovskite [35]. The variety of these vdW heterostructures has proven itself to be potentially a prominent competent for material integration of emerging novel semiconductors.

The vdW integration provides two fundamental advantages over conventional processes for device fabrication based on emerging electronic materials. Firstly, vdW integration decouples the material preparation from device fabrication, bypassing the lattice matching or processing compatibility requirements that seriously limits the variety of heterostructures and devices in traditional integration methods [29]. Secondly, a non-bonding vdW interface avoids strains, defects and disorders that originate from chemical bonding between different crystal structures, as well as any high-energy process-induced damages, allowing to achieve atomically clean and electronic sharp interface with nearly intrinsic charge transport properties [36]. As a result, the vdW integration approach may serves as a universal strategy for creating high-performance heterostructures from

various emerging electronic materials that are not usually compatible with traditional fabrication processes.

Despite the extraordinary potential brought by the freedom of the vdW integration approach, the research field still faces severe challenges in reproducibility, robustness and scalability. These challenges also limit the material combinations of vdW integration despite its theoretical unlimited freedom. To address these challenges requires concerted efforts from multiple disciplines including material chemistry for large area synthesis and fabrication of high-quality vdW building blocks and mechanical engineering for scalable, reliable and automated assembly of vdW heterostructures, which are crucial to unlock the full potential of this approach to achieve a mature integration approach for the prominent emerging electronic materials.

1.3 Overview of this dissertation

In this dissertation, I mostly focus on my efforts in development of vdW integration and other novel device structures beyond 2D heterostructures for probing and pushing the performance limit of the emerging electronic materials.

In Chapter 2, we discussed a unique ultrashort channel WSe_2 transistor structure enabled by feedback controlled electromigration of gold nanowire to create sub-10 nm gap. The short channel transistor shows lower on/off ratio and higher on-current than long channel devices. The vdW integration is fully compatible with the nanowire electromigration approach and can increase the on-current by one to two orders of magnitude due to the damage-free process and the ideal contact interface. This method enable probing quantum transport and pushing the performance of 2D materials in ultrashort channel transistors.

In Chapter 3, we extend the vdW integration approach to 3D materials for flexible integration of highly disparate materials. In particular, by assembling nanomembranes fabricated from bulk platinum, silicon and β-gallium oxide, we demonstrate a variety of functional devices including Schottky diodes, p-n diodes, metal-semiconductor field-effect transistors, and junction field-effect transistors. These devices exhibit excellent electronic performance, in terms of ideality factor, current on/off ratio and subthreshold swing, laying the foundations for constructing high-performance heterostructure devices. With such high-performance devices, we have shown the vdW integration can achieve near intrinsic heterostructures bypassing the strict lattice matching limit for traditional 3D semiconductor integration, which also pave the road for vdW integration to a more general material integration approach.

In Chapter 4, we demonstrate the novel design and fabrication of double feedback gate (FBG) transistors, i.e., source FBG (S-FBG) and drain FBG (D-FBG), to combat the threshold voltage roll-off and bipolar carrier transport. The FBG transistors differ from normal transistors by including an extra feedback-gate, which is directly connected to the source/drain electrodes by extending and overlapping the source/drain electrodes over the yttrium oxide dielectrics on s-TMDs. We show that the S-FBG transistors based on multilayer MoS_2 exhibit nearly negligible V_{th} roll-off at large source-drain bias, and the D-FBG multilayer WSe_2 transistors could be tailored into either n-type or p-type transport, depending on the polarity of the drain bias. The double FBG structure offers an effective strategy to tailor multilayer s-TMD transistors with suppressed V_{th} roll-off and ambipolar transport for high performance and low-power logic applications.

In Chapter 5, we develop a general and convenient plug-and-probe approach based on vdW integration to assemble top-gate and contacts to delicate semiconductors in one step. By peeling off the whole device architecture enabled by graphene sacrificial layer and laminating on the

atomically flat surface of 2D materials and delicate halide perovskite, we can achieve atomically clean and electronically sharp interface of both contact and gate dielectric with channel. The generated 2D transistors have shown nearly ideal subthreshold swing, neglectable hysteresis, decent on/off ratio and on-current. This method is also generally applicable to both MoS_2 and WSe_2 to form n-type and p-type top-gate transistors. Without additional lithography and deposition steps, the generated $CsPbBr_3$ perovskite transistors have achieved the highest reported field-effect mobility and highest channel conductivity. This vdW plug-and-probe method can be extended to centimeter scale to generate 2D/perovskite transistor array with highly uniform performance. Our results has laid the basis for vdW integration to be a general approach for both intrinsic transport study and high-performance device fabrication of delicate semiconductors for future electronics.

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Chapter 2. Study of ultrashort channel WSe_2 field effect transistors via electromigration

2.1 Introduction

Development of traditional silicon-based transistors, described by Moore's Law, has encountered its bottleneck due to physical and technological limit. The effort to increase high on-current density by shrinking channel length is slowed down by the nontrivial impact of short channel effect at ultrashort channel including the gradual loss of gate control and degraded subthreshold swing (SS). As an alternative to silicon, 2D materials show great immunity to short channel effect[1]. Compared to silicon whose thickness cannot be reduced to nanometer scale without degrading its mobility[2], 2D materials have an atom-scale thickness with dangling-bond-free surface, allowing fabrication of high-performance FETs fully exploiting their high mobility to further increase on-current. The ultrathin channel thickness has loosened the requirements for scale-down of gate dielectric thickness, as can be seen from the criterion of device dimensions immune to SCE[3]:

$$L_{\mathrm{ch}} \gg \lambda = \sqrt{\frac{\varepsilon_{\mathrm{semi}}}{N\varepsilon_{\mathrm{ox}}} t_{\mathrm{ox}} t_{\mathrm{semi}}} \quad (1)$$

Where L_{ch} is the channel length, λ is the characteristic length describing gate field penetration to channel, $\varepsilon_{\mathrm{semi}}$ and $\varepsilon_{\mathrm{ox}}$ are dielectric constant of semiconductor and gate oxide, respectively, t_{semi} and t_{ox} are thickness of semiconductor and gate oxide, respectively, N is effective gate number depending on how gate surrounds channel. With channel thickness more than possibly 10 times smaller than current process nodes, the channel length limit of 2D materials is much smaller than silicon [4], not to mention further mobility degradation that silicon and other traditional semiconductors suffer in miniaturization to a sub-5 nm regime [5-6]. Such superior immunity to short channel effects suggests prominent potential of 2D materials in high-performance ultra-short FETs.

They could be a possible substitute of silicon-based transistors and could create more efficient logic gates.

Compared to the mature technology of short-channel silicon-based transistors, 2D materials FETs with channel length less than 10 nm are seldom studied due to a low success rate in device fabrication. Besides, the current industrial device fabrication tools are often too expensive and sophisticated for research, not to mention many steps are not compatible with 2D materials. Several in-lab methods including nanotube gating and contact on partially metalized MoS_2, are reported to achieve ultrashort gating length[7-8], while their actual channel length is micrometer scale with large ungated area, which limits their on-current. Another method of widening grain boundary of graphene electrodes by plasma etching to create ultrashort gap, is heavily relying on random grain boundaries of chemical vapor deposited (CVD) graphene[9], which is not desired for rational designs.

Here we present fabrication of sub-10 nm WSe_2 field-effect transistors via electromigration. Electromigration refers to migration of metal atoms and break of metal wire when applying strong electric field[10], usually responsible for interconnect failure in integrated circuits. However, proper control of electromigration can create very narrow nanogap (less than 10 nm) in a consistent manner[11]. Electromigration can often be observed in metal wires with large current density and metal atoms with high mobility, such as gold. In this method, we applied a feedback-controlled voltage to gold nanowire to open a sub-10 nm gap, which defines the channel length of the WSe_2 transistor. This approach is also compatible with van der Waals (vdW) integration to further increase the on-current density. Our approach provides a convenient way to study the carrier transport and device performance of 2D transistors.

2.2 Experimental section

***Electromigration design*:** A labview program attempting feedback control of electromigration is designed. Normal electromigration cannot be properly controlled when the nanowire starts to break. In this stage the resistance of nanowire begins to increase, resulting in increasing voltage applied on the nanowire, which accelerate the breaking of nanowire and the whole system loses control[12]. Thus, the voltage applied should decrease every time the resistance begins to increase to maintain control of the electromigration. The whole process is totally controlled by program to reduce uncertainty of this method.

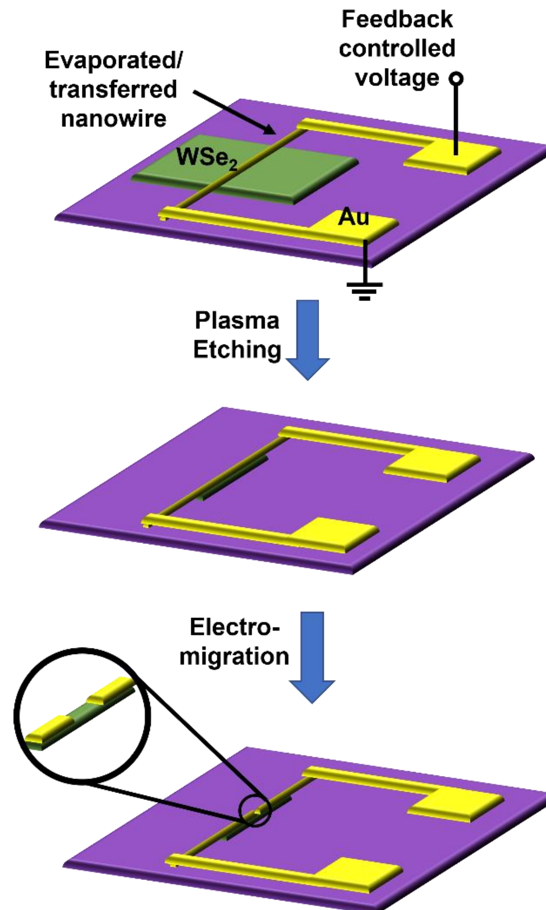

Figure 2.1 Process flow of the ultrashort channel WSe2 device fabrication.

Device Fabrication**:** Gold nanowire with ~100 nm wide is deposited on CVD double-layer WSe_2 by e-beam lithography and e-beam evaporation. Double-layer WSe_2 is used to reduce the damage done by evaporating electrodes directly on material. The gold electrode should be as thin as possible to reduce the fringing effect. For transferred electrodes, the nanowire is first deposited on a sacrificial substrate of SiO_2, and then peeled off by PMMA from the HMDS-treated sacrificial substrate and laminate on the CVD WSe_2. Excess area of WSe_2 is removed by oxygen plasma treating using gold nanowire as a hard mask and the residue are fully cleaned by water. Then the programmed feedback control of electromigration is applied on gold nanowire to create an ultra-short channel of less than 10 nm. High-resolution SEM is used to characterize the physical size of the transistors (Figure 2.1).

Device Characterization**:** Lakeshore TTPX probe station and Agilent B2902A source/measure unit (SMU) is used to measure the output curve and transfer curve under different temperature.

2.3 Device fabrication and characterization

To obtain a ultrashort nanogap repeatably in gold nanowire instead of direct thermal burndown to generate gaps of hundreds of nanometers (Figure 2.2a), the applied voltage across the gold nanowire is actively adjusting according to nanowire resistance to prevent irreversible Joule heating. At first, the voltage is ramping up at a constant speed until a high current density generates enough Joule heat to activate the electromigration, indicated by resistance of the gold nanowire increasing to break a set-up limit (usually 105%-110% of original resistance). Then the voltage is draw back instantly to avoid uncontrollable thermal burndown while still keep electromigration active. The feedback voltage is controlled by a simple Labview program on SMU to ensure in-time response in the order of milliseconds, enough to keep electromigration at a mild speed. Such feedback controlled electromigration will continue until the nanowire will have a

weak connection of only a few atoms wide indicated by resistance reaching a few quantum resistance, when the final breakdown occurs and end the whole process. The I-V curve of the whole process is shown in Fig. 2.2b. With the fast-responding feedback-controlled electromigration, a sub-10 nm gap can be constantly produced (Figure 2.2c). The tunnel current of the nanogap is neglectable at low voltages (Figure 2.2d), which is desired to use the remaining part of the gold nanowire as source and drain electrodes.

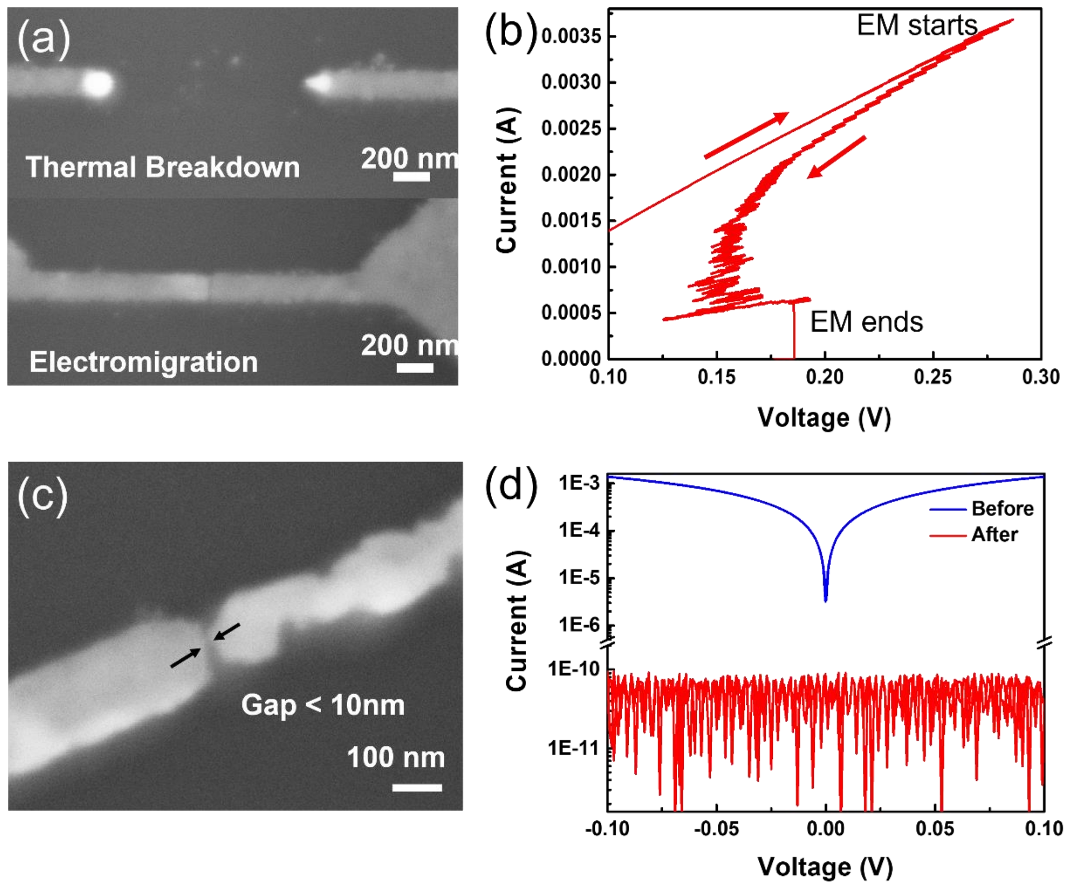

Figure 2.2 Feedback controlled electromigration of gold nanowire to generate sub-10 nm nanogap. (a) SEM images of thermal breakdown vs. electromigration breakdown of a gold nanowire. (b) A typical I-V curve of a gold nanowire during feedback electromigration process. (c) SEM images of a nanogap break by feedback electromigration. (d) The linear I-V sweep of the gold nanowire before and after electromigration.

The precise and repeatable approach to achieve a sub-10 nm gap in gold nanowires can be adapted to the fabrication of a sub-10 nm WSe_2 transistor as described in Figure 2.1 and experimental section. To minimize the disturbance of conductance of WSe_2 to the electromigration process and to prevent the potential degradation to WSe_2 bilayers, we apply a positive back gate voltage to completely turn off the WSe_2 layers, where the current only flows through the gold nanowire during electromigration. The generated WSe_2 has a channel length at the order of 10 nm, which is extremely difficult or complicated to be achieved using classic semiconductor processes. The ultrashort channel WSe_2 devices show gate modulation in channel resistance (Figure 2.3a, 2.3b). However, the on/off ratio is significantly lower than long-channel device, which is a typical short channel effect, indicating the channel length is much shorter than the characteristic length of WSe_2 (tens of nanometers). Another nontrivial difference from long channel is that the on-off ratio rapidly decreases at higher drain voltage (Figure 2.3c), which can be explained by tunnel current of the nanogap at large voltage. This phenomenon is rarely seen in 2D materials but is common in many molecular junctions. Such feedback controlled electromigration could help unravel the largely unexplored charge transport of 2D materials at ultrashort channels, which is previously difficult and expensive to realize. The on-off ratio could be increased to 10^3 by decreasing the temperature to alleviate thermal emission of charge carrier into channel (Figure 2.3d). With such short channel, the on-current density is nearly 3 orders of magnitude higher than long channel device with similar evaporated contacts and back gate.

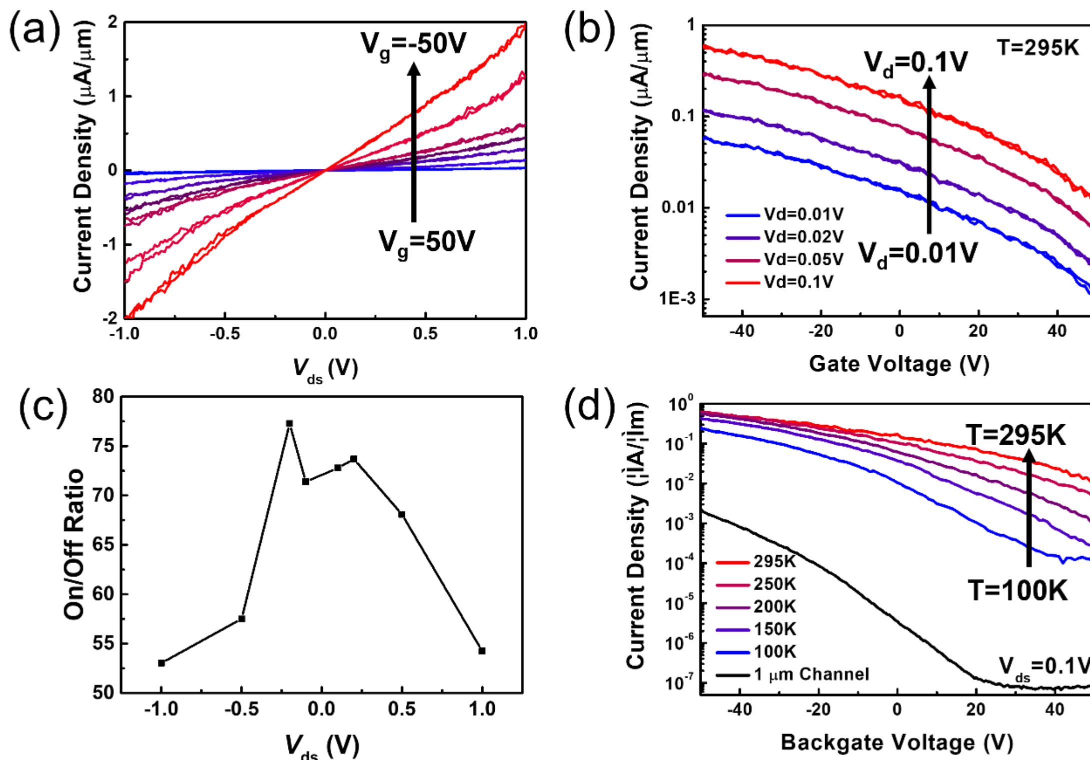

Figure 2.3 The performance of the sub-10 nm WSe_2 transistor fabricated by feedback controlled electromigration of an evaporated gold nanowire. (a) Output curves at various back gate voltages. (b) Transfer curves at various drain voltages. (c) On-off ratio as a function of drain voltage. (d) Transfer curves at various temperatures compared to the transfer curve of a long-channel device.

The current density of both short channel and long channel transistors are limited by the degradation of CVD WSe_2 by the high-energy atom bombardments during metal evaporation. The van der Waals (vdW) integration provides a damage-free approach to assemble the gold nanowire and WSe_2 bilayers via weak vdW force. By simply replacing the deposited nanowire with transferred nanowires in the developed process, we can achieve an on-current of 40 μA/μm at V_{ds}=1 V (Figure 2.4) with similar on/off ratio as evaporated ones and a two-terminal field-effect mobility of 15 $cm^2 V^{-1} s^{-1}$, which are one to 2 orders of magnitude higher than evaporated short channel effect. The optimized vdW interface has freed such sub-10 nm WSe_2 transistors from the

interface disorders introduced by evaporation that impairs its carrier transport properties, unlocking intrinsic probing and pushing the on-current in these ultrashort channel transistors.

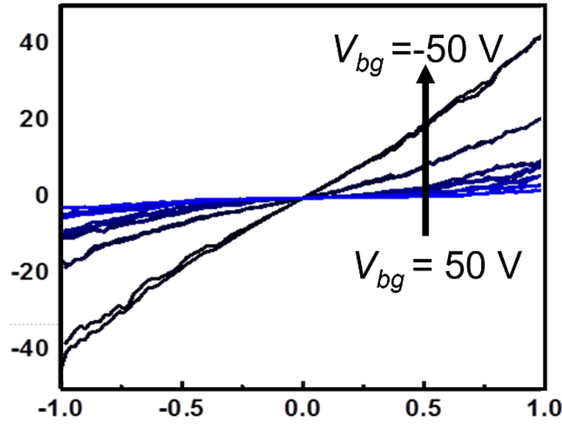

Figure 2.4 Output curves of sub-10 nm WSe_2 transistors fabricated by feedback controlled electromigration of a vdW integrated gold nanowire.

2.4 Conclusion

Our approach of combing the unique ultrashort channel enabled by feedback-controlled electromigration and the vdW integration has provided a potential way to study the unique transport properties such as ballistic transport and like-molecular electronics in ultimately scaled 2D transistors, which is extremely difficult to achieve via traditional device integration approach, benefiting both fundamental research and exploiting the prominent potential of 2D materials beyond silicon-based devices in future electronics.

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Chapter 3. vdW Integrated Devices based on Bulk Materials

3.1 Introduction

Heterostructures, consisting of various metals, semiconductors and insulators, are the material foundation for modern electronics and optoelectronics[1]. A range of high quality heterostructures have been fabricated via well-developed molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) in the past decade[2]. However, these strategies usually involve one-to-one chemical bonds and are generally limited to those materials with highly similar lattice symmetry and lattice constants, thus similar electronic properties. Such an intrinsic limitation poses considerable constraints on the choices of materials for designing functional devices. In contrast, a physical assembly approach that explores van der Waals (vdW) force to integrate distinct materials without direct chemical bonds offers an alternative integration strategy without lattice and processing limitations. This approach, often being referred as van der Waals integration, is becoming especially popular for two-dimensional (2D) material heterostructures and devices[3-14]. Leveraging the unprecedented flexibility of vdW integration to combine 2D materials with radically different chemical compositions, crystal structures or lattice orientations has led to the demonstration of high performance transistors or nearly ideal diodes that truly capture the intrinsic merit of 2D materials[15-18], and the discovery of exotic electronic and photonic characteristics such as unconventional superconductivity and Mott-like insulating behavior in twisted graphene, Moiré excitons in transition-metal dichalcogenides[19-25].

Extending the van der Waals integration approach beyond 2D materials could drastically enrich the materials kit, allowing to explore a rich library of well-developed material systems for realizing unprecedented functionalities by design. Indeed, many exciting developments have been reported on the mixed-dimensional heterostructure of 2D and 3D interface[5], i.e., graphene-silicon

hybrid modulator and detectors[26-28], $MoTe_2$-silicon light emitting diodes and photodetectors[29], Ga_2O_3-Graphene barrister[30], and WSe_2-Ga_2O_3 transistors[31]. Nevertheless, there are few reports of vdW integrated functional devices based on pure three-dimensional (3D) bulk materials[6].

Here, we demonstrate that vdW integration technique could be utilized to construct functional devices based on 3D materials, including Schottky-barrier (SB) diode, p-n diode, metal-semiconductor field-effect transistor (MESFET), and junction field effect transistor (JFET) based on Sn-doped β-Ga_2O_3 strips, peeled off from the bulk crystals, with Ohmic contacted metal electrodes as the basic semiconducting channel platform. Atomically flat Pt metal strips were then fabricated and directly transferred on top of β-Ga_2O_3 via well-developed transfer contacts method, thus forming a typical two-terminal SB diode and three-terminal MESFET simultaneously.Taking a step further, we also constructed p-n junction and JFET by directly peeling off Si strips from the commercial silicon-on-insulator (SOI) wafer and transferring onto the β-Ga_2O_3 strips. With a similar vdW integration process, these building blocks were assembled into p-n junction diode and JFET at the same time. Although traditional methods could be used for the fabrication of β-Ga2O3 FETs[32-37], there is no reports of vdW integrated β-Ga_2O_3 MESFET or Si/β-Ga_2O_3 JFET to date. Finally, we show the resulting diodes and transistors exhibit excellent electronic performance, with an ideality factor of 1.14, current on/off ratio over 10^8, and subthreshold swing (SS) of ~85 mV/dec. Such 3D-3D MESFETs and JFETs have outperformed previous low-dimensional vdW-integrated device due to the mature doping techniques and broader options in bandgap engineering (Table 3.1).

Table 3.1. Performance of van der Waals MESFET/JFETs.

Type	**Materials**	**Ideality factor**	**Normalized on-current $I_{ds}(L/W)$ @V_{ds}=±1V (μA)**	**Gate leakage (pA)**	**Ref**
1D-2D	BP/ZnO JFET	1.32	0.4 μA (nanowire)	10^3	[38]

2D-2D	NiO_x/MoS_2 MESFET	2.49	1	10^{1}	[39]
	NbS_2/MoS_2 MESFET	1.8-4.0	0.1	$<10^{0}$	[40]
	$MoTe_2/MoS_2$ JFET	-	4	10^{2}	[41]
	SnS/MoS_2 JFET	6	3	10^{0}	[42]
2D-3D	WSe_2/Ga_2O_3 JFET	4.3	4	$<10^{-2}$	[43]
	p-Si/MoS_2 JFET	-	0.5	10^{-1}	[44]
3D-3D	Pt/Ga_2O_3 MESFET	1.14	15	10^{-2}	This work
	p-Si/Ga_2O_3 JFET	1.45	36	10^{0}	This work

3.2 Experimental Section

***β-Ga_2O_3 membranes transistor*:** The β-Ga_2O_3 single crystal, which is intentionally n-type Sn-doped with an effective doping density of approximately 1×10^{18} cm^{-3}, was grown by the edge-defined film-fed method (MTI Corp.). β-Ga_2O_3 is a 3D crystal that belongs to the C2/m space group with lattice constants a=1.22 nm, b=0.303 nm, and c=0.580 nm, and angle β=103.8°. The single-crystalline β-Ga_2O_3 with a monoclinic structure could be cleaved into ultra-thin flakes along the (100) plane direction, similar to those exfoliation process in layered 2D materials. The large lattice anisotropy, originating from its strong in-plane force and weak out-of-plane force, enables the simple peeling off process of a single-crystalline β-Ga_2O_3. β-Ga_2O_3 was first exfoliated with scotch tape, yielding flakes with thickness measuring about 100 nanometers. After exfoliation, the nanoflakes were directly transferred onto a doped Si wafer with top SiO_2 thickness of 285 nm. Heavily p-doped Si was used as the back gate, and the gate dielectric was a thermally grown 285-nm thick SiO_2 layer. Ti/Au (20 nm/300 nm) contacts were patterned using EBL followed by EBE process to form the source and drain electrodes.

***Atomically flat metal strips*:** we used typical lift-off process to produce these metal strips on the $SiO_2/p^{++}Si$ with well-polished surface. The deposited metals could duplicate the morphology of the polished Si surface with atomic-level roughness. Combined with the transfer contacts technique that has been well-developed in our group[23], high-quality metal strips could be peeled off in wafer scale.

***Releasing of the Si strips*.** The Si strips are obtained via wet etching sacrificial layer method. To fabricate p-n diode and JFET, silicon-on-insulator (SOI) (top Si of 700 nm thick, p-doped density of $\sim 10^{20}/cm^3$) is purchased from Universal Wafer corporation with a 2-μm thick SiO_2 sacrifice layer on bulk Si substrates. Photoresist was patterned into strip ($3\times10\ \mu m^2$) on substrate using typical photolithography. Using the patterned photoresist as a mask, the exposed Si was dry etched for 5 mins via reactive ion etching (RIE) under 250 mtorr CF_4, 50 mtorr O_2 under 200 W incident power. After that, we dissolved the photoresist in acetone. To release the Si strips, the SiO_2 sacrificial layer is selectively etched by diluted buffer oxide etcher (BOE) for 10 mins. PMMA supported by dummy Si wafer is used to pick up Si strips from the etched SOI wafer (Figures 3.1d, e). Repeat the picking up process to expose the top atomically flat Si surface. The PMMA holding slab with Si strips was dipped in BOE for 1 min to remove the natural SiO_2 layer. Finally, the Si strips were transferred on top of prefabricated β-Ga_2O_3 strips on SiO_2/Si (p^{++}) substrate to form typical p-n diodes and JFET, via home-built transfer station combined with the microscope. Following is typical nanofabrication process to produce contact on top of the Si strip via EBL followed by EBE (Ti/Au, 20/300 nm).

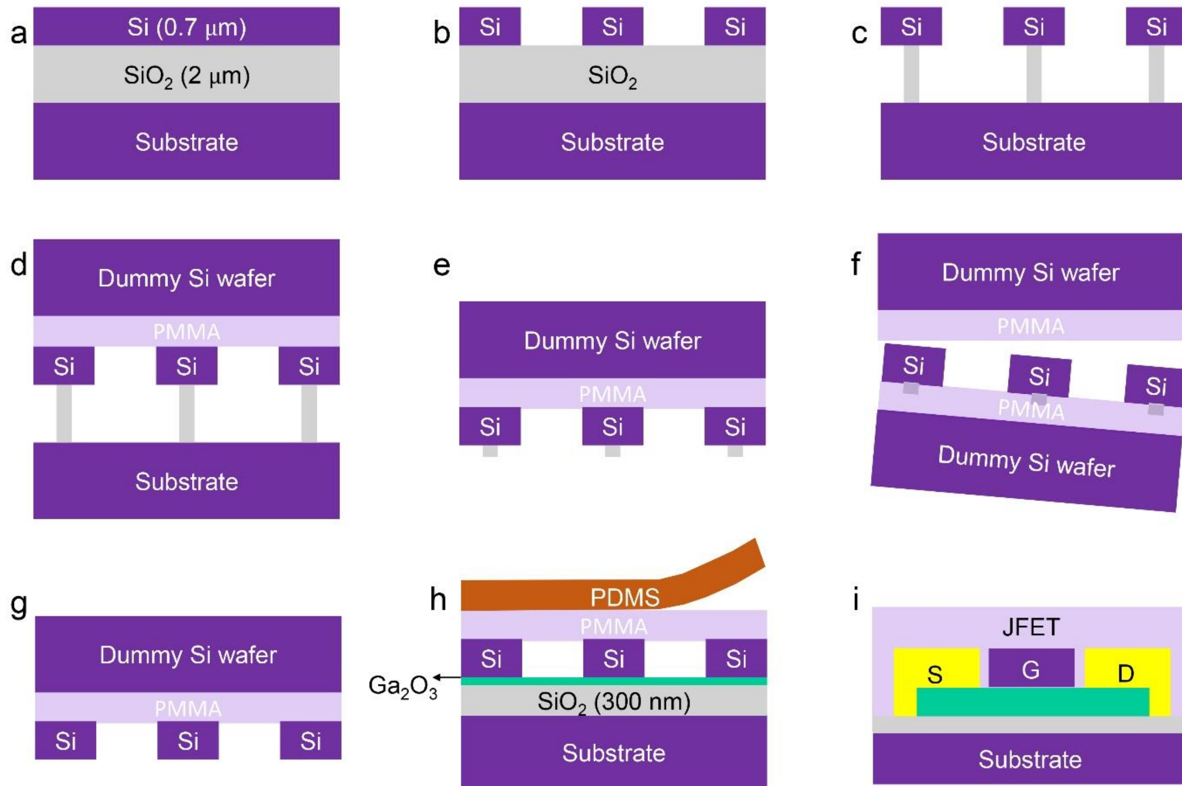

Figure 3.1 Process flow of fabrication of Si strips. Cross-section view of wet etching sacrificial layer processes: commercial SOI (a), Si patterning (b), SiO_2 etching (c), PMMA attaching (d), Si strips releasing and cleaning (e), peeling off to expose the atomically flat Si top surface (f), removing the natural oxide SiO_2 (g), Si integration with β-Ga_2O_3 (h) and final JFET (i).

The derivation and validity of mobility extraction from the linear region. Here is a simple derivation to justify Equation (7) as a valid mobility derivation method for MESFET or JFET:

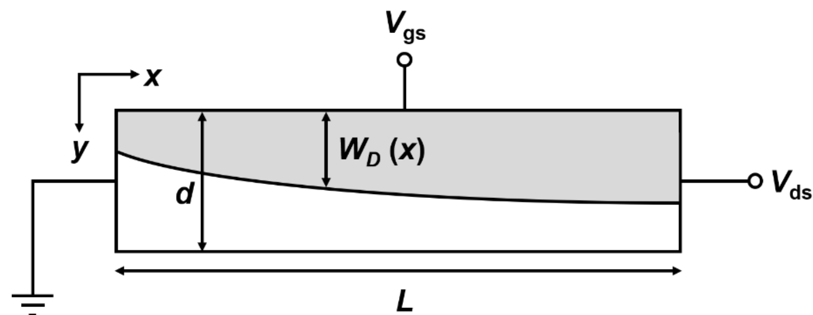

Figure 3.2 General model setup to calculate current and density in MESFET/JFET.

Depletion width at position *x* is $W_d(x) = \sqrt{\frac{2\varepsilon(V_{bi}+V(x)-V_{gs})}{qN_d}}$

Channel charge density at position *x* is $Q(x) = qN_d(d - W_d(x))$

The current is given by integration on the whole channel:

$$I_{ds} = \frac{W}{L} qN_d\mu_{ch} \int_0^{V_{ds}} \left(d - \sqrt{\frac{2\varepsilon(V_{bi}+V-V_{gs})}{qN_d}}\right) \mathrm{d}V$$

$$= \frac{W}{L} dqN_d\mu_{ch} \left[V_{ds} - \frac{2}{3}\left(\frac{(V_{bi}-V_{gs}+V_{ds})^{\frac{3}{2}}-(V_{bi}-V_{gs})^{\frac{3}{2}}}{V_p^{\frac{1}{2}}}\right)\right]$$

$$= \frac{W}{L} dqN_d\mu_{ch} \left[V_{ds} - \frac{2}{3}(V_{bi} - V_{gs})^{\frac{3}{2}}\left(\frac{\left(1+\frac{V_{ds}}{V_{bi}-V_{gs}}\right)^{\frac{3}{2}}-1}{V_p^{\frac{1}{2}}}\right)\right]$$

$$\approx \frac{W}{L} dqN_d\mu_{ch} \left[V_{ds} - \frac{2}{3}(V_{bi} - V_{gs})^{\frac{3}{2}}\left(\frac{\frac{3}{2}\frac{V_{ds}}{V_{bi}-V_{gs}}}{V_p^{\frac{1}{2}}}\right)\right] \qquad \text{(when } V_{ds} \ll V_{bi} - V_g = V_{th} + V_P - V_g\text{)}$$

$$= \frac{W}{L} dqN_d\mu_{ch}V_{ds}\left(1 - \left(\frac{V_{bi}-V_{gs}}{V_P}\right)^{\frac{1}{2}}\right)$$

$$= \frac{W}{L} dqN_d\mu_{ch}V_{ds}\left(1 - \left(1 - \frac{V_{gs}-V_{th}}{V_P}\right)^{\frac{1}{2}}\right)$$

$$\approx \frac{W}{L} dqN_d\mu_{ch}V_{ds}\frac{V_{gs}-V_{th}}{2V_P} \qquad \text{(when } V_g - V_{th} \ll V_P \sim 1\text{V)}$$

$$= \frac{\frac{W}{L}dqN_d\mu_{ch}V_{ds}(V_{gs}-V_{th})}{\frac{qN_d d^2}{\varepsilon}}$$

$$= \frac{W\mu_{ch}V_{ds}(V_g-V_{th})\varepsilon}{Ld}$$

Table 3.2 Variables used in derivation and corresponding symbols.

Variables	**Symbol**
Elemental charge	q
Dielectric constant of material	ε
Channel width	W
Channel length	L
Channel thickness	d
Doping concentration (carrier concentration at Vg=0V)	N_d
Field-effect mobility	μ_{ch}
Drain-source current	I_{ds}
Drain-source voltage	V_{ds}
Gate-source voltage	V_{gs}
Built-in potential	V_{bi} (~1 V for our device)
Pinch-off voltage	$V_P = \frac{qN_d d^2}{2\varepsilon}$
Threshold voltage	$V_{th} = V_{bi} - V_P$ (~-3 V for our device)

Thus transconductance at linear region (small V_{ds}, Figure S9) and near threshold (small $V_{gs} - V_{th}$, by taking tangent line at around V_T) is

$$g_m = \frac{\mathrm{d}\, I_{ds}}{\mathrm{d}\, V_{gs}} = \mu_{ch} \frac{W\varepsilon}{Ld} V_{ds}$$

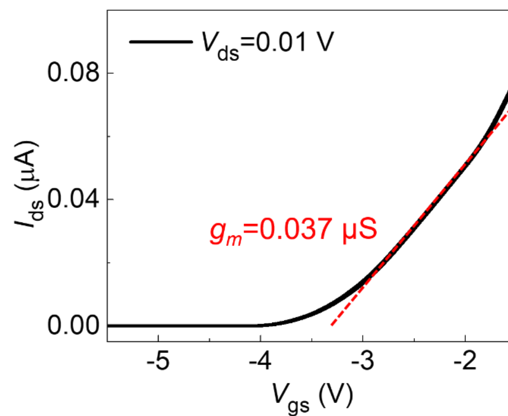

Figure 3.3 Mobility extraction method from linear region.

By plug in the data from transfer curve as well as device dimensions, the mobility can be calculated as:

$$\mu_{ch} = \frac{g_m}{V_{ds}}\frac{Ld}{W\varepsilon} = \frac{(3.7\times10^{-8}\ \mathrm{S})(7.0\times10^{-6}\ \mathrm{m})(1.22\times10^{-7}\ \mathrm{m})}{(1.0\times10^{-2}\ \mathrm{V})(6.6\times10^{-6}\ \mathrm{m})(10.2\times8.854\times10^{-12}\ \mathrm{F/m})} = 53\ cm^2\mathrm{V}^{-1}\mathrm{s}^{-1}$$

There are 2 other common equations to derive mobility[41]. One is to directly calculate from conductivity once we know the carrier concentration ($\mu_{ch} = g_{\mathrm{d}}\frac{L}{W}\frac{1}{qN_d d}$). We did not use this equation because N_d is not accurate. The doping concentration of the bulk material is known to be $1 \times 10^{18}\ \mathrm{cm}^{-3}$ while it cannot be directly used in this equation as doping in thin β-Ga_2O_3 samples usually deviates from bulk ones[45]. N_d can be roughly estimated by the pinch-off voltage of MESFET/JFET ($N_d = \frac{2V_p\varepsilon}{qd^2} = 3 \times 10^{17}\ \mathrm{cm}^{-3}$). The mobility could be estimated by plug in such N_d into the common equation:

$$\mu_{ch} = g_{\mathrm{d}}\frac{L}{W}\frac{1}{qN_d d} = \frac{(2\times10^{-5}\ \mathrm{S})(7.0\times10^{-6}\ \mathrm{m})}{(6.6\times10^{-6}\ \mathrm{m})(1.6\times10^{-19}\ \mathrm{C})(3\times10^{23}\ \mathrm{m}^{-3})(1.22\times10^{-7}\ \mathrm{m})} = 36\ cm^2\mathrm{V}^{-1}\mathrm{s}^{-1}$$

This estimation is close to the results derived from the other equation, which help validate the reliability of extracted mobility.

The other equation is to extract mobility through saturation region $g_m = \frac{\mathrm{d}\, I_{ds,\mathrm{sat}}}{\mathrm{d}\, V_{gs}} = \frac{W}{L} dqN_d\mu_{ch}\left(1 - \left(\frac{V_{bi}-V_{gs}}{V_P}\right)^{\frac{1}{2}}\right)$. A simplified equation $g_m = \frac{W}{L} dqN_d\mu_{ch}$ [39-41] can be used if $\frac{V_{bi}-V_{gs}}{V_P} = 0$, or $V_{gs} = V_{bi}$, and mobility can be calculated from the slope at $V_{gs} = V_{bi}$ (in our case, $V_{gs} \approx 1\ \mathrm{V}$) in the $I_{ds,\mathrm{sat}}$-V_{gs} curve. Again, this formula includes N_d which is not accurately

determined. A rough estimation could also be conducted from the transfer curve at $V_{ds} = 3$ V (our highest V_{ds}).

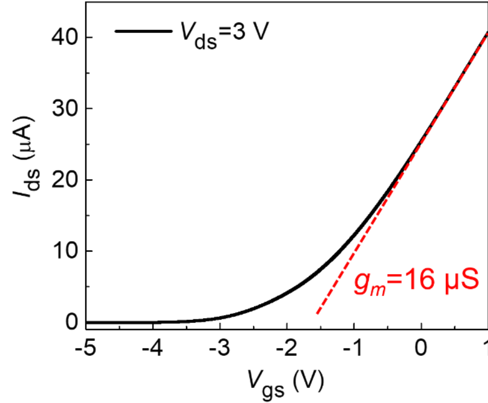

Figure 3.4 Mobility extraction method from saturation region**.**

$$\mu_{ch} = g_{\mathrm{m}} \frac{L}{W} \frac{1}{qN_d d} = \frac{(1.6\times10^{-5}\ \mathrm{S})(7.0\times10^{-6}\ \mathrm{m})}{(6.6\times10^{-6}\ \mathrm{m})(1.6\times10^{-19}\ \mathrm{C})(3\times10^{23}\ \mathrm{m}^{-3})(1.22\times10^{-7}\ \mathrm{m})} = 29\ cm^2\mathrm{V}^{-1}\mathrm{s}^{-1}$$

Please note that this may underestimate mobility because the current is not totally saturated at $V_{gs} = 1$ V and $V_{ds} = 3\ V$. Again, this estimated result is consistent with our method within a reasonable error range.

In general, our equation of extracting mobility from linear region is valid and is independent of estimating the N_d in different sample compared to common methods.

3.3 Fabrication and performance evaluation of Pt/β-Ga_2O_3 vdW heterojunction

Figure 3.5 illustrates the fabrication process to obtain the vdW integrated functional devices such as MESFET and JFET. As shown in Figures 3-1a, 3-1b, we firstly fabricate atomically flat Pt and Si strips, respectively. The Pt strips were first fabricated using typical electron beam lithography (EBL) followed by electron-beam evaporation (EBE) on an atomically flat SiO_2/p^{++}Si substrate (Figure 3.5a, left panel), which could be then mechanically released from the substrate

and transferred onto a target substrate (Figure 3.5b, left panel). The high-quality Si strips were fabricated on a silicon-on-insulator (SOI) substrate, released by a wet etching removal of the SiO_2 sacrificial layer, and transferred onto the target substrate (See Experimental Section and Figure 3.1 for detailed fabrication process).

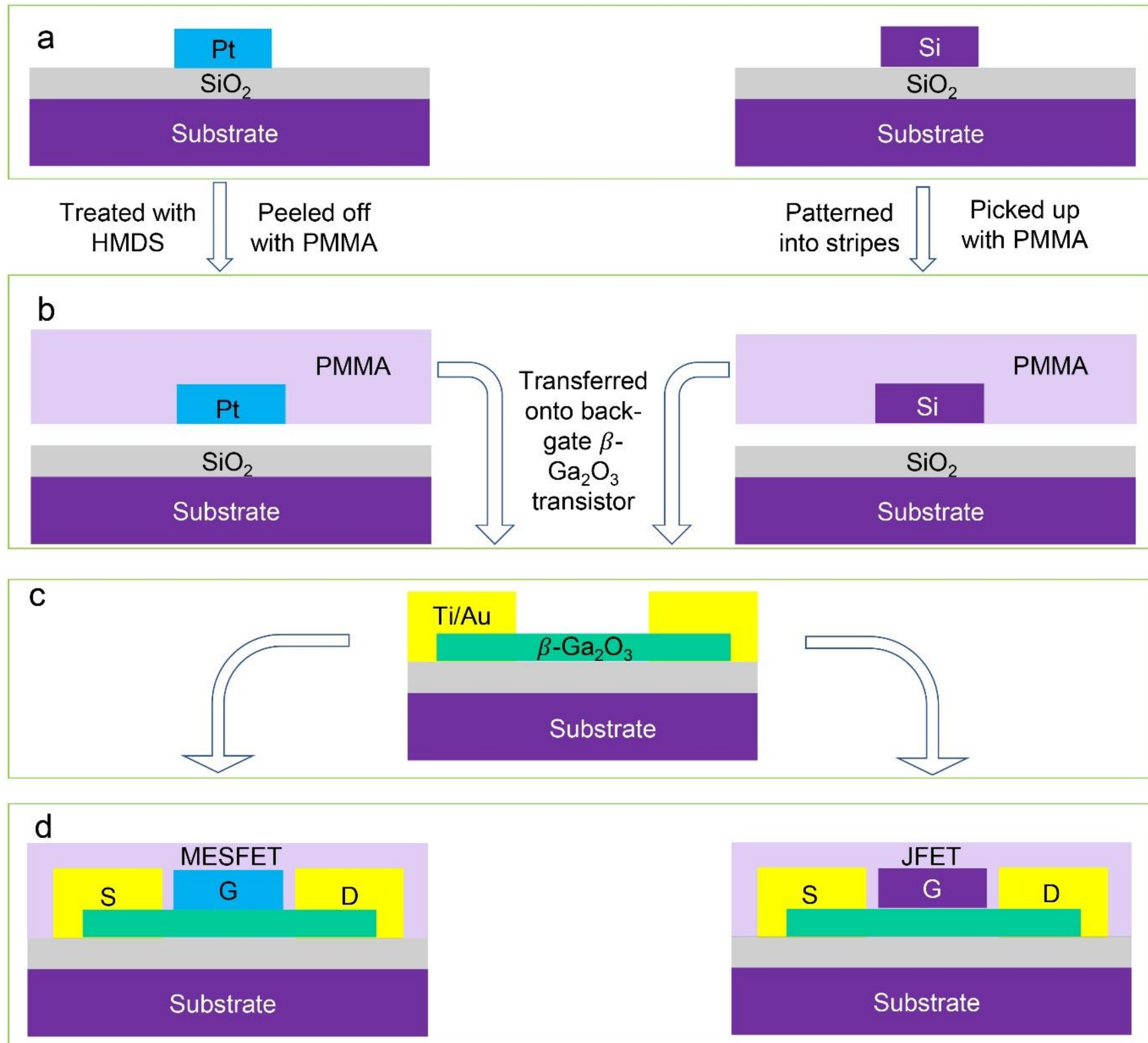

Figure 3.5 Schematics of the fabrication flow. (**a**) Fabrication of Pt electrodes and Si strips. (**b**) Picking up process of Pt electrodes and Si strips. (**c**) Schematics of the back-gate β-Ga_2O_3 transistor. (**d**) Transfer process of the Pt electrodes and Si strips onto the β-Ga_2O_3 channel.

Next, we fabricated back-gate β-Ga_2O_3 transistors as the typical platform for transfer (Figure 3.5c). The back-gate β-Ga_2O_3 transistor could be tuned into normally-on state via a rapid thermal annealing (RTA) process with typical on-off ratio larger than 10^9 and linear output behavior (Details were discussed in Experimental Section, electric characterizations of the back-gate β-Ga_2O_3 transistors before and after annealing were shown in Figure 3.6). Finally, the previously released Pt and Si strips were aligned under an optical microscope and physically laminated on top of the atomically flat β-Ga_2O_3 strips (Figure 3.7) to activate the vdW interaction, resulting in complete Pt/β-Ga_2O_3 Schottky diode (and MESFET) and p-Si/β-Ga_2O_3 p-n diode (and JFET), respectively (Figure 3.5d).

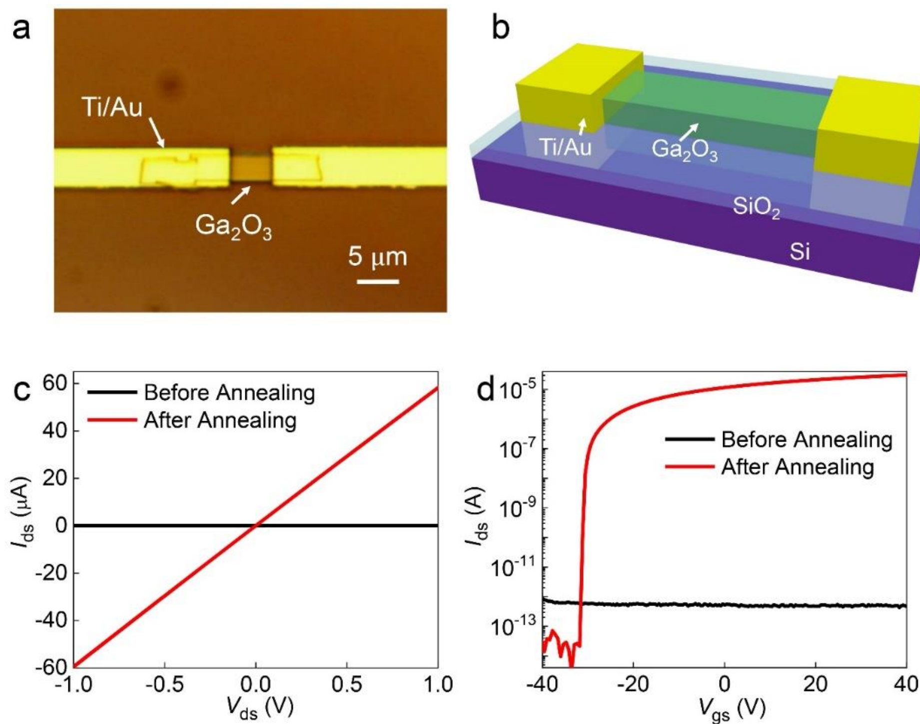

Figure 3.6 Characteristics of β-Ga_2O_3 transistor. (**a**) Optical image of the back-gate β-Ga_2O_3 transistor. The channel length and width of the transistor are 5.5 μm and 2.9 μm, respectively. (**b**) Scheme of a typical β-Ga_2O_3 transistor with Ti/Au contacts. (**c**) I_{ds}–V_{ds} curves from the β-Ga_2O_3 transistor before (black curve) and after (red curve) annealing at 450 °C in argon. (**d**) Corresponding transfer curves of the β-Ga_2O_3 transistor before (black curve) and after (red curve) annealing.

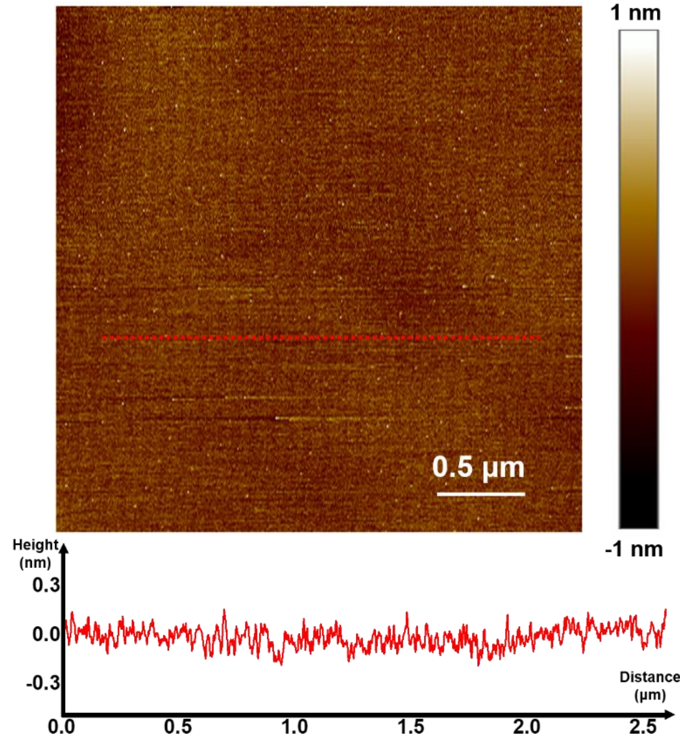

Figure 3.7 AFM scan on the surface of exfoliated β-Ga_2O_3. The surface roughness is 0.102 nm, enabling a clean and smooth vdW interface.

We have then investigated the electronic performance the vdW-integrated Pt/β-Ga_2O_3 Schottky diode and MESFET. Figure 3.8a shows a schematic diagram of the vdW integrated MESFET by transferring Pt electrodes on top of the back-gate β-Ga_2O_3 transistor. Figure 3.8b shows a false-colored SEM image of a typical Pt/β-Ga_2O_3 MESFET, consisting of Ti/Au source-drain contacts and the transferred Pt gate electrode. With a proper rapid thermal annealing (RTA) process, the evaporated Ti/Au contacts form the Ohmic contacts with the β-Ga_2O_3 strip (Figure 3.6). On the other hand, the vdW-integrated Pt electrode display an atomically sharp interface with the β-Ga_2O_3 strip (Figure 3.8c) thanks to its ultraflat surface (Figure 3.9) and can function as a highly reliable Schottky contact, and be configured into either a two-terminal Schottky diode or a three-terminal MESFET simultaneously. Electrical transport studies were carried out in vacuum using Lakeshore TPPX probe station combined with the Keysight B1500 semiconductor analyzer.

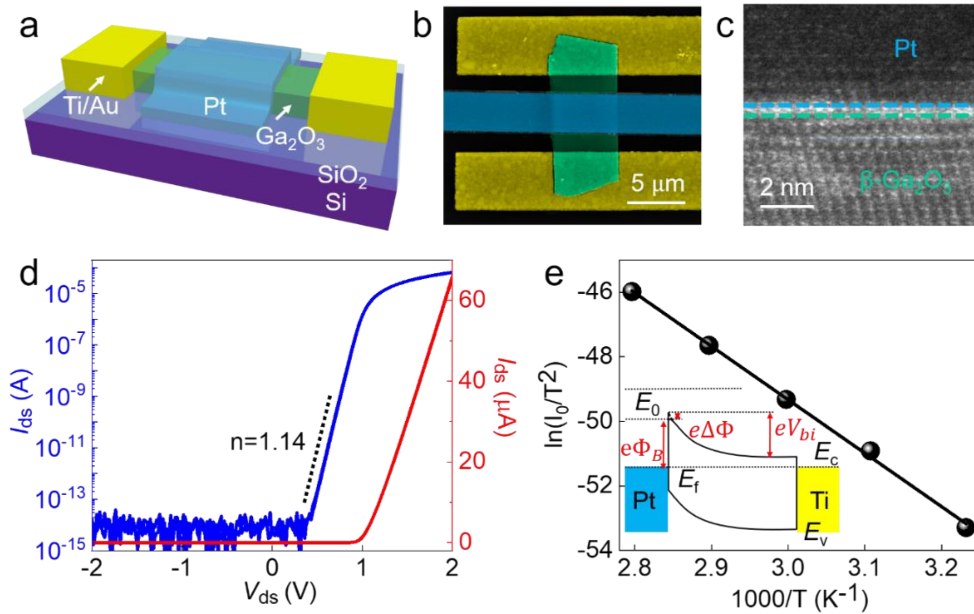

Figure 3.8 Schottky barrier diode based on β-Ga_2O_3 and transferred Pt electrodes. (**a**) Schematics of the MESFET. (**b**) False-color SEM image of the MESFET. (**c**) Cross-sectional TEM image of the Pt/β-Ga_2O_3 interface. (**d**) Temperature-dependent characteristics of I_{ds}-V_{ds} curves of the same β-Ga_2O_3 SB diode. (**e**) Richardson's plot $\ln(I_0/T^2)$ versus 1000/T. Inset is the corresponding energy alignment diagram.

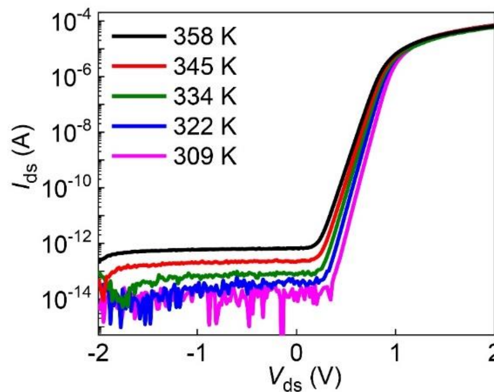

Figure 3.9 Temperature-dependent output characteristics of SB diode.

Figure 3.8d shows the typical *I*-*V* characteristics of the Pt/β-Ga_2O_3 Schottky diode, exhibiting substantially reduced backward current density, uniform diode behavior, and exponentially increasing forward current characteristics that are well-distinguished from the series resistance-

limited region. Explicitly, the reverse current level of the SB diode is of a magnitude of 10^{-14} A, which is the measurement limit of our equipment instead of the lowest value the device could reach. The rectification ratio ($I_{forward}/I_{reverse}$) at ±2V for the vdW integrated Schottky diode reaches up to 10^{10}, which is among the highest state-of-the-art Schottky heterojunctions reported to date[46]. The rapid ramping up of the forward-bias current and the high current density indicated that there was no significant series resistance induced by the ungated β-Ga_2O_3, mainly benefiting from the normally-on behavior of the RTA annealed β-Ga_2O_3 transistor (Figure 3.6d).

The general Schottky diode equations for current transport across the junction can be expressed as[1]:

$$I = I_0 \exp\left(\frac{e(V_A - IAR_s)}{nk_BT}\right)[1 - \exp(-\frac{e(V_A - IAR_s}{k_BT})] \tag{1}$$

$$I_0 = AA^*T^2 \exp(-\frac{e\Phi_B}{k_BT}) \tag{2}$$

$$A^* = \frac{4\pi em^*k_B^2}{h^3} \tag{3}$$

where e, A, R_s, n, k_B, h, T, I_0, A^*, m^*, and Φ_B are the elementary charge, device area, series resistance, ideality factor, the Boltzmann constant, the Plank constant, temperature, saturation current, effective Richardson constant, electron effective mass, and Schottky barrier height at equilibrium (zero bias), respectively. $V_D=V_A-IAR_s$ is the voltage applied on the SB diode. The electron effective mass of β-Ga_2O_3 is $m^*=0.34\ m_0$, with m_0 being free electron mass[47]. According to the method proposed before, when $V_D>3k_BT$/e (~0.08 V), Equation (1) can be simplified as:

$$I = I_0 \exp\left(\frac{e(V_A - IAR_s)}{nk_BT}\right) \tag{4}$$

By fitting the experimental data in Figure 3.8d using Equation (4), an ideality factor of 1.14 was attained, suggesting an excellent vdW interface in Pt/β-Ga_2O_3 heterojunction. The ideality factor of a junction can be expressed as [48]:

$$n = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{W_D} + qN_{SS}\right) \tag{5}$$

where W_D is space charge width, N_{SS} is density of interface states, ε_s and ε_i are the permittivities of semiconductor and interfacial layer, and δ is the thickness of interfacial layer. Notably, the vdW-integrated β-Ga_2O_3/Pt SB diode shows an ideality factor around 1.1 at all temperature measured. Such close-to-unity ideality factor observed in our SB diode indicates a nearly ideal interface with a low density of interfacial states.

To obtain the Schottky barrier height, we have conducted temperature-dependent measurement of the forward *I-V* characteristics of the β-Ga_2O_3 SB diode (Figure 3.9)[49]. The temperature-dependent forward *I-V* characteristics were further analyzed by the Richardson's plot, i.e., the ($\ln\left(\frac{I_0}{T^2}\right) - 1/\mathrm{T}$) plot, as shown in Figure 3.8e. According to Equation (2), it can be deduced that $\ln\left(\frac{I_0}{T^2}\right) = \ln(AA^*) - \mathrm{e}\Phi_B/k_BT$. By fitting through the experimental data, we can get that $\mathrm{e}\Phi_B$ is about 1.43 eV, which is very close to the electron affinity model, indicating that the vdW integration process protects a high-quality interface without introducing unnecessary damages or defects[6]. As shown by the energy band diagram under zero bias in the inset of Figure 3.8e, the relationship between the effective Schottky barrier height $\mathrm{e}\Phi_B$ and built-in potential V_{bi} is expressed as

$$\mathrm{e}\Phi_B = eV_{bi} + \left(E_c - E_f\right) - e\Delta\Phi \tag{6}$$

where E_c and E_f are the conduction band minimum and Fermi level of β-Ga_2O_3, respectively, and $e\Delta\Phi$ is the potential barrier lowering due to the image force produced in the Pt metal under zero bias[1]. It can be deduced that $e\Phi_B$ has 0.17 eV deviation from the theoretical electron affinity model.

With a well-defined Schottky barrier at Pt/β-Ga_2O_3 interface, the Pt/β-Ga_2O_3 heterojunction can be configured into MESFET, in which the Pt electrode functions as a metallic Schottky barrier gate and the β-Ga_2O_3 functions as the semiconducting channel. Taking the study a step further, we characterized the electric transport behavior of the MESFET. The transfer characteristics of the MESFET showed a threshold voltage ocf -3.2 V (V_{th} linear extrapolation details shown in Figure 3.10), SS of 84 mV/dec with a high on/off ratio of $\sim 10^8$. With increasing Drain voltage bias, there is no obvious threshold voltage shift at all. The threshold voltage of the MESFET could be decreased to -0.4 V by applying an additional -40V back-gate voltage (Figure 3.10).

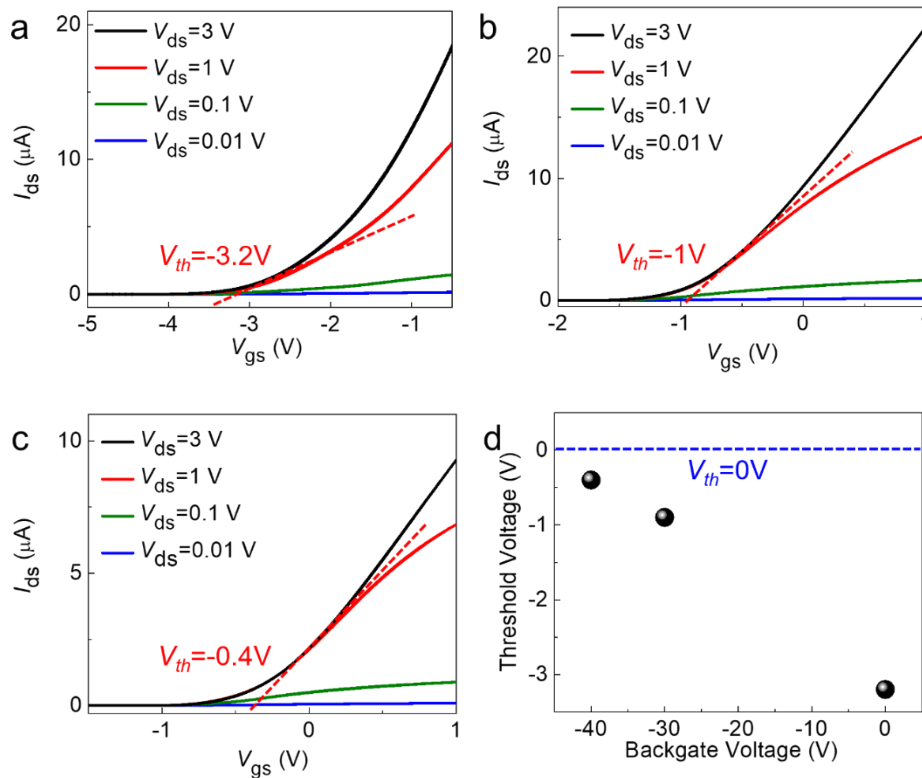

Figure 3.10 Transfer curve of MESFET with backgate voltage of (a) 0 V (b) -30 V (c) -40 V and corresponding threshold voltage against backgate voltage (d).

The room temperature field-effect electron mobility (μ_{ch}) was extracted via the linear region of the transfer curve at small bias and at $V_{gs} \approx V_T$:

$$g_m = \mu_{ch} \frac{W}{L} \frac{\varepsilon}{d} V_{ds} \quad (7)$$

where L and W are the channel length and width, respectively, g_m is transconductance, d of 122 nm is the channel thickness (Figure 3.11), $\varepsilon = 10.2\varepsilon_0$ is the dielectric constant of β-Ga_2O_3[50], N_d of ~10^{18} cm^{-3} is the doping density of the β-Ga_2O_3, and μ_{ch} was extracted of the Pt/β-Ga_2O_3 heterojunction MESFET was approximately 53 cm^2/V·s at V_{ds}=0.01 V. As compared with other mobility extraction methods (shown in methods), this derivation approach does not require a precise determination of the doping level when the conducting channel is scaled from 3D geometry to 2D limit, which is more convenient for determining the carrier mobility. The gate leakage current of the Pt/β-Ga_2O_3 heterojunction MESFET maintained a significantly low level of approximately 10^{-13} A at V_{gs} < -4.3 V. When negative V_{gs} was applied, the depletion region at the gate-channel junction widened and the channel became simultaneously narrower, resulting in an increase in the channel resistance and decrease in source-drain current. Transconductance exhibits the maximum value of 16 μS at a 3 V bias voltage. The I_{ds}–V_{ds} output characteristics of the Pt/β-Ga_2O_3 heterojunction MESFET showed Ohmic behavior, excellent saturation and sharp pinch-off characteristics (Figure 3.12). The excellent transistor characteristics of the Pt/β-Ga_2O_3 heterojunction MESFET again demonstrate high-quality heterojunction interface between the exfoliated β-Ga_2O_3 and transferred Pt electrode.

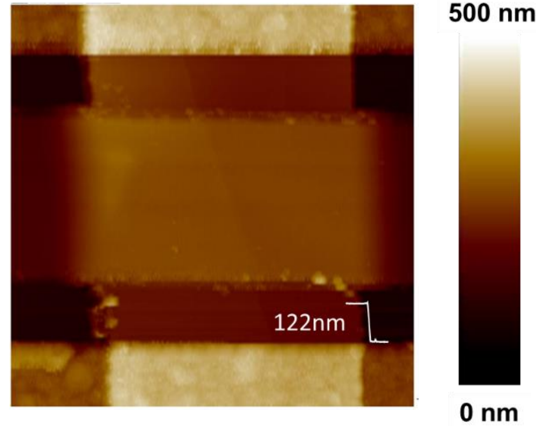

Figure 3.11 AFM image of the MESFET. The thickness of channel material is 122 nm.

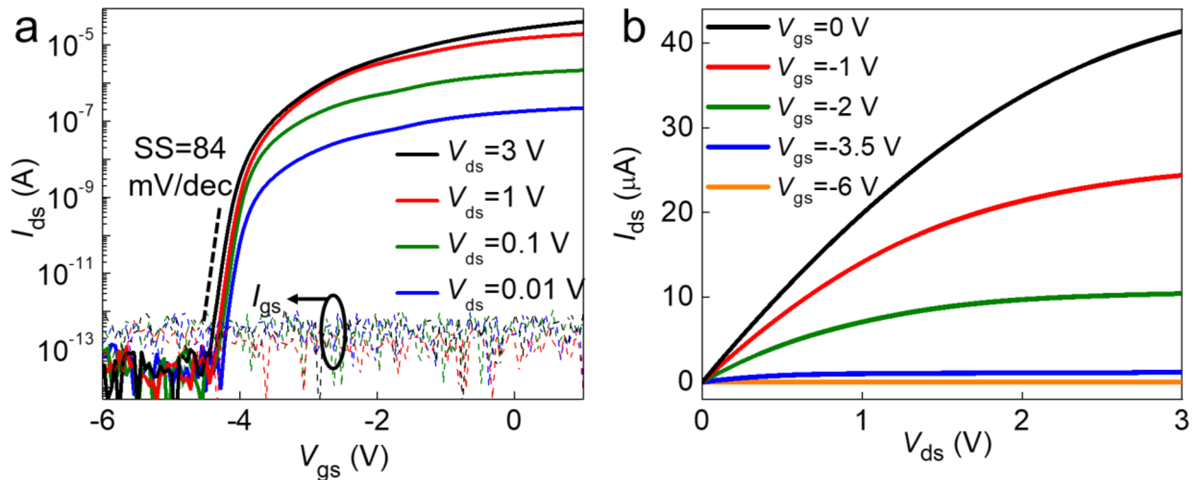

Figure 3.12 Characterizations of MESFET. (**a**) Transfer characteristics of the MESFET. The channel length and width of the transistor are 6.6 μm and 7 μm, respectively. The gate length is 3.5 μm. (**b**) Output characteristics of the MESFET.

3.4 Fabrication and performance evaluation of Si/β-Ga_2O_3 vdW heterojunction

To demonstrate the general applicability of vdW integration in 3D materials, we extended to study the vdW integration among various semiconducting materials that cannot be normally integrated together. To this end, we also used the aforementioned β-Ga_2O_3 as one of the semiconducting channel platforms, and then integrated Si strips atop the channel to form p-n diode

and JFET simultaneously (Figure 3.13a). Ohmic contact with linear *I-V* behavior was made to Si and β-Ga_2O_3 strips by using Ti/Au electrodes with proper RTA processes (Figures 3.13a and 3.13b).

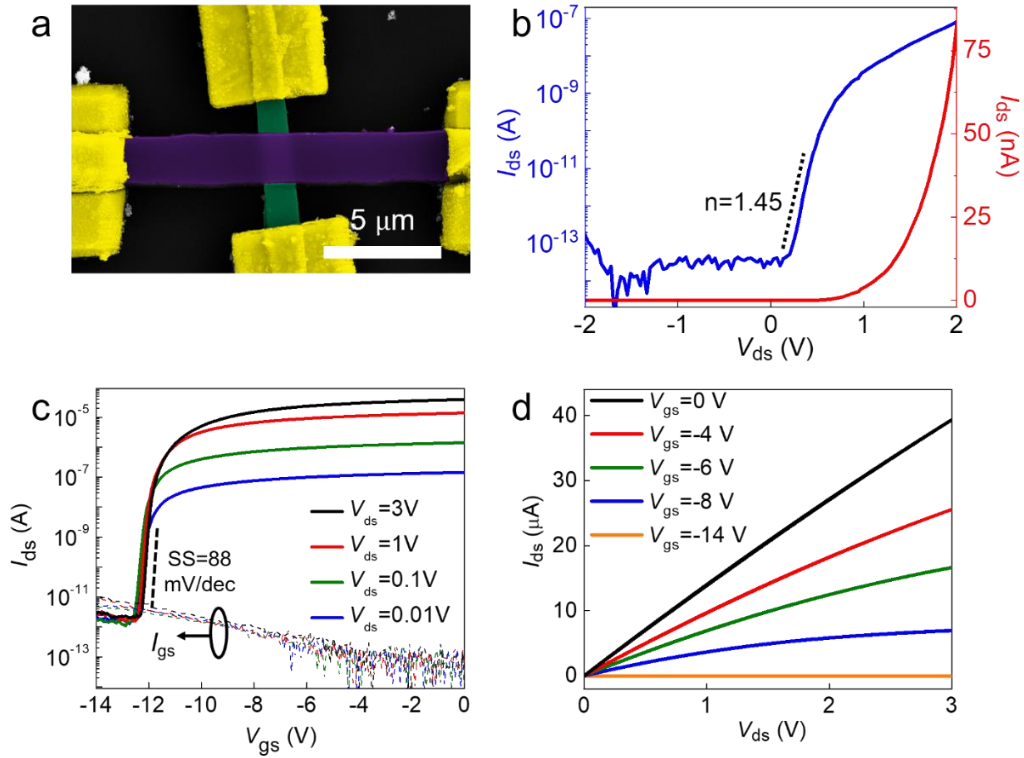

Figure 3.13 Characterizations of p-n diode and JFET. (**a**) False-color SEM image of the JFET. The channel length and width of the transistor are 5.7 μm and 1.4 μm, respectively. The gate length is 2 μm. (**b**) I_{ds}-V_{ds} curves of the Si/β-Ga_2O_3 p-n diode. (**c**) Transfer curves of Si/β-Ga_2O_3 based JFET. (**d**) Corresponding output curves of the JFET.

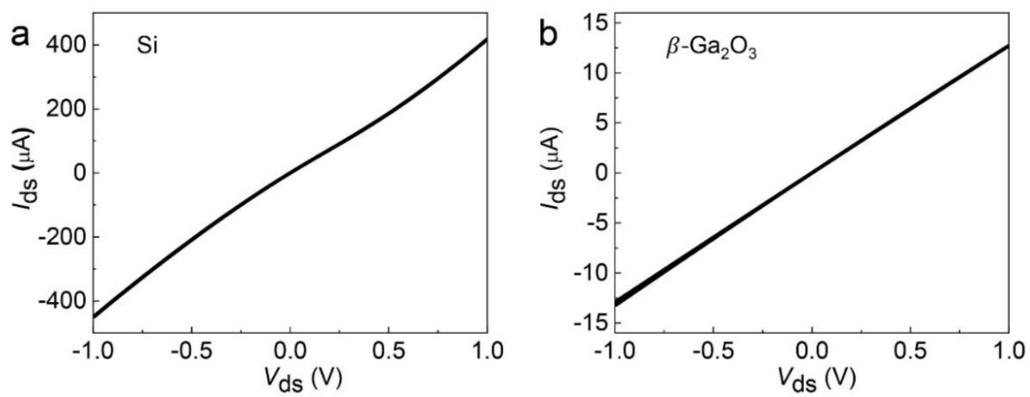

Figure 3.14 Output characteristics of Si (a) and β-Ga_2O_3 (b) transistors used in JFET.

The Si/β-Ga_2O_3 heterostructure exhibits typical rectification behavior with a rectification ratio of about 10^7 (Figure 3.13b). Fitting the I–V characteristic of the Si/β-Ga_2O_3 diode with a standard diode equation results in an ideality factor of 1.45. The relatively large ideal factor than Pt/β-Ga_2O_3 Schottky diode may be attributed intrinsic surface states on Si surface. Similarly, the Si/β-Ga_2O_3 heterojunction can be configured into a heterojunction JFET, in which n-type β-Ga_2O_3 were utilized as the semiconducting channel and the p-type Si as the junction gate. The transfer characteristics (Figure 3.13c) showed a threshold voltage of −12.3 V, SS of 88 mV/dec and a high on/off ratio of ~10^8. By increasing the source-drain voltage bias, there is no threshold voltage shift, indicating that there are few trapped charges at the interface. The I_{ds}–V_{ds} output behavior shows linear I_{ds}–V_{ds} at low bias and clear saturation behavior at high bias (Figure 3.13d), demonstrating excellent transistor characteristics.

3.5 Conclusion

We have demonstrated that vdW integration technique could be extended to 3D materials for creating high quality heterojunction between the materials that cannot be normally combined, enable high performance devices, including Schottky diode, p-n diode, MESFET and JFET, with excellent ideality factor, current on/off ratio, and subthreshold swing. The traditional epitaxial heterostructures usually involve strong chemical bonds (200-1000 KJ mol^{-1}) and often aggressive processing conditions, which could generate substantial interfacial disorder, and thus seriously limits the materials that can be combined. In contrast, the vdW interaction (~10 KJ mol^{-1}) [51-52] doesn't involve direct chemical bond or aggressive chemical processes and thus could allow flexible integration of high disparate materials with preserved chemical and electronic properties for producing heterostructures with nearly ideal interfaces.

3.6 Reference

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Chapter 4. Suppressed Threshold Voltage Roll-off and Ambipolar Transport in Multilayer Transition Metal Dichalcogenides Feed-back Gate Transistor

4.1 Introduction

The rise of semiconducting two-dimensional (2D) crystals has generated much excitement for future electronic and optoelectronic applications[1-2]. Semiconducting transition metal dichalcogenides (s-TMDs) are considered as a potential channel material candidate in the post Moore era[1]. In particular, monolayer MoS_2 transistors could promise high on-off ratio, abrupt subthreshold swing (SS) of 60 mV/decade, and superior immunity to short-channel effects[3-5]. However, monolayer MoS_2 is susceptible to interface trappings and may not be optimum for high-performance applications due to its large bandgap and effective mass[6-7]. To this end, considerable studies have been placed on multilayer s-TMDs to push the on-state current for high-performance applications[8-12]. Nevertheless, multilayer s-TMDs transistors are often plagued by considerable threshold voltage (V_{th}) roll-off, drain-induced-barrier-lowering (DIBL) and ambipolar transport[1, 9, 13-20], all of which could compromise their potential for high-performance and low-power-static modules in modern integrated circuits (ICs)[21]. To date, there is little study on how to mitigate such challenges. Optimizing device geometry could potentially simultaneously suppress these negative effects while retaining high driven output current[22]. In silicon-based CMOS technology, these drawbacks could be well-resolved by using the portfolio of multi-gate techniques such as the tri-gate, Π-gate, Ω-gate and even to state-of-the-art FinFET[23]. However, these mature techniques are not appropriate for 2D materials due to its ultra-thin body nature[2]. Thus, it is necessary to develop new gate geometry to overcome these drawbacks.

Here, we propose a general gate structure to suppress V_{th} roll-off or DIBL as well as tailor the ambipolar transport into unipolar behavior in multilayer TMDs transistors. The device structure

consists of s-TMDs channel, yttrium oxide, source-drain (S-D) contacts and a typical back gate. By extending a segment of S-D contacts over the yttrium oxide, we could introduce two feedback gates (FBGs) adjacent to the S/D, i.e., S-FBGs and D-FBGs, which can effectively clamp the Schottky Barriers (SBs) at the S/D ends, thus making the SB height and width insensitive to the electric field across the channel. Explicitly, we demonstrate that the S-FBGs in multilayer MoS_2 transistors could greatly suppress the V_{th} roll-off as compared with normal back-gate devices, thus effectively reducing DIBL. Furthermore, we showed that the D-FBG multilayer WSe_2 transistors could be tailored into either n-type ($V_{ds}>0$) or p-type ($V_{ds}<0$), depending on the drain bias supply.

Those V_{th} roll-off and ambipolar transport in multilayer s-TMD transistors are fundamentally originated from the competitive control of gate voltage and source-drain bias[24]. At a large drain bias, electric fields created by drain is strong enough to penetrate into the channel region to a certain distance and could compromise the gate control capability over the channel. This penetration increases at high drain voltage. As a result, the potential in the channel region and the resultant concentration of electrons are no longer controlled solely by the gate electrode but are also influenced by the voltage applied to the drain and by the distance between the source and the drain. The loss of charge control by the gate leads to two observable effects: V_{th} roll-off and DIBL[25]. These competition relationships could be analyzed using the three-dimensional Poisson's equation, which shows how the source and the drain compete with gate for the charge control in the channel[25]:

$$\frac{dE_x}{dx} + \frac{dE_y}{dy} + \frac{dE_z}{dz} = \frac{\rho}{\varepsilon} = -\frac{eN_d}{\varepsilon} \text{ (n-type) or } \frac{eN_a}{\varepsilon} \text{ (p-type)} \quad (1)$$

where E_x, E_y, E_z are components of electric fields along x, y, z axis, respectively. ρ is the density of charges, ε is the dielectric constant of the material, e is the element charge, N_d is the n-type doping density, N_a is the p-type doping density, and the latter equal sign only applies at $V_{gs}=V_{th}$.

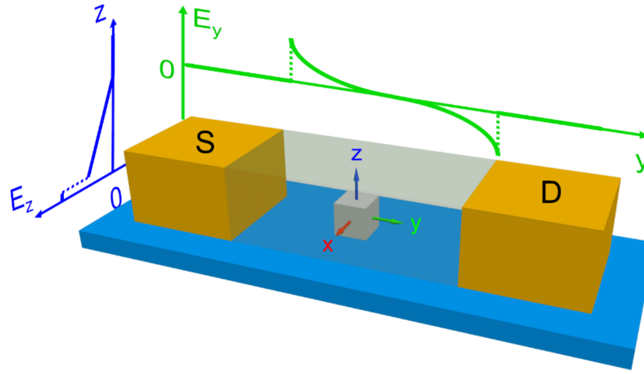

Figure 4.1 Competition among different electric fields for a unit volume in the channel. The unit volume is represented by the grey cube. The vertical component of the electric field, E_z, arises from the top and bottom gates; the lateral component, E_x, arises from the side gates; and the longitudinal component, E_y, from the source and drain contacts. The distributions of electric field components at $V_{gs}<V_{th}$ are shown in the coordinate besides the 3D model.

As shown in Figure 4.1, we assume that the gate control is exerted in the x and z directions (corresponding to the multi-gate devices). Note that in the depletion region near threshold voltage, $\frac{dE_y}{dy}, \frac{dE_x}{dx}, \frac{dE_z}{dz}$ and $\frac{\rho}{\varepsilon}$ always share the same sign (as shown in the field distribution in Figure 4.1) and $\frac{\rho}{\varepsilon}$ remains a constant, where variation of electric field in y direction arising from the drain could compete with gate control. Large drain bias or short channel length leads to a non-neglectable source/drain field penetration into channel material ($\frac{dE_y}{dy}$), impairing control from gate field ($\frac{dE_x}{dx}$ and $\frac{dE_z}{dz}$). As a result, the threshold voltage would have to shift to keep $\frac{\rho}{\varepsilon}$ constant. To stabilize threshold voltage, gate control must be amplified to diminish the field penetration from drain bias.

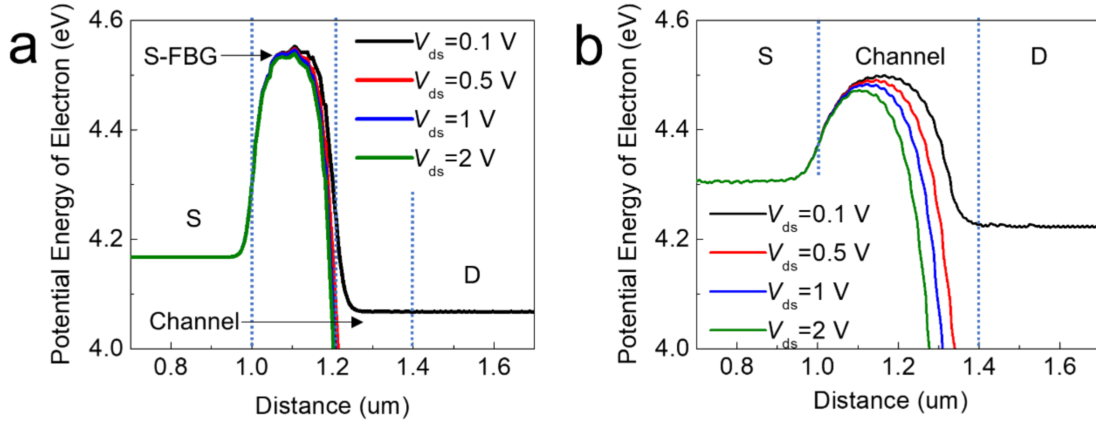

Figure 4.2 Simulation of electron potential energy in the channel region via Finite Element method. Energy potential of electrons at $V_{gs}=V_{th}$ in S-FBG transistor (a) and normal gate transistor (b). Channel materials is set to MoS_2. Material and thickness of FBG oxide is set to be Y_2O_3 and 5 nm, respectively.

Inspired from the analyses, we proposed a new gate structure, double feedback gates, to simultaneously suppress V_{th} roll-off and ambipolar transport. The structure of the double FBGs transistor is depicted in Figure 4.3a, where three split gates are used. G1 beneath the entire structure is the master gate to switch the multilayer TMDs channel. G2 and G3 near the drain and source are connected to the drain electrode and source electrode, respectively. These two gates are used as the feedback gate to suppress V_{th} roll-off and ambipolar transport, respectively. The double FBGs are not intentionally connected with external voltage supply, so we named them feedback gates. Simulation based on Poisson equation confirms that S-FBG could protect electrical potential of channel against distortion caused by large drain bias (as shown in Figure 4.2).

4.2 Experimental section

Device fabrication. Multilayer s-TMDs used in this work were mechanically exfoliated from commercial crystals onto a desired substrate (70 nm Si_3N_4 or 300 nm SiO_2). The device layout patterns were defined via electron-beam lithography (EBL) and all metal films were deposited

using electron-beam evaporation (EBE) with a standard lift-off process. The Y_2O_3 gate insulator was formed by directly depositing a thin film of yttrium followed by a thermal oxidation of 30 mins at 180 °C under ambient condition[26]. All electric measurements were carried out by probe station in vacuum using Agilent B2902A source/measure unit (SMU).

4.3 MoS_2 FBG transistors with suppressed threshold voltage roll-off

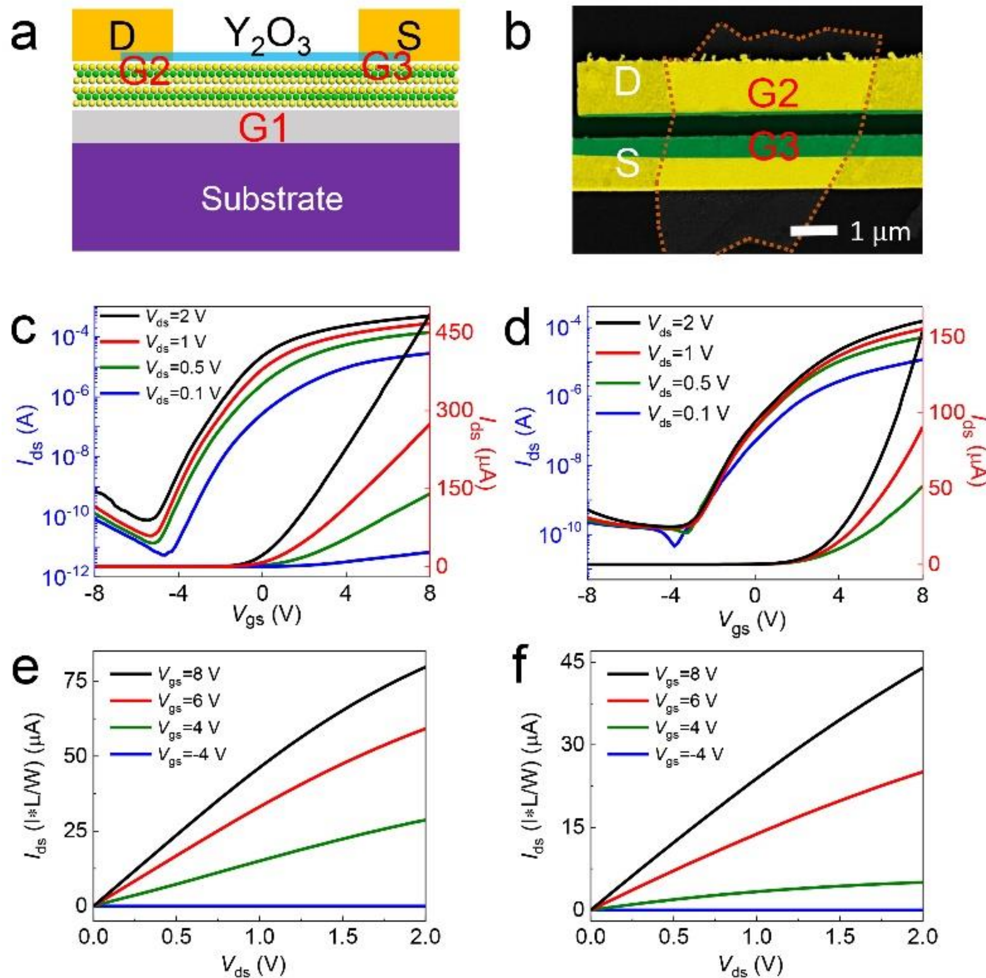

Figure 4.3 Device geometry and DC performance of multilayer MoS_2 transistor. Schematics of double feedback gate transistor (a). False-color SEM image of double feedback gate transistor. Transfer curves of the normal back gate transistor (c) and double feedback gate transistor (d). Normalized output curves of the normal back gate transistor (e) and double feedback gate transistor (f).

False-color scanning electron microscopic (SEM) image of an as-fabricated double FBG multilayer MoS_2 transistor is shown in Figure 4.3b, in which G3 is connected to the source electrode. The double FBG MoS_2 transistor is designed with S-D distance of 1 μm, G3 length is 500 nm and G2 length is 80 nm, respectively. As a comparison, we fabricated a normal multilayer MoS_2 transistor with similar thickness without FBGs (Figure 4.4). Typical transfer curves of the two types of transistors were measured under the same test condition with a series of V_{ds} of 0.1 V, 0.5 V, 1 V and 2 V. Adopting the well-developed fabrication process, the normal multilayer MoS_2 transistor exhibits a typical n-type behavior, with a large on-state current over 75 μA at V_{ds}=2 V and sharp on/off ratio larger than 10^6. However, with V_{ds} increasing from 0.1 V to 2 V, it is obvious to see the V_{th} of the normal transistor drifts to the negative direction severely, indicated as a V_{th} roll-off behavior, making it disqualified as a robust module in ICs. In contrast, the transfer characteristics of the FBGs transistor exhibit much better V_{th} control capability with nearly negligible V_{th} shift and high on-off ratio of 10^6 as well. The output characteristics of the two sets of transistors show typical Ohmic behavior, with a linear output at low bias condition and good saturation behavior at large bias (Figure 4.3e and 4.3f).

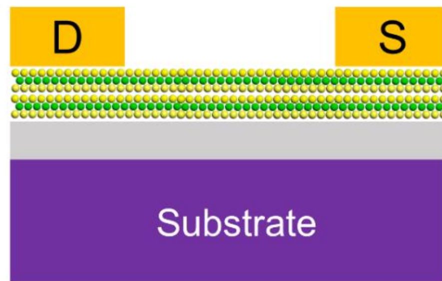

Figure 4.4 Schematics of the normal back gate multilayer MoS_2 transistor.

To demonstrate the effect of the FBGs structure quantitatively, V_{ds}-dependent V_{th} (V_{th} is extracted using typical linear extrapolation method) roll-off is plotted in Figure 4.5a for the two types of transistors shown in Figure 4.3c and 4.3d, in which the V_{th} roll-off is defined as[13]:

$$V_{th} \text{ roll-off} = V_{th} (\text{large } V_{ds}) - V_{th} (\text{small } V_{ds}) \quad (2)$$

With V_{ds} increasing, V_{th} roll-off increases rapidly in normal multilayer MoS_2 transistor, suggesting that the electric field penetration from the S/D gradually takes over the gate control capability. In contrast, since the electric potential near the source electrode is clamped, gate control over this channel region is protected from field penetration from S/D, leading to a nearly negligible V_{th} roll-off. Therefore, the V_{th} in the FBG multilayer MoS_2 transistor remains around 3.26 V with increasing V_{ds}.

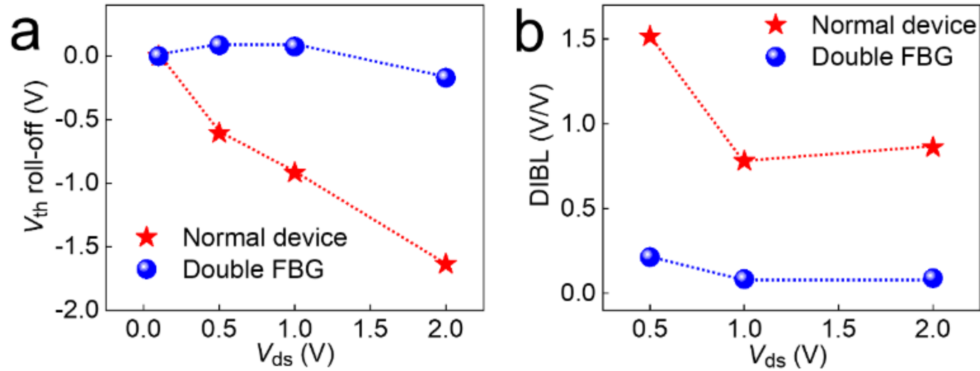

Figure 4.5 Comparison of threshold voltage roll-off (a) and DIBL (b) between the normal back gate transistor and double feedback gate transistor based on multilayer MoS_2.

DIBL is another important device parameter for characterizing transistors[25], and keeping low DIBL at large bias is necessary for designing a stable transistor. Thus, we further extracted the DIBL, which can be described using the equation:

$$\text{DIBL} = -\frac{V_{th}^{high} - V_{th}^{low}}{V_{ds}^{high} - V_{ds}^{low}} \quad (3)$$

where V_{th}^{high} is the threshold under a high voltage bias (V_{ds}^{high}), V_{th}^{low} is the threshold under a high voltage bias (V_{ds}^{low}). The average value of DIBL is larger than 1000 mV/V in the normal multilayer MoS_2 transistor, which may in a way severely degrade device stability and decline the robust characteristics of ICs (Figure 4.5b), in contrast, the DIBL in the FBGs transistor remained at a low value and could be suppressed down to 84 mV/V at V_{ds}=1 V.

It should be noted that the S-FBG could clamp the band structure near source end, thus preventing V_{th} drift resulting from other electrostatic fields as well. These fields are not limited to those effects arising from the drain bias, but could also be originated from charge trapping at interface, such as from adsorption/desorption of water and oxygen on MoS_2 surface[17] and from MoS_2/dielectric interface[27-28]. This could also help explain the superior suppression of threshold voltage roll-off in S-FBG MoS_2 transistors and the S-FBG could possibly be a robust technique to stabilize threshold against various external influences.

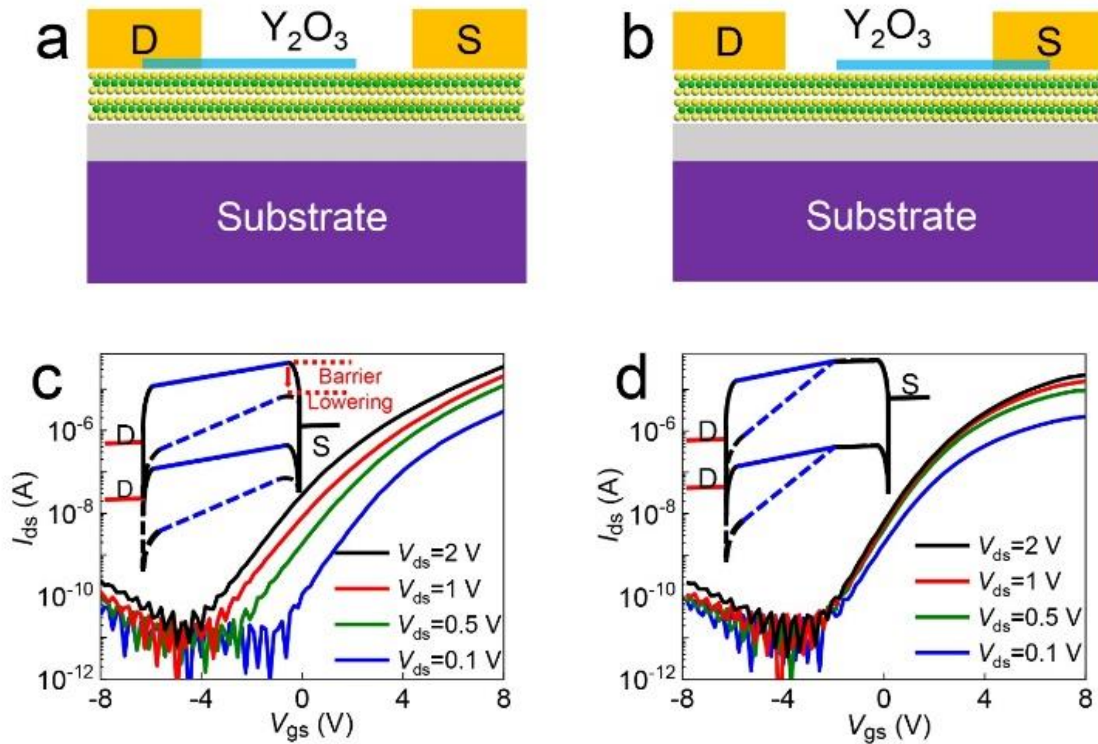

Figure 4.6 Mechanism exploration of the S-FBG multilayer MoS_2 transistor. Test configuration of the D-FBG transistor (a) and S-FBG transistor (b). Transfer characteristics of the D-FBG transistor (c) and S-FBG transistor (d). Insets of (c) and (d) are energy band diagram of the D-FBG transistor and S-FBG transistor under high voltage bias, respectively.

To further explore the switching mechanism of the FBGs transistors, we simplified the device structure to study the electric potential clamping effects at the source end. Explicitly, as shown in Figure 4.6a and 6b, we shortened the length of the yttrium oxide to enable only one contact overlapped with the yttrium oxide. Thus, we could simultaneously measure two sets of transfer characteristics with or without FBG at source end from the same device by switching source and drain configuration. Corresponding to the device configurations shown in Figures 3a and 3b, two sets of transfer characteristics were measured shown in Figure 4.6c and 6d, respectively. Owing to the field penetration from the drain with increasing V_{ds}, the multilayer MoS_2 transistors without FBG at the source end exhibits obvious V_{th} roll-off behavior with V_{th} shift of 3.22 V at V_{ds}=2 V (Figure 4.6c). This is typical for multilayer MoS_2 transistors with well scaled structure, suggesting that transistors built on multilayer MoS_2 with normal gate structure may not be suitable for large scale ICs. While for the same multilayer MoS_2 transistors with FBG at the source end, V_{th} shift behavior is significantly suppressed even at large bias of up to 2 V (Figure 4.6d), with V_{th} roll-off of less than 1.42 V even at a large V_{ds}=2 V. As shown in the band diagram (blue curves in the inset of Figure 4.6c), electrons need to step over the SB at source end to inject into the conducting channel via thermal excitation process to create current in on-state. However, the SB height becomes lower at large V_{ds}. Thus, the threshold potential for electrons from the source to overcome the barrier becomes smaller, thus making the V_{th} left shift. While in the S-FBG transistor, the energy band near the drain is maintained by the FBG that is connected to the source (inset of Figure 4.6d), and the height of the SB is controlled by the FBG and may be designed to significantly

suppress the barrier lowering even at large bias. These experiments further verify that the main act of the S-FBG is to clamp the energy band or maintain potential barrier near the source electrode to suppress V_{th} shift in on-state. In addition, the maximum on-state current is not influenced by introducing S-FBG, with on-state current nearly the same with that shown in Figure 4.6c.

4.4 WSe_2 FBG transistors with tailored unipolar transport

Ambipolar behavior emerges in multilayer TMDs as a trade-off of higher current density compared to monolayers, especially in multilayer WSe_2 based transistors[1, 29]. Explicitly, most high performance 2D materials based transistors are fabricated through a contact metal engineering process[8, 30-32], which may be regarded as Schottky barrier (SB) transistors with a SB height of around E_g is formed at the channel/contact interface in off-state to prevent carriers injection[33]. On scaling down transistors, the gate insulator has to be scaled thinner to maintain excellent electrostatic control over the channel. As a result, the SB in off-state also becomes thinner, leading to more leakage current that increases exponentially with the bias voltage between source and drain. This trend will become more obvious with further scaling down the channel length, and the ambipolar transport will severely degrade the stability and increase the dynamic power consumption in future large-scale ICs[34].

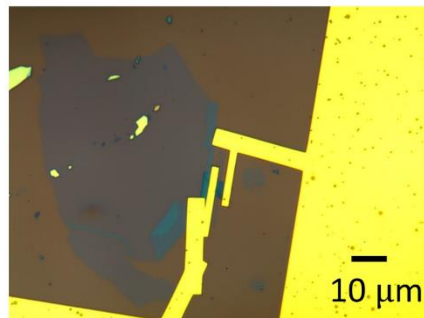

Figure 4.7 Optical image of the D-FBG multilayer WSe_2 transistor.

Next, we'll discuss the suppression of ambipolar transport in the device configuration with FBG at the drain end. We constructed the D-FBG device structure just by changing the conducting channel into multilayer WSe_2, which generally exhibited ambipolar transport behavior. The optical image of D-FBG WSe_2 transistor in Figure 4.7 is designed with S-D distance of 2 μm and G2 length is 600 nm, respectively. In contrast, we fabricated a normal multilayer WSe_2 transistor with similar thickness. Typical transfer curves of the two types of transistors were measured under the same test condition. By using the well-developed fabrication process, the normal multilayer WSe_2 transistor exhibits a typical ambipolar behavior (Figure 4.8g, 4.8j), with on/off ratio at $V_{gs}=\pm 60$ V less than 10 at $V_{ds}=\pm 1$ V. It can also be found that the normal transistor exhibits the ambipolar transport regardless of the polarity of the V_{ds}, making it undesirable for low-power applications in integrated circuits. As a comparison, the transfer characteristics of the D-FBGs transistor exhibit unipolar transfer curves with on/off ratio at $V_{gs}=\pm 60$ V larger than 10^3 even at large $V_{ds}=\pm 2$ V. In addition, the transport can be easily tailored either into n-type or p-type (Figure 4.8a and 4.8d), which depends on the voltage bias supply. The on-state current of the S-FBG transistor is a little bit smaller than that of the normal transistor, which may be attributed to the threshold voltage shift towards normally-off state.

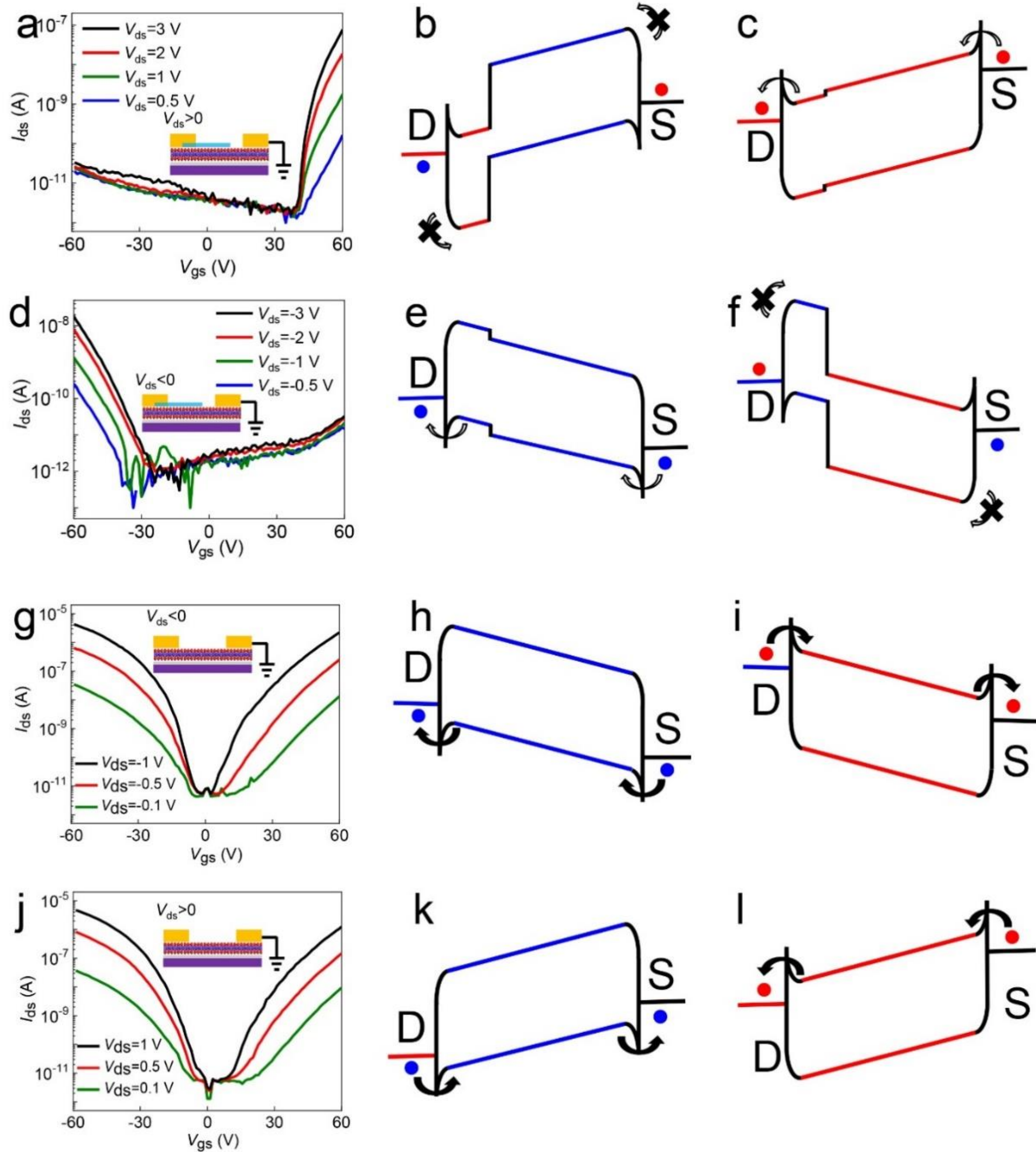

Figure 4.8 Transfer characteristics and operating mechanism of the multilayer WSe_2 D-FBG transistor. (a) Unipolar n-type transfer curves. Energy band diagram in off-state (b) and on-state (c). (d) Unipolar p-type transfer curves. Energy band diagram in off-state (e) and on-state (f). Characteristics and energy band diagram of the normal back gate multilayer WSe_2 transistor. Transfer curves of the normal back gate multilayer WSe_2 transistor under negative V_{ds} (g) and positive V_{ds} (j). Energy band diagrams under $V_{ds}<0$ and $V_{gs}<0$ (h) $V_{ds}<0$ and $V_{gs}>0$ (i) $V_{ds}>0$ and $V_{gs}<0$ (k) $V_{ds}>0$ and $V_{gs}>0$ (l). The channel length and width of the normal WSe_2 transistor is 1.8 μm and 5 μm, respectively.

To clearly demonstrate the mechanism, we depicted the band diagram under negative V_{gs} and positive V_{gs}, respectively. Explicitly, the transfer characteristics behaves as unipolar n-type transition (Figure 4.8a) under positive V_{ds} condition. In off-state with negative V_{gs}, there exists an extra SB adjacent to the drain electrode due to the FBG, which will block the thermal injection of holes into the channel at large bias and gate voltage. Simultaneously, the SB height for electrons is sufficiently large to suppress the electron injection, resulting in no detectable current in the channel (Figure 4.8b). While in on-state, the energy band bending (Figure 4.8c) due to the FBG near the drain would not affect the flowing of electrons, enabling on-state current flow from the source to the drain. Similarly, when introducing negative V_{ds} and positive V_{gs} (Figure 4.8f), electrons are blocked by the wide SB of the multilayer WSe_2 channel beneath the FBG gate, and holes are blocked by the SB near the source electrode, leading to an off-state when $V_{gs}>0$ V. However, the SB near the source becomes very thin at negative V_{ds} and V_{gs} as shown in Figure 4.8e. Holes from the source can thus tunnel through the SB easily leading to large on-state current. As a comparison, in normal WSe_2 transistor without FBG, electrons and holes can tunnel through the thin SB at positive and negative gate voltage, respectively, creating ambipolar transfer curve. These can be reflected in the band diagram shown in Figure 4.8h, 4.8i, 4.8k, 4.8l. Freely tailoring the ambipolar transport into unipolar behavior in a simple FBG structure provides a unique way to construct low-power consumption integrated circuits.

Last but not the least, while we only discussed multilayer TMDs based transistors here, the double FBG structure may be readily used in devices based on other material system with similar problems, such as narrow bandgap InAs system[35], Ge nanowire with high carrier mobility for building high-speed transistors[36], where V_{th} roll-off and ambipolar behavior originated from the small bandgap are highly undesirable for applications in future ICs. In principle, the double FBG

structure discussed here may be in a way to resolve these problems with suppressed V_{th} roll-off and well-tailored unipolar behavior.

4.5 Conclusion

In summary, we have developed a double FBG structure to suppress V_{th} roll-off and ambipolar transport in multilayer TMDs transistors while maintaining their high-performance in on-state. For a S-FBG transistor, the width of the potential barrier near the source is largely fixed by the FBG, which significantly suppresses the undesired barrier lowering near the source and thus V_{th} shift. In terms of a D-FBG transistor, the width of the potential barrier near the drain is easily tuned by the drain bias, which enables us easily to tailor the undesired ambipolar transport into a V_{ds} dependent unipolar behavior. The S-FBG multilayer MoS_2 transistors present nearly negligible V_{th} roll-off and low DIBL value of 84 mV/V even at large source-drain bias of 2 V at room temperature. The D-FBG structured multilayer WSe_2 FETs are demonstrated to be promising to be used in low-static-power logic ICs by virtue of its unipolar transport. The double FBG structure may in principle be used for building transistors based on other semiconductors to suppress V_{th} roll-off and ambipolar transport.

4.6 References

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Chapter 5. A One-Step Plug-and-Probe Approach for Probing Delicate Semiconductor Materials via van der Waals Integration

5.1 Introduction

The miniaturization of silicon-based electronics, following the well-known Moore's law, has powered the information technology revolution over the past half century [1], but is facing increasing challenges for the continued scaling due to fundamental materials limit (e.g., severe mobility degradation in sub-5 nm regime) [2-5]. Alternative to the continued miniaturization of digital devices, also known as the strategy of "more Moore", the International Roadmap for Devices and Systems (IRDS) is shifting attention to "more than Moore" and "beyond Moore" strategy, with function diversifications including integration of analog devices, power electronics, sensors, optoelectronic functions, and biochips to satisfy the needs of specific application domains including the rapidly-developing Internet of Things (IoT) and artificial intelligence (AI) [6]. To achieve such function diversification requires a variety of figure of merits beyond the reach of todays' silicon electronics and has motivated considerable efforts in exploring a new generation of electronic materials, such as 2D layered crystals [7-8] and lead halide perovskites (LHPs) [9-10]. The atomically thin 2D semiconductors with few surface dangling bonds can preserve their superior mobility at single-atom thickness, which could overcome the miniaturization limit of silicon electronic for their better immunity to short channel effects and negligible mobility degradation down to single atom thickness [11]. They are also competitive candidates for flexible electronics [12]. The halide perovskites have shown considerable potential for photovoltaic cells [13] or light-emitting devices, and are also intriguing for spintronic device for their exceptionally large spin-orbital coupling effect [14]. To capture the intrinsic merits of these emerging electronic materials for high-performance devices

requires a close integration of with critical device components such as electrical contacts and dielectric layers with optimum interfaces, which are non-trivial challenges.

Conventional electronics manufacturing approaches, including lithography, vacuum deposition, and plasma etching processes, have frequently been applied for creating proof-of-concept devices from these emerging materials for fundamental studies and performance evaluations. These processes, although well-developed and suited for conventional Si electronics, usually involve aggressive chemical processing and often induce undesired structural disorder into emerging electronic materials, seriously degrading their electronic properties. In particular, most emerging electronic materials feature atomic- or molecular-scale dimensions, and are too delicate to maintain their intrinsic properties in the harsh materials integration and device fabrication steps; they are thus difficult to integrate with traditional contact and dielectric materials to form functional devices with uncompromised performances due to processing incompatibilities. Despite many exciting prospects and proof-of-concept demonstrations, probing the fundamental limits and capturing the intrinsic merits of these emerging electronic materials in functional devices face considerable fundamental challenges from materials science and engineering, particularly in the design and control of interfaces that are critical for advanced manufacturing.

To capture the intrinsic merits of the emerging materials in functional devices, it is essential to retain the pristine contact and dielectric interface with minimum interfacial trapping states. For example, the fabrication of high-quality gate dielectric is crucial for efficient electrostatic control of charge carriers in semiconductors, and it has been a persistent challenge to integrate high-quality dielectrics on 2D materials. With a dangling-bond-free surface [15], the 2D materials is fundamentally incompatible the atomic layer deposition (ALD) [16] process that relies on chemically active sites on material surface for uniform precursor chemsorption and oxide nucleation. Forcing

dielectric deposition on 2D materials using ALD or other physical vapor deposition (PVD) approaches requires carefully engineering the interfacial seeding layer [17-18] and often results in non-uniform oxide profile [19] and/or defective dielectric/2D interfaces [20] that seriously limits the achievable performance. The integration of dielectrics on LHPs is even more challenging [21] since most LHPs rapidly degrade upon in contact with any chemically active species such as water and most organic solvents. As a result, it has been standing challenge to integrate high-quality gate dielectric on LHPs for sufficient gate control to enable room-temperature field effect transistors [22]. Similar challenges exist in contact integration on these delicate emerging materials since conventional high-energy metal deposition process can easily degrade the interfacial atomic structure.

The van der Waals (vdW) integration approach, in which prefabricated material/device components are physically laminated on the delicate electronic material at or near room temperature, offers a low-energy approach for damage-free integration of highly distinct materials beyond the limits of processing compatibility requirements. The weak vdW interactions largely preserves the pristine atomic structure and intrinsic electronic properties of the constituent materials after integration. It can thus enable a new generation of artificial heterojunctions with deterministic control of atomically clean and electronically sharp interfaces by design, unlocking previously inaccessible physical limits and enabling devices with superior performance and unprecedented functions. The vdW integration approach has been separately employed for dielectric [23-24] or contact [25-26] integration on 2D materials and more recently on LHPs [27]. However, simultaneous vdW integration of both the contacts and gate electrodes has not been possible to date, intermediate lithography step is often needed to complete the device fabrication, which could compromise either the dielectric or contact interface, and thus the overall device performance. A

one-step vdW integration of both the contact and the entire gate stack on delicate materials enable complete device fabrication without any lithography process. It could thus avoid any lithography/deposition induced degradation, which is crucial to achieve ideal electronic devices with both the high-quality contact interface and dielectric interface to fully exploit the potential of the emerging semiconductors. Compared to the relatively mature vdW metal contact technique [25, 28] with vast metal variety, the vdW integration of dielectric are still largely limited to low-k 2D or quasi-2D insulator [29]. The vdW integration of high-k dielectric is usμAlly difficult due to the strong adhesion between oxide and sacrificial substrate [30], not to mention further integration of more complicated device structures.

Here we report a general "plug-and-probe" approach for simultaneous vdW integration of both the contact and high-k dielectric gate stack on delicate emerging electronic materials through a 'one-step' transfer/lamination process. This approach allows to separate the high-energy fabrications of high-quality contacts/dielectrics from low-energy device integrations process, enabling damage-free integration of the prefabricated contacts and high-k dielectrics on virtually any emerging materials systems with pristine interfaces for conveniently and accurately probing these emerging electronic materials with minimum extrinsic interfacial scattering. By this approach, we have achieved a nearly ideal subthreshold swing (SS) of 60 mV/dec in top-gate transistors based on 2D transition metal dichalcogenides (TMDs) with a transferred high-k Y_2O_3 gate oxide (comparison in Table 5.1). Besides 2D materials, we apply this approach to more delicate LHP thin films and achieve the first top-gate room temperature $CsPbBr_3$ transistors with low operation voltage and the best 2-terminal field-effect mobility reported (32 cm^2/Vs) (Table 5.2). We further show that this approach could also be extended to a large-scale integration to

centimetre-scale CVD TMDs and CVD grown halide perovskite thin films with respectable electronic performance.

Table 5.1 Performance comparison of TMDC top-gate transistors

Material	Dielectric	SS (mV/dec)	I (μA/μm) @ SS=80	I_{on}@V_{ds}=1 V (μA/μm)	L_{tg} (μm)	EOT (μm)	Equivalent *k*	Ref
Exfoliated MoS_2	30 nm ALD HfO_2	74	10^{-4}	4	0.5	N/A	N/A	[31]
Exfoliated MoS_2	1 nm AlN/ 5 nm AlO_x	120	-	1	1	N/A	N/A	[32]
Exfoliated MoS_2	9 nm HfO_2/5 nm Y_2O_3 (buffer layer)	65	5×10^{-4}	40	3	4.42	12.7	[33]
Exfoliated MoS_2	1.5 nm HfO_2/PTCDA (buffer layer)	60	10^{-3}	18	4	1	6	[18]
Exfoliated MoS_2	19 nm BN	78	10^{-5}	4	2.5	11	6.8	[34]
Exfoliated MoS_2	Transferred 13 nm Al_2O_3	120	-	100	0.116	N/A	N/A	[30]
Exfoliated MoS_2	Transferred 20 nm Y_2O_3 (Backgate)	60 (70)	10^{-3} (5×10^{-3})	0.8 (13)	1	4.2	17.5	This work
CVD MoS_2	6 nm HfO_2/PTCDA (buffer layer)	Average 160	-	Best 0.02	50	2	12	[18]
CVD MoS_2	2.5 nm CaF_2	Best 90 Average 160	-	Best 4	0.6	1	10	[24]
CVD MoS_2	Transferred 20 nm Y_2O_3 with backgate	Best 70 Average 90	Best 5×10^{-5}	Best 0.16	50	~4.2	~17	This work
Exfoliated WSe_2	2.8 nm HfO_2/PTCDA (buffer layer)	67	10^{-5}	0.3	Long Channel	1.3	8.5	[18]

Exfoliated WSe_2	30 nm Transferred BN	64	10^{-3}	10	0.8	23	5	35
Exfoliated WSe_2	Transferred 20 nm Y_2O_3	77	10^{-3}	1.5	5	4.5	17	This work

Table 5.2 Performance comparison of halide perovskite transistors

Material	**Device configuration (Contact and Gate)**	**Current µA (V_g, Temperature)**	**L/W (um)**	**V_{ds}**	**Sheet conductivity (µS)**	**Mobility**	**ON/OFF**	**Ref.**
Epitaxial $CsPbBr_3$	Au BC, Y_2O_3 TG	7 (-2, rt)	100/100	-1	7	32	10^4	This work
Solution $CsPbBr_3$	Au BC, SiO_2 BG	0.2 (-50, rt)	10/10000	-50	4×10^{-6}	10^{-5}	10^3	36
Epitaxial $CsPbBr_3$	ITO BC, PMMA TG	0.02 (-20, rt)	5/5	-3	0.0067	0.89	10^4	37
Epitaxial $CsPbBr_3$	Au BC, SiO_2 BG	0.3 (-60, rt) 0.3 (-60, lt)	20/100	-8	0.0075 0.0075	0.32 1.04	10^4 10^4	38
Epitaxial $CsPbBr_3$	Au TC, SiO_2 BG	2 (-60, rt)	50/100	-40	0.025	0.34	10^3	39
Solution $CsPbBr_3$	Ag BC, SiO_2 BG	1 (-60, 150K)	20/10	-20	0.1	2.3	10^5	40
Solution $MAPbI_3$	Au BC, Cytop TG	500 (60, rt)	20/1000	60	0.017	4.2	10^4	41
Solution $MAPbBr_3$	Au BC, SiO_2 BG	e: 1000 (60, 80K) p: 200 (-60, 80K)	20/1000 10/1000	60 -60	0.33 0.033	10.6 15-20	10^5~10^6	42
Solution Au/RbCsFAMA PbI_3/Au	Au BC, Cytop BG	30 (60, rt)	100/1000	60	0.05	1.2	10^3~10^4	43
Solution $FAMAPbBr_3$	Au BC, Cytop TG	0.8 (-60, rt)	100/1000	-60	0.0013	0.02	10^4	43
Solution $MAPbI_3$	Ti TC, AlO_x BG	80 (-2, rt)	90/1400	-2	2.6	18.8-23.2 18.8±4.4	10^4	44
Solution $MAPbI_{3-x}Cl_x$	Au TC, SiO_2 BG	p: 150 (-40, rt) e: 10 (40, rt)	50/400 30/100	-40 40	0.47 0.075	10±2.5 10±3.4	~10^2 ~500	45
Epitaxial $MAPbBr_3$	Au BC, SiO_2 BG	1 (-40, rt)	50/240	-30	0.0069	3.1	10^5	46
Epitaxial $MAPbI_3$	Au BC, Cytop TG	15 (60, rt)	10/1000	60	0.0025	0.1-0.5	10^4	47
$Cs_x(MA_{0.17}FA_{0.83})_{1-x}Pb(Br_{0.17}I_{0.83})_3$	Au BC, SiO_2 BG	p: 10 (0, rt) n: 10 (120, rt)	20/1000 20/1000	-100 100	0.002 0.002	2.1 2.5	10^3	48
Solution $PEASnI_4$	Au TC, Cytop TG	400 (-50,rt)	95/2000	-50	0.38	15	10^4~10^5	49
Solution $MAPbI_3$	Au TC, SiO_2 BG	p: 80 (-40, rt) n: 10 (40, rt)	50/1000 50/1000	-30 30	0.13 0.017	1.24 1.01	10^3~10^4	50

Solution $MAPbI_3$	Ni TC, SiO_2 BG	p: 10 (-100, 78K) n: 50 (100, 78K)	80/20000 80/20000	-100 100	0.0004 0.002	0.002 0.007	10^2~10^3	51
Solution $PEASnI_4$	Au TC, SiO_2 BG	7.5 (-50, rt)	28/1000	-60	0.0035	0.6	10^4	52
Solution $(TT)_2SnI_4$	Au TC, SiO_2 BG	5000 (-60, rt)	80/6240	-60	1.068	9.35	10^4	53
Solution $FASnI_3$	Au BC, SiO_2 BG	3000 (-80, rt)	20/10000	-20	0.3	0.21	10~10^2	54

5.2 Experimental section

Material preparation. The few-layer MoS_2 and WSe_2 are exfoliated/dropped off on 300 nm SiO_2/p^{++} Si substrate with prepatterned electrode pads for probing. The CVD MoS_2 grown on sapphire is transferred onto 300 nm SiO_2/p^{++} Si via standard wet transfer process and patterned into arrays with alignment marker by CF_4/O_2 plasma and photoresist mask. The single crystal $CsPbBr_3$ array is prepared by epitaxial vapor epitaxial growth on mica in a home-built CVD furnace and patterned by 1:1 IPA/DMF and PMMA mask.

Device fabrication. Two methods are used to prepare graphene on SiO_2/p^{++} Si sacrificial substrate: (1) Few-layer graphenes are mechanically exfoliated on substrate; (2) CVD graphene grown on Cu foil transferred onto substrate by PMMA via standard wet transfer. The graphene is pre-annealed at 250 ^oC for 5 min to release the stress on SiO_2. Ebeam lithography (EBL)/photolithography are used to define small gate pattern/gate array, respectively, then 10-20 nm Y is deposited via ebeam evaporator at 10^{-5} mbar with rate of 0.3 Å/s. The Y is partially oxidized after evaporation, and is further annealed in air at 200 ^oC for 3h before depositing 20/30 nm Ti/Au layer (60/20 nm for perovskite devices) on top of it as top electrodes. The gold source/drain gate pad is then defined by EBL/photolithography to complete fabricating the device architecture.

To fabricate the devices, the whole substrate is treated with saturated HMDS vapor at 120 ^oC for 15 min before spincoating with 2 um PMMA. The PMMA encapsulated structures are peeled off with tape frame/thermal release tape and flip over onto PDMS stamp. The backside of device architecture is treated with 25 W oxygen plasma with 15 sccm O_2 for 5 min. The top-gate and source/drain are transferred onto target materials with a home-made transfer stage and annealed at 150 ^oC for 5 min for glass transition of PMMA. An optional EBL step is used to open window on electrode for probing if no pre-patterned electrode pad is presented.

Material characterization. The roughness of backside of Y_2O_3 is characterized on flipped film embedded in PMMA by Bruker Dimension FastScan Scanning Probe Microscope. The interface is characterized by Nova 600 SEM/FIB system and FEI Titan TEM.

Device characterization. The electric characterization of transistors is performed in vacuumed probestation (Lakeshore TTPX) with Agilent B2902A source/measure unit. During measurements, a 120 $\mu W/cm^2$ white light is illuminate through the thin Au S/D contact to minimize contact resistance while the light is blocked by the thick Ti/Au on gated region to maintain the channel region undoped.

Device parameter extraction. EOT is estimated by threshold voltage drift of top-gate transistor by applying various backgate voltage on 315 nm SiO_2. Hysteresis is derived by subtracting threshold voltages of forward and backward scan of transfer curve.

5.3 Transfer whole device structure via graphene sacrificial layer

To obtain a high-quality contact and high-k dielectric that can easily detach from the sacrificial substrate, we used single-layer graphene as a sacrificial interlayer to reduce the adhesion force of device structures with the underlying silicon substrate (Figure 5.1a). We adopted Y_2O_3 as gate

dielectric for its high dielectric constant of 17-20[55], high crystalline stability, high mechanical strength and simple fabrication by oxidizing deposited yttrium metal film to form dense oxide [56]. First, an yttrium thin film is deposited on top of graphene and annealed in air for oxygen diffusion into film and stress relaxation. Then, after defining the source/drain contacts and top gate electrodes, the whole device architecture is peeled off assisted by polymethyl methacrylate PMMA and graphene is removed by a brief oxygen plasma etching process. The formation of Y_2O_3 can be confirmed by XPS and EDS (Figure 5.3 and Figure 5.4). The peeled-off film with complete gate-stack and source drain electrodes (Figure 5.1b) is then aligned and transferred on to target semiconductors (Figure 5.1c). The backsides of contacts and dielectric replicated the atomically flat surface of graphene/polished SiO_2/Si wafer (Figure 5.1d), thus are able to provide a seamless interface between materials and device architectures to activate vdW interaction. Indeed, the cross-sectional TEM studies demonstrates that vdW-integrated interface exhibits an atomically sharp interface with no apparent disorder between Y_2O_3 and MoS_2 (Figure 5.1e and figure 5.2) compared to the messy interface of ALD Al_2O_3 and MoS_2 full of defects and difussions, which is essential for ensuring high-quality dielectric interface with minimum interface trapping states to achieve nearly ideal device performance. Similarly, the vdW-integrated contact interface also shows atomically clean vdW interface (Figure 5.1f) which is essential for eliminating interfacial trapping states and Fermi level pinning effect.

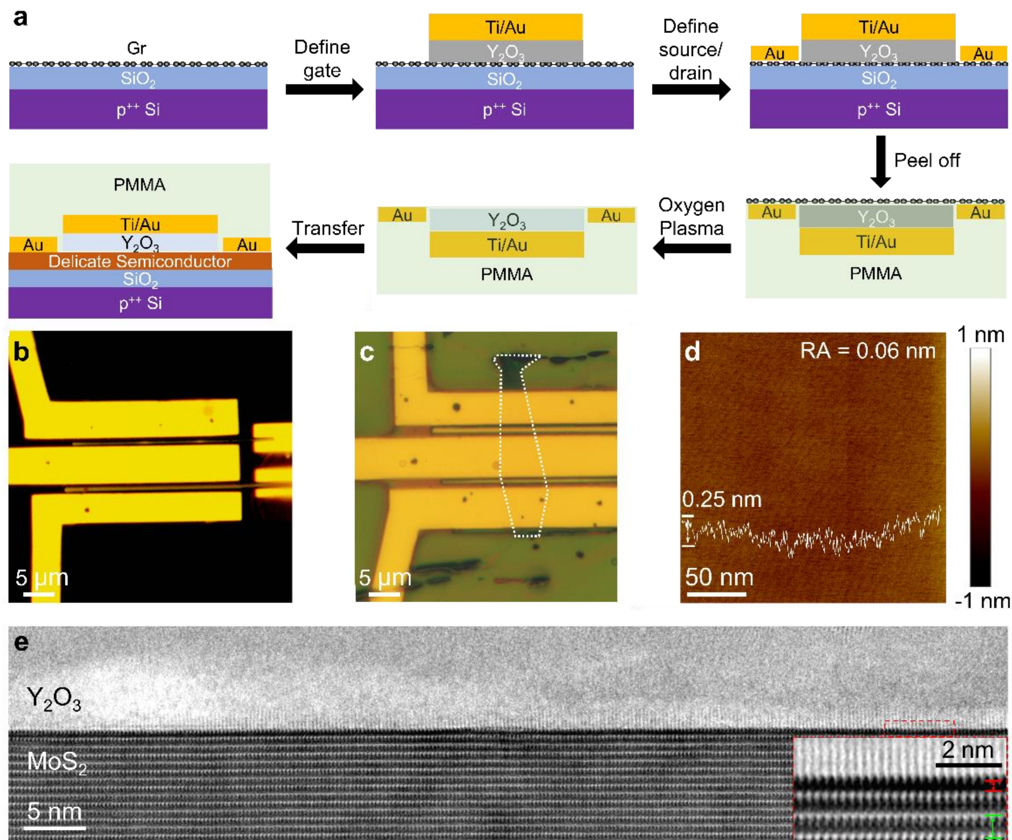

Figure 5.1 The vdW plug-and-probe approach enabled by transfer of metal contact and Y_2O_3 gate dielectric. (a) Schematic of the plug-and-probe process. (b) Optical microscopic image of peeled-off source/drain/gate stack on PMMA. (c) Generated device after transfer the whole device architecture on top of a few-layer WSe_2. (d) AFM map of the backside of peeled off Y_2O_3. The surface roughness is 0.06 nm. (e) High-resolution cross-section TEM image of transferred Y_2O_3/MoS_2 interface with a clean vdW gap. Inset is the TEM image with higher resolution. The red arrow reveals the vdW gap is about 0.3 nm and the green arrow reveals the layer distance of MoS_2 is about 0.65 nm.

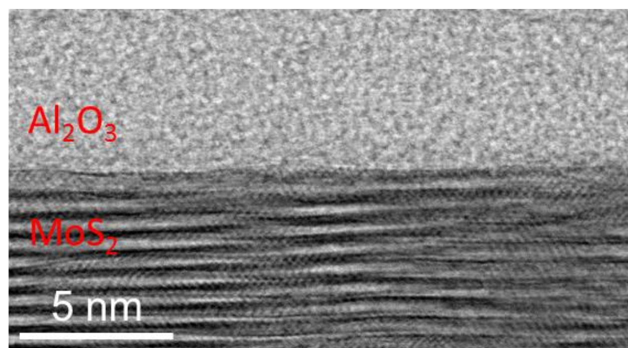

Figure 5.2 Cross-sectional TEM image of the Al_2O_3/MoS_2 interface. The Al_2O_3 is grown by ALD method at 150 °C with trimethylaluminum (TMA) and water precursors.

It should be noted that besides Y_2O_3, this graphene sacrificial substrate could be used to peel off any metal or dielectric that has strong adhesion to SiO_2 substrate. We have peeled off large scale Y_2O_3, Ti, Ni and Cr with 70%-100% yield (Figure 5.5a). These metals can serve as prominent n-type contact to 2D materials (Figure 5.5b, 5.5c), potentially some other options besides Au contact for further development of this plug-and-probe techniques.

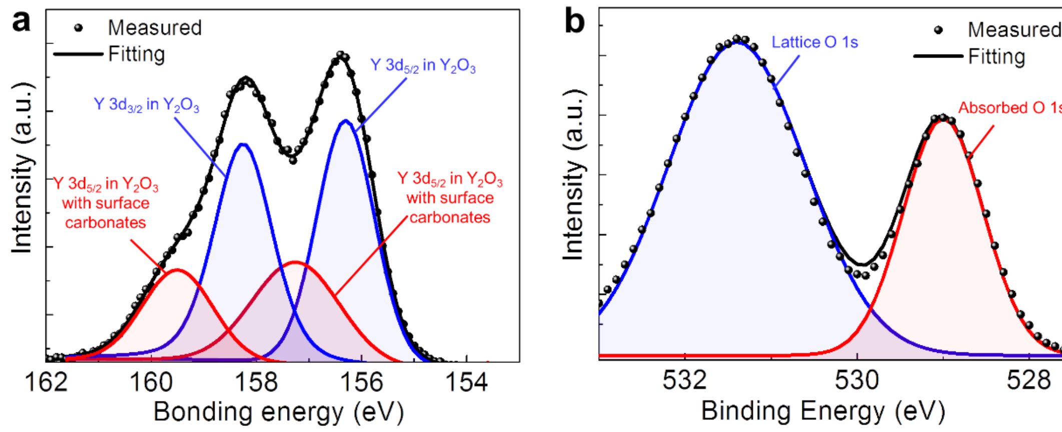

Figure 5.3 XPS of the Y_2O_3 film. Peak fitting of (a) Y 3d signal. (b) O 1s signal.

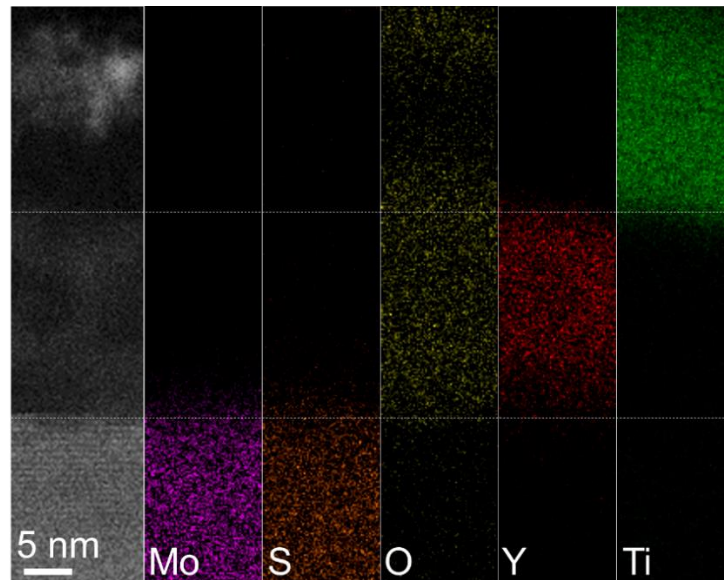

Figure 5.4 TEM image and EDS maps of various elements of the transferred Au/Ti/Y_2O_3/MoS_2 interface.

In this way, the entire device stack (including source-drain contacts, the entire gate stack or other components) can be fabricated on a mother wafer, peeled off and directly transferred onto the target material in one-step lamination process to obtain the complete device with pristine contact and dielectric interface, much more convenient than conventional lithography and deposition to fabricate devices. Without lithography or high-energy deposition, this approach defines an efficient plug-and-probe process for rapid and reliable evaluation of emerging materials with minimum complications from fabrication-induced extrinsic defects or trapping states.

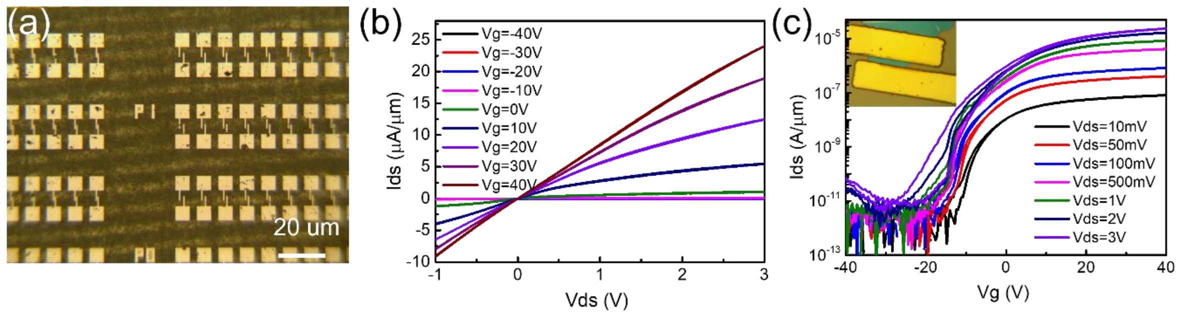

Figure 5.5 Transfer Ti as an n-type contact by graphene sacrificial layer. (a) Peeled-off array of Ti/Au electrodes. (b,c) Output and transfer curves of MoS_2 backgate devices with vdW Ti contact.

5.4 Performance evaluation of the 2D transistors by vdW plug-and-probe

The achievement of atomically clean dielectric interfaces is essential for electrostatic tailoring the charge concentration in semiconductor channels. Electrical transport measurements of MoS_2 transistors with the vdW-integrated top-gate with Y_2O_3 gate stack show excellent gate tunability (Figure 5.6a) with negligible leakage current and steep switching at subthreshold region. In general, the efficiency of gate switch in a typical MOSFET can be characterized by the subthreshold swing (SS), which is highly dependent on the interfacial state density at dielectric/semiconductor interface [4]:

$$SS = \frac{k_B T}{q}\left(1 + \frac{C_{dep}+C_{it}}{C_{ox}}\right) \approx 60 \text{ mV/dec} \times (1 + \frac{qD_{it}}{C_{ox}}) \quad (1)$$

Where D_{it} is interfacial state density, C_{ox} is capacitance density of gate dielectric, C_{dep} is depletion layer capacitance and is considered as zero at subthreshold region due to full depletion of the atomically thin channel. Thus, SS can reach a lower limit of 60 mV/dec at room temperature if interfacial density is zero. Significantly, our analysis shows that such an ideal limit 60 mV/dec is achieved in the MoS_2 transistor with transferred top gate (Figure 5.6b). The ideal SS of the MoS_2 of the fabricated devices indicates very few interfacial states and electronically clean interface, which can be attributed to defect-free vdW dielectric interface. We note that SS achieved in our device with vdW-integrated Y_2O_3 dielectric is also notably lower than the ALD grown Al_2O_3 [57], HfO_2 [31] and evaporated oxidized yttrium gate (Figure S4), where damages and defects are inevitably introduced to interface during the intense chemical or physical processes (Figure 5.7). Additionally, our measurements of the MoS_2 transistors with transfer gate shows essentially negligible hysteresis in gate sweep, further indicating high dielectric quality with negligible trapped charge densities (Figure 5.6c).

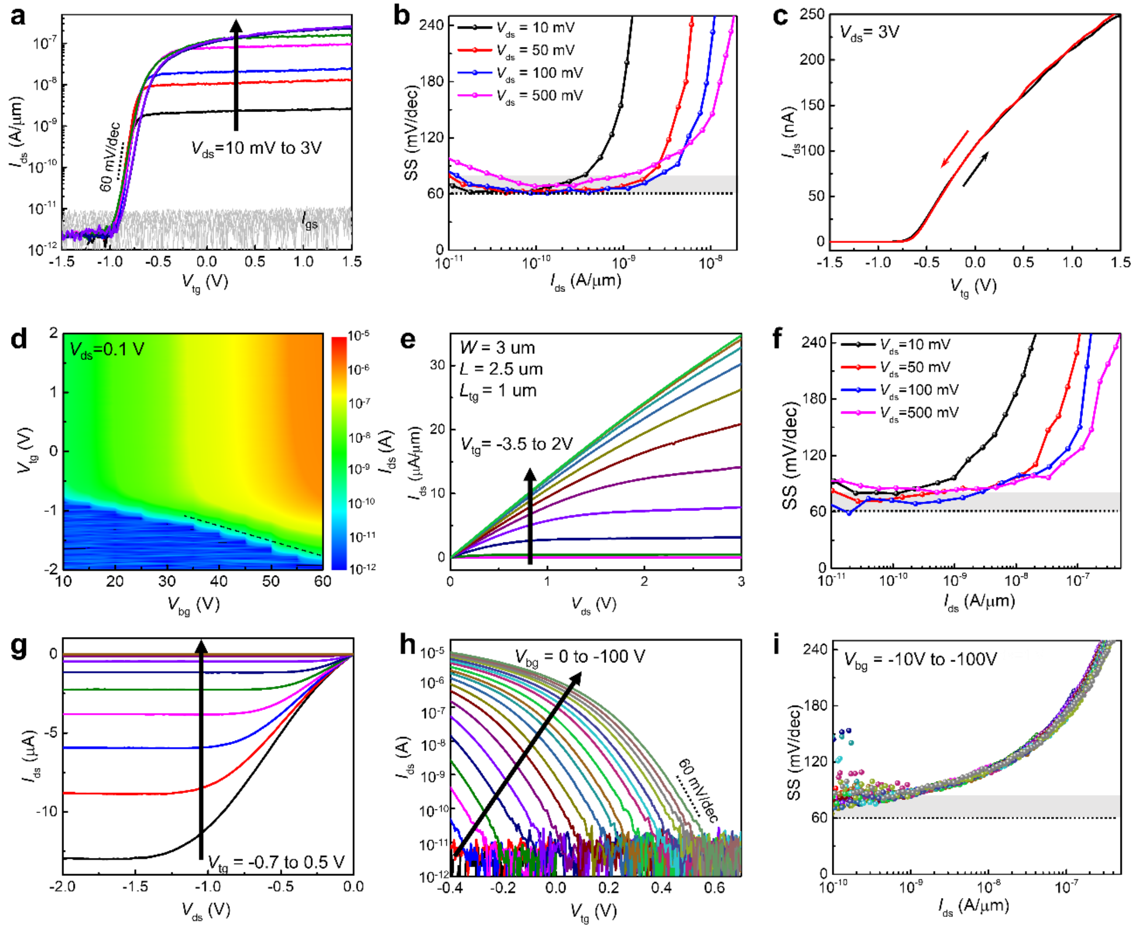

Figure 5.6 Performance of TMD transistors with transferred device architectures. (a) Transfer curves of a vdW-integrated MoS_2 top-gate transistor. (b) Extracted SS at different current densities of the MoS_2 transistor. The minimum SS is 60 mV/dec. (c) Forward and backward transfer curve scan of the device at various drain voltages. (d) Double gate mapping of current of the MoS_2 transistor. (e) The output curves of the MoS_2 transistor under 60V backgate voltage. (f) Extracted SS at different current density when applying 60V backgate voltage on the MoS_2 transistor. (g) Output curves of a WSe_2 transistor with transferred source/drain and gate stacks. (h) Transfer curves of the WSe_2 transistor at various backgate voltages. Drain voltage is -0.5V. (i) Extracted SS of the WSe_2 transistor under various backgate voltages. Drain voltage is -0.5V.

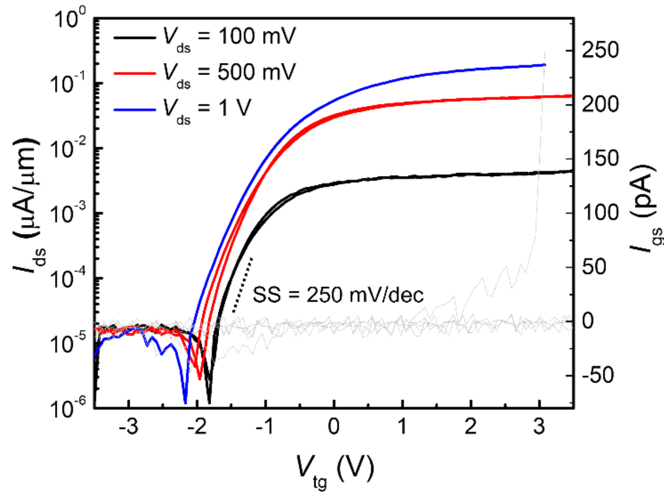

Figure 5.7 Transfer curves of a MoS_2 transistor with 5 nm evaporated and then oxidized Y as top gate. The SS is 250 mV/dec.

To further evaluate the quality of the Y_2O_3 dielectric, we perform a double gate scan of corresponding device with a SiO_2 back gate (Figure 5.6d). The increasing of backgate voltage results in a negative shift in the threshold voltage of top-gate transfer curve, which indicates a competition of n-doping control between the top-gate and back-gate. By evaluating the linear relationship of top-gate threshold voltage versus backgate voltage, we can derive the effective oxide thickness (EOT) and equivalent dielectric constant to be 4.2 nm and 17.5, respectively, which is consistent with C-V studies (Figure 5.8) further highlighting the high quality of pre-deposited Y_2O_3.

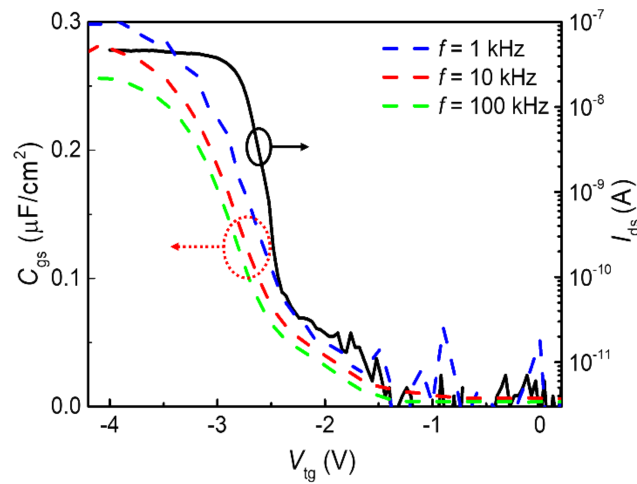

Figure 5.8 C-V and transfer curve of a thick WSe_2 transistor with transferred top-gate and contacts.

We note that there is relatively large gaps between source, drain electrode and the top gate. With limited gate control of the gate region, the on-current of the resulted devices is rather limited by series resistance and intrinsic low doping profile of materials of contact area. To further probe the FET performance of the device, we apply 60 V back-gate voltage to achieve a 40 μA/μm on-current (Figure 5.6e) and slightly higher SS of ~70 mV/dec, probably due to the extra charge introduced by backgate and trapped in the channel. The SS keeps below 80 mV/dec for 3 orders of magnitude until source-drain current reaches ~5×10^{-3} μA/μm (Figure 5.6f), showing steep switching behavior and the excellent modulation ability of the transferred dielectric layer. The transferred gate stack with sacrificial layer of CVD graphene shows similar modulation of MoS_2 channel (Figure 5.9).

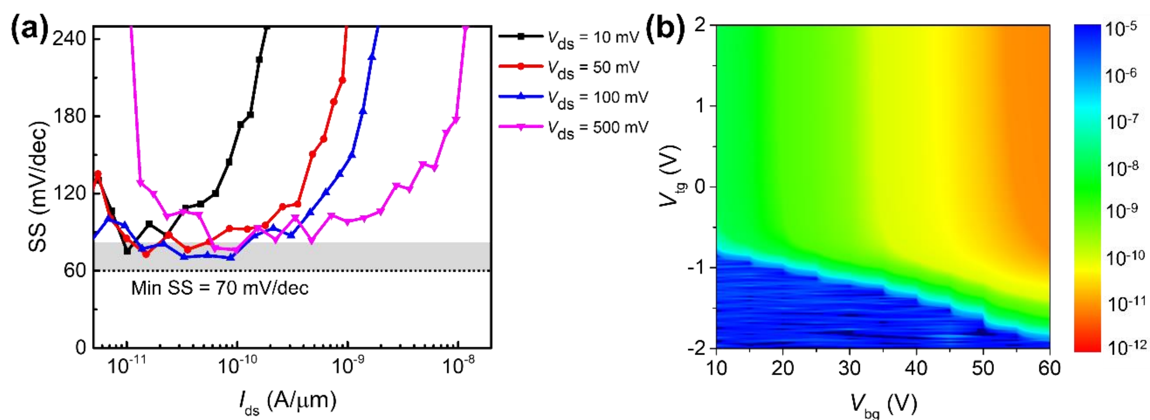

Figure 5.9 Performance of MoS_2 transistor using CVD graphene as sacrificial substrate. (a) Extracted SS. (b) Double gate current mapping.

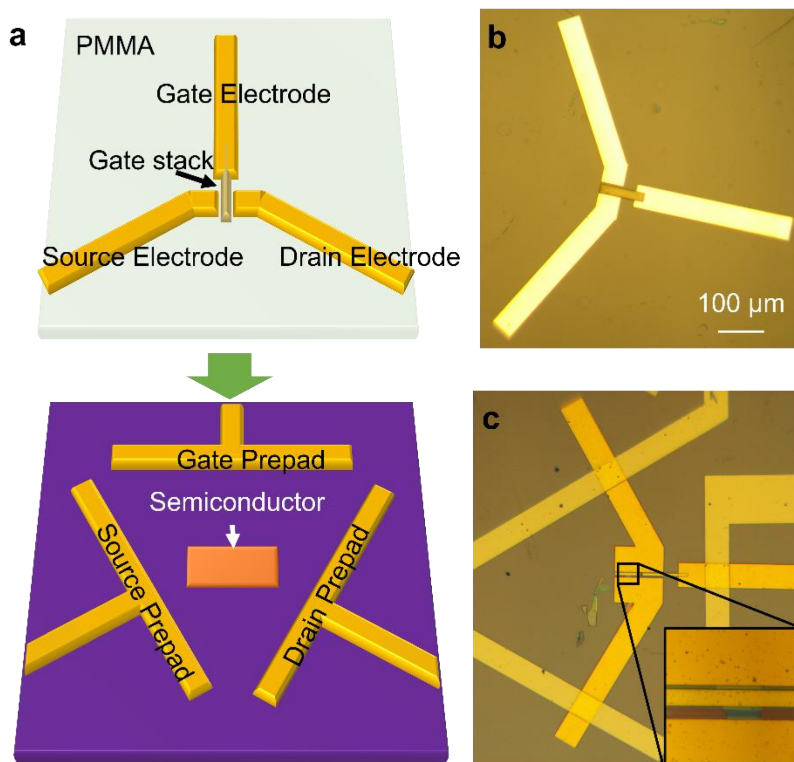

Figure 5.10 (a) Schematic of applying vdW plug-and-probe approach to integrate contact and gate dielectric on exfoliated WSe_2 in one step without any lithography and deposition steps (b) Back side of peeled off device architecture on PMMA. (c) Optical microscopic image of the WSe_2 device fabricated by one-step transferring Y-shaped top-gate transistor architectures.

To further demonstrate the general applicability and simplicity of this approach, we transfer the atomically flat gold contact and Y_2O_3 dielectric on exfoliated few-layer WSe_2 on substrate with predefined electrode pads to fabricate p-type top-gate transistors all at once (Figure 5.10a). The various building blocks of carefully designed Y-shape G/S/D electrode patterns are mass prepared by photolithography in advance. Thus, the WSe_2 device can be promptly fabricated and ready to measure (Figure 5.10b, 5.10c) in less than an hour after material preparation, with no need of any lithographical and deposition steps. A negative backgate voltage is applied to the generated top-gate transistor to turn on the ungated region of the channel material. Similar to MoS_2 transistors, the top-gate shows highly efficient electrostatic tunning of p-type channel with small hysteresis (Figure 5.6g, 5.6h, 5.11b), where the EOT and equivalent dielectric constant can be estimated as 4.5 nm and 17 by the linear relationship of threshold voltage shifts with backgate voltage change (Figure 5.11a), respectively. The SS of the top-gate transistors under various backgate voltages and drain voltages is consistent and has a minimum value of 77 mV/dec (Figure 5.6i, 5.11c). The high dielectric constant has enabled low-voltage operation of the p-type transistor indicated by the output curves (Figure 5.6g). The high-performance n-type MoS_2 and p-type WSe_2 transistors suggest this vdW plug-and-probe method is potentially a general approach compatible to electronically different materials thanks to the universal vdW interaction independent of material types.

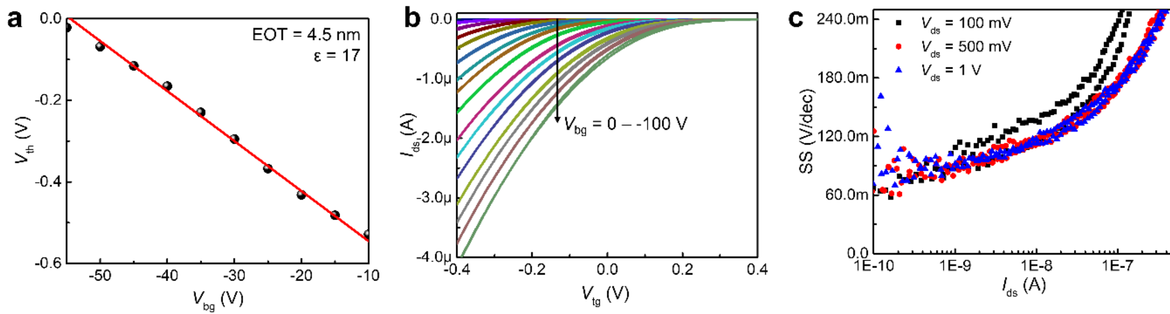

Figure 5.11 Double gate performance of vdW integrated WSe_2 top-gate transistor. (a) Linear plot of top-gate threshold voltage and backgate voltage. (b) Top-gate transfer curves under various back gate with neglectable hysteresis. (c) Extracted SS with various drain voltage under -100V backgate voltage

The "plug-and-probe" approach to a scalable approach can readily applied to large area CVD grown MoS_2 for scalable fabrication of top-gate transistor arrays. To avoid architecture damage and misalignments in later steps caused by large-scale deformation of PMMA, we use a hard and thick thermal-release tape on top of PMMA to assist the peeling-off processes and avoid unintentional stretching of the PMMA layer (Figure 5.12a). After aligning and laminating the device architecture array on prepatterned CVD monolayer MoS_2, the tape is released during the planarization step by thermal annealing, generating transistor array with clean vdW interfaces free of any high-energy processes (Figure 5.12b, 5.12c). The performances of the top-gated transistors are highly consistent with each other (Figure 5.12d) in terms of stable threshold voltage, neglectable hysteresis, low subthreshold swing and high on/off ratio. Most devices have SS falling in the range of 70-100 mV/dec (Figure 5.12e), which is among the best SS performances of CVD 2D materials considering the higher intrinsic defect density than exfoliated materials [16]. With the high-quality high-*k* dielectric integrated, the gate shows excellent electrostatic control of channel under low operation voltages as shown in typical output curves of these transistors (Figure 5.12f). The uniform performances indicate the high quality of device architectures and the clean vdW interface are conservable when increasing the scale or complexity of the integrated device structures.

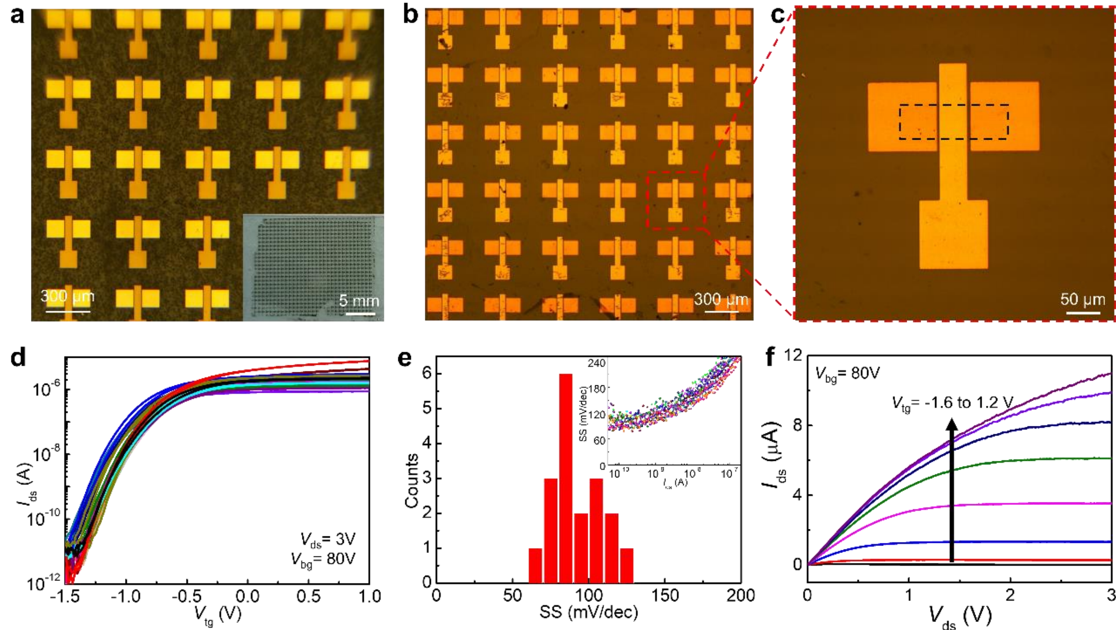

Figure 5.12 CVD MoS_2 transistor array fabricated via vdW plug-and-probe approach. (a) Peeled-off top-gate architecture array. Inset: photo of the array on thermal release tape. (b,c) Optical microscopic image of the derived top-gated CVD MoS_2 transistors. (d) Transfer curves of 18 transistors in the array under 80V backgate voltage. (e) SS histogram of devices in the array. Inset: Extracted SS at various current of all 18 devices. (f) Output curves of a typical MoS_2 transistor in the array.

5.5 Performance evaluation of the LHP transistors by vdW plug-and-probe

The one-step "plug-and-probe" approach offers a non-invasive process for simultaneous vdW integration of both high-quality dielectric/contacts with minimum interfacial damage, and can in principle be extended to arbitrary semiconductor with delicate surfaces. For example, probing the field-effect charge carrier transport in LHP is extremely challenging due to its intrinsic instability and extreme sensitivity to any chemical or high-energy processes. In particular, the LHPs are generally soluble in various solvents and incompatible with typical lithography processes, and they are highly delicate and prone to degradation during conventional vacuum metal deposition processes, making it extremely difficult to create robust top-gate transistors. To this end, the plug-and-probe approach offers an ideal solution for creating top-gate transistor arrays from CVD

grown LHP thin films for probing its intrinsic transport properties. By transferring gold contact and Y_2O_3 top gate-stack (Figure 5.14) directly on $CsPbBr_3$ thin film grown on mica substrate (Figure 5.13a), the transistor array is formed without introducing additional lithographic and deposition steps on the active interface (Figure 5.13b, 5.13c).

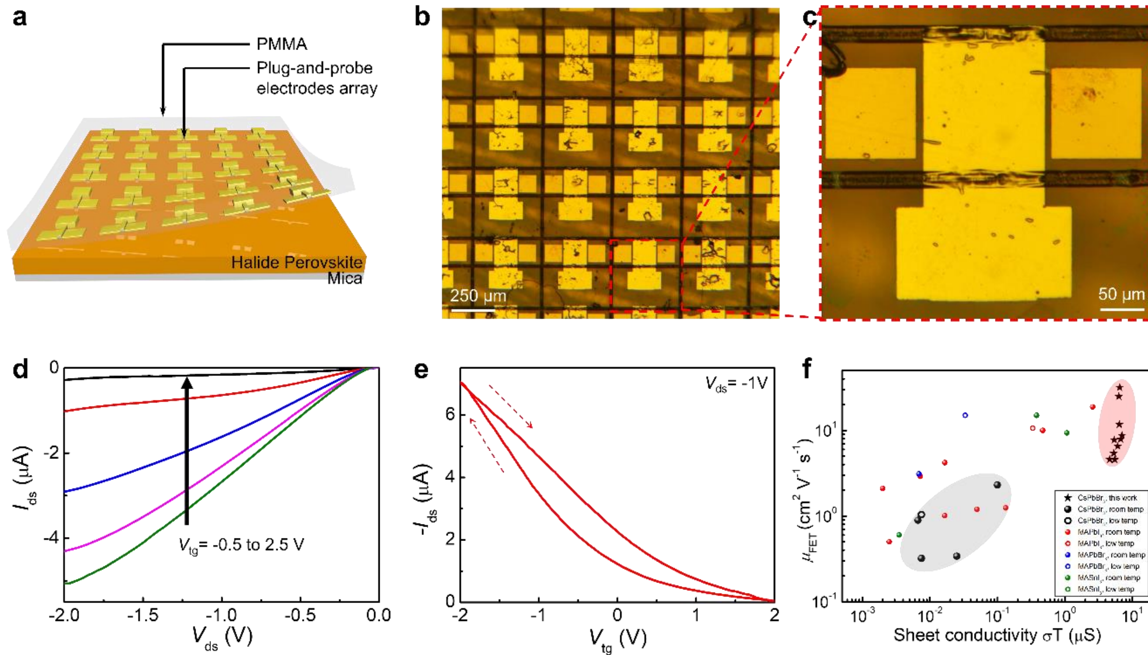

Figure 5.13 Epitaxial single crystalline $CsPbBr_3$ transistor array fabricated via vdW plug-and-probe approach. (a) Schematic of directly probing halide perovskite on mica substrate. (b,c) Optical microscopic image of the derived top-gated perovskite transistors. (d) Output curve of a typical perovskite transistor. (e) Typical transfer curve of a perovskite transistor in the array under 120 μW/cm^2 white light illumination. (f) Performance comparison among reported perovskite transistors in terms of mobility and sheet conductivity.

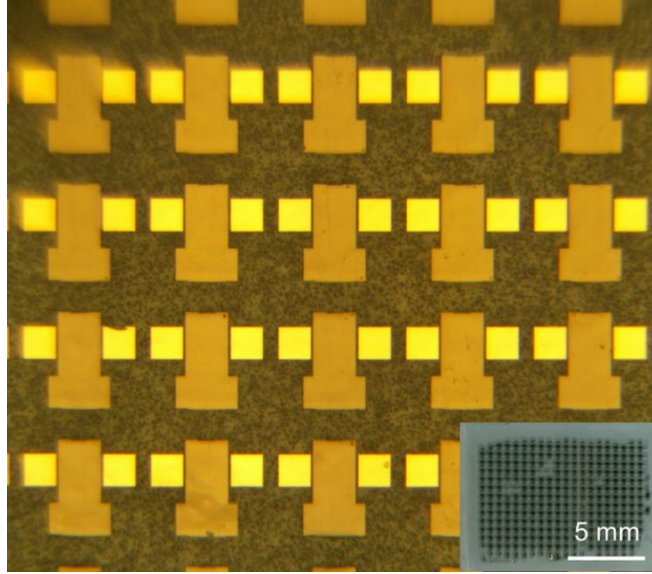

Figure 5.14 Optical microscopic image of the peeled plug-and-probe electrode array for fabricating perovskite transistors.

With optimized vdW contacts and gate dielectric interfaces, the LHP with vdW contacts and vdW gate dielectric show typical transport behavior and effective gate switch with a low operation voltage of 2 V. channel can be electrostatically tuned with decent on-current for all devices in the array (Figure 5.13d, 5.13e). Compared to 2D materials, the transfer curves exhibit a larger hysteresis, which might be explained by the relatively free ion movements during sweeping of gate field. The two-terminal hole field-effect mobility can be extracted from linear region of transfer curve using the following equation [4]:

$$\mu_{FE} = \frac{g_m}{V_{ds}} \frac{L}{W} \frac{1}{C_{ox}} \quad (2)$$

Where g_m is the transconductance of linear region of transfer curve, L and W are channel length and width, respectively, C_{ox} is capacitance density of gate oxide. The field-effect hole mobility of halide perovskite is usually compromised by low conductance dominated by large contact resistance, and lack of compatible top-gate materials with enough electric field to tune 1

μm thick single crystalline perovskite. The 300 nm SiO_2 backgate can hardly tune the conductivity of the LHPs (Figure 5.15). Thus, previous measured field-effect mobility of inorganic halide perovskites can hardly match up to its intrinsic mobility [58], not to mention the large measurement uncertainty due to the low conductivity of channel. By applying the vdW plug-and-probe approach, both difficulties of large contact resistance and low-efficiency dielectric are alleviated by adopting a vdW metal contact and high-quality high-*k* dielectric. Thus, a champion two-terminal field effect mobility of 32 $cm^2/(V{\cdot}s)$ is achieved, which is among the best mobilities measured in perovskite transistors (Figure 5.13f), also significantly higher than other reported $CsPbBr_3$ transistors. In addition, we can achieve the largest conductivities with the vdW gold contact to minimize contact resistance, which is crucial in improving accuracy of mobility measurements. The high-*k* dielectric also unlocks low-voltage tunability of the channel material. This plug-and-probed transistor array provides a convenient and reliable approach for investigating intrinsic transport and apply efficient electrostatic control of halide perovskites, which is highly unexplored area because the pristine transport is usually convoluted by ion-migration inside the crystals.

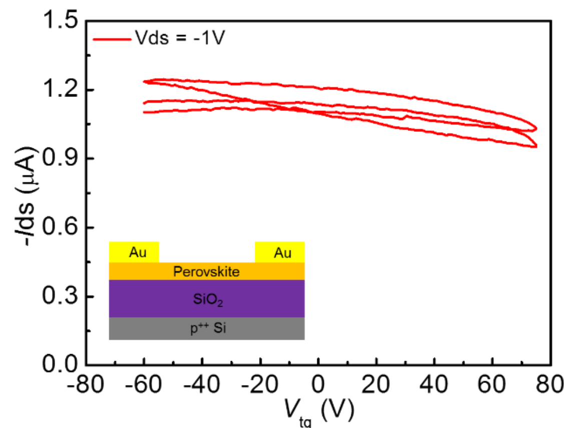

Figure 5.15 *Transfer curve of the perovskite transistor on SiO_2 (300nm) substrate under light illumination of 120 μW/cm2. Mobility is about 0.1 $cm^2/(V{\cdot}s)$. Inset is the transistor structure.*

Besides 2D materials and LHPs, we have also applied this approach on Poly(3-hexylthiophene-2,5-diyl) (P3HT), a polymer p-type semiconductor that is difficult to grow high-k oxide using ALD, and 2,7-Dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT), which is a small organic molecule that can form highly crystalline thin films vulnerable to many chemicals and high-energy processes. The P3HT top-gate transistors show low-voltage operation (Figure 5.16) under 4V compared to 60V using back gate and evaporated contacts. The C8-BTBT transistors shows a similar low-voltage operation and significantly higher current than evaporated contacts (Figure 5.17).

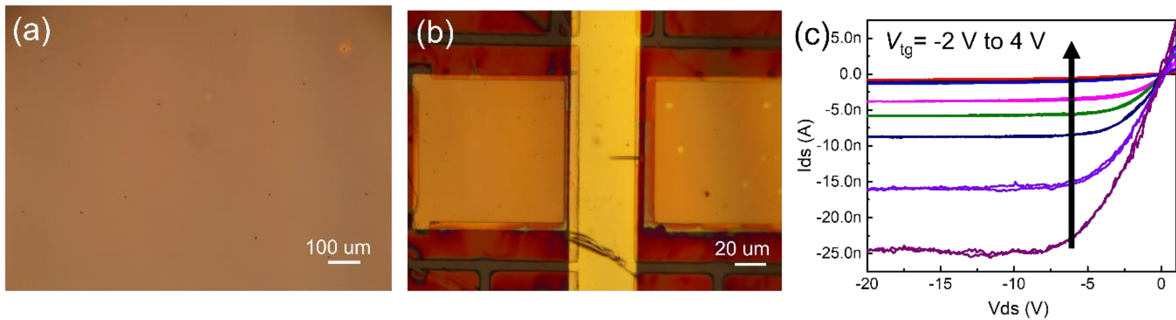

Figure 5.16 P3HT top-gate transistor by vdW plug-and-probe. (a) Spincoated P3HT film with uniform film thickness. (b) Generated devices by transferring both gold contact and Y_2O_3 top gate. (c) Output curves of the P3HT top-gate transistors.

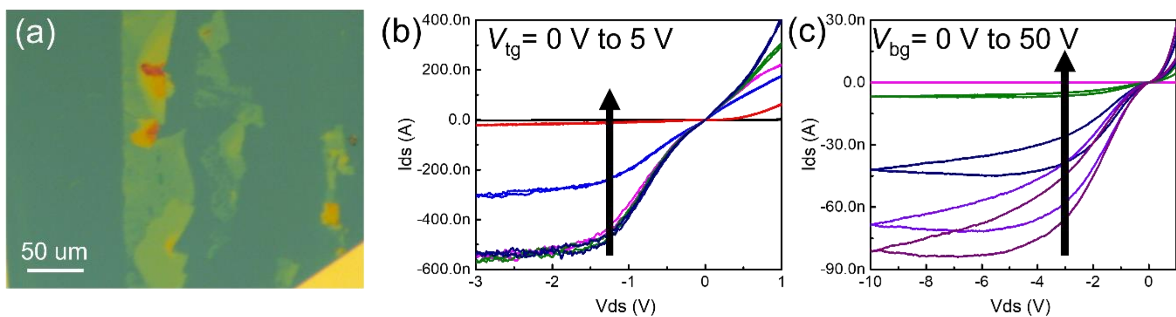

Figure 5.17 C8-BTBT top-gate transistor by vdW plug-and-probe. (a) C8-BTBT crystalline thin film prepared by off-center spincoating on a substrate with prepads. (b) Output curve of the C8-BTBT top-transistor with transferred contact. (c) Output curves of the C8-BTBT transistors with evaporated contact and SiO_2 back gate.

5.6 Conclusion

The superior performances of top-gate transistors of various delicate semiconductors with distinct lattice structures, electronic properties and process limitations has validated the vdW plug-and-probe approach as a universal and convenient method for fundamental transport studies and fabricating high-performance devices. The decouple of high-energy contact/dielectric deposition and device integration has overcome the process incompatibility to enable high-quality device architectures potentially on any semiconductor with delicate surface. Since the device architectures and materials are combined with non-bonding vdW force, the pristine interface is conserved and free of externally introduced damages and disorders, which is crucial to maintain the superior properties of these novel materials. This convenience approach could further evolve into a reusable stamp probe with peeled-off device architectures embedded at the bottom. The electrical characterization can be as easy as stamping on material to take measurements, and then stamp is removed for next test. With the vast compatibility, non-invasive integration and simplicity, two type of materials will benefit most from this technique: the ones that can quickly degrade or easily lose electronic functions by lithographic and deposition processes such as halide perovskite, self-assembled monolayers and black phosphorus which can benefit from the convenient and non-invasive approach; and materials with prominent properties heavily relying on an ideal interface such as 2DSCs for high-performance FETs and spin-injection devices. There is no fundamental challenge for this plug-and-probe technique to integrate more complicated device architectures for advanced probing of exotic transport and integrated circuits of delicate semiconductors, unlocking a promising integration approach for both fundamental materials research and potential applications for future electronics.

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Chapter 6. Conclusion

In this dissertation, we have pushed the van der Waals integration methods a step further to be a more general approach for probing and pushing the performance of novel electronic materials such as 2D materials, large bandwidth oxides, halide perovskite, etc. These materials usually exhibit highly variable chemical compositions and delicate surfaces that are vulnerable to traditional integration approaches, which could result in undesired disorder and defects that could compromise fundamental transport studies and degrade the device performance. The non-bonding vdW integration offers a mild strategy for integrating these emerging electronic materials into functional devices with minimum interfacial damages to ensure atomic clean and electronically sharp vdW interface by design. So far, the vdW integration is still a rising technique with unmature integration of complicated device structures and heterostructures beyond 2D, which are our major concern to solve in this dissertation.

We first show in Chapter 2 that the vdW metal contact could be developed to fabricate sub-10 nm 2D transistors for future miniaturization of integrated circuits. The ultrashort channel and the optimum contact interface have enabled high on-current density and reliable probing quantum transport in 2D materials, which is difficult and expensive to achieve for 2D materials via traditional device fabrication techniques. The vdW integration approach has indeed prominent potential as an alternative to further miniaturization of logic gates and memories especially efficient for the novel electronic materials.

Next, we extend the vdW integration which generally has been previously limited in 2D heterostructures to the vast library of 3D materials in Chapter 3. The 3D semiconductors with passivated surfaces can be readily combined with vdW force to enable completely new devices that are largely unexplored before due to lattice matching requirements. By demonstrating vdW

Pt-Ga_2O_3 and pSi-Ga_2O_3 heterojunction with close-to-unity ideality factor and large rectification ratio, as well as derived MESFETs and JFETs with ultralow off-current, decent on-current and steep switching, we have shown that the vdW integration can also fully exploit the merits of traditional bulk semiconductors to generate heterostructures with brand new material combinations. This study has unlocked rich material choices for vdW integration to create novel devices with diversified functions.

We have also explored other novel device designs to solve other difficulties faced by the delicate materials. In Chapter 4, by extending a high-*k* "feedback" gate from source/drain into channel, the electrostatic control by source/drain can eliminate the threshold roll-off and undesired ambipolar transport, which are some crucial but often overlooked device parameters. This unique device structure is useful to stabilize the device performance of emerging electronic materials for logic gates integration and further applications of 2D materials and other prominent novel semiconductors.

Finally, we successfully developed a vdW plug-and-probe technique of integrating both metal contacts and high-*k* gate dielectric on one step to enable nearly ideal top-gate transistors based on emerging novel semiconductors. The vdW 2D top-gate transistors show an idea subthreshold swing with neglectable hysteresis and decent on-current density. The vdW lead halide perovskite transistors have shown best two-terminal field-effect mobility to date and a large conductivity for precise measurements. More importantly, this plug-and-probe approach is scalable for centimeter-scale top-gate transistor array, where all devices show high uniformity and decent performances. This approach has shown compatibility with complicated device architectures with distinct sets of materials without altering the superior property of the emerging delicate semiconductors, laying a

basis for further miniaturization and function diversification of future devices based on these novel electronic materials.

With the continued development in vdW integrated devices based on emerging electronic materials, the vdW integration will open an entirely new chapter in material science for creating diverse artificial heterostructures and high-performance devices beyond what is possible before. The availability of such widely variable heterostructures and devices with designable electronic interfaces provide a dreamland for condensed matter physics and could enable totally new opportunities for future electronic technologies and beyond.