LOW POWER AND LOW PHASE NOISE VCO FOR PLL APPLICATION

By

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Abstract

In modern communication systems, the voltage-controlled oscillator is an important circuitry that has applications such as clock generations, wireless communication, synchronization, and frequency synthesis. The most concentration in VCO research has been lower phase noise, higher frequency, low power consumption, and wide tuning range. Each of the goals is reachable on its own at the cost of other goals in VCO design. There are tradeoffs in the design where in this thesis, the middle ground is found in order to achieve low phase noise and low power consumption. This paper will provide a detailed analysis of Low Phase Noise and Low power consumption VCO using 65nm technology. The design of the PLL is analyzed where the VCO effect is explained. The types of noise in the VCO that lower the phase noise are discussed in section 2.2.3. The circuit simulation will be demonstrated in order to achieve the goal of low phase noise and power consumption. Isolation techniques will be provided in order to make sure VCO operates properly. This paper will include full layout techniques used to make the VCO for the SSPLL application. Fabricated stand-alone VCO will be measured and compared to the simulation.

Acknowledgment

I would like to give a special thanks to my advisor, Dr. Omeed Momeni, for giving me the chance to pursue my Master's Degree at University of California, Davis and providing me guidance in IC design. Special thanks to Cheng Li, Hao Wang and Hamidreza Afzal for teaching me layout and simulation techniques. Special thanks to my friends Mahan Hafezi, Jesse Palomera, and Pouya Emami for supporting me during my master's. Finally, I would like to thank my family for supporting me through my entire educational experience.

Table of Contents

1 Introduction

1.1 The motivation of Voltage Controlled Oscillator

The Voltage-Controlled Oscillator (VCO) is a critical circuit used in modern communication systems. It is commonly used to produce a given frequency which can be applied to mixers for the downconversion or upconversion of signals. [1] Furthermore, the VCO is commonly designed with the Phase-Lock Loop (PLL) system to synthesize a highly stable output frequency.

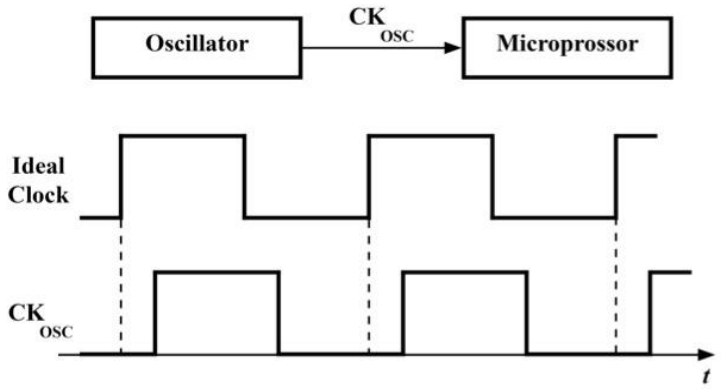


Figure 1: Ideal and non-ideal oscillator clock for Microprocessor

Let's assume an oscillator provides a clock signal to a microprocessor. How would the ambient temperature fluctuation affect the clock? The output signal will suffer. Temperature fluctuations will affect the transistors operation causing random phase accumulations which change the output frequency of the VCO . Compare the affected output signal compared to the ideal clock in Figure 1. As much as the VCO is important in electronics, a system to keep the VCO in check is also required. This is the job of the PLL which will have a control system for the output frequency provided by the oscillator. [2] In the PLL design, the goal is to align the output phase of the oscillator with the input reference. The PLL includes a phase detector, Low pass filter, VCO and divider shown in Figure 2(a).

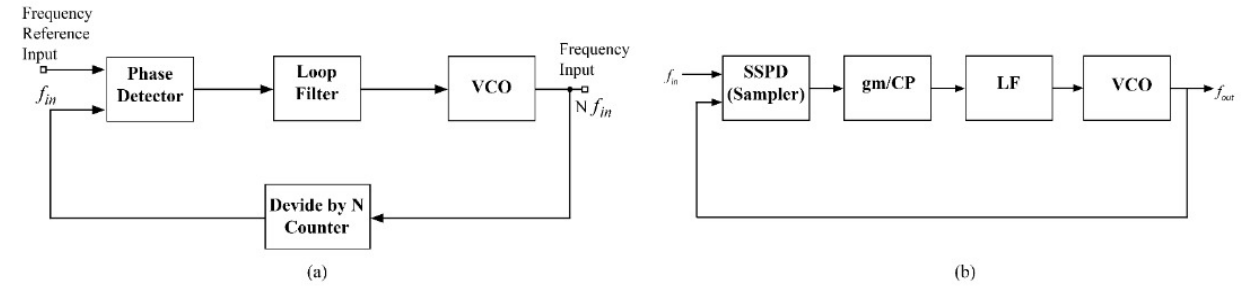


Figure 2: Block Diagram of (a) PLL Design and (b) SSPLL Design

The dynamic of such a synthesizer produces an output frequency N times the reference input. One of the flaws of this system is that the phase noise (PN) of the the output is N^2 times larger than that of the input. [3]. Additionally, if the difference in phase of the input and output signals is large, the system will never lock.. [4] To avoid these issues a Sub-sampling Phase Lock Loop (SSPLL) is introduced. The system dynamic of the SSPLL is shown in Figure 2(b).

The most common topologies of VCO include the Ring Oscillator and LC resonator which are shown in Figure 3. When choosing between these two topologies, phase noise is a critical consideration. We must choose a topology which produces the minimum output referred phase noise in order to minimize the PN of the SSPLL loop.

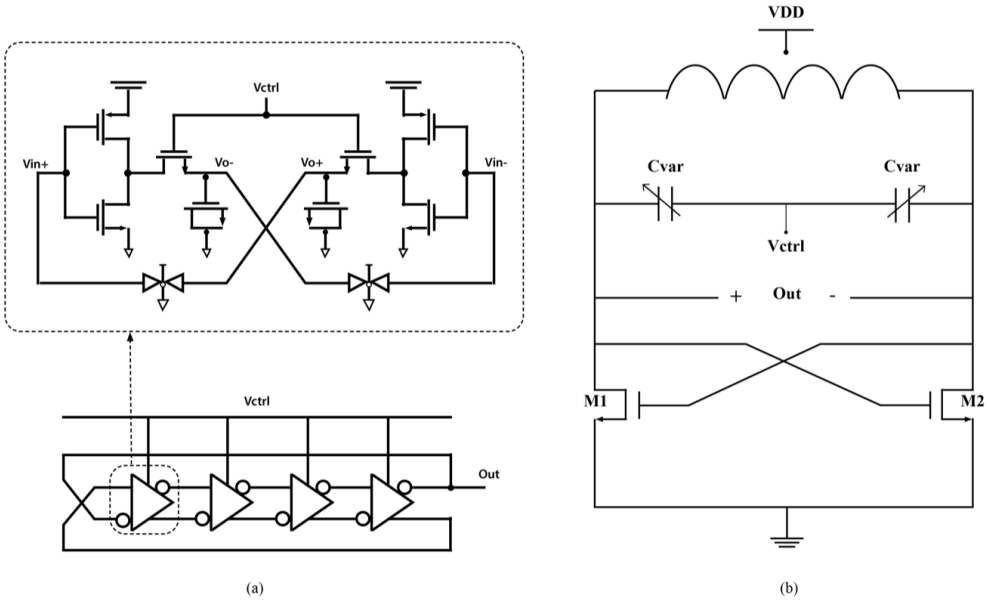


Figure 3: (a) 4-stage Differential Ring Oscillator Design (b) LC VCO

Ring Oscillators are commonly used in PLL design due to their speed, wide tuning range, and small chip area. [5] The LC resonator on the other hand is used due to its low phase noise and low power co. LC Oscillators are also known to have even better speeds than the Ring Oscillator.[6]. Due to the high sensitivity of the SSPLL system to VCO phase noise LC resonators make a good topology choice for the VCO design. Within the LC VCO design, both active and passive parts of the circuit must be considered for PN optimization. [7] Phase noise can also be slightly improved with optimal layout design, specifically the active components of the circuit.

1.2 VCO Metrics

In the VCO design, an input voltage is presented in order to tune the resonator. The ideal Voltage-controlled oscillator design consists of output frequency that is linearly correlated to the input voltage. Output linearity is only one of the essential requirements for a high quality Voltage-Controlled Oscillator design. The steady gain ensures the PLL design to work efficiently. In order to evaluate the

designed Voltage Controlled Oscillator, a few metrics are used which include phase noise,tuning range, power consumption, output amplitude and output power. [8]

The next metric that a quality VCO must have is a proper tuning range. The proper tuning range consists of two rules. The tuning range must be designed in such a way that the desired application frequency is placed in the middle of the tuning range. The second rule is to maintain good frequency stability across process and temperature variation. [9]

In the PLL design, VCO will consume the most power compared to other parts of the system. The success of the VCO depends on numerous metrics that all affect each other. In the VCO design, the tuning range and phase noise take priority because the VCO needs to provide a steady and specific output frequency.

Fluctuations of amplitude and phase will be present in the VCO when flicker noise is upconverted to the output spectrum. In addition to active and passive components in the VCO, power supplies can also contribute to the PN of the circuit. There are several trade-offs in minimizing the phase noise of the VCO, one of which includes the tradeoff between power consumption and PN. In the text, Leeson's linear-time model of phase noise will be presented and used in order to optimize the tradeoff between power consumption and PN.

The last metric is the output amplitude of the VCO signal. Increasing this amplitude will require more power, but also make the VCO less sensitive to noise. Each metric has certain trade-offs and limits for other metrics. This paper discusses the design of a quality VCO that optimized these metrics with careful considerations.

1.3 Application of Proposed VCO Design

The proposed VCO is specifically designed for a SSPLL Application. The 6.84 GHz frequency synthesizer adopts a sub-sampling technique [10] that can achieve low phase noise with low power consumption. However, one of the main issues is that the output of the phase lock loop (PLL) can lock to

the wrong harmonics of the input reference due to the sub-sampling effects. To address this issue, we use a frequency-locked loop (FLL) [10] to assist the SSPL. Figure 4 shows the schematic of the SSPL with FLL. The FLL consists of a divide-by-N and a three-state phase frequency detector (PFD) and CP as in a classical PLL, except that a dedicated dead zone (DZ) is inserted between the PFD and CP. When f_{out} is much different from Nf_{ref}, the phase error between VCO and Ref is large and falls outside of the FLL DZ. The FLL has a larger gain than the core loop, dominates the loop control and brings down the difference between the f_{out} and Nf_{ref}.

When it is close to locking, the phase error between VCO output and f_{ref} is small and falls inside the FLL DZ. The output current of the CP in the FLL will then be zero. Hence, the FLL and the divide-by-N have no influence on the core loop and do not degenerate the PLL jitter performance. After locking is achieved, the CP of the FALL can also be disabled to save power.

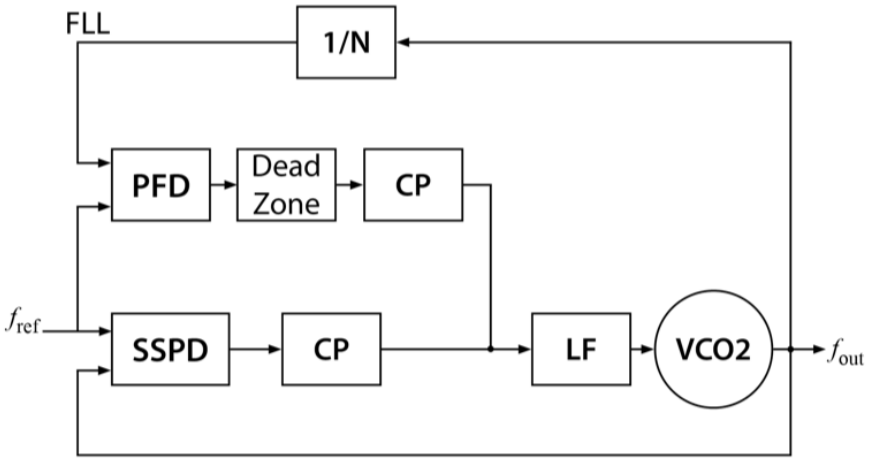


Figure 4: SSPL with FLL loop

In this paper, an LC resonator is proposed for the SSPLL operating at 6.84 GHz. The bandwidth of the SSPL with FLL is set to be 2MHz. The FLL loop has no influence on the core loop after it is locked to the correct harmonics, thus the noise from the FLL loop can be negligible. Since the VCO free-running

frequency is sensitive to variations of process, supply voltage, and temperature (PVT), a switch-capacitor (SC) tuning circuit is added to the VCO LC tank to have a manual tuning mechanism. Figure 5 shows the circuit for the SC and varactors.

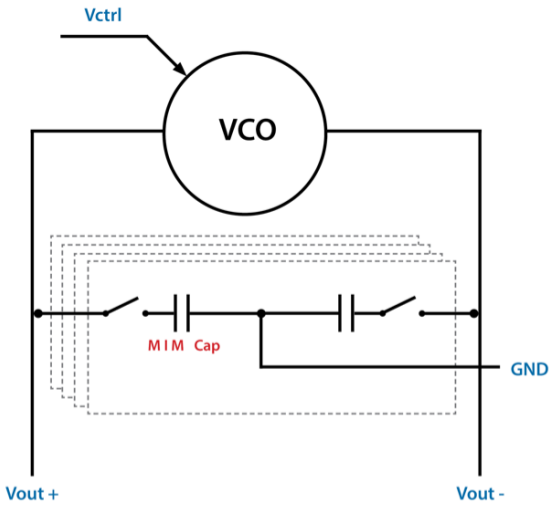


Figure 5: Four Switch Capacitors added for off-chip tuning

Additional varactor capacitor controlled by off-chip biasing voltage is added to achieve continuous tuning of the VCO frequency. When the switch is closed, the capacitor is connected to the LC tank of the VCO in parallel. Hence, the total capacitance of the tank is increased and the frequency of the VCO drops. Each SC configuration can change the VCO frequency at least by 148-MHz. At each configuration, the Vcont tuning range of the VCO is designed to be more than 226 MHz to ensure the frequency tuning is continuous between different SC configurations. Having switch-cap and two varactors, VCO locking to the correct harmonic is manageable due to the PVT. The SC components can account for the variation in frequency over temperature variations. When the temperature changes from -50 °C to 50 °C, the maximum frequency variation due to the temperature variation is less than 40MHz.

By using the SC circuit, the free-running frequency of the VCO can be changed continuously from 6.38GHz to 7.33GHz, which should be enough to compensate for the frequency variations due to the PVT. The variation of the phase noise is 2.5-dB at 1MHz frequency offset, and the worst case of the phase noise can still meet the design requirements. The design requirement for the VCO is -108 dBc/Hz at 1MHz offset. Having such a phase noise will ensure to meet the phase noise requirement. With all the contributions of SSPL elements, the VCO phase noise at 1MHz is designed to be -115 dBc/Hz with EM and layout caliber files included in simulation.

1.4 Thesis Organization

This paper will start with the fundamental design of PLL/SSPPL and the different topologies of VCOs. The next section of the paper will detail the proposed design which includes simulation, layout, and EM optimization which was performed. The last section will discuss the measurement of the design chip which includes stand-alone VCO measurement and VCO in the SSPLL measurements.

2 Basics Fundamentals

2.1 Phase Lock Loop Fundamentals

Phase-locked loop is widely used in Radio Frequency building blocks such as FM demodulators, Signal Re-constitution, Clock Recovery and Frequency Synthesizers. [11] The loop is a voltage driven oscillator where it is constantly checking output frequency to the reference to match the input frequency. The phase detector is used to find the difference between the output frequency of the VCO and reference. Based on the phase difference, a voltage is provided to the VCO where the frequency adjusts. This process continues until the center frequency matches the frequency provided by the low pass filter. A low pass filter between the VCO and phase detector is designed to provide DC control voltage. [11] In the negative feedback loop, a divider can be used for a low-frequency signal where reference noise will be lower. A simplified block diagram of PLL is shown in Figure 2(a).

2.1.1 Phase Detector

For the Phase lock loop design, a circuitry is required to measure the phase difference between input and output in the negative feedback loop. Phase detector's purpose is to find the difference, where the phase difference is translated into voltage. The voltage will be provided to the VCO which changes the output frequency. The relationship between phase difference and voltage is a linear relationship which is illustrated in Figure 6 (a).

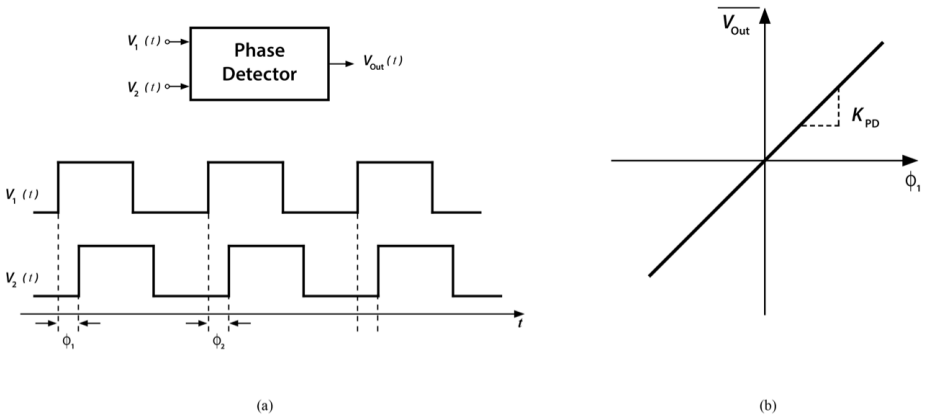


Figure 6 : (a) Phase Detector input and output when VCO is lagging (b) correlation between input and output of VCO

The gain or the slope of the voltage vs phase is denoted as K_{PD} which is expressed as volts per radian. For instance, for one radian of phase difference, a phase detector produces 100mV. This only comes into play when the frequencies are equal for input and output otherwise phase difference changes with time which is shown in Fig 6 (b).

It is crucial to understand the relationship between frequency and phase since we will detect phase difference and compensate for frequency. The input reference can be defined as $V_{in}(t) \approx sin(2\pi f_{in} t)$ which will be compared to output of the VCO which is defined as $V_{out}(t) \approx sin(2\pi N f_{in} t)$. Phase can be defined as $\phi = \omega t$ but this does not define the total phase.

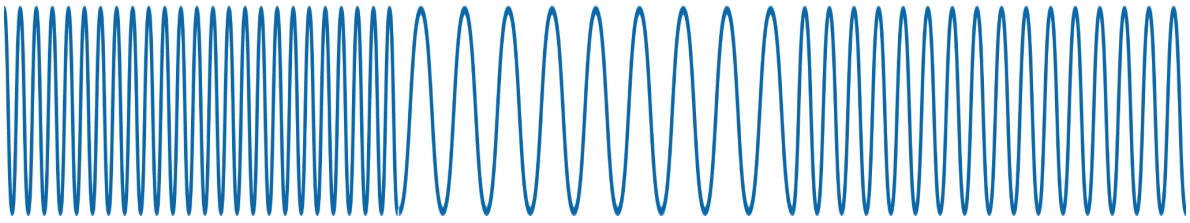


Figure 7: Output of VCO when Vcont changes over time

Looking at Figure 7, we see that frequency changes over time which could be the case with the oscillator as V_{cont} changes to align the output frequency to the input. Our definition $\phi = \omega t$ will no longer be valid in this case since this equation does not define change of phase. In order to define the phase as frequency changes, we must integrate $\phi(t) = \int_0^t \omega(t)\, dt = \int_0^t 2\pi f(t)\, dt$ where $f(t)$ can be defined as $f(t) = \frac{1}{2\pi}\frac{d\phi(t)}{dt}$.

Once the output frequency is aligned meaning phase is locked, then we have

$$\phi_{out} = N\phi_{in} \leftrightarrow f_{out} = Nf_{in}$$

2.1.1.1 Exclusive OR Phase Detector

Most basic design of a phase detector is an exclusive (XOR) gate. If amplitude of the input is large to Gilbert cell, the cell behaves as Exclusive OR gate. When the phase difference drift from 90° causes the output duty cycle to deviate from 50% making the DC output to be proportional to the phase difference between input and output signal. [12] This type of phase detector has acquisitions range benefits since it covers 0° to 180°. The main drawback with this type of phase detector is the dependence upon input duty cycle. If the frequency is far from the input frequency, locking will take a long time or may not even acquire the desired frequency. To solve this issue a phase frequency detector (PFD) is introduced to bring the frequency close to desired frequency, thus putting phase shift in range of 0° to 180°.

2.1.1.2 Phase Frequency Detector with Charge Pump

In order to detect phase and frequency difference, D-flip flop is used to bring the frequency close first then output a voltage proportional to the phase difference. Such a circuit is illustrated in Figure 8.

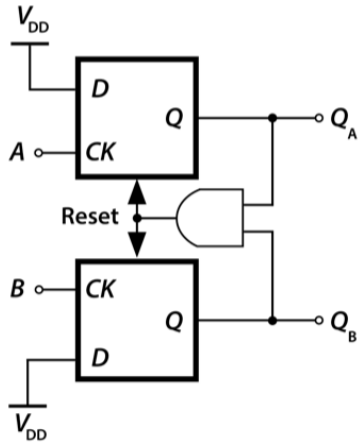


Figure 8: D-Flip Flop circuit design used for Phase Frequency Detector

This type of circuit utilizes two edge-triggered, resettable D-flip flops where the input logic is constant HIGH. [12] The signal in QA goes to the AND gate to be compared to the other D-flip flop QB signal. Assuming both QA and QB are both HIGH which are input to the AND gate where the output will be HIGH which activates the reset to both of the D-flip flops in Figure 8 causing both Qs to reset to LOW.

In Figure 9 (a), we have the case where the frequencies are close, but the phases are not the same. In this case QA will generate the signal that's the difference of the phases between the signals. The reason QB is LOW in part a is due to signal A having the rising edge first which indicates QA is sending a signal to increase the voltage (UP) of the VCO. In the second case, the frequencies are not equal as we see in Figure 9 (b). The larger intervals of QA are sending signals to increase the voltage indicating the frequency must increase. [12] In order to complete this PFD design, a circuit must be included after the PFD to generate the DC control voltage.

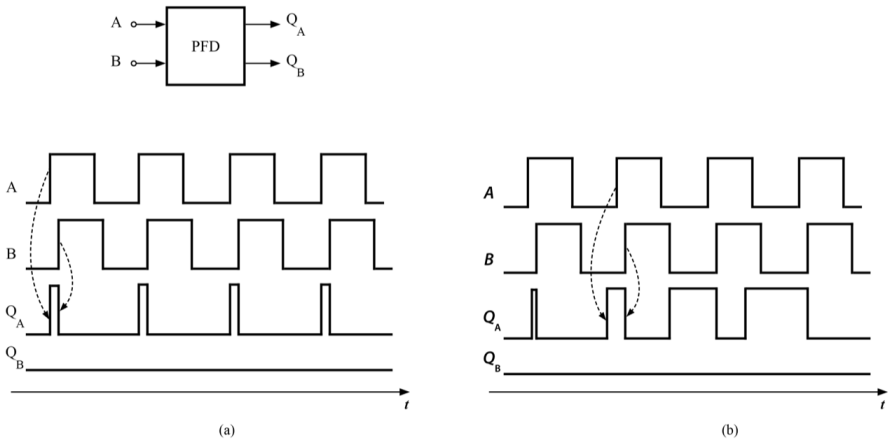


Figure 9: (a) PFD with different input phase difference and (b) different input frequency difference

In the PLL design, a circuit called Charge Pump (CP) is employed in conjunction with a PFD; a simple CP is illustrated in Figure 10.

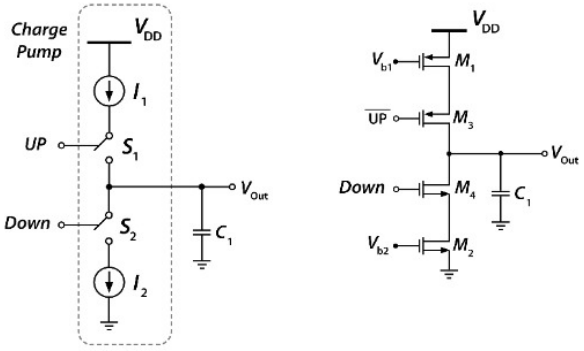


Figure 10: (a) Simple charge pump design and (b) transistor design

The controls in the charge pump are called Up and Down which are a given signal based upon phase and frequency difference compared to which input of the PFD is leading. Assuming UP signal is HIGH, meaning Signal A to the PFD is leading, causing switch 1 (S1) to be on. The reason M3 gate is called UP is because when UP is HIGH then the switch turns on. When S1 is ON then I1 will pour current into Capacitor 1 (C1) causing an increase in voltage across C1. The voltage across C1 is the control voltage feeding the VCO. With this technique, not only do we have the chance to adjust the VCO

frequency compared to input phase, but also based on the frequency. [13] In Figure 11, we can see an operation of the PFD with the charge pump. There's one significant benefit of this circuitry which is that Vout is held, which keeps the VCO control voltage constant until there must be a change. In the basic XOR design shown in Figure X, the voltage is increased when there's a phase difference and where, if there's no difference, the control voltage is LOW.

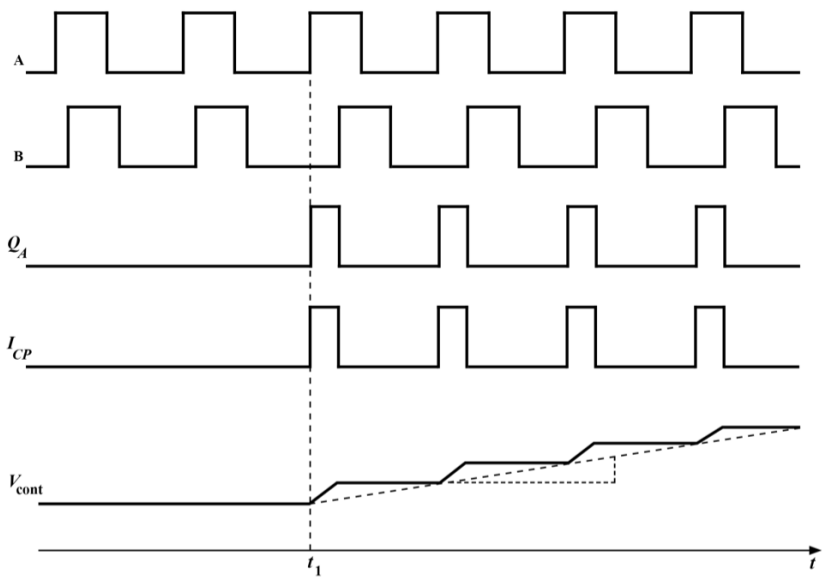


Figure 11: Operation of PFD and Charge Pump

There are some drawbacks with the PFD which skew between UP and DOWN pulses, random mismatches of pulse widths and phase noise. The delay happening between UP and DOWN signals may become comparable with the switching delay near locking condition which creates a dead zone causing jittering at the output. The switches also introduce phase noise to the circuit. The skew and mismatches can be fixed by using large transistors and symmetric layout design. [12]

For each part of the circuit, it is very important to define the transfer function in order to define the stability of the loop and also the phase noise contribution of the circuit to the loop.

Transfer function of the PFD and Charge Pump:

Figure 12: Input and output of Phase Frequency Detector and Charge Pump

The difficulty with writing the transfer function is that input of the PFD/CP is *phase* quantity and the output is *voltage* quantity. The analysis of transfer function begins with impulse response then taking Laplace transform to find the transfer function of PFD/CP. At the input of the PFD/CP, we know that we are looking at the difference between reference input and VCO output signal. Based on the difference shown in Figure 11, we can see that $Q_A$signal is the difference which allows I_{CP} to charges the capacitor during $\Delta T\ or\ \Delta\phi$. [14]

Looking at B input in Figure 11, we see that phase step is $\Delta\phi_1$ at $t = t_1$making Q_A signal to be high for $\frac{\Delta\phi_1}{2\pi} \cdot T_{in}$seconds. During every phase comparison , V_{cont} rises by $\Delta V = \frac{\Delta\phi_1}{2\pi} \cdot T_{in} \cdot \frac{I_P}{C_1}$ during each phase comparison. [15]

Looking at Figure 11, we can do a linearity test since the $V_{cont}$the waveform is nonlinear. If $\Delta\phi_1$ is doubled, we can observe that flat section of V_{cont} double as well. This observation shows us that V_{cont} can be approximated as a continuous ramp shown as a dashed line in Figure 11. During period T_1, the slope of the linear ramp can be written as $\frac{\Delta V}{T_1} = \frac{\Delta\phi_1}{2\pi} \cdot \frac{I_p}{C_1}$. Since we have ΔV and $\Delta\phi$, the equation must

be integrated in order to find the total area under the change. For the input impulse of $\Delta\phi_1\delta(t)$, we get impulse response of $\frac{\Delta\phi_1}{2\pi} \cdot \frac{I_p}{C_1} \cdot u(t)$ where Laplace transform of the impulse response will give us the transfer function of PFD and Charge pump as :

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_p}{2\pi C_1 s}$$

The transfer function signifies one pole at the origin meaning that it is an ideal integrator. [14]

2.1.2 Voltage-Control Oscillator

In circuit design, when frequency needs to be adjusted electronically, a Voltage-Controlled Oscillator is used. It can be treated as a black box illustrated in Figure 13 where the input is Vctrl which outputs a periodic oscillating output $V_{out}(t)$ that could be differential or single-ended. The black box has power supply through VSS and VDD.

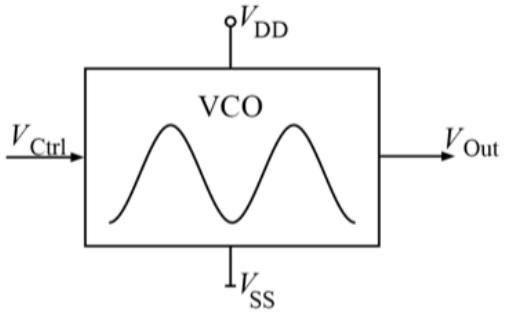


Figure 13: Simple VCO Block

The purpose of this VCO design is to be used within a phase-lock loop to automatically match frequency to a reference. Oscillation can change based on the following control voltages:

Figure 14: Different input voltages of VCO

In order to have steady oscillation, a positive feedback must be created which is illustrated in simple feedback loop in Figure 15 that must satisfy Barkhausen criteria :

$$|H(s)| \geq 1$$

$$< H(s) = 180^{\circ}$$

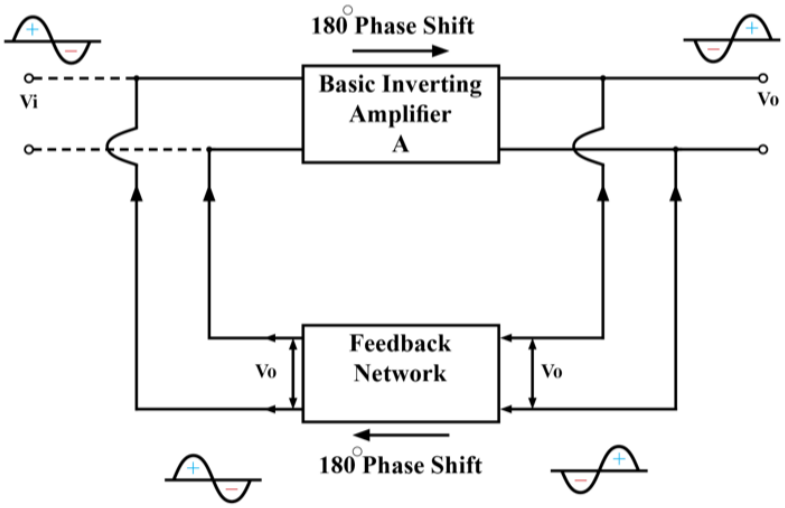


Figure 15 : Positive Feedback of the VCO

Let's assume V_{in} is applied at the input of the amplifier at which the output becomes $V_{out} = AV_{in}$. Voltage of the feedback is set by $V_f = -\beta V_{out}$ meaning the gain of the feedback where the negative

sign indicates phase shift of 180°. Substituting V_{out} into $V_f = -\beta V_{out}$, we get $V_f = -A\beta V_{in}$. The oscillator design requires the feedback output to drive the amplifier where V_f works as V_{in} then we have $-A\beta = 1$. The expression can be written as $A\beta = -1 + j0$, where the magnitude is equal to 1 and phase magnitude must be the same for V_f and V_{in}. Since the amplifier introduces 180° of phase shift then the feedback must introduce another 180° to set V_f and V_{in} phase shift the same. [15] That's the Barkhausen *criterion* for oscillation.

In the beginning operation of the oscillator, there might not be a voltage present at the input therefore the oscillator amplifies the voltage noise to jump start the circuit. To sustain the oscillation, $A\beta$ must be equal to 1 and total phase shift around the loop of 0° or 360°. [15]

There are many types of oscillators, but the most common are ring oscillator and LC oscillator which have an advantage of being easily modified to change oscillation frequency with the control voltage.

2.1.2.1 Ring Oscillator

The ring oscillator design contains N-number of stages within the loop which each stage is an inverter shown in Figure 16 :

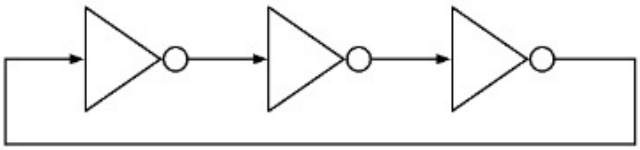


Figure 16: 3-stage cascaded Ring Oscillator

The main advantage of Ring oscillator is wide tuning range, compact layout design and cable of creating multiple phases. Compared to an LC oscillator, a ring oscillator does not require an inductor but

it costs the worst phase noise. The other disadvantage is that ring oscillators operate in low frequency in order to avoid latch up. [16]

Assuming the the inverting amplifier has transfer function of $A = -\frac{A_0}{1+\frac{s}{\omega_0}}$ where the loop gain can be written as $H(s) = -\frac{A_0^3}{(1+\frac{s}{\omega_0})^3}$. The three stages are the amplifier stage meaning the total phase shift must be 180° in order to meet Barkhausen criteria. Since there are three stages in Figure 16, we can conclude that each stage much produce at 60° of phase shift. The phase shift of each amplifier can be written as $60^\circ = tan^{-1}\frac{\omega_{OSC}}{\omega_0}$ where solving for ω_{OSC} the we have $\omega_{OSC}=\sqrt{3}\omega_0$.

The minimum gain requirement for each stage is $H(s) = 1$. We can write the total gain as $-\frac{A_0^3}{(1+\frac{s}{\omega_0})^3} = 1$. Solving the gain equation using $\omega_{OSC}=\sqrt{3}\omega_0$, we can find $A_0 = 2$.

The ring oscillator oscillates at frequency of $2\pi\sqrt{3}\omega_0$, which 3-dB bandwidth of each stage is ω_0 while each stage must have a minimum gain of 2. Adding more stages will result in lower gain per stage but oscillation frequency will decrease. Even though the ring oscillator will have a compact layout design, the phase noise will be worse since each stage will require a capacitor and resistor in order to manipulate the delay of each stage to adjust the frequency. [17] Illustration of a differential ring oscillator stage is shown in Figure 17. [18] Since the requirement of this design is a high frequency output signal and phase noise is extremely important, the ring oscillator is not a good candidate for our PLL design.

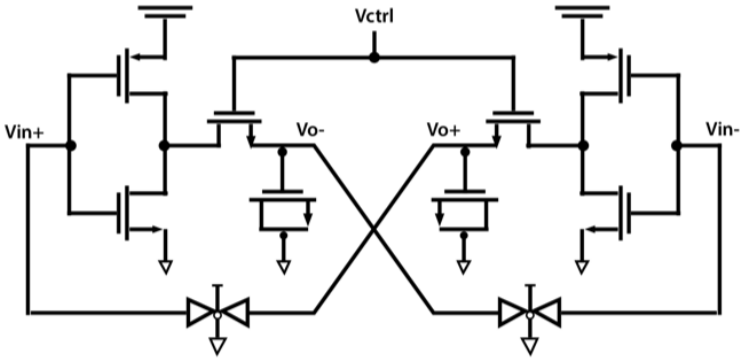


Figure 17: Simple stage design of a Ring Oscillator

2.1.2.2 LC Oscillator

An LC Oscillator design consists of monolithic inductor, capacitor and transistors. The simple circuitry has advantages over ring oscillators in higher frequency. The best way to understand LC voltage oscillators is to look at a simple RLC circuit.

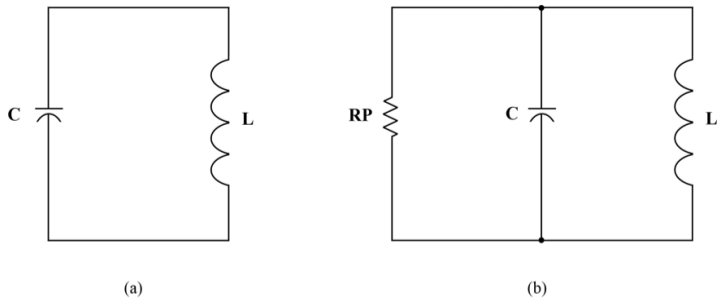


Figure 18: (a) simple LC circuit and (b) simple RLC circuit

In LC circuit in Figure 18(a) , the parallel inductor and capacitor have impedance of

$$Z_L = jL\omega_0$$

$$Z_C = \frac{1}{jC\omega_0}$$

ω_0 = Resonance Frequency

When the impedances of the inductor and capacitor are equal which yields an infinite impedance causing resonance. The frequency resonance can be written as :

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

In practice, capacitor and inductor have parasitic resistance which is illustrated in Figure 18 (b). The RLC circuit defines the tank of the Oscillator and resonant frequency. Knowing the quality factor of the inductor, we can also determine the amount of energy lost in the tank. The quality factor of inductor with parallel parasitic resistance is defined as $Q = \frac{R_P}{\omega L_P}$.

Let's assume the following gain stage with RLC tank:

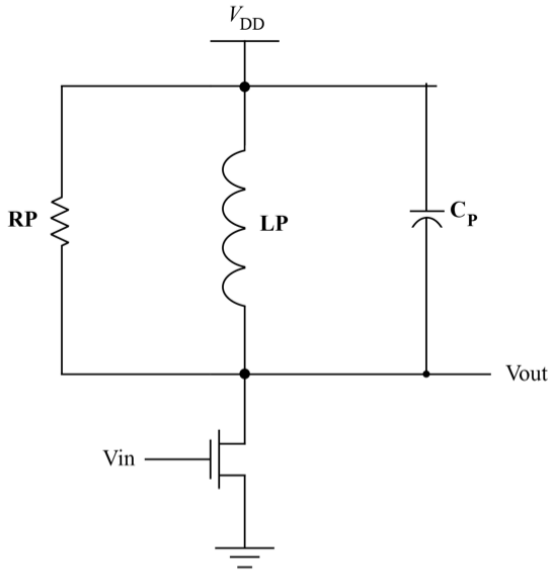


Figure 19: Simple gain stage with RLC tank

The voltage gain at resonance is $-\ gmR_P$. When we feedback the output to become the input of this circuit, the phase shift does not meet the Barkhausen **criteria** since the phase shift will not reach 180° .

Since one stage provides 90° then cascading two gain stages will reach our phase shift requirement, illustrated in Figure 20. The circuit will meet the Barkhausen criteria with large enough gain to oscillate.

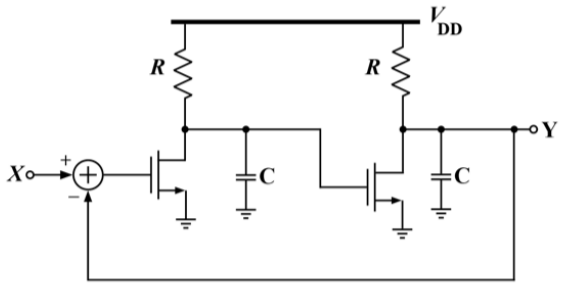


Figure 20 : Two gain stages cascaded

The LC oscillator can be presented in a simpler way, by thinking about an active circuit and lossy resonator. Assume a current impulse applied to a lossless RC circuit shown in Figure 20. The capacitor is charged up by $\frac{I_0}{C_1}$ Volts. Once the capacitor is charged then changes flow to the inductor. The output voltage will fall as charges flow to the inductor and the inductor will have a current of $L_1 \frac{dV_{out}}{dt}$. After the capacitor is empty, inductor current will charge the capacitor in the opposite direction causing the output voltage to reach negative peak. [14] Since there's no loss in the circuit then this energy transfer continues indefinitely.

In practice, the inductor and capacitor will have parasitic resistance therefore the circuit will include a parallel resistor which is shown in Figure 21 (b). This will make the system lossy where as time

passes the amplitude decreases since the resistor burns the capacitor energy as time passes. In order to sustain the oscillation there needs to be addition to the circuit to eliminate the resistance. This process falls *to* the active circuit since it generates negative resistance looking from the drain of the transistor. The addition of active device will be designed to have $-\ R_P$ to ensure oscillation indefinitely.

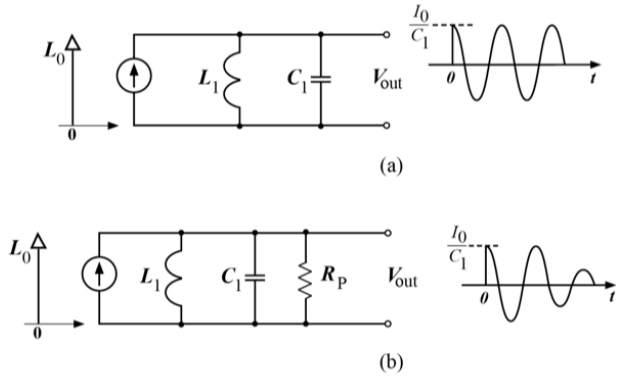


Figure 21 : Ideal and non-ideal resonator

The R_{out} in the feedback can be realized by equation $R_{out} = R_{Active-output}(1 + A\beta)$ if the loop is designed to *provide* positive *feedback* then the $A\beta$ will be a negative number resulting in negative resistance. Figure 22 helps us demonstrate how to calculate the transistor output resistance. The negative resistance can be calculated using a test voltage source, where $V_X = V_1 - V_2$. The I_X can be defined as $I_X = -gm_1V_1 = gm_2V_2$.

Solving for resistance seeing from test voltage

$$\frac{V_X}{I_X} = -\left(\frac{1}{gm_1} + \frac{1}{gm_2}\right) = -\frac{2}{gm}$$

In order to ensure oscillation, parasitic resistance must be canceled by negative resistance of the active part. Assuming parasitic resistance is $2R_P$ then following argument must be true in order for the oscillator to work:

$$2R_P \geq \frac{2}{gm}$$

Hence making the gain to equal to

$$gmR_P \geq 1$$

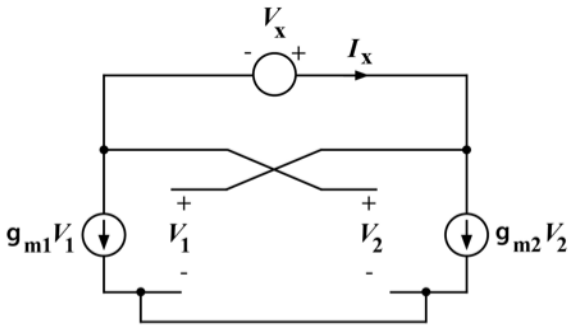


Figure 22: Equivalent circuit of cross-coupled

It is very important to find the transfer function of the voltage controlled oscillator since the input is DC voltage and output is frequency. In oscillator design, as the input which is control voltage changes then the output frequency changes. Looking at Figure 23, it is illustrated voltage change from V_1 to V_2 changes frequency from ω_1 to ω_2. The slope of this line is known to be K_{VCO} which is the gain of the VCO express in unit of $\frac{\frac{rad}{Hz}}{V}$. The output frequency can be defined as the sum of input frequency and VCO gain times control voltage.

$$\omega_{out} = K_{VCO}V_{cont} + \omega_0$$

Throughout the tuning range of the VCO, K_{VCO} must stay constant otherwise VCO maynot be stable. If the input of the VCO which is control voltage changes at a certain time then the output will be changes as well but we can not define total phase as $K_{VCO} \cdot V_{cont}(t) \cdot t$. An integration must be used in order to define the total phase. [14] Total phase can be defined as :

$$\phi(t) = \int_0^t K_{VCO} \cdot V_{cont}(t)\, dt$$

Where taking Laplace would give the transfer function of the VCO:

$$\phi(s) = \frac{1}{s} \cdot K_{VCO} \cdot V_{cont}(s) \rightarrow \frac{\phi(s)}{V_{cont}(s)} = \frac{K_{VCO}}{s}$$

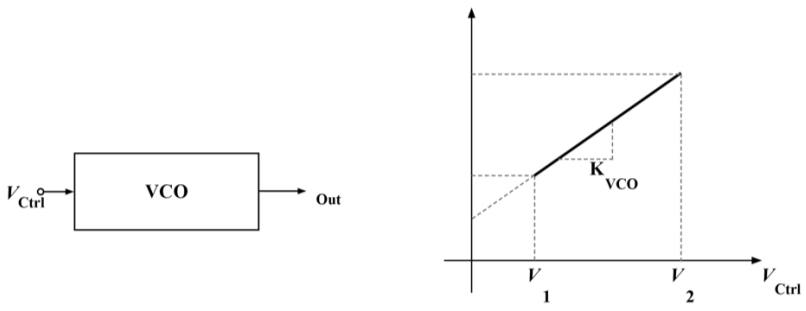


Figure 23: Correlation between input and output of the VCO

In chapter 3, I will present a detailed explanation of designing the LC VCO and my proposed LC VCO design.

2.2 Phase Noise

In electronic circuits, noise and interference affect the circuit's performance, where in an oscillator the phase suffers the most. Types of noise sources include thermal, shot, flicker, supply and

substrate. These types of noise will affect amplitude and phase but since phase noise is more dominant in an oscillator then the amplitude noise is suppressed.

2.2.1 Phase Noise in Time Domain and Frequency Domain

The output of an ideal oscillator is a perfect periodic function in form of $V_{out}(t) = A \cdot cos(\omega_c t)$ where ω_c is oscillation frequency. The zero crossing of the output signal happens at $T_c = \frac{2\pi}{\omega_c}$ where the noise present in the oscillator circuit will disturb zero crossing randomly. This random change can be modeled by $V_{out}(t) = A \cdot cos(\omega_c t + \phi_n(t))$ where the period is changed randomly. This random *change* is called the phase noise, $\phi_n(t)$. The depiction of this random change compared to ideal output is shown in Figure 24. We can see that the frequency changes when the oscillator has noise.

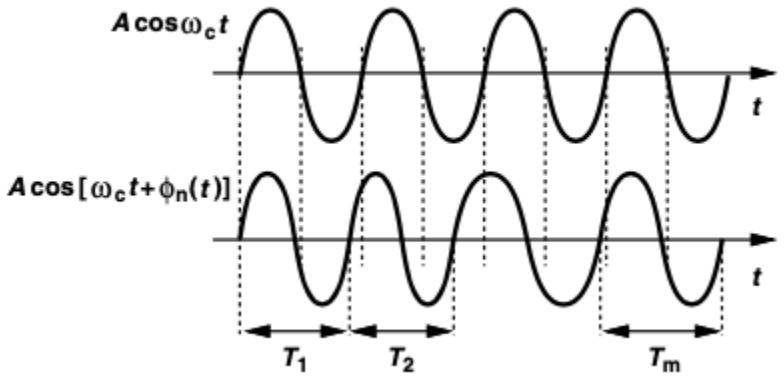


Figure 24: Sinusoidal with and without phase shift

Another view of this could be presented in the Frequency domain. Looking at the spectrum of the output in Figure 25. The ideal oscillator output has an impulse at ω_c where compared to random variation in oscillator, the output deviate from ω_c. Both frequency and amplitude fluctuations cause sidebands shown in Figure 25 (b).

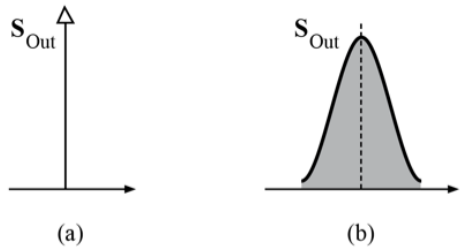


Figure 25: Ideal and non ideal oscillator harmonic

Phase noise can be at a certain offset frequency over a bandwidth of Δω compared to the carrier frequency. Noise power is used in the bandwidth of 1 Hz at an offset divided by carrier power which provides the phase noise at the given offset:

$$L(\Delta\omega) \;=\; 10\,log(\frac{Power\ in\ 1\ Hz\ bandwidth}{Carrier\ Power})\,(\frac{dBc}{Hz})$$

2.2.2 Linear Time Invariant (LTI) Model

One of the well known phase noise models is known as Leeson's Model of Linear Time Invariant. Phase noise of the oscillator is defined as :

$$L(\Delta\omega) \;=\; 10\,log\left[\frac{2FkT}{P_s}\cdot\left[1+(\frac{\omega_0}{2Q_L\Delta\omega})^2\right]\cdot\left[1+\frac{\omega_{1/f^3}}{|\Delta\omega|}\right]\right]$$

F = Oscillator Excess Noise Factor

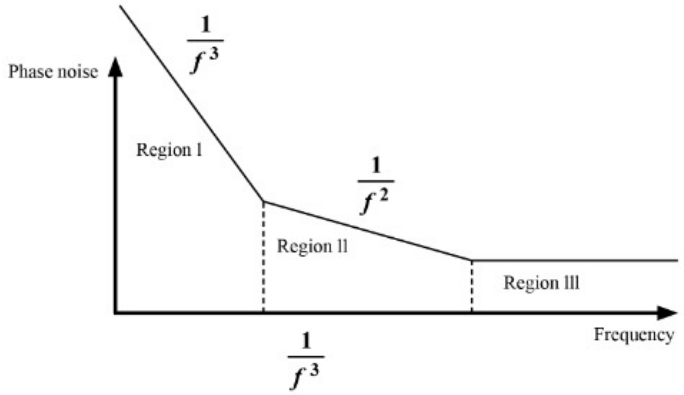
k = Boltzmann’s Constant

T = Absolute Temperature

P_s = Tank Average Power Dissipation

Q_L = Tank Quality Factor

Plot of Lessons phase noise Model can be seen on Plot 1. Plot can be divided into three different regions where the type of noises will affect the phase noise. Region I is the region that is caused by tank noise filtering and low frequency upconversion, also known as thermal noise and flicker noise. This part of the phase noise has a slope of $\frac{1}{f^3}$. Region II is due to tank filtering noise, also known as thermal noise with slope of $\frac{1}{f^2}$. Region III is the noise floor result of buffer noise and measurement equipment noise or the capacitor and inductor series resistances limiting the tank noise. [14]



Plot 1: Lesson's Phase Noise Model plot

2.2.3 Types of Noise in the LC VCO

There are two types of noise that are in the LC VCOs. At low frequency, the drain current noise of the MOSFET is the source of the flicker noise. Flicker noise is generated from oxide near the silicon interface by the random tapping and de-trapping of charges. This fluctuation of charges causes channel carrier density which modulates drain current. [19]

Flicker noise can be modeled as voltage source series with the gate :

$$\overline{V_n^2(f)} = \frac{K}{C_{ox}WL}\frac{1}{f}$$

K = Process-dependent parameter

W = Transistor Width

L = Transistor Length

C_{ox} = Gate Capacitance per unit area

Looking at the voltage source model of flicker noise, we can lower the noise by lowering the W· L. Choosing proper length and width of the transistor while making the VCO to oscillate will help lower phase noise at lower frequency.

The second type of noise in the VCO is the thermal noise which comes from the series resistors of the capacitor and inductor. Vibration of carrier charges in the conductor causes thermal noise. [20] Thermal noise of the resistors can be modeled by voltage source as :

$$\overline{V_n^2(f)} = 4kTR$$

The transistor also has thermal noise from the gate distributed resistance. Thermal noise from the transistor can be modeled as :

$$\overline{V_n^2(f)} = (4kT\gamma g_m)r_0^2$$

k = Boltzmann's Constant

T = Temperature in Kelvin

g_m = Transistor Conductance

For long channels, $\gamma = 2/3$

g_m is the change of drain current over change of gate-source voltage. An approximation of g_m writing it in terms of width and length of the transistor is

$$g_m \sim \frac{W}{L}$$

Transistor thermal noise can be approximated as

$$\overline{V_n^2(f)} = (4kT\gamma\frac{W}{L})r_0^2$$

By lowering width over length ratio, thermal noise will also be lowered affecting the phase noise of the VCO.

2.2.4 VCO Phase Noise in PLL

In order to calculate the phase noise caused from the VCO noise, we must find the transfer function from the ϕ_{VCO} where the noise is introduced to the output, ϕ_{Out}. In Figure 26, the input to output in the PLL is depicted where $\phi_{in} = 0$ since we want to know the effect of noise from VCO.

$$\frac{\phi_{Out}}{\phi_{VCO}} = \frac{1}{1+\frac{I_p}{2\pi}(R_1+\frac{1}{C_1 S})\frac{K_{VCO}}{S}}$$

$$Phase\ Noise\ at\ the\ Output = \left|\frac{\phi_{Out}}{\phi_{VCO}}\right|^2 \times VCO\ Noise$$

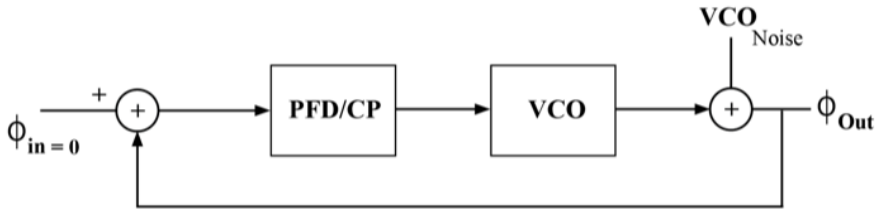


Figure 26 : VCO Noise referred to the output

3 Proposed Voltage-Control Oscillator

3.1 Voltage-controlled Oscillator Considerations and Requirements

This specific 6.84 GHz VCO design is for a Sub-sampling Phase Lock Loop where the AoSense company desires a specific phase noise and power consumption. The total power consumption of the SSPLL is budgeted to be 10mW where 3mW is designated to the VCO. Based on the matlab simulation shown on Plot 1, the VCO Phase Noise at 1 MHz offset must be less than -110 dBc/Hz, otherwise the SSPLL will not meet phase noise requirement. The rest of the requirements can be seen in Table 1.

Table 1: VCO Design Requirements

VCO Design Parameters	**Requirement**
Oscillation Frequency	6.84 GHz
Tuning Range	14 %
Voltage Swing	1.2V
Phase Noise @ 1MHz	Less than -110 dBc/Hz
Supply Voltage	0.6 to 1.2 V
Power Consumption	Under 3mW

3.2 LC Tank Design

There are three considerations that must be considered in designing the tank. The first consideration is that the inductor and capacitor size must be chosen to ensure resonance at the desired frequency.

The resonance frequency is given by:

$$\omega = \frac{1}{\sqrt{LC}}$$

The L and C tank will produce a parasitic resistance which can be modeled as a parallel resistor Rp. In order to enable oscillation in the circuit, we must ensure that the resistance Rp is large enough to set the loop gain of our circuit greater or equal to 1. The equation of this criteria is shown below-

$$gmR_P \geq 1$$

In Chapter 2.1.2.2, the minimum gain was defined to be 1. Gain of 1 may not be sufficient for the VCO to oscillate. The gain is safe to be between 1.5-3 to ensure oscillation. [21]

$$gm \cdot R_p = gain \rightarrow gm = \frac{gain}{\omega QL}$$

The next consideration would be the phase noise contribution of the tank. Increasing the quality factor will lower the phase noise in the VCO which is illustrated with the Lessons phase noise model of the VCO. [14] Note that the Q factor of the tank is dominated by the Q factor of the inductor, hence Q_L in the equation below.

$$L(\Delta\omega) = 10\, log\left[\frac{2FkT}{P_s} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right] \cdot \left[1 + \frac{\omega_{1/f^3}}{|\Delta\omega|}\right]\right]$$

Power consumption will be determined by the tank conductance. The relationship between conductance and RLC values of the tank is shown in the equation below. Note that larger L and lower C

values correlate to lower conductance and therefore a lower power consumption. Larger quality factors will also correlate to lower power consumption.

$$G_{tank} = \frac{1}{\omega_0 L}\left(\frac{1}{Q_L} + \frac{1}{Q_L}\right) = \frac{R_L}{(\omega_0 L)^2} + 2R_C(\omega_0 C)^2$$

When designing the tank, we must ensure the multiple of L and C combine to produce the frequency desired. From there we must ensure that the ratio of LC is shifted to allow Rp (primarily determined by L) to be large enough to meet the criteria of oscillation. From here increasing the ratio of L/C can be played with to tune PN and power consumption.

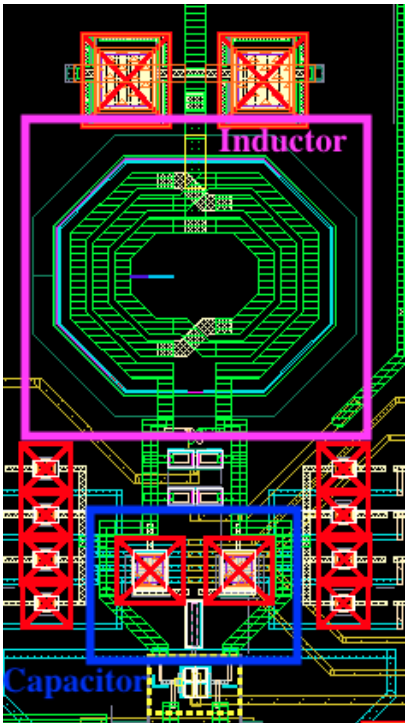


Figure 27: Layout design of the Tank

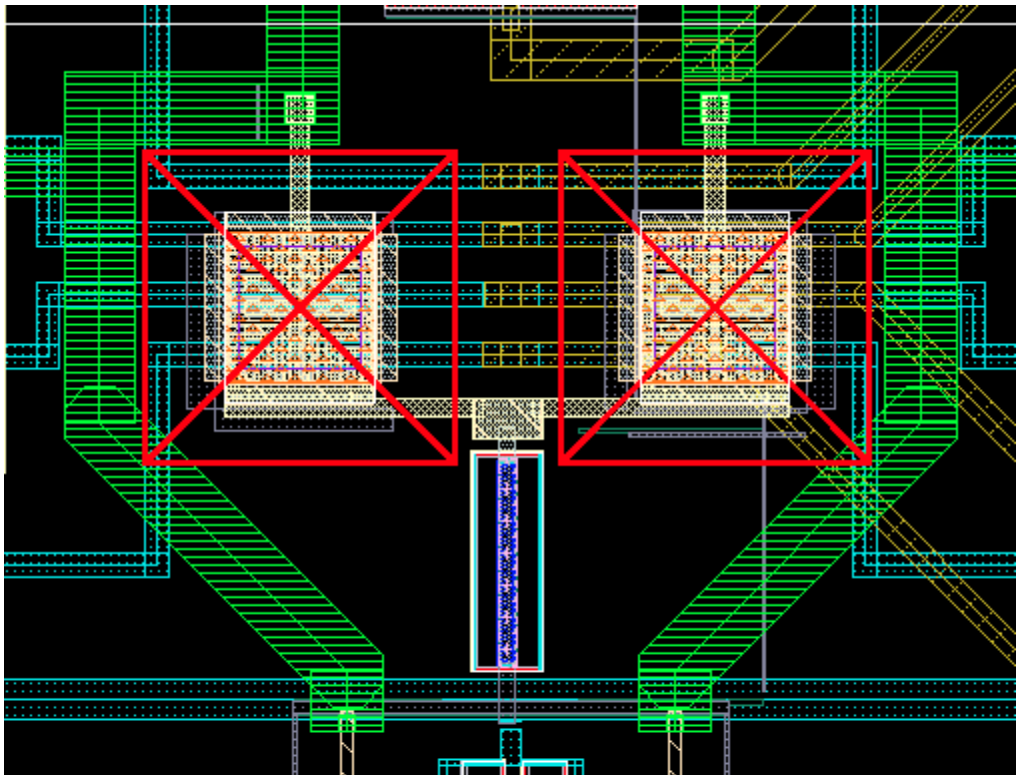


Figure 28: Layout of the capacitor for the proposed VCO

The inductor and capacitor layout tank connection shown on Figures 27 and 28 respectively, is designed to have the shortest wire connection.

3.3 Design of the Cross coupled Transistors

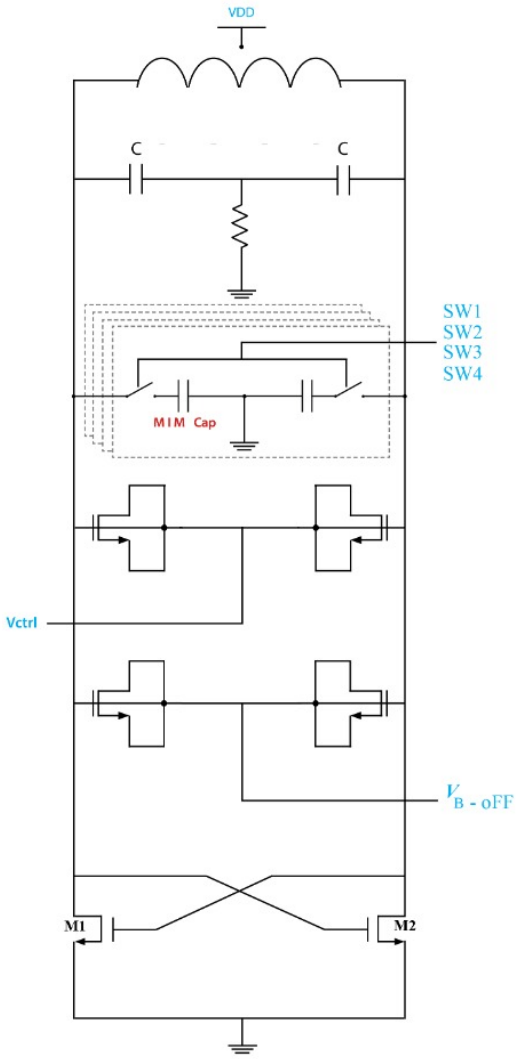
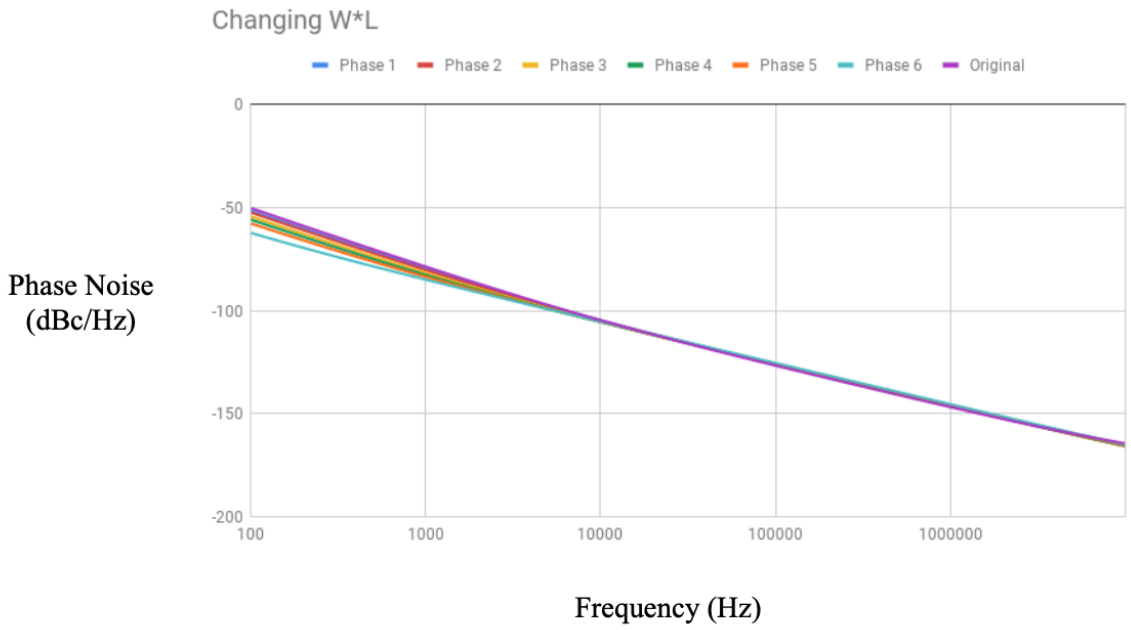


Figure 29: Proposed LC VCO Design

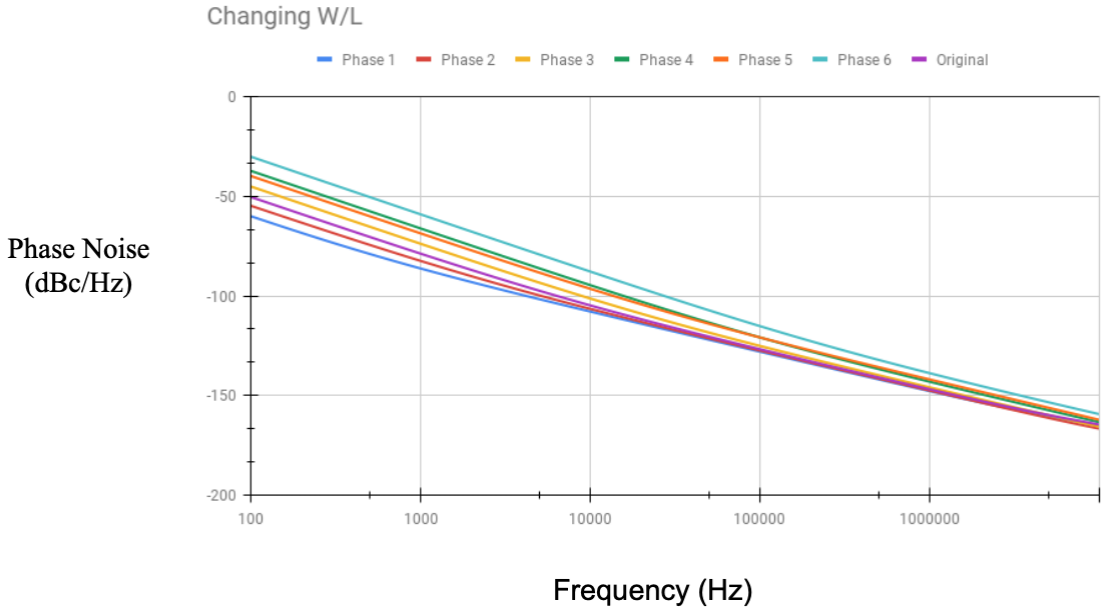
In order to design the cross coupled transistor, the gm must be large enough to ensure $gmR_P \geq 1$. In order to lower the flicker noise and thermal noise coming from the transistor ratio of $\frac{W}{L}$ and multiplication of $W \cdot L$ must be optimized. Variation of $W \cdot L$ determines the flicker noise of the transistors which contribute to the total phase noise of the circuit. Plot 1 shows the variation of $W \cdot L$

and its effect on the total phase noise of the circuit. The simulation in this plot was done while keeping $\frac{W}{L}$ ratio constant.

In order to find the best $\frac{W}{L}$ ratio for minimizing thermal noise of the transistors the multiple of $W \cdot L$ was kept constant while varying $\frac{W}{L}$ ratio. Plot 2 shows the effect of varying W/L on total phase noise of our circuit. These simulations were used for optimizing the phase noise contributions of our transistors in the design.



Plot 2: Phase noise for variation of $W \cdot L$ while keeping $\frac{W}{L}$ ratio constant



Plot 3: Phase noise for variation of $\frac{W}{L}$ while keeping $W \cdot L$ constant

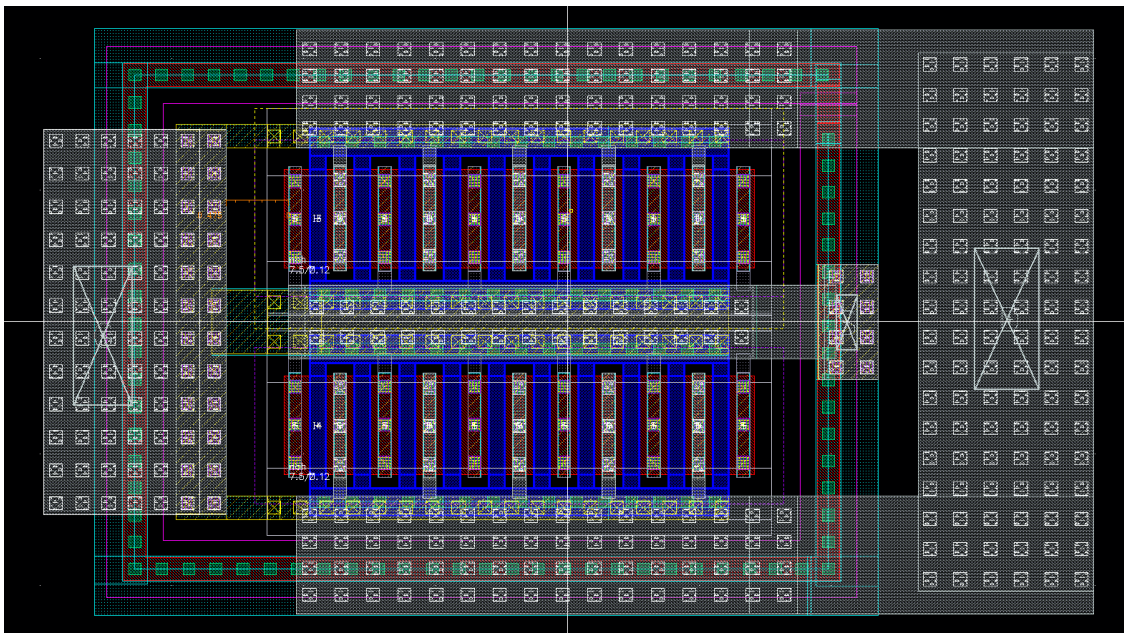


Figure 30: NMOS transistor design for Cross-Couple

The layout technique of using fingers helps us to lower this resistance and making sure the gate receives proper voltage throughout the gate sheet. In the long gate sheet, we can see that the voltages will be different as it passes through the gate. Adding fingers to the transistor will allow gates to parallel while having lower resistance thus lowering the overall gate resistance. If a long gate is used, then some parts of the transistor will be permanently damaged since some parts will have higher voltage than other locations of the gate sheet. The number of fingers was chosen to be 10 which was chosen by simulation of different numbers of fingers. The Ten fingers provide the best phase noise for this transistor size.

The next consideration was adding a multiplier. Assume the transistor has a large current incoming which some technologies can only handle certain currents. Adding a multiplier will make the transistors parallel which means they have the same voltage but the current going to each will be less. With the layout consideration, a large amount of current will not go through the gate damaging it.

For the cross-couple connection, the high metal levels were chosen to ensure lower capacitance between the ground and the metal due to their high distance. Metal 8 and Metal 7 were chosen to make the connection since Metal 9 was used to connect each stage. Layout connection in Figure 31. The cross-couple design must be symmetrical to ensure that both transistors receive the same signals to ensure proper operation. This way there will be no mismatch and if there's process variation they will be close enough that both transistors will be affected. After making the cross-coupled connection, the wires including metal 9 connection were EM simulated (Figure 32) to make the simulation as realistic as possible.

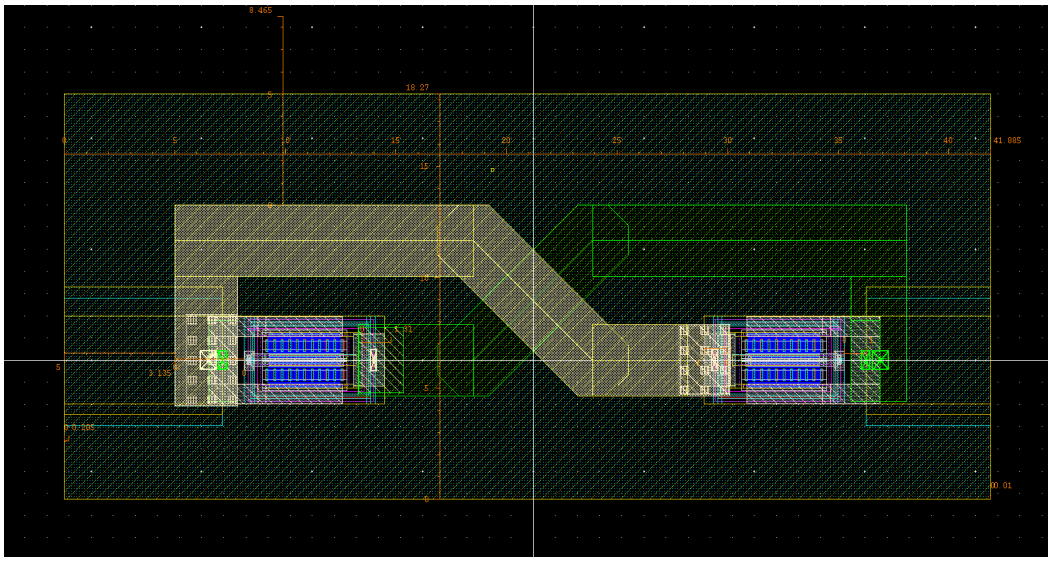


Figure 31:Cross-coupled transistor layout connection with ground layer for EM simulation purpose

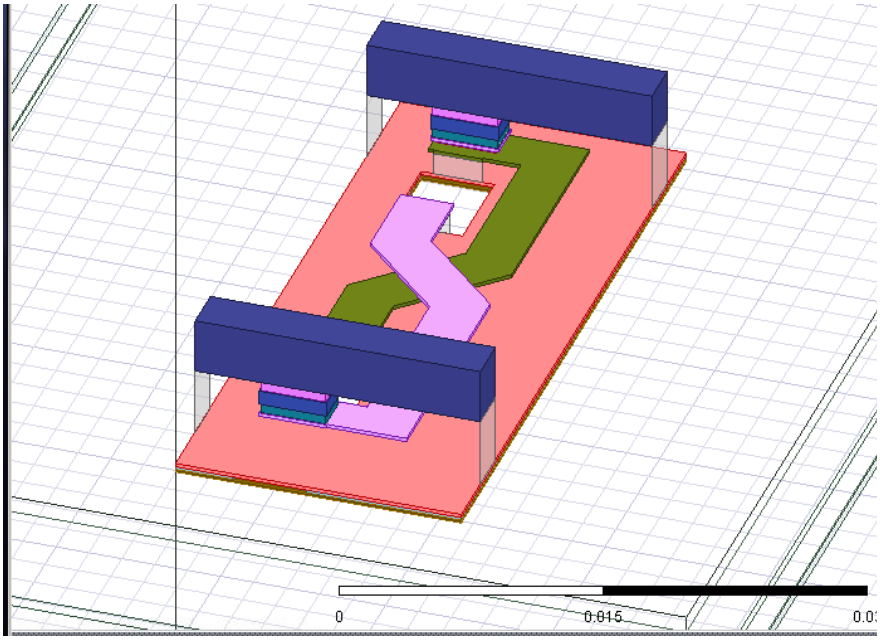


Figure 32: EM Model of the cross-coupled including metal 9 connection

The cross-coupled transistor was placed as close as possible to the inductor to lower the distance that it takes the signal to get to the transistors to lower any mismatch and resistance. Inductor and

cross-couple connection shown in Figure 31. Thick metal 9 was chosen to make the wiring connection to minimize wiring resistance.

3.4 Tuning Range Considerations

The varactor design was accomplished by using MOS varactors. MOS-based varactors have gained popularity in the industry due to their high Q and wider tuning range. Phase noise is lower in MOS varactors due to their high doping levels in silicon which results in lower resistive loss. Since the inductor and capacitor were chosen to resonate at 6.84 GHz, we can make part of the capacitance as a varactor in order to change the frequency.

$$\omega_0 = \frac{1}{\sqrt{L(C_{Fix}+C_{Var})}}$$

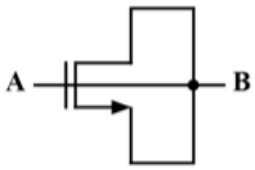


Figure 33: NMOS Varactor Design

The MOS capacitor is achieved by connecting the drain, source and body tied together to make a variable capacitance (Figure 33) that will be between source and gate. MOS Varactors have four regions of operations based on the voltage drop between A and B. The regions include accumulation, depletion, weak inversion and strong inversion which is shown in Figure 34.

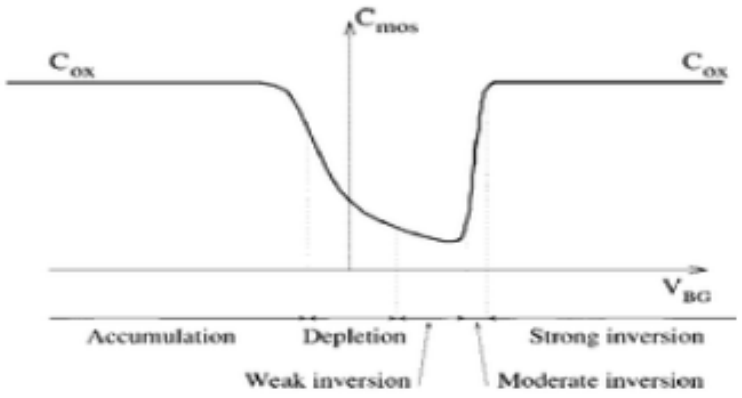


Figure 34 : MOS varactor regions

The MOS varactors are designed in accumulation and strong inversion regions. Studies have shown that strong-inversion provides lower phase noise and lower power consumption since it has lower parasitic resistance. It is realized from Figure 34 that the capacitance is voltage-dependent. [23]

The capacitance in accumulation mode and strong inversion is measured as [24]:

$$C_{ox} = \frac{\varepsilon_{ox} S}{t_{ox}}$$

t_{ox} = Oxide thickness, ε_{ox} =Dielectric constant of oxide, S = Transistor channel area

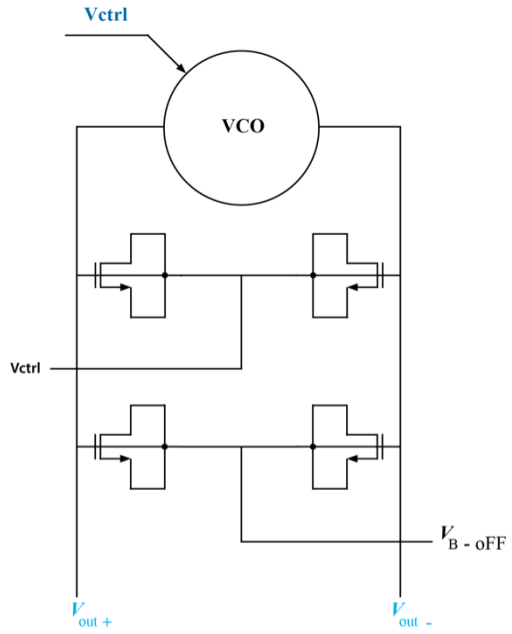


Figure 35: NMOS Varactor circuit for the proposed VCO

Using cadence simulation, the varactor size was designed to have a 250MHz tuning range with variation of control voltage from 0 to 1 V. Two MOS varactors are added with the control voltage in the middle to make sure the circuit is symmetric (Figure 35). In order to have more tuning capability, another varactor was designed where its voltage could be changed manually. Another tuning from off-chip has been added as a switching cap shown below in order to create tuning bands to have an almost 1 GHz of tuning range. By taking away from the fixed capacitance, these switching capacitances were designed. The middle band is the tuning band designed for the VCO is to be set at 6.84 GHz. Each switching cap configuration is as shown in Figure 36, the Vcont tuning range of the VCO is designed to be more than 226 MHz to ensure the frequency tuning is continuous between different SC configurations. In addition, as the temperature increases, the frequency of the VCO goes down. When the temperature changes from -50 °C to 50 °C, the maximum frequency variation due to the temperature variation is less than 40MHz. By using the SC circuit, the free-running frequency of the VCO can be changed continuously from

6.41GHz to 7.38GHz, which should be enough to compensate for the frequency variations due to the PVT.

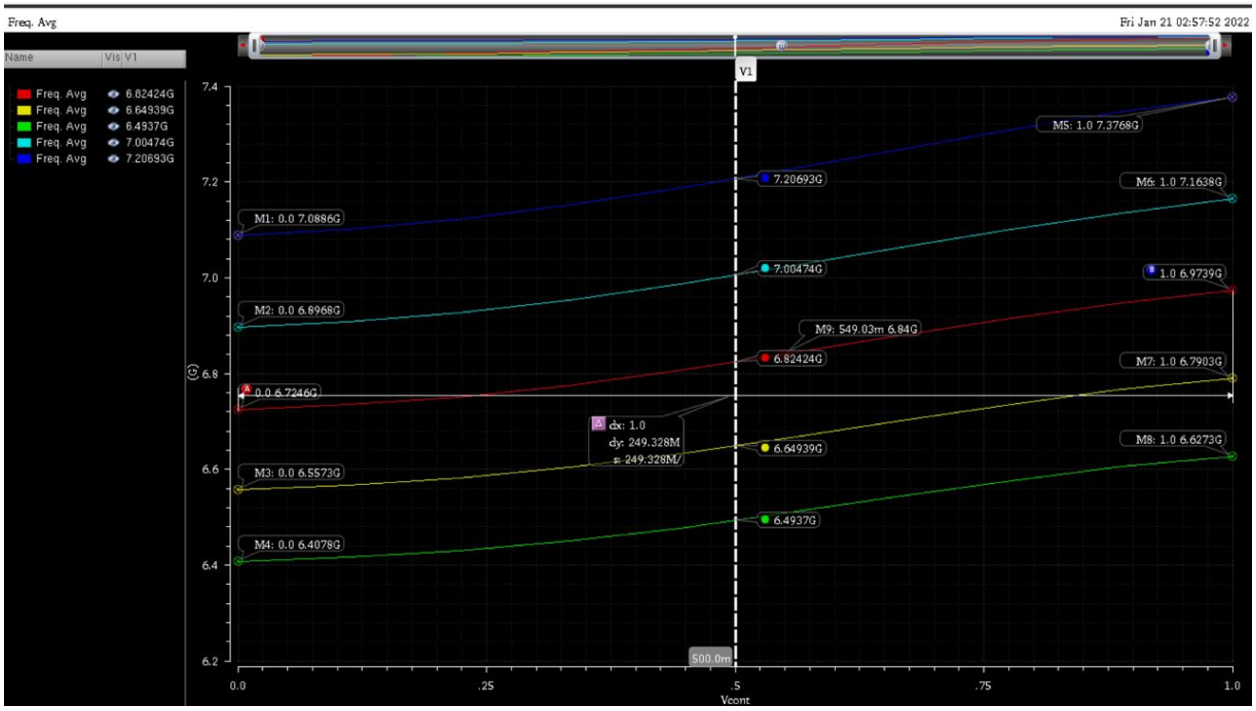


Figure 36: Switching cap bands for the proposed VCO

The layout of the varactors was designed to be as symmetric as possible with 2 fingers on each side to lower the parasitic resistance of the gates. The switch capacitance was also designed to be as symmetric as possible and the voltage connection to turn on the transistors was placed exactly in the middle of the wires to make sure both switches receive voltage at the same time. Metals 1 and 2 were used for the voltage connection since they are under the ground metals 3 and 4. This way the signals and DC wires are separated in order not to affect each other. The varactor layout design can be seen in Figure 37 and the switch caps can be seen on Figures 38 and 39.

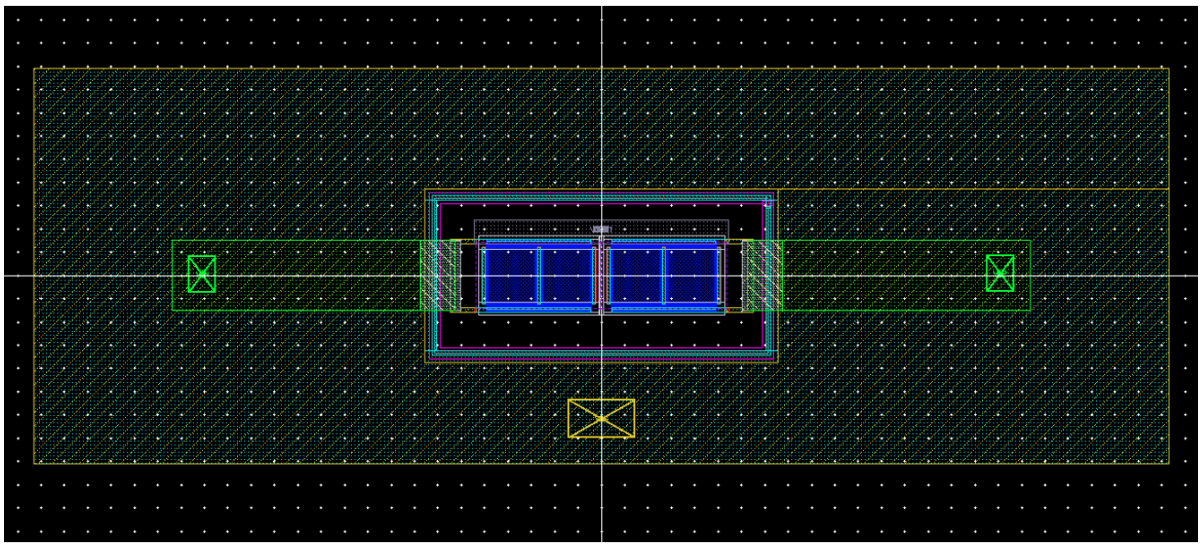


Figure 37: NMOS varactor Layout design

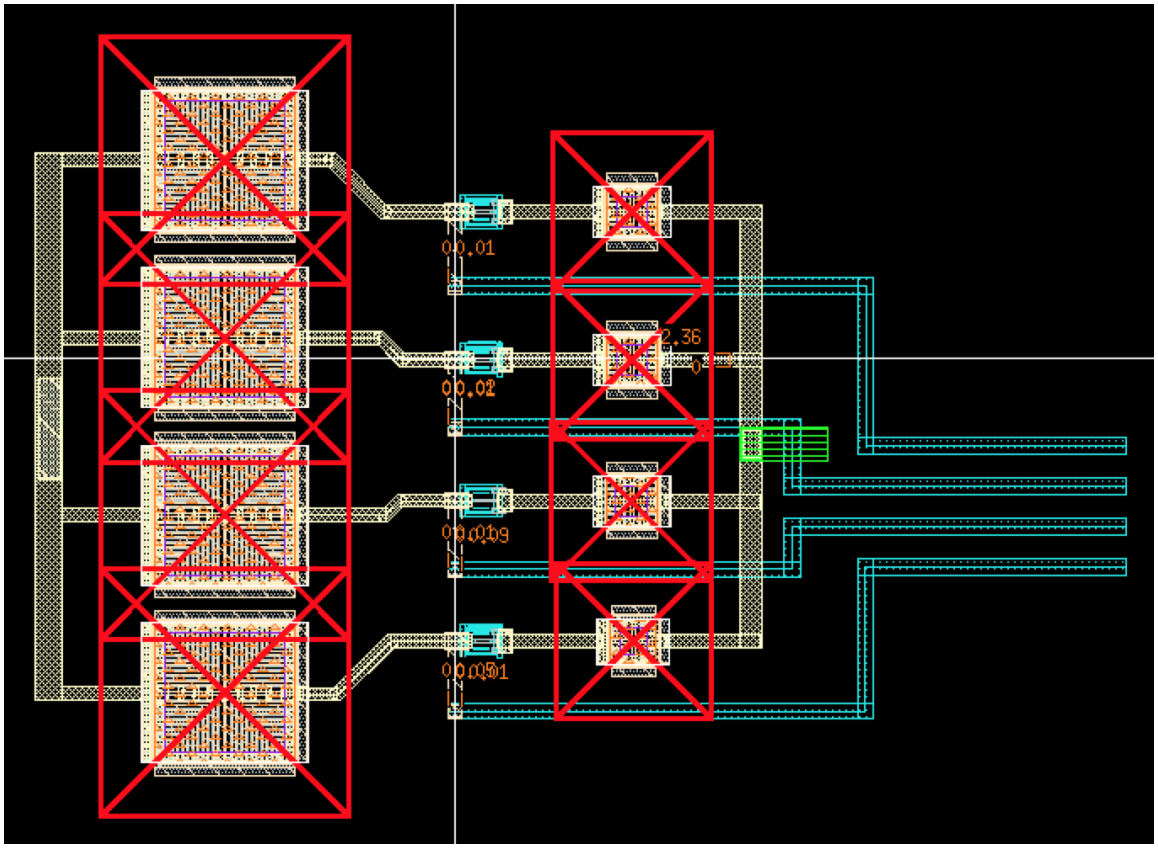


Figure 38:Single side of the switch-cap Design

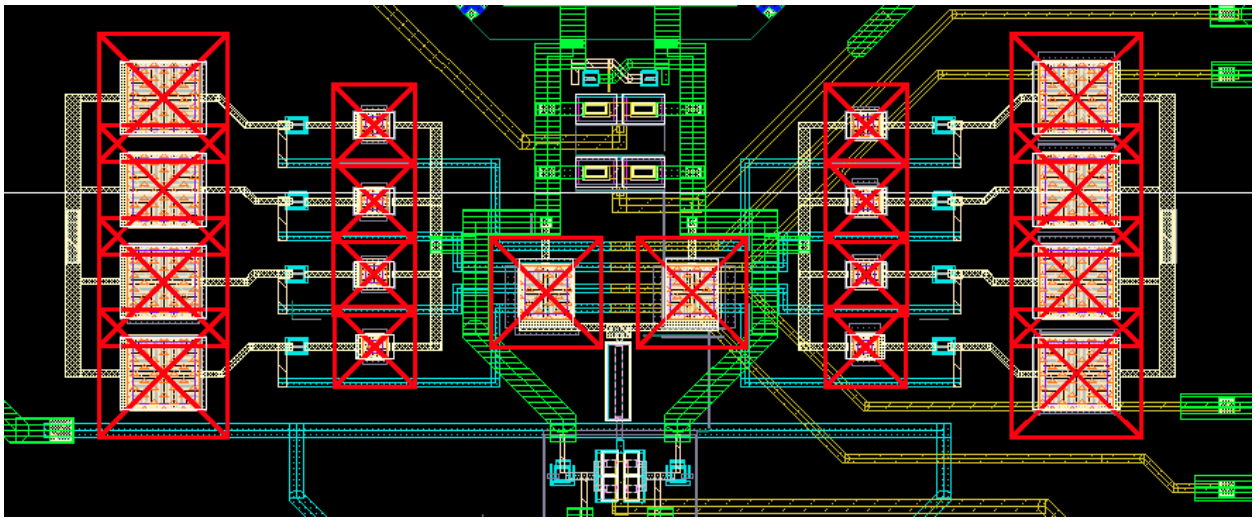


Figure 39: Overall connection of the VCO Tank Capacitance

In order to make the best, realistic model from the layout, the wire connection between the active part of the tank to the first buffer was EM modeled and included in the circuit simulation (Figure 40).

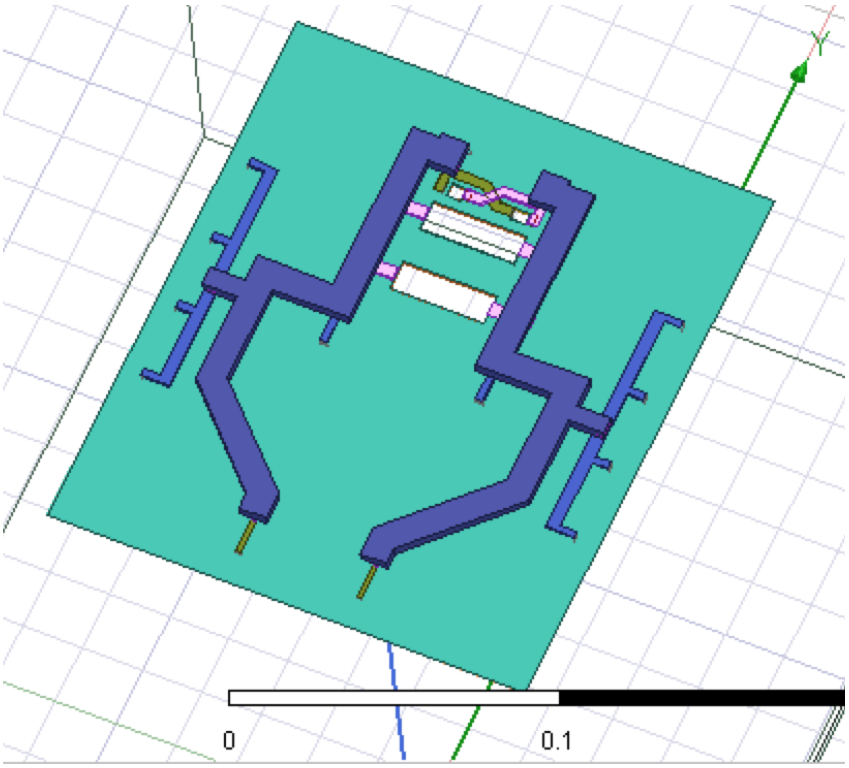


Figure 40: EM Model of the VCO wire connection

3.5 Phase Noise

In order to know the best phase noise at 1 MHz, ideal elements were used for the proposed VCO at which the best phase noise was found to be -119.2 dBc/Hz. Compared to simulated phase noise without any caliber files and EM models, the phase noise is found to be -116.3 dBc/Hz, shown in Figure 41.

Figure 41: Phase noise of ideal and schematic level

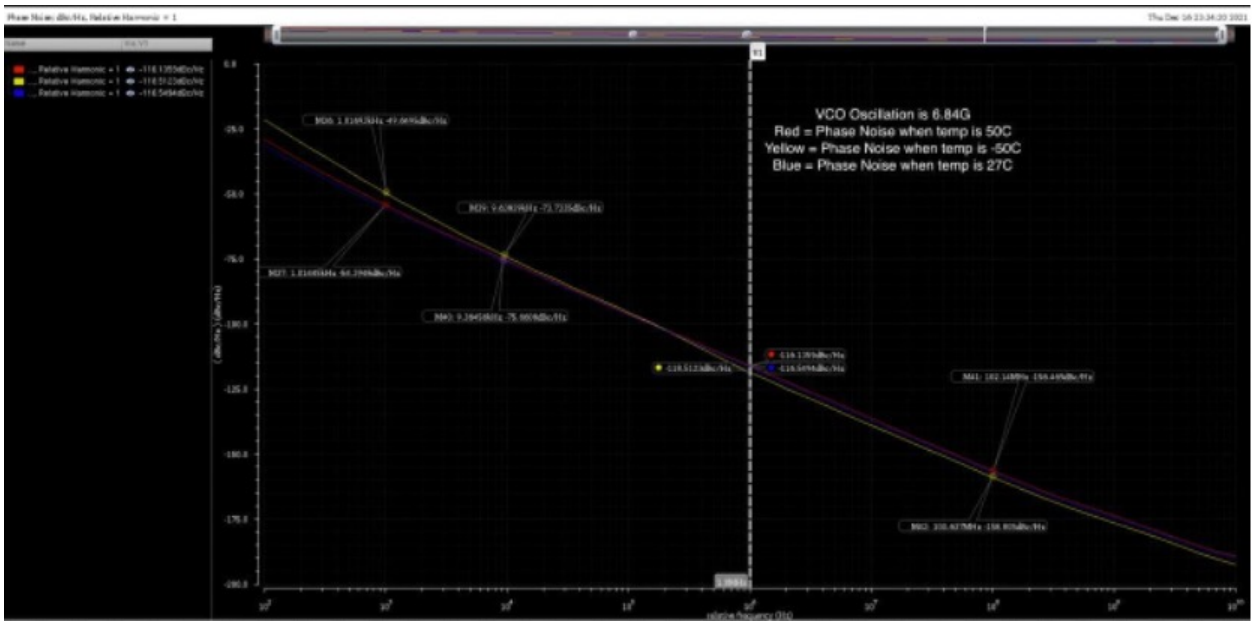


Figure 42: Phase Noise of the VCO at different temperatures

Figure 42 shows the simulated phase noise of the free-running VCO under different temperature conditions and configurations. The variation of the phase noise is 2.5-dB at 1MHz frequency offset, and the worst case of the phase noise can still meet the design requirements.

3.6 VCO Isolation Considerations

The output of the VCO will need to be connected to three different blocks including FLL Loop, Output Probe and SSPD. VCO must be isolated so none of these circuits will affect the operation of the VCO. The first buffer was designed right after the VCO to isolate the output connected to other circuits. Then a buffer for each connection was designed to further isolate the signals. The VCO included four different buffers in order to make sure the operation of the VCO is not affected by other circuits in the SSPLL . The three buffers connected to the VCO can be seen in Figure 43.

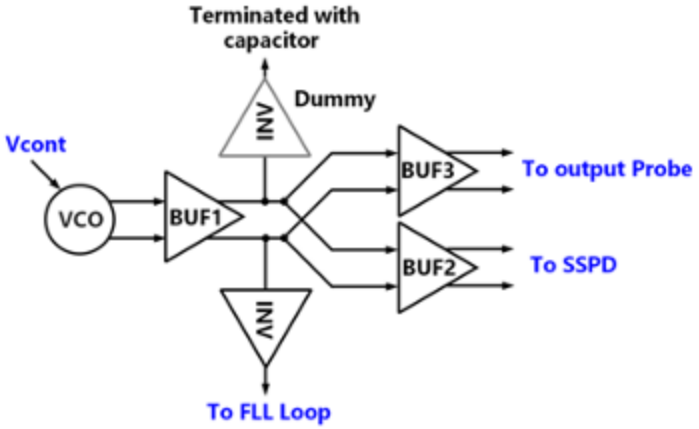


Figure 43: Buffer designs for the VCO

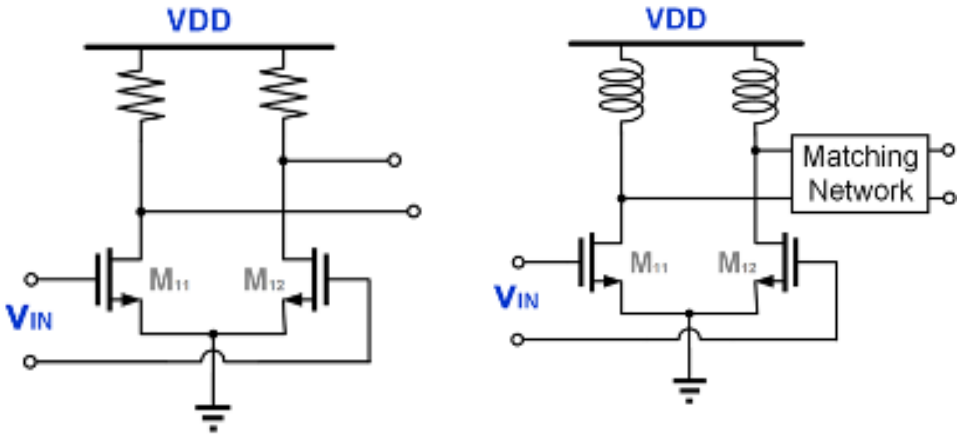


Figure 44: CS amplifier with resistor load for SSPD and CS amplifier with inductive load for test probe

Differential common source amplifiers were used for SSPD and test probes. Average voltage for the SSPD must be 580mV thus providing enough voltage for the SSPD. For the probe buffer, the output must be matched to 50 ohms since an SMA will be connected.

3.7 Chip Layout

The Stand Alone VCO was laid out as shown in Figure 45. The two inductors were placed as far apart from each other in order to make sure they do not couple. The DC voltages were placed in such a way that required minimum wiring length. The DC wires from the VCO were placed on metal 1 and 2 which is under the ground level metal 3 and 4 to separate it from signal wires in the VCO. Once they are far from VCO signal wires then metal 9 was used to connect to the pads to be wire bonded. The overall chip design included stand alone VCO on one side and the SSPLL with the VCO on the left side of the chip. The size of the designed chip was 3mm by 1.21 mm.

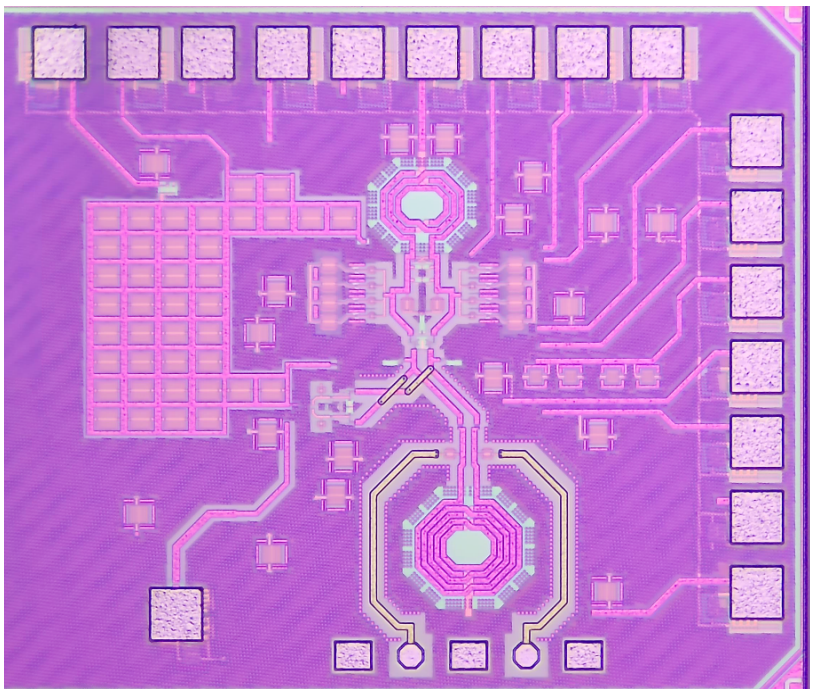


Figure 45: Stand Alone VCO Fabricated Chip

In order to make the most accurate model of the VCO, all the wire connections including the 1st stage buffer connected to the other 3 buffers were EM simulated. The load wire connection was EM simulated as well shown in Figure 46.

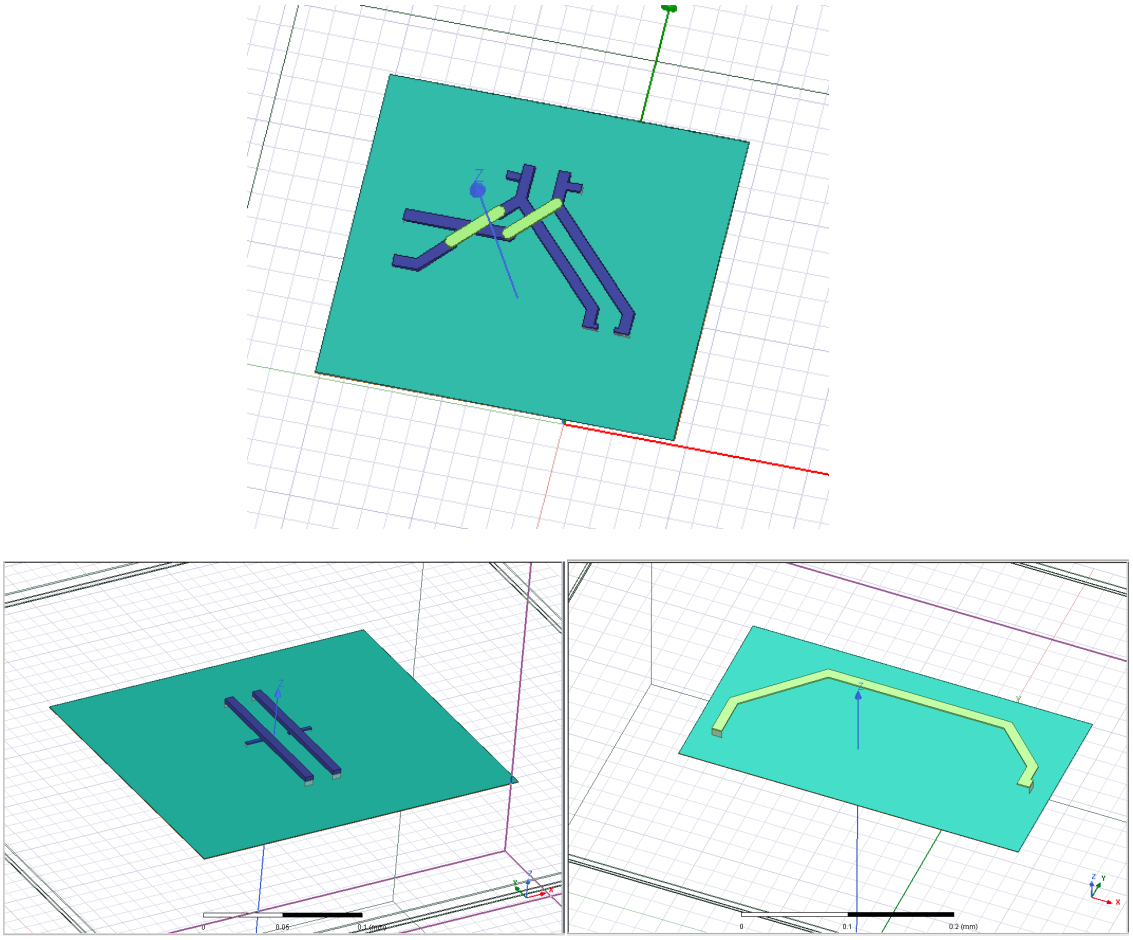


Figure 46: EM Simulations of the wires in the VCO Design

3.8 Chip Measurement

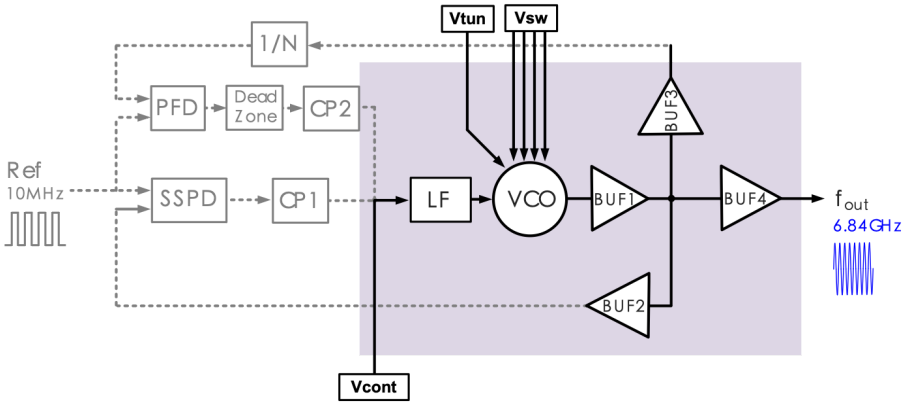


Figure 47: Stand alone VCO Measurement setup

The stand alone VCO design measurement requires only DC voltages that were set in the simulation. The measurement schematic setup is shown in Figure 47. Since the output of the VCO is differential, one port is terminated in 50 ohms, and the other is connected to the spectrum analyzer. The analyzer is set to measure output power, tuning range, and phase noise of the VCO at 6.84 GHz.

When performing the VCO standalone test we measured an increase in VCO output frequency compared to simulation values. This increase in output frequency was corrected by setting VB_OFF to 0v, which isolates one of our varactors from the circuit. The tuning range is shown in plot 5 for two different chip tests.

In Plot 4, we can see the output power of the VCO at 6.84 GHz is -17.75 dBm. If the voltage of the 1st stage buffer VDD is changed, the output power will increase as shown in plot 6. The phase noise of the VCO is also measured as shown in Plot 7. This is the best phase noise measured from the VCO due to the use of low-dropout regulators which lower supply noise.

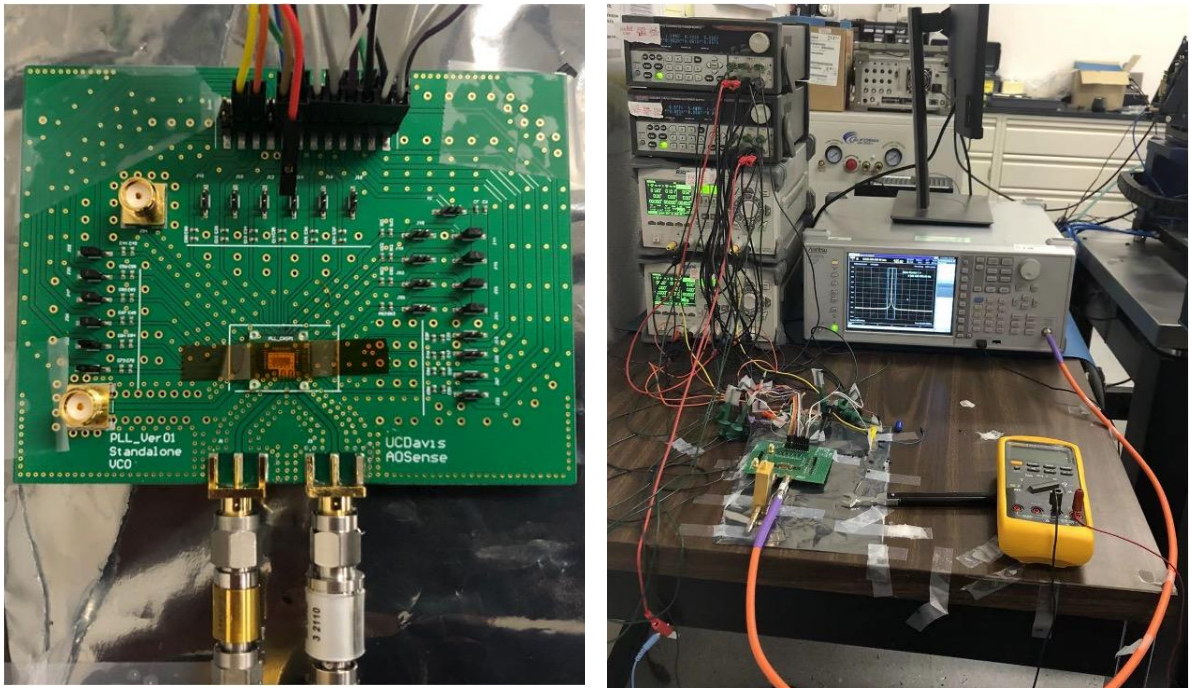
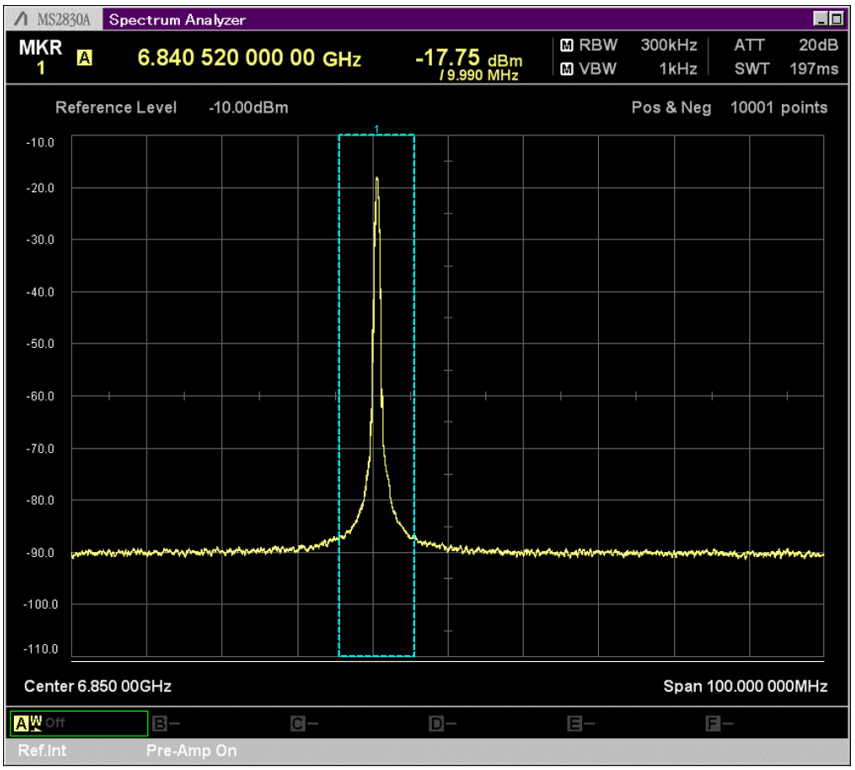
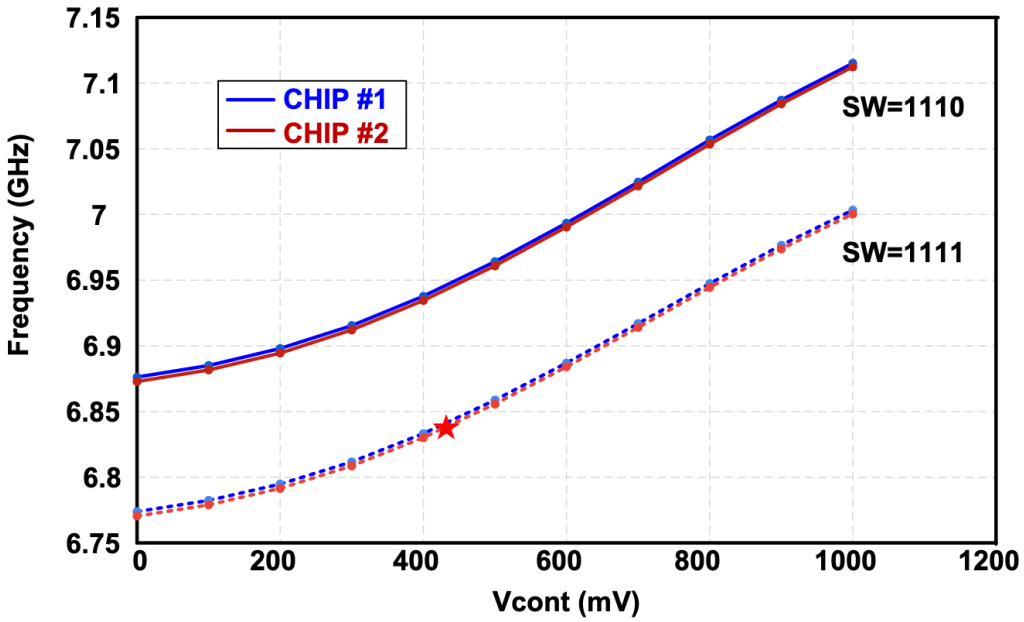


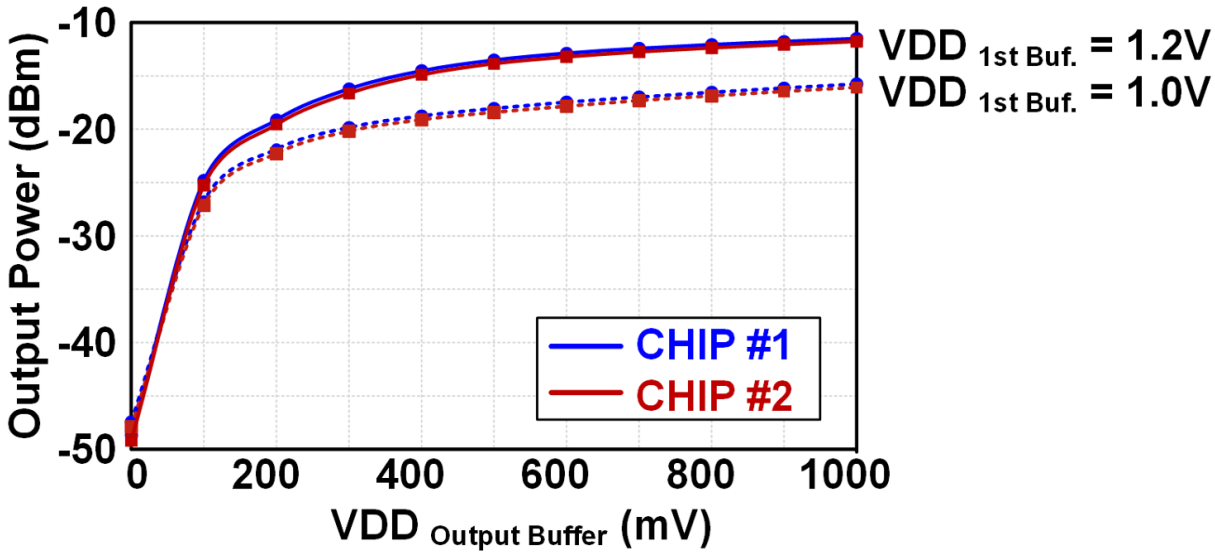
Figure 48: Chip wire bonded to the PCB and measurement setup for standalone VCO



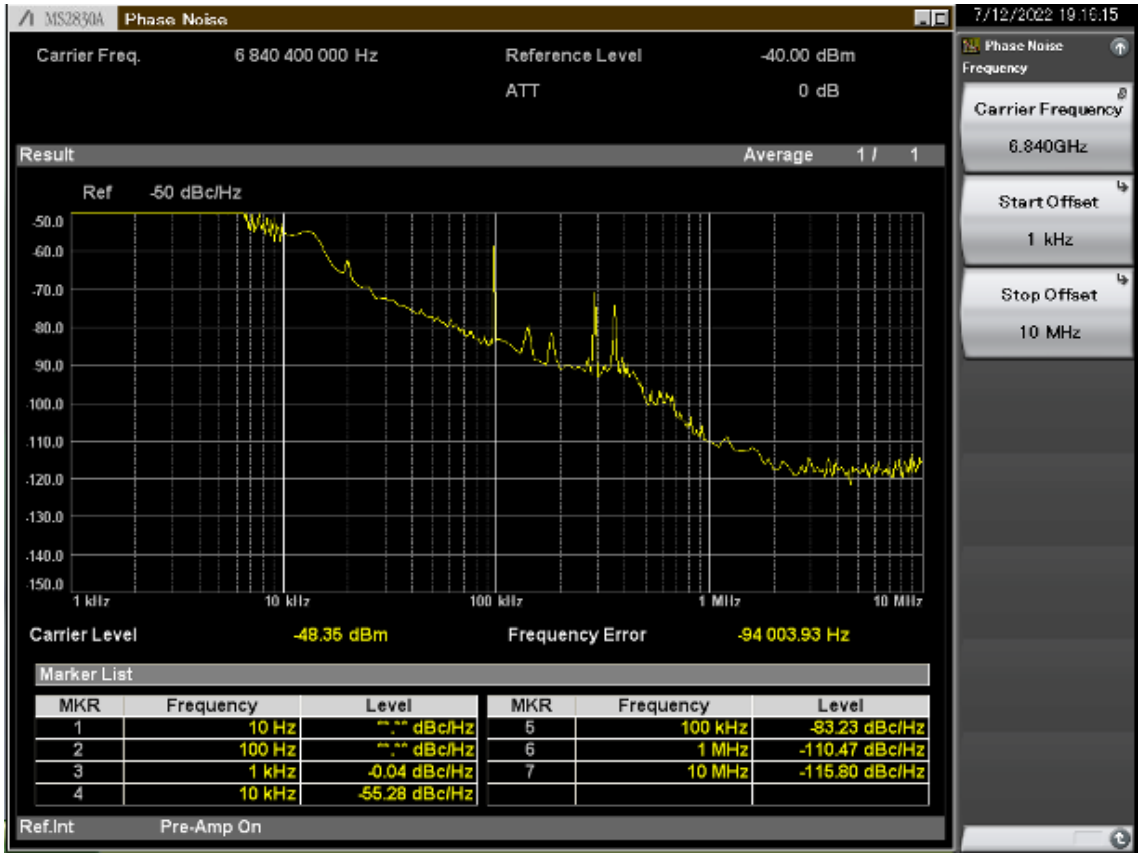
Plot 4 : Output spectrum of the Stand-alone VCO



Plot 5: Measured two tuning range bands of the Stand-alone VCO



Plot 6: Measurement of Output power of the Stand-Alone VCO while changing Load buffer VDD



Plot 7: Phase Noise Measurement of the Stand-Alone VCO

4 Conclusion

Table 2: Comparison of LC VCO Designs

Reference	Tech.	Freq. (GHz)	Tuning Range	Phase Noise @ 1MHz (dBc/Hz)	Supply Voltage (V)	VCO Power Consumption (mW)
This Work	65 nm	6.84	13.5%	-110.47	0.58	3
[24]	65 nm	6.67	28.80%	-109.7	1.2	20.4
[25]	65 nm	5.71	22.40%	-113.7	0.6	0.42
[26]	65 nm	3.3	18.20%	-114	1.2	0.72
[27]	130 nm	6.98	NA	-108.1	NA	3.4
[28]	65 nm	6.6	17%	-116.7	1.2	16.4
[29]	65 nm	3.2	78%	-103.2	1.2	7.25
[30]	90 nm	5.8	45%	-108.5	1.6	14

Table 3: Simulation vs Chip measurement data for the proposed VCO

VCO Design Parameters	Simulation	Measured
Oscillation Frequency	6.84 GHz	6.84 GHz
Tuning Range	14.2%	13.5 %
Phase Noise	-115 dBc/Hz	-110.47 dBc/Hz
Supply Voltage	580 mV	550 mV
Power Consumption	2.99mW	3mW

In modern communication systems, VCO is an important building block specially in PLL design. This thesis discussed an overview of PLL design with VCO design. An integrated LC VCO was successfully implemented in TSMC CMOS 65nm technology. Simulation values of the design were compared to measurement data. The design provides a tuning range of 1 GHz, a phase noise of -110 dBc/Hz at 1 MHz offset and consumpt 3mW power. This proposed VCO does not use a tail current to set the drain currents of the transistors. Comparing different designs of LC VCO shown on table 2, there could be some improvements made in the design. Power consumption and tuning range could be

improved in this design which will also further improve the phase noise. Comparing the simulation and measured result, we can see the phase noise has dropped due to the process variation and not careful modeling of the inductor. This also affected the tuning bands shown in Plot 5. Having the proper model for the inductor and capacitor chosen in the LC VCO design will make sure the frequency is set where it was designed in the tuning range and the band. In future work, the inductors must be EM simulated to provide the fully correct model in the simulation to tune capacitors. To improve the device, a self adjusted active resistor (SAAR) can also be employed to lower the power consumption and further improve the phase noise of the VCO design. [25] PMOS varactors will also be further tested since they provide noise contributions. Overall, the proposed LC VCO design meets the requirement for the PLL application and is found to be locked at the desired frequency.

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