UNIVERSITY OF CALIFORNIA,
IRVINE

Toward Future Brain-Computer Interface: Concurrent Neural Signal Acquisition and Brain Stimulation in CMOS

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical and Computer Engineering

by

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2023

DEDICATION

To my family.

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ABSTRACT OF THE DISSERTATION

Toward Future Brain-Computer Interface: Concurrent Neural Signal Acquisition and Brain Stimulation in CMOS

By

Haoran Pu

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Irvine, 2023

Professor Payam Heydari, Chair

Most people living with spinal cord injury (SCI) suffer from paralysis and loss of sensation below the level of injury. Brain-computer interfaces (BCIs) are a promising approach to addressing SCI and other neurological disabilities by providing an alternative communication pathway between the brain and an external device to bypass the malfunctioned neuromuscular pathway. Among several existing signal platforms for BCI applications, subdurally recorded electrocorticogram (ECoG) gains increasing attention due to its decent spatio-temporal resolution, signal-to-noise ratio (SNR), and being moderately invasive. Such ECoG-based BCI operation requires acquiring and decoding movement intentions to restore motor functions while simultaneously eliciting artificial sensations to restore sensory functions. This concurrent neural data acquisition and brain stimulation poses a significant challenge due to the presence of extremely strong stimulation artifacts which can be orders of magnitude larger than the underlying neural signals. In addition, ECoG-based bi-directional BCIs (BD-BCIs) require fully implantable neural recording and stimulation systems to restore motor and sensory functions, respectively. To reduce the size and power consumption of these fully implantable systems, custom-designed integrated circuits including as much functionality as possible with the minimum usage of external components are needed.

This thesis presents one work of optimization algorithm to solve the problem of stimulation artifacts in ECoG-based BD-BCIs, one silicon-tested prototype including both the recording and stimulation systems for BD-BCI applications, and one stimulation system targeting improved charge balancing performance. In the first work, since artifact cancellation can be achieved by adding an auxiliary stimulation of the opposite polarity between the primary stimulation and the recording sites, a simple constrained optimization algorithm for finding the parameters of the auxiliary stimulation that yields optimal artifact suppression is designed. The BD-BCI prototype presents a high-voltage (HV) multipolar neural stimulation system with time-based charge balancing and a mixed-signal neural data acquisition system using successive approximation register analog-to-digital converters. To improve the performance of charge balancing, the second stimulation system is designed as a multipolar HV compliance system incorporating dual-mode time-based charge balancing. Electrical, *in-vitro* and *in-vivo* experimental measurements have verified the functionality and performance of the systems above.

Chapter 1

Introduction

Recently, Brain-computer interface (BCI) has drawn increasing attention since it becomes a promising solution to neurological disorders like epilepsy and narcolepsy [5,6] and neurological disabilities like spinal cord injury [4]. BCI provides a bi-directional pathway between the patient's brain and external sensors and actuators to bypass the damaged human sensory or motor functions. Subdurally recorded electrocorticogram (ECoG) is an appropriate platform for BCI applications due to its decent spatio-temporal resolution, signal-to-noise ratio, clinical practicality, and resilience to motion artifacts. Existing ECoG-based BCI implemented using off-the-shelf components has proven its potential in restoring human movement and sensation in hospital environment [7]. However, to reduce the size and power consumption of the envisioned fully implantable BCIs, custom-designed integrated circuits (ICs) including as much required functionality as possible with the minimum usage of external components are needed. To acquire sub-100 μV ECoG signals continuously from multiple sites in the human brain, the recording ICs require extremely high sensitivity at their inputs and ultra-low power consumption. To effectively elicit artificial sensations in the brain and account for different bio-impedances, the stimulation ICs necessitate >10 mA of stimulation current and >20 V of voltage compliance [8]. Due to the capacitive nature of the electrode-electrolyte

interfaces, injecting stimulation currents into the brain tissue through such interfaces lead to voltage build-up, causing electrode corrosion and tissue damage [9]. To protect the brain tissues and increase the longevity of the BCIs, stimulation ICs require a charge-balancing mechanism. Considering both stimulation and recording systems, BD-BCIs for movement restoration must acquire neural signals to decode movement intentions while simultaneously injecting stimulation currents to elicit artificial sensations. Simultaneous recording and stimulation in this fashion poses a significant challenge due to the presence of extremely strong stimulation artifacts [10]. By employing multipolar stimulation, the electric field potential changes induced by the current injections are localized [11, 12] and the stimulation artifacts propagating to the recording sites are suppressed [13]. However, choosing the locations and intensity of the stimulation currents heuristically can hardly guarantee optimal artifact suppression performance. Therefore, an optimization procedure is needed to find these stimulation parameters.

This thesis presents: (1) an optimization algorithm to find the locations and intensity of the stimulation currents leading to the minimum stimulation artifacts, (2) an ECoG-based BD-BCI including both the recording and stimulation systems with novel techniques to improve sensitivity, reduce power consumption, increase maximum stimulation current and voltage compliance, and conduct charge balancing, and (3) a stimulation system to further improve charge balancing performance.

In the second chapter, a novel method for the suppression of stimulation artifacts before they reach the recording analog front end is developed. Using elementary biophysical considerations, we devised an artifact suppression method that employs a weak auxiliary stimulation delivered between the primary stimulator and the recording grid. The exact location and amplitude of this auxiliary stimulating dipole were then found through a constrained optimization procedure. The performance of our method was tested in both simulations and phantom brain tissue experiments. The solution found through the optimization procedure

matched the optimal canceling dipole in both simulations and experiments. Artifact suppression as large as 28.7 dB and 22.9 dB were achieved in simulations and brain phantom experiments, respectively. We developed a simple constrained optimization-based method for finding the parameters of an auxiliary stimulating dipole that yields optimal artifact suppression. Our method suppresses stimulation artifacts before they reach the analog front-end and may prevent the front-end amplifiers from saturation. Additionally, it can be used along with other artifact mitigation techniques to further reduce stimulation artifacts.

The third chapter presents a multipolar neural stimulation and mixed-signal neural data acquisition (DAQ) chipset for fully implantable bi-directional brain–computer interfaces (BD-BCIs). The stimulation system employs four 40 V compliant current stimulators, each capable of sourcing/sinking a maximum 12.75 mA stimulation current, connected to 16 output channels through a high-voltage (HV) switch fabric. A novel time-based charge balancing (TBCB) technique is introduced to reduce the residual voltage on the electrode-electrolyte interface during the inter-pulse time interval, achieving 2 mV charge balancing precision. Additionally, an analytical study of the charge balancing accuracy for the proposed technique is provided. The recording system incorporates a dual-mode DAQ architecture that consists of a 32-element front-end array and a mixed-signal back-end including analog-to-digital converters (ADCs) for both training (i.e., full-band) and decoding (i.e., baseband) operations. Leveraging the flexibility of the multipolar operation, stimulation-side contour shaping (SSCS) artifact cancellation is adopted to significantly suppress stimulation artifacts by up to 45 dB. The SSCS method prevents the recording front-ends from saturation and greatly relaxes the dynamic range requirement of the recording system, enabling a truly bi-directional operation. The prototype chipset is fabricated in an HV 180-nm CMOS process and demonstrates a significant performance improvement compared to the prior art.

The last chapter presents a multipolar neural stimulation system for fully implantable bi-directional brain-computer interface (BCI) applications. The stimulation system employs

four stimulators connected to 16 electrodes through a 4 by 16 switch fabric. Each stimulator is capable of sourcing/sinking a maximum 14 mA stimulation current and provides 40 V output voltage compliance. Additionally, each stimulator is equipped with a novel dual-mode time-based charge balancing (DTCB) loop to reduce the residual voltage on the electrode-electrolyte interface. When the residual voltage is large, the interpulse-bounded time-based charge balancing (IB-TCB) mode of DTCB is enabled and the loop performs active charge balancing during the inter-pulse time interval. On the other hand, if the residual voltage is small, the artifactless time-based charge balancing (AL-TCB) mode is activated, and the compensation currents are added into the following biphasic stimulations to perform charge balancing without introducing extra stimulation artifacts. Additionally, an inter-channel interference attenuator (ICIA) and a digital DC gain booster (DDGB) are utilized in the AL-TCB mode to suppress the multipolar stimulation-induced inter-channel interference (ICI) and improve charge balancing accuracy without impairing loop stability, respectively. The system also includes a high voltage (HV) supply generator to accommodate different bio-impedances, a phase-locked loop (PLL) to generate required clock signals and a digital core for general control.

Chapter 2

Optimal Artifact Suppression in Simultaneous ECoG Stimulation and Recording for BD-BCI Applications

2.1 Introduction

Most people living with chronic spinal cord injury (SCI) are affected by impairment of sensory and motor functions below the level of injury. Brain-computer interfaces (BCIs) may be a promising approach to addressing SCI and many other neurological conditions [14]. Subdurally recorded electrocorticogram (ECoG) is a suitable signal platform for BCI applications because ECoG electrode grids are not as invasive as intracortical microelectrode arrays, yet their spatio-temporal resolution, signal-to-noise ratio (SNR), and susceptibility to artifacts are far superior to those of electroencephalogram (EEG) [15]. Recent studies showed promising results in using ECoG-based BCIs to restore motor functions to those with severe paralysis [16, 17]. However, these BCI systems exclusively relied on visual feedback.

Therefore, their performance was arguably suboptimal due to the lack of proprioceptive and tactile feedback. Since these percepts can be elicited by ECoG electrostimulation [18,19], it can be envisioned that sensory information will be integrated into future ECoG-based BCIs. These bi-directional (BD)-BCIs will have the capability to concurrently restore motor and sensory functions in a biomimetic manner.

Unlike similar bi-directional brain interfaces, such as responsive neurostimulators (RNSs) [20], where simultaneous recording and stimulation are not necessary, BD-BCIs for movement restoration must decode movement intentions while simultaneously eliciting artificial sensation. Simultaneous recording and stimulation in this fashion poses a significant challenge due to the presence of extremely strong stimulation artifacts [10]. For example, given a typical electrode-tissue impedance of 1 kΩ [21] and sensation-eliciting stimulating current of 5 mA [18], the stimulation voltage of 5 V may be necessary. In contrast, recorded ECoG signals have substantially smaller amplitudes ($<$100 μV [15]). To mitigate this problem, various artifact suppression techniques have been proposed [22], ranging from those focused on analog front-ends [23,24] to digital filtering [23,25,26]. However, these approaches would fail if the amplifiers were saturated by extremely strong artifacts, and no amount of signal processing could recover neural signals of interest. Amplifier saturation is even more likely for analog front-ends operating in an ultra-low power (ULP) regime, which is a basic requirement for fully implantable BCIs. This issue thus necessitates a solution that works at the front-end in order to prevent saturation and preserve the recording.

Recently, we introduced an artifact cancellation technique [27], where the stimulation artifacts were reduced by introducing weak canceling currents via ECoG electrodes located between the primary stimulator and the recording electrodes. The major advantage of this approach is that it suppresses artifacts *before* they reach recording electrodes while minimally increasing the stimulation power overhead. Although successful, this proof-of-concept study used canceling patterns that were chosen heuristically. In contrast, this study ex-

ploits insights from volume conduction theory and casts the artifact cancellation problem within a mathematical framework [27]. Specifically, we formulate artifact cancellation as an optimization problem, wherein the effect of stimulation artifacts on the recording side is minimized, while satisfying physical and physiological constraints. The optimal canceling patterns produced by our method have been successfully validated both in simulations and brain phantom tissue experiments. If successfully tested in humans, our method may offer a promising solution to subdural artifact cancellation which could be widely adopted in future ECoG-based BD-BCI systems.

2.2 Methods

2.2.1 Artifact Cancellation by Auxiliary Stimulation

Our approach exploits the primarily resistive volume conduction nature of the brain. Namely, at frequencies below 10 kHz, the brain tissue largely behaves as a bulk resistive medium [28–31]. While the electrode-tissue interface has non-negligible capacitive effects and, thus, may introduce phase lags, we previously found a consistently tight phase-locking of stimulation artifacts across spatially distributed ECoG electrodes [32,33]. This observation suggests that, despite the heterogeneous composition of neural tissue and capacitive effects of electrode-tissue interface, the spatial distribution of artifacts can be accurately described by a resistive model, such as a dipole [27, 32, 33]. The artifact potential field could then be controlled by placing an auxiliary stimulation dipole of the opposite polarity nearby.

This concept is best demonstrated using a simple monopole model, as shown in Fig. 2.1. After introducing an auxiliary stimulating (canceling) current between the primary stimulation site and the recording region, the net artifact falls below a hypothetical analog front-end saturation voltage across the entire recording region.

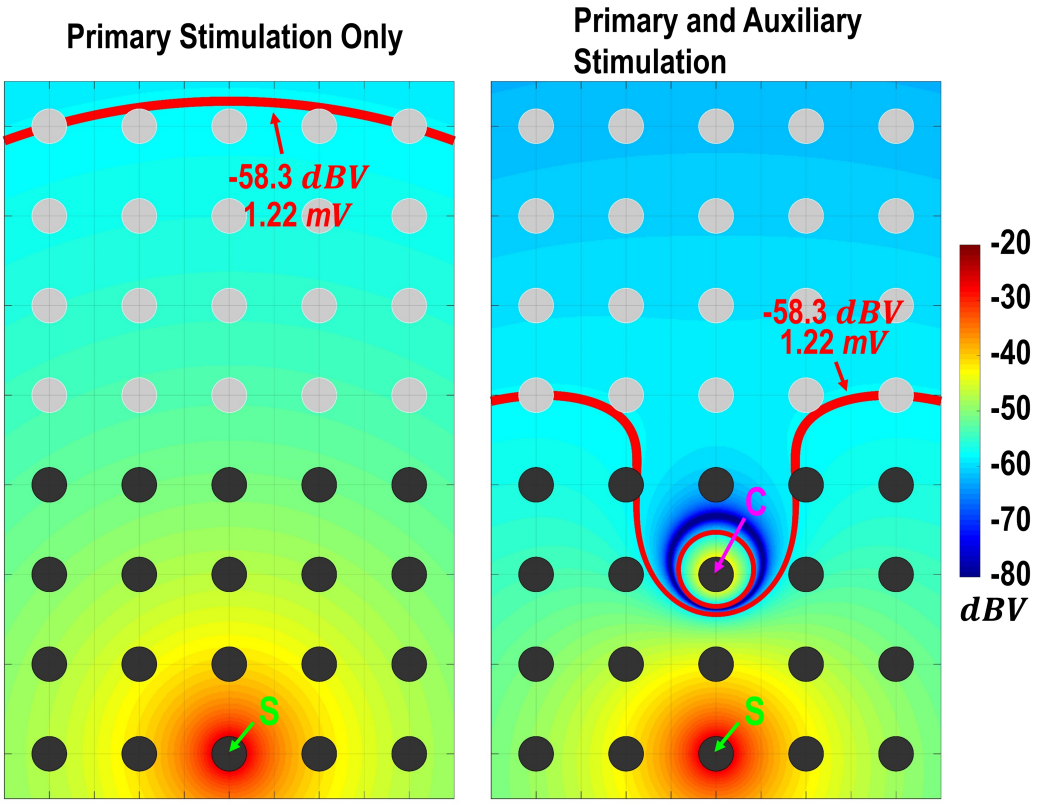


Figure 2.1: **Voltage distributions due to primary stimulation (left) and both primary and auxiliary stimulation (right).** Black and grey dots mark the electrodes on stimulating and recording grids, respectively. S - the primary stimulating monopole; C - the canceling (auxiliary) monopole. The voltage distribution due to a monopolar current source (S or C) is described by: $V = I/(4\pi\sigma r)$, where V is the voltage at a distance r from the current source, I is the current amplitude, and σ is the conductivity of the medium [1, 2]. The primary and auxiliary stimulating currents are of opposite polarity, with the auxiliary current set to 25% of the primary current. For a hypothetical analog front-end saturation voltage of 1.22 mV and a bulk conductivity of 1.79 S/m (cerebrospinal fluid conductivity) [3], the entire recording grid is saturated (left). In contrast, the auxiliary stimulation prevents the saturation entirely without significantly interfering with the primary stimulation (right).

To further advance this idea, we note that the potential field generated by a bipolar charge-balanced ECoG stimulation (a standard clinical practice) can be described by a dipole model (see A.1 for details). Our preliminary study [27] provides empirical evidence for this idea and shows that the addition of an auxiliary dipole produces a cancellation effect that reduces the amplitude of artifacts. However, choosing the location and intensity of the canceling dipole heuristically can hardly guarantee optimal artifact suppression performance. Therefore, this study proposes to find these parameters through an optimization procedure.

2.2.2 Proposed Optimization Framework

To minimize the worst case artifacts across the recording grid, the optimal canceling pattern (canceling dipole locations and canceling currents) must be found through an optimization process. Additionally, such an optimal canceling pattern must satisfy several physical and physiological constraints. These constraints are defined as binary variables (0 when the constraints are satisfied, 1 otherwise). First, a canceling dipole physical constraint (PC) is introduced to prevent primary and/or canceling dipole overlap. Second, the canceling dipoles may cause unwanted sensation if their currents are too large. To address this issue, a local sensation constraint (SC) is defined to restrict the canceling currents to a threshold. Third, the voltages created by canceling dipoles can potentially counteract the voltage induced by the primary stimulating dipole and cause a loss in sensation. Therefore, an interference constraint (IC) is introduced to impose a restriction on the voltage induced by the canceling dipoles. Formally, the artifact cancellation problem can be cast as the following constrained optimization problem:

$$\boldsymbol{os} = \underset{\boldsymbol{cs}}{\operatorname{argmin}}\, F(\boldsymbol{cs}) \qquad \text{subject to} \quad PC + SC + IC = 0 \tag{2.1}$$

where $\boldsymbol{cs}$ is a candidate solution, $\boldsymbol{os}$ is the optimal solution (see A.2 for details) and $F(\boldsymbol{cs})$ is the objective function. Specifically, $F(\boldsymbol{cs})$ is defined as the maximum net voltage observed by the recording grid (details in Section 2.2.2). Variables to be optimized are canceling dipole locations and currents (parametrized by β, where $\beta \in [0,1]$ is the amplitude ratio of the auxiliary and primary stimulating currents). The optimization algorithm iteratively inspects all the candidate solutions, and determines whether they satisfy the three constraints. Based on the optimization algorithm, a mathematical model is constructed accordingly to characterize concurrent ECoG stimulation and recording as well as incorporate cancellation (see A.3 for details). The pseudo-code for the optimization framework is shown in Algorithm 1 with all the notations defined in table 2.1.

Algorithm 1 Iterative approach to find canceling pattern with the minimum amount of artifacts.

Require: MP
  Generate A from MP
  $\boldsymbol{os} \leftarrow$ Randomly choose a candidate solution in A
  $A \leftarrow A \setminus \{\boldsymbol{os}\}$
  while $A \neq \varnothing$ **do**
    $\boldsymbol{cs} \leftarrow$ Randomly choose a candidate solution in A
    if $F(\boldsymbol{cs}) \leq F(\boldsymbol{os})$ **then**
      Update PC, SC, IC
      if $PC + SC + IC = 0$ **then**
        $\boldsymbol{os} \leftarrow \boldsymbol{cs}$
      end if
    end if
    $A \leftarrow A \setminus \{\boldsymbol{cs}\}$
  end while
  return $\boldsymbol{os}$

Table 2.1: Notations for Algorithm 1.

MP	A set of all the model parameters (see A.3)
A	A set which contains all the possible candidate solutions
$\boldsymbol{os}$	Optimal solution for the optimization problem
$\boldsymbol{cs}$	Candidate solution: containing all the variables to be optimized
$F(\boldsymbol{cs})$	Objective function
PC	Canceling dipole physical constraint ($PC = 1$ for violation; $PC = 0$ otherwise)
SC	Local sensation constraint ($SC = 1$ for violation; $SC = 0$ otherwise)
IC	Interference constraint ($IC = 1$ for violation; $IC = 0$ otherwise)

We elaborate on the optimization framework in subsequent sub-sections.

Objective Function $F(\boldsymbol{cs})$

To explicitly demonstrate all the variables to be optimized in the candidate solution ($\boldsymbol{cs}$), we define $P_{\mathrm{t}}(\hat{x}_{\mathrm{r}}, \hat{y}_{\mathrm{r}}, \boldsymbol{cs})$ as the net voltage amplitude at a recording electrode location $(\hat{x}_{\mathrm{r}}, \hat{y}_{\mathrm{r}})$ (by substituting equation A.12 and A.13 into equation A.5), i.e.,

$$P_{\mathrm{t}}(\hat{x}_{\mathrm{r}}, \hat{y}_{\mathrm{r}}, \boldsymbol{cs}) = V_{\mathrm{t}}(\hat{x}_{\mathrm{r}}, \hat{y}_{\mathrm{r}}) \tag{2.2}$$

Accordingly, we define the objective function to represent the largest net artifact over all possible recording electrode locations, i.e.,

$$F(\boldsymbol{cs}) = \max_{p_{\mathrm{r}}, q_{\mathrm{r}}} |P_{\mathrm{t}}(\hat{x}_{\mathrm{r}}, \hat{y}_{\mathrm{r}}, \boldsymbol{cs})| \tag{2.3}$$

where $p_r = 0, 1, ..., X_r - 1$, $q_r = 0, 1, ..., Y_r - 1$, and X_r and Y_r are the number of rows and columns in the recording grid, respectively (see A.3).

Canceling Dipole Physical Constraint (PC)

PC excludes the candidate solution(s) based on two sub-constraints (see A.4 for details). The first sub-constraint excludes cases wherein one or more canceling electrodes overlap with the primary stimulating electrodes. The second sub-constraint leaves out candidate solution(s) with two or more canceling dipoles sharing electrodes. The reason for this exclusion is that overlapped electrodes can ruin the dipolar structure of the canceling currents, which may cause difficulties in practical implementation. On the other hand, if two canceling dipoles fully overlap, this solution is redundant and can be recreated by decreasing the number of canceling dipoles, N, (see A.3).

Local Sensation Constraint (SC)

Assuming the primary stimulation meets all the FDA safety requirements, the auxiliary stimulation should not raise any safety concerns so long as $\beta \leq 1$. However, from a physiological perspective, a strong cancellation (large β) may in itself cause unwanted sensation. In addition, choosing a large β significantly increases the power consumption, which is highly undesirable in implantable devices. Therefore, SC is added to set the upper limit for allowable canceling-to-stimulating current-ratio to be $\beta_{\max}$, i.e.

$$I_{\mathrm{c},n} \leq \beta_{\max} \cdot I_{\mathrm{s}}, \forall n = 1, 2, ..., N \tag{2.4}$$

In practice, $\beta_{\max}$ needs to be chosen empirically, but for the purpose of this study, $\beta_{\max} = 50\%$ was deemed sufficient (see Section 2.4.1 for additional discussion).

Interference Constraint (IC)

Strong cancellation may also interfere with the primary stimulation, potentially leading to the loss of artificial sensation. To constrain this interference on sensation, we first modeled the effect of auxiliary stimulation on cortical excitation underneath the primary stimulating dipole. Specifically, neural excitation generated by external stimulation sources can be quantified by the activating function [34, 35], which is equal to the second spatial derivative of the external potential along the axon of interest. Assuming the stimulation is more likely to activate neurons whose axons are perpendicular to the cortical surface, the activation function af is calculated along the z-direction. This assumption reflects the fact that neurons in cortical gyri are more likely to be activated than those in sulci due to their greater proximity to the cortical surface [36]. Specifically, we calculated af at an observation point (x, y, z) as:

$$af\left(x,y,z\right)=\frac{\partial^2 U\left(x,y,z\right)}{\partial z^2} \tag{2.5}$$

where $U\left(x,y,z\right)$ denotes the potential at an observation point outside of an axon. Applying $U_{\mathrm{s}}\left(x,y,z\right)$ and $U_{\mathrm{c},n}\left(x,y,z\right)$ (Eqs. (A.1) and (A.2)) to the generic expression of $af\left(x,y,z\right)$, the activating functions due to the primary and auxiliary stimulations at observation points located underneath the primary stimulating dipole are represented by $AF_{\mathrm{s}}\left(z\right)$ and $AF_{\mathrm{c},n}\left(\boldsymbol{cs},z\right)$, respectively (see A.5 for details).

To quantify the interference due to the auxiliary stimulation, an interference function IF is then defined as the absolute value of the ratio between the activating functions due to the auxiliary and primary stimulations, i.e.,

$$IF\left(\boldsymbol{cs},z\right)=\left|\frac{\sum_{n=1}^{N}AF_{\mathrm{c},n}\left(\boldsymbol{cs},z\right)}{AF_{\mathrm{s}}\left(z\right)}\right| \tag{2.6}$$

We assume that, at the observation point located underneath the stimulating dipole, if IF is less than the tolerable interference threshold α, the influence of auxiliary stimulation on the artificial sensation can be neglected. In this study, $\alpha=0.5\%$ is used. However, the exact value of α can only be found empirically (see Section 2.4.1 for additional discussion). This restriction on IF is formulated as the interference constraint (IC), i.e.,

$$IF\left(\boldsymbol{cs},z\right)\leq\alpha,\forall z\in\left[-6.5,0\right] \tag{2.7}$$

The average thickness of cerebrospinal fluid (CSF) plus cortex is around 6.5 mm [37, 38]. Therefore, IF is inspected down to 6.5 mm underneath the primary stimulating dipole electrodes. Details can be found in A.5.

Summary of the Optimization Framework

Combining the objective function $F(\boldsymbol{cs})$ with the three constraints PC, SC, and IC, the optimization framework is summarized in Table 2.2.

Table 2.2: Summary of the optimization framework.

Objective		$\boldsymbol{os} = \underset{\boldsymbol{cs}}{\operatorname{argmin}} F(\boldsymbol{cs})$, where $F(\boldsymbol{cs}) = \max_{p_\mathrm{r},q_\mathrm{r}} \lvert P_\mathrm{t}(\hat{x}_\mathrm{r}, \hat{y}_\mathrm{r}, \boldsymbol{cs})\rvert$
Subject to	PC	There is no canceling electrode which overlaps with a primary stimulating electrode. There are no canceling dipoles which share electrodes.
	SC	$I_{\mathrm{c},n} \leq \beta_{\max} \cdot I_\mathrm{s}, \forall n = 1, 2, ..., N$
	IC	$IF(\boldsymbol{cs}, z) \leq \alpha, \forall z \in [-6.5, 0]$ where $IF(\boldsymbol{cs}, z) = \left\lvert \frac{\sum_{n=1}^{N} AF_{\mathrm{c},n}(\boldsymbol{cs}, z)}{AF_\mathrm{s}(z)} \right\rvert$

2.2.3 Validation of the Proposed Optimization Methodology

Phantom Tissue

To create a phantom tissue, table salt (Morton Salt, Chicago, IL) was mixed with deionized water, and the mixture was heated until boiling. Food-grade agar (Now Foods, Bloomingdale, IL) was then added into the boiling mixture to prepare a gel compound, which was poured into a Petri dish and an open-ended cylindrical mold. Both were placed in a refrigerator to cool down. The conductivity of the gel was manipulated by table salt concentration [39], and was calculated based on the size and measured resistance of the gel within the cylindrical mold.

Experimental Setup

A standard ECoG grid (Ad-Tech, Oak Creek, WI) with platinum electrodes (4 mm diameter, 2.3 mm exposed, 10 mm spacing) delivered stimulating/canceling currents and recorded

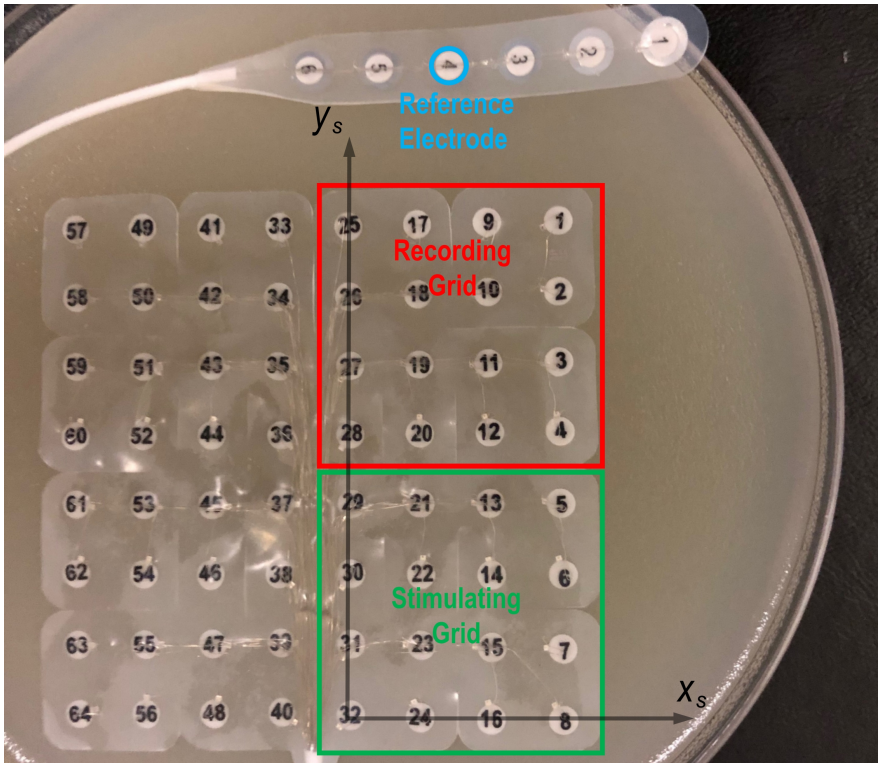


Figure 2.2: **ECoG grids on phantom tissue.** The stimulating and canceling dipoles are located on a 4×4 stimulating grid. All electrodes on the 4×4 recording grid are used to record artifacts. The reference electrode is chosen from the 1×6 ECoG strip, positioned far away from the stimulation region. The recording ground is connected to earth ground via the recording amplifier.

artifacts, as shown in Fig. 2.2. A thin layer of 1× phosphate buffered saline (PBS) (Aldon Corporation, Avon, NY) was added between the grid and the gel to ensure full contact. Due to the limited number of recording amplifiers and the availability of the ECoG grid, two 4×4 arrays of an 8×8 grid were designated as the stimulating and recording grids. In addition, the relative position $(x_{\mathrm{rs}}, y_{\mathrm{rs}})$ and relative angle θ were set to $(0, 40)$ mm and 0 rad. A 1×6 ECoG strip was placed away from the stimulation region and its closest electrode to the central axis of the primary stimulating dipole was designated as the reference.

Fig. 2.3 demonstrates the experimental setup for primary stimulation and recording. The leads of the stimulating dipole were connected to a function generator (supplying an 89 Hz sine wave) in series with an oscilloscope. Since the function generator is a voltage-controlled

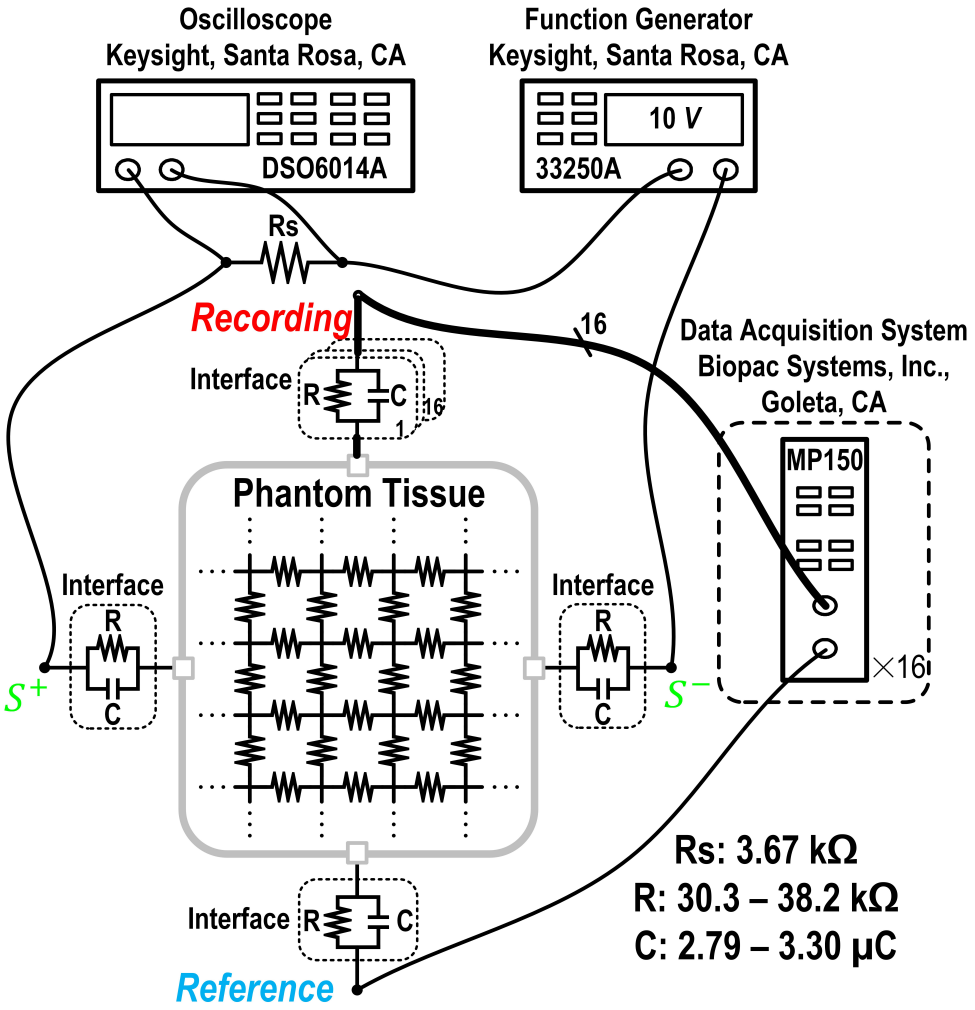


Figure 2.3: **Experimental setup for primary stimulation and recording.** S^+ and S^- respectively denote the source and sink electrodes of the stimulating dipole, whose leads were connected to a function generator. The resistor R_S was added to monitor the stimulating current through an oscilloscope. On the recording side, the leads of the 16 recording electrodes were connected to the data acquisition system. All 16 amplifiers shared a common reference voltage.

device, a resistor R_S was placed in parallel with the oscilloscope to monitor the stimulating current. The 89-Hz tone was chosen because it produces a narrowband response on the recording grid, which greatly simplifies data analysis. In addition, this frequency is not harmonically related to the 60-Hz noise. An additional function generator and resistor were added for the canceling dipole (details omitted from the figure for clarity). The two function generators were synchronized and produced sine waves with calibrated phase shift in order

to create 180° phase difference between stimulating and canceling currents. The leads of the recording grid and the reference electrode were connected to a data acquisition system where the recorded artifacts were amplified by 5,000× and sampled at 4 kHz. We collected 30 s of data under both stimulation-only and stimulation+cancellation conditions, where the strength of cancellation was systematically varied (details below).

Estimation of Stimulating Current I_s

For simplicity, a fixed value of the stimulating current, I_s, was used across all experiments. To account for impedance differences across stimulation sites and find I_s that works for all experiments, the following analysis was used. According to Fig. 2.3, the total impedance seen by the function generator consists of the impedance of the electrode-electrolyte interfaces, resistance of the current monitoring resistor, R_S, and the equivalent resistance of the phantom tissue connected in series. To estimate this impedance, electrode-electrolyte interfaces were modeled as parallel RC circuits [9], and the phantom tissue was modeled as a distributed resistive network (Fig. 2.3). The total impedance of the interfaces and phantom tissue was then measured across frequency. Subsequently, curve-fitting was applied to the impedance frequency response to estimate the resistance and capacitance of these interface models as well as the equivalent resistance of the phantom tissue. Based on these estimated values, the total impedance of the interfaces and phantom tissue was calculated to be 562-1928 Ω at 89 Hz. The result is consistent with clinical measurement [40, 41]. Therefore, the total impedance seen by the function generator was calculated to be 4-6 kΩ. Given that the maximum voltage of the function generator was 10 V, this total impedance allowed an I_s of 1.5 mA across all the cases.

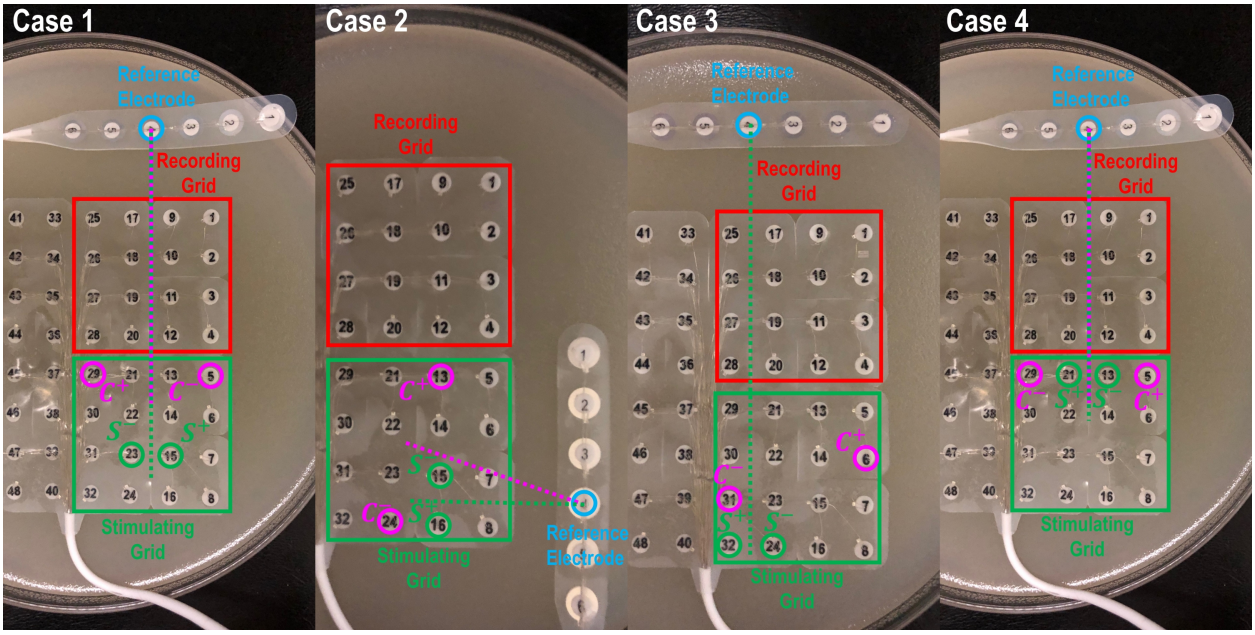


Figure 2.4: **Physical configuration of experiments for all the cases.** Case 1: electrode pair 15-23 (source-sink) realized the primary stimulating dipole. Electrode pairs 22-14, 21-13, 30-6, and 29-5 (shown) were used one at a time as the canceling dipole. Reference electrode was placed far away from the stimulating grid near the hypothetical zero-potential line at the central axis of both stimulating and canceling dipoles. Case 2: electrode pair 16-15 realized the primary stimulating dipole. Electrode pairs 13-8, 21-8, 13-24 (shown), and 5-24 were used one at a time as the canceling dipole. When possible, the reference electrode was placed near the central axes of both the stimulating and canceling dipoles (shown). Otherwise, it was placed near the central axis of the stimulating dipole. Case 3: electrode pair 32-24 realized the primary stimulating dipole. Electrode pairs 6-31 (shown), 7-30, 6-30, and 7-31 were used one at a time as the canceling dipole. Reference electrode was placed far away from and near the central axis of the primary stimulating dipole. Case 4: electrode pair 21-13 realized the primary stimulating dipole and electrode pair 5-29 was used as the canceling dipole. Reference electrode was placed far away from the stimulating grid near the central axes of both stimulating and canceling dipoles.

Experiments

The experimental setup (discussed in Section 2.2.3) was used in four different cases, shown in Fig. 2.4, to demonstrate the performance of the optimization algorithm under different stimulating dipoles. The phantom tissue with a conductivity of 1.79 S/m was chosen to mimic the bulk conductivity of subdural head tissues which is dominated by the CSF [3]. The dipole model used to describe the artifact propagation (see A.1) requires an assumption

of an infinitely far reference. Since this is not physically achievable in reality, the reference is placed far from the primary stimulating dipole on the zero potential line to best fulfill the referencing assumption.

A single electrode pair was used as the stimulating dipole. Case 1 is the most straightforward situation in which the stimulating dipole is oriented horizontally and its central axis coincides with the axis of symmetry of the recording grid. Case 2 is similar except that the stimulating dipole was oriented vertically. In Case 3, the stimulating dipole is oriented horizontally, while the recording grid is not symmetric with respect to the dipole's central axis. Case 4 mimics the worst-case scenario, where the horizontally oriented stimulating dipole is adjacent to the recording grid, so the artifacts will be projected the furthest into the recording grid.

Running Optimization Algorithm

Before running the optimization algorithm, the model parameters, as listed in table A.1, need to be specified. To this end, the geometric characterization and primary stimulation parameters were extracted for each case based on Fig. 2.4. As discussed in Section 2.2.2 and 2.2.2, we chose $\beta_{\max} = 50\%$ and $\alpha = 0.5\%$, and we assumed a single canceling dipole ($N = 1$). As listed in table 2.3, all the cases shared the same model parameters except for the primary stimulation locations. Based on these parameters, the optimization algorithm was executed for each case and the optimal canceling patterns were found. These optimal patterns were verified by simulation (details in Section 2.2.3) and experimentally (details in Section 2.2.3), respectively.

Simulation Verification

To illustrate the effectiveness of the optimal canceling pattern in each case, the voltage distributions were calculated using Eqs. (A.3)-(A.5) for the following conditions: (i) stimulating

Table 2.3: Model parameters for Cases 1–4.

Geometric characterization parameters	X_s, Y_s	4, 4
	X_r, Y_r	4, 4
	d	10 mm
	x_{rs}, y_{rs}	0 mm, 40 mm
	θ	0 rad
Dipole model parameter	σ	1.79 S/m
Primary stimulation model parameters	x_s^+, y_s^+	20 mm, 10 mm (Case 1)
		20 mm, 0 mm (Case 2)
		0 mm, 0 mm (Case 3)
		10 mm, 30 mm (Case 4)
	x_s^-, y_s^-	10 mm, 10 mm (Case 1)
		20 mm, 10 mm (Case 2)
		10 mm, 0 mm (Case 3)
		20 mm, 30 mm (Case 4)
	I_s	1.5 mA
Number of canceling dipoles	N	1
Constraint system parameters	β_{max}	50%
	α	0.5%

dipole only, and (ii) both stimulating and the optimal canceling dipoles. These voltage values were color-coded and mapped onto the grid for comparison. In addition, to characterize the effectiveness of the optimal canceling pattern, the artifact suppression was quantified by dividing the largest artifact magnitude under conditions (i) and (ii).

To further verify the effectiveness of the optimal canceling pattern, the location and/or the canceling ratio, β, of the optimal canceling dipole were perturbed. The corresponding artifact suppression was then quantified and compared to that of the optimal solution. For example, in Case 1, in addition to the optimal canceling dipole (electrode pair: 30-6), the following canceling dipole locations were tested: 22-14, 21-13, and 29-5. Note that these are the immediate neighbors of the optimal pair 30-6 (see Fig. 2.4). For all the canceling dipoles, β was swept from 0 to β_{max} in 1% increments. Similar analysis was applied to other cases. The only exception was Case 4, where it was obvious that the perturbation of the optimal canceling dipole location would not produce competitive results.

Experimental Verification

The above simulation verification and analysis were then replicated experimentally using the procedure discussed in Section 2.2.3. The 30 s of data recorded under both stimulation only and stimulation+cancellation conditions were analyzed offline using Matlab. The data were first filtered by a bandpass finite impulse response (FIR) filter with 85-93 Hz passband (for an 89-Hz test input), 0.1% inband ripple, and 40 dB stopband attenuation. Each set of the filtered data was decomposed into 30 non-overlapping segments. These segments were then converted into frequency domain, and their amplitude spectra were calculated and averaged to reduce noise. For all the recording channels, the artifacts' amplitudes were estimated as the values of the voltage spectra at 89 Hz. These values were then spatially interpolated, color-coded, and mapped for analysis. Similar to Section 2.2.3, the optimal canceling pattern (as found by the algorithm) was experimentally tested and compared to those found by perturbation.

2.3 Results

2.3.1 Simulation Results

Figs. 2.5(A) and (B) respectively show the spatial distribution of simulated artifacts before and after optimal cancellation for Case 1. The optimal canceling pattern was a dipole located at the electrode pair 30-6 with β=18%. We found these parameters by running the optimization algorithm as explained in Section 2.2.3. Table 2.4 shows the algorithm run time for this as well as other cases. Note that the symmetric arrangement of the stimulating and canceling dipoles caused the symmetry in the spatial distribution of artifacts. By applying optimal cancellation, the largest artifact experienced by the recording grid decreased from

-71.7 dBV to -100.4 dBV for a total artifact suppression of 28.7 dB.

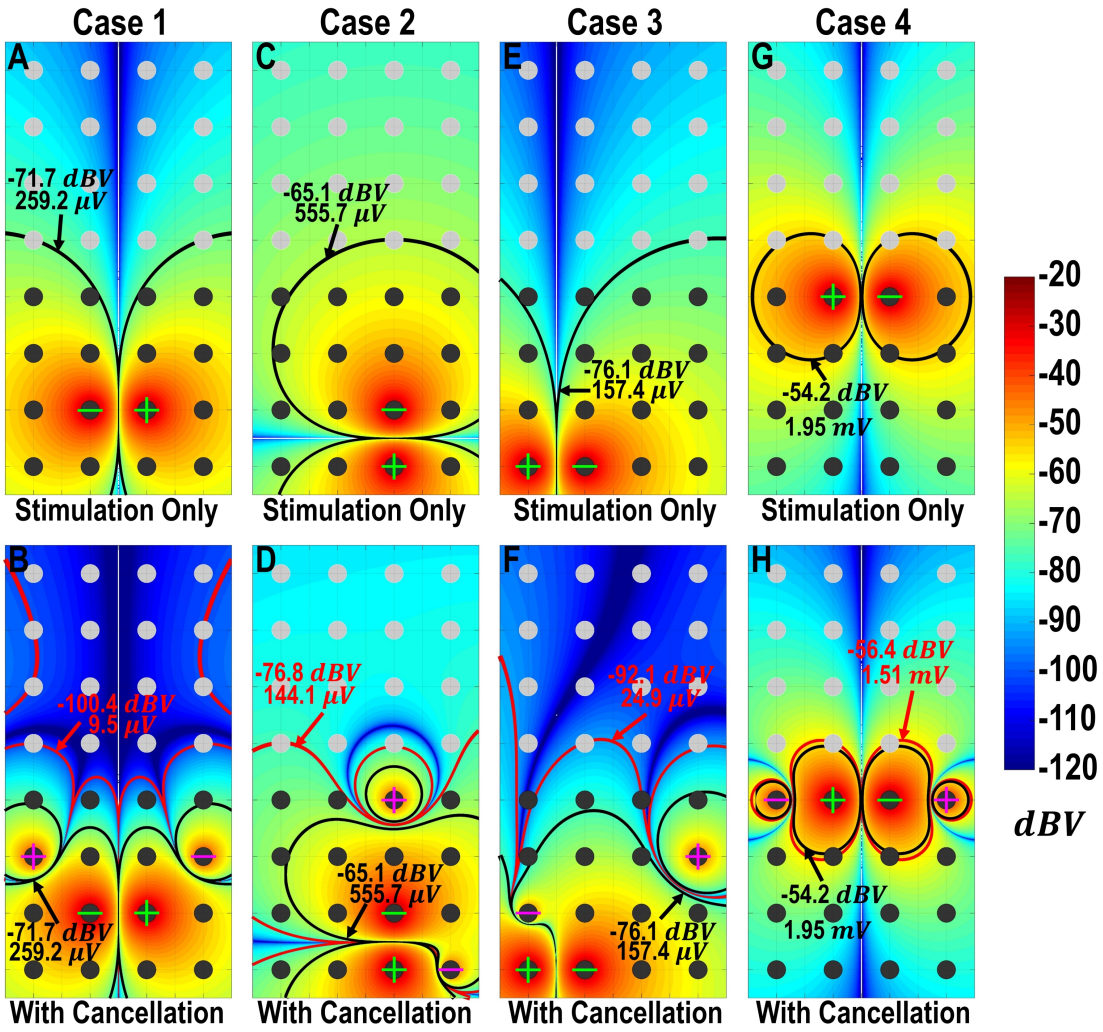


Figure 2.5: **Spatial distribution of simulated artifacts under stimulation only and stimulation + optimal cancellation conditions for Cases 1–4. Grey: recording grid. Black: stimulating grid. Green: stimulating dipole. Magenta: canceling dipole.** A: Case 1–the stimulating dipole is formed by electrode pair 15-23 (see Fig. 2.4 for reference). Black contour marks the largest observed artifact. B: Case 1–the optimal canceling pattern is formed by using electrode pair 30-6 with $\beta = 18\%$. The largest-artifact contour (red) indicates the artifact has been suppressed from 259.2 to 9.5 μV (or by 28.7 dB). At the same time, the original largest-artifact contour (black) is well outside the recording grid. C: Equivalent of A for Case 2. D: Equivalent of B for Case 2 (optimal $\beta = 13\%$). An artifact suppression of 11.7 dB has been achieved. E: Equivalent of A for Case 3. F: Equivalent of B for Case 3 (optimal $\beta = 10\%$). An artifact suppression of 16.0 dB has been achieved. G: Equivalent of A for Case 4. H: Equivalent of B for Case 4 (optimal $\beta = 25\%$). An artifact suppression of 2.2 dB has been achieved.

Figs. 2.5(C) and (D) show the equivalent maps for Case 2. The optimal canceling pattern

reduced the largest artifact by 11.7 dB. This result is inferior to Case 1 due to the unfavorable (vertical) orientation of the stimulating dipole.

Figs. 2.5(E) and (F) show the spatial distribution of simulated artifacts for Case 3. An optimal suppression of 16.0 dB was achieved, but the pre-cancellation artifacts were smaller than those in Case 1 and 2. It is worth mentioning that the artifact tends to be larger at electrodes located away from the central axis of the stimulating dipole. Hence, as shown in Fig. 2.5(F), the source electrode of the canceling dipole, obtained from the optimization algorithm, was placed closer to the recording grid than the sink to provide larger cancellation to the recording sites further away from the central axis.

Figs. 2.5(G) and (H) show the equivalent distribution for Case 4. Intuitively, higher artifact suppression can be achieved by continuously increasing β. However, increasing β beyong 25% cause violation of IC (refer to Section 2.2.2). Therefore, $\beta = 25\%$ was chosen by the optimization algorithm as the optimal solution, resulting in an artifact suppression of 2.2 dB.

Table 2.4: Algorithm run times (Intel® Core™ i5-7400, 8 GB RAM)

Case 1	13.367 sec
Case 2	14.692 sec
Case 3	13.566 sec
Case 4	13.514 sec

Table 2.5: Algorithmically optimal solutions tested in simulation and experimentally.

	Case 1		Case 2		Case 3		Case 4	
Result type	Sim	Exp	Sim	Exp	Sim	Exp	Sim	Exp
Largest artifact among all the recording sites without cancellation (μV)	259.2	350.5	555.7	767.2	157.4	151.2	1950.2	2693.1
Largest artifact among all the recording sites with optimal cancellation (μV)	9.5	25.1	144.1	204.4	24.9	31.6	1510.0	1995.2
Artifact suppression (dB)	28.7	22.9	11.7	11.5	16.0	13.6	2.2	2.6
Optimal canceling dipole (source-sink)	$30-6$	$30-6$	$13-8$	$13-8$	$6-31$	$6-31$	$5-29$	$5-29$
Optimal canceling ratio β_{opt}	18%	18%	13%	13%	10%	10%	25%	25%

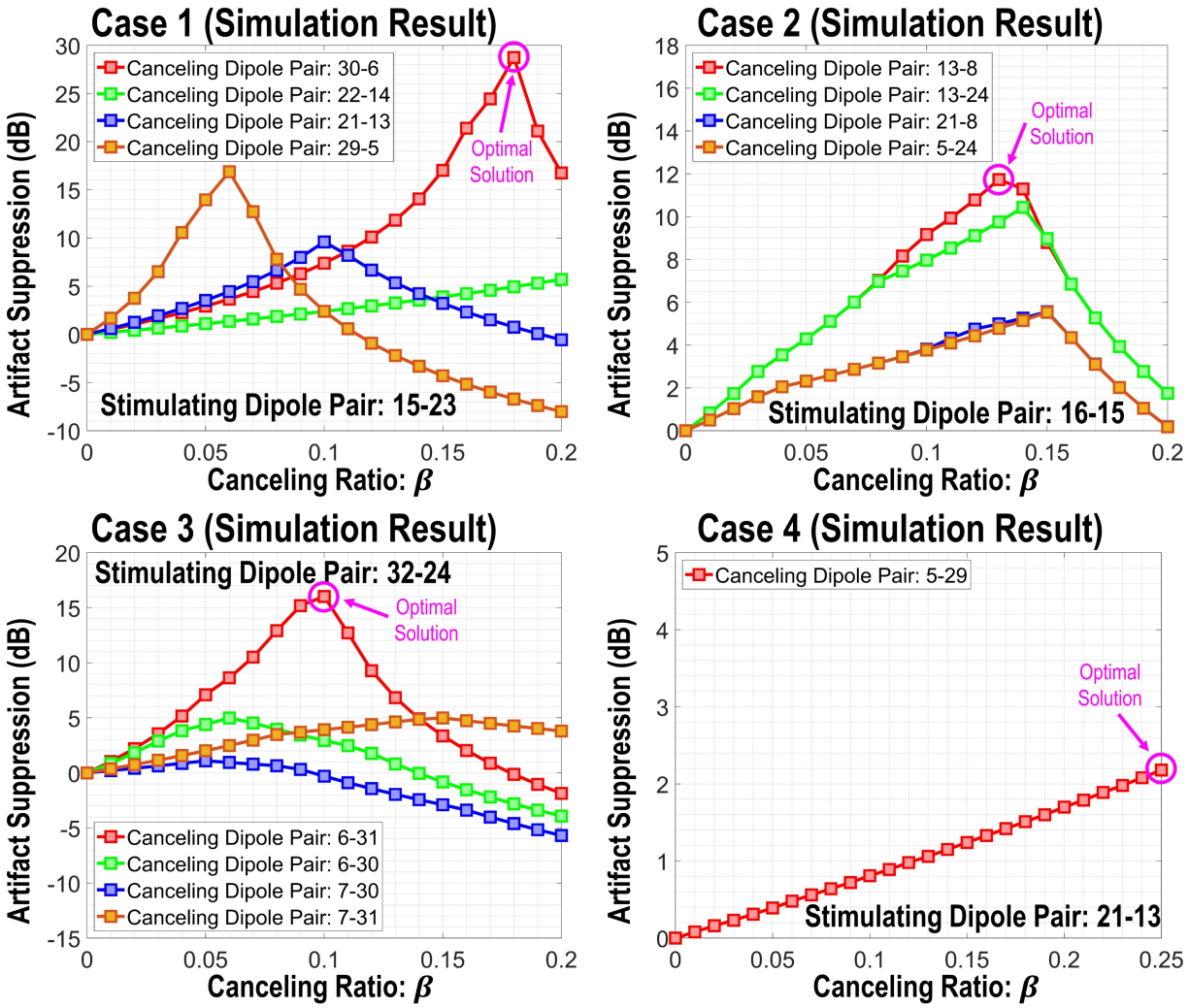


Figure 2.6: **Perturbation analysis: simulation results.** In Case 1, the perturbations of canceling dipole location and β demonstrate inferior artifact suppression compared to the optimal solution (marked in magenta) found by the optimization algorithm. Similarly, Case 2 and Case 3 exhibit superiority of the optimal solutions. In Case 4, the artifact suppression increases monotonically with β as predicted. The largest artifact suppression happens when β reaches 25% (limited by IC). This result is consistent with the optimal solution found by the optimization algorithm.

Perturbations of the optimal canceling dipole location and β were then simulated and compared to the optimal solution for each case (see Fig. 2.6). For Cases 1–3, three additional competitive canceling dipole locations were tested (see Section 2.2.3). In addition, since the optimal β never exceeded 20%, the perturbations of β up to 20% were selected to show in Fig. 2.6. For Case 4, the upper bound for β was 25% (as discussed above), and no competitive canceling dipoles could be created by location perturbation (as discussed in Section 2.2.3). In Fig. 2.6, it is clearly seen that the optimal solutions demonstrate the largest amount of artifact suppression. These optimal solutions for Cases 1–4 are summarized in Table 2.5.

2.3.2 Experimental Results

Following validation of the optimization framework with simulation, phantom tissue experiments (see Section 2.2.3) were conducted to further demonstrate the effectiveness of the proposed algorithm. Similar to Fig. 2.5, the artifact spatial distributions were visualized with and without the optimal canceling pattern (see Fig. 2.7). A more detailed collection of artifact suppression maps can be found in the supplementary material.

The optimal solutions tested experimentally are summarized in table 2.5. The comparison between experimental and simulation results indicates that the optimization algorithm makes accurate predictions about the artifact suppression.

Similar to Fig. 2.6, perturbations of the optimal canceling dipole location and β were experimentally tested (see Fig. 2.8). A comparison with the plots of Fig. 2.6 reveals that experimental results closely follow those obtained by simulations. More precisely, in Case 1, the best artifact suppression was reported by both the experiment and simulation when the electrode pair 30-6 with β=18% was used as the canceling pattern. Moreover, referring to Fig. 2.8, the artifact suppression first increases with β for canceling dipoles 30-6, 21-13, and 29-5, before it reaches its peak value. The reason for this monotonically increasing trend is

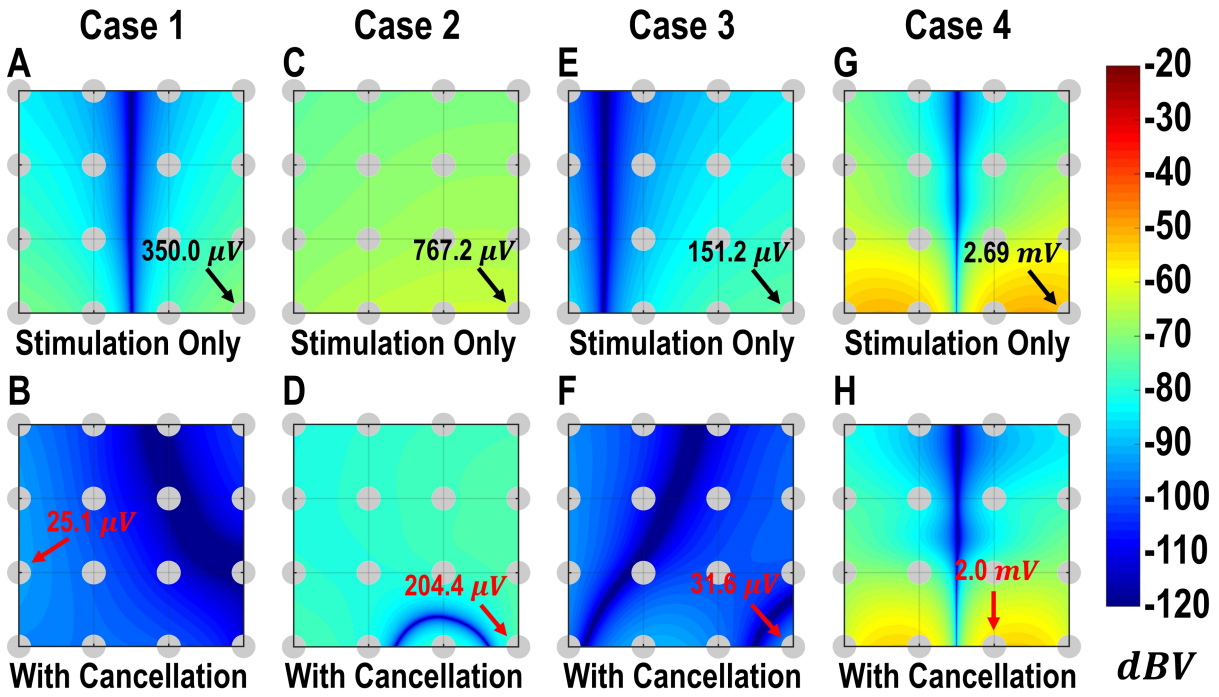


Figure 2.7: **Artifact spatial distribution under stimulation only and stimulation+optimal cancellation conditions for Cases 1–4. Grey: recording grid. Unlike Fig. 2.5, the artifact distribution outside the recording grid is not shown because artifacts were only recorded within the recording grid. (see Section 2.2.3).** A: Case 1–the stimulating dipole is formed by electrode pair 15-23 (see Fig.2.4 for reference). The largest artifact was recorded as 350.5 μV (marked in black). B: Case 1–the optimal canceling pattern is formed by using electrode pair 30-6 with $\beta = 18\%$. The largest artifact after the optimal cancellation was measured as 25.1 μV (marked in red), leading to an artifact suppression of 22.9 dB. C: Equivalent of A for Case 2. The largest artifact was recorded as 767.2 μV. D: Equivalent of B for Case 2 (canceling pair 13-8 with $\beta = 13\%$, leading to 11.5 dB artifact suppression). E: Equivalent of A for Case 3. The largest artifact was recorded as 151.2 μV. F: Equivalent of B for Case 3 (canceling pair 6-13 with $\beta = 10\%$, leading to 13.6 dB artifact suppression). G: Equivalent of A for Case 4. The largest artifact was recorded as 2693 μV. H: Equivalent of B for Case 4 (canceling pair 5-29 with $\beta = 25\%$, leading to 2.6 dB artifact suppression).

that the artifact due to cancellation is still smaller than that due to the primary stimulation. For larger β values, the artifact suppression decreases (even becomes negative) as the artifact due to cancellation starts to dominate. For canceling dipole 22-14, even with a β of 20%, the artifact due to primary stimulation still dominates and artifact suppression shows a monotonic behavior. This is because the electrode pair 22-14 is in the vicinity of the primary stimulation, which requires larger β to achieve the same amount of artifact suppression as

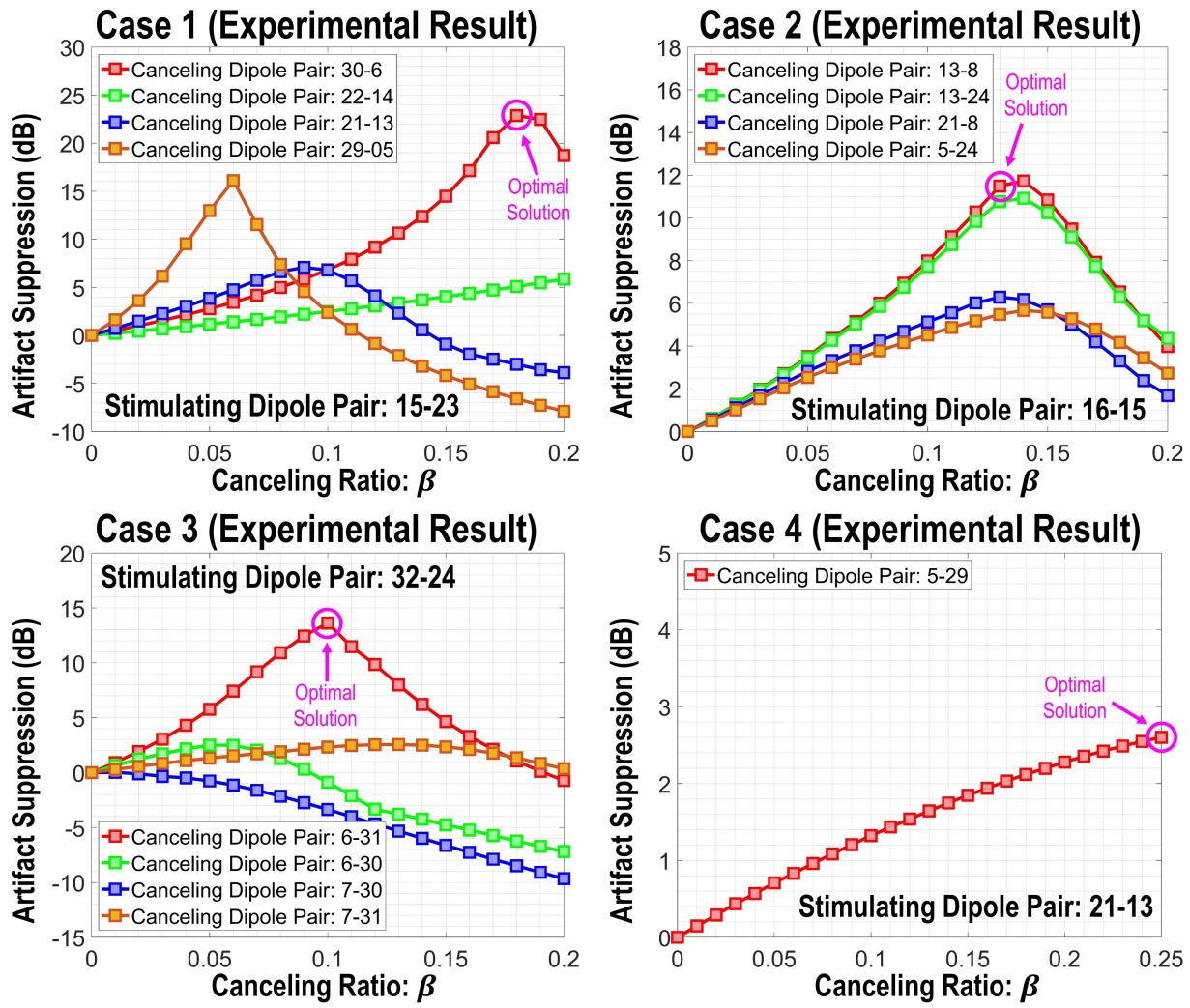


Figure 2.8: **Perturbation analysis: experimental results.** In Case 1, the perturbations of canceling dipole location and β demonstrate inferior artifact suppression compared to the optimal solution (marked in magenta) found by the optimization algorithm. In Case 2, instead of the optimal solution (electrode pair 13-8 with $\beta = 13\%$), the same canceling dipole with $\beta = 14\%$ demonstrates the largest artifact suppression. Similarly to Case 1, Case 3 exhibits superiority of the optimal solutions. In Case 4, the artifact suppression increases monotonically with β as predicted. The largest artifact suppression happens when β reaches 25% (limited by IC). This result is consistent with the optimal solution found by the optimization algorithm.

the other canceling dipoles in this case.

For Case 2, the optimal solution for the simulation and experiment were similar except for a 1% difference in β. Additionally, the artifact suppression plots for the electrode pairs 13-24 and 13-8 closely follow one another with the latter providing slightly better cancellation. This

slight improvement was also captured by the simulation, as shown in Fig. 2.6, which further proves the necessity of this algorithm for cases where visual inspection alone is incapable of finding the optimal solutions.

For Case 3, the optimal solution found by the algorithm was confirmed experimentally. In Case 4, the optimal solution also matches the one found experimentally. In addition, the artifact suppression increases monotonically, as also observed in Fig. 2.6. The reason for keeping $\beta \leq 25\%$ is that, beyond this point, the optimization algorithm found IC to be violated (IF exceeds α). Note that calculating IF requires a full 3D voltage distribution, which is achievable in simulations but not experimentally. Therefore, in our experiments, we chose the same range of β values as in simulations.

In summary, the experimentally optimal canceling patterns closely follow the optimal one found by the proposed optimization algorithm. Additionally, comparing Fig. 2.6 with Fig. 2.8 verifies that the results from phantom tissue experiments match those from simulations.

2.4 Discussion

In this work, we have developed an optimization framework based on the electric dipole model to optimally suppress stimulation artifacts across ECoG recording electrodes. Our simulation and experimental results confirmed that the optimal canceling patterns found by the algorithm provided superior artifact suppression compared to other solutions. Additionally, the optimal canceling dipole found by the algorithm performed consistently in both simulations and experiments (there was only a minor disagreement in Case 2, where β was off by 1%). Generally, experimentally measured artifacts were stronger than the simulated ones (see Table 2.5). This discrepancy could be explained by the model assuming an unbounded, isotropic, and homogeneous volume conduction. In contrast, for the phantom

tissue placed in a Petri dish, this assumption generally does not hold. Its finite volume and non-negligible boundary conditions may have resulted in a stronger electric field than the dipole model's prediction. Additionally, the model assumed infinitely far reference, whereas in experiments, the reference electrode was typically 3 cm to 9 cm away. Infinitely far reference could be mimicked experimentally by placing the reference electrode at the intersection of the stimulating and canceling dipole axes (e.g., Fig. 2.4: Case 1). However, this was not always possible (e.g., Fig. 2.4: Case 3). Nevertheless, these discrepancies did not seem to affect the solution, i.e., the optimal canceling patterns were nearly identical in simulations and experiments.

An important feature of our technique is that it suppresses artifacts before they reach recording electrodes. This feature is especially useful for future fully implantable BD-BCIs, which will require ULP operation and will, therefore, be highly susceptible to amplifier saturation. In contrast, existing artifact mitigation techniques, whether focused on analog front-ends [23, 24] or digital filtering [23, 25, 26], require that the recorded signals remain in the linear region (without saturation). For example, [23] used adaptive filters to estimate the artifact contribution to recorded signals, followed by the subtraction of these artifact components before amplification at the front-end. Although capable of achieving large artifact suppression (42 dB), this technique is not applicable if the front-end is saturated. The technique in [42] proposed artifact cancellation by exploiting symmetrical differential stimulation. However, this technique places constraints on the spatial arrangement of stimulation and recording channels. In contrast, our approach was validated using four different cases, underscoring the applicability of our method under a variety of spatial arrangements. Finally, we note that our method can be used in conjunction with these existing artifact mitigation techniques, which can lead to further suppression of stimulation artifacts.

In conclusion, the simulation and experimental results suggest that our artifact cancellation approach, along with the optimization framework, could be used in future fully-implantable

BD-BCI systems to significantly suppress stimulation artifacts or protect its ULP front-end from saturation.

2.4.1 Constraint Parameters $\beta_{\max}$ and α

In clinical practice, I_s is typically chosen as the minimum current exceeding the sensation threshold. Thus, theoretically, any $\beta < 100\%$ should not cause unwanted sensation (see Section 2.2.2). Since brain tissue excitability is location dependent [18], we limited the amplitude of the auxiliary stimulation by setting $\beta_{\max} = 50\%$. Our algorithm yielded the optimal values of β ranging from 10% to 25% (See Figs. 2.6 and 2.8), suggesting that $\beta_{\max}$ was chosen appropriately. From an optimization standpoint, this means that the constraint SC was not active. For practical applications, $\beta_{\max}$ must be determined empirically, although the values obtained in this study may serve as an informed initial guess.

To reduce the interference of auxiliary stimulation with the primary stimulation (see Section 2.2.2), we chose $\alpha = 0.5\%$ as an arbitrary small number. However, in practical applications, α must be chosen empirically. If this value is not sufficiently small, then the primary stimulation dipole may be weakened by the auxiliary dipole to the point of no longer eliciting sensation. A potential mitigation strategy then would be to increase the primary stimulating current, I_s, above the sensation threshold to compensate for this interference. Note that the upper bound on I_s is determined by the FDA charge density guidelines. For example, since the sensation can be elicited with as low as 12.7 μC/cm^2/phase [18], which is lower than the FDA recommended safety limit of 25 μC/cm^2/phase [43], the above strategy of countering interference by increasing I_s seems feasible.

2.4.2 Multi-polar Cancellation

In this study, a single canceling dipole ($N = 1$) was used. This limitation was imposed by the complexity of the experimental setup and the need to synchronize two independent function generators (Introducing additionally canceling dipole would require yet another function generator to be added). However, the simulation results (figures omitted in the interest of space) indicate that $N = 2$ provides a superior solution. For example in Case 1, the artifact suppression went from 28.7 dB ($N = 1$) to 39.5 dB ($N = 2$). Although multi-dipolar cancellation ($N > 1$) can boost the artifact suppression, it will also increase computational cost because the run time of the algorithm increases exponentially with N. Additionally, it leads to an increase in power consumption which is highly undesirable in fully-implantable devices. This trade-off between power consumption and artifact cancellation suggests that N needs to be chosen empirically in practice to prevent the front-end amplifiers from reaching saturation. Our future plans involve designing a multi-polar stimulator that will seamlessly integrate all the features of this optimization algorithm. In addition, human tests will be conducted. However, these tests require FDA clearance and thus could not be performed at this point.

2.4.3 Limitations

Limitation Due to Grid Geometry

Our approach is primarily limited by the number of electrodes available for cancellation. Take for example Case 4, where the primary dipole lies adjacent to the recording electrodes. However, the addition of auxiliary stimulation may still suppress artifacts (cf. Table 2.5), which could mean the difference between saturation and non-saturation. Ultimately, our approach may not always succeed in cases like this. However, these extremely unfavorable

primary dipole configurations are not very likely to occur. These considerations also suggest that our technique would favor higher-density ECoG grids [44], as there is a larger solution space to search over.

Single Tone Verification

We chose a single 89-Hz tone as our test signal rather than a broadband biphasic square pulse train to simplify data analysis (see Section 2.2.3). Compared to a single tone, the group delay varies across frequency for broadband signals. However, we previously showed that the peaks of stimulation artifacts are tightly phase-locked across spatially distributed ECoG electrodes [32,33], suggesting that the capacitive effects can be neglected. Therefore, the results from this study are expected to generalize to more realistic broadband stimulation signals.

Computational Efficiency

The execution times (Table 2.4) show that the algorithm can produce solutions within seconds for a relatively small (4×4) grid. Generally, the complexity of the algorithm scales quadratically with the number of electrodes ($\mathcal{O}(n^2)$), which given a typical grid size of 32 electrodes, is not expected to cause any computational concerns. The problem becomes exponentially more complex with multi-dipolar ($N > 1$) cancellations. For example, for $N = 2$ the run times were 5-10 min. For larger grids, this could become prohibitively expensive and these computations could be accelerated by finding β through a gradient descent approach. Note, however, that unlike the search method employed here, such an approach may return a locally optimal solution.

Curvature of the ECoG Grid

We assumed that the recording and stimulating grids lie on a planar surface (A.1), which is justified for sensory and motor cortices—the primary areas of interest in BD-BCI applications. Consequently, our simulations and experimental set up were designed to reflect this situation. Note, however, that the dipole model and the interference constraint are natively 3D, and so our approach could be extended to cortical surfaces with prominent curvature. The experimental validation of such a scenario would, however, be challenging and was not pursued in this study.

2.5 Conclusion

This work presents a novel technique for the suppression of artifacts due to cortical electrostimulation. The method introduces auxiliary (canceling) dipoles and proceeds to find the parameters of these dipoles through a constrained optimization framework. These optimal canceling patterns significantly reduce the stimulation artifacts before they reach the recording grid and analog front-ends, which can potentially prevent amplifiers from saturation. Our method is especially useful in future fully-implantable BCI systems which are required to operate in an ULP regime and are therefore highly susceptible to saturation. In addition, our method is compatible with existing techniques which could collectively result in an even greater degree of artifact suppression. Our future plans involve the development of a custom ULP cortical stimulator that can seamlessly integrate multi-polar features and the synchronization of primary and auxiliary dipoles. We will also test the function of such a stimulator in humans.

Chapter 3

A CMOS BCI Prototype with 2-mV Precision Time-Based Charge Balancing and Stimulation-Side Artifact Suppression

3.1 Introduction

An estimated half a million people worldwide suffer from spinal cord injury (SCI) [45] and its lifelong complications each year, and currently no biomedical solution exists to restore motor and sensory functions after SCI. Implantable bi-directional brain-computer interfaces (BD-BCIs) are emerging platforms that could enable future closed-loop therapeutic devices to restore sensorimotor function. Such BD-BCIs are required to perform two major concurrent tasks: stimulation and recording. Electrical brain stimulation technique excites neurons in the brain by injecting current pulses through electrodes. To accommodate different modal-

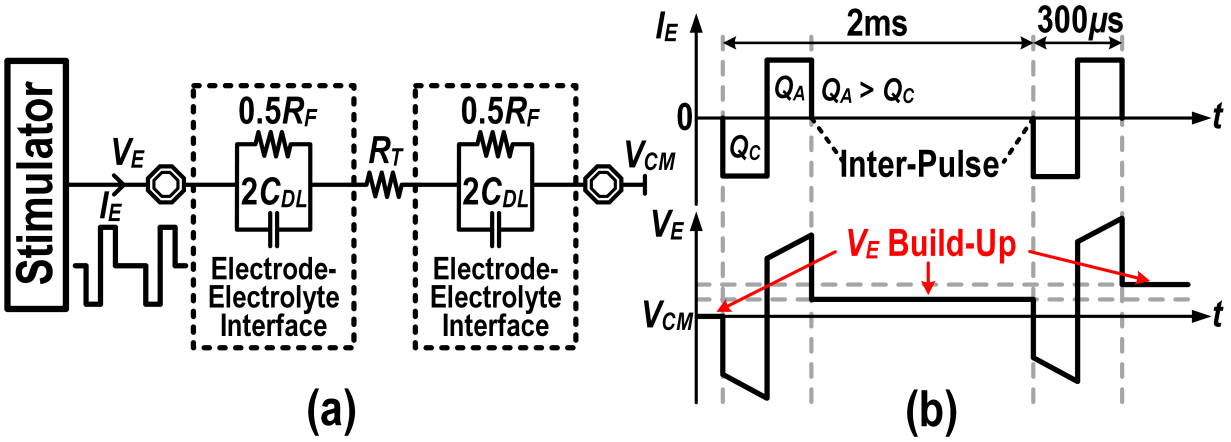


Figure 3.1: (a) Brain stimulation electrical model, assuming electrode-electrolyte interfaces have the same impedance. (b) Typical waveforms of the stimulation current through the electrode, I_E, and the voltage appearing on electrode, V_E.

ities, stimulators are required to be highly configurable, especially in terms of stimulation current and voltage compliance. For instance, cortical stimulation using electrocorticography (ECoG) grids requires up to 10 mA of current to elicit artificial sensation, whereas deep brain stimulation (DBS) needs only a few hundreds of μA [18, 46]. Furthermore, the required voltage compliance must account for the tissue impedance for the maximum stimulation current, which can be as high as few kΩ [40]. Thus, stimulators, in principle, require high-voltage (HV) programmable supplies ranging from few volts to a few tens of volts.

The brain stimulation electrical model is shown in Fig. 3.1(a). The brain tissue is represented by a resistor, R_T, and each electrode-electrolyte interface is modeled as a double-layer capacitor, $2C_{DL}$, in parallel with a Faradaic resistor, $0.5R_F$ [9]. Fig. 3.1(b) shows the typical waveforms of stimulation current, I_E, and voltage, V_E, appearing on the electrode. V_{CM} denotes the body's quiescent potential. Because of the mismatch between positive and negative current pulses, a voltage build-up may occur on the electrode, as depicted in the inter-pulse time interval. The voltage across double layer capacitors slowly decays through each Faradaic resistor during this interval, leading to long-term unidirectional charge transfer. Consequently, this charge accumulation on the electrode leads to voltage build-up, causing electrode corrosion and tissue damage [9]. To solve this issue, several charge balancing techniques have

been introduced by prior works. Passive charge balancing [47] performs electrode shortening by turning on a low resistive discharge path between V_E and V_{CM} in the inter-pulse time interval to remove the residual charges in the interfaces. However, the discharging current is not well-controlled and determining the resistance of the discharge path requires a-priori knowledge of the interface characteristics. The charge-pack injection (CPI) technique [48–52] uses well-controlled charge packs to remove the residual voltage on the stimulating electrode following each stimulation, while avoiding false sensation. However, it requires a predefined charge for each pack, which highly depends on the interface characteristics. In addition, CPI suffers from a strict trade-off between compensation time (i.e., shorter compensation time with larger pack) and accuracy (i.e., higher accuracy with smaller pack). Dynamic current mirrors (DCMs) [53–55] monitor and balance the anodic and cathodic charges during stimulation. However, its charge balancing accuracy is limited due to the absence of closed-loop monitoring of the residual voltage and the inability to capture current transient mismatches. Offset regulation (OR) technique [47, 49, 56] creates a compensating current continuously injected to the interface as an offset current in the background. Although it monitors the voltage on the electrode in a closed-loop fashion, OR is unable to remove the residual charge after each stimulation pulse and requires a long settling time when the stimulator initially starts or the stimulation waveform changes. Other charge balancing approaches, such as inter-pulse charge control (IPCC) [47], do not incorporate well-controlled compensation current and pulse-width, thus leading to false sensation. Based on the work presented in [57], this paper presents a time-based charge balancing (TBCB) technique capable of establishing both closed-loop monitoring of the residual voltage and well-controlled charge injection to avoid false sensation. Additionally, TBCB breaks the tight trade-off between compensation time and accuracy, and performs effective charge balancing without requiring a-priori knowledge of the interface characteristics.

When being used to realize the closed-loop operation in BD-BCIs, electrical brain stimulation induces undesired artifacts in the neural recordings. The presence of artifacts imposes

excessive dynamic-range requirement on the recording sub-system, which calls for artifact cancellation techniques. Recently, several studies [11, 12, 58] have demonstrated the significance of localizing tissue activation by shaping the electric field within the brain. In practice, the geometry of electrode grids poses a strict constraint on the location of brain stimulation. In addition, voltage distributions created by monopolar or bipolar stimulation cannot be confined completely to the vicinity of stimulating electrodes [4]. As such, these stimulations tend to cause severe artifacts, which may result in performance degradation or even saturation of the analog recording front-ends in a BD-BCI system. By employing multipolar and multi-site stimulation, the electric field potential changes induced by the current injections are localized [11,12] and the stimulation artifacts propagating to the recording side are significantly suppressed [4, 13]. The proposed stimulation system is designed to accommodate multipolar and multi-site configuration as a way to localize neural activation, thereby achieving significant artifact suppression. It is worth noting that this multipolar stimulation requires each stimulator to have independent cathodic and anodic currents, which cannot be merely realized by conventional H-bridge-based topologies [24, 48, 59, 60] despite the fact that they tend to exhibit less anodic and cathodic mismatch. This charge imbalance induced by mismatch is mitigated by the proposed TBCB technique, as will be explained in Section 3.3.1.

Existing neural recording architectures based on conventional approach of acquiring brain signals with maximum frequency content are ill-suited for high channel-count real-time processing, as they consume significant power, thereby limiting the longevity of implantable BD-BCIs. One particular neural recording modality of interest is the minimally-invasive ECoG that is specifically useful for therapeutic implants targeting individuals with SCI condition. It has been observed that high spatiotemporal resolution ECoG recordings from primary motor cortex, M1, contain rich movement information (i.e., duration and speed) related to upper and lower extremities in γ-band, and in particular, high-γ ($\sim$ 80-160 Hz) band [61–65]. Hence, this notion inspires cognitive-driven signal acquisition and processing

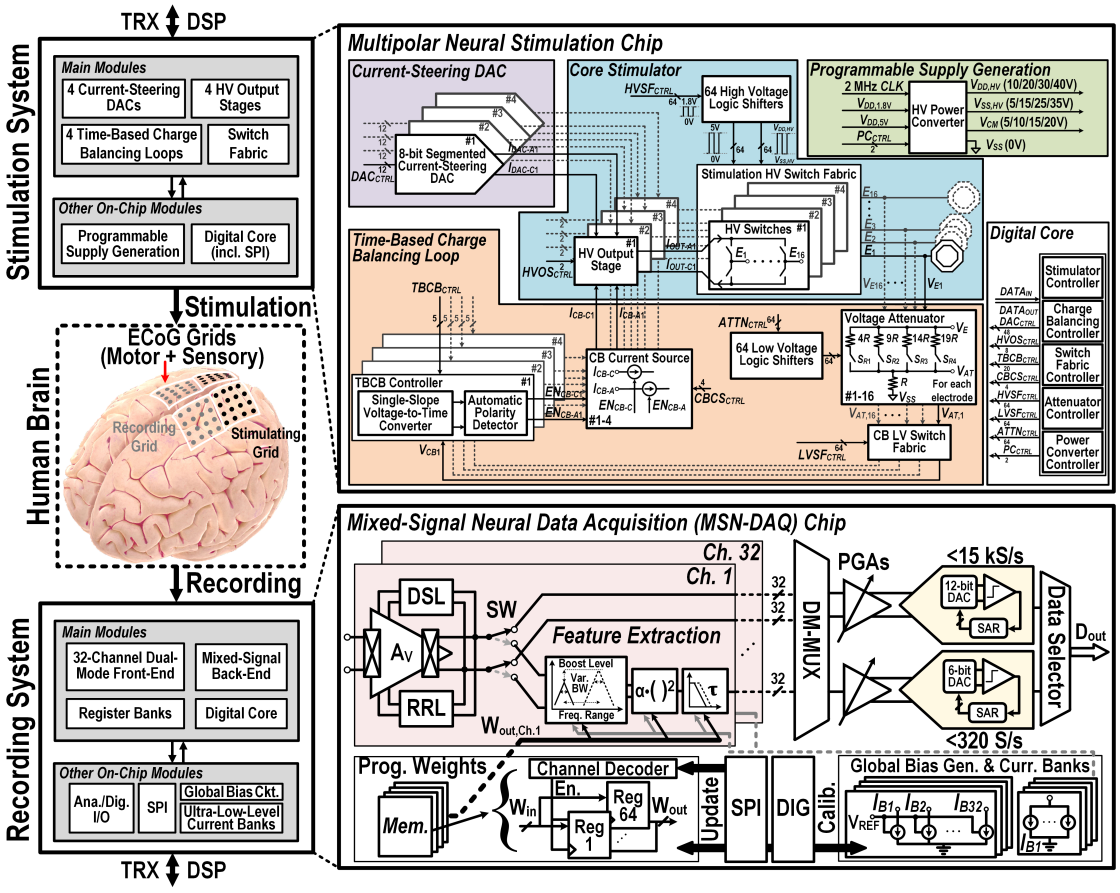


Figure 3.2: Architecture of the proposed BD-BCI system.

architectures that could potentially offer power-saving advantage by exploiting the intrinsic characteristics of neural signals, thus enhancing the system longevity. A plausible approach is to employ a dual-mode analog signal processing method in the neural data acquisition system, which facilitates extracting low-bandwidth neural features from high-γ band at the early stages of signal acquisition prior to digitization [66]. As a consequence, the dual-mode operation avoids the unduly high data processing rates and associated power dissipation in the digital back-end.

To realize a clinically-viable implantable BD-BCI, the aforementioned challenges are addressed in this work by introducing (1) precision time-based charge balancing, (2) stimulation-side contour shaping artifact cancellation, and (3) ultralow power (ULP), mixed-signal, dual-mode neural data acquisition. The rest of this paper is organized as follows. In Section 3.2, the top-level description of the proposed BD-BCI system is provided. The intuition be-

hind time-based charge balancing, stimulation-side contour shaping artifact cancellation, and ULP, mixed-signal, dual-mode neural acquisition are described in Section 3.3. The circuit implementations of the stimulation and recording systems are illustrated in Sections 3.4 and 3.5, respectively. The complete measurement results are presented in Section 3.6, and finally, the concluding remarks are given in Section 3.7.

3.2 Top-Level Description of the Proposed BD-BCI

The proposed BD-BCI chipset consists of a stimulation and a recording system, as indicated in Fig. 3.2. Each system is designed to interface with the ECoG grid placed over the motor and sensory cortices. In order to establish a bi-directional link between the BD-BCI chipset and end-effectors (e.g., base-station and exoskeleton), the proposed BD-BCI system is envisioned to incorporate additional modules such as digital signal processor (DSP) and transceiver (TRX), as depicted in Fig. 3.2. In the next two subsections, each individual system and its high-level implementation is further described.

3.2.1 Stimulation System

The proposed stimulation system is shown in Fig. 3.2, where at its core, four HV current-stimulators are connected to sixteen electrodes through an HV switch fabric. Each stimulator is capable of providing a maximum current of 12.75 mA, which is sufficient for cortical stimulation [18]. This current is generated by an 8-bit segmented current-steering DAC. In addition, a fully-integrated programmable power converter generates the necessary supply voltages to accommodate different bio-impedances.

The TBCB loop is enabled after each stimulation pulse. The loop starts with a voltage attenuator that senses the voltage on each stimulating electrode and lowers it down to 1.8-V

low-voltage (LV) regime. Subsequently, an LV switch fabric in the loop feeds this voltage to the corresponding TBCB controller. The TBCB controller - comprising a single-slope voltage-to-time converter (SSVTC) and an automatic polarity detector (APD) - generates a control signal with its duration proportional to the voltage sensed at the TBCB controller input. The TBCB loop function is completed by generating a compensation current pulse whose duration is controlled by the output of the TBCB controller, which is then fed back to the core stimulator to perform charge balancing. The operation details of each building block will be discussed in Section 3.4.

3.2.2 Recording System

Fig. 3.2 illustrates the top-level system block diagram of the ULP mixed-signal neural data acquisition (MSN-DAQ). The 32-channel dual-mode front-end array is accompanied with register banks to store the channel-specific programmable weights for feature extraction. The mixed-signal back-end and digital core consist of dual-mode multiplexer (DM-MUX), programmable gain amplifiers (PGAs), and ADCs with distinct bit-resolution and bandwidth tailor-made for training (i.e., full-band (FB)) and decoding (i.e., base-band (BB)) modes. Other on-chip blocks include serial peripheral interface (SPI) for communication and configuration, and bias circuits for global current generation which are tuned by external reference voltages (V_{REF}'s) applied to on-chip diode-connected current mirrors, digitally-controlled ultra-low current banks for local bias and analog/digital input-output (I/O) modules. Details of operation will be disclosed in Section 3.5.

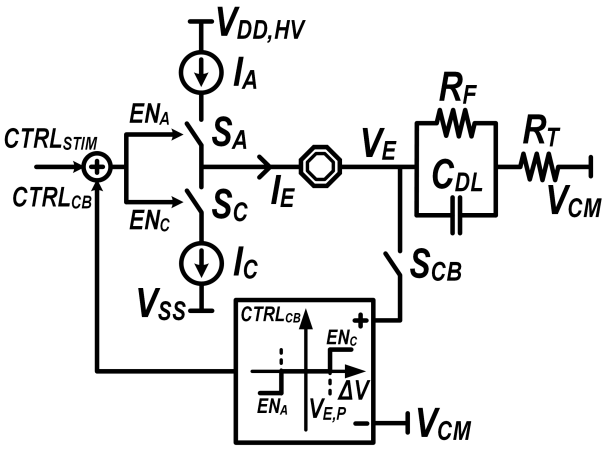


Figure 3.3: Conventional CPI loop.

3.3 Implantable BD-BCI Prerequisites and Proposed Design Philosophies

3.3.1 Time-Based Charge Balancing Technique

As mentioned in Section 4.1, CPI is one of the most widely used charge balancing methods (Fig. 3.3). It uses a feedback mechanism to monitor the residual voltage $V_E - V_{CM}$ and injects charge packs to the electrode-electrolyte interface in the inter-pulse time interval T_{IP} (Fig. 3.4) to compensate for the remaining charges [48–52]. Although this technique minimizes the residual charges on electrode after each stimulation pulse, and further provides a means of controlling both the maximum current and pulse-width to avoid false sensation, it suffers from the trade-off between charge balancing accuracy and compensation time. Through repetitive injections of compensation charge Q_X per cycle, the charge-pack injection loop is designed to converge to a desired residual voltage smaller than or equal to the charge-balancing voltage precision, $V_{E,P}$, after M cycles. This is mathematically expressed, as follows:

$$\frac{1}{C_{DL}}|Q_I - MQ_X| \leq V_{E,P} \tag{3.1}$$

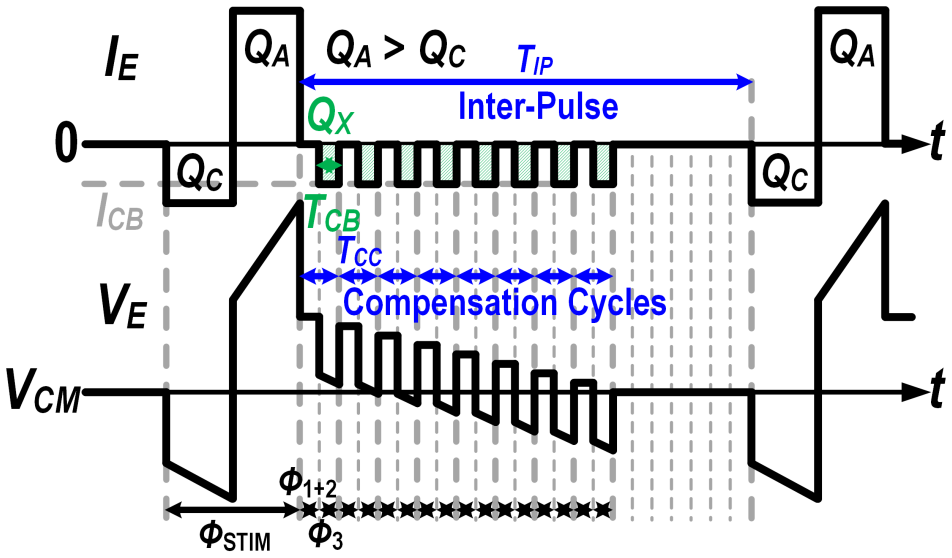


Figure 3.4: Typical electrode current I_E and voltage V_E for the conventional CPI technique. Note that the gradual dissipation of charge on C_{DL} through a typically very large R_F is omitted. Eq. (3.1) implies that for a fixed compensation period of T_{CC} and an initial charge imbalance of Q_I ($Q_I = Q_A - Q_C$), $V_{E,P}$ can be reduced by assigning smaller values of Q_X, but at the cost of increasing number of compensation cycles, M (i.e., compensation time). Consequently, if M that satisfies Eq. (3.1) exceeds the maximum allowable compensation cycles $M_{\max} = \lfloor T_{IP}/T_{CC} \rfloor$, CPI will be incapable of removing all the residual charges prior to the next stimulation pulse, thereby failing to perform effective charge balancing. Although lowering T_{CC} can increase $M_{\max}$, Q_X is reduced accordingly in the CPI scheme where a fixed current I_{CB} - imposed by the patient's sensation threshold - is utilized for charge balancing (Fig. 3.4). A smaller Q_X, in turn, leads to a larger M despite a shorter T_{CC} (Eq. (3.1)). Therefore, T_{CC} scaling has a limited impact on the reduction of the total charge balancing time. Additionally, to ensure convergence of the CPI technique, $V_{E,P}$ and Q_X should be chosen such that $V_{E,P} > \frac{Q_X}{2C_{DL}}$. In practice, due to the lack of knowledge about electrode-electrolyte interface (e.g., C_{DL} value), this technique requires a brute-force search to find the largest value of Q_X under a certain $V_{E,P}$ requirement.

Fig. 3.5 depicts the proposed TBCB technique. In essence, the TBCB loop consists of a voltage-to-time converter (VTC) and a compensating current source/sink. The TBCB loop

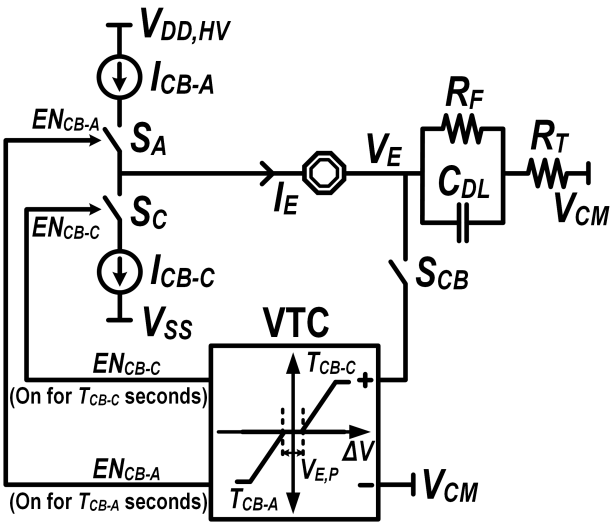


Figure 3.5: Proposed TBCB loop.

operates in three consecutive phases within each compensation period T_{CC}, following the biphasic pulse stimulation, as illustrated in Fig. 3.6. During ϕ_1, VTC is reset and auto-zeroing is performed to eliminate the input-referred voltage offset of the amplifier in VTC. In the next phase, ϕ_2, switch S_{CB} is activated and the residual voltage $\Delta V = V_E - V_{CM}$ is applied to VTC, which conducts sample-and-hold operation on ΔV (Fig. 3.5). Both ϕ_1 and ϕ_2 are very small in duration, as shown in Fig. 3.6. Next, in ϕ_3, the TBCB loop starts compensating for the residual charges. Referring to Fig. 3.6, the compensation current I_{CB} during ϕ_3 is a fixed amount, whereas the compensation time $T_{CB,n}$ associated with the n^{th} compensation cycle and produced by VTC is a continuously varying quantity proportional to ΔV_n sensed during ϕ_2. Consequently, $Q[n]$ accepts a value commensurate with ΔV_n.

The detailed operation of VTC itself is, as follows: For ΔV greater than a circuit-dependent threshold V_{TH} (Fig. 3.6), $T_{CB,1}$ is ultimately limited by the duration of ϕ_3, T_{ϕ_3} (i.e., $T_{CB,1} = T_{\phi_3} = T_{CC} - T_{\phi_{1+2}}$). T_{ϕ_3} is obtained based on the patient's sensation threshold during clinical trials so as to avoid false sensation. The maximum allowable compensation charge, $Q_{X,M}$, is created during $T_{CB,1}$ (i.e., $Q[1] = Q_{X,M}$) by I_{CB-A} or I_{CB-C} to obliterate the residual charges over this T_{CC} period (Case 1), as shown in Fig. 3.6. It is worth mentioning that $Q_{X,M}$ could be much greater than Q_X in the CPI technique. On the other hand, for a

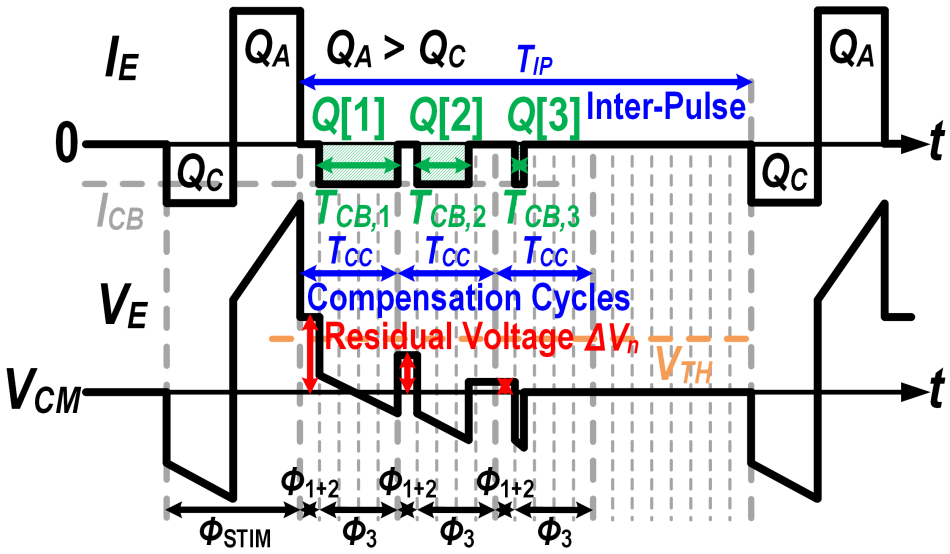


Figure 3.6: Typical waveforms of the current through the electrode, I_E and the voltage on electrode, V_E for the proposed TBCB technique.

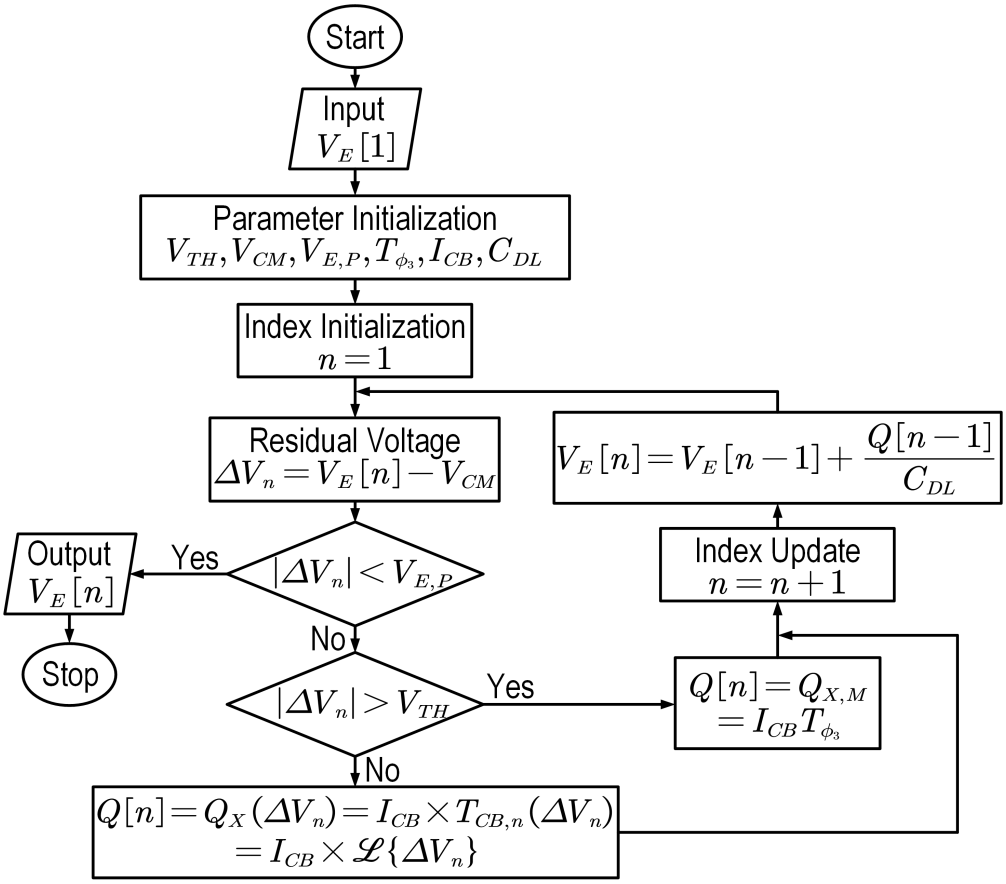


Figure 3.7: Operation of the proposed TBCB loop.

residual voltage less than V_{TH}, VTC creates a $T_{CB,n}$ proportional to $V_E - V_{CM}$ and the operation falls into the linear region characterized by $T_{CB,n}(\Delta V_n) = \mathscr{L}\{\Delta V_n\}$, where $\mathscr{L}\{\cdot\}$

represents a linear function. Correspondingly, $T_{CB,n}$ only takes a portion of T_{ϕ_3} (Case 2) (Fig. 3.6). If $V_E - V_{CM}$ is very small and close to $V_{E,P}$, $Q[n]$ becomes much smaller than Q_X in CPI, thereby significantly increasing charge balancing accuracy. Finally, for residual voltages falling within a small sensitivity zone $\pm V_{E,P}$ (e.g., ±2-mV), the charge balancing loop will turn off for all the succeeding compensation cycles to avoid toggling (Case 3). The operation of the proposed TBCB loop is summarized by the flow-chart in Fig. 3.7 and is formulated, as follows:

$$\Delta V_n = \begin{cases} \Delta V_{n-1} + \dfrac{I_{CB} T_{\phi_3}}{C_{DL}}, & \text{if } |\Delta V_{n-1}| \geqslant V_{TH} \\ \Delta V_{n-1} + \dfrac{I_{CB} \cdot \mathscr{L}\{\Delta V_{n-1}\}}{C_{DL}}, & \text{if } V_{E,P} \leqslant |\Delta V_{n-1}| \leqslant V_{TH} \\ \Delta V_{n-1}, & \text{if } |\Delta V_{n-1}| \leqslant V_{E,P} \end{cases} \tag{3.2}$$

Although the cycle-by-cycle operation is discrete-time, within each T_{CC}, the TBCB loop essentially performs continuous-time operation. During the compensation cycle in which $V_{E,P} \leqslant |\Delta V_n| \leqslant V_{TH}$, the compensation charge $Q[n] = I_{CB} \times \mathscr{L}\{\Delta V_n\}$ is generated by a fixed charge balancing current I_{CB} over a "continuously varying" time interval, $T_{CB,n}$. This continuous-time operation draws a major distinction between TBCB and CPI, in that, the residual charge compensation is performed by quantized charge packs in CPI that inevitably yields a finite quantization error. Consequently, Eq. (3.1) will no longer hold for TBCB and $V_{E,P}$ value can, in fact, be arbitrarily small without the need for increasing compensation time. Therefore, the proposed TBCB technique mitigates the trade-off between compensation time and accuracy. In addition, as shown in Figs. 3.5 and 3.7, when ΔV_n comes very close to $V_{E,P}$, an arbitrarily small $Q[n]$ is generated and the condition of convergence ($V_{E,P} > \frac{Q[n]}{2C_{DL}}$) can be satisfied for an arbitrarily small $V_{E,P}$. Therefore, the charge balancing accuracy $V_{E,P}$ in TBCB is only limited by the imperfections, such as offset voltage created by transistor mismatches and charge injection of switches, and is independent of Q_I, charge

balancing time, and the interface characteristics.

Fig. 3.8 shows three examples that compare the proposed TBCB technique with the conventional CPI method. The comparison is made under the assumptions that both TBCB and CPI use the same clock frequency to synchronize the charge balancing operation, and the detection phases ϕ_{1+2} in Figs. 3.4 and 3.6 take one clock period T_{CLK} for both (Fig. 3.8). In addition, the initial charge imbalance is assumed to be $Q_I = 8.6 I_E T_{CLK}$, which is a non-integer multiple of $I_E T_{CLK}$. For demonstration purpose, in the TBCB example, $T_{CC} = 5T_{CLK}$, while in the two CPI examples shown in Fig. 3.8, $T_{CC} = 2T_{CLK}$ and $3T_{CLK}$, respectively. It is worth mentioning that the charge pack Q_X used in the two CPI examples are $I_E T_{CLK}$ and $2I_E T_{CLK}$, respectively (Fig. 3.8). As mentioned above, the guaranteed convergence of TBCB allows $V_{E,P}$ to be very small such that the total compensation charge $Q_{X,\text{tot}} = Q[1] + Q[2] + Q[3] = Q_I$. On the other hand, the condition of convergence in CPI forces $V_{E,P}$ to be larger than the values indicated in Fig. 3.8. Additionally, the use of quantized charge pack in CPI leads to unmitigated charge errors. Specifically, for $Q_X = I_E T_{CLK}$, $Q_{X,\text{tot}} = 9 I_E T_{CLK}$ is close to the nearest integer of Q_I, leaving a charge error of $0.4 I_E T_{CLK}$. Similarly, for $Q_X = 2 I_E T_{CLK}$, a charge error of $0.6 I_E T_{CLK}$ will remain uncompensated, as shown in Fig. 3.8. Therefore, TBCB can achieve much higher charge balancing accuracy than CPI. It is noteworthy that T_{CC} can be greatly reduced to significantly lower $V_{E,P}$ in the CPI technique, thereby improving charge balancing accuracy. However, this leads to a dramatic increase in the clock frequency.

Unlike CPI that uses only the polarity information of the residual voltage, TBCB employs both the polarity and amplitude of ΔV to determine the polarity of compensating charge and pulse-width of I_{CB}. The amplitude detection and VTC operations in the TBCB technique increase power consumption when compared to CPI. Nevertheless, the major sources of power consumption in both methods stem from circuits responsible for the charge delivery to the tissue, because they operate in HV domain as opposed to the detection circuits operating

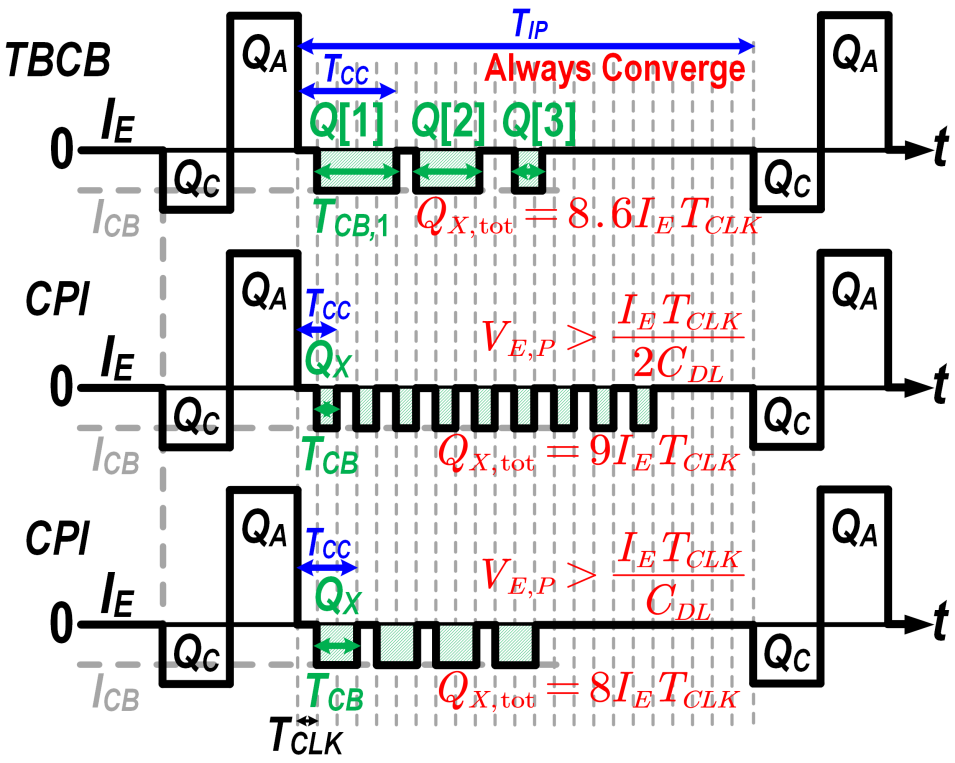


Figure 3.8: Comparison of the proposed TBCB and the conventional CPI techniques.

in LV domain. Therefore, the extra power consumption overhead in TBCB contributes negligibly to the overall power consumption of the charge balancing operation.

3.3.2 Stimulation-Side Contour Shaping Artifact Cancellation

In this work, the stimulation-side contour shaping (SSCS) technique is used as the main artifact cancellation method. This technique is based on the electric field potential distributions within the brain tissue. To understand the voltage characteristics caused by the stimulation in the brain tissue under bi-directional multi-site stimulation and recording, the monopole model is applied to each current source or sink to calculate the voltages induced at various locations [4, 13]. One example of multipolar, multi-site stimulation involves a primary stimulating dipole and a canceling dipole to form two pairs of current sources and sinks [4]. As shown in Fig. 3.9, electrode 24 and 16 form a primary stimulating dipole and deliver 10 mA

current to the tissue. Concurrently, a canceling dipole (electrode 7 and 31) with reversed polarity is introduced between the primary stimulating dipole and recording side to reshape artifact contours. With rapid attenuation of artifacts through the conductive medium of the brain, the cancellation magnitude can be made smaller than the primary stimulation (e.g., 1.25 mA). Hence, the canceling dipole causes no degradation of the artificial sensation, while significantly suppresses the artifacts on the recording electrodes without incurring any power overhead on the recording system. SSCS essentially reshapes the spatial distribution of artifacts, and as such, its performance is dependent on stimulation location. Nevertheless, since SSCS is on stimulation side, it is complementary to existing recording-side artifact cancellation techniques, such as adaptive filtering [60] and track-and-zoom [67]. Therefore, if used together, they can further suppress stimulation artifacts.

3.3.3 Ultralow Power Dual-Mode Neural Data Acquisition

Shown in Fig. 3.10 is a typical multi-channel neural interface consisting of a data acquisition (DAQ), a DSP, and a TRX. The neural recording architectures employed in DAQ are commonly based on conventional topologies such as capacitively-coupled InAmp+ADC [68], DC-coupled digitally-assisted amplifier [69] and direct conversion (time-based [70], delta-sigma [71, 72]) schemes. These approaches target acquisition and digitization of the brain signals across a wide range of frequencies (near DC up to 1 kHz) that leads to an excess dynamic range and bandwidth, resulting in an unduly high data throughput. Hence, a significant power and computing burden is placed on DSP and TRX, introducing a prominent data-processing power bottleneck for massive channel-count systems [73].

Since the most relevant physiological neural information, such as movement intentions, is often found within a fraction of brain signal frequency range (e.g., high-γ band) whose content requires significantly less dynamic range and bandwidth compared to the raw neural

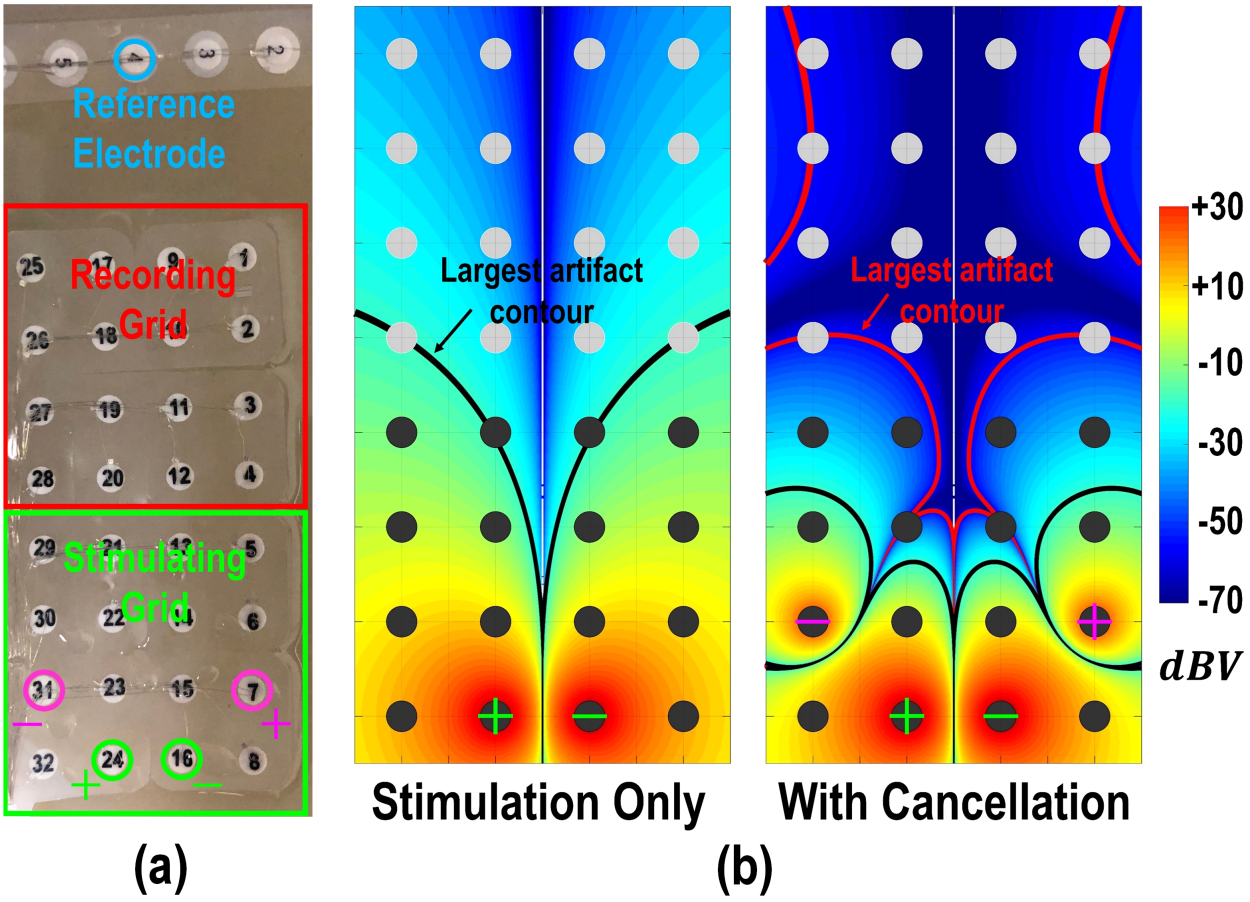


Figure 3.9: (a) Physical configuration of the stimulation electrodes, stimulating and recording grids [4]. (b) Voltage spatial distributions under stimulation only and stimulation + cancellation conditions. Grey: recording grid. Black: stimulating grid. Green: primary stimulating source and sink electrodes. Magenta: canceling source and sink electrodes.

signal [65], a cognitive-driven DAQ is highly desired to address this major power bottleneck. Inspired by our work in [66], the proposed MSN-DAQ allows dual-mode acquisition that is capable of extracting useful neural features in the analog domain via a highly reconfigurable analog signal processing (ASP) unit, which significantly relaxes the system-level requirements (e.g., data throughput and power dissipation) to enable prolonged operation time in implantable BD-BCIs.

The power-saving advantage of the dual-mode operation in MSN-DAQ can be quantified by

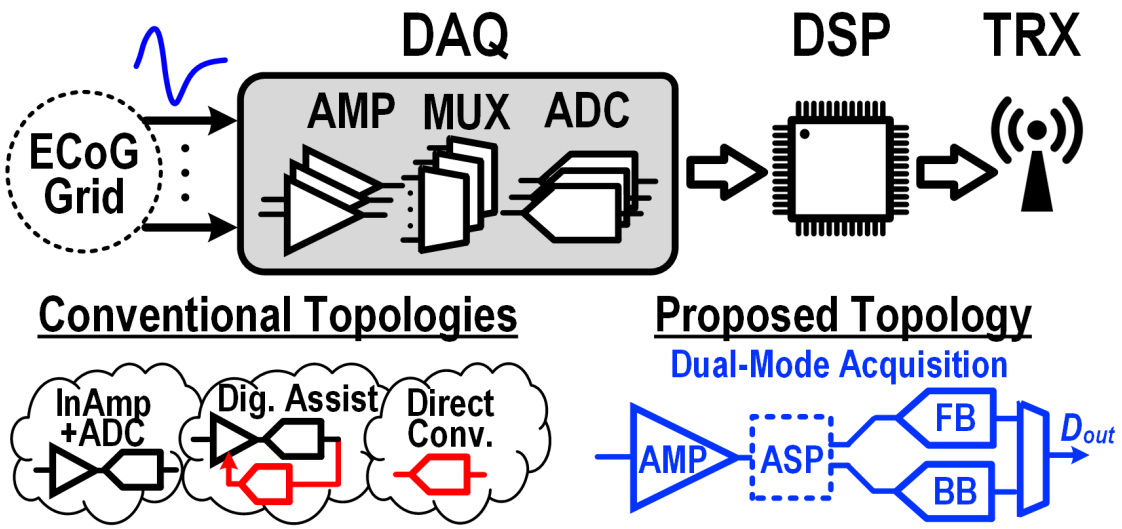


Figure 3.10: Conventional and proposed topologies for data acquisition system.

the power ratio, H, defined and expressed as:

$$H \triangleq \frac{P_{FB}}{P_{BB}} \approx \frac{S+1}{\alpha \cdot S + \eta} \tag{3.3}$$

Eq. (3.3) is a compact form of Eq. (1) in [66] for m=1. $S = [1 + P_D/(N \times P_U)]^{-1}$, $\eta = (f_{s,FB}/f_{s,BB})^{-1}$ and α is a multiplier factor representing the power overhead introduced by the dual-mode operation in the analog front-end. N, P_D, and P_U represent the number of channels and power consumption of digital processing unit and front-end amplifier, respectively. Additionally, η represents the ratio of sampling rates in BB- and FB-mode operations. To gain better insight into H, each amplifier is assumed to consume no more than 0.8 μW per channel with $\alpha = 1.25$ and $\eta = 0.02$, as studied comprehensively in [66]. For a 32-channel neural signal acquisition and processing system, the recently published results from a fabricated 130-nm system-on-chip in [74] are used to estimate the power consumption of the digital back-end. Since a brain-state classifier with similar classification rate (e.g., 4 Hz) as reported in [74] can be employed for decoding movement intentions, its associated power dissipation (i.e., 476 μW) is used to approximate H. In this case, the dual-mode operation can achieve a 12-fold improvement in the overall power consumption.

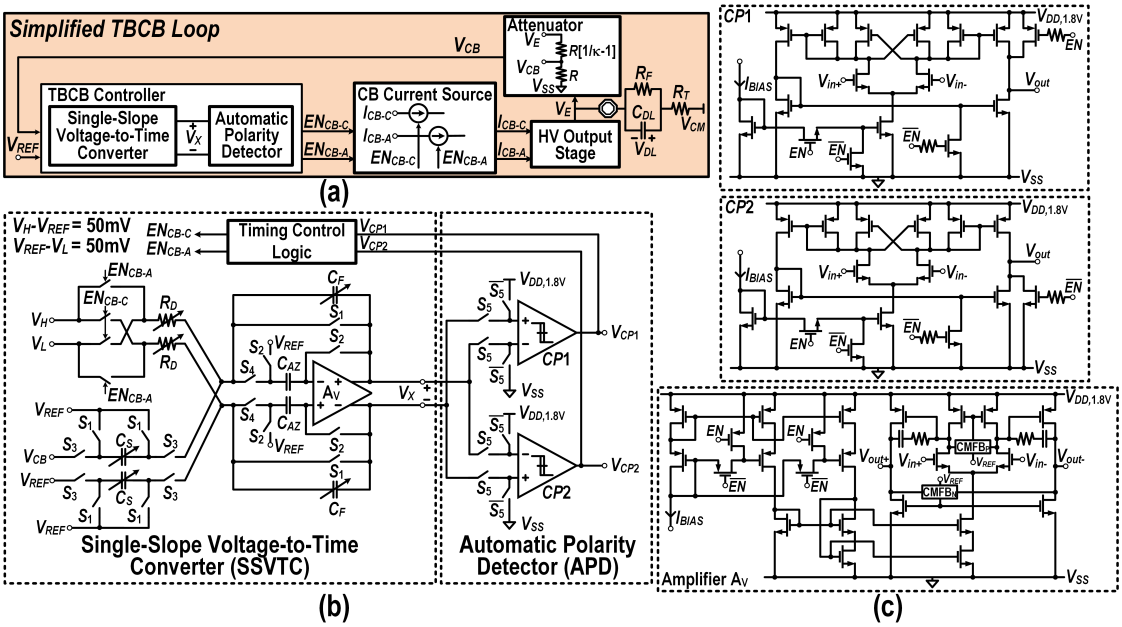


Figure 3.11: (a) Simplified time-based charge balancing loop. (b) Circuit implementation of the TBCB controller. (c) Circuit schematics of comparators CP1 and CP2, and amplifier A_V.

3.4 Stimulation Circuit Implementation

3.4.1 Time-Based Charge Balancing Controller

A simplified block diagram of the TBCB loop is shown in Fig. 3.11(a). During the inter-pulse time interval, the attenuated version of V_E, V_{CB}, is compared against V_{REF} in low-voltage domain and the voltage difference is processed by the TBCB controller. VTC, described in Section 3.3.1, within the TBCB controller of Fig. 3.11(a) controls the duration of the charge balancing current, which is injected back to the electrode through HV output stage to perform charge balancing.

As mentioned in Section 3.3.1, VTC entails three phases of operation in each compensation period, ϕ_1, ϕ_2, and ϕ_3 with ϕ_1 and ϕ_2 each taking one and ϕ_3 K clock cycles ($K = 6$ in Fig. 3.12(a)). In addition, depending on the input voltage amplitude, three cases may occur. The details of VTC operation is shown in Fig. 3.11(b) and Fig. 3.12. Referring to Fig. 3.11(b) and Fig. 3.12(b), in the first phase of operation (ϕ_1), S_1 turns on and the charges

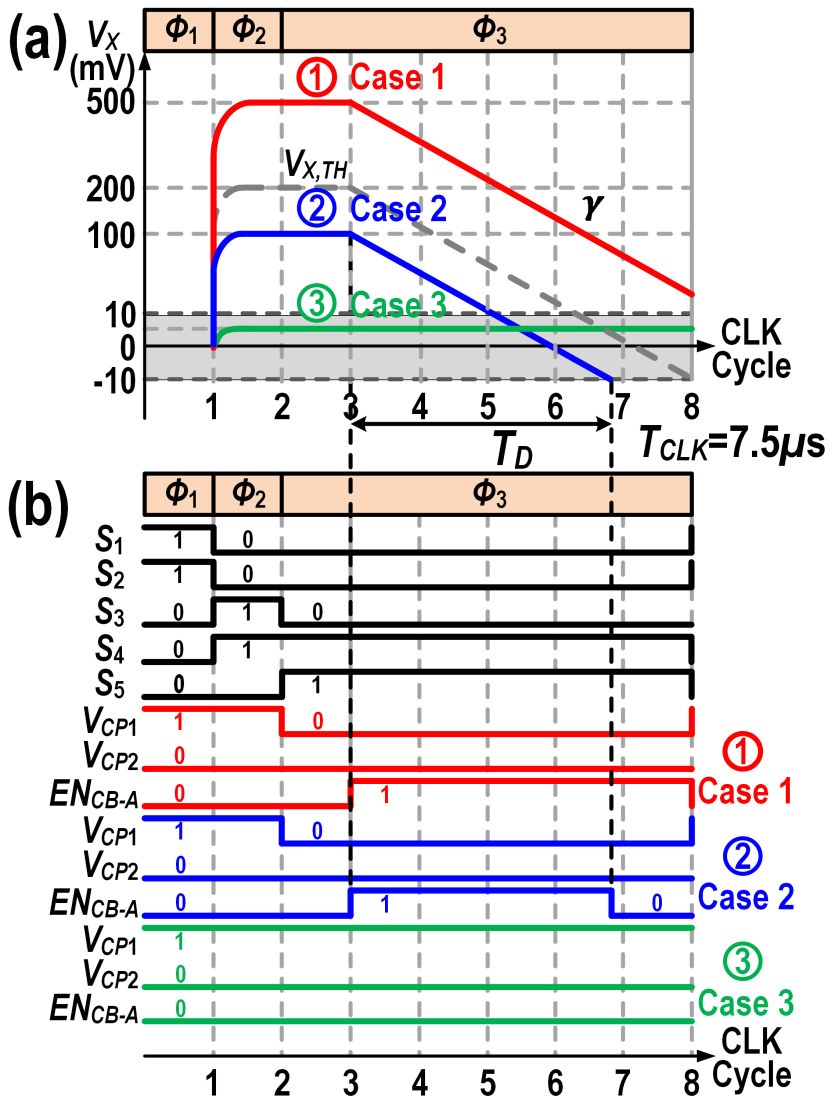


Figure 3.12: (a) Single-slope voltage characteristics of V_X at the output of amplifier. (b) Waveforms of the control signals, typical waveforms at the output of two comparators V_{CP1}, V_{CP2}, and charge balancing current control EN_{CB-A} under $V_X > 0$ condition.

on C_S and C_F are reset to zero. At the same time, S_2 turns on and the input-referred offset voltage of the amplifier A_V is stored on C_{AZ} to perform auto-zero offset cancellation. During this phase, S_5 is off and the output of the upper comparator $CP1$ is '1', while the lower comparator $CP2$ is connected in the opposite fashion and its output is thus '0'. In this phase, [V_{CP1},V_{CP2}] is logic '10' and the output EN_{CB-A} is off.

During ϕ_2, $S_{1\text{-}2}$ turn off and $S_{3\text{-}4}$ turn on. The sampled and amplified version of the input voltage is stored on C_F and appears as V_X at the amplifier's output whose magnitude is

proportional to the residual voltage on the electrode ($V_{DL} = -(V_E - V_{CM})$). Similar to operation in ϕ_1, S_5 is still off, thus [V_{CP1},V_{CP2}] will keep its '10' state and EN_{CB-A} will remain off.

At the beginning of ϕ_3, S_3 turns off and S_5 turns on. The two comparators in APD will determine the polarity of subsequent compensation current based on the V_X value attained at the end of ϕ_2. To be more specific, consider that both comparators are designed to exhibit a hysteresis of $\pm V_{\text{hys}}$ (= $\pm$10 mV). If V_X is larger than V_{hys}, [V_{CP1},V_{CP2}] will toggle from '10' to '00' in the first clock cycle of ϕ_3, as shown in Fig. 3.12(b). Subsequently, in the next clock cycle, EN_{CB-A} will turn on to start injecting anodic compensation current to the electrode. Similarly, if V_X is smaller than $-V_{\text{hys}}$, [V_{CP1},V_{CP2}] will change from '10' to '11' and EN_{CB-C} rather than EN_{CB-A} will turn on (for simplicity, only the operation of $V_X > 0$ is shown in Figs. 3.12(a)-(b)). Finally, if V_X is within $\pm V_{\text{hys}}$, due to comparators hysteresis, [V_{CP1},V_{CP2}] will keep its logic state of '10', as shown in Fig. 3.12(b): Case 3, and neither EN_{CB-A} nor EN_{CB-C} will turn on.

Following the study of APD in determining the polarity of charge balancing during ϕ_3, the operation principle of the SSVTC in this phase is further illustrated. As shown in Fig. 3.12(a), at the beginning of the second clock cycle of ϕ_3, EN_{CB-A} turns on and V_X starts to decrease at a constant rate γ. This rate is determined by the single-slope discharging of C_F through R_D ($\gamma = -\frac{V_H - V_L}{R_D C_F}$), as shown in Fig. 3.11(b). If $V_X > V_{X,TH} = -\gamma\,(K-1)\,T_{CLK} - V_{\text{hys}}$ at the end of ϕ_2 (Case 1), the discharging process through an enabled EN_{CB-A} will continue until the end of ϕ_3 (Fig. 3.12(a)). Otherwise, similar to Case 2, the discharging process will stop when V_X reaches $-V_{\text{hys}}$. In this way, the discharging time T_D ($T_D = -\frac{1}{\gamma}\,(V_X + V_{\text{hys}})$) is approximately proportional to V_X held at the end of ϕ_2, and hence, to the residual voltage sensed by the TBCB loop. As a result, the operation of the TBCB controller follows the time-based charge balancing principle introduced in Section 3.3.1.

The schematics of the two comparators in APD and the amplifier in SSVTC are shown in

Fig. 3.11(c). For the purpose of power saving, an enable signal EN turns off the TBCB circuitry after charge balancing is achieved. Both $CP1$ and $CP2$ are comprised of a first stage with cross-coupled load to provide high-gain amplification and a differential-to-single-ended second stage to increase driving capability. The hysteresis is realized by the internal positive feedback in the first stage and by sizing the cross-coupled PMOS pair slightly larger than the diode-connected pair [75]. When the TBCB loop is disabled, the outputs of $CP1$ and $CP2$ are set to logic '1' and '0', respectively, to avoid false charge compensation. In SSVTC, a two-stage amplifier with wide-swing cascode current mirror as biasing circuit is used to provide high-gain and large dynamic-range amplification. The input-referred-offset of the amplifier is critical in determining the accuracy of the TBCB loop, and therefore, auto-zeroing is employed to eliminate it. On the other hand, the offsets due to the comparators' mismatches are divided by the closed-loop gain (40 dB) of the preceding amplifier when referred to the amplifier's input. Therefore, these offsets cause negligible degradation to the accuracy of TBCB.

The following analysis is conducted to quantify the charge balancing precision of the proposed TBCB technique. The attenuation ratio, κ, in this design can be tuned from 1/5 to 1/20 (Fig. 3.2). Accordingly, different ratios and their associated mismatches affect the charge balancing precision. Nevertheless, the forthcoming analysis considers the worst-case scenario (i.e., $\kappa = 1/20$). The charge-balancing operation is first examined for an ideal case of no circuit mismatches or other sources of error (e.g., current leakage at the interface). The attenuated residual voltage ($V_{CB} - V_{REF}$) appearing at the input of SSVTC is equal to $\kappa(V_E - V_{CM})$. After amplification (i.e., $\mathrm{A_V} = -C_S/C_F$), the sampled and held value of V_X at the end of ϕ_2 is denoted as $V_{X,H}$. Note that the relative magnitude of $V_{X,H}$ and $V_{X,TH}$ ($V_{X,TH} = \kappa \mathrm{A_V} V_{TH} = -\gamma\,(K-1)\,T_{CLK} - V_{\mathrm{hys}}$) determines the operation case, as shown in Fig. 3.12(a). Once the residual voltage becomes negligible, as depicted in Case 3 of Fig. 3.12(a), the following condition must be satisfied in order for the charge balancing

operation to be completed:

$$|V_{X,H}| = \left| \kappa \frac{C_S}{C_F} \left[V_E(0) - V_{CM} \right] \right| < V_{\text{hys}} \tag{3.4}$$

where $V_E(0)$ is the initial electrode voltage at the beginning of the compensation period. Under the ideal conditions, Eq. (3.4) indicates that an arbitrarily small V_{hys} yields a small residual voltage V_{DL} on the interface. However, in reality, several sources of inaccuracy prevent us from choosing a very small V_{hys}, which will be further discussed.

During ϕ_1 and ϕ_2, given that the resistive attenuator is used to convert V_E from HV domain to V_{CB} in LV domain prior to the amplification in SSVTC, the inaccuracies associated with this conversion significantly affect the charge balancing accuracy. To be more specific, two major sources of inaccuracies contribute to the degradation of charge balancing precision. The first one is the circuit mismatches in the resistive attenuator. Accounting for this inaccuracy, the modified attenuation ratio becomes $\kappa/[(1 \pm \epsilon)]$, where ϵ is the passive mismatch (typically 0.1%). Another source of error stems from the current passing through the attenuator. This current causes not only a small voltage drop across R_T which results in a V_{DL} different from $V_{CM} - V_E$ (Fig. 3.11(a)), but also slowly discharges V_{DL}. Considering these two non-idealities, according to Fig. 3.11(a), the voltage $V_{DL}(t)$ across the double layer capacitor is calculated as:

$$V_{DL}(t) = \beta V_{CM} \left(1 - e^{-\frac{t}{\beta R_\epsilon C_{DL}}} \right) - \left[V_E(0) - V_{CM} \right] e^{-\frac{t}{\beta R_\epsilon C_{DL}}} \tag{3.5}$$

where the total resistance in series with the electrode-electrolyte interface is $R_\epsilon = \frac{1}{\kappa} R(1 \pm \epsilon) + R_T$ and the coefficient $\beta = 1/\left(R_\epsilon / R_F + 1\right)$. The first and second terms denote the zero state and zero input responses, respectively. Considering that the speed of Faradaic reaction is very slow ($R_F \gg R_\epsilon$) [9], the degradation due to finite R_F is neglected ($\beta = 1$). Therefore,

$V_{DL}(t)$ at the end of ϕ_2 is expressed as:

$$V_{DL}\left(t\right)|_{t=T_{\phi_{1+2}}} = -\left[V_E\left(0\right)\exp\left(-\frac{2T_{CLK}}{R_\epsilon C_{DL}}\right) - V_{CM}\right]. \tag{3.6}$$

From Eq. (3.6), $V_{CB}(t)$ at the end of ϕ_2 is calculated as:

$$V_{CB}\left(t\right)|_{t=T_{\phi_{1+2}}} = \frac{R}{R_\epsilon}\left[V_{CM} - V_{DL}\left(t\right)\right]|_{t=T_{\phi_{1+2}}} = \frac{R}{R_\epsilon}V_E\left(0\right)\exp\left(-\frac{2T_{CLK}}{R_\epsilon C_{DL}}\right). \tag{3.7}$$

Another source of inaccuracy that degrades the charge balancing precision is the input-referred offset of the amplifier ($\mathrm{A_V}$ in Fig. 3.11(a)), which is significantly suppressed by $1/(A+1)$ using auto-zero offset cancellation in phase ϕ_1 (A is the open-loop gain of $\mathrm{A_V}$). Additionally, the mismatches due to the charge injection of switches are resolved by using a fully differential switched-capacitor amplifier, as shown in Fig. 3.11(b). Thus, the voltage held by SSVTC at the end of ϕ_2 is derived from Eq. (3.7):

$$|V_{X,H}| = \left|\frac{C_S}{C_F}\left[V_{REF} - V_{CB}\left(t\right)|_{t=T_{\phi_{1+2}}}\right]\right| = \left|\frac{C_S}{C_F}\left[V_{REF} - \frac{R}{R_\epsilon}V_E\left(0\right)\exp\left(-\frac{2T_{CLK}}{R_\epsilon C_{DL}}\right)\right]\right| \tag{3.8}$$

in which $|\mathrm{A_V}| = C_S/C_F$ (e.g., $|\mathrm{A_V}| = 100$). As shown in Fig. 3.12(a): Case 1, if $|V_{X,H}| > V_{X,TH}$, T_D is a constant and equal to $(K-1)T_{CLK}$. If $V_{X,TH} > |V_{X,H}| > V_{\mathrm{hys}}$, T_D is variable and the SSVTC employs linear voltage-to-time conversion (Case 2). To ensure convergence in Case 3 (similar to Eq. (3.4)), we should have $|V_{X,H}| < V_{\mathrm{hys}}$. Note that the charge balancing accuracy, $V_{E,P}$, is the range of $V_{DL}\left(t\right)|_{t=T_{\phi_{1+2}}}$ (Eq. (3.6)) such that the condition $|V_{X,H}| < V_{\mathrm{hys}}$ is satisfied. Thus, the variation range of $V_{DL}\left(t\right)|_{t=T_{\phi_{1+2}}}$ and the corresponding $V_{E,P}$ are expressed as follows:

$$\left(V_{CM} - \frac{R_\epsilon}{R}V_{REF}\right) - \frac{R_\epsilon}{R}\frac{C_F}{C_S}V_{\mathrm{hys}} < V_{DL}\left(t\right)|_{t=T_{\phi_{1+2}}} < \left(V_{CM} - \frac{R_\epsilon}{R}V_{REF}\right) + \frac{R_\epsilon}{R}\frac{C_F}{C_S}V_{\mathrm{hys}} \tag{3.9}$$

$$V_{E,P} = \left(V_{CM} - \frac{R_\epsilon}{R} V_{REF}\right) \pm \frac{R_\epsilon}{R} \frac{C_F}{C_S} V_{\text{hys}}. \tag{3.10}$$

The second term outside the parenthesis in Eq. (3.10) determines the charge balancing accuracy, while the term inside exemplifies an offset whose magnitude is purposely varied to be smaller than the one outside such that the second term remains dominant. Considering a passive mismatch of $\epsilon \sim 0.1\%$ [76] and assuming $R_T \ll R$, the second term approximately equals $\pm\frac{1}{\kappa|\text{A}_\text{V}|}V_{\text{hys}}$ ($= \pm 2$ mV). As for the term inside the parenthesis, V_{CM} and V_{REF} are 20 V and 1 V, respectively, with V_{REF} being tunable within ± 1 mV so as to compensate for the attenuator mismatch. The required 100 ppm accuracy (guaranteeing the second term in Eq. (3.10) to remain dominant) for V_{REF} is achievable both on-chip and using an off-chip voltage reference. Additionally, since R_T varies from several hundreds of Ω to a few kΩ for different stimulation electrodes [40], the effect of R_T cannot merely be compensated by V_{REF} tuning. In this work, $\frac{1}{\kappa}R$ was designed to vary from 0.5- to 3-MΩ, and was thus much larger than R_T.

3.4.2 High Voltage Output Stage

One HV output stage of the core stimulator is shown in Fig. 3.13(a). For cathodic stimulation, the current from the DAC I_{DAC-C} is mirrored and amplified 5 times to create the cathodic stimulation current I_{OUT-C}. For anodic stimulation, however, another dual-gate PMOS current mirror ($M_{6\text{-}7}$ and $M_{11\text{-}12}$), placed in HV deep n-well, is used to convert the current into the anodic stimulation current I_{OUT-A}. Unlike the H-bridge-based stimulator, in the proposed output stage, I_{OUT-C} and I_{OUT-A} are independent, which means, if multiple stimulators are enabled, all accompanying current sources and sinks will be well-controlled. In this way, the proposed system can perform multipolar, multi-site stimulation. The output

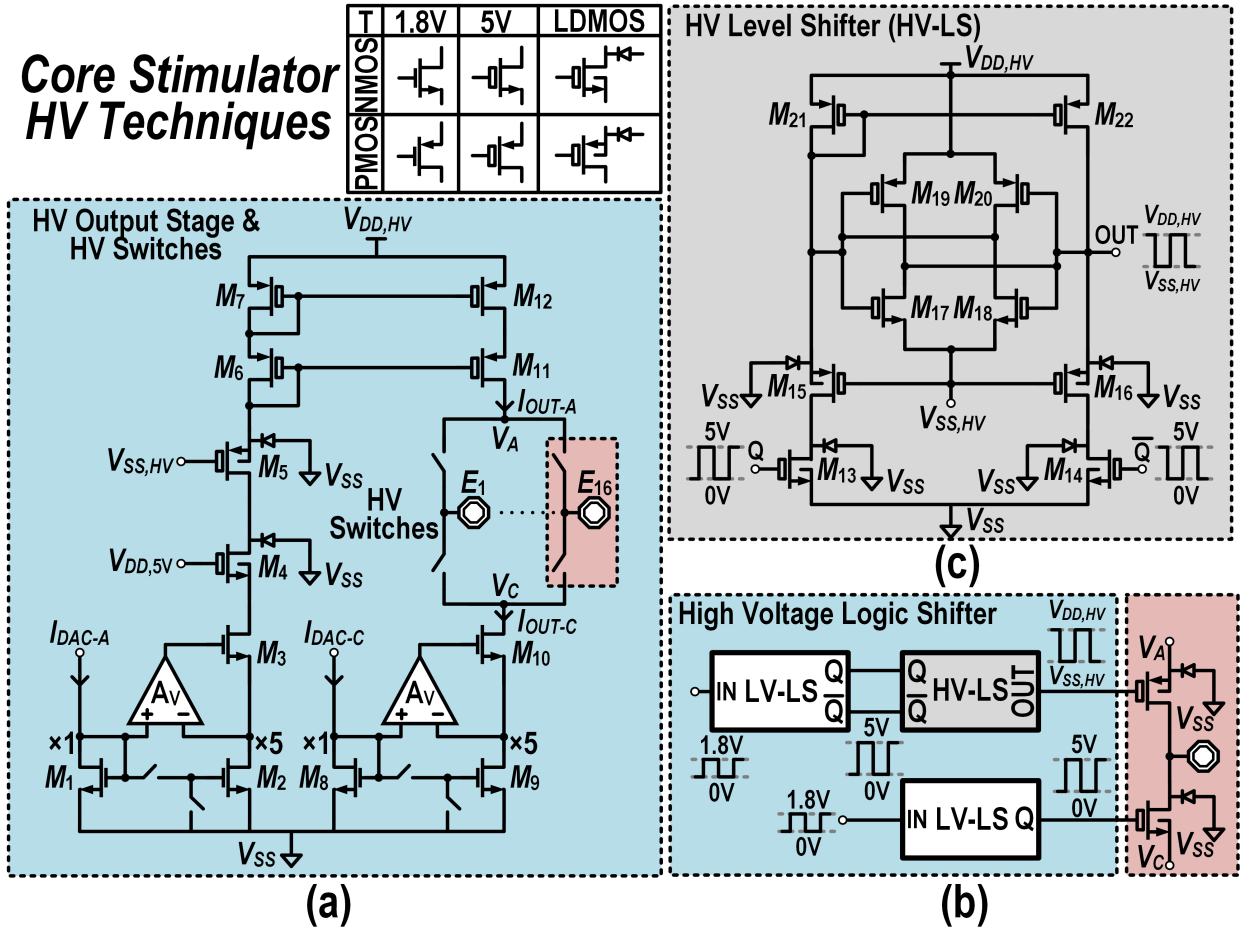


Figure 3.13: (a) Schematic of one HV output stage, which is connected to 16 electrodes through 16 HV switch pairs. (b) Schematic of one HV switch and its logic control circuit. (c) Schematic of the HV level shifter (HV-LS).

of the HV output stage is connected to 16 electrodes through 16 HV switch pairs. Each pair is composed of a p-type and an n-type laterally-diffused metal-oxide semiconductor (LDMOS) switch, as shown in Fig. 3.13(b). Additionally, for the logic control circuit of the p-type LDMOS switch, an HV level shifter (HV-LS) is needed to translate 0- and 5-V to $V_{DD,HV}$ and $V_{SS,HV}$, corresponding to logic '0' and '1', respectively. The proposed HV-LS schematic is shown in Fig. 3.13(c). When Q is logic high (5-V), M_{13} is on and sinks a small DC current (10 μA) from the diode-connected transistor M_{21}, lowering the gate voltages of M_{21} and M_{22}. At the same time, since M_{14} is off ($\bar{\text{Q}}$ is logic low), M_{22} is forced into the triode region and the output reaches $V_{DD,HV}$. On the other hand, if Q is logic low, M_{13} turns off, bringing the drain voltage of M_{21} up to $V_{DD,HV}$. At the same time, M_{14} is in triode region,

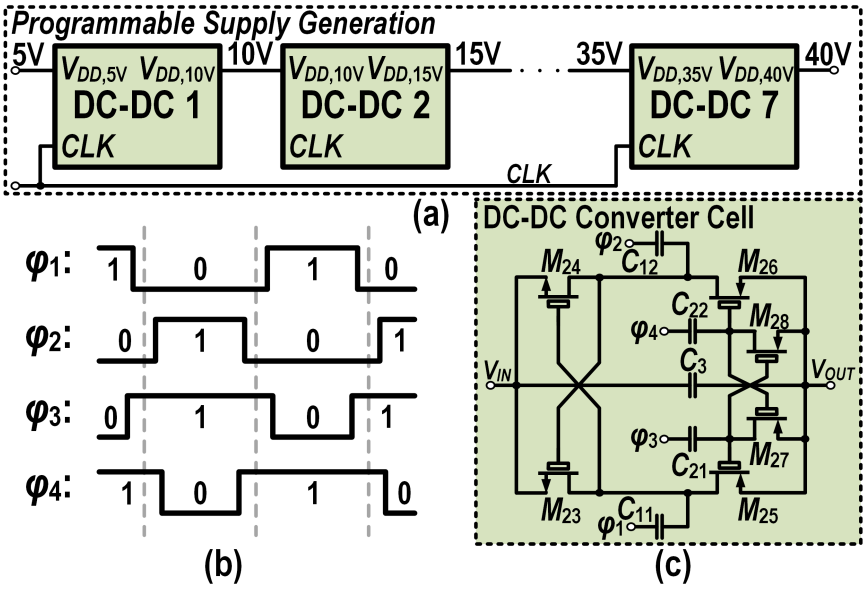


Figure 3.14: (a) Programmable supply generation using a seven-stage charge-pump-based DC-DC converter. (b) Timing diagrams for all four phases of the clock. (c) Schematic of one DC-DC converter cell.

lowering the output voltage to $V_{SS,HV}$. $M_{15\text{-}16}$ pair limits the output swing and protects 5-V dual-gate transistors, and $M_{17\text{-}20}$ form a pair of back-to-back inverters, boosting the speed of the HV-LS.

3.4.3 Programmable Supply Generation

To generate all the HV supplies for the HV output stages and switch fabric, a seven-stage charge-pump-based DC-DC converter [77] is designed, as shown in Fig. 3.14(a). Each stage employs a four-phase voltage doubler [78] in HV deep n-well (Fig. 3.14(c)), which boosts the supply voltage by 5-V. In steady state, V_{OUT} is charged to 5-V above V_{IN}. Depending on the logic state of CLK, either M_{23} and M_{26} or M_{24} and M_{25} turn on, and a voltage boost of 5-V is thus maintained between V_{IN} and V_{OUT} [79]. In addition, two-phase non-overlapping clock signals $\varphi_{1\text{-}2}$ (Fig. 3.14(b)) are connected to $C_{11\text{-}12}$, while two-phase overlapping clock signals $\varphi_{3\text{-}4}$ (Fig. 3.14(b)) are connected to $C_{21\text{-}22}$ to eliminate any possible charge reversal from V_{OUT} to V_{IN} [78].

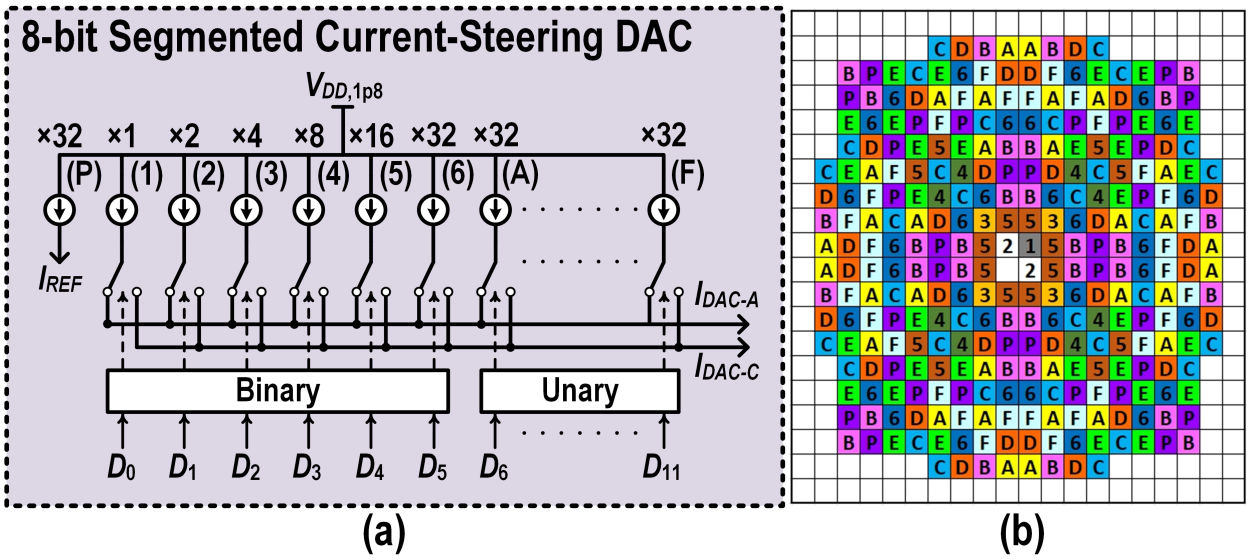


Figure 3.15: (a) Schematic of one 8-bit segmented current-steering DAC. (b) Layout of the DAC.

3.4.4 8-bit Segmented Current-Steering DAC

The 8-bit segmented current-steering DAC is shown in Fig. 3.15. A combination of unary and binary weighted architecture is adopted to improve DNL. Specifically, as shown in Fig. 3.15(a), bits 1 to 6 are binary weighted and the most two significant bits 7 and 8 (denoted as A to F), are unary weighted. The current-steering technique is used to increase the DAC speed such that the system can perform arbitrary current-waveform stimulation. Additionally, since for the majority of time, the stimulator and the corresponding current DAC are off, a relatively large reference current I_{REF} (weighted ×32) is used to reduce the start-up time of the current DAC. The DAC layout (Fig. 3.15(b)) employs common centroid technique to mitigate first-order process variation and, for the most two significant bits, maintain their average distance to the center so as to mitigate the nonideality induced by mismatches.

3.5 Recording Circuit Implementation

3.5.1 Dual-Mode Front-End and Analog Interface Circuits

To allow low-noise amplification of the neural signals, a chopper-stabilized amplifier based on folded-cascode structure is employed in the dual-mode front-end [66], as depicted in Fig. 3.16. Two auxiliary loops are placed between the output and folding nodes in order to minimize the output voltage offset and undesirable ripples. A DC-servo loop [80] facilitates the reduction of the output offset, and provides additional attenuation of low-frequency signals. Moreover, a ripple-reduction loop [80] ameliorates the chopping ripple caused by up-converted voltage offset of the input transistor pair. While chopping technique helps mitigate the flicker noise contribution of transistors, it further alleviates the degrading effect of transistor mismatches on common-mode rejection ratio (CMRR). To attain a higher CMRR, the input capacitors were sized appropriately to minimize their mismatches, and the common-mode feedback (CMFB) circuitry was enhanced by introducing the feedback to the tail current, and thus, achieving a higher loop gain.

Given that the amplified raw signals entail digitization with higher bit-resolution and sampling rate compared to the extracted neural features [66], it follows that channel serialization and post-multiplexing amplification in each acquisition mode adhere to a drastically different settling speed requirement. In particular, FB-PGA must undergo less settling time to accommodate proper sampling of the signal by FB-ADC, which implies that a higher unity gain-bandwidth product is needed at the cost of increasing power dissipation. On the other hand, processing of neural features is carried out at much lower bandwidth, and therefore, BB-PGA consumes significantly less power in BB mode.

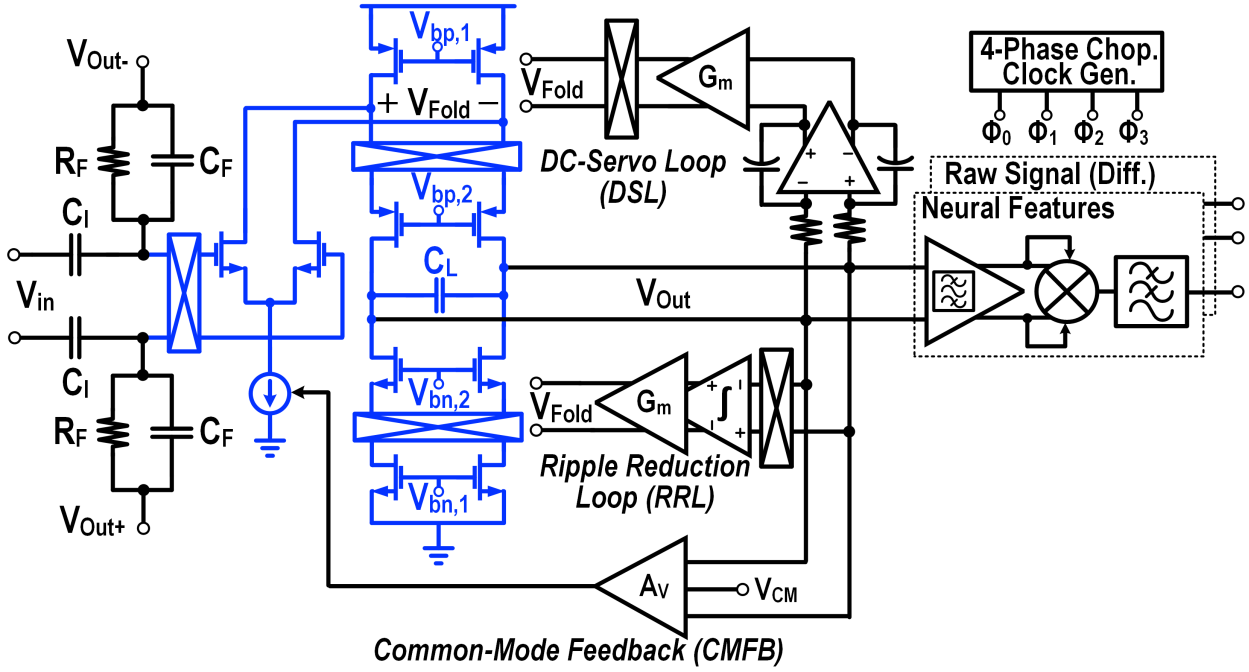


Figure 3.16: Schematic of dual-mode front-end module, incorporating DC-servo loop, ripple reduction loop and common-mode feedback.

3.5.2 Successive Approximation Register ADCs

To facilitate the ULP operation and achieve the desired accuracy, successive approximation register (SAR)-ADC is adopted in the proposed neural data acquisition system. While both FB- and BB- ADCs follow the same operation principle, the latter has relaxed requirements which translate into fewer circuit design challenges. The differential N-bit (i.e., N=6 for BB, N=12 for FB) SAR-ADC, as depicted in Fig. 3.17, employs a V_{CM}-based binary-weighted capacitive DAC, an acquisition-mode-specific comparator and a compact modular non-redundant SAR logic and control with minimum circuit overhead. The unit capacitors (C_0) used in this design for 12- and 6-bit SAR-ADCs are 25 fF and 100 fF, respectively. The V_{CM}-based switching technique provides significant improvement in switching energy efficiency compared to the conventional charge redistribution scheme [81]. Moreover, the comparator in FB mode utilizes a multi-stage pre-amplifier chain with output offset cancellation (OOS) [82] to reduce the input-referred voltage offset and the kickback noise from the regenerative latch. Meanwhile, a conventional dynamic comparator with current source is

used in BB mode because of the lower bit-resolution and reduced power dissipation. Additionally, the DAC and comparator are connected using twisted differential signaling [83] which helps mitigate common-mode noise (Fig. 3.17), an important attribute for FB-ADC.

Shown in Fig. 3.17, the SAR logic and control needed for V_{CM}-based switching are implemented with minimum combinational and sequential circuits. In specific, digital control circuitry (shaded in light blue) uses one D-flipflop, one inverter and two AND gates for each bit. The details of the circuit operation can be summarized as follows: During sample and hold phase, every D-flipflop in the digital control of SAR is reset by $CK_{S/H}$. This activates all S_3 switches in the capacitive DAC, causing every capacitor's bottom plate to be tied to the common-mode voltage (V_{CM}), and makes ready for sampling. To accomplish the binary search algorithm, SAR logic is first initialized and a leftward-propagating pulse is generated in the shift register to mark each sequential step of bit-cycling. During the conversion phase, the comparator's output is captured synchronously with CK_{SAR} and following the relevant bit position, its value is stored in a MUXed D-flipflop (shaded in light brown). In addition, each capture-and-store interval represents a comparison window in which the direction of the binary search is decided, beginning with the most significant bit. The SAR control circuitry detects the onset of transitions in the bit-cycling sequence and generates the control signals for the capacitive DAC based on the stored bit value in a given comparison window. As a result, the corresponding pair of DAC switches (S_1 or S_2) is activated immediately after S_3 is disabled for each bit, performing the necessary charge addition/subtraction. This process continues until all the bits have been resolved for a sampled voltage value, followed by a new sample and hold phase.

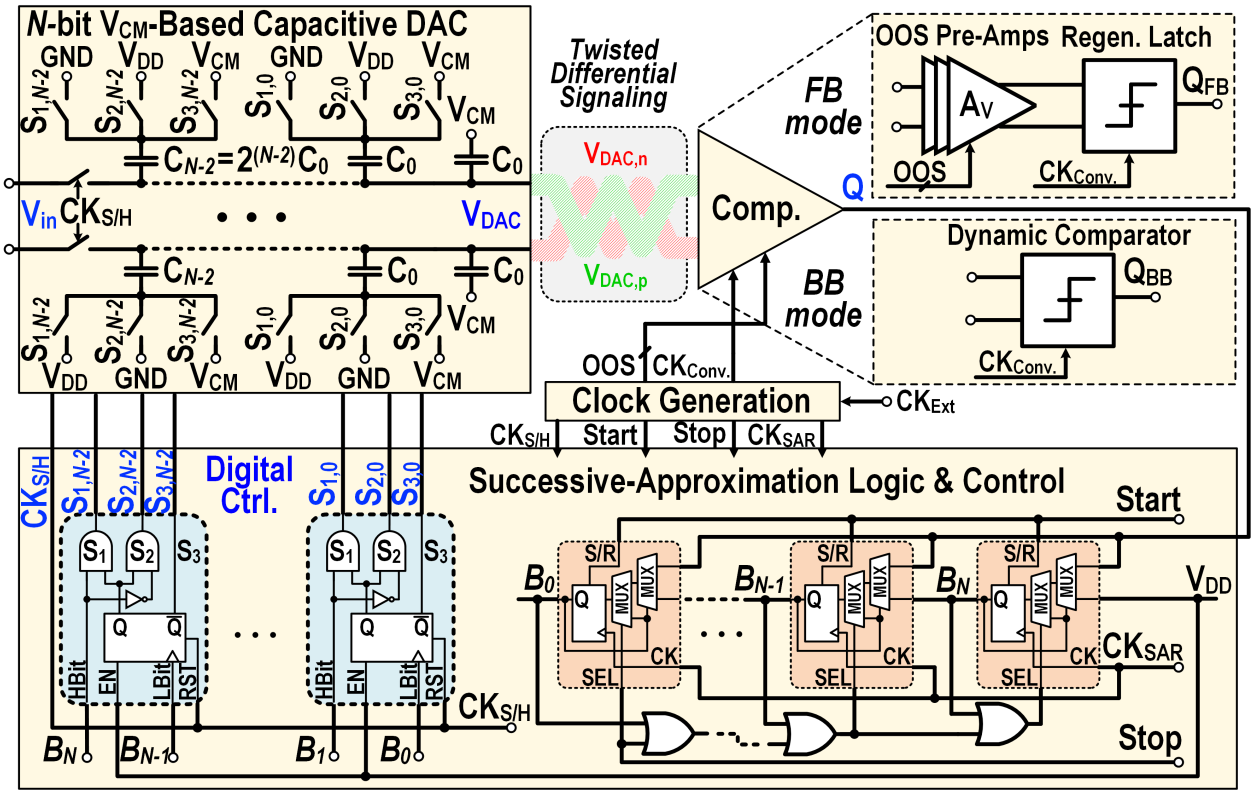


Figure 3.17: Schematic of SAR-ADC comprised of V_{CM}-based capacitive DAC, comparator and digital logic & control circuitry.

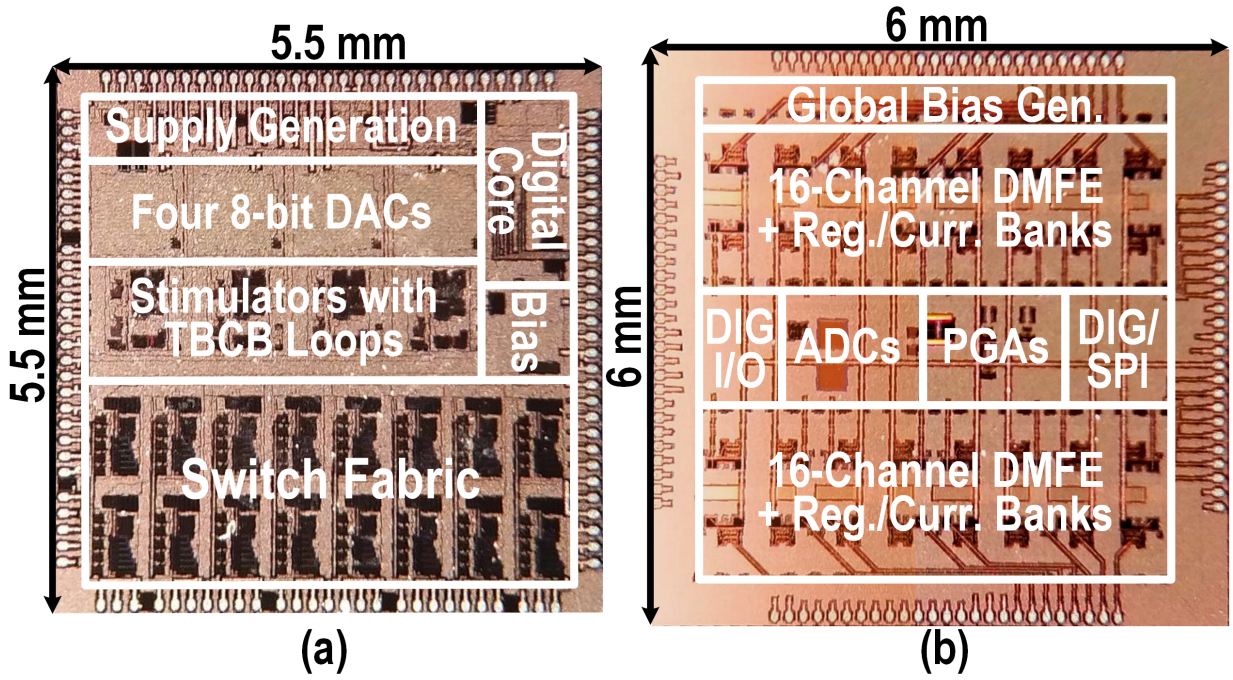


Figure 3.18: Chip micrograph of the stimulation system (a) and the recording system (b).

3.6 Experimental Results

Both the stimulation and recording systems were designed and fabricated in an HV 180-nm CMOS technology occupying 5.5×5.5 mm^2 and 6×6 mm^2 of die areas, respectively (Fig. 3.18). The functionality of the stimulation system was verified first by electrical measurement and then tested by using *in vitro* phantom measurements. The performance of the recording system was verified by using pre-recorded bio-signals. In addition, the bi-directional measurement was conducted *in vitro* with phantom brain tissue.

The phantom brain tissue was created to mimic the cerebral cortex [4]. Specifically, table salt was added to deionized water, and the mixture was stirred evenly and heated until boiling. Then, agar powder was added into the boiling mixture gradually to create a gel compound. The compound was poured into a Petri dish to form the phantom brain tissue as shown in Fig. 3.20(a) and the Petri dish was placed in a refrigerator to cool down. The conductivity of phantom brain tissue was controlled by salt concentration [39] and was approximately equal to the conductivity of the human cerebral cortex [84]. Additionally, a thin layer of phosphate-buffered saline (PBS) was added on top of the phantom brain tissue to mimic the cerebrospinal fluid (CSF) [4]. Placed inside PBS, a standard subdural ECoG grid with platinum electrodes (4 mm diameter, 2.3 mm exposed, 10 mm spacing) was used for both recording and stimulation (Fig. 3.20(a)). The values of C_{DL} and R_F in the electrical model (Fig. 3.1(a)) were estimated by first measuring the impedance of the electrode-electrolyte interface across frequency and then applying curve-fitting to the impedance frequency response based on the electrical model. C_{DL} and R_F were approximately equal to 880 nF and 2 MΩ, respectively.

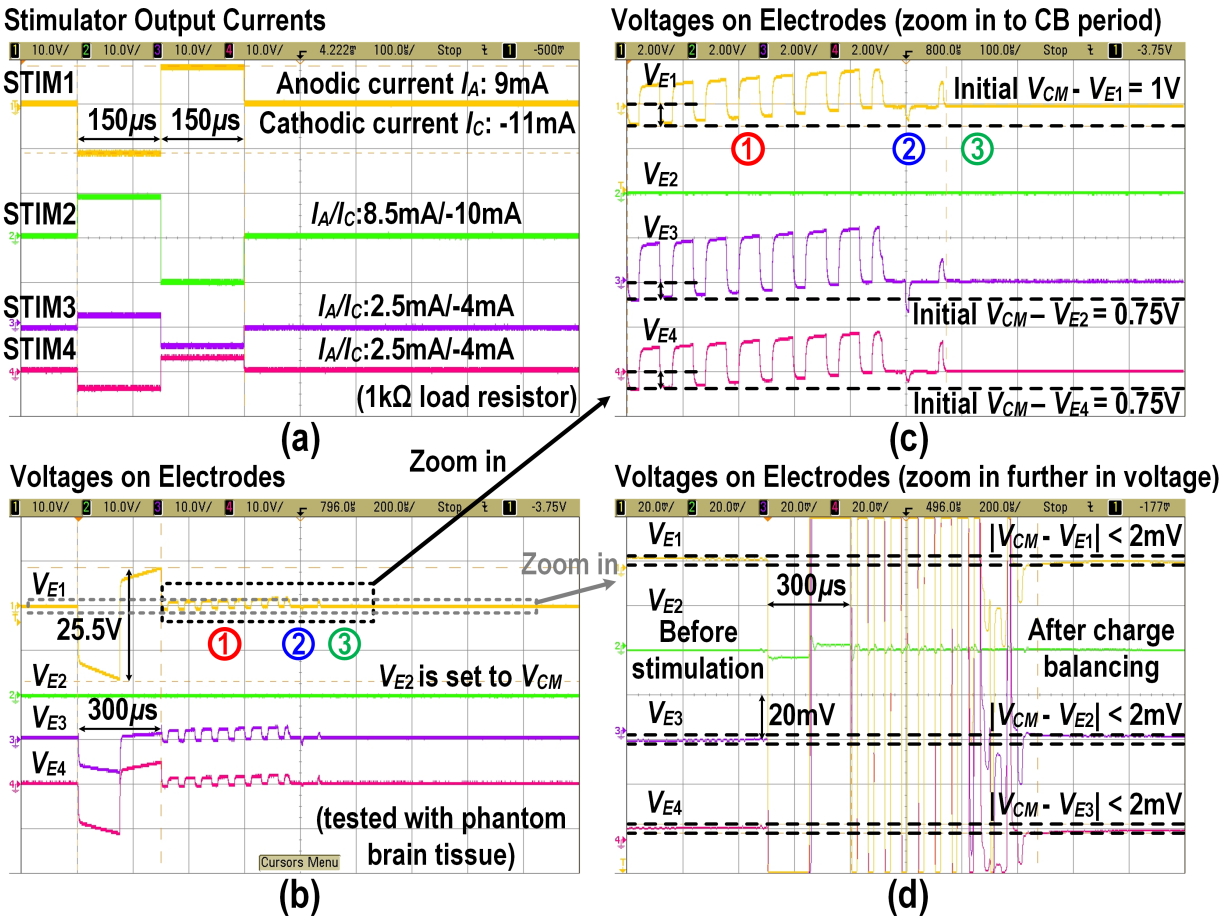


Figure 3.19: (a) Stimulator output currents. (b) Voltages on electrodes. (c) Voltages on electrodes (zoom in to CB period). (d) Voltages on electrodes (zoom in further in voltage domain to demonstrate charge balancing precision).

3.6.1 Stimulation System Measurement Results

The measurement setup of the stimulation system is shown in Fig. 3.20(a). A microcontroller (MCU) was used to control the stimulation system and the outputs of the stimulation system were connected to either a test board or phantom brain tissue through an ECoG grid (Fig. 3.9(a)). The test-board electrical test and the *in vitro* phantom measurement were used to characterize output currents and evaluate the performance of TBCB, respectively. For the test board measurement, the output of each stimulation channel was loaded with a 1 kΩ resistor and the output current was characterized by measuring the voltage across this resistor.

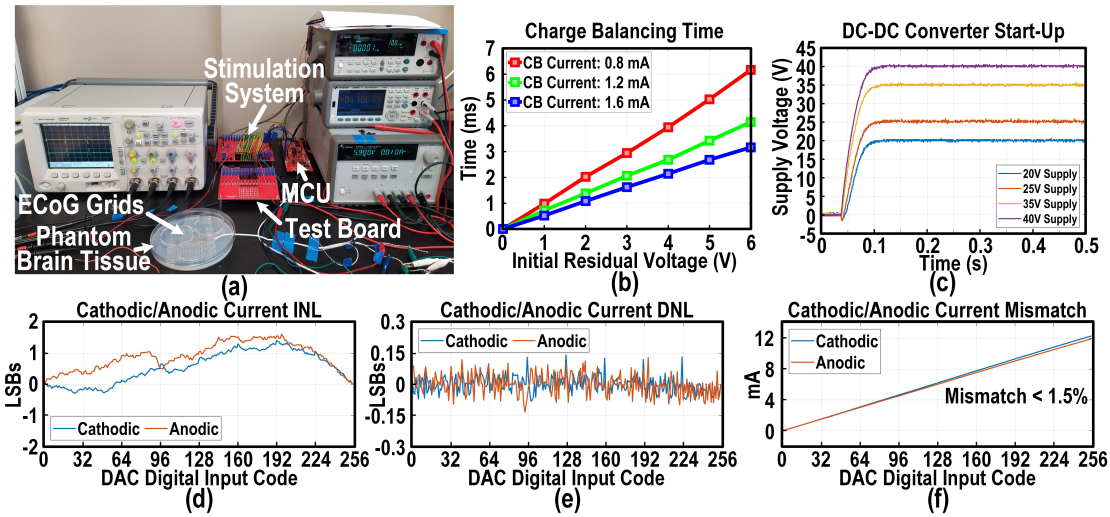


Figure 3.20: (a) Stimulation system *in vitro* measurement setup. (b) Total charge balancing time for various compensation currents and initial residual voltages. (c) DC-DC converter start-up. (d) INL of the stimulator output current. (e) DNL of the stimulator output current. (f) Cathodic and anodic currents mismatch.

The measured characteristics of the stimulator output current is shown in Fig. 3.19(a) and Figs. 3.20(d)-(f). The measured static behavior shows that the DAC INL, DNL, and cathodic/anodic current mismatch are less than 1.4 LSB, 0.14 LSB, and 1.5%, respectively. To demonstrate the performance of multipolar, multi-site stimulation, all four stimulators were turned on concurrently, as shown in Fig. 3.19(a). For demonstration purposes, each stimulator independently delivered an unbalanced biphasic square pulse with 150 μs pulse-width for each phase of the current injection. The measurement results for multipolar stimulation incorporating TBCB technique are shown in Figs. 3.19(b)-(d). As discussed in Section 3.3.2, stimulators 1-2 (STIM1-STIM2) and 3-4 (STIM3-STIM4) were connected to electrode pair 24-16 and 31-7 to perform primary stimulation and cancellation, respectively (Fig. 3.9(a)). Given the fact that grid placement on the brain is governed by functional mapping to establish motor and sensory areas of interest, this typically allows physical separation between the stimulation and recording sites. In this demonstration, electrode pair 24-16 was chosen as the primary stimulation dipole to allow maximum distance between the stimulation and recording electrodes using a single grid. Electrode pair 31-7 was determined by the optimization algorithm [4] as the optimal location to achieve the maximum artifact cancel-

lation. In real tissue, the monopole-model-based optimization algorithm [4] may not yield a globally optimum cancellation due to the complicated boundary conditions of the brain and unsatisfiable condition of infinitely far reference. However, the optimization algorithm is still effective and can provide better accuracy if an improved mathematical model is used to describe the electrical field distribution in the brain. Such study is beyond the scope of this work. In addition, one of the primary stimulation electrodes (i.e., electrode 16 corresponding to V_{E2} in Fig. 3.19(b)) is connected to V_{CM} as the reference electrode to collect the return stimulation current. The voltage on each electrode was measured, as shown in Fig. 3.19(b). Note that the stimulation current flowing through the reference electrode (corresponding to V_{E2} in Fig. 3.19(b)) will charge and discharge the double-layer capacitor of the reference electrode, as well (Fig. 3.1). Therefore, the measured voltages V_{E1}, V_{E3} and V_{E4}, as shown in Fig. 3.19(b), are the summation of the residual voltages of the reference electrode and the corresponding stimulating electrodes. To better illustrate the transient waveforms during the TBCB operation, Fig. 3.19(c) shows a zoomed-in version of Fig. 3.19(b). In the absence of charge balancing mechanism, the initial residual voltage ($V_{CM} - V_E$) on electrode was 1 V for STIM1 and 0.75 V for STIM3 and STIM4. With TBCB technique being activated, the TBCB loop switches from Case 1 to Case 2, and finally to Case 3, and halts all subsequent charge balancing cycles (Fig. 3.19(c)). The charge balancing precision is demonstrated in Fig. 3.19(d), where the residual voltages on all electrodes are brought down to within ± 2 mV of the common-mode voltage.

Fig. 3.20(b) demonstrates the charge balancing time for various compensation currents and initial residual voltages under the condition of a fixed compensation period. As expected, the charge balancing time increases linearly with the initial residual voltage and decreases with an increase in the compensation current. As described in Section 3.3.1, in practice, clinicians should determine the maximum compensation current in conjunction with the duration of ϕ_3 such that the charge delivered in each period T_{CC} causes no false sensation. The start-up waveforms of four selected output supply voltages of the DC-DC converter are depicted in

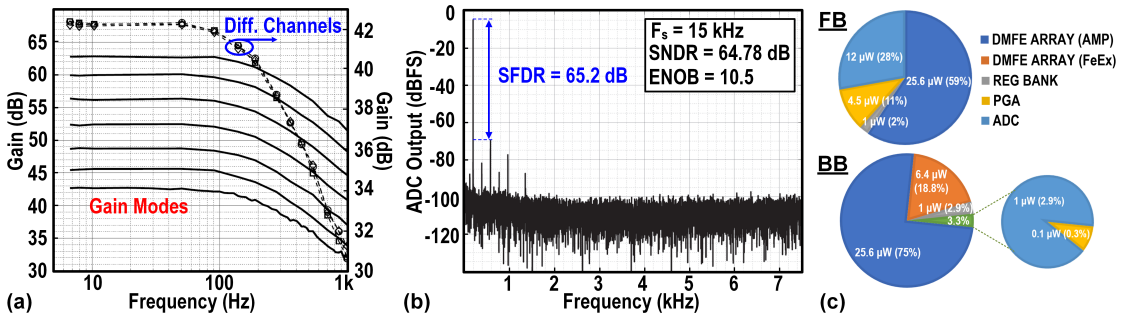


Figure 3.21: (a) MSN-DAQ measured frequency response, (b) ADC measured output power spectrum and (c) power dissipation breakdown.

Fig. 3.20(c). It takes less than 0.1 s for supply voltages to reach their nominal values.

3.6.2 Recording System Measurement Results

Operating at 1-V supply voltage, the MSN-DAQ chip achieves a minimum closed-loop gain of 42.5-dB, an input-referred noise of 1.03 μV_{rms} across 2-200 Hz with an equivalent noise and power efficiency factors (NEF/PEF) of 2.37/5.62, and 88-dB average CMRR for 10 mVpp interference within 50-160 Hz range. Furthermore, the measured frequency response of MSN-DAQ in different gain modes of one channel as well as across 3 neighboring channels is depicted in Fig. 3.21(a). The measured FFT from the 12-bit SAR-ADC output for a 193.17-Hz tone (i.e., upper edge of the frequency band) at maximum sampling rate of 15 kHz, as shown in Fig. 3.21(b), exhibits a signal to noise-and-distortion ratio (SNDR) of 64.78 dB, a spurious-free dynamic range (SFDR) of 65.2 dB, and an effective number of bits (ENOB) equal to 10.5. The power dissipation of each operating mode is further quantified in Fig. 3.21(c), exhibiting significantly reduced power consumption for PGA and ADC in BB-mode as compared to FB-mode operation.

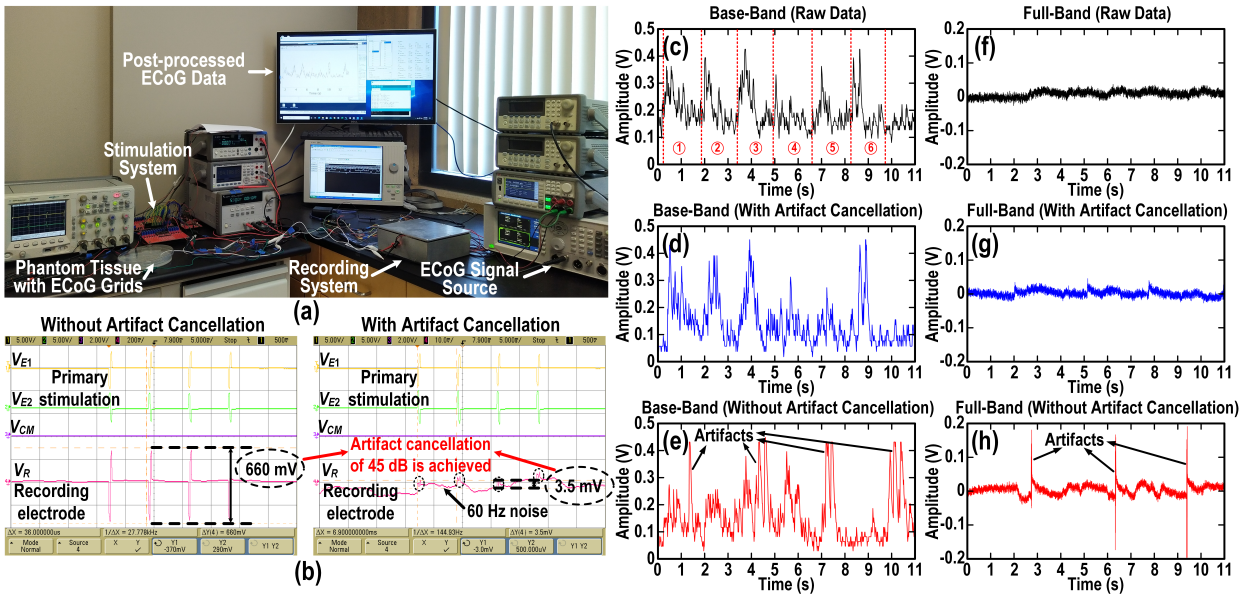


Figure 3.22: (a) Bi-directional *in vitro* measurement setup. (b) Artifact V_R shows up on the recording electrode without/with stimulation side contour shaping artifact cancellation. (c) Post-processed base-band ECoG data without stimulation. (d) Base-band data with both stimulation and artifact cancellation. (e) Base-band data with stimulation but without artifact cancellation. (f) Full-band data without stimulation. (g) Full-band data with both stimulation and artifact cancellation. (h) Full-band data with stimulation but without artifact cancellation.

3.6.3 In-Vitro Phantom Bi-Directional Measurement Results

The measurement setup and results for bi-directional *in vitro* phantom brain tissue experiment are shown in Fig. 3.22. Referring to Fig. 3.22(a), pre-recorded ECoG data was re-produced by a high-resolution signal generator and delivered to electrode 26 (Fig. 3.9(a)) to mimic neural signals. Concurrently, four channels of the stimulation system turned on. The primary stimulation current (10 mA) was delivered through electrode pair 24-16 and the cancellation (1.25 mA) was delivered through 7-31 (Fig. 3.9(a)). This setup was employed based on the primary dipole stimulation and the optimal cancellation described in Section 3.3.2 and Section 3.6.1. Electrode 18 was chosen as the recording channel and was connected to both the recording system and one channel of the oscilloscope (denoted as V_R in Fig. 3.22(b)).

Fig. 3.22(b) demonstrates how the artifact, V_R, shows up on recording electrode with/without artifact cancellation. After applying cancellation, the artifact dropped from 660 mV to 3.5 mV with a suppression ratio of 45 dB. These measured artifacts contain both common and differential components, but only the differential component (which is a small portion) is sensed by the recording system. Therefore, the proposed SSCS technique is capable of suppressing stimulation artifacts effectively before reaching the recording system and thus, preventing the AFEs from saturation. Figs. 3.22(c)-(h) shows the post-processed data from the recording system. In particular, the extracted high-γ features from BB mode are shown in Fig. 3.22(c), exhibiting power modulations during six consecutive elbow flexion and extension periods as annotated. For base-band operation, Figs. 3.22(c)-(d) demonstrate the envelopes of the pre-recorded ECoG signals under no stimulation and stimulation with cancellation conditions, respectively. As expected, these two envelopes closely follow one another. However, in the absence of cancellation (Fig. 3.22(e)), the power envelope is severely contaminated by the stimulation artifacts. Similar results for full-band operations are shown in Figs. 3.22(f)-(g).

Tables 3.1 and 3.2 show performance summary and comparison between the proposed stimulation and recording systems and the prior art. The stimulation system incorporating TBCB technique achieves 12.75-mA maximum current, 40-V voltage compliance and 2-mV charge balancing precision, considered to be the lowest value on the record to date. Furthermore, the recording system achieves excellent performance that includes 88 dB CMRR, 10.5 ENOB and NEF/PEF of 2.37/5.62. The power consumption per channel is 1.07μW and 1.32μW for BB- and FB-mode operation, respectively.

Table 3.1: Stimulation System Performance Comparison

Reference	TBioCAS 2016 [54]	BioCAS 2018 [56]	JSSC 2018 [47]	JSSC 2020 [60]	JSSC 2020 [67]	ISSCC 2020 [48]	JSSC 2021 [85]	ISSCC 2021 [86]	This Work
Number of Channels / Stimulators	1/1	6/6	1/1	4/4	32/32	8/8	16/16	1/1	16/4
I_{MAX} (mA)	3	10	5.12	2	1.5	0.775	1.35	0.2	12.75
Resolution (bits)	4	9	9	8	8	5	8	-	8
Charge Balancing Method	DCM+ Passive	OR	IPCC+OR	No	Passive	CPI	No	No	TBCB
Charge Balancing Precision	±13.2mV[a] 6.6nA@3mA	±20mV	±20mV	-	-	±50mV	-	-	±2mV 1nA@10mA[a]
Voltage Compliance (V)	12	49	22	22	3.3	4	3.3	1	40
Multipolar Stimulation	No	No	No	No	No	No	No	No	Yes

[a]Calculated based on 2MΩ R_F.

Table 3.2: Recording System Performance Comparison

Reference	TBioCAS 2017 [87]	JSSC 2017 [72]	JSSC 2018 [71]	JSSC 2019 [70]	TBioCAS 2020 [88]	JSSC 2021 [85]	ISSCC 2021 [86]	ISSCC 2021 [89]	This Work
Number of Channels	16	64	16	4	64	16	64	8-24	32
Supply Voltage (V)	1.8	1.2/2.5	0.8	1.2	0.5/2.5	0.6/1.2/3.3	0.5-1.6	1.8	1
Power/Channel (μW)	15	0.63	0.8	3.9	2.98	0.99	0.14	14.94/13.94	1.07(BB)/ 1.32(FB)
Artifact Cancellation	Mono/Bipolar Pole-Shifting	Passive	Fast Recovery	Artifact Tolerant	Template Subtraction	Artifact Tolerant	Artifact Tolerant	No	SSCS
Bandwidth (Hz)	0.3-7k	0.01-500	500	200	1-1k	1-500	10k	0.5-1k	2-200
CMRR (dB)	81	88	81	>75	76	>78	-	-	88
NEF/PEF	4.77/41.1	2.86[b]/-	1.81/2.6	4.9/28.81	2.21/-	3.5/15.2	4.7/13.2	-/-	2.37/5.62
ENOB (bit)	7.9[a]	11.7[a]	10.7	13.2	15.7	9.7	8	11[e]	10.5
IRN (μV_{rms})	4.57	1.13	0.99	1.3	1.66	2.6	-	2.72/2.31	1.03
Input Impedance (MΩ)	-	0.99-1.02	>26	160	92	>1000	40[c]/100[d]	-	>44

[a]Calculated. [b]Amplifier+ADC. [c]For 25 kHz chopping frequency. [d]For 10 kHz chopping frequency. [e]ADC resolution.

3.7 Conclusion

A companion chipset incorporating both stimulation and recording systems for fully-implantable BD-BCI applications was presented. The detailed operation of the high voltage compliance multipolar stimulation system together with the conceptual and analytical formulation of the proposed TBCB technique was provided. The neural stimulator achieves a record-breaking charge balancing precision of 2-mV and a maximum stimulation current capability of 12.75-mA. In addition, for the recording system, a fully-integrated 1μW/channel dual-mode neural data acquisition was demonstrated. Enabled by the multipolar operation, the SSCS artifact cancellation technique was adopted to significantly suppress the stimulation artifacts. Measurement results for the fabricated prototype in an HV 180-nm CMOS process further validated the performance of the proposed chipset.

Chapter 4

A Novel Multipolar Neural Stimulation System with Dual Mode Time-Based Charge Balancing

4.1 Introduction

Brain-computer interface (BCI) is an emerging technology that provides an alternative communication pathway between the brain and external devices to bypass the human peripheral nervous system and muscles [90, 91]. It can be used to detect neurological disorders like epilepsy and narcolepsy [5, 6] and treat neurological disabilities like spinal cord injury [4]. Subdurally recorded electrocorticogram (ECoG) is an appropriate modality for BCI applications because ECoG electrodes are not as invasive as intra-cortical microelectrodes but the spatial and temporal resolutions of ECoG arrays are much better than those of electroencephalogram (EEG) grids [4]. Recently, ECoG-based BCIs have been proven capable of both restoring motor functions by recording neural signals directly from the sensorimotor cortex

of humans [16] and eliciting artificial sensation by ECoG electrical stimulation [18]. It is required for a bi-directional BCI to perform concurrent neural signal recording and brain electrical stimulation [4]. However, simultaneous recording and stimulation faces a significant challenge of stimulation artifact [10], since the magnitude of the voltage introduced by electrical stimulation in the sensorimotor cortex is orders of magnitude larger than the neural signals [13]. Recently, several studies [11,12] have shown that localizing activation by shaping the electric field within the brain can significantly reduce the stimulation artifact on the recording side but this method requires adding auxiliary stimulation, thus leading to a significant increase in power consumption. One promising solution is to have a high dynamic range recording to capture both the stimulation artifact and the underlying neural signals and then apply adaptive-filter-based artifact cancellation technique to separate neural signals from the artifact in back-end processing [60, 92]. This technique is feasible because the recorded neural signals can be considered uncorrelated with the pre-defined stimulation pattern [23]. The other challenge in ECoG-based BCIs is the stimulator design itself. Subdural cortical stimulation using ECoG grids requires up to 10 mA of current to elicit artificial sensation while intra-cortical stimulation such as deep brain stimulation (DBS) needs only a few hundreds of microamperes [18]. To deliver this large current to the cortex with a typical tissue impedance of a few kiloohms [40], a large voltage compliance (a few tens of volts) is required at the output of the stimulator. Thus, stimulators require high-voltage (HV) output current drivers and on-chip HV supply generation circuits. Additionally, for a typical biphasic current stimulation, the mismatch between the positive and negative current pulses leads to voltage build-up on the stimulation electrode due to the capacitive nature of the electrode-electrolyte interface [8]. This residual voltage leads to a long-term unidirectional charge transfer across the interface causing electrode corrosion and tissue damage [9]. Thus, a charge balancing technique is needed to continuously monitor the residual voltage and compensate for the remaining charges on the stimulation electrode. Several charge balancing techniques have been introduced by prior works including passive

charge balancing [93], charge-pack injection (CPI) [48, 52], dynamic current mirrors [54, 55], offset regulation (OR) [47,93], inter-pulse charge control (IPCC) [47], and time-based charge balancing (TCB) [94]. Among all the charge balancing techniques, active charge balancing by sensing and feeding back the voltage across the stimulation and reference electrodes (electrode voltages) and then injecting well-controlled compensation charges back to the electrode (i.e., CPI, OR, and TCB) is prominent due to two major advantages: 1) well-controlled charge balancing current to avoid secondary sensation; 2) achieving relatively good accuracy because of the feedback operation. To compensate for the residual charge on the stimulation electrode, all these active charge balancing techniques must accurately detect the polarity and magnitude the residual voltage across the electrode-electrolyte interface and use the voltage in the feedback to determine the direction and amplitude of the charge compensation. However, the residual voltage across the interface is not accessible because the stimulator circuits only have connections to one side of the interface. Thus, all existing active charge balancing techniques detect the electrode voltage and use it as a substitute for the residual voltage because they assume that the polarities of these two voltages are the same and their magnitudes are proportional. However, this assumption holds valid only for monopolar stimulation or bipolar stimulation with the counter electrode as the reference electrode [9]. For multipolar stimulation, since several stimulators perform biphasic stimulation concurrently, the mismatches between positive and negative current pulses of all stimulators will contribute to the residual charge of the reference electrode. In addition, after all the stimulation currents are off, each electrode voltage is the summation of the residual voltage on that electrode and the reference electrode. Thus, the electrode voltage depends not only on the residual voltage of this electrode but also on the residual voltages of all the other stimulation electrodes. This detrimental effect is defined as inter-channel interference (ICI) which could potentially increase the charge balancing time and decrease the charge balancing accuracy. Therefore, an inter-channel interference attenuator (ICIA) is needed in the feedback of the active charge balancing such that the resulting representa-

tion of the electrode voltage is proportional to the residual voltage on the electrode. It is proved in the following sections that the ICIA process requires arithmetic operation among electrode voltages of all the stimulation electrodes. Thus, the electrode voltages should be captured first and then digitized before the operation of ICIA. Among all the active charge balancing techniques, the TCB technique achieves the best charge balancing accuracy [8]. It converts the electrode voltage to an enable signal with its duration proportional to the electrode voltage, and then the enable signal is used to turn on either the anodic or cathodic compensation current. The current is injected back into the stimulation electrode in the inter-pulse time interval between two biphasic stimulations to perform charge balancing. Thus, the TCB technique inevitably introduces significant stimulation artifacts beyond the duration of the biphasic stimulation. Furthermore, these compensation current pulses due to TCB are uncorrelated to the stimulation and thus the adaptive-filter-based back-end artifact cancellation cannot be applied. Therefore, TCB is not suitable for performing active charge balancing in bi-directional BCI applications. A novel charge balancing technique is needed to retain the accuracy of TCB but instead of injecting compensation current in the inter-pulse time interval, compensation should be added to the current pulses of the following biphasic stimulation. In this way, the pulse width of the compensation current is fixed since the pulse width of the stimulation current is predefined. In the new approach, the amplitude of the compensation current must be proportional to the duration of the enable signal generated in the original TCB idea to create compensation charges proportional to the electrode voltage. This operation requires a mixed-signal system with a time-to-digital converter (TDC) to translate the pulse-width information into digital signals and a digital-to-analog converter (DAC) to convert the digital stream to compensate for current amplitude. This active charge balancing technique, defined as the artifactless time-based charge balancing (AL-TCB), is combined with the original TCB technique [8] (redefined as the interpulse-bounded TCB, or IB-TCB) to form a novel dual-mode TCB (DTCB) technique. When the residual voltage is large, IB-TCB is activated to remove the residual voltage before the next stimulation to

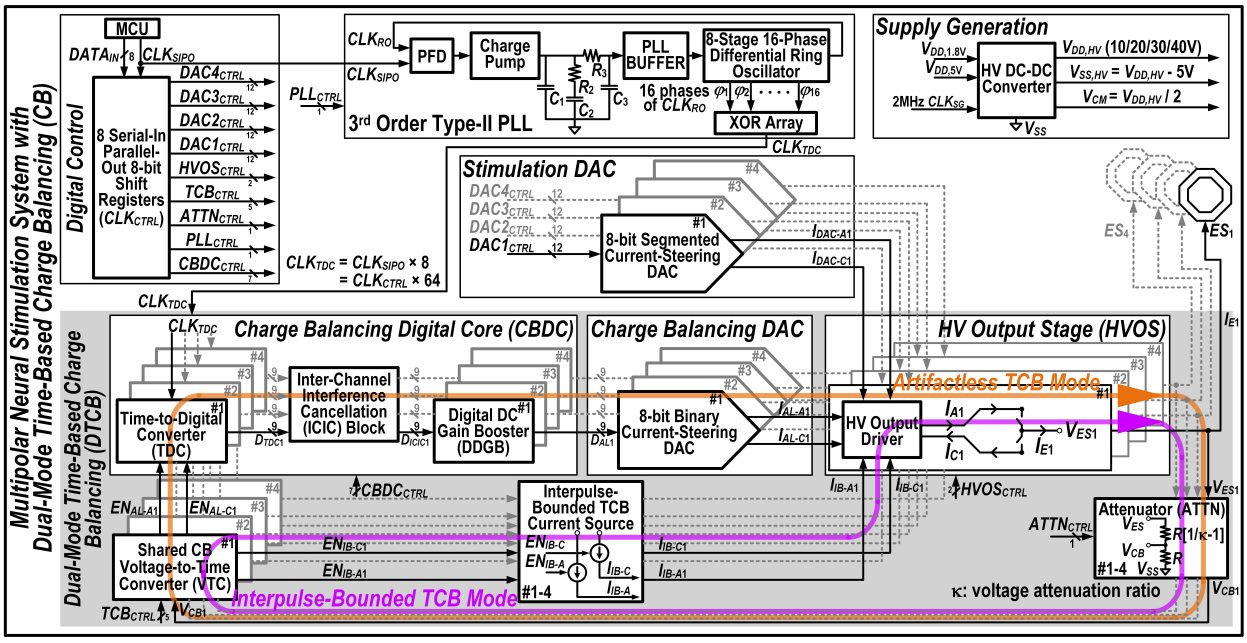


Figure 4.1: Proposed multipolar neural stimulation system with dual-mode time-based charge balancing loop.

protect the tissue whereas if the residual voltage is small, AL-TCB is enabled to suppress the voltage in several cycles of biphasic stimulation without introducing excessive stimulation artifact. In the AL-TCB mode, a digital ICIA is used to correct the digital representation of the electrode voltage to suppress ICI. In addition, a digital filter named digital DC gain booster (DDGB) following ICIA improves the charge balancing accuracy of the loop without sacrificing loop stability. Details of the proposed stimulation system are discussed in the following sections.

4.2 Proposed Multipolar Neural Stimulation System

The proposed multipolar neural stimulation system is shown in Fig. 4.1. The system has four stimulators which are controlled by the digital core independently. Each stimulator has an 8-bit segmented current-steering DAC to generate the required stimulation current waveforms and an HV output driver capable of providing a maximum current of 14 mA and voltage compliance of 40 V. The output drivers of the four stimulators are connected

to 16 electrodes through a 4 by 16 switch fabric. To compensate for the residual charges on the electrode, each stimulator is equipped with a DTCB loop with two operation modes: 1) the IB-TCB mode; 2) the AL-TCB mode. Immediately after the biphasic stimulation, the IB-TCB is activated if the electrode voltage is larger than a threshold voltage ($V_{\mathrm{TH,AL}}$), whereas the AL-TCB turns on only when the electrode voltage is less than $V_{\mathrm{TH,AL}}$. Both operations share the same attenuator and voltage-to-time converter (VTC). The attenuator lowers the sensed voltage on electrode (V_E) down to 1.8 V low-voltage (LV) regime (V_{CB}) and then the VTC converts V_{CB} to enable signals ($EN_{\mathrm{AL}\text{-}A}$, $EN_{\mathrm{AL}\text{-}C}$, $EN_{\mathrm{IB}\text{-}A}$, and $EN_{\mathrm{IB}\text{-}C}$) with their duration proportional to V_{CB}. In IB-TCB, the constant charge balancing currents ($I_{\mathrm{IB}\text{-}A}$ and $I_{\mathrm{IB}\text{-}C}$) activated by the enable signals ($EN_{\mathrm{IB}\text{-}A}$ and $EN_{\mathrm{IB}\text{-}C}$) inject directly back to the high voltage output driver to perform charge balancing in the inter-pulse time interval. On the other hand, the enable signals in AL-TCB ($EN_{\mathrm{AL}\text{-}A}$ and $EN_{\mathrm{AL}\text{-}C}$) are converted to a digital stream first by TDC (D_{TDC}). Then, D_{TDC} containing both the amplitude and polarity information is corrected and processed by ICIA and DDGB, respectively. The signal at the output of the charge balancing digital core (CBDC), namely D_{AL}, controls an 8-bit binary current-steering DAC to generate AL-TCB currents ($I_{\mathrm{AL}\text{-}A}$ and $I_{\mathrm{AL}\text{-}C}$), which are then fed back to the HV output driver to perform charge balancing by adjusting the amplitude of the following stimulation pulses. In addition, several auxiliary blocks are designed to support the main functions of the stimulation system. Eight serial-in parallel-out 8-bit shift registers receive the data ($DATA_{\mathrm{IN}}$) and clock (CLK_{SIPO}) from a microcontroller (MCU) and then provide 64 parallel signals to control the operation of the entire stimulation system. A third-order type-II PLL is used to generate the clock signal of the TDC (CLK_{TDC}) with its frequency equal to 64 times the clock frequency of the control signals (CLK_{CTRL}) from the shift registers. The PLL is comprised of a phase frequency detector (PFD), a charge pump, a third-order loop filter, a PLL buffer, an 8-stage 16-phase differential ring oscillator, and an array of XOR gates to create CLK_{TDC}. Additionally, a fully integrated HV DC-DC converter generates the necessary supply voltages to accommodate different bio-impedances.

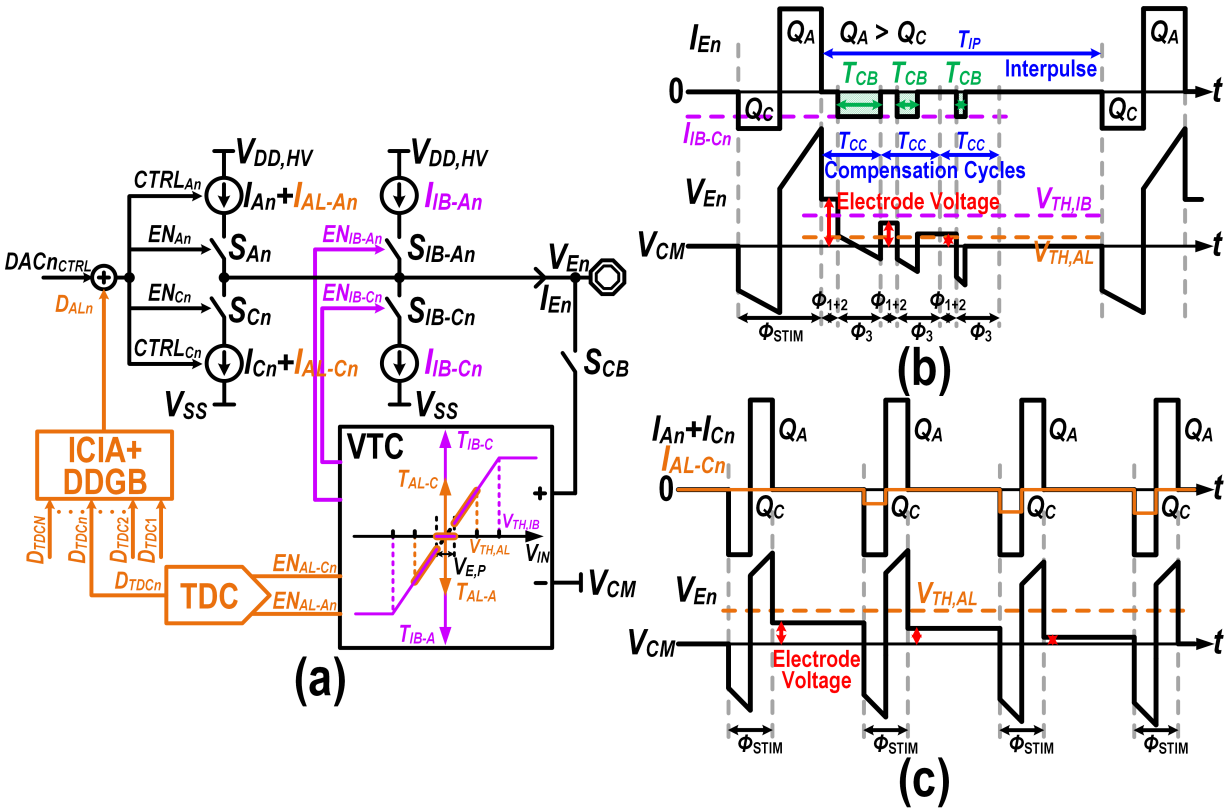


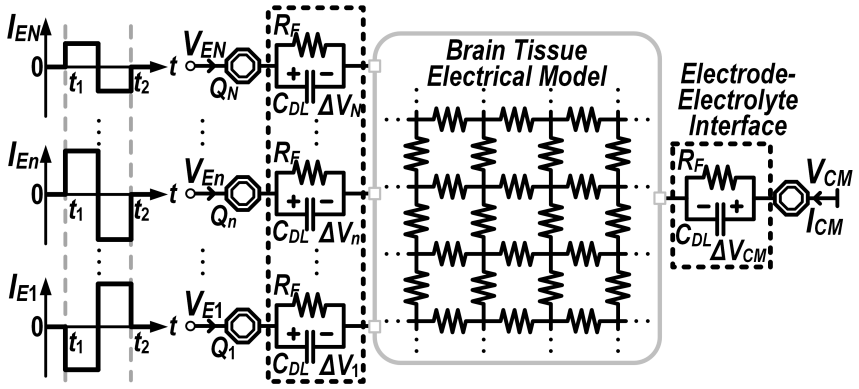
Figure 4.2: (a) Operation principle of dual-mode time-based charge balancing (DTCB) loop for the n^{th} stimulation electrode. (b) Typical waveforms of the current through the n^{th} electrode, I_{En} and the voltage on the electrode, V_{En} for the interpulse-bounded time-based charge balancing (IB-TCB) mode of DTCB. (c) Typical waveforms for the artifactless time-based charge balancing (AL-TCB) mode.

4.3 Dual-Mode Time-Based Charge Balancing Operation Principle

Assuming there are N (N=4 in this prototype) stimulators performing multipolar neural stimulation concurrently, the operation principle of the DTCB loop for the n^{th} stimulator (n=1,2, $\cdots$,N) is shown in Fig. 4.2(a). Both IB-TCB and AL-TCB loops start with sensing the voltage on the electrode (V_{En}) and comparing it with the body's quiescent potential (V_{CM}). If the initial $|V_{En} - V_{\text{CM}}|$ sensed immediately after the biphasic stimulation is larger than the threshold voltage $V_{\text{TH,AL}}$, IB-TCB is activated and the voltage difference is converted to enable signals ($EN_{\text{IB-}An}$ and $EN_{\text{IB-}Cn}$) with their duration proportional to the voltage

difference if the VTC is not saturated or the difference is large enough not to fall within the precision window of $\pm V_{\mathrm{E,P}}$. These enable signals turn on the IB-TCB currents ($I_{\mathrm{IB\text{-}}An}$ and $I_{\mathrm{IB\text{-}}Cn}$) which are injected back into the electrode in the inter-pulse time interval to perform charge balancing. Note that $I_{\mathrm{IB\text{-}}An}$ and $I_{\mathrm{IB\text{-}}Cn}$ have fixed magnitude, thus leading to a compensation charge proportional to $|V_{En} - V_{\mathrm{CM}}|$. If the initial $|V_{En} - V_{\mathrm{CM}}|$ sensed immediately after the biphasic stimulation is smaller than the threshold voltage $V_{\mathrm{TH,AL}}$, AL-TCB turns on. In the AL-TCB loop, $V_{En} - V_{\mathrm{CM}}$ is sensed the same way as in the IB-TCB loop and VTC is shared between the two loops. The VTC is designed in such a way that when the AL-TCB is enabled, the voltage-to-time conversion is always in the linear region if $|V_{En} - V_{\mathrm{CM}}|$ is larger than $V_{\mathrm{E,P}}$. Thus, the enable signals for the AL-TCB loop ($EN_{\mathrm{AL\text{-}}An}$ and $EN_{\mathrm{AL\text{-}}Cn}$) are either proportional to $|V_{En} - V_{\mathrm{CM}}|$ or stay zero as shown in Fig. 4.2(a). Subsequently, TDC converts $EN_{\mathrm{AL\text{-}}An}$ and $EN_{\mathrm{AL\text{-}}Cn}$ to a digital stream $D_{\mathrm{TDC}n}$ in two's complement and then $D_{\mathrm{TDC}n}$ is corrected and processed by ICIA and DDGB, respectively. In multipolar stimulation, ICIA uses digital streams from the TDC outputs of the AL-TCB loops of other stimulators to correct the error introduced by ICI. DDGB incorporates feed-forward paths with different gains to increase charge balancing accuracy without sacrificing the AL-TCB loop stability. Both ICIA and DDGB will be discussed in detail in the following sections. The digital stream $D_{\mathrm{AL}n}$ at the output of ICIA and DDGB is used to enable and control the amplitude of the AL-TCB currents ($I_{\mathrm{AL\text{-}}An}$ and $I_{\mathrm{AL\text{-}}Cn}$), which are added to the following biphasic stimulation pulses. Unlike in IB-TCB where $I_{\mathrm{IB\text{-}}An}$ and $I_{\mathrm{IB\text{-}}Cn}$ have fixed amplitude while the duration of the currents depends on $|V_{En} - V_{\mathrm{CM}}|$, in AL-TCB, the pulse width of the compensation currents ($I_{\mathrm{AL\text{-}}An}$ and $I_{\mathrm{AL\text{-}}Cn}$) is equal to that of the following stimulation pulses, whereas the amplitude of the current is dependent on $|V_{En} - V_{\mathrm{CM}}|$. The operation of the two loops is further illustrated in Figs. 4.2(b) and 4.2(c). After biphasic stimulation, the initial residual voltage ($|V_{En} - V_{\mathrm{CM}}|$) immediately after the second phase of the stimulation determines the mode of operation. If the initial $|V_{En} - V_{\mathrm{CM}}|$ is larger than $V_{\mathrm{TH,AL}}$, the system resets all the shift registers in the AL-TCB loop and the IB-TCB

loop turns on, as shown in Fig. 4.2(b). If the initial $|V_{En} - V_{\mathrm{CM}}|$ is smaller than $V_{\mathrm{TH,AL}}$, instead of IB-TCB, the AL-TCB loop turns on, as shown in Fig. 4.2(c). The IB-TCB, in essence, is a cycle-by-cycle operation turned on in the inter-pulse time interval between two biphasic stimulation pulses. The loop operates in three consecutive phases ($\phi_{1\text{-}3}$) within each compensation cycle T_{CC}. During ϕ_1, VTC is reset and performs auto-zeroing to significantly reduce the input-referred offset of the amplifier in VTC. Next, in ϕ_2, switch S_{CB} turns on, and the electrode voltage $V_{En} - V_{\mathrm{CM}}$ is captured by VTC, which samples and holds the voltage for the next operation of voltage-to-time conversion. After that, in ϕ_3, VTC converts $V_{En} - V_{\mathrm{CM}}$ to an enable signal ($EN_{\mathrm{IB}\text{-}An}$ or $EN_{\mathrm{IB}\text{-}Cn}$ based on the polarity) with its duration T_{CB} proportional to the magnitude of $V_{En} - V_{\mathrm{CM}}$. At the same time, the corresponding compensation current ($I_{\mathrm{IB}\text{-}An}$ or $I_{\mathrm{IB}\text{-}Cn}$) is activated for the duration of T_{CB} to perform charge balancing. As shown in Figs. 4.2(a) and 4.2(b), if $|V_{En} - V_{\mathrm{CM}}|$ is larger than a threshold voltage $V_{\mathrm{TH,IB}}$, VTC saturates and T_{CB} takes the entire ϕ_3. If $|V_{En} - V_{\mathrm{CM}}|$ is between $V_{\mathrm{TH,IB}}$ and $V_{\mathrm{E,P}}$, the voltage-to-time conversion is linear and T_{CB} is less than the duration of ϕ_3. This cycle-by-cycle operation of IB-TCB will continue to operate until the electrode voltage falls into the precision window of $\pm V_{\mathrm{E,P}}$. As shown in Fig. 4.2(c), the AL-TCB conducts charge balancing by adjusting the amplitude of the following stimulation pulses instead of injecting compensation charges in the inter-pulse time interval. After each biphasic stimulation, $|V_{En} - V_{\mathrm{CM}}|$ is captured by VTC and converted to an enable signal ($EN_{\mathrm{AL}\text{-}An}$ or $EN_{\mathrm{AL}\text{-}Cn}$ based on the polarity) similar to the VTC operation of IB-TCB, but the voltage-to-time conversion characteristics in AL-TCB does not include the saturation part because the condition of activating this loop is that the initial $|V_{En} - V_{\mathrm{CM}}|$ is less than $V_{\mathrm{TH,AL}}$, which has already fallen within the linear region of the VTC, as shown in Fig. 4.2(a). TDC converts the time domain information in the enable signal to the polarity and magnitude information in the digital domain, which is used to adjust the magnitude of either positive or negative compensation current pulse. This current pulse ($I_{\mathrm{AL}\text{-}An}$ or $I_{\mathrm{AL}\text{-}Cn}$) is injected back into the electrode along with the stimulation current pulse (I_{An} or I_{Cn}), causing no



Inter-channel interference (ICI) of the n^{th} stimulation electrode:

$$V_{En} - V_{CM} = \frac{Q_n}{C_{DL}} + \left(\sum_{n=1}^{N} Q_n \Big/ C_{DL} \right)$$

Inter-channel interference attenuator (ICIA) in analog domain:

$$\Delta V_n' = (V_{En} - V_{CM}) - \frac{1}{N+1} \sum_{n=1}^{N} (V_{En} - V_{CM})$$

ICIA in digital domain:

$$D_{ICIAn} = D_{TDCn} - \left\lfloor \frac{1}{N+1} \sum_{n=1}^{N} D_{TDCn} \right\rfloor$$

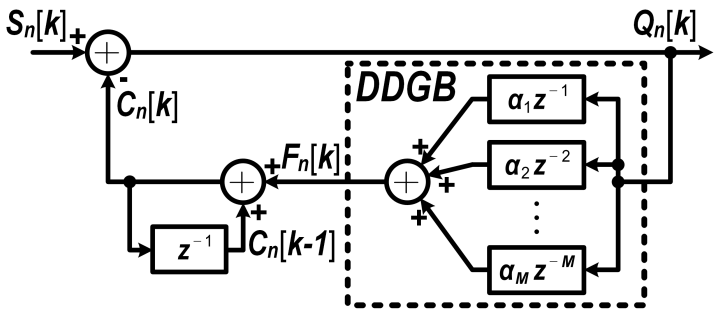
Figure 4.3: Multipolar neural stimulation electrical model, inter-channel interference (ICI), and inter-channel interference attenuator (ICIA).

extra charge-balancing-induced stimulation artifacts, as shown in Fig. 4.2(c). The AL-TCB loop will continue to operate until the stimulator is turned off or $|V_{En} - V_{\mathrm{CM}}|$ after a certain biphasic stimulation becomes unexpectedly larger than $V_{\mathrm{TH,AL}}$, which turns off the AL-TCB but turns on the IB-TCB to compensate for the charge imbalance.

4.4 Inter-Channel Interference and Its Attenuation

The multipolar neural stimulation electrical model, the effect of ICI and its solution ICIA are shown in Fig. 4.3. The multipolar stimulation model includes an electrical model for brain tissue, one electrode-electrolyte interface model for the reference electrode, and N interface models for N stimulation electrodes, respectively. The brain tissue is represented by a distributed resistive network [4] and each electrode-electrolyte interface is modeled as a double-layer capacitor C_{DL} in parallel with a Faradaic resistor R_{F} [9]. The voltage on the n^{th} stimulation electrode and the current from the n^{th} stimulator are denoted by V_{En} and

I_{En}, respectively. Initially, the voltages on all the stimulation electrodes are reset to V_{CM}. After several unmatched biphasic stimulation and when all stimulation currents are turned off, the n^{th} electrode voltage ($V_{En} - V_{\mathrm{CM}}$) is the subtraction between the residual voltage on this electrode (i.e., $\Delta V_n = Q_n/C_{\mathrm{DL}}$, where Q_n is the residual charge) and the residual voltage on the reference electrode (ΔV_{CM}). Since -ΔV_{CM} is equal to the total residual charges of all the stimulators (Q_1+Q_2+ $\cdots$+Q_N) divided by C_{DL}, then $V_{En} - V_{\mathrm{CM}}$ depends not only on ΔV_n or Q_n, but also on the residual charges of all the other stimulation electrodes. Note that most of the active charge balancing techniques rely on accurately detecting $V_{En} - V_{\mathrm{CM}}$ to determine the amplitude and polarity of the residual charge (Q_n). The influence of the residual charges of all the other stimulation electrodes on the value of $V_{En} - V_{\mathrm{CM}}$ (defined as ICI) degrades the charge balancing accuracy and increases the charge balancing time. To suppress the detrimental effect of ICI, an attenuator for ICI (ICIA) is designed to correct the value of the sensed voltage $V_{En} - V_{\mathrm{CM}}$ for the n^{th} stimulator by using the electrode voltages of all the other stimulation electrodes. This leads to a resulted voltage (i.e., $\Delta V_n^{'}$) proportional to Q_n, as shown in Fig. 4.3. Ideally, $\Delta V_n^{'}$ should be designed equal to ΔV_n and can be used to indicate the amplitude and polarity of Q_n. However, the arithmetic operation involved in ICIA is very difficult to perform in analog domain, which calls for a mixed-signal operation sensing and digitizing the electrode voltages first and then conducting ICIA in the digital domain. As shown in Fig. 4.3, $D_{\mathrm{ICIA}n}$ and $D_{\mathrm{TDC}n}$ are the digital representations of $\Delta V_n^{'}$ and $V_{En} - V_{\mathrm{CM}}$, respectively. Note that two sources of error are presented in the digital ICIA operation: (1) digitization introduced quantization error. (2) rounding down in the digital division operation. Both errors can be reduced by increasing the resolution of the TDC. In this prototype, the TDC can be configured from 6-bit to 8-bit, which is enough to make the effect of the two errors negligible.



$$\alpha_1 = G_{AA} G_{VTC} G_{TDC} \Delta_I T_{STIM} / C_{DL}$$

$$\alpha_m = \frac{\alpha_m}{\alpha_1} \cdot \alpha_1, \ \forall m = 2, 3, ..., M$$

G_{AA}: total DC gain of the attenuator and the amplifier in VTC.
G_{VTC}: voltage-to-time conversion gain.
G_{TDC}: time-to-digital conversion gain.
Δ_I: fine charge balancing DAC LSB.
T_{STIM}: the duration of both stimulation phases.

Loop gain $L(z)$: $$L(z) = -\frac{z}{z-1} \cdot \sum_{m=1}^{M} \alpha_m z^{-m}$$

Transfer function $H(z)$:
$$H(z) = \frac{Q_n(z)}{S_n(z)} = \frac{z^{M-1}(z-1)}{z^M + (\alpha_1 - 1) z^{M-1} + \alpha_2 z^{M-2} + \cdots + \alpha_M}$$

Output $Q_n(z)$:
$$Q_n(z) = \frac{Q_{Sn} z^M}{(z-1)\left[z^M + (\alpha_1 - 1) z^{M-1} + \alpha_2 z^{M-2} + \cdots + \alpha_M\right]}$$

The residual charge in steady state:
$$\lim_{k \to \infty} Q_n[k] = \left(Q_{Sn} \Big/ \sum_{m=1}^{M} \alpha_m \right) \cdot u[k]$$

Figure 4.4: Simplified artifactless time-based charge balancing discrete-time model, loop gain $L(z)$, transfer function $H(z)$, output function $Q_n(z)$, and the residual charge in steady state.

4.5 Simplified Discrete-Time Model of AL-TCB and Digital DC Gain Booster

A simplified discrete-time model of the AL-TCB loop is shown in Fig. 4.4, in which DDGB is highlighted and its operation is further illustrated in charge domain. The input ($S_n[k]$) and the feedback term used to be subtracted from the input ($C_n[k]$) are charges on the n^{th} stimulation electrode due to k cycles biphasic stimulation and charge balancing, respectively. Assuming each biphasic stimulation leads to a charge mismatch of $Q_{\text{S}n}$, then $S_n[k]$=$kQ_{\text{S}n}u[k]$

where $u[k]$ is the unit step function. The output ($Q_n[k]$=$S_n[k]$-$C_n[k]$) is total remaining charge on the n^{th} stimulation electrode after k cycles of stimulation and charge balancing. In the feedback path, DDGB uses the total remaining charge as the input and takes the summation of several delayed versions of $Q_n[k]$ with different coefficients, as illustrated in Fig. 4.4. The output of DDGB ($F_n[k]$) is the charge injected back to the n^{th} stimulation electrode due to the AL-TCB loop during the k^{th} cycle. Thus, $C_n[k]$ is the cumulative sum of $F_n[k]$ and the loop is closed by taking the integral of $F_n[k]$. Note that the digitization process, ICIA before DDGB, and digital-to-analog conversion between integrator and DDGB are neglected in Fig. 4.4 for better understanding of the loop operation. By performing analysis on the system in z-domain, the loop gain ($L(z)$), transfer function ($H(z)$), and output ($Q_n(z)$) can be calculated in terms of the coefficients in DDGB, as shown in Fig. 4.4. Assuming all poles of $H(z)$ are inside the unit circle and the system is stable, in steady state, the residual charge on the n^{th} stimulation electrode is inverse proportional to the summation of all coefficients in DDGB (see Fig. 4.4). Therefore, the summation, namely, the DC gain of DDGB should be increased to decrease the residual charge in steady state, which improves the charge balancing accuracy. For M=1, it can be proved that the system is stable only if the summation of coefficients (i.e., α_1) is less than 2, which poses a strict trade-off between the charge balancing accuracy and stability. In this prototype, this trade-off is relaxed by increasing M to 4 and setting α_1=2, α_2=1, α_3=0.5, and α_4=0.25, leading to a summation of coefficients of 3.75. the charge balancing accuracy of AL-TCB can be further improved by increasing M and performing optimization on the coefficients in DDGB at the cost of increasing complexity of digital circuitry.

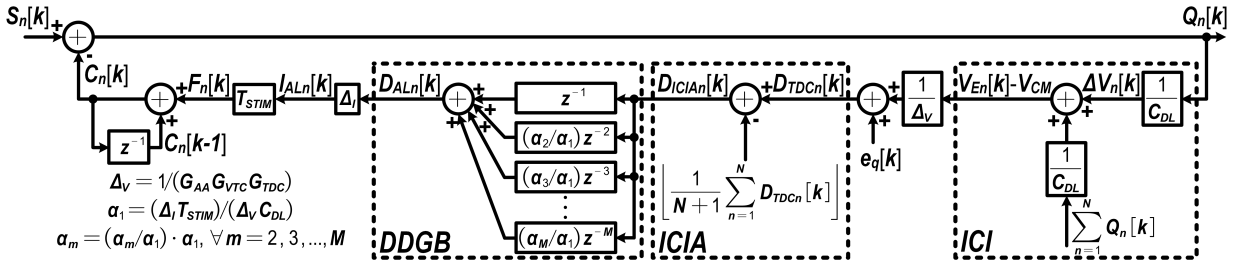


Figure 4.5: Complete discrete-time model of the artifactless time-based charge balancing (AL-TCB) loop including inter-channel interference attenuator (ICIA) and digital DC gain booster(DDGB).

4.6 Complete Discrete-Time Model of AL-TCB

Fig. 4.5 demonstrates the complete discrete-time model of the AL-TCB loop. The total residual charge $Q_n[k]$ is first divided by C_{DL} creating the residual voltage on the interface of the n^{th} stimulation electrode $\Delta V_n[k]$. Then, the summation of the residual voltages on all stimulation electrodes is added to $\Delta V_n[k]$ due to ICI (Fig. 4.3) and the result is the voltage across the n^{th} stimulation electrode and the reference electrode ($V_{En}[k]-V_{\mathrm{CM}}$). The electrode voltage is captured at the input of the charge balancing feedback path (Fig. 4.1) and then processed by the attenuator, VTC and TDC leading to a digital stream $D_{\mathrm{TDC}n}[k]$ (Fig. 4.5), which includes both the polarity and the amplitude information of $V_{En}[k] - V_{\mathrm{CM}}$. In this process, Δ_V represents the total voltage-to-digital conversion LSB and the quantization error is represented by $e_q[k]$, as shown in Fig. 4.5. After that, $D_{\mathrm{TDC}n}[k]$ is processed by the digital ICIA (Fig. 4.3) and the result ($D_{\mathrm{ICIA}n}[k]$) is the digital representation of $\Delta V_n[k]$ containing both the polarity and amplitude information of $Q_n[k]$. $D_{\mathrm{ICIA}n}[k]$ is further processed by DDGB to relax the tight trade-off between the loop stability and the charge balancing accuracy. The output of DDGB ($D_{\mathrm{AL}n}[k]$) controls both the polarity and amplitude of the AL-TCB current ($I_{\mathrm{AL}n}[k]$) through the binary current-steering DAC (Fig. 4.1). Subsequently, $F_n[k]$ is created by injecting $I_{\mathrm{AL}n}[k]$ back to the stimulation electrode during the k^{th} biphasic stimulation and the integration of $F_n[k]$ is subtracted from $S_n[k]$ to close the AL-TCB loop.

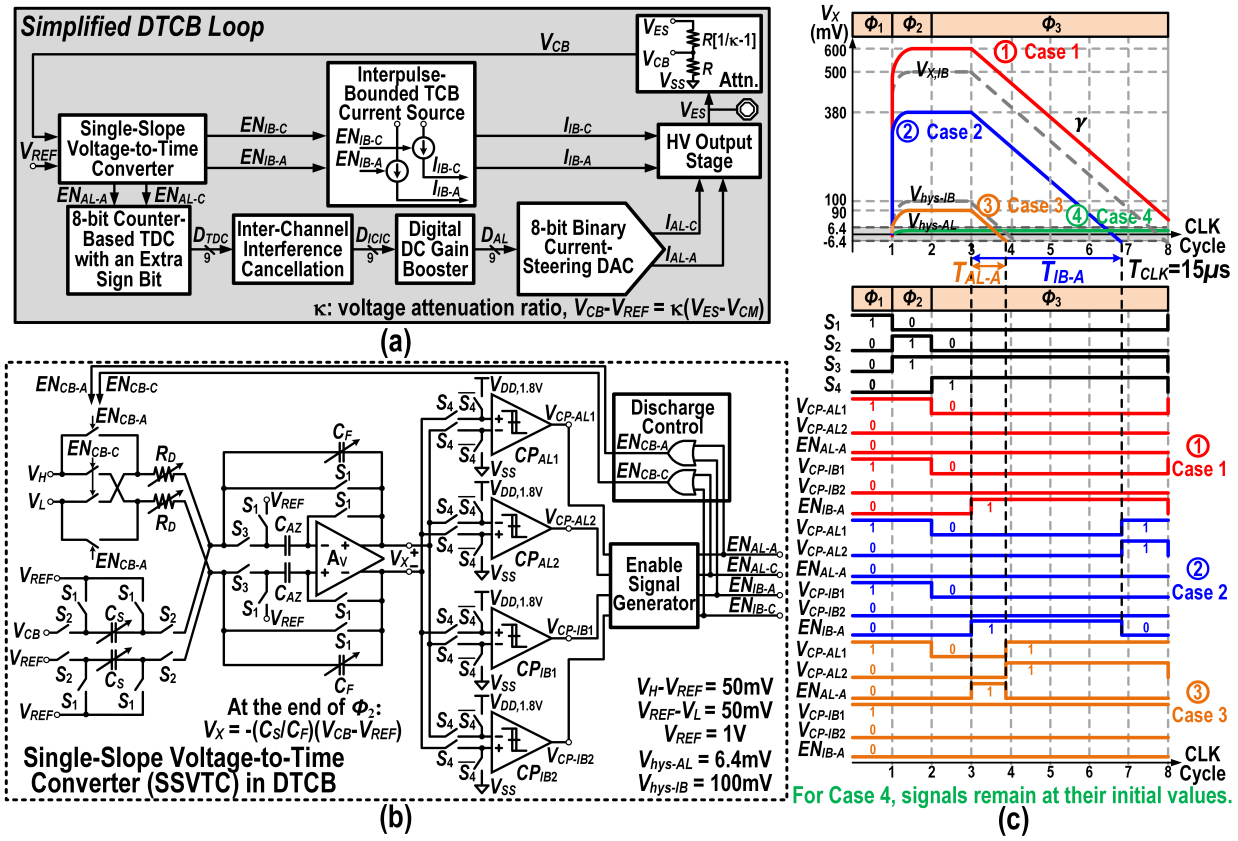


Figure 4.6: (a) Simplified dual-mode time-based charge balancing (DTCB) loop. (b) Circuit implementation of the single-slope voltage-to-time converter. (c) Voltage characteristics of V_X and the corresponding control and output signal waveforms.

4.7 Implementation of the Dual-Mode Time-Based Charge Balancing

A simplified block diagram of the DTCB loop is shown in Fig. 4.6(a). During the inter-pulse time interval, the attenuated version of V_E, V_{CB}, is compared against V_{REF} in the LV domain, and the voltage difference is processed by the single-slope voltage-to-time converter (SSVTC). Depending on the voltage difference immediately after biphasic stimulation, SSVTC determines whether to turn on the IB-TCB or AL-TCB loop by setting $EN_{\mathrm{IB}\text{-}A}$ and $EN_{\mathrm{IB}\text{-}C}$ or $EN_{\mathrm{AL}\text{-}A}$ and $EN_{\mathrm{AL}\text{-}C}$, respectively. For the IB-TCB loop, the corresponding charge balancing current $I_{\mathrm{IB}\text{-}A}$ or $I_{\mathrm{IB}\text{-}C}$ activated by $EN_{\mathrm{IB}\text{-}A}$ or $EN_{\mathrm{IB}\text{-}C}$ is injected back into the electrode

through the HV output stage to perform charge balancing. As shown in Fig. 4.6(b), the IB-TCB happens in the inter-pulse time interval, and SSVTC controls the duration of $I_{\text{IB-}A}$ and $I_{\text{IB-}C}$ though the magnitude of these currents is fixed. For the AL-TCB loop, an 8-bit counter-based TDC converts $EN_{\text{AL-}A}$ or $EN_{\text{AL-}C}$ into D_{TDC}, which contains both the polarity and amplitude information of the electrode voltage. Subsequently, D_{TDC} is corrected by ICIA (Fig. 4.3) and processed by DDGB (Fig. 4.4), and the output of DDGB (D_{AL}) determines the polarity and amplitude of the AL-TCB current ($I_{\text{AL-}A}$ and $I_{\text{AL-}C}$) through an 8-bit binary current-steering DAC. $I_{\text{AL-}A}$ or $I_{\text{AL-}C}$ is injected back into the electrode through the HV output stage during the following biphasic stimulations to avoid charge-balancing-induced stimulation artifacts, as shown in Fig. 4.2(c). The operation of SSVTC and how it is used to generate the enable signals are further illustrated in Figs. 4.6(b) and 4.6(c). As mentioned in Fig. 4.2, after each biphasic stimulation, the DTCB loop turns on and starts the first T_{CC}, and the initial electrode voltage $|V_E - V_{\text{CM}}|$ in the first T_{CC} determines whether the IB-TCB or AL-TCB should be activated. As shown in Fig. 4.2(b), each T_{CC} is comprised of three consecutive phases, reset phase (ϕ_1), amplification phase (ϕ_2), and discharging phase (ϕ_3) with ϕ_1 and ϕ_2 each taking one but ϕ_3 K clock cycles (K=6 in Fig. 4.6(c)). During ϕ_1, S_1 is activated to discharge both C_S and C_F (Fig. 4.6(b)), and the input-referred offset voltage of the amplifier A_V is stored in C_{AZ} to perform auto-zero offset cancellation. At the same time, S_4 is off and the outputs of comparators CP_{AL1} and CP_{IB1} are logic "1," while the outputs of the other two comparators CP_{AL2} and CP_{IB2} are "0" since their inputs are connected in the opposite direction (Fig. 4.6(b)). In this phase, both [$V_{\text{CP-AL1}}$, $V_{\text{CP-AL2}}$] and [$V_{\text{CP-IB1}}$, $V_{\text{CP-IB2}}$] are logic "10" (Fig. 4.6(c)), and all the enable signals at the output of SSVTC are off. In the amplification phase (ϕ_2), S_1 turns off but S_2 and S_3 turn on. The sampled and amplified version of $V_{\text{CB}} - V_{\text{REF}}$ is stored on C_F and reveals itself as V_X at the output of the amplifier (Fig. 4.6(b)). In the meantime, S_4 remains off, thus [$V_{\text{CP-AL1}}$, $V_{\text{CP-AL2}}$] and [$V_{\text{CP-IB1}}$, $V_{\text{CP-IB2}}$] will keep their "10" states and all the enable signals at the SSVTC output will remain off (Fig. 4.6(c)). In the discharging phase (ϕ_3) of the first T_{CC} immediately after

biphasic stimulation, SSVTC must determine the mode of the charge balancing operation. At the beginning of ϕ_3, S_2 turns off but S_4 turns on. The outputs of the four comparators in SSVTC ($V_{\text{CP-AL1}}$, $V_{\text{CP-AL2}}$, $V_{\text{CP-IB1}}$, and $V_{\text{CP-IB2}}$) will determine the enable signals at the output of SSVTC ($EN_{\text{AL-}A}$, $EN_{\text{AL-}C}$, $EN_{\text{IB-}A}$, and $EN_{\text{IB-}C}$) based on the value of V_X at the beginning of ϕ_3. Specifically, consider the AL-TCB and IB-TCB comparator pairs ([CP_{AL1}, CP_{AL2}] and [CP_{IB1}, CP_{IB2}]) are designed to exhibit hysteresis of $\pm V_{\text{hys-AL}}$ (= $\pm$6.4mV) and $\pm V_{\text{hys-IB}}$ (= $\pm$100mV), respectively. As shown in Fig. 4.6(c), if V_X is larger than $V_{\text{hys-IB}}$ at the beginning of ϕ_3, both outputs of the comparator pairs ([$V_{\text{CP-AL1}}$, $V_{\text{CP-AL2}}$] and [$V_{\text{CP-IB1}}$, $V_{\text{CP-IB2}}$]) will toggle from "10" to "00" (Case 1 and Case 2). Under these circumstances, only the IB-TCB loop turns on. Subsequently, in the second clock cycle of ϕ_3, $EN_{\text{IB-}A}$ will turn on to start injecting anodic compensation current $I_{\text{IB-}A}$ back into the electrode while the enable signals for the AL-TCB loop remains off. If $V_{\text{hys-AL}} < V_X < V_{\text{hys-IB}}$, [$V_{\text{CP-AL1}}$, $V_{\text{CP-AL2}}$] will switch from "10" to "00" but [$V_{\text{CP-IB1}}$, $V_{\text{CP-IB2}}$] will keep their logic values of "10" in the first clock cycle of ϕ_3 (Case 3). In this situation, the AL-TCB loop will turn on, but the IB-TCB will remain off. In the next clock cycle, $EN_{\text{AL-}A}$ will turn on and the duration of $EN_{\text{AL-}A}$ is designed to be less than one clock cycle (Fig. 4.6(c)). The pulse width of $EN_{\text{AL-}A}$ is converted to a digital stream and stored in registers to control $I_{\text{AL-}A}$ which is injected back into the electrode during the following biphasic stimulations. Note that, if the first T_{CC} is in Case 3, all the following compensation cycles within the current inter-pulse time interval are deactivated since the loop is performing AL-TCB. The operations of $V_X < -V_{\text{hys-IB}}$ and $-V_{\text{hys-IB}} < V_X < -V_{\text{hys-AL}}$ are similar to the operations of $V_X > V_{\text{hys-IB}}$ and $V_{\text{hys-AL}} < V_X < V_{\text{hys-IB}}$ above but just the polarity is the opposite (for simplicity, only the operation of $V_X > 0$ is shown in Fig. 4.6(c)). Finally, if V_X is within $\pm V_{\text{hys-AL}}$, both [$V_{\text{CP-AL1}}$, $V_{\text{CP-AL2}}$] and [$V_{\text{CP-IB1}}$, $V_{\text{CP-IB2}}$] will keep their initial states of "10" during ϕ_3 and thus neither [$EN_{\text{AL-}A}$, $EN_{\text{AL-}C}$] nor [$EN_{\text{IB-}A}$, $EN_{\text{IB-}C}$] will turn on. Therefore, DTCB determines the charge balancing mode in the first T_{CC} (Fig. 4.2(b)), and then the following compensation cycles in the current inter-pulse time interval are kept activated only if the

operation is in IB-TCB mode. In the following cycles of T_{CC}, the IB-TCB loop operates in either Case 1 or Case 2 until the residual charge is small enough to result in a V_X at the beginning of ϕ_3 falls into $\pm V_{\text{hys-AL}}$ (Case 4) and then the loop turns off and wait for the next biphasic stimulation. The difference between Case 1 and Case 2 is that, for Case 1, V_X is larger than a threshold voltage $V_{\mathrm{X,IB}}$ (= 500mV) such that $EN_{\text{IB-}A}$ is on until the end of ϕ_3 (Fig. 4.6(c)), but for Case 2, $EN_{\text{IB-}A}$ turns off before the end of ϕ_3 and the compensation time $T_{\text{IB-}A}$ is proportional to V_X and thus $V_E - V_{\mathrm{CM}}$, as mentioned in [8].

4.8 Conclusion

A multipolar neural stimulation system with DTCB for ECoG-based bi-directional BCI applications was presented. The operation of the DTCB under multipolar stimulation condition together with the analytical formulation of the AL-TCB loop using the discrete-time modeling was demonstrated. The circuit implementation, and the control and output signal waveforms of major building blocks were provided to further illustrate the detailed operation of the DTCB.

Appendix A

Appendix for Optimization Algorithm

A.1 Dipole Model

According to the dipole model, the spatial voltage distribution due to subdurally delivered stimulation can be expressed as [27]:

$$U_{\mathrm{s}}(x,y,z) = \frac{I_{\mathrm{s}}}{4\pi\sigma}\left[\frac{1}{r_{\mathrm{s}}^{+}(x,y,z)} - \frac{1}{r_{\mathrm{s}}^{-}(x,y,z)}\right] \tag{A.1}$$

where $U_{\mathrm{s}}(x,y,z)$ is the voltage amplitude seen at the observation point (x,y,z), I_{s} is the current amplitude of the primary stimulation, σ is the average bulk conductivity of the brain tissue and tissues between the electrodes and the brain (arachnoid, cerebrospinal fluid, blood vessels, and pia mater). These layers are assumed to be isotropic, homogeneous, and purely resistive volume conductors [2, 34]. r_{s}^{+} and r_{s}^{-} denote the Euclidean distances between the point (x,y,z) and the stimulating dipole source and sink electrodes, respectively. Note that the voltage and current are represented in amplitude since stimulation patterns are typically chosen as constant-magnitude biphasic pulse trains. Similar to Eq. (A.1), the spatial voltage

distribution due to the n^{th} auxiliary stimulation can be expressed as:

$$U_{\text{c},n}(x,y,z) = -\frac{I_{\text{c},n}}{4\pi\sigma}\left[\frac{1}{r^{+}_{\text{c},n}(x,y,z)} - \frac{1}{r^{-}_{\text{c},n}(x,y,z)}\right] \tag{A.2}$$

where $n = 1, ..., N$ (N–the total number of canceling dipoles), $I_{\text{c},n} = \beta_n \cdot I_{\text{s}}$ is the current amplitude of the n^{th} auxiliary stimulation ($\beta_n \in [0,1]$), and $r^{+}_{\text{c},n}$ and $r^{-}_{\text{c},n}$ denote the Euclidean distances between the point (x,y,z) and the source and sink electrodes of the n^{th} canceling dipole, respectively.

Due to the proximity and relatively small sizes of the arm or leg primary motor/sensory cortices, which are the main target areas for BD-BCIs, we assume that the curvature of ECoG grids can be neglected, even for those grids placed over the cortical convexity. Thus, a two-dimensional dipole model is sufficient to describe the voltage distribution at the cortical surface:

$$V_{\text{s}}(x,y) = U_{\text{s}}(x,y,z)\big|_{z=0} \tag{A.3}$$

$$V_{\text{c},n}(x,y) = U_{\text{c},n}(x,y,z)\big|_{z=0} \tag{A.4}$$

where $z = 0$ is the plane of the ECoG grid. The net voltage amplitude V_{t} is obtained as the algebraic summation of stimulating and canceling voltage amplitudes, i.e.,

$$V_{\text{t}}(x,y) = V_{\text{s}}(x,y) + \sum_{n=1}^{N} V_{\text{c},n}(x,y) \tag{A.5}$$

A.2 Definitions of a candidate solution *cs* and the optimal solution *os*

Since a canceling pattern involves all the canceling dipole locations and canceling currents, a candidate solution ***cs*** can be defined as:

$$\boldsymbol{cs} = \left\{ I_{\mathrm{c},1}, x^{+}_{\mathrm{c},1}, y^{+}_{\mathrm{c},1}, x^{-}_{\mathrm{c},1}, y^{-}_{\mathrm{c},1}, I_{\mathrm{c},2}, x^{+}_{\mathrm{c},2}, y^{+}_{\mathrm{c},2}, x^{-}_{\mathrm{c},2}, y^{-}_{\mathrm{c},2}, ..., I_{\mathrm{c},N}, x^{+}_{\mathrm{c},N}, y^{+}_{\mathrm{c},N}, x^{-}_{\mathrm{c},N}, y^{-}_{\mathrm{c},N} \right\} \quad \text{(A.6)}$$

where $\left(x^{+}_{\mathrm{c},n}, y^{+}_{\mathrm{c},n}\right)$ and $\left(x^{-}_{\mathrm{c},n}, y^{-}_{\mathrm{c},n}\right)$ are the coordinates of the source and sink electrodes of n^{th} canceling dipole ($n = 1, 2, ..., N$ and N is the total number of auxiliary stimulating dipoles used for cancellation, see A.3), and $I_{\mathrm{c},n} = \beta_n \cdot I_{\mathrm{s}}$ is the amplitude of the current delivered by the n^{th} canceling dipole. Accordingly, the optimal solution ***os*** is defined as:

$$\boldsymbol{os} = \left\{ I^{\mathrm{opt}}_{\mathrm{c},1}, x^{+,\mathrm{opt}}_{\mathrm{c},1}, y^{+,\mathrm{opt}}_{\mathrm{c},1}, x^{-,\mathrm{opt}}_{\mathrm{c},1}, y^{-,\mathrm{opt}}_{\mathrm{c},1}, I^{\mathrm{opt}}_{\mathrm{c},2}, x^{+,\mathrm{opt}}_{\mathrm{c},2}, y^{+,\mathrm{opt}}_{\mathrm{c},2}, x^{-,\mathrm{opt}}_{\mathrm{c},2}, y^{-,\mathrm{opt}}_{\mathrm{c},2}, ... \right. \quad \text{(A.7)}$$

$$\left. , I^{\mathrm{opt}}_{\mathrm{c},N}, x^{+,\mathrm{opt}}_{\mathrm{c},N}, y^{+,\mathrm{opt}}_{\mathrm{c},N_{\mathrm{opt}}}, x^{-,\mathrm{opt}}_{\mathrm{c},N}, y^{-,\mathrm{opt}}_{\mathrm{c},N} \right\} \quad \text{(A.8)}$$

where $\left(x^{+,\mathrm{opt}}_{\mathrm{c},n}, y^{+,\mathrm{opt}}_{\mathrm{c},n}\right)$ and $\left(x^{-,\mathrm{opt}}_{\mathrm{c},n}, y^{-,\mathrm{opt}}_{\mathrm{c},n}\right)$ represent the optimal locations of the source and sink electrodes of n^{th} canceling dipole, and $I^{\mathrm{opt}}_{\mathrm{c},n}$ is the optimal amplitude of the current delivered by the n^{th} canceling dipole ($n = 1, 2, ..., N$).

A.3 Mathematical model

To construct the mathematical model characterizing concurrent ECoG stimulation and recording, a set of model parameters MP, listed in table A.1, is introduced. Details are discussed in the following sections.

Table A.1: Mathematical model parameters (unitless unless noted otherwise).

Geometric characterization parameters	$X_\mathrm{s}, Y_\mathrm{s}$	Number of columns and rows of the stimulating ECoG grid
	$X_\mathrm{r}, Y_\mathrm{r}$	Number of columns and rows of the recording ECoG grid
	d (mm)	Electrodes contact spacing
	$x_\mathrm{rs}, y_\mathrm{rs}$ (mm)	Relative position
	θ (rad)	Relative angle
Dipole model parameter	σ (S/m)	Conductivity
Primary stimulation model parameters	$x_\mathrm{s}^+, y_\mathrm{s}^+$ (mm)	Stimulating dipole source electrode location
	$x_\mathrm{s}^-, y_\mathrm{s}^-$ (mm)	Stimulating dipole sink electrode location
	I_s (mA)	Stimulating current
Number of canceling dipoles	N	Number of auxiliary dipoles used to suppress artifacts
Constraint system parameters	β_max	Maximum allowable canceling to stimulating current ratio
	α	Tolerable sensation interference threshold

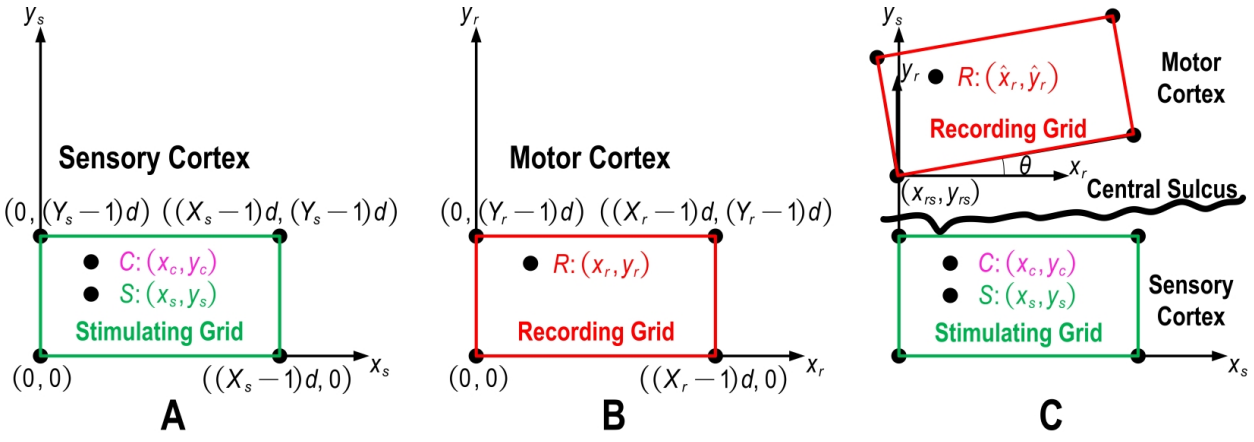


Figure A.1: **Physical configuration of the mathematical model.** A: the location of the stimulating grid. B: the location of the recording grid. C: the stimulating and recording grids in one coordinate system to show their relative position and angle.

We define electrodes contact spacing in both stimulating and recording grids to be d, and the number of rows and columns of stimulating grid to be Y_{s} and X_{s}, respectively, as shown in Fig. A.1(A). Thus, a stimulation electrode location S is represented as:

$$(x_{\mathrm{s}}, y_{\mathrm{s}}) = (p_{\mathrm{s}} \cdot d, q_{\mathrm{s}} \cdot d)\,, \quad p_{\mathrm{s}} = 0, 1, ..., X_{\mathrm{s}} - 1, \quad q_{\mathrm{s}} = 0, 1, ..., Y_{\mathrm{s}} - 1 \tag{A.9}$$

Since both primary and auxiliary stimulating dipoles deliver currents through the same stimulating grid, we also define a canceling electrode location C as:

$$(x_{\mathrm{c}}, y_{\mathrm{c}}) = (p_{\mathrm{c}} \cdot d, q_{\mathrm{c}} \cdot d)\,, \quad p_{\mathrm{c}} = 0, 1, ..., X_{\mathrm{s}} - 1, \quad q_{\mathrm{c}} = 0, 1, ..., Y_{\mathrm{s}} - 1 \tag{A.10}$$

Similarly, we define the number of rows and columns of the recording grid to be Y_{r} and X_{r}, respectively, as shown in Fig. A.1(B). Thus, a recording electrode location R is represented as:

$$(x_{\mathrm{r}}, y_{\mathrm{r}}) = (p_{\mathrm{r}} \cdot d, q_{\mathrm{r}} \cdot d)\,, \quad p_{\mathrm{r}} = 0, 1, ..., X_{\mathrm{r}} - 1, q_{\mathrm{r}} = 0, 1, ..., Y_{\mathrm{r}} - 1 \tag{A.11}$$

The physical configuration of the model is constructed by placing the recording grid into the Cartesian coordinate system whose origin coincides with the bottom-left corner of the stimulating grid, as shown in Fig. A.1(C), where $(x_{\mathrm{rs}}, y_{\mathrm{rs}})$ and θ are the relative position and angle, respectively. It follows readily that the recording electrode position $(\hat{x}_{\mathrm{r}}, \hat{y}_{\mathrm{r}})$ in this coordinate system is:

$$\hat{x}_{\mathrm{r}} = \sqrt{p_{\mathrm{r}}^2 + q_{\mathrm{r}}^2} \cdot d \cdot \cos\left(\arctan\left(q_{\mathrm{r}}/p_{\mathrm{r}}\right) + \theta\right) + x_{\mathrm{rs}} \tag{A.12}$$

$$\hat{y}_{\mathrm{r}} = \sqrt{p_{\mathrm{r}}^2 + q_{\mathrm{r}}^2} \cdot d \cdot \sin\left(\arctan\left(q_{\mathrm{r}}/p_{\mathrm{r}}\right) + \theta\right) + y_{\mathrm{rs}} \tag{A.13}$$

Therefore, from geometric characterization perspective, the model needs eight model param-

eters, namely X_{s}, Y_{s}, X_{r}, Y_{r}, d, x_{rs}, y_{rs}, and θ, to define the location of the grids and their relative position and angle. These eight model parameters depend on clinical conditions and are predefined by clinicians.

A.4 Canceling dipole physical constraint *PC*

Since the canceling dipole electrodes are chosen from those on the stimulating grid, the source and sink electrode locations of all the canceling dipoles are represented as:

$$(x^{+}_{\mathrm{c},n}, y^{+}_{\mathrm{c},n}) = (p^{+}_{\mathrm{c},n} \cdot d, q^{+}_{\mathrm{c},n} \cdot d), \forall n = 1, 2, ..., N \tag{A.14}$$

$$(x^{-}_{\mathrm{c},n}, y^{-}_{\mathrm{c},n}) = (p^{-}_{\mathrm{c},n} \cdot d, q^{-}_{\mathrm{c},n} \cdot d), \forall n = 1, 2, ..., N \tag{A.15}$$

where $p^{+}_{\mathrm{c},n}, p^{-}_{\mathrm{c},n} = 0, 1, ..., X_{\mathrm{s}} - 1$ and $q^{+}_{\mathrm{c},n}, q^{-}_{\mathrm{c},n} = 0, 1, ..., Y_{\mathrm{s}} - 1$.

Among all the possible coordinates of the canceling dipole electrode, the first sub-constraint excludes cases wherein a canceling electrode overlaps with one of the primary stimulating electrodes, which is illustrated as:

$$(x^{+}_{\mathrm{c},n}, y^{+}_{\mathrm{c},n}) \neq (x^{+}_{\mathrm{s}}, y^{+}_{\mathrm{s}}), \forall n = 1, 2, ..., N \tag{A.16}$$

$$(x^{+}_{\mathrm{c},n}, y^{+}_{\mathrm{c},n}) \neq (x^{-}_{\mathrm{s}}, y^{-}_{\mathrm{s}}), \forall n = 1, 2, ..., N \tag{A.17}$$

$$(x^{-}_{\mathrm{c},n}, y^{-}_{\mathrm{c},n}) \neq (x^{+}_{\mathrm{s}}, y^{+}_{\mathrm{s}}), \forall n = 1, 2, ..., N \tag{A.18}$$

$$(x^{-}_{\mathrm{c},n}, y^{-}_{\mathrm{c},n}) \neq (x^{-}_{\mathrm{s}}, y^{-}_{\mathrm{s}}), \forall n = 1, 2, ..., N \tag{A.19}$$

The second sub-constraint excludes cases wherein two canceling dipoles share electrodes,

which is shown as:

$$(x_{\mathrm{c},i}^{+}, y_{\mathrm{c},i}^{+}) \neq (x_{\mathrm{c},j}^{+}, y_{\mathrm{c},j}^{+}), \forall i, j = 1, 2, ..., N \text{ and } i \neq j \tag{A.20}$$

$$(x_{\mathrm{c},i}^{+}, y_{\mathrm{c},i}^{+}) \neq (x_{\mathrm{c},j}^{-}, y_{\mathrm{c},j}^{-}), \forall i, j = 1, 2, ..., N \text{ and } i \neq j \tag{A.21}$$

$$(x_{\mathrm{c},i}^{-}, y_{\mathrm{c},i}^{-}) \neq (x_{\mathrm{c},j}^{+}, y_{\mathrm{c},j}^{+}), \forall i, j = 1, 2, ..., N \text{ and } i \neq j \tag{A.22}$$

$$(x_{\mathrm{c},i}^{-}, y_{\mathrm{c},i}^{-}) \neq (x_{\mathrm{c},j}^{-}, y_{\mathrm{c},j}^{-}), \forall i, j = 1, 2, ..., N \text{ and } i \neq j \tag{A.23}$$

A.5 Derivation of the interference function *IF*

By substituting $U_{\mathrm{s}}(x, y, z)$ and $U_{\mathrm{c},n}(x, y, z)$, defined in A.1, into Eq. 2.5, the activating functions due to the stimulating dipole $AF_{\mathrm{s}}(x, y, z)$ and the n^{th} canceling dipole $AF_{\mathrm{c},n}(x, y, z)$, $n = 1, ..., N$, are derived to be:

$$af_{\mathrm{s}}(x, y, z) = \frac{I_{\mathrm{s}}}{4\pi\sigma}\left[-\frac{\left(r_{\mathrm{s}}^{+}(x, y, z)\right)^2 - 3z^2}{\left(r_{\mathrm{s}}^{+}(x, y, z)\right)^5} + \frac{\left(r_{\mathrm{s}}^{-}(x, y, z)\right)^2 - 3z^2}{\left(r_{\mathrm{s}}^{-}(x, y, z)\right)^5}\right] \tag{A.24}$$

$$af_{\mathrm{c},n}(x, y, z) = -\frac{I_{\mathrm{c},n}}{4\pi\sigma}\left[-\frac{\left(r_{\mathrm{c},n}^{+}(x, y, z)\right)^2 - 3z^2}{\left(r_{\mathrm{c},n}^{+}(x, y, z)\right)^5} + \frac{\left(r_{\mathrm{c},n}^{-}(x, y, z)\right)^2 - 3z^2}{\left(r_{\mathrm{c},n}^{-}(x, y, z)\right)^5}\right] \tag{A.25}$$

where r^{+} and r^{-} represent the distances from observation point (x, y, z) to dipole source and sink electrodes, respectively.

The interference constraint IC is based on two assumptions. First, since $af_{\mathrm{s}}(x, y, z)$ reaches the maximum right beneath the two primary stimulating electrodes, we assume that the artificial sensation happens underneath the primary stimulating dipole where the interference is needed to be evaluated. Thus, (x, y) is equal to $(x_{\mathrm{s}}^{+}, y_{\mathrm{s}}^{+})$ or $(x_{\mathrm{s}}^{-}, y_{\mathrm{s}}^{-})$. To explicitly

demonstrate all the variables to be optimized in the candidate solution ($\boldsymbol{cs}$), the activating functions are written as $AF_{\mathrm{s}}(z)$ and $AF_{\mathrm{c},n}(\boldsymbol{cs}, z)$, where

$$AF_{\mathrm{s}}(z) = af_{\mathrm{s}}(x,y,z)|_{(x,y)=(x_{\mathrm{s}}^{+},y_{\mathrm{s}}^{+}) \text{ or } (x,y)=(x_{\mathrm{s}}^{-},y_{\mathrm{s}}^{-})} \tag{A.26}$$

$$AF_{\mathrm{c},n}(\boldsymbol{cs}, z) = af_{\mathrm{c},n}(x,y,z)|_{(x,y)=(x_{\mathrm{s}}^{+},y_{\mathrm{s}}^{+}) \text{ or } (x,y)=(x_{\mathrm{s}}^{-},y_{\mathrm{s}}^{-})} \tag{A.27}$$

Second, since the averaged thickness of CSF plus cortex is around 6.5 mm [37, 38], we postulate that the sensation can be predicted by the activating function along the z-axis from $z = -6.5$ mm to $z = 0$ mm. Therefore, the regions of interest we need to evaluate the interference are $(x_{\mathrm{s}}^{+}, y_{\mathrm{s}}^{+}, z)$ and $(x_{\mathrm{s}}^{-}, y_{\mathrm{s}}^{-}, z)$ where $z \in [-6.5, 0]$. Under the above assumptions, we introduce an interference function (IF) which is defined to be the absolute value of the ratio between the activating functions of the canceling currents and stimulating current, i.e.,

$$IF(\boldsymbol{cs}, z) = \left| \frac{\sum_{n=1}^{N} AF_{\mathrm{c},n}(\boldsymbol{cs}, z)}{AF_{\mathrm{s}}(z)} \right| \tag{A.28}$$

IC states that, at the observation point located underneath the stimulating dipole, if IF is less than the tolerable interference threshold α (e.g., 0.5%), the influence of auxiliary stimulation on the artificial sensation can be neglected.

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