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Investigations of Tunneling for Field Effect Transistors

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Investigations of Tunneling for Field Effect Transistors

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Abstract

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Over 40 years of scaling dimensions for new and continuing product cycles has introduced new challenges for transistor design. As the end of the technology roadmap for semiconductors approaches, new device structures are being investigated as possible replacements for traditional metal-oxide-semiconductor field effect transistors (MOSFETs). Band-to-band tunneling (BTBT) in semiconductors, often viewed as an adverse effect of short channel lengths in MOSFETs, has been discussed as a promising current injection mechanism to allow for reduced operating voltage for beyond MOSFET technology.

This dissertation discusses the proposal of BTBT for tunneling field effect transistors (TFETs). Some early work is briefly reviewed to better appreciate the academic research landscape regarding BTBT. Then, experimental observations of a steeply switching enhanced-Schottky-barrier MOSFET are analysed in detail and the steep characteristic is plausibly explained by metal impurity trap states near the source tunneling junction. Next, follow-up experiments to investigate the role of traps in BTBT are reviewed with a likely explanation that traps in close proximity to the tunneling junction can lower the activation energy for BTBT. Finally, a source design study for a planar homojunction germanium-on-insulator TFET finds that a static reverse bias can dramatically alter the optimal doping profile for the source tunneling junction and highlights the importance of tight electrostatic control for improved $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ in TFETs.

To my family and friends.

For their continual support throughout my graduate school odyssey, most especially my parents and my siblings for their limitless patience and understanding.

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Chapter 1

Introduction

1.1 CMOS Solid State Switching Devices

The continued improvement of metal-oxide-semiconductor field effect transistor (MOSFET) performance is due in large part to the scalability of semiconductor manufacturing and demand driven new-product cycles. A simple description of a MOSFET is as follows: with a bias applied between the source and the drain, the gate electrode can dramatically alter the resistance of the channel by capacitively coupling to the semiconductor region immediately below the gate. A schematic cross-section of a MOSFET is presented in Fig. 1.1. The gate capacitively couples to the silicon (Si) substrate and controls a source side energy barrier, modulating the current flowing from the source to the drain (see Fig. 1.2).

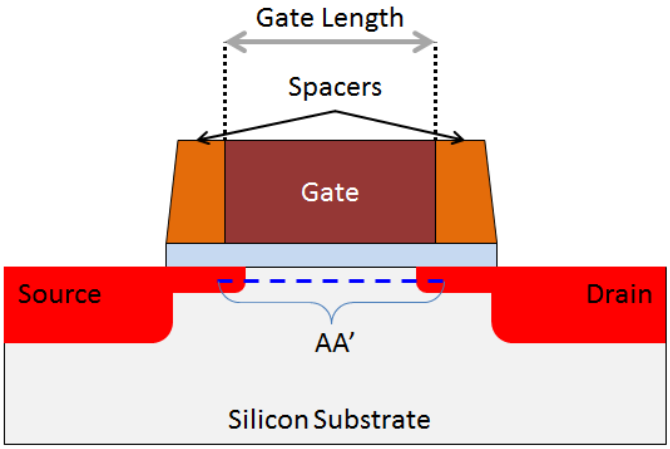

Figure 1.1: A schematic cross-section of a typical MOSFET. Historically, scaling down the printed gate length improved I_{ON}. MOSFET design requires a balance between the separation distance between the source and drain doping profiles and the operating voltage of the device. The cut-line AA' approximately references the location of the channel for the band diagram in Fig. 1.2

Scaling, or reducing key physical dimensions of the transistor structure, has regularly

improved device performance and density for over 40 years. With decreasing critical dimensions and increasing device density, new design challenges are continually addressed to meet the demand in a growing market for electronics. An important concern raised in literature (e.g., reference [1]) is that an increase in the passive power density for current MOSFET technology is unavoidable with continued scaling. Various alternative devices have been proposed to replace or complement MOSFETs and all are designed to maintain or improve performance while reducing the off-state power consumption.

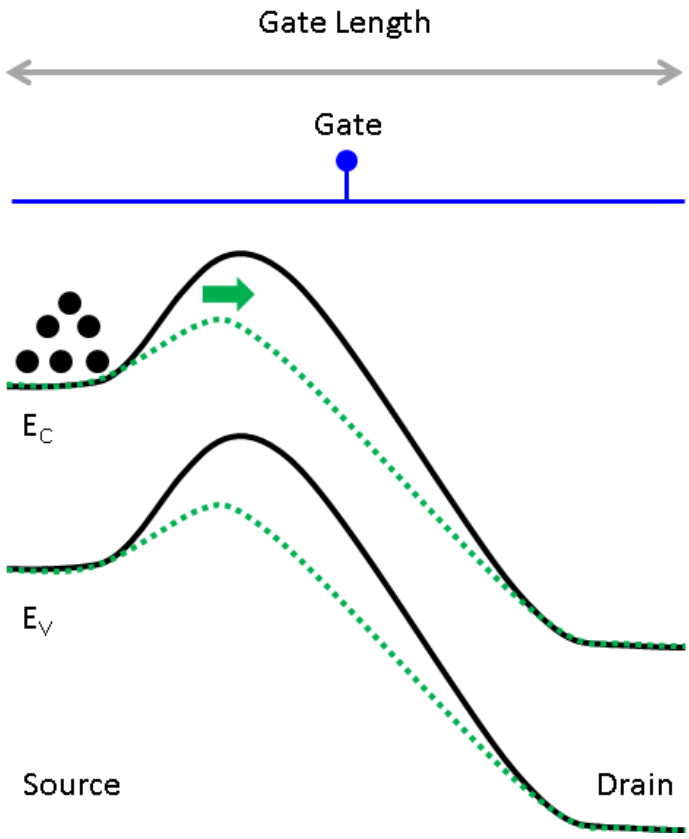

Figure 1.2: A band diagram for the MOSFET from the AA' cutline in Fig. 1.1. The off-state (black lines) presents a source side energy barrier to prevent carriers from entering the channel. In the on state (green dotted lines), the barrier is lowered and carriers move from the source to the drain.

1.2 Proposed Alternatives to CMOS-based Logic

A lower limit for the switching efficiency of a MOSFET relates the strength of the capacitive coupling of the gate to the distribution of mobile charge carriers in the source. For MOSFETs, the distribution of carriers in the source is sometimes referred to as a Boltzmann distribution in energy peaking near the conduction (valence) band edge for an n-channel (a

p-channel) device.[2] A metric for the efficiency of gate coupling to the channel is the inverse subthreshold slope, SS:[1]

$$SS = \left(\frac{d\left(\log_{10} I_{\mathrm{D}}\right)}{dV_{\mathrm{GS}}} \right)^{-1} = \ln\left(10\right) \frac{k_{\mathrm{B}}T}{q} \left(1 + \frac{C_{\mathrm{dm}}}{C_{\mathrm{ox}}} \right). \tag{1.1}$$

In equation 1.1, k_{B} is Boltzmann's constant, q is the charge of one electron, C_{ox} is the areal gate oxide capacitance and C_{dm} is the areal depletion layer capacitance. Equation 1.1 approaches a lower limit of approximately 60 mV/dec at T = 300K when ${}^{C_{\mathrm{dm}}}/_{C_{\mathrm{ox}}}$ is close to zero.

Scaling has historically involved decreasing L_{G} and increasing C_{ox} (by decreasing the effective oxide thickness) so as to increase I_{ON}. Even with the co-optimization of material properties (e.g., peak doping concentration, strain engineering), an aggressively scaled MOSFET can exhibit short channel effects that reduce the gate control of the channel. New device structures have been proposed to replace MOSFETs when decreasing L_{G} and increasing C_{ox} is no longer possible due to material constraints (or economically viable).

A promising alternative for new current injection mechanisms is any switch that is not limited to a $\frac{k_{\mathrm{B}}T}{q}\ln\left(10\right)$ minimum. Fig. 1.3 qualitatively shows the benefit of a low SS for an alternative device. A steeply switching device allows for a lower threshold voltage, V_{T}, (hence a lower power supply voltage, V_{DD}) and the possibility of a lower I_{OFF} which decreases the passive power consumption.

Proposals for alternative devices include scaled down mechanical relays [3], impact ionization FETs [4], feedback FETs [5], FETs with negative gate capacitance [6], and band-to-band tunneling (BTBT) FETs.[7] This dissertation explores the properties of BTBT and trap-assisted tunneling (TAT) in the context of tunneling FETs (TFETs).

[1] SS equally refers to the subthreshold swing.

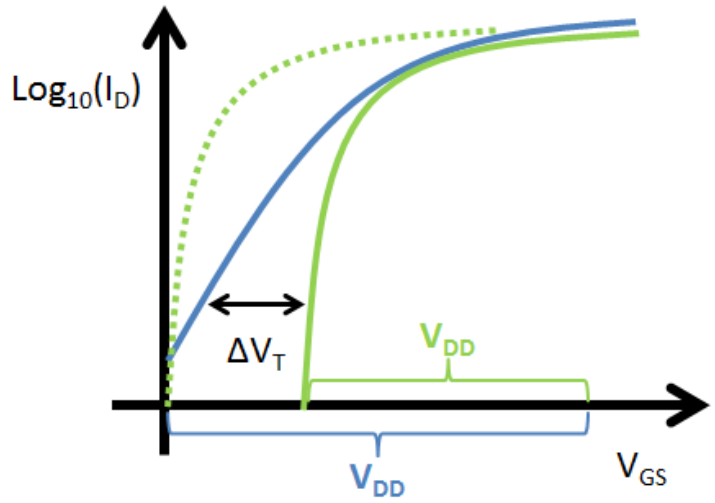

Figure 1.3: A steeply switching device proves a compelling goal for a MOSFET replacement. The blue curve represents a traditional MOSFET I-V transfer characteristic. The solid green curve comparatively highlights the main benefit of a steeper transfer characteristic: a reduction in the power supply voltage, V_{DD}. Presumably, a steeper SS characteristic can be threshold-voltage shifted (as depicted in the dashed green curve).

1.3 Tunneling Field Effect Transistors: Basic Design and Operation

Models for the tunneling probability and the tunneling current (via BTBT) in semiconductors were succinctly and nearly simultaneously proposed by Leonid V. Keldysh and Evan O. Kane.[8, 9] Equation 1.2 gives the tunneling current density for a direct bandgap material commonly found in literature.[10]

$$J_{\mathrm{T}} = \frac{2\sqrt{2m^*}q^2F}{3\pi^3\hbar^2E_{\mathrm{g}}^{1/2}} \exp\left[-\frac{\pi\sqrt{m^*}E_{\mathrm{g}}^{3/2}}{2\sqrt{2}\hbar qF}\right] \tag{1.2}$$

m^* is the carrier effective mass, F is the electric field, E_{g} is the semiconductor bandgap, and $\hbar$ is Planck's constant. Consolidating the electric field pre-factors of equation 1.2 gives the more common expression for Kane's equation,

$$J_{\mathrm{T}} = AF \cdot e^{-B/F}, \tag{1.3}$$

where A and B represent material properties for the semiconductor of interest. For a TFET, equation 1.3 implies that the BTBT generation rate of carriers into the channel is exponentially sensitive to the electric field at the tunneling junction. Whereas for a MOSFET, the population of carriers in the channel is exponentially sensitive to the surface potential (or the channel potential).

Immediately apparent in equations 1.2 and 1.3 is that a larger electric field at the tunneling junction produces a larger BTBT current (i.e., a larger I_{ON}). Incorporating a larger built-in electric field into the design of a TFET should then increase I_{ON} (and thus performance) for a given power supply voltage. A conventional TFET design typically utilizes a very steep doping profile in the source in order to realize a large built-in electric field near the BTBT junction. Despite advancements in low energy ion implantation, flash annealing, and *in situ* doping during epitaxial growth, fabricating very steep doping profiles remains a challenge.

In 1994, Reddick and Amaratunga proposed and fabricated the first known Si based BTBT transistor.[11] Motivated by the potential for increased functionality due to negative differential resistance observed in other tunneling devices, a gated reverse biased diode was fabricated on bulk Si. This proposed structure called for modulating the tunneling current by modulating the tunneling barrier width, determined in part by the band gap (E_{g}), the applied bias, and the depletion width.[11] Reddick and Amaratunga also acknowledged the potential advantage of a necessarily narrow tunneling barrier for the purpose of scaling beyond complementary MOS (CMOS) transistor technology limits.

Since 1994, numerous experimental avenues seeking sub-60 mV/dec SS at room temperature have been explored. Most approaches have focused (and continue to focus) on the importance of a large built-in electric field obtained either by *in situ* epitaxial growth, heterostructure formation, 1D quantum confinement, or hyperabrupt depleted pocket doping.[7, 12–15]

1.4 Thesis Organization

This dissertation details three experiments investigating the role of traps within or near a tunneling junction and follows with a new design approach for a simplified source doping profile design without an ambitiously steep gradient. In chapter 2, a SB-MOSFET structure is modified to take advantage of a steep doping profile obtained via dopant segregation from silicide. Sub-$\frac{k_{\mathrm{B}}T}{q}\ln(10)$ SS is observed and interpreted as a trap based tunneling process followed by thermionic emission of carriers near the source.

In chapter 3, erbium (Er) impurity atoms are purposely introduced into Si near a heterojunction formed with p+ poly-crystalline germanium (Ge). The presence of traps in p-i-n heterodiodes is verified with temperature dependent measurements and a trap-assisted tunneling simulations using a commercially available TCAD semiconductor device simulation software package. A very low activation energy, E_{A}, is observed for a p+/n+ heterodiode with Er electronic trap states present within the bandgap of Si and TCAD simulations highlight the limitations of tunneling models for tunneling into and out of trap states.

Er based trap-assisted TFETs (Er-TATFETs) were fabricated on silicon-on-insulator (SOI) substrates and subsequently characterized. Results from temperature-dependent measurements are presented in chapter 4. Low temperatures (T $\leq \sim$200K) were necessary in order to mitigate thermal generation current due to trap states. The E_{A} in the subthreshold

regime for Er-TATFETs was found to be slightly lower in comparison to the E_{A} for p-i-n control TFETs.

Chapter 5 extends an SOI TFET simulation study to explore the role of reverse back bias for n-channel germanium-on-insulator (GeOI) based TFETs. A gate-overlapped source is found to provide superior $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ enhancement with $V_{\mathrm{B}} < 0V$ in comparison to a steeply graded gate-aligned source. Applying a reverse back bias with a gate-overlapped source can trigger a large area tunneling junction at turn-on and also mitigate some SCEs.

Finally, chapter 6 summarizes this dissertation and highlights some of challenges facing TFET devices.

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Chapter 2

Enhanced Schottky Barrier MOSFET with Steep Subthreshold Swing at Low Current

2.1 Introduction

When a metal is placed in intimate contact with a semiconductor surface, an intrinsic potential barrier forms at the interface between the metal and the semiconductor and is referred to as a Schottky barrier (SB).[1] A non-zero barrier acts to disrupt (though not prohibit) the free flow of charge carriers across the interface and a depletion region forms in equilibrium to maintain charge neutrality.[1] The value of this SB and how it can be modified is important when designing low resistance contacts to semiconductor devices such as diodes, transistors, and resistors.

Metal-semiconductor alloys are routinely formed to reduce the contact resistance of semiconductor devices. For a silicon based device, the alloy is a silicide and serves as the metal in a metal-semiconductor junction. Silicides are the result of an elevated temperature alloying process referred to as silicidation. For a MOSFET, proper design of the transistor allows for self-aligned silicidation to take place. For example, platinum is deposited as a blanket film on top of a MOSFET structure; under thermal treatment, platinum-silicide (PtSi) forms where Si is exposed to the Pt film. If Pt does not react with the underlying material, the silicidation process is selective and forms only where Si is exposed.

A Schottky barrier MOSFET (SB-MOSFET) is similar to a conventional MOSFET but utilizes a SB interface at the source and drain junctions instead of an impurity doped semiconductor. A generic SB-MOSFET is schematically shown in Fig. 2.1. The main difference between the two device structures is that the source-side potential barrier of a MOSFET is replaced by a SB with an associated Schottky barrier height (SBH). Replacing the source and drain doping profiles with a silicide holds some promise towards addressing challenges

[1] For real material systems.

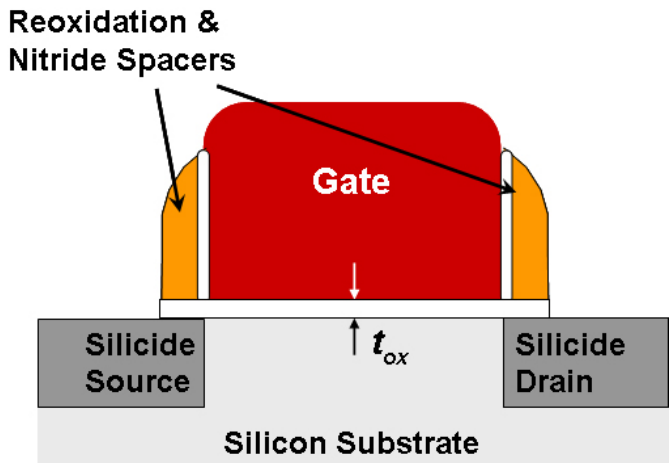

Figure 2.1: A SB-MOSFET device structure. The metal (or silicide) source and drain are well aligned with the gate edge.

associated with scaling the source and drain profiles in a conventional MOSFET. Reference [2] provides a good introduction to SB interfaces, some underlying physics and assumptions, as well as a topical review of the present state of SB-MOSFETs.

Ideally, a well-designed SB-MOSFET provides a solution to various scaling problems including:[2, 3]

- Low parasitic resistance or access resistance.
- Reduced variability due to source and drain extension profiles near the channel.
- Improved mitigation of short channel effects (SCE).
- Reduced off-state leakage due to the intrinsic SBH.
- Elimination of parasitic bipolar action.

In Fig. 2.1, the source and drain SB junctions are closely aligned to the gate edge with no gate-to-metal overlap. Aligning the SB interface near the gate edge is important so that capacitive control of the channel is not compromised.

A key design goal for a SB-MOSFET is a low SBH for carriers injected into the channel. A low SBH increases the on-current (I_{ON}) (in strong inversion) and presumably the transistor performance. The intrinsic SBH is determined by the silicide-silicon work function difference. A SBH can be modified, however, by doping the silicon near the SB.[4] Figure 2.2 shows a band diagram alignment for a SB interface with and without dopants modifying the SBH.

Optimal SB-MOSFET design necessitates the careful choice of metal for the silicide formation. An additional requirement is that the silicide formation must also be manageable from a fabrication perspective. The silicidation process involves the co-diffusion of Si into

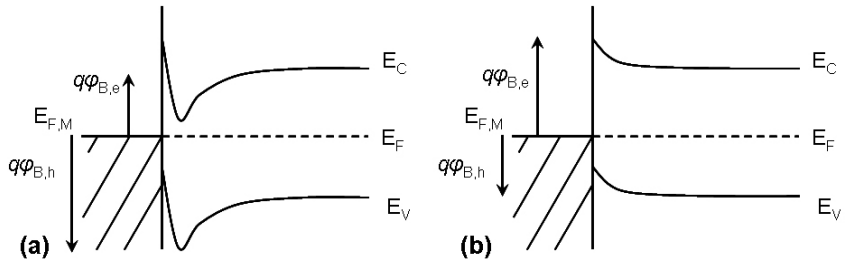

Figure 2.2: Band diagram of a metal-semiconductor interface with (a) and without (b) dopants. Dopants near the interface are used to engineer, or adjust, the SBH. ϕ_B is the SB potential.

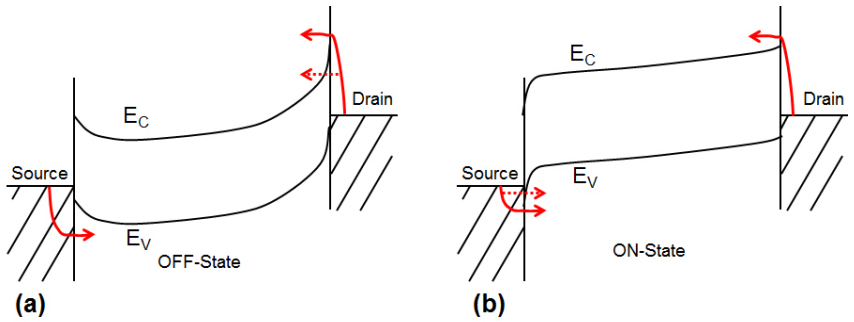

Figure 2.3: Qualitative band diagrams of a SB-MOSFET in the (a) off-state and (b) the on-state. Various leakage (a) and current injection routes (b) are highlighted in the schematic.

the metal and vice-versa. This alloying reaction produces a reactive interface, or reaction front, which moves away from the original metal-silicon interface.[5] The choice of the metal, optional interface materials, silicidation temperature, and geometry of the silicon device all factor into the final position of the silicide-silicon interface. Consequently, SB junctions well aligned to the gate edge present a processing and device physics challenge.

Fig. 2.3 shows band diagrams in the off-state and on-state of a SB-MOSFET. When the potential drop across the source-side SB junction is large enough, the depletion width in the semiconductor narrows such that field emission tunneling current, I_{FE}, through the thin triangular barrier is appreciable and becomes the dominant current injection mechanism. In this way, I_{ON} is limited by the SBH at the source. When the SBH is too large, a smaller fraction of the available states in the metal source contributes to current injection. In general, SB-MOSFET non-idealities include low I_{ON}, subsurface SB junction leakage away from the active channel of the device, and parasitic metal-semiconductor diode behavior apparent in the output characteristics ($I_D(V_{GS}, V_{DS})$ vs. V_{DS}).[2]

SB-MOSFET fabrication techniques provide an additional avenue towards fabricating an alternative solid-state switching device. Modifying the SBH using dopant segregation of impurities implanted into silicide (ITS), relatively steep doping profiles can be realized

with a low thermal budget.[4] As discussed in chapter 1, a steep doping profile yields a large built-in potential and thus a large built-in electric field near the proposed tunneling junction. Since the band-to-band tunneling (BTBT) probability increases nearly exponentially with the electric field, a large built-in potential near the tunneling junction is desirable.

2.2 Silicide/Silicon Interface

An inherent shortcoming of any thermal process in forming a silicide is the stochastic nature of small imperfections in the initial conditions during semiconductor processing. Most theoretical and empirical models typically assume an atomically abrupt interface regarding metal-semiconductor junctions.[2, 6] However, the formation of a silicide by thermal processing necessarily involves co-diffusion of metal atoms into Si and Si atoms into the metal.[5] Fick's law of diffusion can be applied to a silicide growth system assuming steady state conditions [2] during certain phases of the growth.[7, 8] For diffusion limited silicide formation, the final atomic profile of a metal impurity in silicon represents an exponential decay extending from the silicide/silicon interface.[9] The metal impurity peak concentration is strongly correlated with the final silicide stoichiometry and nearly equals the atomic density of crystalline silicon. The characteristic decay length is governed by the time and temperature of the silicidation process.

Another consideration is the orientation of silicide grains as the silicide forms. While on aggregate the reaction interface can be smooth (as schematically depicted in [5]), silicides commonly considered for SB-MOSFET applications are known to be poly-crystalline. As such, each grain in the poly-crystalline silicide forms in an energetically favorable orientation for that particular localized reaction front. Consequently, silicide/silicon interfaces appear rough on a scale close to or less than the average grain size. This is unfortunate in the context of scaled SB-MOSFETs in that the silicide/silicon interface is not atomically abrupt and inherently leads to variability.[10] The stochastic nature of the resulting interface increases device sensitivity to key device parameters such as subthreshold swing (SS) and threshold voltage, V_{T}. Reducing variability is important in almost any type of device scaling, especially for alternative devices such as TFETs where the SS is very sensitive to local electric field fluctuations at the tunneling junction.

As a result, a silicide/silicon interface for the purpose of a steeply switching transistor must, in addition to previous requirements on processing and device design, be uniform across the width of the device if the interface is close to the tunneling junction. One contributing factor to a rough interface is the rapid thermal anneal (RTA) process often used to form a silicide. While an RTA process can reduce the thermal budget, poly-crystalline grain size can be sensitive to RTA process parameters. By trading a short RTA process time for a longer temperature ramping time, localized temperature fluctuations at the silicide reaction front can be mitigated.

[2] Such as constant flux or diffusion limited growth.

Finally, using a Kissinger analysis to model the silicide thickness with the classical growth rate equation (equation 2.1) yields a predictive RTA process parameter set which can be incorporated into a modified SB-MOSFET design. The growth rate equation predicts the silicide thickness, Z, for a known activation energy, E_A, temperature dependent diffusivity, $D = D_0 \exp\left(\frac{-E_A}{k_B T}\right)$, pre-exponential diffusion coefficient, D_0, a given temperature range from T_0 to T, and a known temperature ramp rate, dt/dT: [5, 8, 11]

$$Z^2 = \int_0^t D dt = \int_{T_0}^{T} D \left(\frac{dT}{dt}\right)^{-1} dT$$
$$= D_0 \left(\frac{dT}{dt}\right)^{-1} \frac{k_B}{E_A} \left\{ T^2 \exp\left(-\frac{E_A}{k_B T}\right) - T_0^2 \exp\left(-\frac{E_A}{k_B T_0}\right) \right\}. \quad (2.1)$$

When the temperature remains constant, the thickness is simply estimated by integrating 2.1 (without a variable substitution) to obtain

$$Z^2 = D(T) \cdot t. \quad (2.2)$$

Predictive modeling of the silicide thickness allows for a lower temperature ramp rate with the end goal of a uniform silicide/silicon interface.

Additionally, when engineering the SBH with doping near the interface, the ITS method piles up dopants near the interface, similar to dopant segregation induced by silicidation. However, the ITS method results in a steeper doping profile.[12]

Thus, key requirements for an adequate silicide/silicon interface include:

- Known diffusion coefficients and activation energies for the metal-silicon material system.
- A steep, electronically active impurity doping profile near the gate edge.
- A desirable work function yielding a low SBH for the injected charge carriers.
- A uniform, or smooth, silicide/silicon interface parallel to the gate edge.

2.3 Modified Designs for Band-to-Band Tunneling

PtSi was chosen as the lead candidate material for the source and drain for a modified SB-MOSFET design. PtSi formation is relatively well understood with a low intrinsic SBH for holes for p-channel FET operation and satisfies many of the aforementioned requirements.[4, 5, 8, 12] To redesign a SB-MOSFET for BTBT current, an asymmetric p-i-n doping profile is incorporated across the channel region. An additional method to enhance the built-in electric field near the tunneling junction involves creating a small depletion region, or pocket

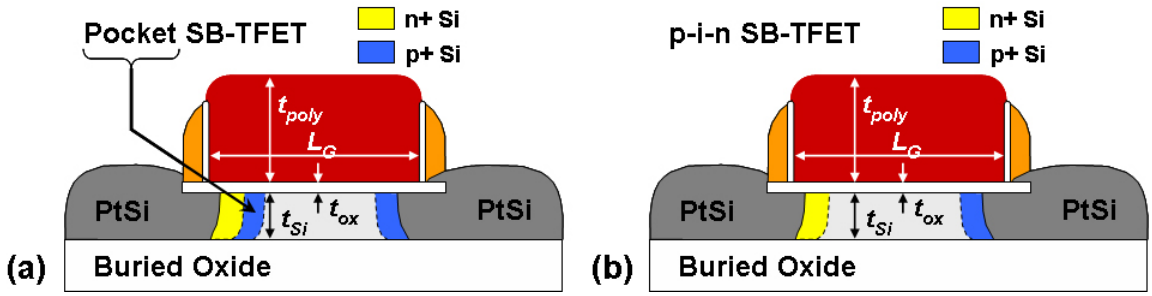

Figure 2.4: Schematic cross-section of a p-i-n TFET with SB junctions very near the source and drain. In (a), a pocket doping profile via ITS is introduced prior source ion implantation. In (b), a p-i-n doping profile via ITS is proposed as a control structure to examine the effect of the pocket formation via ITS. The ITS method is proposed to form the steep doping profiles necessary for a lower threshold for BTBT.

of opposite doping, near the source tunneling junction.[13] Fig. 2.4 shows a schematic cross-section of a SB based TFET with and without a doped pocket profile.

Figure 2.5 highlights key fabrication steps for the devices and shows a plan-view scanning electron micrograph of the fabricated device. The fabrication process for the SB-MOSFET is described in more detail in section 2.3. The PtSi formation was accomplished with the following RTA process parameters:

1. 20°C/min temperature ramp rate.
2. 300°C for 5 min.
3. 25°C/min temperature ramp rate.
4. 400°C for 5 min.
5. 25°C/min temperature ramp rate.
6. 425°C for 3 min. with O_2 flowing at 25 sccm.
7. Cool down to room temperature.

Out-diffusion of Si to the surface of the PtSi occurs during the final thermal steps. Flowing oxygen during the final step is necessary to form a protective SiO_x layer on top of the PtSi. This protective SiO_x layer prevents removal of the PtSi during a necessary soak in heated, dilute aqua regia to remove the remaining Pt that did not react with Si.[14]

Fabrication of p-Channel SB S/D FETs

A lightly p-type doped ($1{\cdot}10^{15}$ cm^{-3}) silicon-on-insulator (SOI) wafer was used as the starting substrate. Conventional planar processing steps were used to fabricate SB-FETs with a body

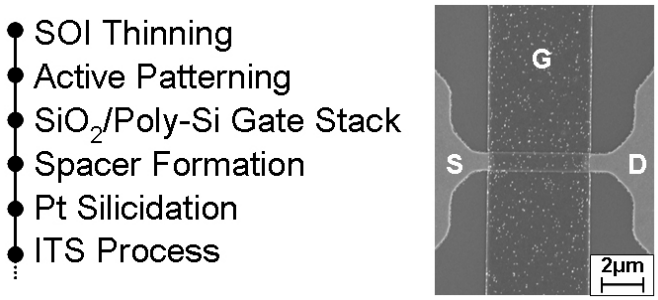

Figure 2.5: The sequence of key device fabrication process steps is shown on the left, and a plan-view scanning electron micrograph of a fabricated device is shown on the right with the source, gate, and drain labeled.

thickness $t_{\mathrm{Si}} = 25$ nm and a thermal gate-oxide thickness $t_{\mathrm{ox}} = 2.8$ nm. Note that the self-aligned PtSi formation step is performed prior to the introduction of any source or drain dopants. This silicide was formed by sputter deposition of a 17 nm-thick Pt layer followed by thermal annealing according to the steps listed in the previous section and similar to the process in [14]. Following silicidation, the n-type source and p-type drain regions were sequentially formed by ITS processes as follows. First,a drain-masked As^+ implantation process ($1 \cdot 10^{15}$ cm^{-2} at 10 keV) followed by a dopant segregation anneal in N_2 at 450 °C for 15 min was used to form the n-type source region. Second, a source-masked BF_2^+ implantation process ($1 \cdot 10^{15}$ cm^{-2} at 10 keV) followed by a dopant segregation anneal in N_2 at 500 °C for 5 min was used to form the p-type drain region. The peak doping concentration in the Si is primarily a function of the segregation anneal temperature [15] and Secondary Ion Mass Spectrometry (SIMS) analysis of test samples in [15] indicates that the peak As concentration at the PtSi-Si interface is between 10^{19} cm^{-3} and 10^{20} cm^{-3}.

Preliminary n-channel SB-MOSFETs were fabricated similar to reference [15] to verify the silicidation and ITS processing parameters. Experimental splits included pocket SB-TFETs with control p-i-n SB-TFETs along with temperature and time variations in the final RTA dopant segregation anneals.

2.4 Device Characterization and Discussion

Device characterization was performed using an HP4155C semiconductor parameter analyzer and a wafer-probe station with a temperature-controlled chuck. Long integration time was used so that the noise floor is approximately 10 fA.[3] While fabricated n-channel SB-MOSFETs showed decent transfer characteristics to verify the process flow design (similar to [15]), SB-MOSFETs modified as pocket TFETs did not yield promising results. A working hypothesis is as follows:

[3]Each data point represents an average of values measured over a period of 266 ms.

- Silicide formation inherently involves a Si supply from the SOI substrate and, thus, the active area of the device.
- When Si diffuses and reacts with Pt, vacancy sites are left behind in near the silicide/silicon interface.
- The RTA process following ITS uses a low temperature anneal and yields electronically active dopants near the interface.
- If dopant atoms are electronically active, then the dopant atoms occupy lattice sites.
- The formation of a pocket doping profile via a second ITS procedure with a subsequent dopant segregation necessarily involves the second impurity species displacing the first impurity species from lattice sites between the PtSi-Si interface and the pocket profile
- If the second impurity species does not displace an appreciable fraction of the first impurity species in a controlled manner, then the second species merely compensates the first species resulting in a poorly performing asymmetric SB-MOSFET.

Fig. 2.6 highlights typical transfer characteristics exhibited by pocket SB-TFETs co-fabricated with p-i-n modified SB-MOSFETs. The pocket transistors display ambipolar behavior. Similar to SB-MOSFET operation, carriers are likely injected over a thermal barrier due to a poorly defined pocket dopant profile.

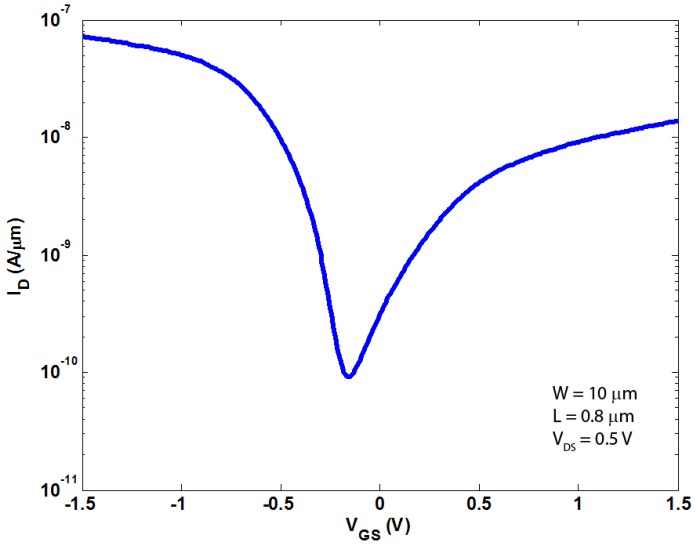

Figure 2.6: Transfer characteristic of a modified SB-MOSFET with a pocket doping profile near the source. Low $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ and poor SS are representative of a typical pocket TFETs fabricated in this manner.

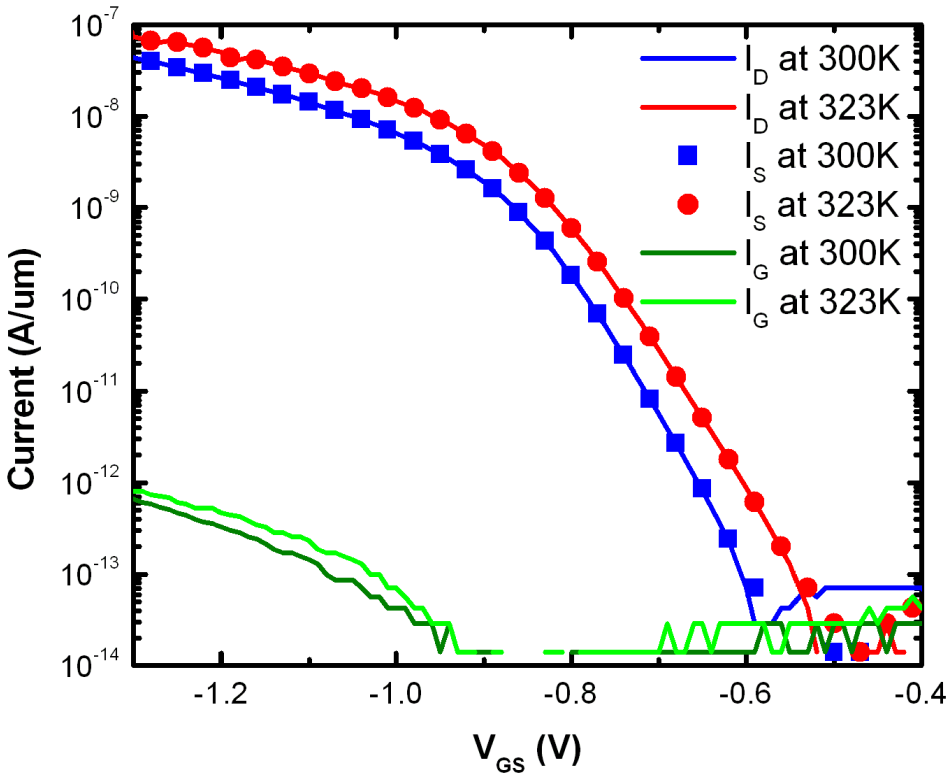

Figure 2.7: Initial measurements of the transfer characteristics of a p-channel enhanced SB-MOSFET (with channel length L_G = 5 μm and channel width W = 0.7 μm) at two temperatures. The gate voltage step is 10 mV and V_{DS} = -0.5 V. Solid symbols are used for the source current at every third gate voltage step.

Fig. 2.7 shows the initially measured transfer characteristics ($|I_D|$ vs. V_{GS}) for an interesting p-channel p-i-n SB-FET at two temperatures, 300 K and 323 K. A large negative gate voltage is required to invert the surface of the source region due to the n+ poly gate material and heavy source doping.[4] Note that a change in polarity for I_D is evident near V_{GS} = -0.6 V. This polarity change is likely due to reverse-bias diode leakage, which could account for the observed small opposite-polarity component (approximately 50 fA/μm) of drain current for V_{GS} > -0.6 V.

Subsequent, more detailed measurements of the transfer characteristics are shown in Fig. 2.8. The increased gate current is most likely due to cumulative stress over many measurements made using a long integration time. Despite this increase in the direct gate

[4] $|V_T|$ can be lowered to be close to 0 V by using a gate material with a larger work function (e.g. p+ poly-Si) and also by lowering the active source doping concentration (by adjusting the dopant segregation anneal conditions.

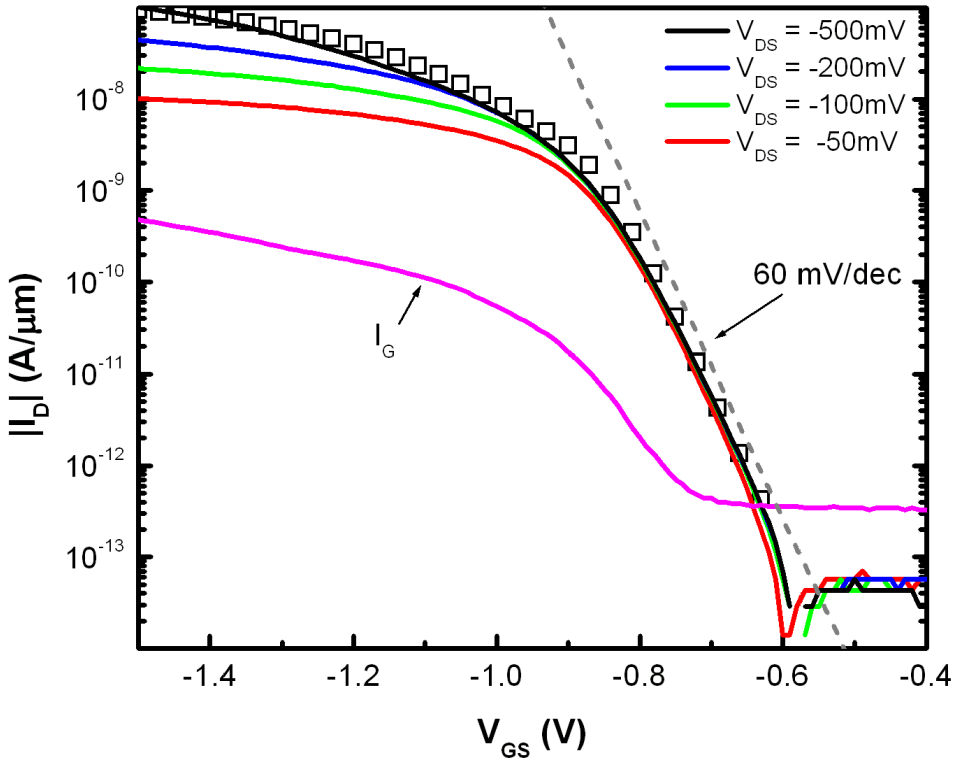

Figure 2.8: Measured transfer characteristics of a p-channel enhanced SB-MOSFET (with channel length $L_G = 5$ μm and channel width W = 0.7 μm) at 300K for various values of V_{DS}. The gate voltage step is 10 mV. The light-gray dashed line indicating 60 mV/dec sub-threshold swing is shown for reference. The solid magenta line is the measured gate current for V_{DS} = -0.5 V.

current, I_D is unchanged and continues to show steep switching behavior. Also of note, the opposite-polarity component of I_D is independent of both V_{GS} and V_{DS} (Figs. 2.7 and 2.8). The hollow square symbols in Fig. 2.8 correspond to a two-dimensional (2-D) device simulation of a SB-MOSFET,[16] discussed in more detail below. For a low operating voltage, this device exhibits a relatively high on/off current ratio: $I_{ON}/I_{OFF} = 1.17{\cdot}10^3$ for 0.2 V gate-voltage swing (from -0.63 V to -0.83 V) at V_{DS} = -0.2 V. Although this device exhibits relatively low drive current (even at high voltages), an appreciable I_{ON}/I_{OFF} is observed.

To elucidate the limiting mechanism of carrier transport in this device, E_A was extracted from the more detailed $|I_D|$-vs.-V_{GS} measurements made in the temperature range from 10 °C to 50 °C (V_{DS} = -0.5 V). E_A is only calculated for $|I_D| > |I_G|$, corresponding to $V_{GS} <$ -0.63 V, in order to avoid any artifacts due to the aforementioned small opposite-polarity

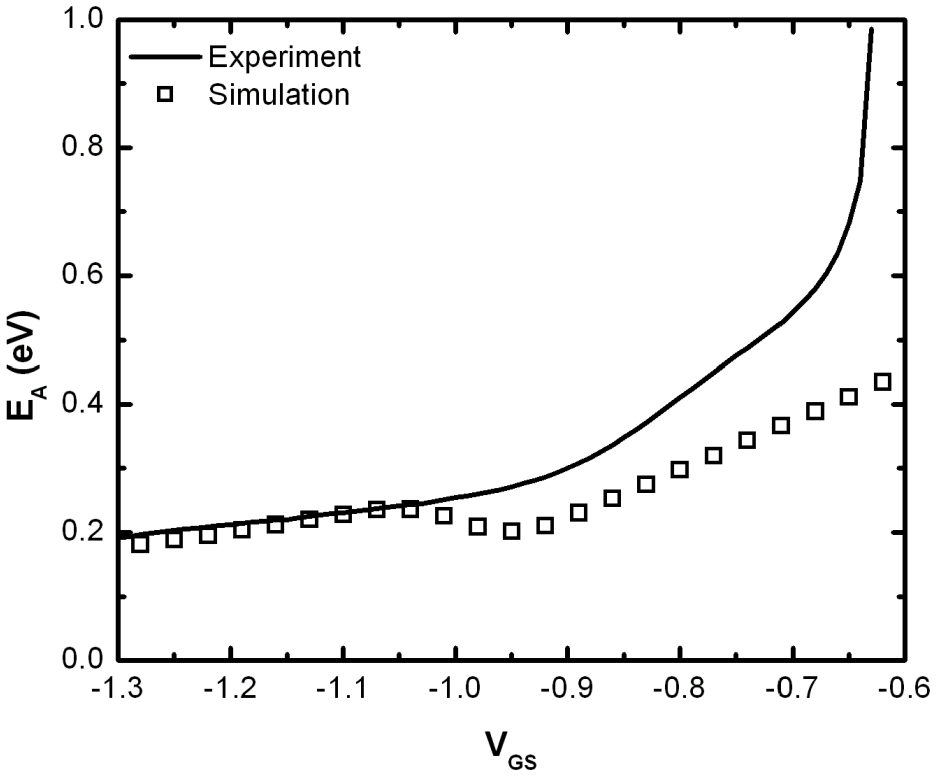

Figure 2.9: The inset shows the activation energy (E_A) extracted from measurements of log $|I_D|$ vs. 1/T, for T in the range from 10 °C to 50 °C. The open squares (shown for every third gate-voltage step) correspond to 2-D device simulation for V_{DS} = -0.5 V.

component of drain current. The dependence of E_A on V_{GS} (Fig. 2.9) indicates that the current-limiting mechanism changes with gate bias: at low biases ($|V_{GS}| < 0.7$ V) E_A is very large (which suggests that the current is limited by thermionic emission of holes either over a large barrier or from deep traps) and changes more rapidly than qV_{GS}. At moderate biases (0.7 V $< |V_{GS}| <$ 0.9 V), E_A decreases directly with increasing $|V_{GS}|$, as expected for a SB-MOSFET when the thermal barrier is greater than the SBH. At high biases ($|V_{GS}| > 0.9$ V), E_A becomes a weaker function of $|V_{GS}|$ as the current becomes limited by SB tunneling.

The rapid change in E_A near turn-on is most likely due to thermionic emission of holes from deep acceptor-like trap states into the valence band (see Fig. 2.10). These trap states are associated with metallic impurities and/or crystalline defects located close to the PtSi/Si interface, and holes can be supplied to them via tunneling from the PtSi, a process that turns on abruptly with increasing $|V_{GS}|$. As the gate overdrive increases to bring the Si into strong inversion, injection of holes into the channel from trap states is eventually superseded by

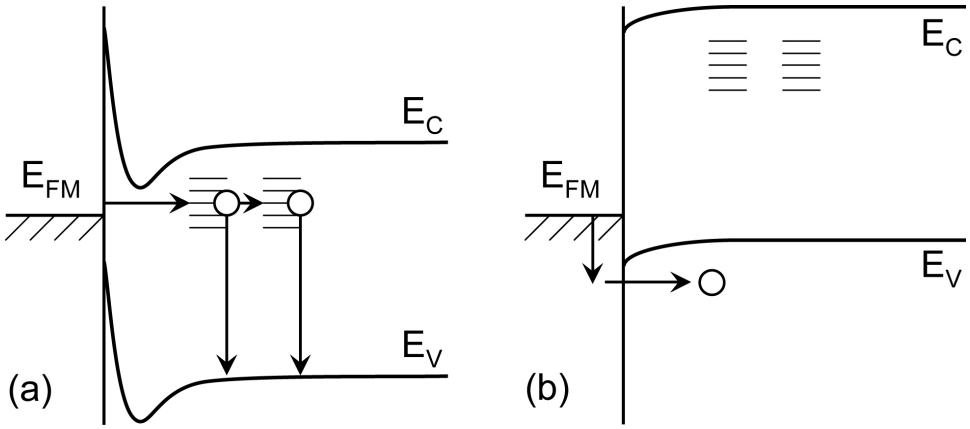

Figure 2.10: Schematic energy band diagrams illustrating two carrier injection mechanisms in an enhanced p-channel SB MOSFET. (a) Before the Si is inverted, holes tunnel to and can hop between electronic trap states which are distributed both in energy and space near the metal source. They then move to the Si valence band via thermionic emission. (b) When the Si is inverted, carrier injection is dominated by traditional thermionic emission over the Schottky barrier from the metal source.

thermionic emission of holes over the source side Schottky barrier.

The transfer characteristic in Fig. 2.8 was simulated using Synopsys Sentaurus Device TCAD software [16]. The design parameters for the simulated structure are the same as for the fabricated device: $L_G = 5$ μm, W = 0.7 μm, $t_{Si} = 25$ nm, $t_{ox} = 2.8$ nm, n-type source doping $N_D = 10^{19}$ cm^{-3}, and p-type drain doping $N_A = 10^{19}$ cm^{-3}. By employing a SB at the source and drain electrodes with an effective SBH of 0.33 eV and a reduced minority carrier lifetime (300 ns) to reflect the presence of traps, good agreement between simulated and measured characteristics (for V_{DS} = -0.5 V) is achieved for the gate voltage range beyond the steep switching regime. The difference between the simulated and experimental E_A (see Fig. 2.9) highlights the fact that the device simulator does not account for the effect of tunneling into trap states with a metal boundary condition. As an additional note, no BTBT model was invoked in the device simulator; thus the simulated device characteristic does not show sub-60mV/dec switching behavior.

The relatively slow temperature ramp rate described in the previous section (20 °C/min, see 2.3) and extended anneal time used for the silicidation process in this work likely resulted in a very extended spatial distribution of Pt atoms within the silicon, as has been observed for Ni silicidation [9, 17]. Pt impurities in n-type Si have been reported to behave as deep-level acceptor-like traps [18], supporting the explanation of the large activation energy at turn-on.

Consistent with the E_A measurements, $SS < 60$ mV/dec is seen at low current levels (below 10 pA/μm) corresponding to $|V_{GS}| < 0.7$ V, for multiple values of V_{DS} as well as at elevated temperature (Fig. 2.11). SS values are shown only for $|I_D| > |I_G|$, again to avoid any artifacts due to the aforementioned small opposite polarity component of drain current.

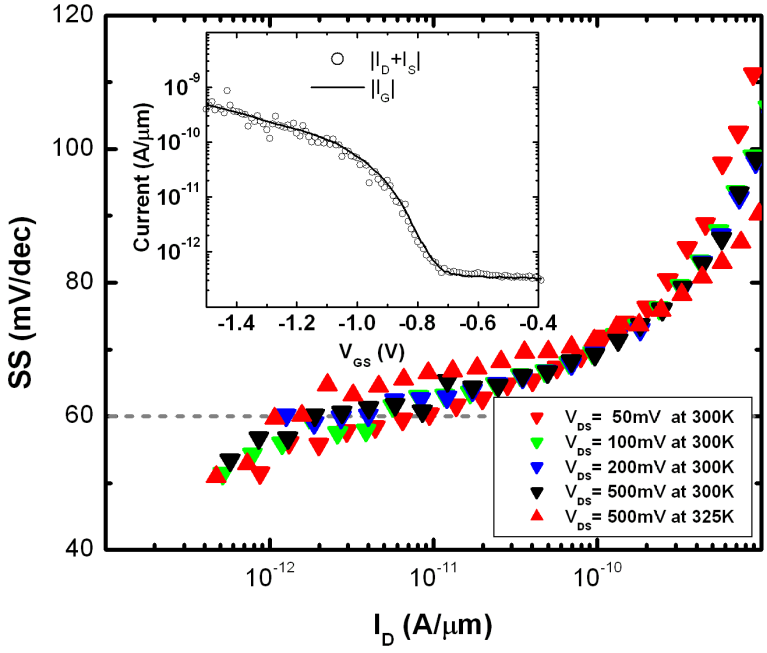

Figure 2.11: Sub-threshold swing (SS) vs. drain current, derived from the measurements in Fig. 2.8. The sub-60 mV/dec behavior seen below 5 pA/μm is only weakly dependent upon $V_{\rm DS}$ and temperature. The inset shows that no charging is occurring (to possibly account for the sub-60 mV/dec behavior) for $V_{\rm DS}$ = -0.5 V since $|I_{\rm D}+I_{\rm S}|$ matches $|I_{\rm G}|$ very well.

The inset of Fig. 2.11 shows that even after many measurements $I_{\rm G}$ remains relatively low and that all current is accounted for in the measurement (i.e., no charge build-up occurs to possibly account for the sub-60 mV/dec behavior). Also, $I_{\rm G}$ cannot possibly cause the observed sub-60 mV/dec SS since $I_{\rm G}$ changes gradually in the range $|V_{\rm GS}| < 0.7$ V. At higher current levels, SS increases with $I_{\rm D}$ as expected for a SB-MOSFET.

The transfer characteristics in Fig. 2.12 show that with back bias ($V_{\rm B}$) the threshold voltage (for Si inversion) is reduced with forward back biasing ($V_{\rm B} < 0$), and increased with reverse back biasing ($V_{\rm B} > 0$).[5] The dependence on $V_{\rm B}$ with increasing reverse back biasing decreases as the backside of the n-type source region becomes accumulated. Note that SS below 60 mV/dec is maintained with back biasing. The results in Fig. 2.13 further suggest that the hole tunneling process occurs in series with thermionic emission into the valence band (as illustrated in Fig. 2.10(a)), since $V_{\rm B}$ does not affect the range of $I_{\rm D}$ over which steep switching is observed.

[5]Similar to a SOI-MOSFET.

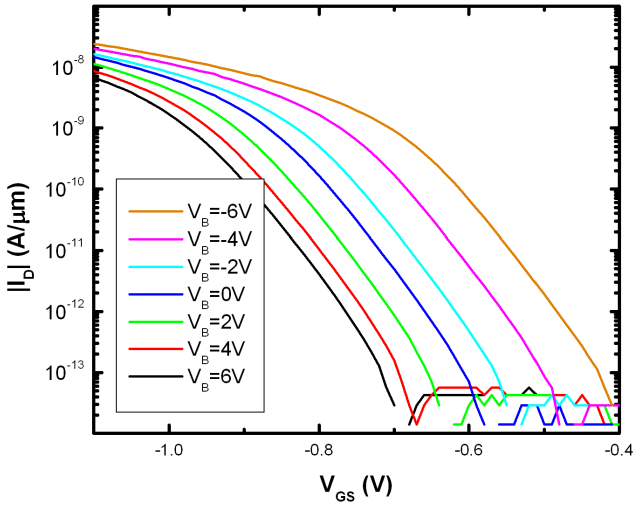

Figure 2.12: Transfer characteristics for various back biases.

Fig. 2.14 shows the measured output characteristics (I_D vs. V_{DS}) for the same device. Linear behavior is seen at low V_{DS}, which is consistent with a p+ doped drain [19, 20]. (The current is limited by carrier drift across the channel region (rather than by SB tunneling) at low drain biases [19].)

The on/off current ratios in Fig. 2.15 are derived from the transfer characteristics presented in Fig. 3, for each value of V_{DD}. The two reference lines in Fig. 2.15(a) represent SS = 75 mV/dec and 100 mV/dec, which span a range of typical values for conventional short-channel MOSFETs. It can be seen that the enhanced SB-MOSFET achieves a higher on/off current ratio than a conventional MOSFET for $V_{DD} < \sim$0.25 mV. In Fig. 2.15(b), the on/off current ratios at V_{DD} = 0.2 V are presented as a function of temperature. The enhanced SB-MOSFET shows a reduced temperature dependence compared to the lower limit of temperature dependence for a conventional MOSFET. This is consistent with a carrier injection mechanism that is not limited by thermionic emission. One example of a carrier injection mechanism not limited by thermionic emission would be band-to-band tunneling and a previous study of band-to-band tunneling transistors also shows a reduced dependence on temperature [21].

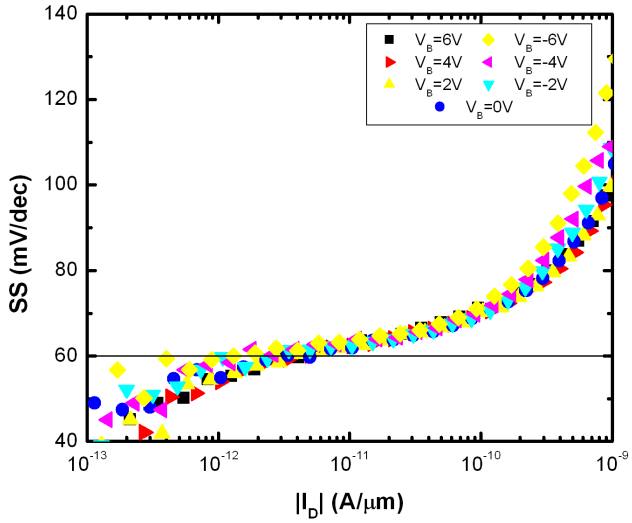

Figure 2.13: *SS* in the steep-switching regime shows little dependence on V_{B}, suggesting that electronic trap states near the silicide/silicon interface provide for an alternative hole injection process.

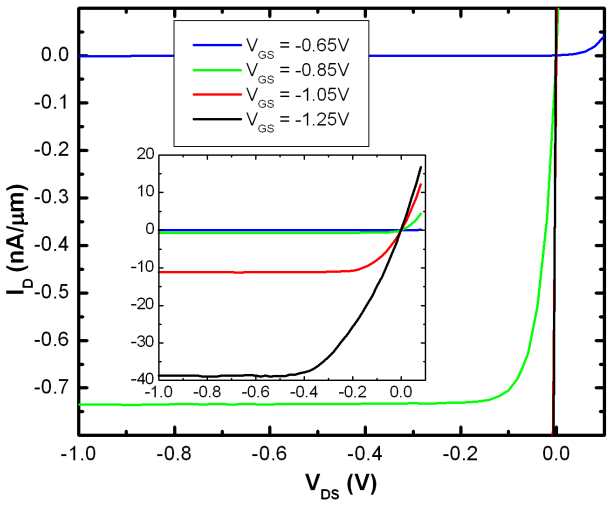

Figure 2.14: Measured output characteristics of the enhanced SB-MOSFET of Fig. 2.7. I_{D} is linear with V_{DS}, at low values of V_{DS}. The inset shows a zoomed-out view of the same plot, so that the curves for larger gate biases can be seen.

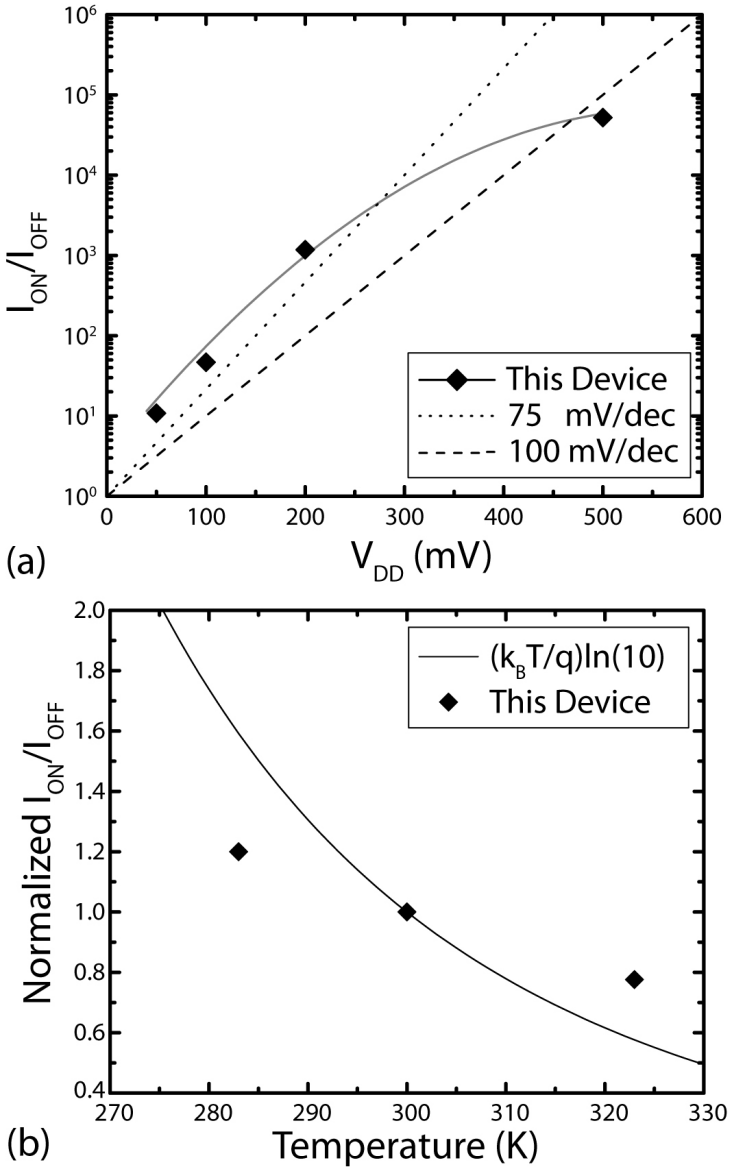

Figure 2.15: On/off current ratios for the reported device. I_{ON} is taken to be I_D at V_{GS} - $V_T = V_{DD}$ while I_{OFF} is taken to be I_D at $V_{GS} = V_T$. V_T is defined to be V_{GS} for $|I_D| = |I_G|$, in this case V_T = -0.63 V. In part (a), the on/off current ratio is plotted as a function of V_{DD} and with log-linear reference lines of 75 mV/dec and 100 mV/dec for comparison. A polynomial fit (grey curve) helps illustrate the low power on/off performance trend for this device. Part (b) shows the on/off current ratio at V_{DD} = 0.2 V as a function of temperature and a lower thermal limit reference line of a conventional MOSFET device calculated for a voltage range of 0.2 V.

2.5 Summary

The experimental results reported in this chapter indicate that the presence of trap states within a narrow, barrier-enhancing doped silicon region next to a Schottky source junction offers an interesting approach towards observing sub-60 mV/dec SS for MOSFET devices. Similar work has been presented in literature.[22–24] Silicide TFET devices presented in the literature perhaps utilize the same or similar operating mechanism, though each article typically explains the steep switching as a result of BTBT. In general, a exponential decay with a high concentration of metal impurity atoms in a transition zone in close proximity to a silicide-silicon interface may augment the electronic band structure such that the effective band gap for tunneling is reduced.

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Chapter 3

Engineered Electronic Trap States in Tunneling Diodes

3.1 Introduction

Well documented investigations of the role of traps in band-to-band tunneling (BTBT) typically focus on reverse biased or Esaki-like tunneling diode structures.[1–3] These structures offer simple device physics modeling for studying tunneling since there is only a single pn junction. A motivating factor for investigating trap states and BTBT is the unexplained observation of excess current in Esaki diodes.[4] At a low forward bias, an Esaki diode conducts current primarily via BTBT up to an applied bias corresponding to a peak bias (see Fig. 3.1). When the band overlap reaches zero, BTBT should cease and the current should diminish to the normal forward bias diode current (approximately given by the diode equation). However, an excess current is observed due to tunneling into and out of electronic trap states located within the band gap as well as from states located within the band edge tails.[4]

Figure 1 in [4] schematically presents various trap assisted tunneling routes as a basis for modeling the excess current. Excess current is often attributed to intrinsic defects in crystalline silicon and a deliberate introduction of crystal imperfections by radiation bombardment correlates with a dramatic increase in the excess current (see Figure 4 in [4]).

Early theoretical and experimental investigations into BTBT laid the foundation for understanding the role of tunneling in leakage for scaled down silicon MOSFET devices.[5][1] Modeling work by Hurkx and later Schenk led to improvements in the BTBT models incorporated into semiconductor device simulations.[3, 5, 6] Qualitatively, when these models are employed in a device simulation, the BTBT generation rate is calculated at each grid point. This generation rate is heavily dependent on the value of the electric field at that grid point. Other factors, such as minority carrier lifetimes and the presence of trap states,

[1]For example, increasing the peak doping concentrations or utilizing steep doping profiles while scaling down dimensions

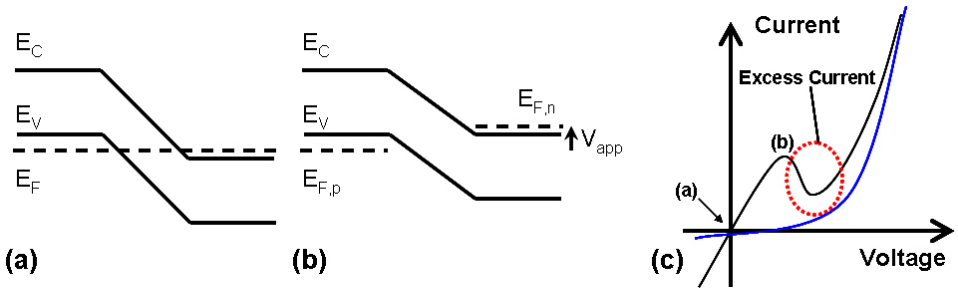

Figure 3.1: An Esaki diode in thermal equilibrium (a). The heavily doped p and n quasi-neutral regions cause band overlap between the valence and conduction bands in the off state. (b) A small forward bias is applied such that the band overlap is zero. (c) Qualitative I-V characteristics for a typical Esaki diode (black line) show excess current greater than the forward bias diode current (blue line) when the applied voltage exceeds the bias point labeled as (b). The bias points for parts (a) and (b) are labeled in part (c).

are incorporated into calibration parameters for improvements to the model. While these models work well in predicting the tunneling rate in and around a reverse biased pn junction, the models do not account for any spatially dependent term in the calculation of the BTBT generation rate.

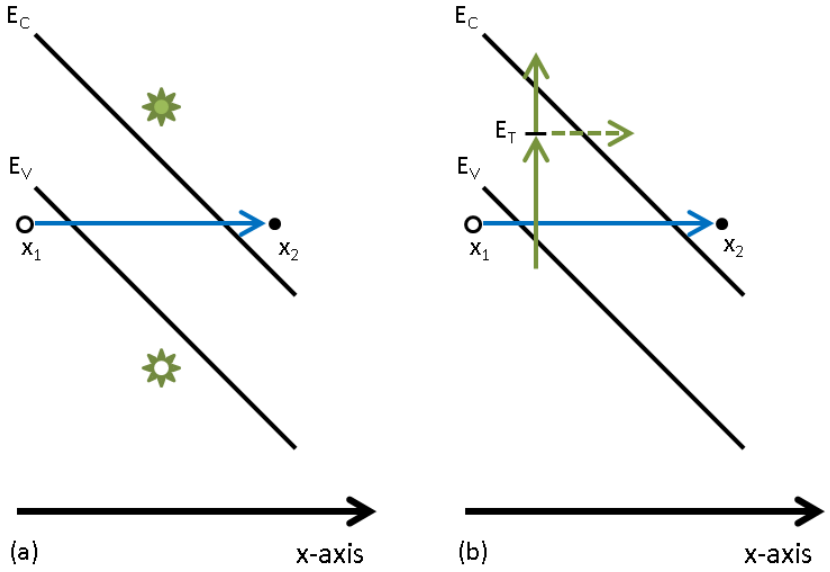

Figure 3.2: In (a), a BTBT generation rate is calculated with (blue arrow) and without (green dots) a spatial dependence for the tunneling model. Part (b) illustrates both thermal excitation to and from traps (solid green arrow) and an additional path for carriers exiting from traps, field emission tunneling (dashed green arrow). Field emission from the trap is modified in a local tunneling model by calibration parameters.

A spatial dependence is necessary for accurate device structure modeling when the band-

to-band overlap occurs over an appreciable distance. Without a spatially dependent term in the tunneling model, tunneling from an occupied state to an unoccupied state is approximated by a tunneling generation rate calculated at a single point. Additionally, the role of traps is relegated to generation and recombination models near the grid point when the tunneling rate is calculated. Figure 3.2 highlights the difference between a local and nonlocal tunneling model. These models are approximations and therefore insufficient for TFET design and simulation where the role of traps in BTBT is under investigation.

The Synopsys TCAD Sentaurus simulation engine includes a robust dynamic nonlocal BTBT tunneling model which greatly improves the accuracy of TFET simulation and design work. The dynamic nonlocal trap-assisted tunneling model, however, does not explicitly model tunneling into and out of electronic trap states in conjunction with the BTBT tunneling model.[7] Rather, this model incorporates previous trap-assisted tunneling models (e.g, Hurkx and Schenk) with a modified electric field calculated by the maximum of the gradient of the potential profile. This highlights a shortcoming of most tunneling models to accurately calculate discrete tunneling into and out of electronic trap states.

The lack of a robust numerical tunneling model for traps necessitates the use of experimental methods to further investigate the role of traps in BTBT. A powerful analysis for investigating electronic trap state properties is to calculate the activation energy, E_{A}, from temperature dependent current-voltage measurements (see 2.9). Calculation of the activation energy is possible with an Arrhenius analysis [8] and calculating E_{A} as a function of the applied bias assists in determining how trap states affect the normal operation of a tunneling device.

For an Arrhenius analysis, the data is presumed to have an exponential dependence related to the thermal energy:

$$I \propto A \cdot \exp\left(\frac{-E_{\mathrm{A}}}{k_{\mathrm{B}}T}\right). \tag{3.1}$$

A is an exponential prefactor and $k_{\mathrm{B}}T$ is the thermal energy. Taking the natural logarithm of both sides yields the slope intercept form $y = m \cdot x + b$ where the slope is $\frac{-E_{\mathrm{A}}}{k_{\mathrm{B}}}$ and the dependent variable is $\frac{1}{T}$.

$$\ln(I) \propto \ln(A) - \frac{E_{\mathrm{A}}}{k_{\mathrm{B}}} \cdot \frac{1}{T}, \tag{3.2}$$

The slope of a best fit line of the natural logarithm of the temperature dependent data versus $\frac{1}{T}$ allows the straight forward calculation of E_{A}. For electronic trap states, determining E_{A} helps identify the energy level of the trap state as well as the dominant current injection method.

3.2 Impurity Selection for Electronic Trap State

Fig. 3.3 shows four possible routes for carriers to enter and exit an electronic trap state located within the band gap. By lowering the temperature of the semiconductor, carriers

exhibit a lower thermal energy and so reduces the probability of thermal excitation into and out of the trap. Ideally, a low enough temperature will quench the trap assisted thermal excitation process. As suggested in the example in Fig. 3.3, this leads to a greater fractional tunneling component in the generation rate of carriers in the conduction band. An electronic trap state energy level, E_T, appreciably far from both the valence and conduction bands can assist in isolating the role of tunneling into and out of trap states in a dynamically biased semiconductor junction. E_T sufficiently far from both band edges at a low temperature should enhance the tunneling probability into and out of the trap as the thermal excitation probability is decreased. Heterodiodes were fabricated to explore the role of traps states in close proximity to a BTBT junction.

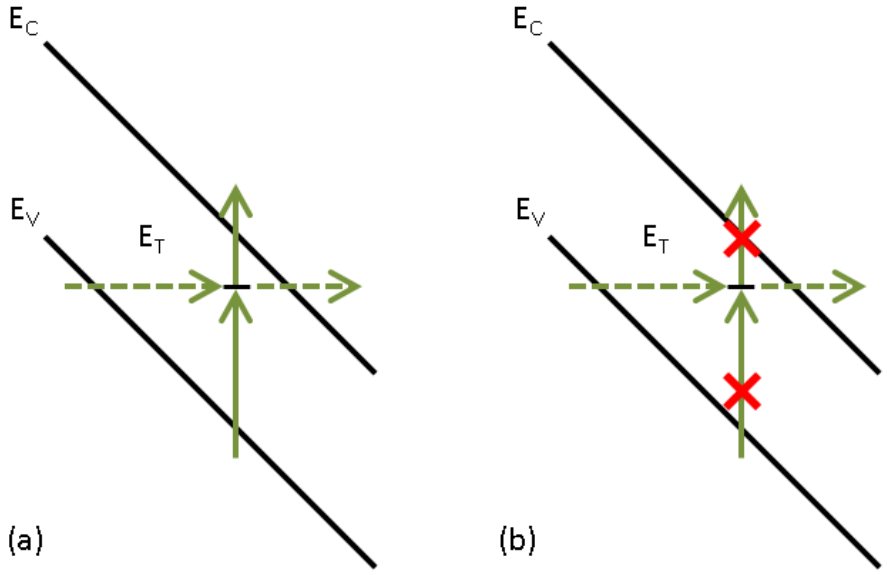

Figure 3.3: Four routes are shown in (a) for carriers entering and exiting a trap state and energy E_T. Thermal excitation is shown in solid green arrows while tunneling into and out of the trap is shown with dashed green arrows. (b) Lowering the temperature of the measurement can reduce the thermal excitation components.

A dated but comprehensive chart of electronic trap state types and energy levels appears in section 1.4.2 of [8]. From the chart in [8], chromium is immediately identified as a single level trap close to the mid-gap of Si ($E_C - E_T = 0.41\,\text{eV}$). However, very few reports exist detailing the electronic properties of chromium in Si. A more detailed search of the literature suggests erbium (Er) as another likely candidate for engineered electronic trap states.[9–12] A majority of the literature regarding Er impurities in Si focuses on the opto-electronic properties for the purpose of integrated Si based photonics. Er typically exhibits a trap state energy level between the mid-gap of Si and the conduction band edge. A trap located close to the mid-gap of Si is advantageous since a larger energy is necessary to excite a carrier either to or from a trap.

Various reports identify multiple energy levels for Er in Si ranging from $0.18\,\mathrm{eV} < E_\mathrm{C} - E_\mathrm{T} < 0.6\,\mathrm{eV}$ with mid gap trap states seemingly more likely to occur in.[9–11, 13] The concentration of Er atoms, the background doping of the Si, as well as the proximity of oxygen atoms and crystalline defects in the Si all influence the electronic trap state properties. With this in mind, reference [12] notes that the optically active Er concentration is limited to approximately $3 \cdot 10^{17}\,\mathrm{cm}^{-3}$. The work reported here targets an Er concentration close to $10^{17}\,\mathrm{cm}^{-3}$ so as to avoid adverse effects of a high concentration of impurities, some of which may not be fully electronically active.

3.3 Experimental Design Goals

To explore the role of traps in BTBT, Er was purposely introduced into heterodiode devices, schematically depicted in Fig. 3.4. On-wafer splits were employed to provide control samples for co-fabricated devices. The device structures consist of either a p+-i-n+ or p+/n+ heterodiode with p+ poly-germanium (Ge) selectively deposited on the Si surface of an silicon-on-insulator (SOI) wafer. For the Er^+ on-wafer split, the top half of the wafer remained in the original state while the bottom half was implanted with Er^+ ions with a dose of $7 \cdot 10^{11}$ cm^{-2} and an implant energy of 10 keV. Ge was chosen for the heterostructure material since Ge has a lower band gap than Si and poly-crystalline Ge can be selectively deposited onto Si using low pressure chemical vapor deposition (LPCVD). Fig. 3.4 shows four experimental splits incorporated into the top and bottom half of the wafer for a total of eight splits.

TRIM simulations using SRIM software were used to predict a peak concentration for the device structure.[14] Low temperature oxide (LTO) deposited by LPCVD was used to protect the surface of the structure during ion implantation and can be easily removed with a hydrofluoric (HF) acid wet etch prior to further processing. Fig. 3.5 shows the results of numerical calculations performed by SRIM (using a TRIM calculation) of Er^+ ions implanted into a test structure. Nearly all of the Er^+ ions remain within the first 15nm (150 angstroms) of Si for a 10 keV energy implant through a 10nm thick LTO film. Ideally, engineering the trap profile to be close to the Si surface will promote a trap assisted BTBT (TA-BTBT) process since tunneling junction is designed to coincide with the heterojunction.

Sample preparation involved typical planar processing techniques with the following key fabrication steps listed below:

- Active area definition.
- Er^+ ion implantation for the bottom half of wafer.

  Energy = 10 keV, Dose = $7{\cdot}10^{11}$ cm^{-2}
- As^+ ion implantation.

  Energy = 10 keV, Dose = 10^{15} cm^{-2}

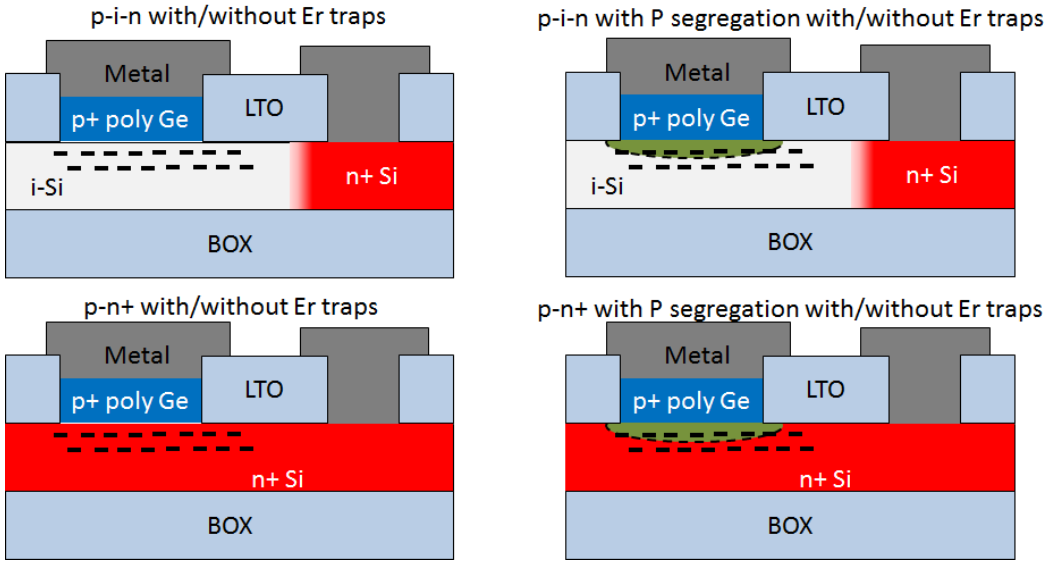

Figure 3.4: Four device structures are shown, each co-fabricated on the same wafer. Each of the four splits was fabricated with and without implanted Er^+ for a total of eight splits. Trap states are represented in the diagrams as narrow hyphenated marks.

Split for a blanket As^+ and masked As^+. (See Fig. 3.4.)

Solid phase epitaxy regrowth (SPER) anneal at 550°C for 4 hours.

Rapid thermal anneal (RTA) at 1050°C for 10 seconds.

- Selective p+ poly-Ge deposition with *in situ* doping near $3{\cdot}10^{19}$ cm^{-3}.

  LPCVD 425°C with 3:1 ratio of BCl_3:GeH_4 gas flow.

- P^+ ion implantation split.

  P segregation anneal for 1 hour at 700°C.

The intention of the phosphorus implant and segregation anneal split is to test a phosphorus "pile up" at the poly-Ge/Si interface. Such a pile up could induce a deeper n-type well as a test for cutting off BTBT at energies from the valley of the well to $E_{C,Si}$ beyond the well. Fig. 3.6 qualitatively highlights this proposal for cutting off the BTBT near the tunneling heterojunction.

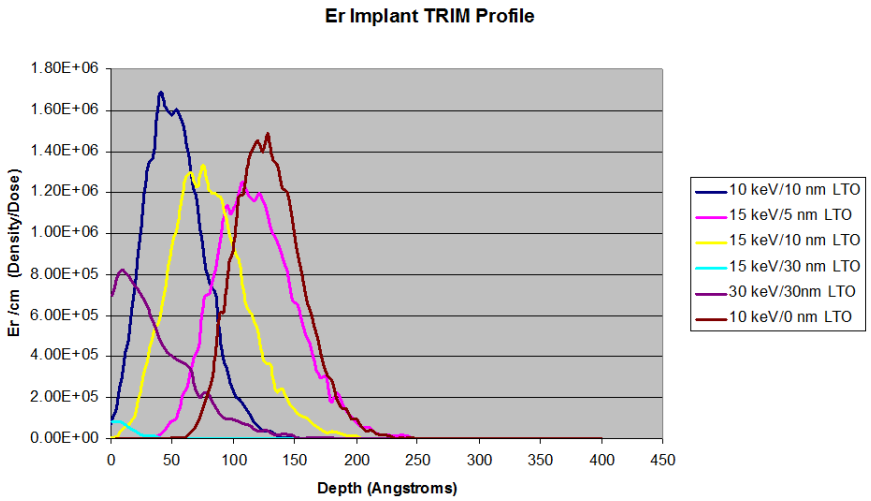

Figure 3.5: Erbium ion implantation numerical calculations performed by SRIM software. Various combinations of the Er^+ implant energy and LTO film thickness are displayed. The curves are plotted from the silicon substrate surface and implanted concentrations normalized to the dose.

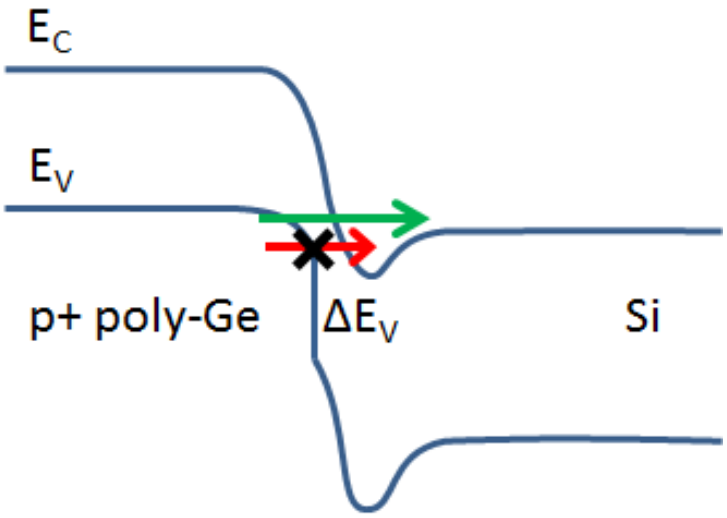

Figure 3.6: As proposed, an n-type well near the tunneling heterojunction should cut off some BTBT paths. The majority of the band gap difference between Ge and Si is represented by ΔE_V.

3.4 Diode I-V Characteristics and Temperature Dependence

Fabricated diodes were characterized using either a HP4155C or an Agilent B1500A semiconductor parameter analyzer. Initial measurements of all of the experimental splits showed some diodes with rectifying behavior and others with resistive behavior. Table 3.1 summarizes the experimental split yield. Diode I-V curves were measured with an applied bias on the p+ poly-Ge contact with a 5 mV step size at medium to long integration time for lower noise and low current accuracy. Temperature dependent measurements were carried out on rectifying diodes from 300K to as low as 150K and used to determine the activation energy as a function of applied bias. For each temperature dependent measurement, the samples were held at the target temperature for at least 45 minutes in order to achieve a stable thermal equilibrium in the measurement probe station.

Reasons explaining why only some of the experimental splits did not yield rectifying behavior remains unknown. Unfortunately, an interesting rectifying split for p+/n+ heterodiodes without phosphorus and with Er has no control device (i.e., a similar device without Er) for a more direct comparison to isolate the role of Er trap states in a tunneling junction. One hypothesis is that the presence of Er atoms mitigated some of the damage caused by the blanket As^+ implant. Testing this hypothesis was beyond the scope of this work. Alternative process flows to enhance the yield of a similar experiment could include a thicker SOI layer for improved recrystallisation during the SPER anneal or a lower dose As^+ implant. The rest of this section focuses on the tunneling diode results with some comparisons to control p-i-n diodes as well as simulated diode behavior when appropriate.

Blanket As^+	P^+	Er^+	Rectifying?
0	0	0	Yes
0	1	0	Yes
0	0	1	Yes
0	1	1	Yes
1	0	0	No
1	1	0	No
1	0	1	Yes
1	1	1	No

Table 3.1: Experimental heterodiode splits and rectifying device yield.

Fig. 3.7 shows temperature dependent current-voltage (I-V) characteristics of fabricated p-i-n heterodiodes with and without Er trap states. Heterodiode p-i-n devices fabricated with implanted Er atoms showed a slightly greater dependence on temperature at small reverse bias. This can be observed in the slightly larger spread in reverse bias saturation

current.[2] Additionally, comparing the first derivatives of the I-V characteristics, Fig. 3.8, shows that p-i-n heterodiodes with Er have a smaller slope across a range of reverse bias. That is, the reverse bias diode saturation current is more than likely dominated by the Er trap states purposely introduced into the Si substrate.

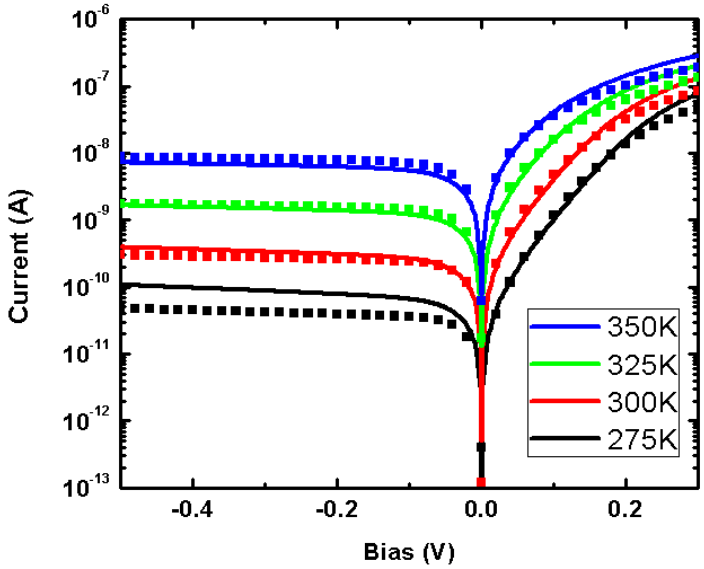

Figure 3.7: I-V characteristics for a p-i-n control heterodiode (solid lines) and a p-i-n heterodiode with Er trap states (symbols) over a temperature range of 275K to 350K. For a small reverse bias, the I-V characteristics for the heterodiodes with Er traps states show a slightly greater temperature dependence than for the control device.

E_A was calculated using an Arrhenius analysis described in section 3.1. Preliminary calculations for E_A using the I-V curves in Fig. 3.7 are shown in Fig. 3.9. E_A for the p-i-n heterodiode with Er trap states appears slightly greater (0.6 eV) than the p-i-n control diode (0.5 eV). Presumably, the majority of carrier generation in a p-i-n heterodiode control structure occurs in the depleted intrinsic Si region. With an energy very close to the middle of the band gap (∼0.5 eV), this most likely corresponds to inherent point defects in the intrinsic Si. When Er traps are present, the traps plays a greater role in the generation and recombination of carriers and as such an Er trap level dominates the activation energy over a range of reverse bias. An Er in Si trap state energy level of 0.6 eV is in good agreement with a trap energy value reported in literature provided this trap level is the dominant generation-recombination center in comparison with other known trap levels of Er in Si.[9, 10]

[2]Both devices represented in Fig. 3.7 are fabricated to the same physical dimensions.

TCAD simulations using Synopsys Sentaurus [7] were employed to verify that E_A corresponds to the trap energy level of the Er impurity atoms. For simplicity in the simulation, crystalline Ge material parameters were used for the poly-Ge material. Fig. 3.9 shows the calculated E_A for two experimental p-i-n diodes as well as the activation energies from simulated p-i-n heterodiodes with and without traps. Each simulation uses a dynamic nonlocal BTBT model as well as a recombination-generation based dynamic nonlocal trap assisted tunneling model. No other models for the physics of trap states in a semiconductor were used. The simulated trap energy level was set such that $E_C - E_T = E_A$ calculated from the measured I-V characteristics. Trap states were included in the simulation at a concentration chosen to be $N_T = 5{\cdot}10^{17}$ cm^{-3}. This N_T yields an E_A in close agreement with experimental results for a p-i-n heterodiode with Er. Simulation results with $N_T = 0$ cm^{-3} show a much higher activation energy, suggesting that the simulation software does not correctly account for intrinsic electronic trap states without use of additional generation-recombination models.

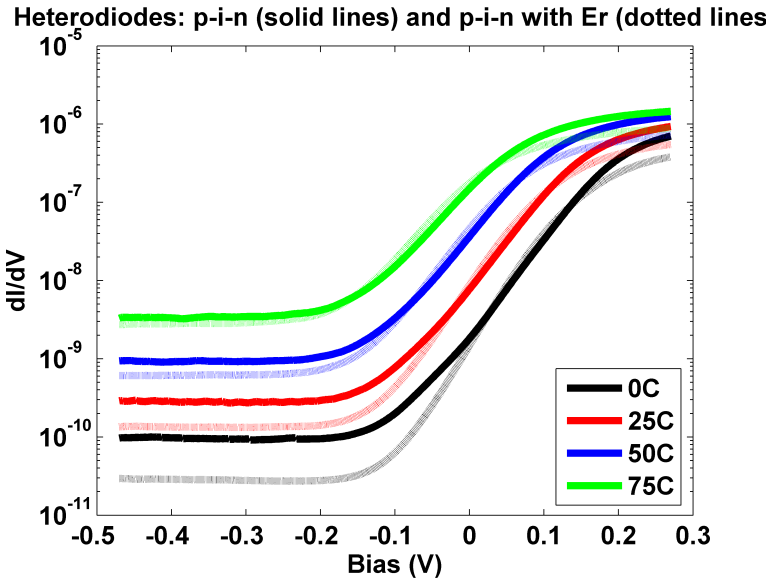

Figure 3.8: The first derivative of the I-V characteristics in Fig. 3.7 are presented for the p-i-n heterodiode control (solid lines) and p-i-n heterodiodes with Er trap states (dotted lines). The slopes for the heterodiodes with Er trap states remain less than the corresponding slopes for the heterodiode controls.

While the p+/n+ heterodiode with Er traps show tunneling behavior in reverse bias and rectifying behavior in forward bias, the control devices for this experimental split do not show any rectifying behavior. While the simulation software does not explicitly account for tunneling into and out of a trap state, the previous verification of the behavior of Er trap states as generation-recombination centers serves to substantiate at least a nominally correct incorporation of trap states in a simulation. Ge/Si (p+/n+) structures with and without trap states and with no intrinsic region were simulated for I-V characteristics at temperatures down to 175K.

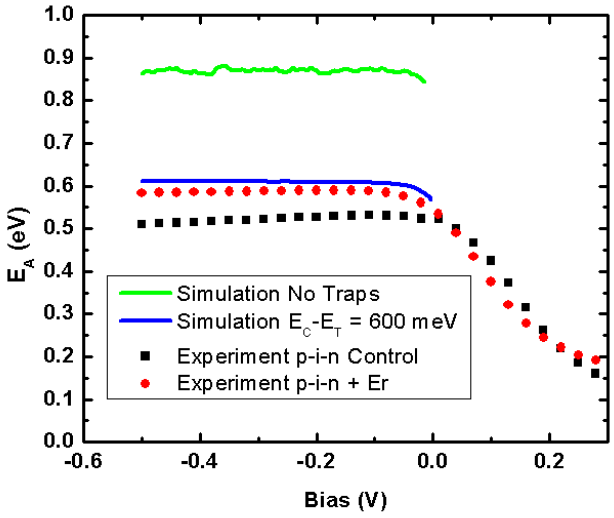

Figure 3.9: E_A calculated from experimental results for a p-i-n control heterodiode and a p-i-n heterodiode with Er trap states in Si (symbols). E_A calculated from simulated temperature dependent heterodiode I-V curves (solid lines) shows some agreement with the incorporation of Er in Si. The simulation result for no traps appears at higher energy and is noisy due to the numerical errors in the simulator at very low current. The symbols are plotted with fewer data points for clarity.

Fabricated p+/n+ heterodiode devices with Er trap states show tunneling behavior in reverse bias (see Fig. 3.10), however, no peak-to-valley current ratio or negative differential resistance (indicative of Esaki tunneling behavior [8, 15]) is evident at any forward bias despite the expected Esaki band alignment at zero bias (see Fig. 3.11). Fig. 3.12 shows the calculated E_A for the experimental I-V curves presented in Fig. 3.10. E_A for the p+/n+ tunnel diode with Er trap states remains very low with applied reverse bias - E_A is 55 meV at very small reverse bias and decreases with increasing reverse bias. Since there is no negative differential resistance at small forward bias, the conduction and valence bands may not be overlapping in energy at zero bias. Since the traps lie within the Si, further application of a reverse can lower the trap state energy levels below the energy of tunneling carriers. This could explain why the experimentally determined E_A decreases with reverse back bias towards the lower tunneling energy for a reverse biased p+/n+ heterodiode.

Simulated temperature dependent I-V characteristics for a p+/n+ heterodiode with no trap states shows E_A trending to 0 eV at zero bias. As noted for Fig. 3.11, band overlap at zero bias is expected for the simulated structure where the simulated physical parameters are in close agreement to experimental values (either predicted or measured), so E_A trending to 0 eV at zero bias suggests that the simulation software assumes little to no activation energy necessary for BTBT in an Esaki tunneling diode. E_A calculated from simulated characteristics increases with increasing reverse bias (Fig. 3.12) though still remains low throughout

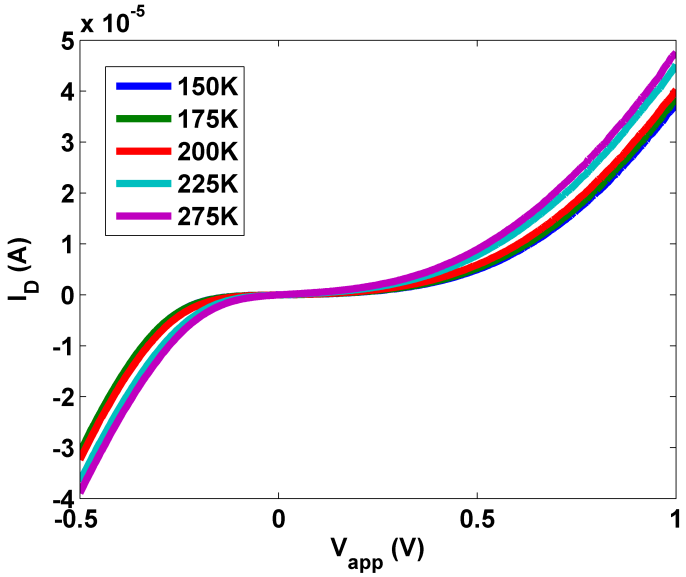

Figure 3.10: Typical tunneling diode characteristics for fabricated p+/n+ heterodiodes measured across various temperatures. Not all temperatures are displayed for clarity. Note that there is no negative differential resistance characteristic of an Esaki tunneling diode.

the same reverse bias range. Unfortunately, simulated p+/n+ heterodiode structures with trap states show little to no change in E_A when compared to simulated results for a p+/n+ heterodiode with no trap states.

Other simulation studies (not presented here) suggest that the simulation software does not couple the dynamic nonlocal trap assisted tunneling model with the dynamic nonlocal BTBT model (i.e., the models appear to be non-interacting).[3] While tunneling is a majority carrier process,[8] the close proximity of a large concentration of trap states to a tunneling junction is expected to alter the tunneling dynamics. This effect is likely not accurately captured in the simulation software.

[3]For example, a simulated Esaki-like p+/n+ heterodiode without the dynamic nonlocal BTBT model but with the dynamic nonlocal trap assisted tunneling model shows no indications of BTBT, with or without traps.

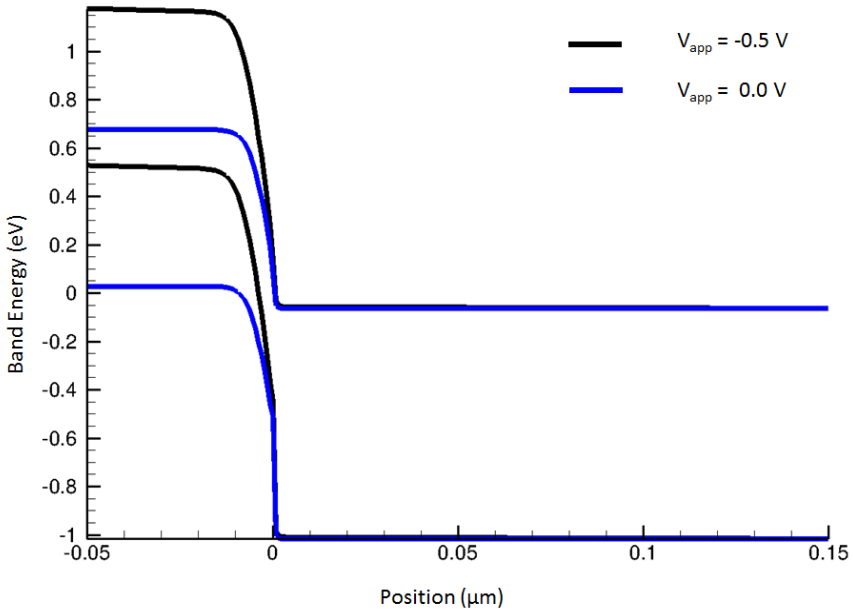

Figure 3.11: Simulated band diagrams for E_C and E_V for a poly-Ge/Si p+/n+ heterodiode at zero applied bias and a reverse bias of V_{app} = -0.5 V. The alignment at zero bias suggests Esaki tunneling diode behavior should be observable.

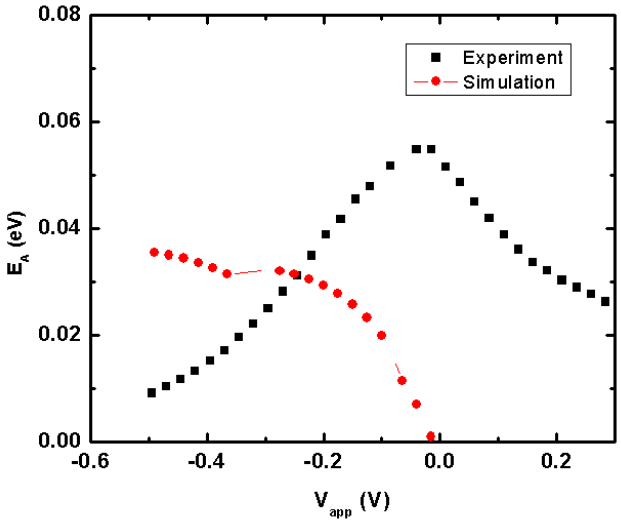

Figure 3.12: The calculated E_A from fabricated p+/n+ tunnel diodes with Er trap states shows a very low activation energy from small reverse bias to V_{app} = -0.5 V. Simulated I-V characteristics for a p+/n+ heterodiode without trap states also result in a low E_A for -0.5 V $\leq V_{app} \leq$ 0 V.

3.5 Conclusion

Failed experimental splits for the fabrication of p+ poly-Ge on SOI heterodiodes made it challenging to isolate the effects of Er impurity atoms in close proximity to BTBT junctions. Experimental splits involving phosphorus segregation from the poly-Ge either did not exhibit rectifying behavior or did not yield any significant variation in operation of the device. Results for p-i-n heterodiode structures suggest that engineering an Er trap density in the intrinsic Si region can change the activation energy in reverse bias towards an expected trap energy level of Er in Si.[9, 10]

When possible, TCAD simulations using Synopsys Sentaurus commercial software were employed to validate and explore the role of traps near a tunneling junction. While the dynamic nonlocal models for BTBT and trap assisted tunneling have been independently verified,[7] the models together were insufficient in explaining the role of Er trap states in a p+/n+ heterodiode tunneling junction.

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Chapter 4

Erbium Trap Assisted TFET

4.1 Introduction

Drawing upon previous results reported in chapters 2 and 3, the experiment reported here was co-designed with the heterodiode work to explore the broader role of traps in a TFET. To investigate how trap states alter the activation energy of band-to-band tunneling (BTBT) in a transistor, planar SOI TFETs were fabricated with and without ion implanted erbium (Er) intended to form electronic trap states within the band gap. The overall design (depicted schematically in Fig. 4.1) calls for the traps to be located in close proximity to the tunneling junction as well as preferentially between the mid-gap of Si and the conduction band edge of Si.

Er impurity atoms were again chosen to form the electronic trap states with a target concentration near 10^{17} cm^{-3}. Er ions were implanted prior to the silicon nitride spacer

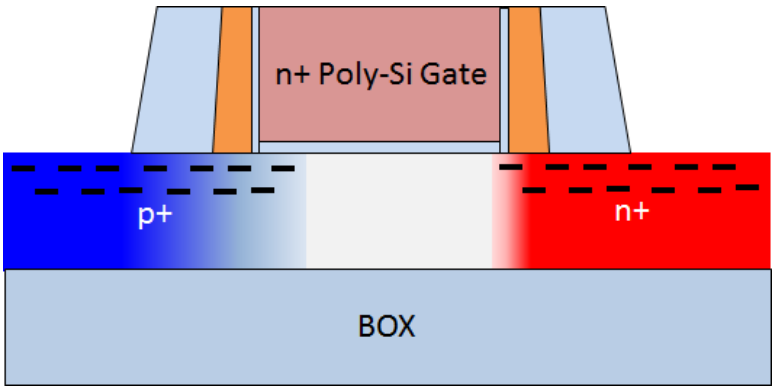

Figure 4.1: Traps are located in close proximity to the tunneling junction which is designed to be near the gate edge of the SOI TFET. A self aligned Er^+ ion implant avoids the introduction of trap states in the channel region. The spacers are comprised of thermally grown oxide on poly-Si (light blue), a silicon nitride thin film (orange), and a low temperature oxide (light blue).

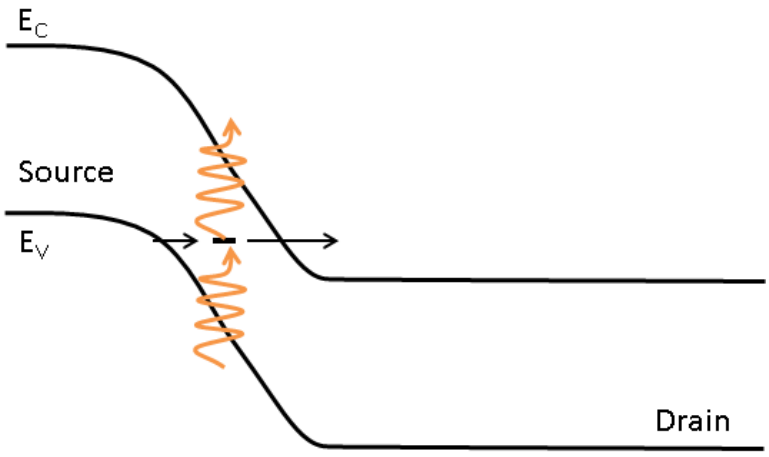

Figure 4.2: Er electronic trap states in crystalline Si should be located between $E_C - E_T = 0.18\,\text{eV}$ and $E_C - E_T = 0.6\,\text{eV}$. The orange arrows indicate thermal excitation routes while the black arrows suggest tunneling paths available to carriers in close proximity to the traps.

formation so that the traps are well aligned with the gate edge near the source. Fig. 4.2 shows a schematic energy band diagram with a trap state located near the tunneling junction. Figs. 4.1 and 4.2 represent an n-channel Er-based trap-assisted TFET (Er-TATFET) design with hash marks indicating the qualitative position of the traps.

Low temperature measurements were again employed in order to reduce the thermal excitation to and from the trap states (see Fig. 3.3). Careful analysis of the temperature dependence yields the activation energy (E_A) as a function of the applied gate bias for the Er-TATFETs.

4.2 Experimental Design Goals

An on-wafer experimental split allows for the co-fabrication of experimental Er-TATFETs and control p-i-n SOI TFETs. Using photolithography, one half of the wafer is masked during the Er^+ ion implantation so that p-i-n TFETs are fabricated without any engineered electronic trap states. Key fabrication steps include:

- Active area definition, thermal oxide for gate dielectric, and gate stack formation.

  $t_{ox} = 2.81$ nm.

- Poly-Si gate definition and gate sidewall re-oxidation.

- Er^+ ion implantation

  Energy = 10 keV, Dose = $7{\cdot}10^{11}$ cm^{-2}.

- Silicon nitride spacer formation.
- TFET source masked As^+ ion implantation: Energy = 20 keV, Dose = $1.5{\cdot}10^{15}$ cm^{-2}.
- Solid phase epitaxy regrowth (SPER).

  Anneal at 550°C for 4 hours.
- Second spacer formation with low temperature oxide.
- TFET drain masked B^+ ion implantation: Energy = 10 keV, Dose = $5{\cdot}10^{15}$ cm^{-2}.
- Solid phase epitaxy regrowth (SPER).

  Anneal at 550°C for 4 hours.
- Two step rapid thermal anneal (RTA) for 900C/15s and 1050C/15s.

No metal contact layer is used in part to avoid any risk of metal impurities in close proximity to the tunneling junction.

4.3 Electrical Characterization and Temperature Dependence

Er-TATFETs were characterized using either an HP4156C or Agilent B1500A semiconductor parameter analyzer. Care was taken to ensure accuracy of low current measurements both in the electronic measurement and the experimental setup. The temperature dependence was investigated in the range from 77K to 300K in a vacuum cold-probe station. Due to a low fabrication yield, all fabricated devices were first screened using an ElectroGlas Autoprobe system modified for use with an HP4156C analyzer. Some ambipolar TFET behavior is expected for a planar SOI TFET. Overall, the asymmetric design exhibited better n-channel behavior across all active devices in this experiment. Measurement parameters for DC transfer characteristics consisted of $V_S = 0$ V, $V_{DS} = 1$ V and 1.5 V, and sweeping V_{GS} from 1 V to beyond 4 V to provide adequate gate overdrive. A large drain bias is necessary so that the tunneling current can increase significantly beyond the gate leakage current.

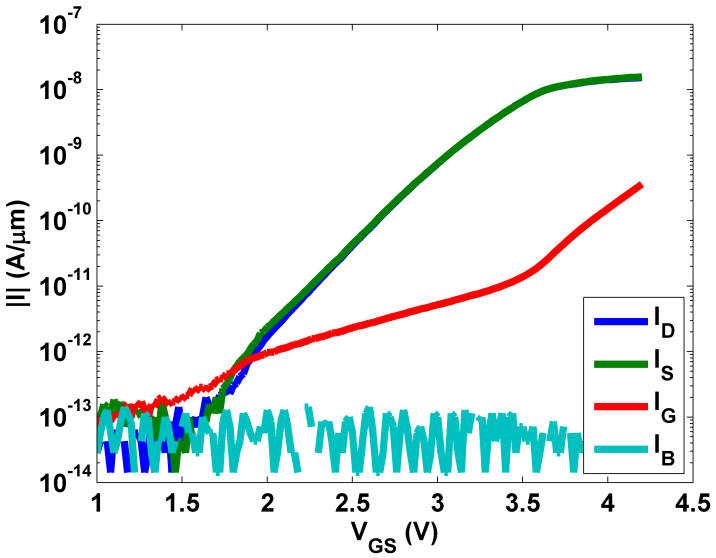

Figure 4.3: Typical DC transfer characteristics for an SOI Er-TATFET. W = 0.7 μm , L_G = 0.82 μm, and V_{DS} = 1.5 V.

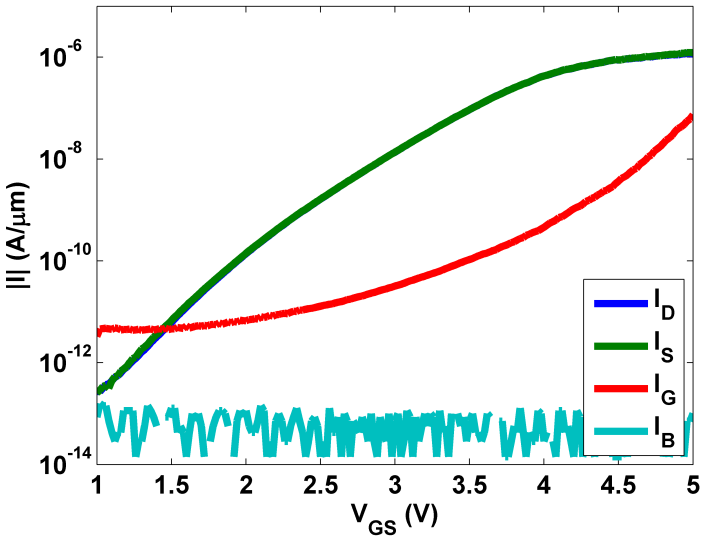

Figure 4.4: Typical DC transfer characteristics for a control SOI TFET. W = 0.7 μm, L_G = 10 μm, and V_{DS} = 1.5 V.

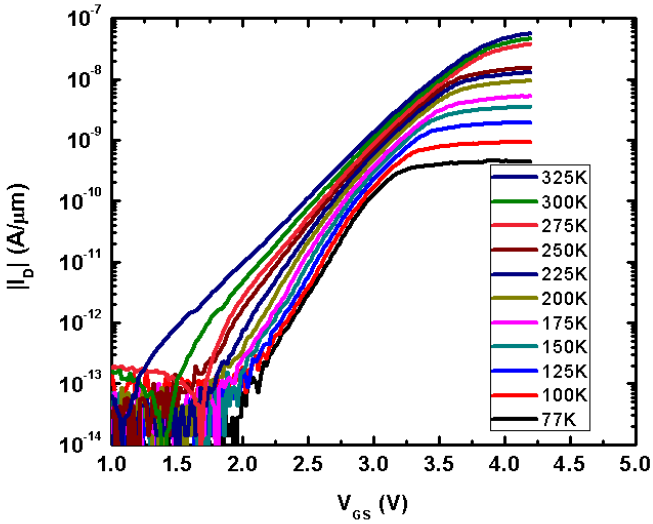

Figure 4.5: Temperature dependent DC transfer characteristics for an Er-TATFET from 77K to 300K. W = 0.7 μm, L_G = 0.82 μm, and V_{DS} = 1.5 V.

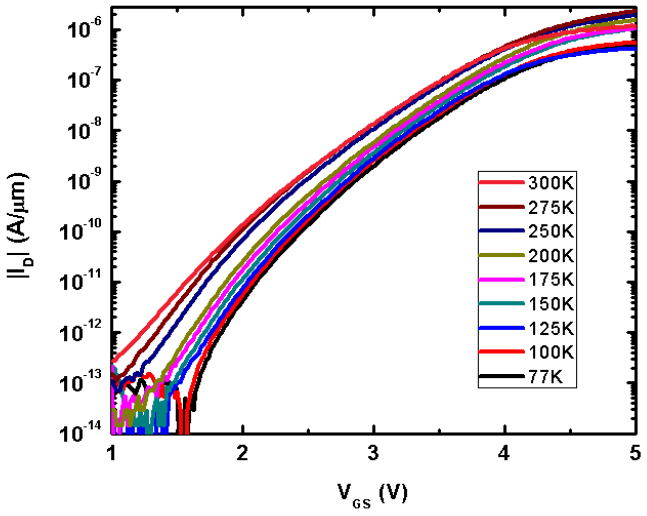

Figure 4.6: Temperature dependent DC transfer characteristics for a p-i-n control TFET from 77K to 295K. W = 0.7 μm, L_G = 10 μm, and V_{DS} = 1.5 V.

Figs. 4.3 and 4.4 show typical DC transfer characteristics ($I_{\mathrm{D}}(V_{\mathrm{GS}})$ vs. V_{GS}) for an n-channel Er-TATFET and a control SOI TFET. $|I_{\mathrm{G}}| > |I_{\mathrm{D}}|$ at lower biases is most likely due to the aggressively thin gate oxide. While strong capacitive coupling to the channel is necessary for good control of the tunneling junction, an aggressively thin gate oxide will "leak" gate current to the channel via direct tunneling and Fowler-Nordheim tunneling.[1] An obvious disadvantage for silicon based TFETs is the relatively large bandgap of silicon (1.12 eV at room temperature) requiring a larger operating voltage to achieve an adequate I_{ON}.

Figs. 4.5 and 4.6 show the temperature dependent characteristics of an Er-TATFET. I_{D} in the on-state decreases with temperature due in part to the lower thermal generation of carriers in the depleted region of the active area. Additionally, dopants begin freeze-out in Si at temperatures below 200K which reduces the active carrier concentrations. For some measurements, I_{D} did not decrease monotonically with temperature due to variable contact resistance related to difficulty in probing the device pads at lower temperatures. The subthreshold swing (SS) appears to show little dependence on temperature, verifying that BTBT has a weak dependence on temperature.

Due to the low yield of fabricated devices, temperature dependent measurements were conducted for only six TFETs: two p-i-n control TFETs and four Er-TATFETs. Table 4.1 lists dimensions and labels the transistors reported in this section. Variability across devices (e.g., 10^{-8} A/μm $\leq I_{\mathrm{ON}} \leq 10^{-6}$ A/μm) prevents a direct comparison of I-V characteristics.

TFET	W (μm)	L (μm)	Type
T1	0.7	5	p-i-n Control
T2	0.7	10	p-i-n Control
T3	0.7	2	Er-TATFET
T4	10	2	Er-TATFET
T5	0.7	0.76	Er-TATFET
T6	0.7	0.82	Er-TATFET

Table 4.1: Transistor dimensions for control and experimental devices.

Comparing Figs. 4.5 and 4.6, the SS for the Er-TATFET shows a greater sensitivity with temperature whereas the SS for the control TFET is relatively insensitive to an increase in temperature. This is not unexpected for a transistor at elevated temperatures with deep level traps near the source. Figs. 4.7 and 4.8 show how the SS changes with the drain current for an Er-TATFET and a control TFET, respectively. Qualitatively, Fig. 4.7 shows a greater temperature sensitivity for an Er-TATFET SS that is more readily apparent, especially at lower currents and higher temperatures. Direct quantitative comparisons of SS may prove misleading due to the variability observed across devices. Interestingly, the Er-TATFET SS improves as the temperature decreases and the temperature sensitivity decreases for T $\leq$ 200K. This validates the experimental design hypothesis that a lower temperature can

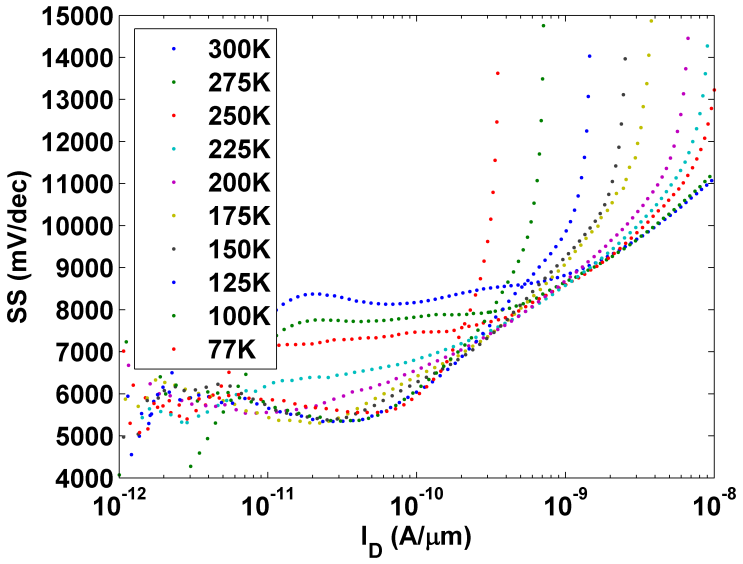

Figure 4.7: *SS* shown as a function of I_{D} for a range of temperatures for a TFET with Er trap states near the source. *SS* degrades with increasing temperatures, especially at lower drain current.

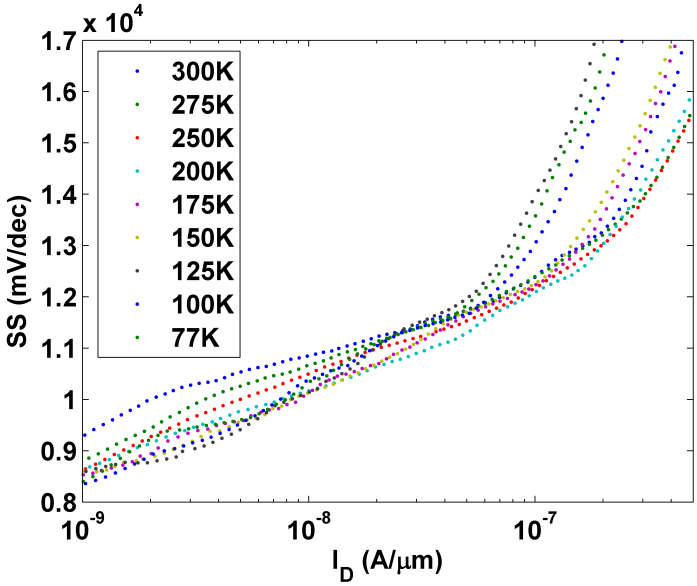

Figure 4.8: *SS* shown as a function of I_{D} for a range of temperatures for a control TFET. *SS* remains relatively insensitive to increasing temperatures.

reduce the thermal excitation generation current due to the trap states and partially isolate behavior of the traps at low temperature.

E_A calculated for the p-i-n control TFETs over a temperature range of 77K-300K is presented in Fig. 4.9. E_A for the control TFETs remains low from weak to strong inversion. The E_A calculated for all six TFETs for 77K $\leq$ T $\leq$ 200K is plotted in Fig. 4.10 as function of the drain current at 175K (close to the middle of the temperature range for this experiment). Calculating E_A for T $\leq$ 200K helps insure that any quantitative comparison of E_A between control and experimental devices isolates the role of trap states with minimal thermal generation current. Fig. 4.10 shows that the incorporation of a nominal concentration of Er trap states in Si slightly lowers E_A for BTBT in a transistor in weak inversion.

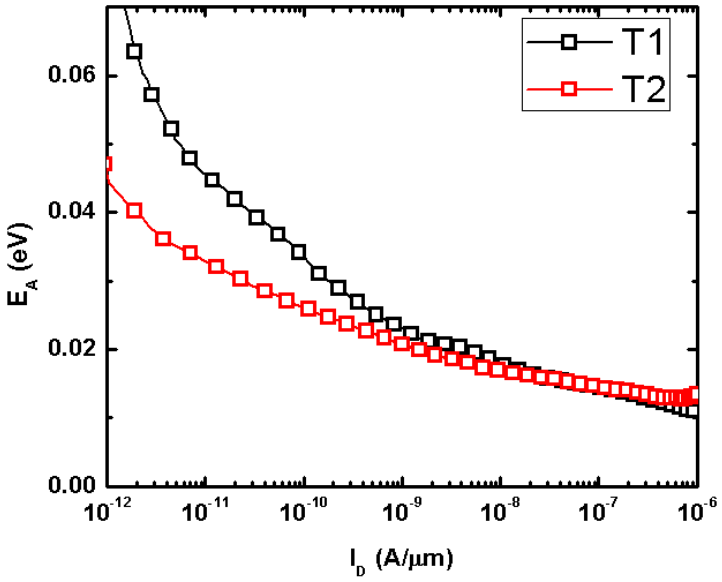

Figure 4.9: E_A shown as a function of I_D calculated for temperature 77K $\leq$ T $\leq$ 200K for p-i-n control TFETs. A low E_A validates a weak temperature dependence for BTBT.

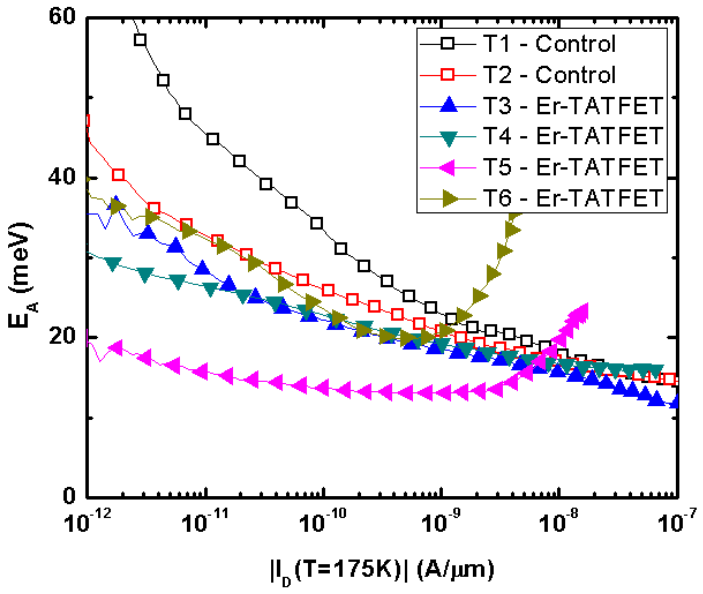

Figure 4.10: E_{A} shown as a function of I_{D} for comparison across devices. The independent variable is chosen to be $I_{\mathrm{D}}\,(T = 175K)$) for TFET. For small ranges of I_{D} in the subthreshold region, Er-TATFETs exhibit a slightly lower E_{A} (closed symbols) in comparison to E_{A} for p-i-n control TFETs with no Er traps (open symbols).

4.4 Conclusion

Isolating the role of a single trap in a large device through electrical characterization requires a prohibitively low current measurement. Targeting an impurity trap concentration near the maximum observed limit for electronically active Er in Si should improve the signal compared to isolated trap states, though a higher concentration may also alter the trap properties.[2] It has been noted that the properties of traps in a semiconductor are dependent on the proximity to nearby trap states, the doping polarity of the semiconductor, and the thermal processing steps subsequent to the formation of the trap state.[3] Qualitatively, this makes sense: if a single trap state interrupts the periodicity of the semiconductor crystal, then if follows that traps in close proximity further interrupt this periodicity.

As a thought experiment, one could imagine a 'trap state' concentration so great that a mini-band of delocalized states is formed within the band gap of the semiconductor (a goal for exotic materials research for photovoltaics).[4, 5] If the presence of a miniband within the band gap significantly reduces the effective energy band gap for tunneling, then a natural conclusion to this thought experiment is to use a lower bandgap material at the tunneling junction. The advantage of a heterostructure is that it can lower the effective tunneling bandgap and so increase the tunneling current (I_{ON} for a TFET). In short, a TFET design

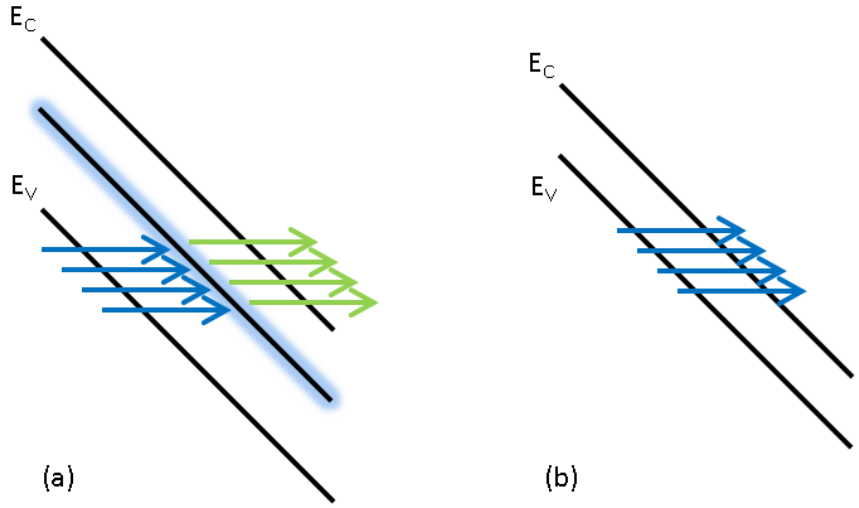

Figure 4.11: (a) A substantially high concentration of electronically active traps states present in the tunneling junction could form a quasi-continuous third band within the bandgap of the semiconductor. (b) In the context of BTBT junction design, a lower bandgap material should provide a cleaner and more efficient tunneling path.

should necessarily incorporate strong electrostatic control so that a reduced effective bandgap can be employed in the source without sacrificing off-state leakage.

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Chapter 5

Design Optimization of Homojunction TFETs with Back Biasing

5.1 Introduction

One target metric for any solid state switching device is a large I_{ON}/I_{OFF} current ratio. Since the steepest switching for a band-to-band tunneling (BTBT) transistor occurs at lower current (see equation 1.3 and Figs. 1 and 4 in [1]), minimizing leakage current and maintaining a low I_{OFF} is necessary in order to observe a steep subthreshold slope (SS). Strong electrostatic control over the entire active region of a TFET is then necessary to mitigate off-state leakage and maintain a low I_{OFF}. A narrow tunneling barrier width at the onset of tunneling and a large tunneling area both act to increase I_{ON}. Increasing the tunneling area can be accomplished by parallel band bending (or parallel band-to-band overlap) across the width of the tunneling junction. The SS for a TFET with a large area BTBT junction is then limited by the steepness of the density of states energy distribution (provided I_{OFF} remains low).

Various TFET structures have been proposed to improve upon early planar gated reverse-biased p-i-n diode designs. These designs often increase the fabrication complexity. (For example: heterostructures, compound semiconductor materials, quantum confinement for a density-of-states cutoff, or an asymmetric bi-layer structure.[2–4]) To maintain a simple design approach for a TFET, this chapter explores a planar homojunction design for ease of manufacturability.

An initial investigation of a planar p-i-n silicon-on-insulator (SOI) TFET structure showed that a reverse back bias ($V_B < 0$ V) can improve I_{ON}/I_{OFF}.[5] An SOI substrate allows for the application of a static reverse back-side bias (throughout the DC transfer characteristic) which enhances the vertical component of BTBT. Figs. 5.1 and 5.2 show a >50% improvement in I_{ON}/I_{OFF} for V_B = -3 V. The SOI TFET structure was optimized at $V_B = 0$ V. As reported in [6], reducing the semiconductor body thickness improves the gate

control provided that t_{BODY} remains large enough to avoid quantum conofinement effects.[1] A sufficiently thin t_{BODY} allows for a fully depleted active area and also reduces the thermal generation-recombination current for a reverse biased p-i-n diode TFET.[7] Since the benefit of a static reverse back bias should be transferrable to a lower bandgap material, a germanium-on-insulator (GeOI) TFET design study is presented in the remaining sections of this chapter.

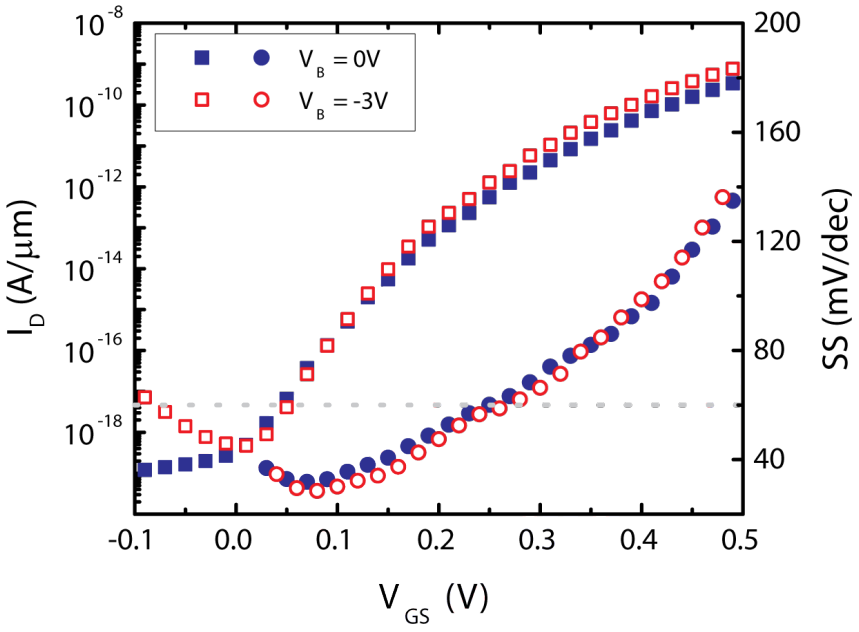

Figure 5.1: Simulated SOI TFET $I_{\mathrm{D}}\,(V_{\mathrm{GS}})$ with (open squares) and without (filled squares) back bias. $SS\,(V_{\mathrm{GS}})$ with (open squares) and without (filled squares) a reverse back bias. The lefthand y-axis corresponds to the I_{D}-V_{GS} transfer characteristic and the righthand y-axis corresponds to the SS.

[1] For a thin semiconductor, the bandgap increases with increasing quantum confinement.

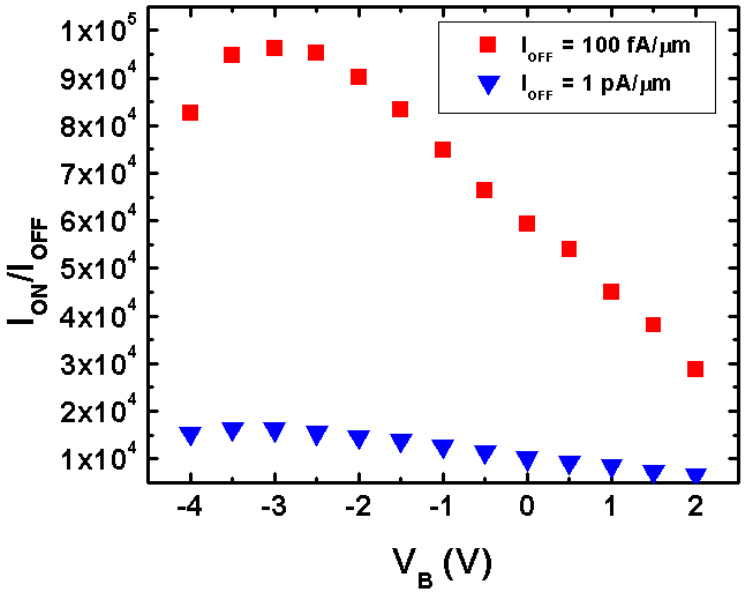

Figure 5.2: I_{ON}/I_{OFF} for two different constant current I_{OFF} values. In both cases, I_{ON}/I_{OFF} improves with reverse back bias with a greater effect for a lower I_{OFF}.

5.2 Simulation Structure to Investigate Lower E_g Materials for Planar Homojunction TFET

Fig. 5.3(a) shows a schematic diagram of the planar GeOI TFET design simulated in this study. The net doping profiles within the semiconductor layer along the A-A' cutline are illustrated in Fig. 5.3(b), for two TFET source profile designs. One has a maximum p-type source dopant concentration of $2{\cdot}10^{19}$ cm^{-3} aligned to the gate edge, and a narrow Gaussian source doping profile that corresponds to a gradient of 1 nm/dec; this is heretofore referred to as the gate-aligned (GA) source design. The other has a maximum p-type source dopant concentration of $4{\cdot}10^{19}$ cm^{-3} offset from the gate edge by 10 nm, and a wide Gaussian source doping profile that corresponds to a gradient of 20 nm/dec; this is heretofore referred to as the gate-overlapped (GO) source design. As will be shown below, the GA source design is optimal if $V_B = 0$ V, but the GO source design is optimal if V_B = -1.7 V.

Fixed Parameters

The default value for the gate length (L_G) is 30 nm to avoid significant short-channel effects, as will be discussed below. The other fixed design parameters are chosen to achieve good electrostatic integrity: the Ge thickness (T_{Ge}) is 10 nm; the gate dielectric has an equivalent oxide thickness of 0.8 nm, and the buried oxide (BOX) layer is 10 nm thick. The gate-sidewall

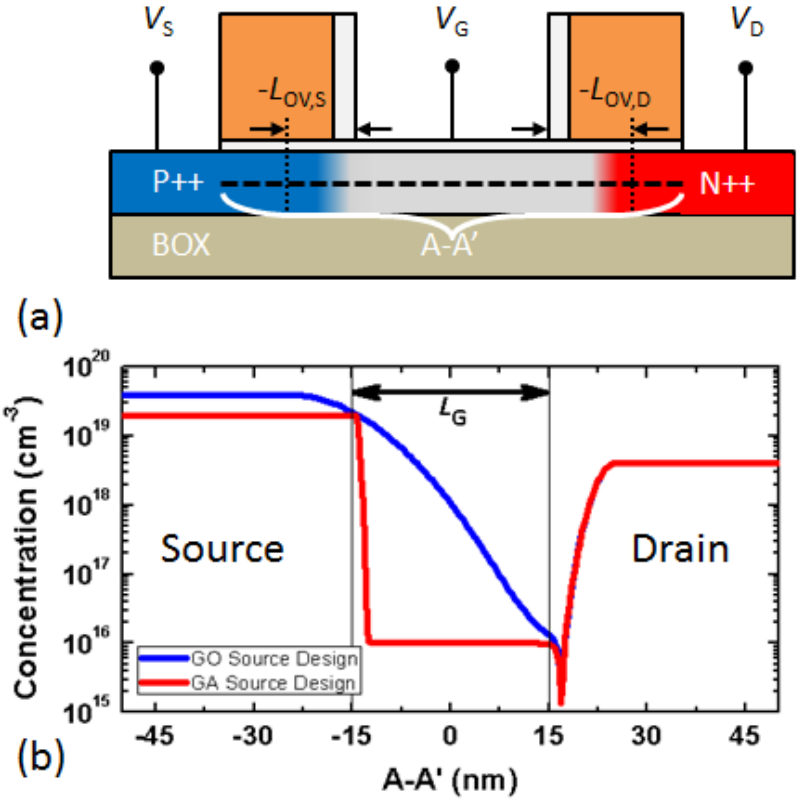

Figure 5.3: (a) Schematic cross-section of an n-channel planar GeOI TFET. A-A is the cutline for which the absolute value of the net dopant concentration profile is shown in (b). (b) Comparison of the net doping profiles for a gate-overlapped (GO) source design (solid line) and a gate-aligned (GA) source design (dashed line). The center of the channel region is located at $x = 0$ nm.

spacers are comprised of an inner 5-nm-thick silicon-dioxide layer and an outer 15-nm-thick silicon-nitride layer. The Ge channel region is lightly doped p-type at 10^{15} cm^{-3}. The gate material is metallic with a work function of 4.0 eV. Ohmic contacts to the source and drain regions (each 30 nm long) are made along the upper Ge surfaces outside of the spacers. The underlying substrate is p-type Si with a 10^{19} cm^{-3} dopant concentration. The n-type drain has a maximum dopant concentration of $4{\cdot}10^{18}$ cm^{-3} that is offset from the edge of the gate by 10 nm, and a Gaussian doping profile that corresponds to a gradient of 5 nm/dec (see Fig. 5.3(b)). This drain design was found to be optimal for minimizing off-state leakage without degrading I_{ON}/I_{OFF}, for $V_{DD} = 0.25$ V and $V_B = 0$ V.

Variable Parameters

The maximum source dopant concentration, N_{SRC}, was varied from $1{\cdot}10^{18}$ cm^{-3} to $1{\cdot}10^{20}$ cm^{-3} in this study. The source doping profile decays as a Gaussian function toward the channel region. The gate-to-source overlap, $L_{OV,S}$, is defined as the distance from the gate

edge to the position where the Gaussian decay begins. (If $L_{OV,S}$ is negative, the source doping profile begins decaying from a position to the left of the gate edge. If $L_{OV,S}$ is positive, the source doping profile begins decaying from a position to the right of the gate edge, underneath the gate.) $L_{OV,S}$ was varied from -14 nm to 6 nm, and the doping gradient (DG) was varied from 1 nm/dec to 22 nm/dec, in this study. The three source design parameters (N_{SRC}, $L_{OV,S}$, and DG), as well as the body thickness T_{Ge}, influence the location and size of the tunneling region and thereby I_{ON}/I_{OFF}.

Simulation

Synopsys TCAD software was used to study the performance of GeOI TFETs via 2D device simulations. Sentaurus Structure Editor was used to define the TFET structure, and Sentaurus Device was used to simulate device operation using a dynamic non-local BTBT model based on Kane's model.[8] Equation 1.3 in chapter 1 represents a simplified version of Kane's model. The properties of Ge are well characterized, so the default Ge material parameters were used in this work: A = $2.8{\cdot}10^{15}$ cm^{-3} s^{-1}, and B = $1.9{\cdot}10^{7}$ V/cm. The dynamic non-local BTBT model has been demonstrated to be in good agreement with experimental results.[9]

5.3 Planar GeOI TFET Performance Enhancement via Back Bias

Gate Aligned and Gate Overlapped Designs

I_{ON}/I_{OFF} is the primary figure of merit used to assess the effect of the source doping profile parameters for TFETs in this study. I_{ON} is defined to be the drain current, I_D, at V_{GS} - V_{OFF} = 0.25 V for V_{DS} = 0.25 V, where V_{OFF} is defined to be the value of the gate-to-source voltage (V_{GS}) that corresponds to $I_D = I_{OFF}$ = 100 fA/μm. (In other words, it is assumed that, in practice, gate work function engineering and delta doping can be used to tune V_T, as for a MOSFET, so that V_{OFF} = 0 V.)

Fig. 5.4 shows I_{ON}/I_{OFF} contours and highlights the dependence of I_{ON}/I_{OFF} on $L_{OV,S}$ and the DG. Contours are presented for two values of N_{SRC}, Fig. 5.4(a) represents N_{SRC} = $2{\cdot}10^{19}$ cm^{-3} with V_B = 0 V and Fig. 5.4(b) represents N_{SRC} = $4{\cdot}10^{19}$ cm^{-3} with V_B = -1.7 V. These peak doping concentrations in the source correspond to the optimized GA and GO source designs. The hatched region in Fig. 5.4(a) indicates the range of $L_{OV,S}$ and DG combinations that result in I_{OFF} > 100 fA/μm due to the short-channel effect.

Fig. 5.4(a) shows that for V_B = 0 V, the optimal source design is the GA profile (i.e. provides for the highest I_{ON}/I_{OFF}), since the contours peak when $L_{OV,S}$ is near 0 nm and the DG is close to 1 nm/dec. (This is representative of the trend seen for the entire range of N_{SRC} values studied in this work, when V_B = 0 V.) Note that the design window for optimal performance is relatively narrow. This is because tunneling occurs primarily from the GA

source region to the channel inversion layer, so that it is highly sensitive to the alignment between the source-channel junction and the gate edge: if the gate underlaps the source, then gate coupling to the channel at the source junction is degraded; if the gate overlaps the source, then the source depletion width (hence tunneling distance) is increased.

Fig. 5.4(b) shows that the GO source design is optimal when V_B = -1.7 V, since the contours peak at larger values of the DG. (If the DG·1 dec > -$L_{OV,S}$ then the source doping profile extends underneath the gate electrode, as in Fig. 5.3(b)). Note that the design window for optimal performance is relatively wide. This is because tunneling occurs primarily within the GO source region, so that I_{ON} is largely dependent on the extent of the gate-to-source overlap: many combinations of the DG and $L_{OV,S}$ result in a similar overlap and hence comparable I_{ON}; I_{ON} falls off with increasing $L_{OV,S}$ when the short-channel effect becomes significant.

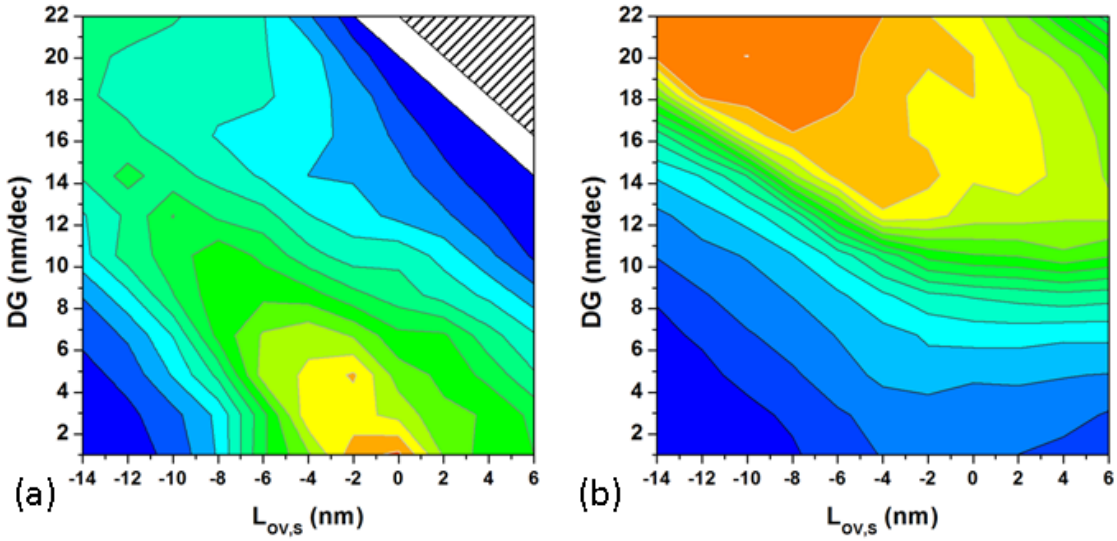

Figure 5.4: Simulated I_{ON}/I_{OFF} contour plots showing how GeOI TFET performance depends on the source doping gradient and the gate-to-source overlap, for optimized peak source profile concentrations. (a) N_{SRC} = 2·10^{19} cm^{-3} and V_B = 0 V, (b) N_{SRC} = 4·10^{19} cm^{-3} and V_B = -1.7 V.

As shown in Fig. 5.5, reverse back-biasing is beneficial for both source designs (using the doping profiles optimized for L_G = 30 nm), but more so for the GO design so that it becomes superior to the GA design when V_B < -0.25 V. I_{ON}/I_{OFF} reaches a peak at V_B = -1.7 V for the GO design, whereas it does not reach a peak for the GA design within the range of V_B values studied. To elucidate the reasons for this, Fig. 5.6 shows log-scale contour plots of the BTBT generation rate at V_{GS} - V_{OFF} = 0.25 V and V_{DS} = 0.25 V, for four cases: the GA design and the GO design each at V_B = 0 V and V_B = -1.7 V. The dashed line in each plot indicates the horizontal position of the gate edge. The lower contours which extend to the left beyond the gate edge indicate the hole generation rate, while the upper contours which

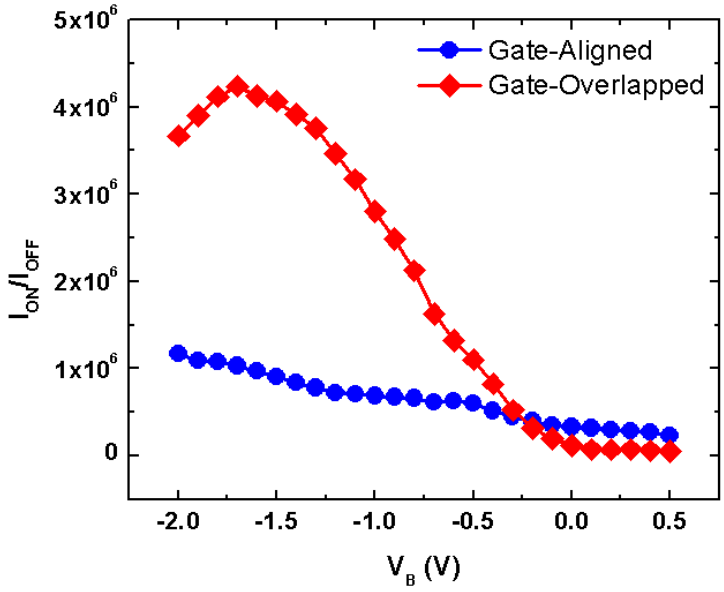

Figure 5.5: Simulated impact of back bias voltage on I_{ON}/I_{OFF} for the two GeOI TFET designs: gate-aligned (GA) source and gate-overlapped (GO) source.

extend to the right under the gate electrode indicate the electron generation rate. For the GA design (Figs. 5.6(a) and 5.6(b)), it can be seen that tunneling occurs primarily from the source region to the channel inversion layer; the application of a reverse back-bias enhances the vertical component of the electric field and thereby improves I_{ON}/I_{OFF}. For the GO design, it can be seen that tunneling occurs primarily within the overlapped source region. With zero back bias, the GO design serves as poorly gated Zener diode (Fig. 5.6(c)). Since reverse back-biasing enhances the vertical component of the electric field, resulting in BTBT over a relatively wide region within the source underneath the gate electrode; the larger tunneling area results in larger I_{ON} for the reverse-back-biased GO design (Fig. 5.6(d)).

For a fixed value of L_G and a given drain doping profile, I_{ON}/I_{OFF} for the GO design reaches a peak near V_B = -1.7 V. This is because a significant hole accumulation region forms near the drain junction and thereby introduces significant series resistance which decreases I_{ON} for V_B < -1.7 V. (Although a similar peak is not observed for the GA design within the range of V_B values studied, increasing drain-side series resistance should eventually limit the improvement in I_{ON}/I_{OFF} for this design as well.) Further optimization of the drain doping profile may lead to greater I_{ON}/I_{OFF} improvement for large reverse back-bias voltages.

Fig. 5.7 compares the transfer characteristics for the two optimized source designs, with and without reverse back-biasing. The GA design (optimized at $N_{SRC} = 2{\cdot}10^{19}$ cm^{-3}, $L_{OV,S}$ = 0 nm, and DG = 1 nm/dec) achieves $I_{ON}/I_{OFF} = 3.26{\cdot}10^5$ at V_B = 0 V and I_{ON}/I_{OFF} = $1.03{\cdot}10^6$ at V_B = -1.7 V, representing more than 3× improvement with reverse back-

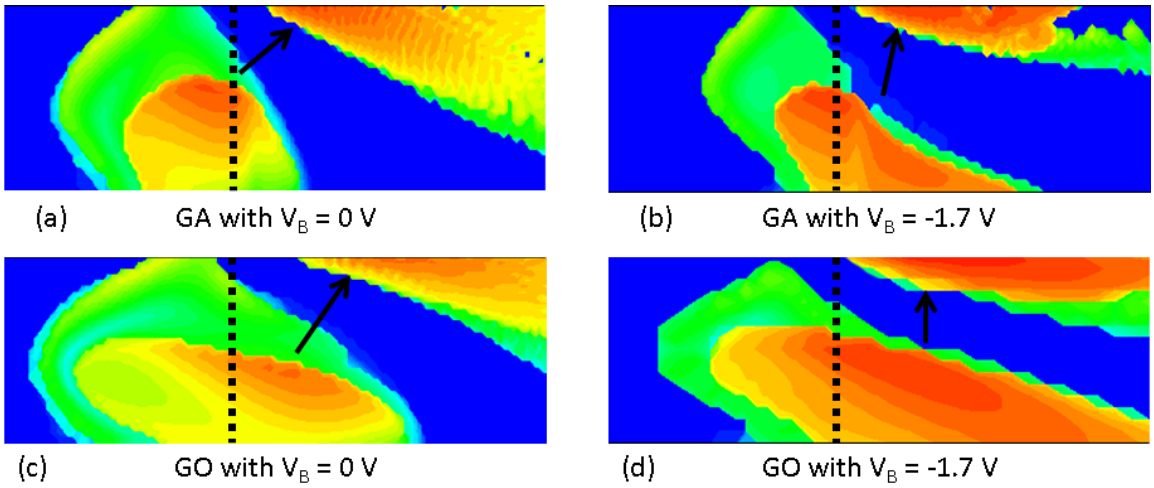

Figure 5.6: Simulated contour plots for GeOI TFET on-state (V_{GS} - V_{OFF} = 0.25 V, V_{DS} = 0.25 V) BTBT rate (log scale, arbitrary units) contour plots for (a) GA source design with V_B = 0 V, (b) GA source design with V_B = -1.7 V, (c) GO source design with V_B = 0 V, (d) GO source design with V_B = -1.7 V. The arrows indicate the general direction of tunneling electrons.

biasing. The GO design (optimized at $N_{SRC} = 4{\cdot}10^{19}$ cm^{-3}, $L_{OV,S}$ = -10 nm, and DG = 20 nm/dec) achieves $I_{ON}/I_{OFF} = 1.22{\cdot}10^5$ at V_B = 0 V and $I_{ON}/I_{OFF} = 4.24{\cdot}10^6$ at V_B = -1.7 V, representing more than 34× improvement with reverse back-biasing. These results affirm that the GA design is superior when there is no applied back bias (solid dark curve in Fig. 5.7), and that the GO design becomes superior if a significant reverse back-bias is applied (grey dotted line in Fig. 5.7).

The off-state leakage current is slightly larger with V_B = -1.7 V for both the GA and GO designs, due to an increase in the volume of the space-charge region resulting in more recombination- generation current. It should be noted that the turn-on voltage (V_{OFF}) increases and that SS becomes steeper with reverse back-biasing. This is somewhat analogous to the increase in V_T and improved electrostatic integrity of a thin-body MOSFET with reverse back-biasing.[10] For the GA design, a larger gate voltage is required to form an inversion layer in the lightly doped channel region (to which carriers tunnel from the source region) when a reverse back-bias is applied, and an enhanced electric field in the on state provides for greater BTBT current. For the GO design, a larger gate voltage is also required to invert the Ge surface (to allow BTBT to occur within the source region); however, since the source has a graded doping profile, this increase in required gate voltage is not uniform across the lateral extent of the source - it increases with decreasing dopant concentration. Since a larger gate voltage is required to invert the surface of a more heavily doped semiconductor when V_B = 0 V, the effect of the reverse back-bias is to induce a graded shift in turn-on voltage so that band overlap occurs more uniformly across the source region and hence the TFET switches more abruptly.

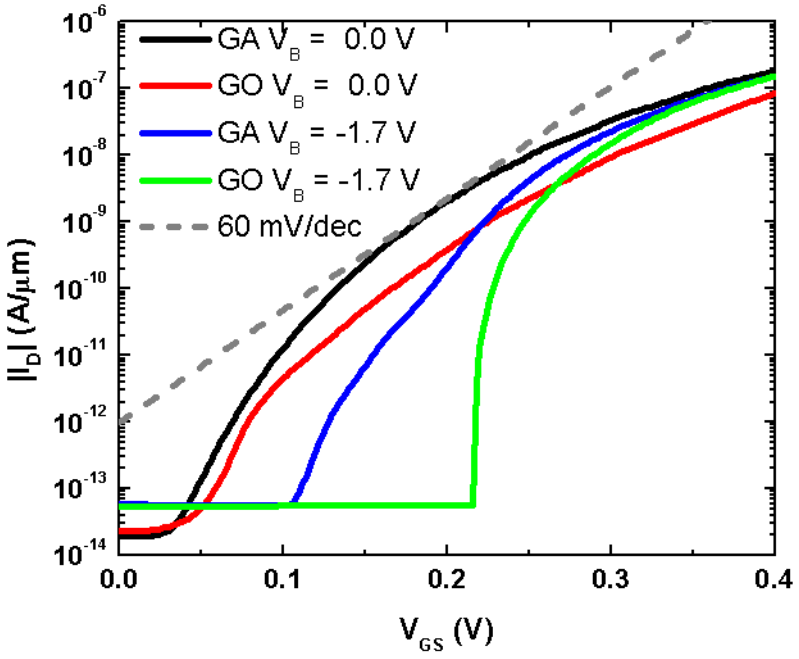

Figure 5.7: Comparison of simulated GeOI TFET transfer characteristics for the GA and GO source designs, with and without reverse back-biasing.

Short Channel Effect Mitigation

Fig. 5.8 shows how GeOI TFET performance depends on L_G for the GA and GO source designs optimized for $L_G = 30$ nm. Note that there is no gate-length dependence for $L_G > 30$ nm; in this regime, the drain bias has little influence on the BTBT rate. As L_G decreases below 30 nm, the lateral electric field induced at the tunneling junction by the drain voltage increases sufficiently to cause BTBT to occur at a smaller gate voltage. This is manifested as a decrease in V_{OFF} with decreasing L_G (Fig. 5.8(a), $V_B = 0$ V). As a result, the influence of the gate voltage is diminished, i.e. SS becomes less steep and hence I_{ON}/I_{OFF} decreases (Fig. 5.8(b), $V_B = 0$ V). It is interesting to note that, although the GO design results in a much shorter electrical channel length, degradation in I_{ON}/I_{OFF} occurs only slightly earlier (i.e. beginning at slightly longer L_G) because BTBT occurs in a more vertical direction so that drain-induced BTBT is not much more significant than for the GA design, as can be deduced from the comparison of drain-induced BTBT effect (DIBE) in Fig. 5.9.

Reverse back-biasing provides for more dominant gate control of the BTBT current and thereby reduces the short-channel effect. As L_G decreases below 30 nm, the average p-type doping underneath the gate electrode increases so that the gate voltage required to induce BTBT (i.e., V_{OFF}) increases. Also, for the GO design, I_{ON}/I_{OFF} decreases with decreasing L_G due to decreased tunneling area. Re-optimizing the source and drain doping profiles for

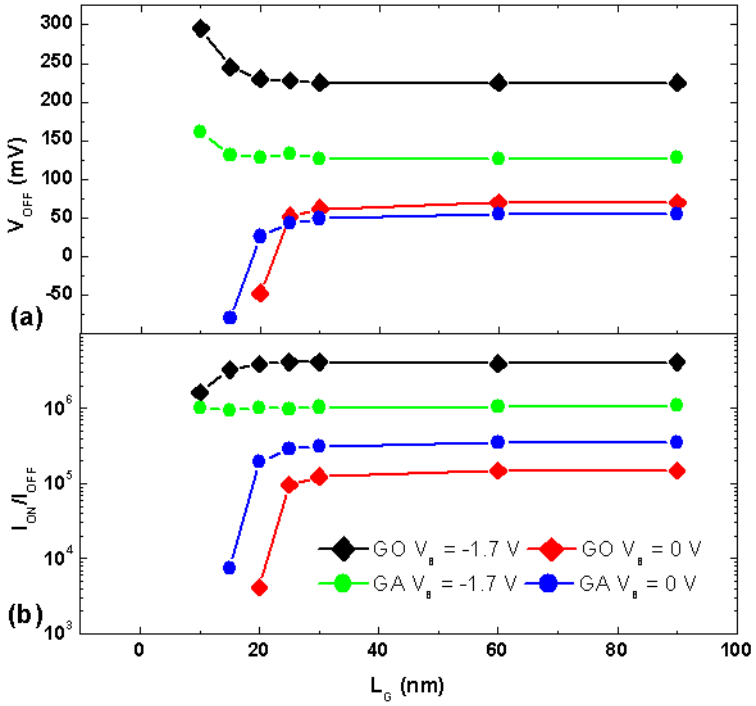

Figure 5.8: Dependence of (a) V_{OFF} and (b) $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ on $L_{\mathrm{G}} \geq 10$ nm for GeOI TFETs with gate-overlapped (GO) or gate-aligned (GA) source designs, with or without reverse back bias. V_{OFF} is defined as V_{GS} when $I_{\mathrm{D}} = 100$ fA/μm. Reverse back biasing mitigates the short channel effect and therefore improves scalability. $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ($V_{\mathrm{B}} = $ -1.7 V) decreases with decreasing L_{G} for the GO design due to a corresponding decrease in the gate area overlapping the tunneling area. V_{OFF} and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ are not defined when I_{D} never falls below 100 fA/μm.

each value of $L_{\mathrm{G}} < 30$ nm can help to mitigate these short-channel effects.

Source Design Optimization for Vertical Tunneling

From Fig. 5.6 it can be deduced that the highest I_{ON} is achieved when BTBT occurs within the source (i.e., in a more vertical direction), because the tunneling area can be readily increased by increasing the gate-to-source overlap and/or applying a reverse back-bias, in this case. Many combinations of DG and $L_{\mathrm{OV,S}}$ result in the same overlap, but a closer examination of Fig. 5.4(b) reveals that higher $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ is achieved with a more graded source doping profile when a significant reverse back-bias is applied. For a fixed value of DG·1 dec + $L_{\mathrm{OV,S}} > 0$ nm, higher $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ is achieved with larger DG rather than with larger $L_{\mathrm{OV,S}}$, (i.e., with a graded source rather than with a uniform source). This is because lighter source doping at the channel junction reduces the likelihood of lateral (source-to-channel) BTBT which is associated with worse SS (ref. Fig. 5.7). To highlight this point, the impact of N_{SRC} is shown in Fig. 5.10, for the GA and GO source designs as well as a

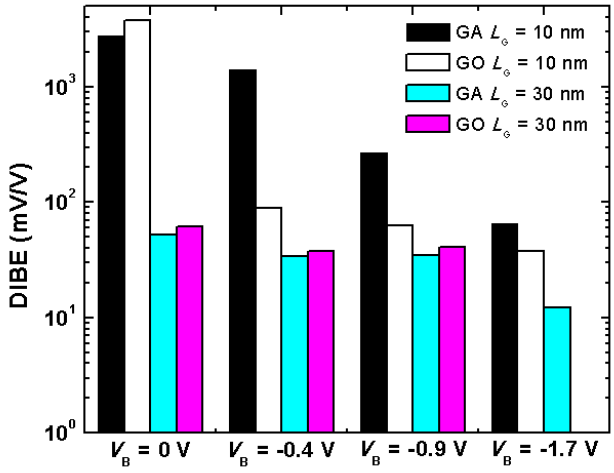

Figure 5.9: Comparison of the drain induced BTBT effect (DIBE) on a log scale for GA vs. GO source designs, at various values of back bias voltage. DIBE is the change in V_{OFF} (in mV) for 0.025 V $\leq V_{DS} \leq$ 0.25 V. For L_G = 30 nm, both designs show low DIBE (which disappears altogether for the GO design at V_B = -1.7 V). For L_G = 10 nm, reverse back-biasing mitigates DIBE more effectively for the vertical tunneling (GO) design than for the lateral tunneling (GA) design, since the latter is inherently more susceptible to the influence of the drain bias on the lateral electric field.

uniformly doped source design with $L_{OV,S}$ = 10 nm and a DG = 1 nm/dec. (L_G = 60 nm in this figure only, to avoid the short channel effect for the uniformly doped source design.) I_{ON}/I_{OFF} for the uniformly doped source design dips below that for the GO source design near $N_{SRC} = 1{\cdot}10^{19}$ cm^{-3} as BTBT transitions from tunneling primarily within the source (as for the GO source design) to tunneling primarily from the source to the channel (as for the GA source design).

Fig. 5.11 shows the simulated GeOI TFET output characteristics for the GA and GO source designs, with and without reverse back-biasing. The small-signal output resistance ro is taken to be the inverse slope of a best-fit line from 0.20 V $\leq V_{DS} \leq$ 0.25 V for $V_{GS} - V_{OFF}$ = 0.25 V. Reverse back-biasing depletes the drain offset region, forming a barrier to electron flow; this barrier (rather than BTBT at the source) is modulated by the drain bias, so that r_o is reduced when V_B = -1.7 V. Despite this, intrinsic gain ($g_m r_o$, evaluated at $V_{GS} - V_{OFF}$ = V_{DS} = 0.25 V) remains well above 1, decreasing from 13.0 to 5.7 for the GA design and from 20.1 to 9.1 for the GO design when V_B is changed from 0 V to -1.7 V. As can be seen in Fig. 5.11, reverse back-biasing improves the linearity of the I_D-V_D characteristic at low values of V_{DS}, which is consistent with a reduction in DIBE (see Fig. 5.9).

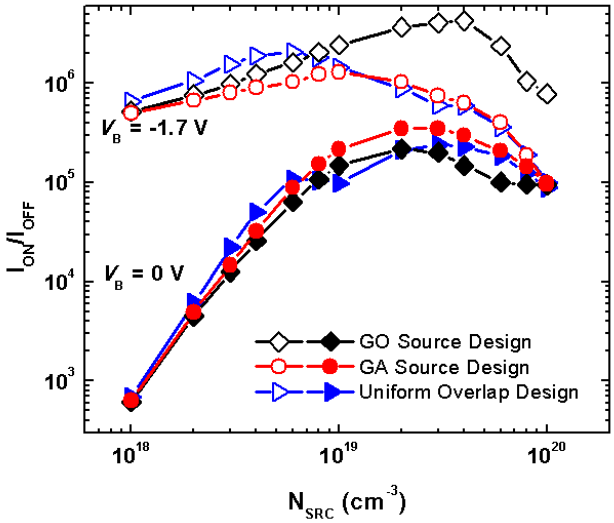

Figure 5.10: Impact of peak source dopant concentration (N_{SRC}) on $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$, for GeOI TFETs with GA, GO, or uniform source ($L_{\mathrm{OV,S}}$ = 10 nm and DG = 1 nm/dec) design. L_{G} = 60 nm to avoid the short channel effect. The uniformly doped source design transitions from tunneling within the source to tunneling from source to channel near $N_{\mathrm{SRC}} = 10^{19}$ cm^{-3}. The GO design outperforms the other designs at V_{B} = -1.7 V, for $N_{\mathrm{SRC}} \geq 10^{19}$ cm^{-3}.

T_{Ge} Dependence

T_{Ge} should be sufficiently thick so as to avoid fully vertically depleting the source region underneath the gate if vertical BTBT within the source is desired. (Also, if T_{Ge} is too thin, quantum confinement effects can reduce the density of states for tunneling, even if lateral BTBT from the source to the channel is desired.) For a source doping level of $2{\cdot}10^{19}$ cm^{-3}, T_{Ge} should be at least 10 nm to avoid full vertical depletion. As shown in Fig. 5.12, reverse-biased diode leakage is adequately suppressed at this thickness.

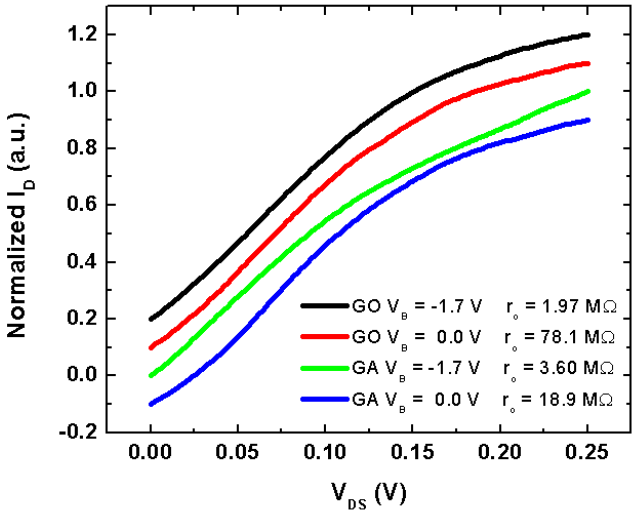

Figure 5.11: Comparison of output current normalized to the maximum value at $V_{GS} - V_{OFF} = 0.25$ V and $V_{DS} = 0.25$ V, as a function of the drain-to-source voltage. The output characteristics have been offset for clarity.

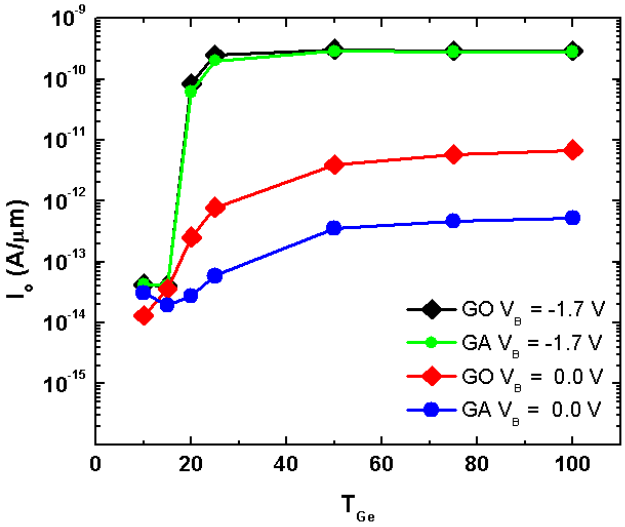

Figure 5.12: Off-state leakage current (I_D at $V_{GS} = 0$ V) in a GeOI TFET as a function of the Ge thickness, for the different source designs with and without reverse back-biasing. Reverse diode leakage current (due to BTBT at the drain junction) increases linearly with the diode area, and is dramatically enhanced by reverse back-biasing to increase the electric field.

5.4 Conclusion

With a proper design of the source doping profile, an optimal reverse back bias increases the vertical tunneling component and results in greater than 30× enhancement in I_{ON}/I_{OFF} for a GeOI TFET. Reverse back bias for a lateral tunneling design, however, only yields approximately 3× enhancement.

For the reverse back-biased vertical tunneling design, a graded source doping profile provides for superior performance due to reduced short channel effect and more uniform band overlap across the lateral extent of the source region. The results of this study indicate that reverse back-biasing is a more effective performance booster for a GeOI TFET than for an SOI TFET.[5] This is because band overlap can be induced across a shorter distance within Ge, because of its smaller bandgap, so that more vertical tunneling can be induced with reverse back-biasing in a thin-body Ge TFET vs. a thin-body Si TFET. (Likewise, the benefit of reverse back-biasing should be greater for semiconductor materials with even smaller bandgap.) Finally, reverse back-biasing is also beneficial for improving TFET scalability, particularly if the source and drain doping profiles are co-optimized together with the gate length.

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Chapter 6

Conclusion

6.1 Summary of Contributions

Detailed electrical characterization for an enhanced Schottky-Barrier MOSFET (SB-MOSFET) confirmed a steep subthreshold swing (SS) at low current with an operating voltage window of 0.5 V. This enhanced SB-MOSFET structure utilized a steep doping profile produced by dopant segregation from silicide. Silicidation processes most likely produce a diffusion tail of metal impurity atoms beginning near the silicide/silicon interface and extending into the active region of the device.[1, 2] Despite the sub-$\frac{k_{\mathrm{B}}T}{q}\ln(10)$ SS, electrostatic simulation of the structure for the same operating voltages did not indicate any band overlap in the device. Temperature dependent I-V measurements in addition to back bias dependent characterization suggest a plausible operating mechanism where electronic trap states augment the source injection of carriers with a combination of tunneling to trap states followed by thermal excitation of the carriers to produce sub-60 mV/dec SS at room temperature.

To further explore the role of traps in close proximity to the band-to-band tunneling (BTBT) junction, erbium (Er) impurity atoms exhibiting deep level electronic trap behavior in Si were introduced near the tunneling junction of p+ poly-Ge/Si heterodiodes. Comparing the activation energy, E_{A}, of p+-i-n+ heterodiodes with and without Er trap states confirms a previously documented energy level of Er in Si of $E_{\mathrm{C}} - E_{\mathrm{T}} = 0.6$ eV.[3, 4] Exploring the role of traps for a p+-n+ tunneling heterodiode, however, was limited without a control device for comparison or an accurate trap-assisted tunneling model for semiconductor device simulation.

An additional investigation of the role of trap states in BTBT included testing Er-based trap-assisted TFETs (Er-TATFETs) fabricated on an SOI substrate. Isolating the role of trap states is possible by significantly reducing the thermal generation-recombination current in the device. Low temperature measurements helped identify the temperature range over which the thermal generation rate due to traps is dramatically reduced. Er-TATFETs show a slightly lower E_{A} compared to p-i-n control TFETs for T $\leq$ 200K over a range of operation within the subthreshold regime.

Finally, a reverse back bias applied to planar SOI or GeOI homojunction TFETs improves I_{ON}/I_{OFF} by increasing the vertical component of BTBT. A conventional source design for a planar p-i-n TFET typically calls for a steeply graded doping profile in order to take advantage of the large built-in electric field provided by a nearly abrupt doping profile. Applying a reverse back bias ($V_B < 0$ V for an n-channel TFET), however, dramatically relaxes the source doping gradient design window for BTBT in Ge at low power supply voltages. A gate-overlapped graded source doping profile with reverse back bias shows significant improvement in I_{ON}/I_{OFF} due to BTBT within the source rather than from the source to the channel (as is the case for a gate-aligned abrupt source profile). The use of a source-optimized profile with reverse back bias also mitigates short channel effects. Further improvement in I_{ON}/I_{OFF} and aggressive scaling may be possible by co-optimizing the source and drain doping profiles with a static reverse back bias.

6.2 TFET Design Challenges

Many challenges likely need to be addressed for further TFET development. A partial list below highlights some of the more fundamental problems.

- Fabrication complexity
  - Homojunction versus heterojunction
  - Semiconductor materials choice
  - Non-conventional planar processing techniques
  - Asymmetry in device design
- BTBT Junction Design
  - Density of States (DOS) switching versus tunneling barrier width modulation
- BTBT semiconductor device modeling
  - Empirical BTBT models
  - Infinitely sharp band edges

Fabrication Complexity

Historically, each technology node advancement in transistor development introduces at most only a few "radical" changes to the design of the final product. (One example would be the transition to an alternate gate dielectric material with a metal gate within one generation.) The successful co-integration of TFETs with MOSFET technology will likely require simple TFET designs using proven processing techniques and materials. BTBT within homojunctions are advantageous due to the material simplicity whereas BTBT with heterojunctions may not be economically viable. Introducing a compound semiconductor heterostructure

(e.g., a quantum well structure) further complicates the processing requirements for non-similar devices such as MOSFETs. Finally, the inherent doping (and sometimes structural) asymmetry in TFETs places additional demands on lithographic patterning and wafer real estate.

BTBT Junction Design

One very simple conceptual requirement for BTBT is that a carrier must originate from an occupied state and tunnel to an unoccupied state. A BTBT junction design where the tunneling current is modulated by changing the barrier width only changes the tunneling probability and varying the channel potential beyond strong inversion is similar to a law of diminishing returns. A perhaps better junction design would utilize a large number of available tunneling states at turn-on rather than simply trying to increase the tunneling probability.

Semiconductor Device Modeling for BTBT

Most device simulation BTBT models make use of empirical equations for calculation at a grid point. While numerically efficient, this approach does not account for wavefunction overlap. While improved BTBT models make a dynamic calculation of the tunneling direction, the models still rely on simplified material fitting parameters and are not always accurate. For example, despite the dynamic nonlocal BTBT model in Synopsys Sentaurus, Esaki tunneling diode simulations still do not account for experimentally observed excess current. Simulation results are optimistic due to the infinitely sharp band edges assumed in the band structure model. As such, many TFET structures in Synopsys Sentaurus show steeper switching than when studied using atomistic models and a non-equilibrium Green's function approach.

6.3 Concluding Remarks

Future research for TFETs most likely must address these challenges and more in order to present statistically significant experimental results. Additionally, this field in general is in dire need of co-fabricated complementary TFETs that outperform complementary MOSFETs on some level. Since the field of semiconductor device research is often tied to the semiconductor industry, compelling results are often those where industry (and presumably the consumer) stand to benefit.

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Appendix A

Appendix: Process Flow Template

A general template for a TFET process flow is included in this appendix. Process steps are specific to the UC Berkeley Microlab and UC Berkeley Nanolab.

Step	Process Name	Process Specification	Equipment	Comment
1.00	SOI wafers	6 inch prime SOI wafers		Tsi = 100nm
1.01	labeling	Label with diamond scribe		
1.02	SOI thickness measurement	All wafers	nanoduv	Tbox = 200nm
		Tsoi Thinning		
1.03	preclean	piranha, 120C, 10 min, QDR + SRD	sink6	
1.04	dry oxidation	2DRYOXA, 900C, variable time	tystar2	
1.05	oxide strip	piranha, 120C, 10 min, QDR, 10:1 HF, variable time	sink6	surface dewets
1.06	SOI thickness measurement	If Tsoi is too large, repeat dry oxidation process	nanoduv	Tsoi = 25-45nm
		PM Marks (Necessary for ASML Alignment)		
2.00	preclean	piranha, 120C, 10 min, QDR + SRD	sink6	
2.01	PR coat	HMDS prime + DUV PR, recipes 1/2/1	svgcoat6	
2.02	litho	combi reticle mask; 22 mJ/cm2, std foc	asml	
2.03	develop	PEB + DUV develop recipe 1/1	svgdev6	
2.04	inspect		uvscope	
2.05	hard bake	recipe U	uvbake	
2.06	PM etch	etch Tsoi ~1200 A target timed etch	lam8	
2.07	PR ash	standard recipe (250C/2.5 min)	matrix	
2.08	clean	piranha, 120C, 10 min, QDR + SRD	sink8	
2.09	test PM marks	coat with PR, run active exposure for alignment test	asml	record wafer quality
2.10	PR ash	standard recipe (250C/2.5 min)	matrix	
		Active Area Definition		
3.00	clean	piranha, 120C, 10 min, QDR + SRD	sink8	
3.01	PR coat	HMDS prime + DUV PR, recipes 1/2/1	svgcoat6	
3.02	litho	device group active mask; variable energy/focus	asml	
3.03	develop	PEB + DUV develop recipe 1/1	svgdev6	
3.04	inspect		uvscope	
3.05	hard bake	recipe U	uvbake	
3.06	active etch	target etch thickness is Tsoi + 30% over etch	lam8	
3.07	PR ash	standard recipe (250C/2.5 min)	matrix	
3.08	inspect		uvscope	
3.09	inspect	profilometry	asiq	
3.10	inspect	Tbox and Tsoi	nanoduv	
3.11	clean	piranha, 120C, 10 min, QDR + SRD	sink8	
		Gate Stack Formation		
4.00	preclean	piranha, QDR, 25:1 fresh HF (right side, ~10s), QDR, SRD	sink6	

4.01	gate oxidation	1GATEOXA; 850C for 70 sec; 11' to ramp to 900C; 20' anneal at 900C	tystar1	sandwich with dummies
4.02	poly-si deposition	10SDPLYA; 3 hrs 37 min; target 150nm	tystar10	sandwich with LTO dummies
4.03	inspect	tystar1 dummy for tox	sopra	tox ~ 3nm
4.04	inspect	tystar1 dummy for Dit	sca	Dit quite variable
4.05	inspect	tystar10 dummy for tpoly	nanoduv	tpoly ~150 nm
		Gate Definition		
5.00	preclean	piranha, 120C, 10 min, QDR + SRD	sink8	
5.01	PR coat	HMDS prime + DUV PR, recipes 1/2/1	svgcoat6	
5.02	litho	device group gate mask; variable energy/focus	asml	
5.03	develop	PEB + DUV develop recipe 1/1	svgdev6	
5.04	inspect		uvscope	
5.05	hard bake	recipe U	uvbake	
5.06	gate etch	target etch thickness is tpoly + 30% over etch	lam8	
5.07	inspect	ensure poly is gone	uvscope	
5.08	inspect	measure Tbox	nanoduv	
5.09	PR ash	standard recipe (250C/2.5 min)	matrix	
5.10	clean	piranha, 120C, 10 min, QDR + SRD	sink8	
		Spacer Definition		
6.00	preclean	piranha, QDR, 25:1 HF (right side, <10s), QDR, SRD	sink6	
6.01	re-oxidation	1GATEOXA; 850C for 70 sec; 11' to ramp to 900C; 20' anneal at 900C	tystar1	sandwich with dummies
6.02	SiN deposition	9SNITA, 3 min 10 sec, target 15nm	tystar9	sandwich with LTO dummies
6.03	inspect	measure tox on a tystar1 dummy	sopra	
6.04	inspect	measure tSiN on a tystar9 dummy	nanoduv	
6.05	spacer etch	etch tSiN target thickness + 10-20% over etch	centura-mxp	oxide left on top of Si
		Asymmetric Source Implant		
7.00	clean	piranha, 120C, 10 min, QDR + SRD	sink8	
7.01	PR coat	HMDS prime + DUV PR, recipes 1/2/1	svgcoat6	
7.02	litho	device group TFET mask source; variable energy/focus	asml	
7.03	develop	PEB + DUV develop recipe 1/1	svgdev6	
7.04	inspect		uvscope	
7.05	hard bake	recipe U	uvbake	
7.06	CoreSystems	Dose 1.5E15/cm2; 20 keV; tilt = 7 for As	send out	
7.07	PR ash	standard recipe (250C/2.5 min)	matrix	
7.08	clean	piranha, 120C, 10 min, QDR + SRD	sink8	

7.09	preclean	piranha, 100:1 HF for 10 s	sink6	
7.10	SPER	2LTANNLA; load at 400C; 550C/4hrs; unload at 375C	tystar2	
		2nd Spacer (with LTO)		
8.00	preclean	piranha, 100:1 HF for 10 s	sink6	
8.01	LTO deposition	11SULTOA for 2' 15", target is 35nm	tystar11	sandwich with dummies
8.02	inspect	measure tystar11 dummy for tLTO	nanoduv	
8.03	spacer etch	MXP-OX-VAR; 9.5 sec (ER ~30.5 A/s); 60/120sccm CH3F/Ar; 200 mT; 500W	centura-mxp	
		Asymmetric Drain Implant		
9.00	PR coat	HMDS prime + DUV PR, recipes 1/2/1	svgcoat6	
9.01	litho	device group TFET mask source; variable energy/focus	asml	
9.02	develop	PEB + DUV develop recipe 1/1	svgdev6	
9.03	inspect		uvscope	
9.04	hard bake	recipe U	uvbake	
9.05	CoreSystems	Dose 5E15/cm2; 10 keV; tilt = 7 for B	send out	
9.06	PR ash	standard recipe (250C/2.5 min)	matrix	
9.07	clean	piranha, 120C, 10 min, QDR + SRD	sink8	
9.08	preclean	piranha, 100:1 HF for 10 s	sink6	
9.09	SPER	2LTANNLA; load at 400C; 550C/4hrs; unload at 375C	tystar2	
		Dopant Activation		
10.00	preclean	piranha, 100:1 HF for 10 s	sink6	
10.01	RTA	variable: 900-1050C for 15-45 sec	heatpulse4	