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Towards Chirality-Encoded Domain Wall Logic

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Non-volatile logic networks based on spintronic and nanomagnetic technologies have the potential to create high-speed, ultra-low power computational architectures. In this article, we explore the feasibility of "chirality-encoded domain wall logic", a nanomagnetic logic architecture where data is encoded, transported and processed by the chiral structures of domain walls in networks of ferromagnetic nanowire. We use high resolution magnetic imaging to test two critical functionalities: the inversion of domain wall chirality at tailored artificial defect sites (logical NOT gates) and the chirality-selective output of domain walls from 2-in-1-out nanowire junctions (common operation to AND/NAND/OR/NOR gates). Our results demonstrate both operations can be performed to a good degree of fidelity even in the presence of complex magnetisation dynamics that would nominally be expected to destroy chirality-encoded information. Together, our results represent a strong indication of the feasibility of devices where chiral magnetisation textures are used to directly carry, rather than merely delineate, data.

As CMOS approaches the limits of its scaling potential there is substantial interest in exploring emerging devices that could either replace CMOS, or work alongside it in heterogeneous systems targeted at overcoming specific limitations of existing hardware [1].

Nanomagnetic and spintronic devices are considered promising "Beyond-CMOS" technologies due to their fast operating speeds, non-volatile nature and well-developed routes to reading and writing data [1]. Motivated by this, there have been a variety of proposals to create spintronic logic networks. Most prominent amongst these have been nanomagnetic logic/quantum cellular automata networks in which data are represented by the magnetisation states of individual, bistable magnetic islands. These are placed in complex geometric arrangements such that dipolar interactions between elements implement logic operations and propagate data through the network [2,3]. There have also been proposals to create logic networks from magnetic tunnel junctions (MTJ) of the type used in commercially available magnetic random access memory (MRAM) chips [4]. In these devices signals are propagated by either spin [5] or conventional electrical currents [6], and logical operations performed by the switching of the MTJ's layer configurations.

In the devices described above, the magnetisation states of discrete magnetic elements are used to represent data, an approach broadly equivalent to that utilised for data storage in MRAM. However, other proposed logic devices are more closely related to the approach of racetrack memory [7–9], where data are encoded along the length of continuous magnetic nanowires. For example, in magnetic domain wall logic (DWL), data streams are encoded by the positions of domain walls (DWs) along soft ferromagnetic nanowires [10]. Rotating magnetic fields drive these domain wall sequences through a variety of junctions to realise logic operations on the data. Similarly, there have been

propositions for nanowire-based logic schemes where trains of skyrmions are used to represent data [11].

In conventional DWL domain walls essentially delineate data, rather than encode it directly. However, in many systems DWs also have an internal degree of freedom, chirality, that could also be used to encode data. In a previous publication we used micromagnetic simulations to demonstrate the feasibility of a logic architecture in which the chirality (clockwise or anticlockwise circulation) of "vortex" type domain walls (VDWs) [12] are used to encode and process data [13]. A later publication by *Vandermeulen et. al.* also showed the feasibility of a similar architecture based on the chirality of transverse domain walls [14].

Chirality-encoded architectures have an important advantage over conventional DWL: In conventional DWL, data cannot be moved entirely coherently due to the half field cycle lag of the motion of head-to-head (H2T, 1-to-0 data transitions) and tail-to-tail (T2T, 0-to-1 data transitions) around the circuits. This makes useful circuit design architecturally challenging. In chirality-encoded logic, where data are carried by a continuous alternating stream of H2H and T2T DWs this is no longer an issue. Chirality-encoded logic also encodes data within the structures of inherently digital magnetic textures with sizes dictated by fundamental length scales of magnetism, making such approaches highly scalable. However, challenges are presented by the fact that DW structures are typically unstable during propagation due to complex Walker breakdown dynamics [15–17], effects that could lead to data loss.

In this paper, we use magnetic imaging experiments to demonstrate the feasibility of two of the critical operations of chirality-encoded logic architectures: Firstly, we demonstrate inversion of a VDW chirality at a defect site; a Logical NOT operation in the proposed architecture. Secondly, we show that in a 2-in-1-out nanowire junction the outputted VDW chirality is controlled by the sequence in which the input nanowires switch. This is a common functionality required for the operation of AND/NAND/OR/NOR gates [13]. Our results are of significance as they have been performed in standard soft magnetic wires composed of $Ni_{80}Fe_{20}$ at fields above Walker breakdown. That these operations are still possible with good fidelity in the presence of complex magnetisation dynamics is a strong indication of the robustness of the approach.

Methods

$Ni_{80}Fe_{20}$ magnetic nanowire devices were fabricated on silicon nitride membranes by electron-beam lithography, thermal evaporation and lift-off processing. Vector network analyser ferromagnetic resonance (VNA-FMR) measurements of equivalent continuous films provided values of saturation magnetisation, M_s = 715 kA/m, Gilbert damping constant , α = 0.02, respectively higher and lower than would be expected for stoichiometric $Ni_{80}Fe_{20}$, suggesting our films were slightly Nickel rich. The film's anisotropy field H_k was found to be negligible. Where required, additional Ti/Au current lines were added via a second lithography, evaporation and lift off step.

Magnetic Transmission X-ray Microscopy (MTXM) imaging of the nanowire devices was performed at beamline 6.1.2 of the Advanced Light Source (ALS). In-plane magnetic fields with amplitudes of up to 1 kOe were applied using an in-situ electromagnet. Where current pulses were required these were provided by an Avtech AVM-4 pulse generator with a maximum pulse length of 5 ns.

Micromagnetic simulations were performed with the mumax[3] simulation package. Material parameters were taken from the VNA-FMR measurements described above, aside from the exchange stiffness, A_{ex} = 13 pJ/m, which was assigned a standard value. For quasi-static simulations the Gilbert damping constant was set to an artificially high value, α = 0.5, while for dynamic simulations it was given the measured value. In simulations of NOT gates, we used cell sizes of 4 x 4 x 5 nm^3, while for the larger-scale (and more computationally demanding) 2-in-1-out junctions we used cell sizes of either 4 x 4 x 40 nm^3 (quasi-static simulations) or 4 x 4 x 10 nm^3 (dynamic simulations). All cell sizes used for dynamic simulations were found to show phenomenologically

similar Walker Breakdown dynamics to those for a 2.5 x 2.5 x 2.5 nm^3 (i.e. fully sub-exchange length) mesh.

NOT Gates

The basic geometry of a NOT gate in the chirality-encoded logic architecture[13] is illustrated schematically in Figure 1(a). The NOT gate consists of a deep, double notch defect, which inverts the chirality of clockwise (CW) VDWs (binary 0) to anticlockwise (ACW) VDWs (binary 1) and vice versa as they are drive through it (Figure 1(b)).

The operating principle of the NOT gates is illustrated using quasi-static micromagnetic simulations in Figures 2(a) & (b), which respectively show ACW and CW VDWs being inverted as an applied field ramp is used to drive DWs through a pair of 135 nm wide/deep notches in a 50 nm thick nanowires. This inversion behaviour can be understood using the topological charge model of DWs, as originally proposed by Tchernyshyov *et. al.*[18]. Within this framework, a VDW is described as a combination of two -½ edge topological charges at the edges of the nanowire, and a single +1 charge at the centre of the vortex (Figure 2). The chirality of the VDW is controlled by the positioning of the -½ charges; if the leading charge lies on the bottom (top) edge of the nanowire the VDW has ACW (CW) chirality. Using Figure 2(a) as an example, one can see that the leading -½ charge of the initial ACW VDW lay at the lower edge of the nanowire. As the DW was pushed through the notch, the nanowire on its left hand side underwent a complex series of vortex and antivortex nucleation/annihilation events (that none-the-less must retained 0 net charge[18]), resulting in switching progressing further on the upper edge of the nanowire than the lower edge. This placed a new, leading -½ charge at the upper edge of the nanowire, such that the outputted VDW was CW. Thus passing VDWs through the notches exchanged the positions of their -½ topological charges, inverting their chiralities.

To demonstrate this behaviour experimentally we fabricated the nanowire device shown in Figure 3(a). The device consisted of a 400 nm wide, 50 nm thick $Ni_{80}Fe_{20}$ nanowire connected to a nucleation pad, and containing a 135 nm depth/width double notch defect at its centre. A 2 µm wide Au/Ti was fabricated directly over the notch.

The experiment proceeded as follows. Beginning with the device saturated along -x, an applied field of H = 100 Oe was used to nucleate VDWs from the pad and move them to the double notch defect. The Au/Ti current prevented imaging of the nanowire beneath it. Thus, to determine the initial VDW chiralities we applied a 20 V pulse to the current line, producing a field along -x, while simultaneously applying a small field of H = -15 Oe. This pushed the VDWs from under the current line and propagated them backwards it until they stopped at intrinsic defects in the nanowire, allowing their initial chirality to be determined. A field of H = +100 Oe was then applied to push the VDW back to the defect site. Finally we applied an inverted 20 V pulse while applying a field H = 15 Oe. Together these pushed the VDWs through the defect site and caused them to pin just beyond the current lines edge, allowing their final chirality to be determined.

Figure 3(b) presents typical MTXM results from obtained from applying this protocol. In the upper image (taken after the first current pulse application), a VDW was present before the current line, with its ACW chirality determinable from the asymmetry in contrast between the lower and upper edges of the nanowire. In the lower image, taken after the VDW had been driven through the notch, a CW VDW was visible just beyond the current line, thus indicating the NOT gate was operating as expected. The experiment described above was repeated a total of 13 times, with only a single anomalous measurement showing VDW chirality to be preserved, rather than inverted.

Figure 3(c) presents further MTXM data in which a VDW was repeatedly toggled back and forth across the NOT gate. Here, the MTXM contrast was produced via dividing the initial configuration, m_1, by the final configuration, m_2, such that the presented images show the change in the magnetisation configuration $\Delta m = m_1/m_2$. The resulting images, which can be understood with the help of the schematic diagrams in the figure, clearly show repeated switching of the VDW chirality over four consecutive toggles. Figure 3(d) plots the toggling of the VDW chirality over a larger

number of experiments; we observed a total of ten successful toggles before an event where chirality was preserved across the gate occurred. Our experimental results thus show the NOT operation to be successfully performed by a double notch defect.

The simulations previously presented in Figure 2 show the operation of the NOT gates under a quasi-static approximation (α = 0.5) and with a globally applied field. To more accurately simulate the nanowires dynamics we performed further simulations with a realistic value of damping (α = 0.02), and with the field from the current line applied over a 2 μm window in the centre of the simulation. As our experimental setup did not allow direct determination of the profile of the pulse in the current line we performed simulations for a relatively large range of feasible field amplitudes (H_{line} = 140 - 290 Oe) and rise/fall times ($t_{rise/fall}$ = 0 - 2.5 ns). Details of how these values were selected can be found in this article's supplementary material.

Figure 4(a) and & (b) present dynamic simulation results for H_{line} = 230 Oe and $t_{rise/fall}$ = 1 ns. While, the observed dynamics were much more complex than in the quasi-static simulations, the results agreed with those observed experimentally, with a ACW DW inverting to CW on moving left-to-right across the notch, and a CW VDW inverting to ACW on moving right-to-left. However, the complexity of the dynamics also appeared to affect the reliability of the process. For example, for the parameters described above, chirality inversion was not observed for an ACW VDW moving right-to-left across the notches. Furthermore, across the full range of simulation parameters studied (see supplementary material), we observed a range of behaviors including chirality recification (i.e. both input chiralities producing the same output), chirality transmission (neither chirality inverting) and the intended inversion process. This suggested the dynamics of the system were highly sensitive. It was therefore surprising that we observed such robust chirality inversion in our experimental measurements. One possible explanation is that the edge roughness of the nanowires, which was not included in the simulations, helps suppress dynamic complexity, as has previously been suggested for the case of free-propagating DWs [19].

2-in-1-out junctions

The operating principles of 2-in-1-out junctions, as used to create chirality AND/NAND/OR/NOR gates is illustrated in Figure 1(c). The key property is that the chirality of the outputted VDW is controlled by the order in which the input wires switch; if the top wire switches first a CW VDW is outputted, while if the bottom wire switches first a ACW VDW is outputted. In full AND/NAND/OR/NOR gates additional notches are added to the top and bottom input nanowires so that the chirality of the inputted VDWs determines their arrival order at the junction[13]. However, in the following we focus on a demonstration of the universal operation of the junctions themselves.

Figure 5(a) presents the results of quasi-static micromagnetic simulations of junctions in 40 nm thick, 400 nm wide nanowires with junction angles of 30°. As expected, the results showed that, independent of the chirality of the inputted VDW, the switching of the first input nanowire resulted in the formation of a transverse DW (TDW) spanning between the centre of the junction and the point where the input nanowire meets the output. The switching of second input nanowire completes the switching of the junction, producing a VDW in the output nanowire. The chirality of the outputted VDW depended on the nanowire switching order as expected; if the top (bottom) nanowire switching first the outputted chirality was CW (ACW).

As for the NOT gates, the behaviour of 2-in-1-out junctions can be understood using the topological charge model of DW structure. Figures 5(b) & (c) show the switching process of the junction in detail. As previously, inputted VDWs consisted of a central +1 charge and two -½ edge charges. As the first VDW reached the junction (Figure 5(b)) the central +1 charge annihilated the upper -½ charge, leaving a +½ charge at the centre of the junction and a -½ charge at the point where the input nanowire met the output, thus creating a TDW. As the second VDW approached the junction

(Figure 5(c)), a complex series of vortex nucleation/annihilation events occurred where the moving charges of the VDW combined with the static -½ charge at the junction to create new +1 and -½ charges. These respectively formed the core and trailing -½ edge charge of a new VDW in the output wire. The leading -½ charge of the outputted VDW was that of the previously deposited TDW, and as this lay on the lower edge of the output nanowire, the outputted VDW had ACW chirality. Hence, the switching order of the input nanowires determined the positioning of the leading edge charge in the outputted VDW, and thus its chirality.

To demonstrate this behaviour experimentally we fabricated nanowire devices of the design shown in figure 6(a). The devices consisted of a 2-in-1-out junction with nucleation pads attached to each of the input nanowires to act as sources of DWs. Double notch defects with depths of 130 nm and widths of 160 nm were placed ~2 μm after the junction to pin the outputted VDWs, such that their chiralities could be determined. In some devices, a single notch was added into one of the input nanowires to try and modify the input switching sequence, although in practice the stochastic nature of DW pinning[20,21] meant these perturbed rather than strictly determined this. The nanowires' width, thickness and junction angle were as in the previously described simulations.

Figure 6(b) presents the results of an example MTXM imaging experiment on the 2-in-1-out junctions. Here, both the junction and output notches were imaged while the applied field was ramped, such that both the switching order of the input nanowires, and the chirality of the outputted VDWs could be observed. For example, in the results shown in Figure 6(b), the bottom input switched first, forming the expected TDW across the end of the input nanowire. This was followed by switching of the top input, resulting in the propagation of an ACW VDW to the output notches.

Figure 6(c) presents further data showing all four of the possible input switching/output chirality combinations, as observed from a single device with no notches in its input nanowires. As expected, these results did not manifest with equal probability: Across 18 total measurements we observed 10 occurrences where the top input switched first; these favoured CW over ACW output by a factor 8:2. In the remaining 8 events, where bottom input switched first, ACW output was favoured by a factor 7:1. Thus, the device strongly favoured the behaviours predicted by the quasi-static simulations. To confirm this was a property of the junctions we performed a total of 67 measurements across 6 different devices. The results of these measurements are summarised in Figure 6(d), and clearly show the strong correlation between input switching order and output chirality. Full details of the results from each device measured can be found in this article's supplementary material.

To gain understanding of the minority of events where the output VDW chirality was not correlated to the input nanowire switching order we performed dynamic simulations of the junction's behaviours. Figure 7(a) presents example results for the switching of the first (in this case lower) input nanowire via the propagation of a CW VDW at H = 105 Oe. This field was lower than those in the experimental measurements, as for higher fields the DW propagated straight through the junction without stopping. We suggest that nanowire edge roughness assisted pinning in the experimental measurements, and note that the applied field in the simulation was still substantially above the Walker breakdown field (~20 Oe in the measured/simulated nanowires[20]. The DW behaved as observed in the experiments and quasi-static simulations, forming a TDW across the junction between the input and output nanowires. Equivalent behaviour was observed for all permutations of which input switched first and input VDW chirality.

More complex behaviour was observed for the switching of 2nd input nanowire. Figures 7(b) & (c) contrast the dynamics observed for the switching of the second (top) input at two applied fields, H = 105 and 95 Oe. The Walker breakdown dynamics of the two simulations were broadly similar during the switching of the top input wire, but diverge substantially as the DWs reached the output nanowire; while the simulation for H = 105 Oe formed the expected ACW VDW, that at H = 95 Oe

formed a CW VDW. The results of further simulations performed for fields in the range H = 85 - 110 Oe are summarised in this articles supplementary material. Each of these showed similar results, such that for a given field some combinations of input nanowire and chirality would produce the expected output, while others would not. We note that the field amplitude here was primarily used to as a handle with which to explore variations in the Walker breakdown dynamics. In real devices similar variations in dynamics would be produced by thermal perturbations, even for a single well defined applied field [22].

The results above indicate that complex Walker breakdown dynamics can cause the operation of 2-in-1-out junctions to break down. However, much like for the NOT gates, the experimental devices were more reliable than would be anticipated from the complex, dynamical simulations. We again suggest that edge roughness may play a role in simplifying DW dynamics[19] such that the replicate the functionality observed in quasi-static simulations with to a reasonable level of reproducibility.

Conclusions

In this paper we have used magnetic imaging and micromagnetic simulations to demonstrate the feasibility of two functions critical to the operation of chirality-encode domain wall logic: the inversion of VDW chirality by a double notch defect (NOT gate) and the control of output VDW chirality in 2-in-1-out junctions (essential for AND/NAND/OR/NOR gates).

Our experimental results were found to reproduce the basic functionality observed in quasi-static simulations, with a modest number (<20 %) of anomalous events. We attribute these to complex Walker-breakdown dynamics, which are capable of flipping the chirality of VDWs [15–17,22]. Interestingly, the results of our experiments lay closer to those expected from the quasi-static simulations, than from true dynamical simulations, perhaps suggesting that nanowire edge roughness had an inhibiting effect on the complexity of DW dynamics [19]. However, that the required functionalities could be observed with a good degree of reliability even in systems with low damping is an excellent indicator of the feasibility of chirality-encoded logic schemes. Further improvements in device reliability could be achieved by manipulation of the nanowires' damping constant to further simplify DW dynamics, e.g. by doping with rare-earth materials such as Ho or Tb [23–25]. As we have shown in a previous paper[26], this would also allow for deterministic pinning at artificial defect sites, which is the final function required to fully realise AND/NAND/OR/NOR gates.

Further work will certainly be required to realise full chirality-encoded logic circuits. However, our work provides a promising foundation for experimental investigations into the remaining elements required to create these (e.g. FAN-OUT, cross-over elements). We note that the functionality of 2-in-1-out junctions also offer a clear route to writing chirality-encoded data into devices, while an inversion of this structure has already been shown to be an excellent detector of chirality [27]. Another important question is whether similar functionality can be realised in materials systems where DWs can be driven efficiently by spin-torque. This is an interesting challenge, as in the current state of the art, where DWs are driven by the spin hall effect, DW chirality is no longer a degree of freedom [28–30]. Nevertheless, our results represent a substantial step along the road to realise logic networks where information is carried, rather than merely delineated, by magnetic domain walls.

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1. International Technology Roadmap for Semiconductors (ITRS). *Beyond CMOS*. *Itrs* (2015).

2. Cowburn, R. P. Room Temperature Magnetic Quantum Cellular Automata. *Science*

(80-.). (2000). doi:10.1126/science.287.5457.1466

3. Imre, A. *et al.* Majority logic gate for magnetic quantum-dot cellular automata. *Science (80-.).* (2006). doi:10.1126/science.1120506

4. Kent, A. D. & Worledge, D. C. A new spin on magnetic memories. *Nature Nanotechnology* (2015). doi:10.1038/nnano.2015.24

5. Behin-Aein, B., Datta, D., Salahuddin, S. & Datta, S. Proposal for an all-spin logic device with built-in memory. *Nat. Nanotechnol.* (2010). doi:10.1038/nnano.2010.31

6. Ney, A., Pampuch, C., Koch, R. & Ploog, K. H. Programmable computing with a single magnetoresistive element. *Nature* (2003). doi:10.1038/nature02014

7. Parkin, S. S. P., Hayashi, M. & Thomas, L. Magnetic domain-wall racetrack memory. *Science* (2008). doi:10.1126/science.1145799

8. Parkin, S. & Yang, S. H. Memory on the racetrack. *Nature Nanotechnology* (2015). doi:10.1038/nnano.2015.41

9. Fert, A., Cros, V. & Sampaio, J. Skyrmions on the track. *Nature Nanotechnology* (2013). doi:10.1038/nnano.2013.29

10. Allwood, D. A. *et al.* Magnetic domain-wall logic. *Science* (2005). doi:10.1126/science.1108813

11. Zhang, X., Ezawa, M. & Zhou, Y. Magnetic skyrmion logic gates: Conversion, duplication and merging of skyrmions. *Sci. Rep.* (2015). doi:10.1038/srep09400

12. McMichael, R. D. & Donahue, M. J. Head to head domain wall structures in thin magnetic strips. *IEEE Trans. Magn.* (1997). doi:10.1109/20.619698

13. Omari, K. A. & Hayward, T. J. Chirality-based vortex domain-wall logic gates. *Phys. Rev. Appl.* (2014). doi:10.1103/PhysRevApplied.2.044001

14. Vandermeulen, J., Van De Wiele, B., Dupré, L. & Van Waeyenberge, B. Logic and memory concepts for all-magnetic computing based on transverse domain walls. *J. Phys. D. Appl. Phys.* (2015). doi:10.1088/0022-3727/48/27/275003

15. Schryer, N. L. & Walker, L. R. The motion of 180° domain walls in uniform dc magnetic fields. *J. Appl. Phys.* (1974). doi:10.1063/1.1663252

16. Lee, J. Y., Lee, K. S., Choi, S., Guslienko, K. Y. & Kim, S. K. Dynamic transformations of the internal structure of a moving domain wall in magnetic nanostripes. *Phys. Rev. B - Condens. Matter Mater. Phys.* (2007). doi:10.1103/PhysRevB.76.184408

17. Kim, S. K., Lee, J. Y., Choi, Y. S., Guslienko, K. Y. & Lee, K. S. Underlying mechanism of domain-wall motions in soft magnetic thin-film nanostripes beyond the velocity-breakdown regime. *Appl. Phys. Lett.* (2008). doi:10.1063/1.2968138

18. Tchernyshyov, O. & Chern, G. W. Fractional vortices and composite domain walls in

flat nanomagnets. *Phys. Rev. Lett.* (2005). doi:10.1103/PhysRevLett.95.197204

19. Nakatani, Y., Thiaville, A. & Miltat, J. Faster magnetic walls in rough wires. *Nature Materials* (2003). doi:10.1038/nmat931

20. Hayward, T. J. & Omari, K. A. Beyond the quasi-particle: Stochastic domain wall dynamics in soft ferromagnetic nanowires. *J. Phys. D. Appl. Phys.* (2017). doi:10.1088/1361-6463/aa553f

21. Omari, K. A. & Hayward, T. J. A Micromagnetic Protocol for Qualitatively Predicting Stochastic Domain Wall Pinning. *Sci. Rep.* (2017). doi:10.1038/s41598-017-17512-w

22. Hayward, T. J. Intrinsic Nature of Stochastic Domain Wall Pinning Phenomena in Magnetic Nanowire Devices. *Sci. Rep.* (2015). doi:10.1038/srep13279

23. Bailey, W., Kabos, P., Mancoff, F. & Russek, S. Control of magnetization dynamics in Ni81Fe19 thin films through the use of rare-earth dopants. *IEEE Trans. Magn.* (2001). doi:10.1109/20.950957

24. Rebei, A. & Hohlfeld, J. Origin of increase of damping in transition metals with rare-earth-metal impurities. *Phys. Rev. Lett.* (2006). doi:10.1103/PhysRevLett.97.117601

25. Woltersdorf, G., Kiessling, M., Meyer, G., Thiele, J. U. & Back, C. H. Damping by slow relaxing rare earth impurities in Ni80Fe20. *Phys. Rev. Lett.* (2009). doi:10.1103/PhysRevLett.102.257602

26. Broomhall, T. J. & Hayward, T. J. Suppression of Stochastic Domain Wall Pinning Through Control of Gilbert Damping. *Sci. Rep.* (2017). doi:10.1038/s41598-017-17097-4

27. Pushp, A. *et al.* Domain wall trajectory determined by its fractional topological edge defects. *Nat. Phys.* (2013). doi:10.1038/nphys2669

28. Haazen, P. P. J. *et al.* Domain wall depinning governed by the spin Hall effect. *Nat. Mater.* (2013). doi:10.1038/nmat3553

29. Emori, S., Bauer, U., Ahn, S. M., Martinez, E. & Beach, G. S. D. Current-driven dynamics of chiral ferromagnetic domain walls. *Nat. Mater.* (2013). doi:10.1038/nmat3675

30. Ryu, K. S., Thomas, L., Yang, S.-H. & Parkin, S. S. P. Chiral spin torque at magnetic domain walls. *Nat. Nanotechnol.* (2013). doi:10.1038/nnano.2013.102

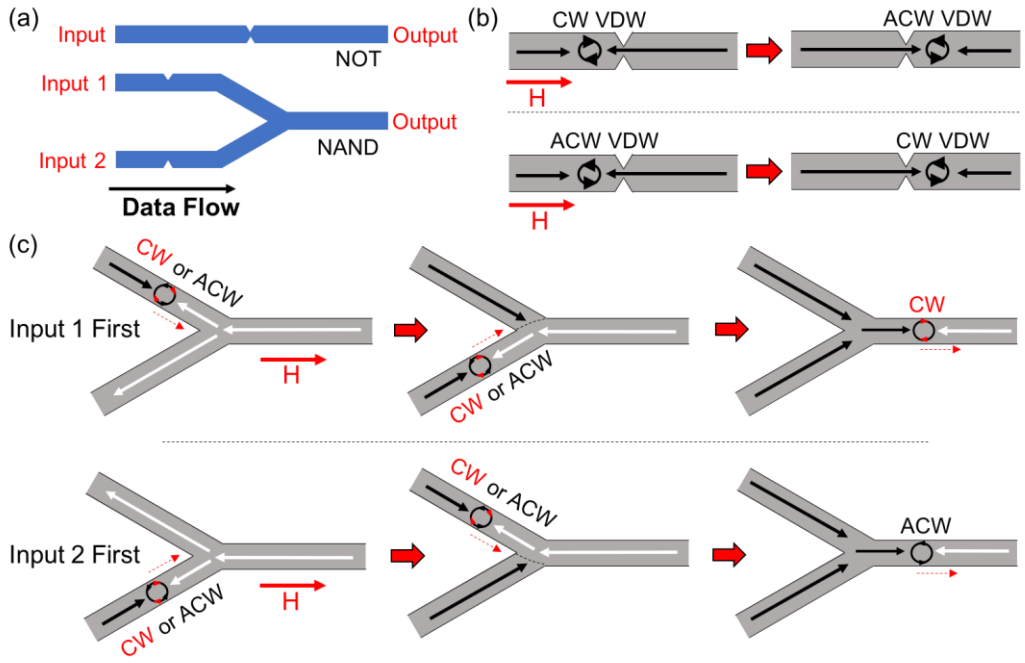

Figure 1: (a) Schematic diagrams illustrating the geometry of NOT and NAND gates in chirality encoded domain wall logic schemes. (b) Illustration of the operating principle of the NOT gates; as the domain walls pass through the double notch defect their chiralities are inverted. (c) Illustration of the operating principle of the 2-in-1-out junctions in AND/NAND/OR/NOT gates; the chirality of the domain wall in the output wire is determined by the switching order of the input nanowires.

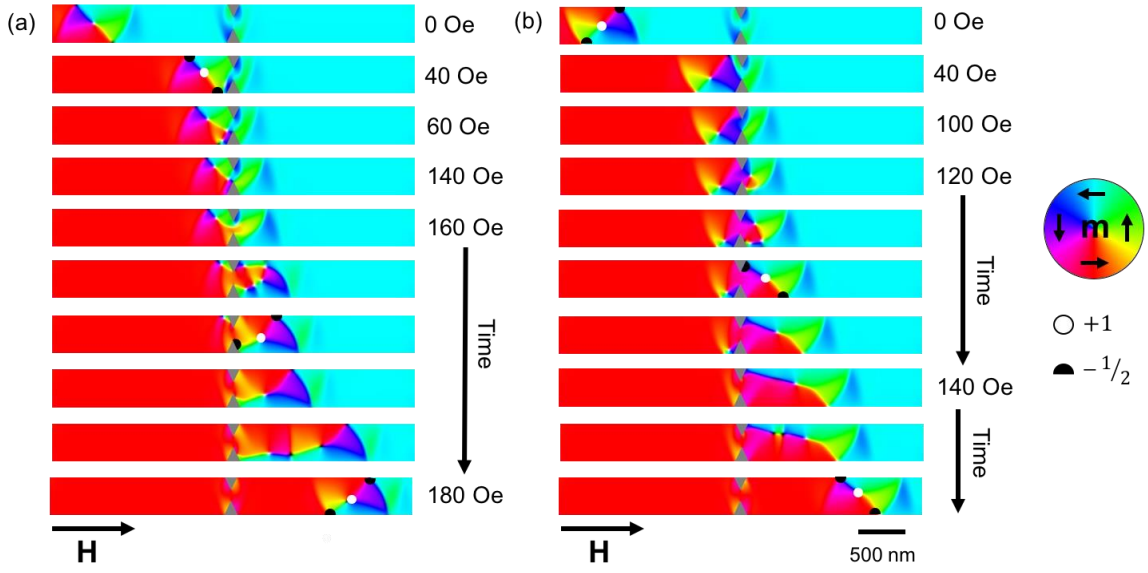

Figure 2: Quasistatic micromagnetic simulations showing the operation of a NOT gate in a 400 nm wide, 50 nm thick nanowire. The notches each had depths and widths of 135 nm (a) an initial ACW VDW is inverted to a CW VDW (b) an initial CW VDW is inverted to a ACW VDW. In some images symbols are used to represent the locations of topological charges in accordance with the key on the right of the figure.

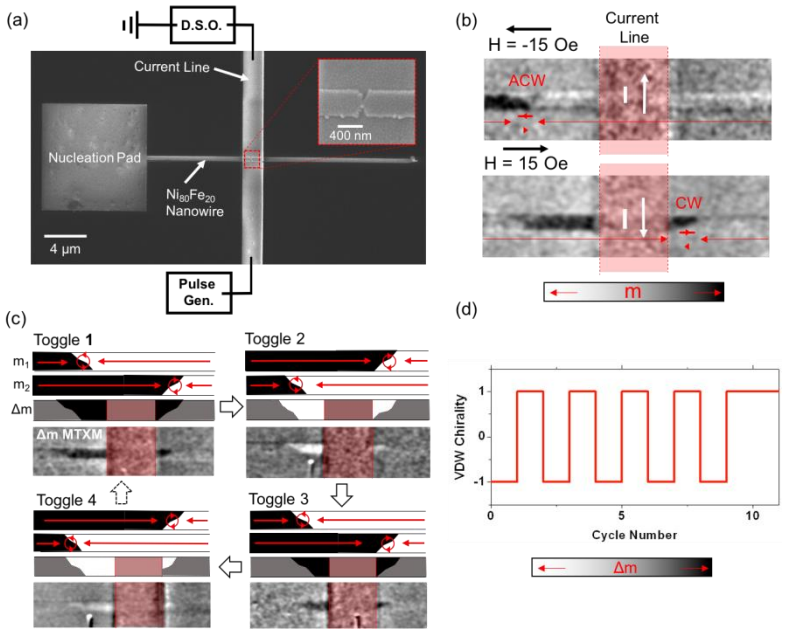

Figure 3: (a) SEM image of the NOT gate device. The inset figure shows an expanded image of the notched region (viewed through the gold current line). (b) MTXM images showing an ACW VDW being inverted to CW chirality on being passed through the double notches. The shaded red region represents the location of the current line, which obscures magnetic contrast. (c) Series of four MTXM images illustrating the toggling of a VDWs chirality as it is passed back and forth across the double notches. Contrast here was created by dividing the initial image (m_1) by the final image (m_2) resulting in an image of $\Delta m = (m_1/m_2)$. Schematic diagrams are provided above the MTXM images to assist the reader's interpretation of the contrast. (d) Plot showing how the chirality (CW = 1, ACW = -1) of a VDW varied for 10 passages back and forth across the notches.

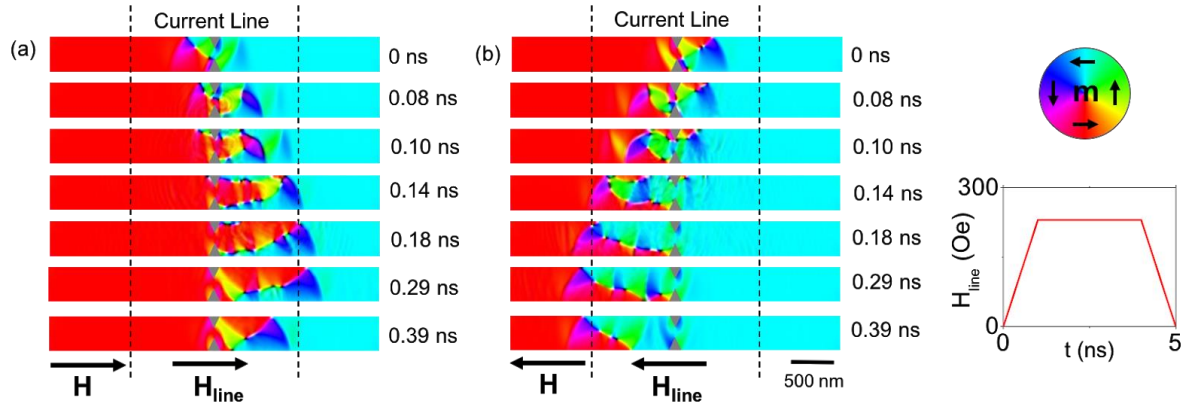

Figure 4: Dynamic micromagnetic simulations of VDWs passing through a NOT gate in a 400 nm wide, 50 nm thick nanowire. The notches each had depths and widths of 135 nm. (a) ACW VDW passes left-to-right through notches. (b) CW VDW passes right-to-left through the notches. The simulated field from the current line was localised between the two dashed lines and had the profile shown in the plot on the right of the figure (H_{line} = ±230 Oe and $t_{rise/fall}$ = 1 ns). A uniform field of H = ±15 Oe was also applied to emulate the externally applied field in the experimental measurements.

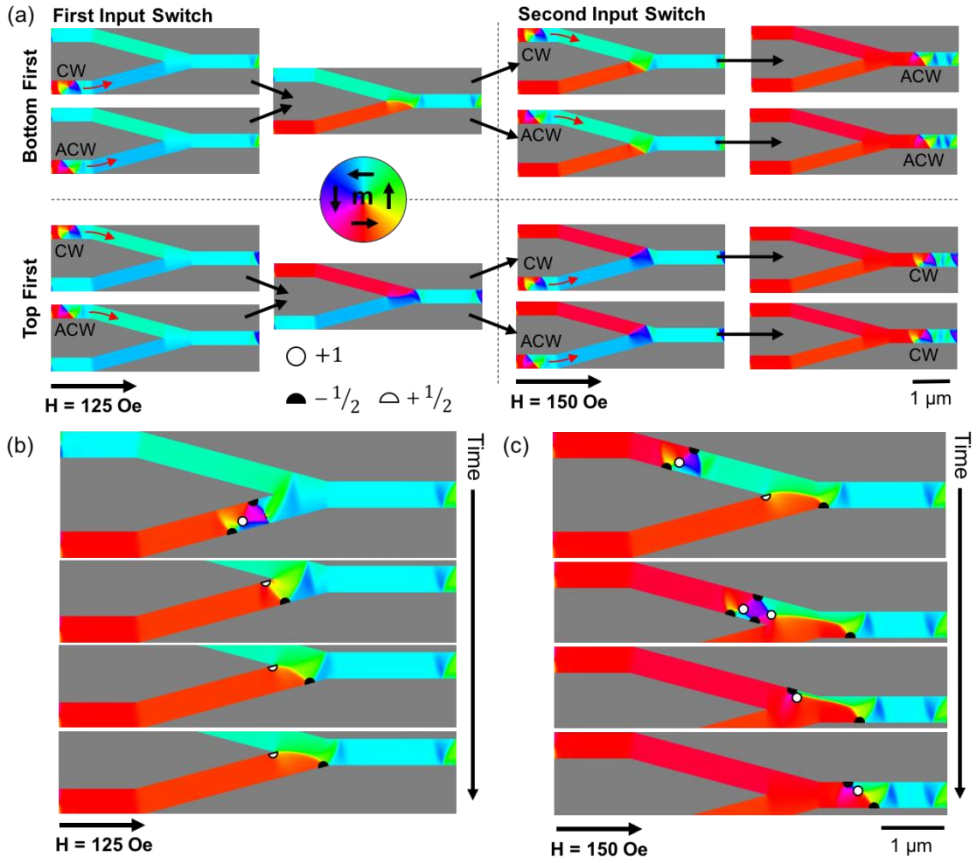

Figure 5: (a) Results of quasi-static micromagnetic simulations showing the various switching paths available for a 2-in-1-out junction. The input and output nanowires all had widths of 400 nm and thicknesses of 40 nm. (b) Detailed images showing the interaction of a CW VDW with the junction during the switching of the first (bottom) input nanowire. (c) images showing the interaction of a CW VDW with the junction during the switching of second (top) nanowire. in (b) & (c) the locations of topological charges are indicated with symbols in accordance with the key in the centre of the figure.

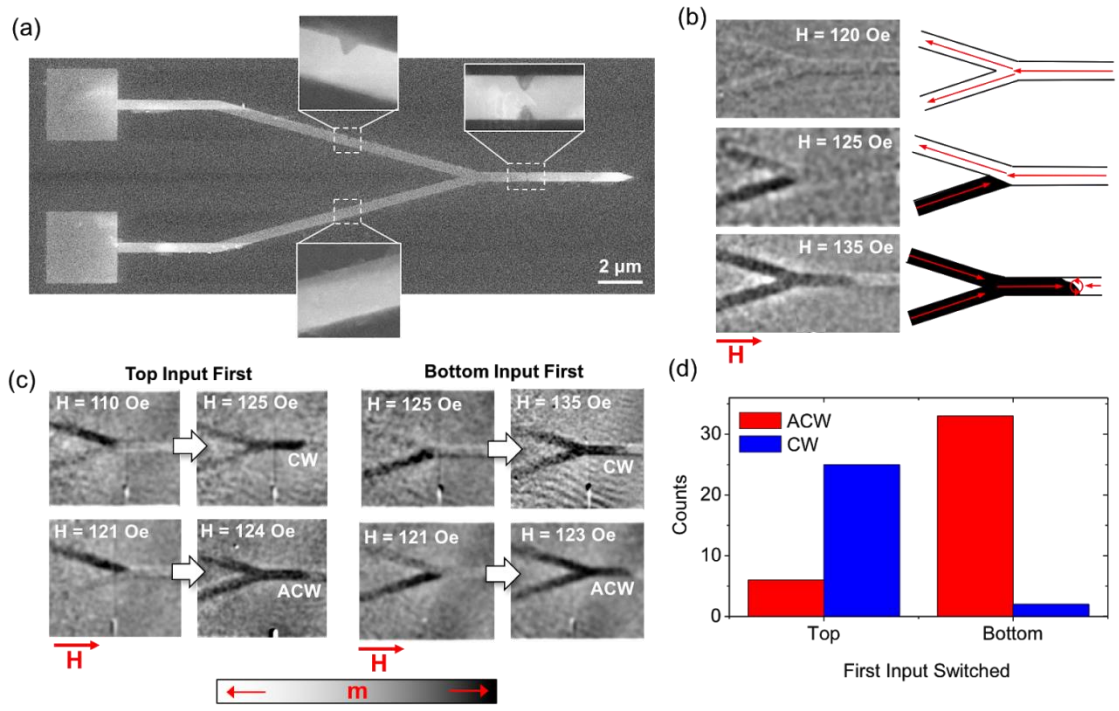

Figure 6: (a) SEM images showing one of the 2-in-1-out junctions measured in this study. The inset figures show the notched regions of the nanowires in detail. For the device shown only the top of two the input nanowires contained a notch. (b) Example MTXM images showing the switching of a 2-in-1-out junction as the applied field was ramped. In this case the bottom input switched first, followed by the top input resulting in an ACW VDW at the output notches. (c) MTXM images illustrating the four possible switching paths for the 2-in-1-out junctions as observed a in single device. (d) Distribution of switching paths observed over a total of 67 measurements across 7 different devices.

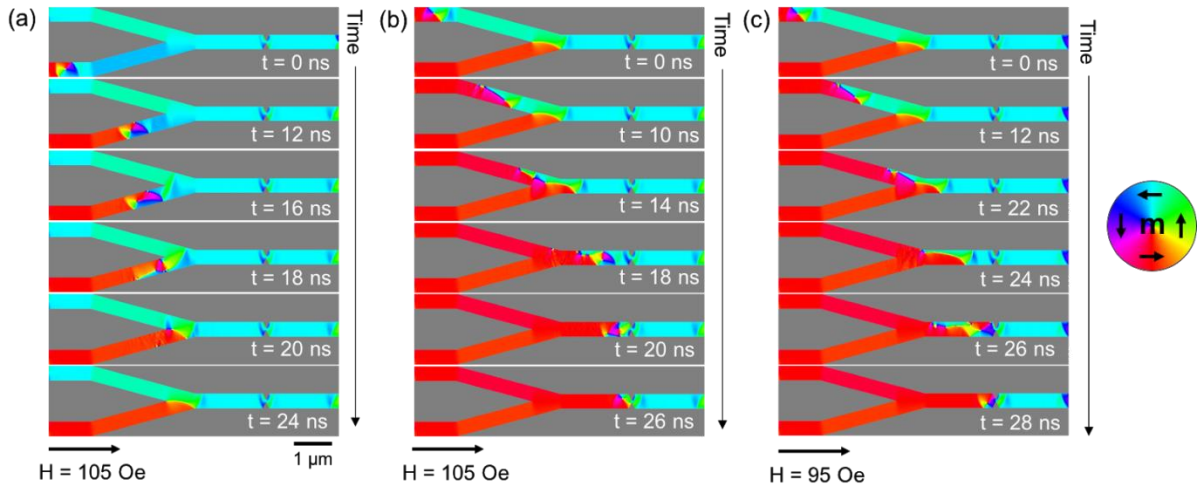

Figure 7: Dynamic micromagnetic simulations of the switching of 2-in-1-out junctions. The input and output nanowires all had widths of 400 nm and thicknesses of 40 nm. (a) Switching of the first (bottom) input by a CW VDW at H = 105 Oe. (b) Switching of the second (top) input by a ACW VDW at H = 105 Oe. (c) Switching of the second (top) input by a ACW VDW at H = 95 Oe.

Supplementary Material

I. Estimation of field from current line in NOT gate experiment

In the experimental measurements of the NOT gates, the magnitude and profile of the current pulse (which was short with respect to the cable lengths) through the current line was not measured directly. We therefore estimated the strength of the applied field pulse as follows:

A 20 V pulse was produced at the 50 Ω output impedance of the pulse generator, resulting in an approximate peak input power P_{in} = 8 W injected into the impedance matched cables. Assuming that the impedance of the strip line was dominated by its 330 Ω resistance we can estimate the amplitude of the reflected voltage pulse using the scattering parameter:

$$S_{11} = \frac{Z_L - Z_S}{Z_L + Z_S}$$

Where the load impedance, Z_L = 330 Ω and the source impedance, Z_S = 50 Ω. For these values we calculate S_{11} = 0.74, such that a 14.8 V pulse propagates back through the system, dissipating 4.4 W into the pulse generators output impedance. At the oscilloscope's 50 Ω input impedance we observe a ~10 V pulse, accounting for a further 2 W of power. We assume that the remaining 1.6 W of power is dissipated resistively in the current line, suggesting a peak current of 73 mA. At the current line's lines surface this is expected to produce a field:

$$H_{line} = \frac{I}{2w}$$

where w = 2 μm is the current line width. From this we estimate a peak field of H_{line} = 230 Oe. Due to the uncertainty in how reflections in the system affect the pulse profile we perform simulations for a large range of fields around this value (H_{line} = 140 – 230 Oe) and for profiles ranging from a rectangular pulse ($t_{rise/fall}$ = 0 ns) to a triangular pulse ($t_{rise/fall}$ = 2.5 ns).

II. **Results of dynamic NOT gate simulations**

The tables below summarise the results of dynamic micromagnetic simulations for all values of H_{line} and $t_{rise/fall}$. For each set of input parameters simulations were performed for input VDWs with both CW and ACW chirality:

Key: *I = VDW chiralities inverted, T = VDW chiralities transmitted without change, R-CW = VDWs rectified to CW chirality, R-ACW = VDWs rectified to ACW chirality. N = switching not complete.*

VDWs moving left-to-right:

	H_{line} (Oe)					
t_{rise}	**140**	**170**	**200**	**230**	**260**	**290**
0	T	I	R-CW	R-CW	I	R-ACW
0.5	T	I	R-CW	R-CW	R-CW	R-CW
1	T	T	R-CW	I	R-CW	R-CW
1.5	R-ACW	I	R-CW	T	R-CW	R-CW
2	I	R-ACW	R-ACW	R-CW	I	R-CW
2.5	I	I	R-ACW	R-ACW	I	I

VDWs moving right-to-left:

	H_{line} (Oe)					
t_{rise}	**140**	**170**	**200**	**230**	**260**	**290**
0	R-CW	R-CW	R-ACW	I	R-CW	R-CW
0.5	I	R-CW	T	T	R-ACW	I
1	R-CW	R-CW	R-CW	R-ACW	I	R-ACW
1.5	I	I	T	R-ACW	R-ACW	R-ACW
2	R-ACW	I	I	R-CW	R-ACW	R-ACW
2.5	N	R-ACW	I	T	R-CW	R-ACW

III. Results of 2-in-1-out junction measurements

The tables below summarise the data from each of the six 2-in-1-out devices measured.

Device 1:

Output Chirality	First Input to Switch	
	Top	Bottom
CW	0	0
ACW	0	12

Device 2:

Output Chirality	First Input to Switch	
	Top	Bottom
CW	8	1
ACW	2	7

Device 3:

Output Chirality	First Input to Switch	
	Top	Bottom
CW	3	1
ACW	1	7

Device 4:

Output Chirality	First Input to Switch	
	Top	Bottom
CW	4	0
ACW	2	2

Device 5:

Output Chirality	First Input to Switch	
	Top	Bottom
CW	10	0
ACW	1	0

Device 6:

Output Chirality	First Input to Switch	
	Top	Bottom
CW	0	0
ACW	0	6

IV. **Results of Dynamic 2-in-1-out simulations**

The following tables summarise the results of dynamic simulations of the 2-in-1-out devices. Simulations were performed for the switching of the second input wire of the junction, for both input VDW chiralities, and at a range of field amplitudes. Results indicated in **bold** are anomalous i.e. the output chirality did not match that observed in the quasi-static simulations/favoured in the experimental measurements. Where the results is listed as "**pass**" the outputted VDW did not become pinned at the output notch.

H = 85 Oe:

Input VDW Chirality	**Second Input to Switch**	
	Top	**Bottom**
CW	ACW	**Pass**
ACW	ACW	CW

H = 95 Oe:

Input VDW Chirality	**Second Input to Switch**	
	Top	**Bottom**
CW	**CW**	**Pass**
ACW	**CW**	CW

H = 105 Oe:

Input VDW Chirality	**Second Input to Switch**	
	Top	**Bottom**
CW	**CW**	CW
ACW	ACW	**ACW**

H = 110 Oe:

Input VDW Chirality	**Second Input to Switch**	
	Top	**Bottom**
CW	ACW	**ACW**
ACW	ACW	**Pass**