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Design of Ultra-Low Power Amplifier Array in Weak Inversion Region for Electrocortigraphy (ECoG) Signal Acquisition

THESIS

submitted in partial satisfaction of the requirements
for the degree of

MASTER OF SCIENCE

In Electrical and Computer Engineering

by

Akshay Mahajan

Thesis Committee:
Professor Payam Heydari, Chair
Professor Michael Green
Professor Ender Ayanoglu

2015

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DEDICATION

To

My parents

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Lastly, I would like to thank my parents, brother and friends for their constant support throughout my graduate studies.

ABSTRACT OF THE THESIS

Design of an Ultra-Low Power Amplifier Array in Weak Inversion Region for Electrocortigraphy (ECoG) signal acquisition

By

Akshay Mahajan

Master of Science in Electrical and Computer Engineering

University of California, Irvine, 2015

Professor Payam Heydari, Chair

Design and implementation of a novel ultra-low power (ULP) operational transconductance amplifier (OTA) meant for recording Electrocorticography signals is presented in this thesis. The design of the amplifier is done in weak inversion (or sub-threshold) region of operation of MOSFET and was fabricated in IBM 130 nm standard CMOS process. This thesis discusses the design and measurement challenges associated with analog/mixed signal design in this region of operation. The ULP closed loop fully differential OTA is designed for voltage gain of 40 dB for a frequency ranging from 15 Hz to 270 Hz with input referred noise voltage less than 5 uV_{rms} across bandwidth of operation. Total power dissipation for the novel complementary OTA structure designed in weak inversion region is measured to be 216 nW for a supply of 0.4 V.

List of Symbols

ECoG – Electrocorticography

OTA – Operational Transconductance Amplifier

ULP – Ultra Low Power

BCI – Brain Computer Interface

SNR – Signal to Noise Ratio

NEF – Noise Efficiency Factor

PEF – Power Efficiency Factor (PEF = Nef^2 x Supply Voltage)

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

WI – Weak Inversion Region of MOSFET

SI – Strong Inversion Region of MOSFET

MI – Moderate Inversion Region of MOSFET

CMFB – Common Mode Feedback

BW – Bandwidth

k - Boltzmann constant

q - Elementary Charge

T – Absolute Temperature

U_T – Thermodynamic voltage [$U_T = kT/q$, measure of the thermal energy of electrons]

r_o – Intrinsic output resistance of MOSFET

g_m – transconductance

INTRODUCTION

This thesis is part of a long term Brain computer Interface (BCI) project which wishes to acquire High Density (HD) - ECoG signals from brain and ultimately help human kind suffering from spinal cord injury (SCI) and other neurological disorders regain normal bodily activities such as walking. The focus of this thesis is to introduce an ultra-low-power (ULP) Operational transconductance amplifier (OTA) designed for acquiring HD-ECoG signals.

Motivation

- Throughout the world, people suffer from SCI and other neurological disorders where neural connectivity from spinal cord to limbs is affected leading to loss of motor control of limbs.
- [1] Introduces a novel approach of BCI controlled lower extremity prostheses. Compelling evidence and results show that such a technique for restoring brain controlled ambulation post SCI event is feasible.
- Based on [1] and [2], the aim is to capture brain waves through an HD-ECoG which upon use of novel DSP algorithms can identify between states of rest and motion of body/ limbs.
- Upon careful considerations for such HD-ECoG environment and signal characteristics we can identify specifications and challenges of designing a system for BCI control.

Here we designed a system to capture the ECoG signals from a 64-channel electrode grid, providing faithful amplification and multiplex it to a single stream. Meaningful range of frequencies for such signals range from near sub-Hz to 200Hz.

Chapter 1 discusses details of the system and specifications, with a brief introduction of ECoG. An overview and considerations for analog design in Weak Inversion (WI) region of operation of MOSFET is discussed in chapter 2. Chapter 3 and 4 discourses design and measurement of a novel complementary fully differential topology of OTA operating in WI region.

CHAPTER 1: System Overview

In this chapter we talk about the general system architecture on which this research is based. We look at the properties of ECoG signal which was crucial in design considerations. Also briefly discussed is the multiplexer associated digital circuitry which was mainly designed by Alireza Karimi Bidhendi, my peer in this project.

Fig 1 shows the overall system architecture of a typical brain signal acquisition system. An array of 64 low-power low-noise amplifiers are used to boost weak brain signals to acceptable range for processing by later stages. Depending on the designed architecture and application, further amplification may be required before ADC. This can be achieved by using a tunable buffer amplifier. This work revolves around implementation of just the amplifier and multiplexer (MUX) part.

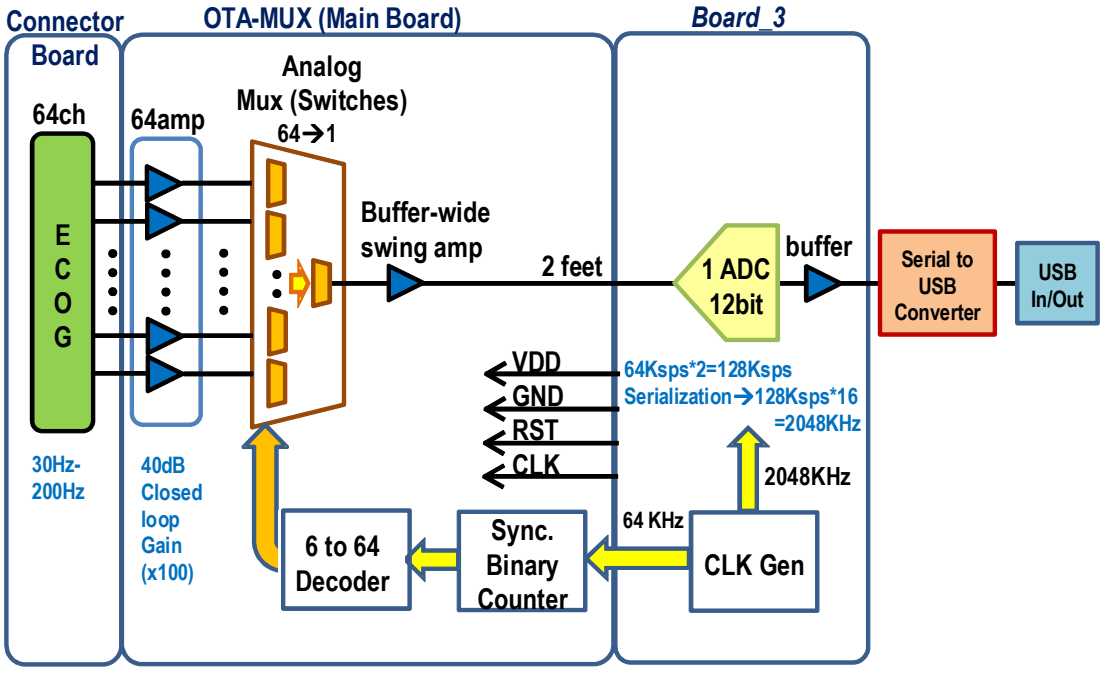

Figure 1: System Overview

Fig 1 also shows specifications for the whole system based on nyquist criteria. For input signal ranging up-to 200 Hz and a time sharing across 64 channels through analog MUX reveals 64 KHz clocking required for 4X sampling compared to nyquist rate (25.6 KHz).

1.1 ECoG considerations

Electrocorticography is considered mildly invasive in nature compared to electroencephalography (EEG) but provides much stronger signals in gamma range (30 – 200 Hz). Therefore, it helps to gain much better insight of brain activity and develop more efficient algorithms for the applications in mind.

Table 1: Characteristics of Electrophysiological Signals [3]

	Bandwidth	**Amplitude**	**Spatial Resolution**	**Invasiveness**
Single-Unit	0.1-7 KHz	< 500 uV	0.2 mm	Invasive
Local Field Potential (LFP)	< 200 Hz	< 5 mV	1 mm	Moderately invasive
Electrocorticography (ECoG)	0.5-200 Hz	< 100 uV	0.5 cm	Moderately invasive
Electroencephalography (EEG)	< 100 Hz	10-20 uV	3 cm	Non-invasive

Table 1 shows signal characteristics of different electrophysiological signals comparing their BW, amplitude, invasiveness and spatial resolution. As expected there is a trade-off between invasiveness and amplitude of brain waves. Single unit provides the best amplitude but the drawbacks for using this technique for humans are that it is invasive, leads to damage of brain tissue and we get a very poor spatial resolution. For purpose of walking we can detect low gamma and high gamma signals of ECoG ranging beyond 30 Hz to 200 Hz which carry useful information and provide a higher signal amplitudes compared to EEG. Thus ECoG is the best approach when considering all the factors for a viable long term implantable system.

Use of ECoG also imposes some other biomedical constraints on implantable systems. Concerns are the heat dissipation from the system (<1°C in surrounding tissue) and very low power dissipation to support ≥24 hours of battery life in between recharges. The system does not need to be designed for a wide range of temperature change which becomes obvious considering near constant temperature of human body.

1.2 Multiplexer (MUX) design

This section briefly discusses MUX design and considerations for this system. From fig 1, for satisfying the nyquist sampling rate criteria for 64 channels, 64 KHz clock frequency has been chosen for serializer circuitry. Although for minimizing the power, which is the primary target of this research, minimum size transistors could be used [6], slightly larger sizes were chosen to mitigate the non-ideal effects of operating in weak inversion (especially threshold voltage variation) on functionality, speed, noise margin and driving capability of transistors.

The analog MUX in fig 1 is consists of a 6-bit synchronous binary counter, a 6-64 decoder and a 2x64 complementary MOS switches for selecting differential output of amplifiers. These MOS switches are the only components in signal path of system and rest is just peripheral circuitry used for controlling and detecting the channel being used at an instant. Clock feedthrough can be a concern and thus proper sizing of switches should be considered for this phenomenon. In final design, the MOS switches are embedded within the ULP OTA structure.

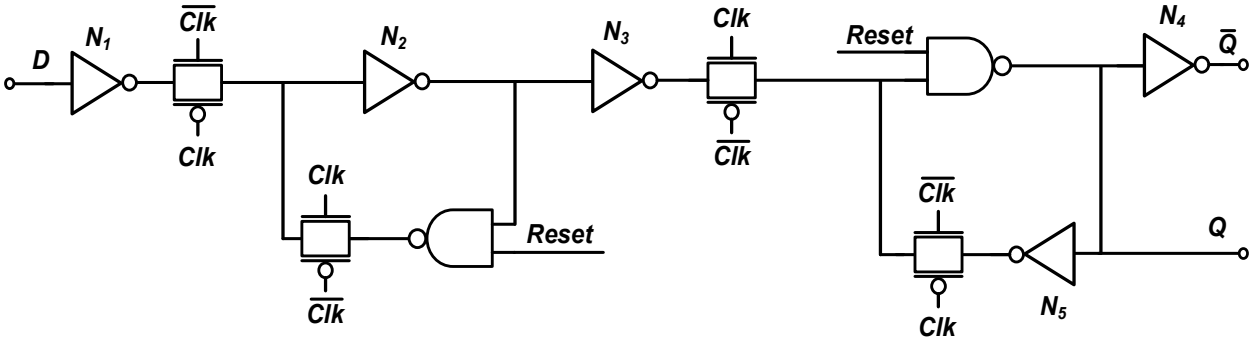

Figure 2: Schematic of Flip flop implemented in synchronous counter (part of serializer)

The generation of complementary clocks for MOS switches can be easily done since time period is much larger than gates delay, even in WI operation. The decoder is built by using four 4 to 16 dual-tree decoders. Although, asynchronous counter provides lower loading effect on clock path and lower power consumption, it was not chosen because of unwanted transient hazards which can disrupt the multiplexer operation. Counter is built by cascading of 6 Toggle Flip-Flops (TFF). Static flip-flop configuration was used since effect of leakage current on dynamic logic is more severe in WI region of operation. We also have additional sensitivity of WI operated logic circuits to Process Voltage Temperature

(PVT). Minimizing interconnect lengths is necessary to decrease capacitive loading on gates. Fig 2 shows the schematic of master-salve DFF with asynchronous active low reset capability. Reset signal is required to put the circuit in a known state. This structure also avoids stack of more than 3 transistors, guarantying proper operation at low supply voltage.

CHAPTER 2: Weak Inversion (WI) Operation

For our applications of implantable bio-medical devices, low power is of more concern compared to performance in terms of speed. It provides a good solution for longer battery life and low heat generation. Use of MOS in WI region of operation instead of strong inversion (SI) serves this purpose well but adds its own challenges which we will walk through in this chapter.

2.1 Brief history

Over the years, focus has shifted to minimizing power, while retaining performance. Ultra-Dynamic Voltage Scaling allows same circuit to operate at high performance for critical applications and in sub-threshold region (low frequency of operation) for energy constrained applications namely micro-sensor networks/ wireless sensor network (WSN), Radio Frequency Identification (RFID), low power digital signal processors (DSP), microcontrollers (MCU) and recently discovered energy harvesting systems [8].

The first application that required very-low power (at micro-watt) was electronic watch which incorporated a crystal oscillator requiring sufficient continuous transconductance. Early work by Eric A. Vittoz was done in this field and weak inversion came to existence as it got attention from digital design community [7]. The device current in this region of operation was modeled by Barron in 1972. Swanson and Meindl pioneered early work on slope factor followed by Troutman and Chakravarti in 1973.

[8] Both small signal model and first experimental prototype of analog circuit was published in 1976 exploiting weak inversion. It met some skepticism and it was even commented that such circuits, which use the "leakage current" of transistors, could not be reliable. During the following decade, the interest for exploiting WI in analog circuits was very limited world-wide, and mostly concentrated in Switzerland (EPFL). The EPFL group designed circuits in both weak and strong inversions. It led to work on EKV model to build a continuous model by C. Enz and E. Vittoz. It was in 80's that a new wave of interest in weak inversion circuits started to come through from work lead by Mead at Caltech.

2.2 EKV model Overview and WI design considerations

MOS operates in different regions of operations, namely strong inversion (SI), moderate inversion (MI) and weak inversion (WI) regions depending on biasing of device. Basically, upon reducing the gate-to-source voltage of transistor to less than threshold voltage, the device enters the weak inversion region. In this region, the current conduction mechanism is mainly diffusion [9], which is different from a familiar mode of operation (SI) where current is due to drift of carriers in inverted channel between drain and source terminals of MOSFET.

For describing MOSFET behavior in WI region, C. Enz and E. Vittoz proposed a universal model that works the best for low voltage operation known as EKV model [7] and is especially useful for designing circuits in Weak inversion or moderate inversion region of operation of MOSFET. The drain source current is presented as [8]:

$$I_{DS} = I_{spec}\left(\ln^2\left(1+e^{\left(\frac{V_p - V_S}{2U_T}\right)}\right) - \ln^2\left(1+e^{\left(\frac{V_p - V_D}{2U_T}\right)}\right)\right) \tag{2.1}$$

Where U_T is thermal voltage, V_P is device pinch-off voltage given in equation (2.2) and I_{spec} is specific current of transistor given in equation (2.3)

$$V_P \cong \frac{V_G - V_{T0}}{n} \tag{2.2}$$

$$I_{spec} = 2n\mu_{eff} C_{ox} \frac{W}{L_{eff}} U_T^2 \tag{2.3}$$

Here, n is the subthreshold slope factor given by equation (2.4) where C_d is MOSFET depletion capacitance.

$$n = 1 + \frac{C_d}{C_{ox}} \tag{2.4}$$

Equation (2.1) can be approximated to the well-known quadratic equation of drain-source current for SI region of operation given by equation (2.5) and an approximation in WI region provides the equation (2.6)

$$I_{DS} \approx \frac{\mu_{eff} C_{ox}}{2} \frac{W}{L_{eff}} (V_{GS} - V_{T0})^2 \tag{2.5}$$

$$I_{DS} \approx I_{spec}\left(e^{\left(\frac{V_p - V_S}{U_T}\right)} - e^{\left(\frac{V_p - V_D}{U_T}\right)}\right) \approx 2n\mu_{eff} C_{ox} {U_T}^2 \frac{W}{L_{eff}} e^{\left(\frac{V_{GS} - V_{T0}}{nU_T}\right)} \tag{2.6}$$

The transition between the modes of operation defines as WI, moderate inversion (MI) and SI is not abrupt thus, there is no clear-cut boundary between them. However, for understanding and analyzing the behavior of MOSFET some factors need to be defined. Inversion Coefficient (IC) defined as ratio of I_{DS}/I_{spec} is used in literature for identifying device operating condition. Conventionally, IC > 10, 1 < IC < 10 and IC < 1 are corresponding to SI, MI and WI regions respectively. Another more intuitive but rough metric for defining the boundaries of regions is based on gate-source voltage. In this approach, equating the WI and SI currents and their derivatives [9] or equating the g_m / I_D ratios which are given by equation (2.7) and (2.8) will result in (2.9)

$$\frac{g_m}{I_D} = \frac{1}{nU_T} \tag{2.7}$$

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_{th}} \tag{2.8}$$

$$V_{GS} = V_{th} + 2nU_T \tag{2.9}$$

It can be shown that in WI, g_m/I_D is maximized, resulting in highest power efficiency but the transit frequency (f_T) of MOSFET is lowest in this region making is inherently slower. Thus design in WI is approached for application with lower speed of operation where low power is desired. Despite this advantage, operating in WI region imposes several challenges. In WI, we face high sensitivity to process-voltage-temperature (PVT) variation. Leakage is another issue which may become serious in some designs especially digital VLSI systems incorporating millions of transistors on a single die. The signal-to-noise ratio is adversely affected in WI region because of lower signal swing and high

contribution of device noise, especially flicker noise. Proper sizing of MOSFET devices is one of the ways to address the noise problem. Use of large device size helps to reduce flicker noise and also helps to mitigate undesirable mismatch as well as process variation effects in design. The undesirable sub-threshold effects are more prominent as we move towards more advanced sub-micron technology nodes for MOSFET. Amongst others, process variation, leakage and Drain Induced Barrier lowering (DIBL) are some effects which can be more prominent as we move towards smaller device size, making them less attractive for applications targeted around WI region of operation [10] where achieving ultra-low power is main concern as opposed to high speed performance.

CHAPTER 3: Fully Differential ULP Low Noise OTA Design

3.1 Introduction

With advancement of technology and wide-spread use of electronics in day-to-day life, power efficient design has become indispensable in Digital and Analog circuits. This research focuses on design of ULP Integrated Circuit for bio-medical applications. With recent exploration in field of Brain-Computer Interface (BCI) and futuristic applications like controlling artificial human limbs and devices through BCI control, it becomes essential to make use of low power and efficient design to make such applications realizable in true form.

Here we propose design of an ULP OTA to be used as the first stage in front-end for ECoG detection and would be implanted inside skull bone. The design specifications according to system architecture and environment make it essential to achieve remarkable power dissipation reduction while maintaining signal integrity and durability of the highest standard. Other important factors coming into picture are low input referred noise, Power Supply Rejection Ratio (PSRR), Common Mode Rejection Ratio (CMRR) and good output signal swing since meaningful input differential signals have been observed to be in range of < 300 uV pk-pk. A design advantage seen in such system is a low bandwidth or speed requirement since meaningful ECoG signal ranges less than 200 Hz (including gamma activity of brain).

3.2 Design Specifications

One of the most important specifications for ECoG signals is input referred noise which must be kept less than 5-10 uV_{rms} [3]. It can be understood from the fact that the input signal level range is 10 – 150 uV with a bandwidth of subHz – 200 Hz. To get a good SNR we must keep the noise level introduced by circuit less than the background noise. We want to achieve as low power as possible to mitigate heat generation from the integrated circuit, elongate lifetime of such battery operated systems and enable large recording array as seen in some recent works [12].

3.3 Design and Analysis of Proposed OTA

Use of WI region is appropriate for this application as it gives much higher efficiency in terms of g_m/I_D compared to SI region. Thus we can achieve sufficient gain for lower power dissipation. Several design and measurement issues are associated with designing in WI region namely sub-threshold effects discussed earlier and very high output impedance which demands special considerations for CMFB, feedback and measurement to avoid loading. Fig 3 shows the top level structure of proposed ULP OTA with capacitive feedback and $M_{1\text{-}4}$ are used as "pseudo-resistors" for self-biasing of the amplifier. We use a capacitive feedback essentially to provide isolation of DC path between amplifier and ECoG electrode. It is not only good from biasing prospective as it avoids DC offsets from electrode-tissue interface of ECoG grid but also acts as additional safety measure for implantable electronics. Some existing bio-amplifiers use very large off-chip capacitors to filter out DC offsets and provide a low corner frequency of pass-band but this approach is not feasible for large array of implantable bio-signal acquisition systems [11]. Assuming a large open

loop gain for amplifier the closed loop gain is determined by ratio of input capacitor C_1 to feedback capacitor C_2.

Closed loop gain, $A_{CL} \approx \frac{C_1}{C_2}$ (3.1)

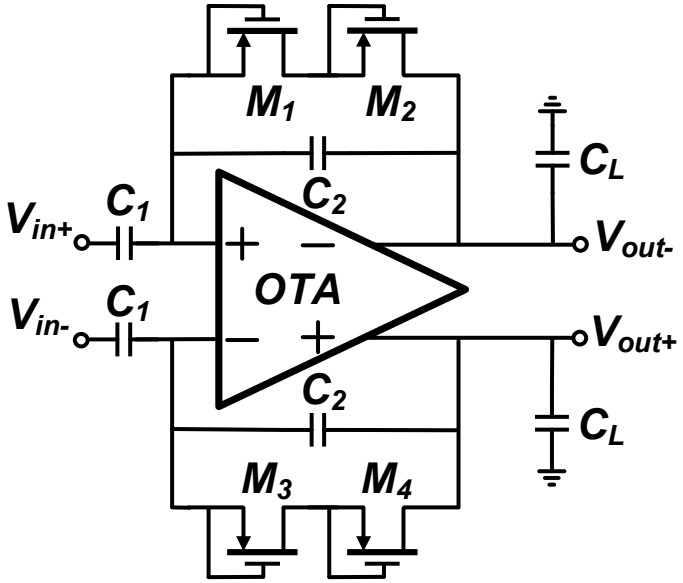

Figure 3: Fully Differential ULP low noise OTA

For this amplifier, we have set the closed loop gain to 40 dB as per requirement from system level design. Thus values of C_1 and C_2 are selected to be 20 pF and 200 fF respectively to provide the required feedback factor and in conjunction with lower corner frequency close to 5-10 Hz. The area required by C_1 is 80 um x 54.5 um using dualmimcap of IBM 130 nm process and 8.5 um x 11 um for C_2 respectively. We are able to contain the size and values of the capacitors by use of pseudo-resistors which provides very high resistance of the order of several Giga-Ohms [11], [13]. Use of MOS as pseudo-resistors helps to provide a sub-Hz high-pass frequency corner as a result we can confine the size of C_1 which making large array of 64 channels or even higher arrays possible in an

implantable integrated circuit. We will discuss MOS-bipolar device as pseudo-resistors later. Upon analysis it can be seen that if C_1, C_L >> C_2 the bandwidth can be approximated as

$$BW \approx \frac{g_m}{A_{CL} \times C_L} \tag{3.2}$$

Where, g_m is transconductance of the OTA and load capacitance C_L is set as 10 pF. This also helps to achieve a band-pass behavior starting from sub-Hz up-to few hundred Hz which not only provide attenuation to out of band interferences but also help to achieve ultra-low power design. Resulting bandwidth of the designed structure is ~10 Hz to 270 Hz

3.3.1 OTA Core Structure

Fig 4 shows the schematic of the proposed novel ULP low noise OTA structure. This OTA is designed in weak inversion (WI) region for IBM 130 nm CMOS process. The supply voltage used for this design is V_{DD} of 0.4 V. Upon detailed study of weak inversion region we know that the minimum headroom for a single transistor to be biased in weak inversion region is approximately 3-4 U_T (100 mV at 273 K) [8] and thus for a design with 3-4 stacked transistors a minimum supply of 0.25 V is possible as used in [17]. It is also known that at lower supply voltage the sub-threshold effects such as PVT variation, mismatch and leakage effects are exacerbated. Thus, we want to choose an optimum point for operation in weak inversion region to obtain low power, low noise and a robust performance mitigating these sub-threshold effects. Another point of consideration is that at lower supply voltages the ratio of sub-threshold current versus various leakage currents reduces, making the design more susceptible to the non-ideal effects discussed in chapter 2.

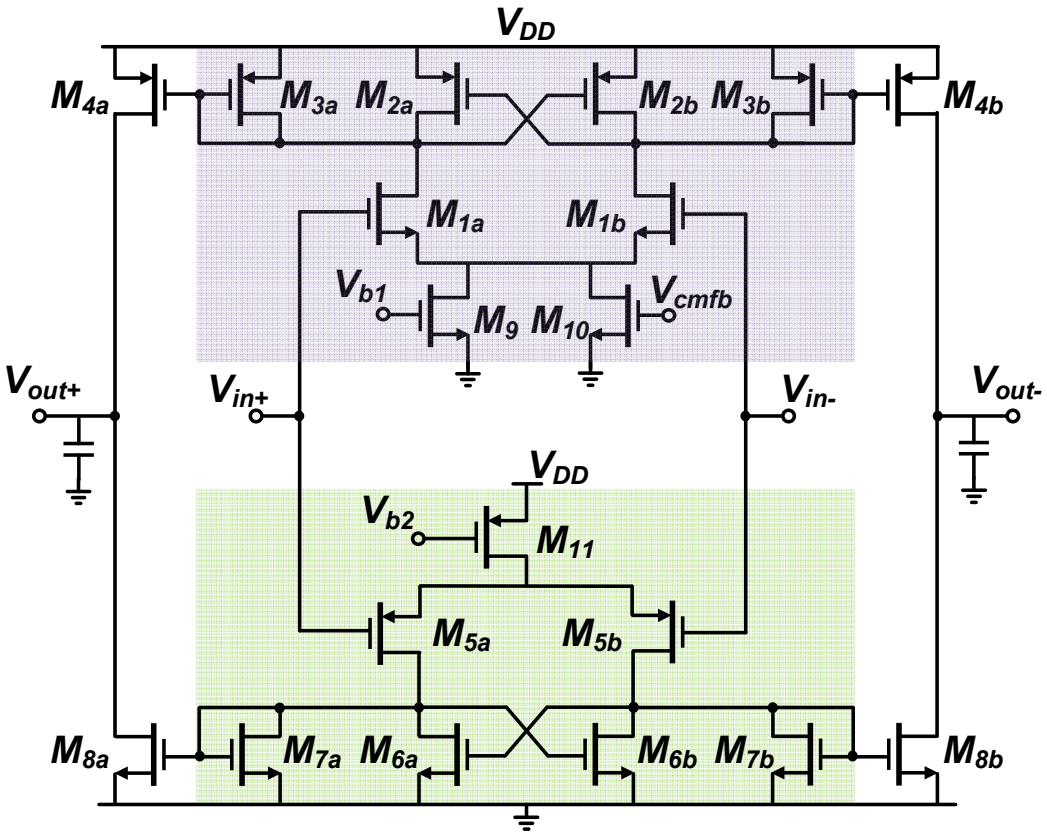

Figure 4 : ULP low noise OTA core schematic

Upon careful consideration of these effects and leaving a good margin for robustness we choose our supply voltage. This design is an OTA with very large input and output resistance. Reason for choosing an OTA topology is that it only drives a capacitive load comprising of load capacitor C_L, an analog multiplexer switch followed by a buffer which helps to achieve higher speed of operation in this inherently slow region of operation.

The OTA structure comprises a complimentary differential input stage with cross-coupled positive feedback and diode connected transistors in parallel that act as current mirror to output stage which is a class AB type of structure and achieves almost full scale rail-to-rail output signal swing. The complementary structure helps in boosting g_m and

doubles the inherent gain. In addition it also reduces the input referred noise voltage by a factor of $\sqrt{2}$ compared to simple differential structure [3]. The transistors M_3 and M_7 act as current mirror by multiplying first stage current with proper aspect ratio to output stage and help defining proper bias condition for first stage. This eliminates the requirement of CMFB in first stage. In addition, there is no need for additional biasing circuitry. The positive feedback provided by transistors M_2 and M_6 in cross-coupled pair configuration helps in additional g_m enhancement. Another effect of adding this cross-coupled pair in parallel to current mirror is increase in gain from current steering away from M_3 and M_7 by boosting its r_o. The sizing of this cross-coupled pair should be done carefully to avoid stability and latching issues. This can be done by keeping g_m of cross-coupled pair much lower than input transistors. The ratio of g_m of cross-coupled pair compared to input transistors inversely affects input referred noise due to thermal and flicker noise which provide one more reason to keep g_m lower.

The gain analysis of the OTA reveals the following equations. Solving for subsections, we have gain for first stage Fig 4-purple box (NMOS input) is given as A_{V1} and green box (PMOS input) is given as A_{V2} in equation (3.3, 3.4).

$$A_{V1} = \left(\frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m3} - g_{m2}} \right), \text{ where } g_{ds} = 1/\, r_o \tag{3.3}$$

$$A_{V2} = \left(\frac{g_{m5}}{g_{ds5} + g_{ds6} + g_{ds7} + g_{m7} - g_{m6}} \right) \tag{3.4}$$

Total voltage gain A_V is given by equation (3.5)

$$A_V = \frac{V_{out}}{V_{in}} = \left(A_{V1} g_{m4} + A_{V2} g_{m8} \right) \times R_{out} \tag{3.5}$$

Here, total transconductance G_M and effective output resistance R_{out} are given as

$$G_M = \left(A_{V1} g_{m4} + A_{V2} g_{m4}\right) \tag{3.6}$$

$$R_{out} = \frac{1}{g_{ds4} + g_{ds8}} \tag{3.7}$$

In noise analysis, total input referred noise can be broken down to sum of $V_{n,inN}$, $V_{n,inP}$ and $V_{n,in4,8}$ which are noise contribution due to Fig 4 purple box (NMOS input), green box (PMOS input) and output stage respectively.

$$V_{n,inN} = 8KT\gamma\left(\frac{g_{m1} + g_{m2} + g_{m3}}{g_{m1}^2}\right) + \frac{2}{C_{ox} f}\left(\frac{K_N}{(WL)_1} + K_N\left(\frac{g_{m2}^2}{g_{m1}^2 \times (WL)_2} + \frac{g_{m3}^2}{g_{m1}^2 \times (WL)_3}\right)\right) \tag{3.8}$$

$$V_{n,inP} = 8KT\gamma\left(\frac{g_{m5} + g_{m6} + g_{m7}}{g_{m5}^2}\right) + \frac{2}{C_{ox} f}\left(\frac{K_P}{(WL)_5} + K_P\left(\frac{g_{m6}^2}{g_{m5}^2 \times (WL)_6} + \frac{g_{m7}^2}{g_{m5}^2 \times (WL)_7}\right)\right) \tag{3.9}$$

$$V_{n,in4,8} = 8KT\gamma\left(\frac{g_{m4} + g_{m8}}{G_M^2}\right) + \frac{2}{G_M^2 C_{ox} f}\left(\frac{K_N g_{m4}^2}{(WL)_4} + \frac{K_N g_{m8}^2}{(WL)_8}\right) \tag{3.10}$$

Design methodology and other sizing considerations for input stage are also discussed in this section. The bottleneck for sizing and current division comes from noise specification. We can get very high gain with this topology at much lower DC power dissipation close to few Nano-Watts (which has also been reported recently in other works [17]) as seen from equations (3.3, 3.4 and 3.5) but the thermal noise from MOSFET is inversely proportional to g_m which in turn is proportional to bias current. Based on noise we obtain a minimum value of g_{m1} and g_{m5}. For a particular technology we have fixed g_m/I_D in WI region which can be used to determine DC current for input stage. Having large size helps to mitigate flicker noise which also has a significant contribution in our bandwidth of

operation. Large sizes also help to get a more linear performance across process variations and mitigate mismatch effects. Although device sizes are large to minimize PVT variation and noise, mechanisms for controlling device sizes and threshold voltages (like adaptive body biasing) can be included for reaching perfect operation. However this will complicate the circuit structure and is not necessary for this application (ECoG).

In output stage we have a class AB type of structure which provides an almost rail-to-rail swing when biased in WI region. Rail-to-rail swing avoids saturation of certain spikes at the input from neural activity. From system level design considerations gain of 40dB was required from the OTA. Noise of second stage is not a pressing concern since gain from first stage is quite high. Transistors in output stage have large sizes and the conversion factor of current mirror from M_3 to M_4 is <<1. This is based on several factors. The DC current in output branch can be kept much lower since noise contribution is much lower. Lower current also increases r_o of these transistors which enhances overall gain. Large size is still needed to mitigate effect of mismatch and process variation on overall gain and power dissipation. Sizing is based on factors discussed above and to provide good match between g_m of PMOS and NMOS of output stage to maximize the gain and get a truly complimentary stage. Compared to a cascade type of output stage we have lot of benefits such as no need for extra biasing circuitry which also reduces power dissipation and higher output voltage swing. Sizing of current source transistors $M_{9\text{-}11}$ is done considering effect of r_o and noticeable process variation in WI region. Larger size helps in mitigating flicker noise and provides more headroom for input transistors M_1 and M_5 which also helps in increasing g_m. Although large transistors are used in the circuit, still the capacitances dominate the total area of the chip.

3.3.2 Common mode feedback

Being a fully differential amplifier, there is need for CMFB especially at output stage to properly define the output level and maximize output resistance. Use of standard common mode feedback such as buffers or resistive feedback in not feasible for this design as the output impedance is of the order of 35 MΩ and to avoid loading effect the resistors have to be very large in area. We use a common mode sensing circuit given by [14].

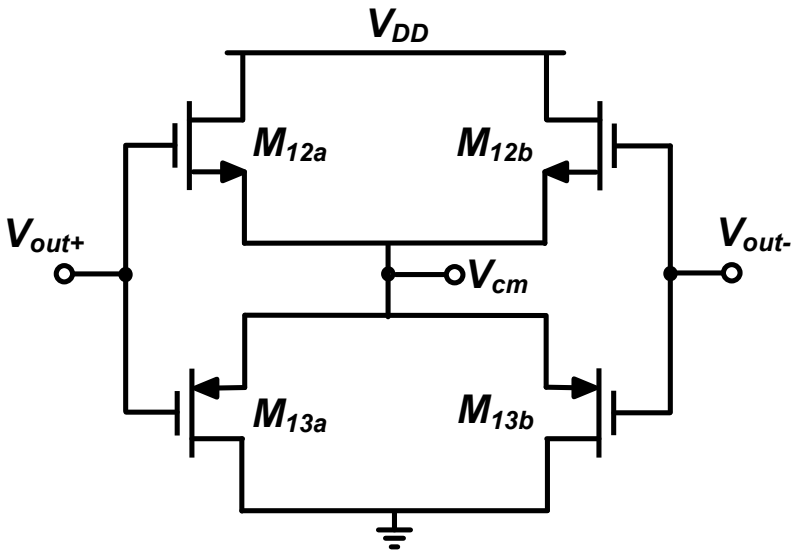

Figure 5: Common mode sensing circuit

Fig 5 shows the common mode voltage detector circuit introduced in [14] and shows a very good linearity even for low supply voltages as low as 0.4 V. As we discussed earlier, the need for very large resistors to detect common mode voltage at output of differential amplifier is addressed using this approach. As opposed to NMOS or PMOS only designs which are typically used for this purpose, in very low supply voltage circuits these are not able to provide a rail-to-rail operation as they get turned off within considerable range of voltages as well as positive offsets for PMOS and negative offsets for NMOS only

detection circuits. Here as we can observe from visual inspection, both PMOS and NMOS acts in source follower configuration and works well for both SI and WI regions of operation. Author in [14] also talks about proper sizing to reduce differential gain and with proper ratio of PMOS and NMOS. The offset voltage increases for lower supply voltage and is observed in the simulated result shown in Fig 4 and also a very good linearity for our range of operation. This structure also dissipates minimal power compared to OTA core structure and we see a general trade-off of power dissipation vs noise throughout design process. The noise effect from CM sensing structure is minimal and we can use minimum size transistors for M_{12} and M_{13}.

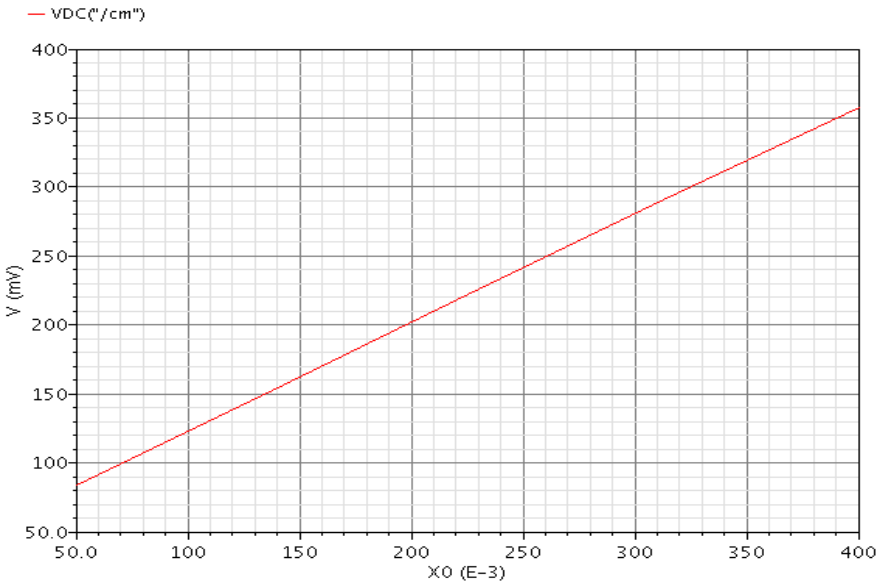

Figure 6: Simulated transfer curve of common mode sensing circuit

The CMFB comprises of CM sensing circuit shown in Fig 5 and CMFB amplifier which compares the output of CM sensing circuit with an external tunable reference voltage. Use of the external reference voltage also provides a degree of freedom during

measurement as the offset may vary across PVT and we have direct control of output DC voltage. CMFB is also essential in maintaining the gain and we observe that without it not only DC is undefined but gain is affected as well. This affect in gain is due to change in V_{DS} of NMOS and PMOS transistors M_4 and M_8 which leads to unbalanced and reduced output impedance thereby reducing the overall gain of OTA.

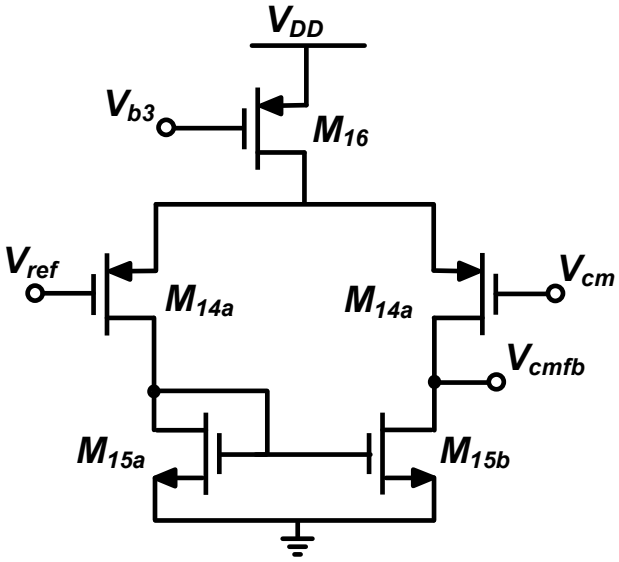

Figure 7: CMFB Amplifier

Fig 7 shows the structure of CMFB amplifier. It is a very simple differential topology with PMOS input M_{14} and current mirror load M_{15}. This structure is used compared to NMOS input stage due to input and output voltage compatibility. The output voltage V_{cmfb} is designed to provide a good dynamic range considering rail-to-rail initial condition of output common-mode voltage of OTA core. The stability of CMFB should also be considered in designing the whole architecture. Power consumption of this structure needs to be less than OTA and its BW should be greater that OTA

3.3.3 MOS-Bipolar Pseudoresistor

In Fig 3, transistors $M_{1\text{-}2}$ are MOS-Bipolar devices and acts as pseudoresistors and for small voltage across the devices. The use of MOS as pseudoresistors for OTA application was first introduced by Harrison in [11] and which is referred back to [5] for base ideas. From [5], it is stated that with negative V_{GS}, each device functions as diode connected pMOS transistor and with positive V_{GS}, the parasitic source–well–drain p-n-p bipolar junction transistor (BJT) is activated, and the device acts as a diode-connected BJT. For small voltage across the devices the incremental resistance can go beyond $10^{11}\ \Omega$ as per [11]. Authors in reference [15] talk about control of the resistance through control of gate voltage. It also defines the value of pseudo-conductance derived from drain current equation in WI region [15]. Gate voltage control is used in several bio-amplifiers but it adds more biasing circuitry and is generally used for wide tunable ranges.

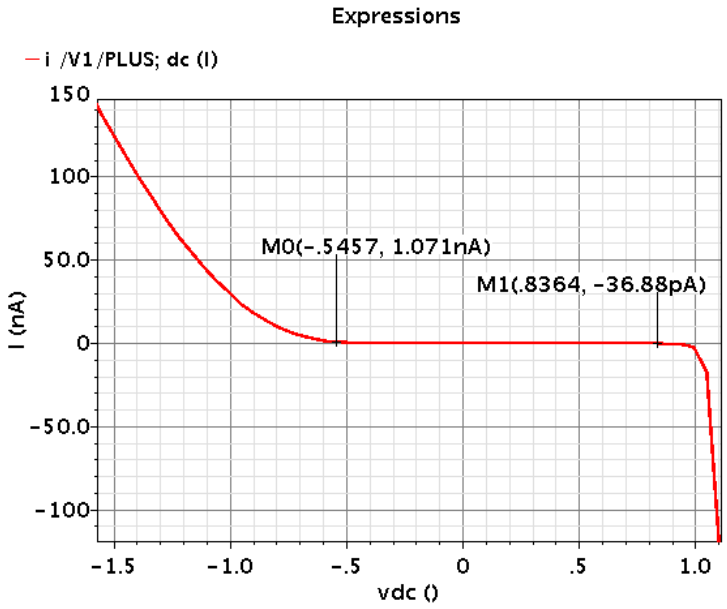

Figure 8: Simulated I-V curve of MOS-Bipolar element ($M_{1\text{-}2}$ of Fig 3).

Use of two back to back transistors in the configuration shown in Fig 3 helps to reduce distortion for large swing signals at the output. The transistors are sized 600 nm x 40 um for our application and we can see the V-I relationship in Fig 8. It shows the region of operation and a good approximation of pseudoresistor value for calculation of low-frequency cut-off of ac coupled OTA. The low-frequency cut-off for this topology is calculated from RC time-constant from input capacitor C_1 and effective resistance of pseudoresistor calculated for our range of operation. As seen in Fig 8, for low voltages values the incremental value of pseudo-resistor exceeds $10^{10}\,\Omega$.

3.3.4 Figure-of-merit (FOM)

There are a several FOMs that are used to evaluate the trade-off between performance matrixes of such low power bio-signal amplifiers. Since this design and application requires minimizing power for a given noise budget we must consider the trade-off between noise and power for a given bandwidth of operation. Noise Efficiency Factor (NEF) was introduced in 1987 [5] quantifies the trade-off between input referred noise $V_{ni,rms}$ of amplifier, total amplifier supply I_{tot} and BW is shown in equation 3.11. NEF is comparison of $V_{ni,rms}$ of amplifier with respect to input referred noise $V_{ni,rms,BJT}$ of ideal BJT (without base resistance and flicker noise) having NEF of one.

$$NEF = \frac{V_{ni,rms}}{V_{ni,rms,BJT}} = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{3.11}$$

Lack of supply voltage information in equation (3.11) makes it incomplete when considering power efficiency and heat budget. Another FOM based on similar systems

which addressed contribution of supply voltage is defined by Power Efficiency Factor (PEF) [16] as follows:

$$PEF = NEF^2 \times V_{DD} \tag{3.12}$$

As discussed in [4], "PEF solves the power efficiency comparison issue in (3.11), but it has limitations in overall system optimization, as a neural recording channel with low backend quantization resolution may still have a very low PEF by reducing. In order to compare the system suitability to practical applications, a system efficiency factor (SEF) is proposed".

$$SEF = \frac{NEF^2 \times V_{DD}}{DR_{out}} \tag{3.13}$$

, where dynamic range is $$DR_{out} = 10\log\frac{V^2_{amp,\max}}{2 \cdot G^2_{AFE} \cdot V^2_{ni,rms}} \tag{3.14}$$

Here, $V_{amp,max}$ is the maximum signal amplitude at the AFE output, and G_{AFE} is the AFE voltage gain. As proposed in [4], "SEF takes the system noise, power and dynamic range performances into account. Therefore it is more suitable for system level comparison and optimization."

3.3.5 Simulation Results

This chip was designed for IBM 130 nm CMOS process and upon careful consideration of all the trade-off and effects discussed earlier in this chapter. The design ratios are shown in Table 2.

Table 2: Amplifier transistor sizes

Transistors	**W/L Ratio (m)**
M1	53.5u/1.35u
M2, M3	50u/10u
M4	3.7u/32u
M5,	140u/1.2u
M6,M7	15u/30u
M8	400n/40u
M9,M10	80u/360n
M11	120u/130n
M12	3u/130n
M13	1u/130n
M14	3u/360n
M15	3u/360n
M16	4u/130n
Pseudo-resistor M_{1-4}	600n/40u

The supply voltage is 0.4V and a bias network is used to provide bias voltages of V_{b1}=294.9 mV, V_{b3}=312.4 mV, V_{b2}= 32.34 and V_{cmfb}=53.51 mV approximately using an external bias resistor of 1MΩ sinking 294.9 nA. This type of bias is designed to get more control while measurement and an SMU can be used to replace the bias resistor.

The simulated plots for Gain-BW, input referred noise, CMRR, PSRR, common mode input resistance and differential mode input resistance are shown in Fig 9-14 respectively.

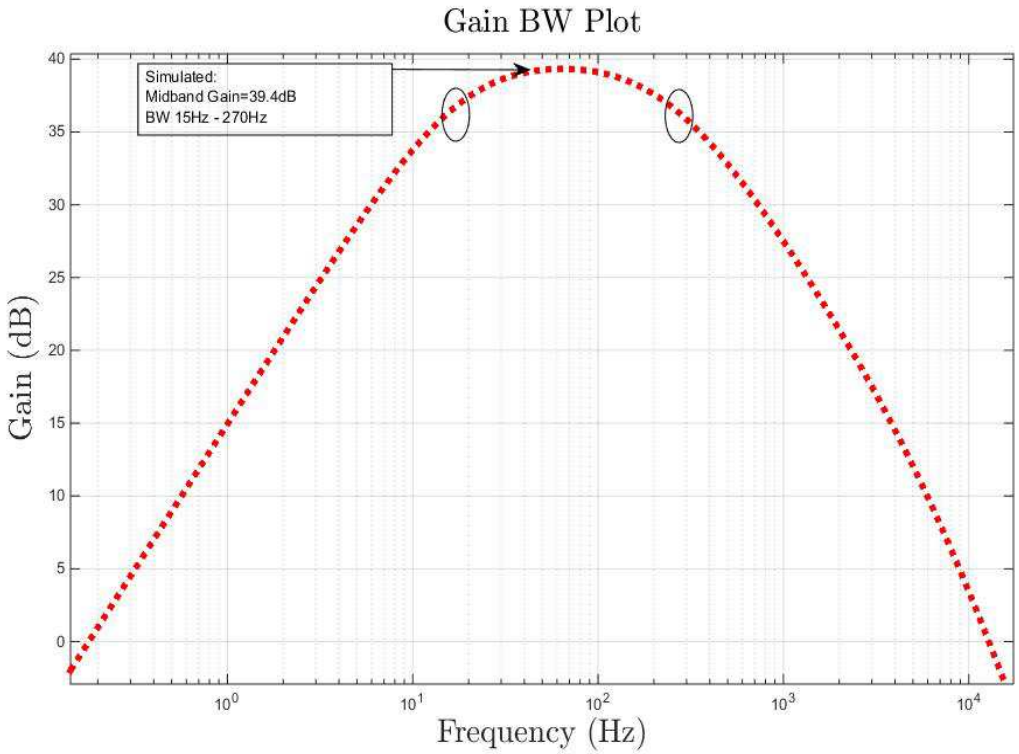

Figure 9: Gain-BW of OTA (simulated)

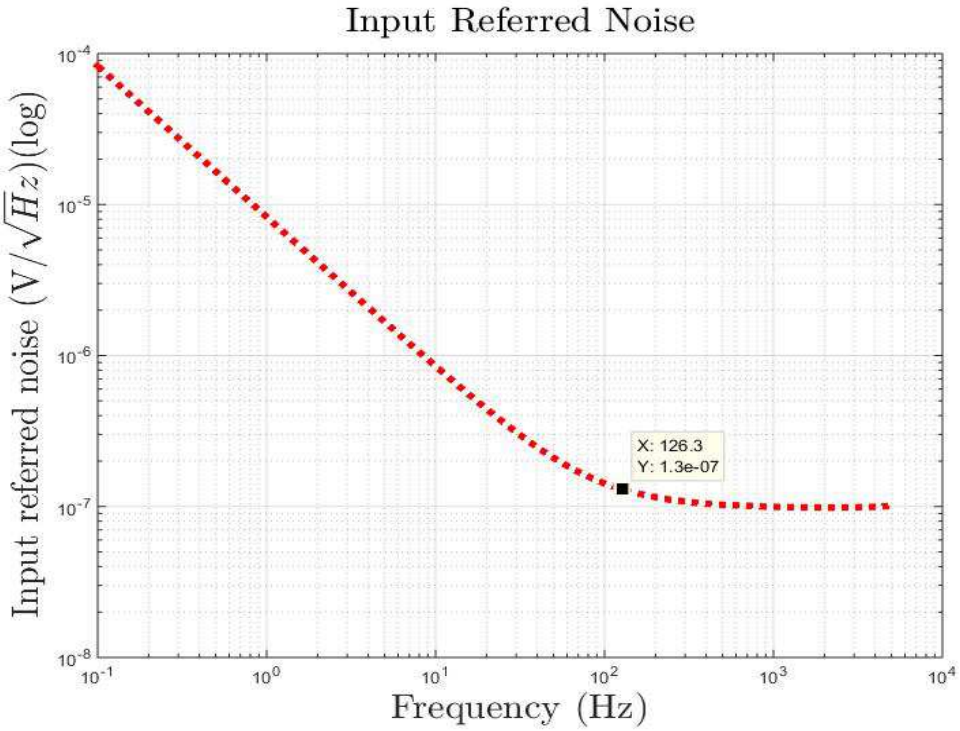

Figure 10: Input referred noise of OTA (dB-dB scale) (simulated)

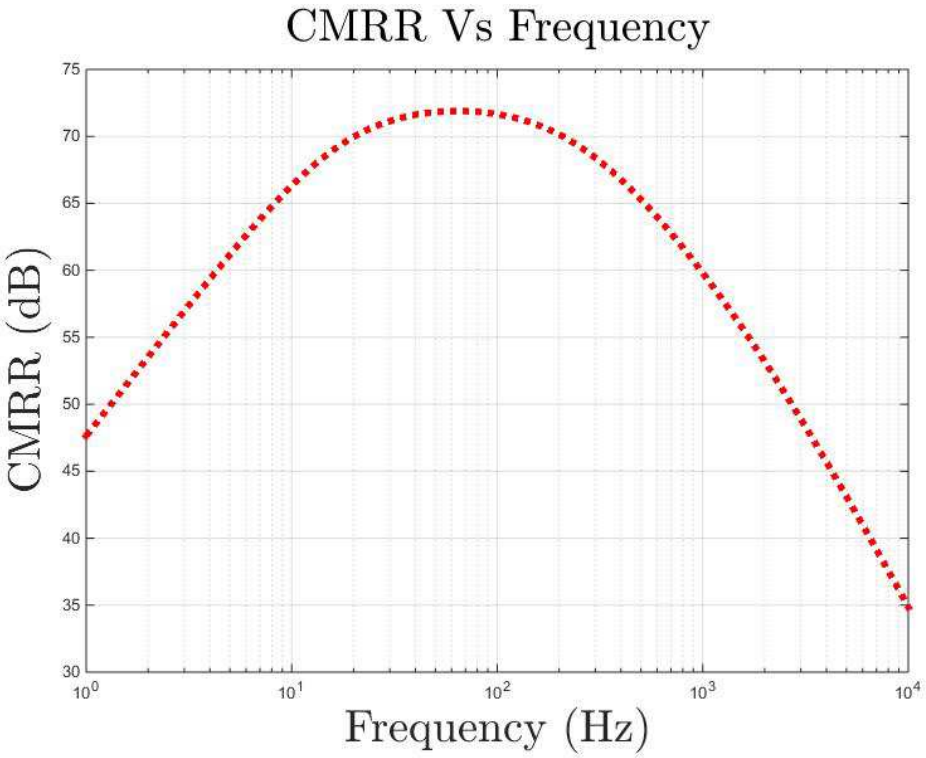

Figure 11: CMRR of closed loop fully differential OTA (simulated)

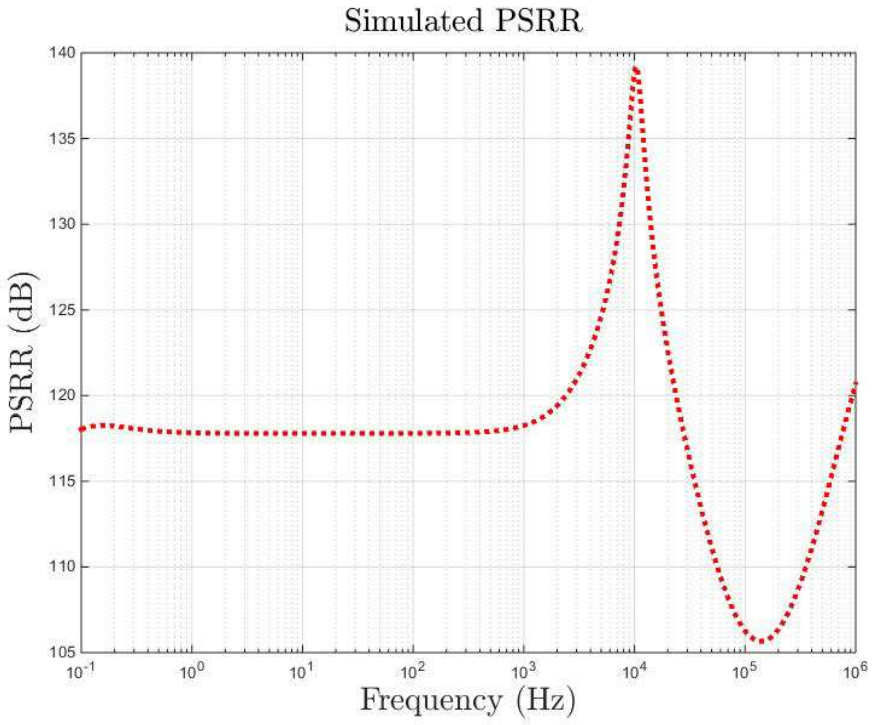

Figure 12: PSRR of closed loop fully differential OTA (simulated)

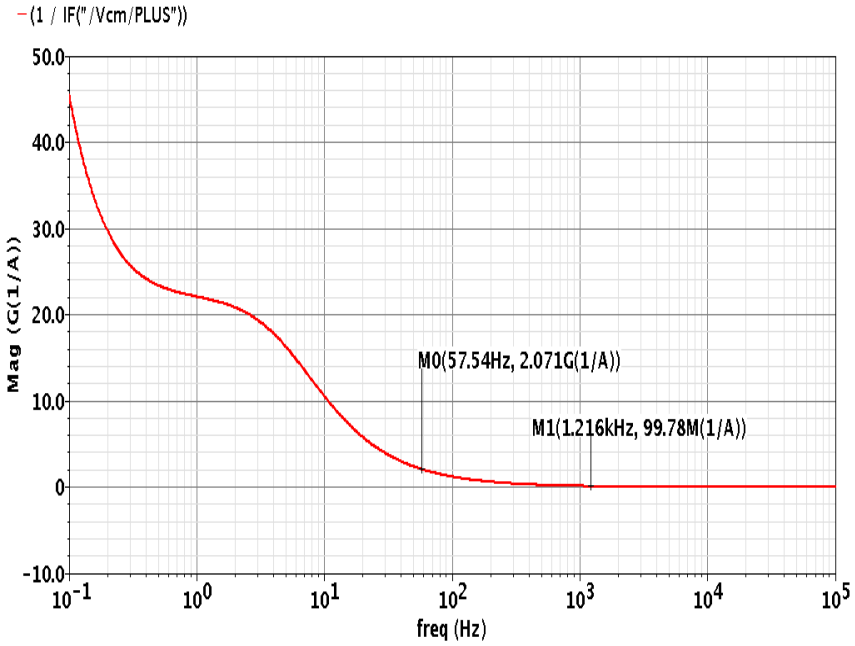

Figure 13: Common mode input impedance of OTA with respect to frequency

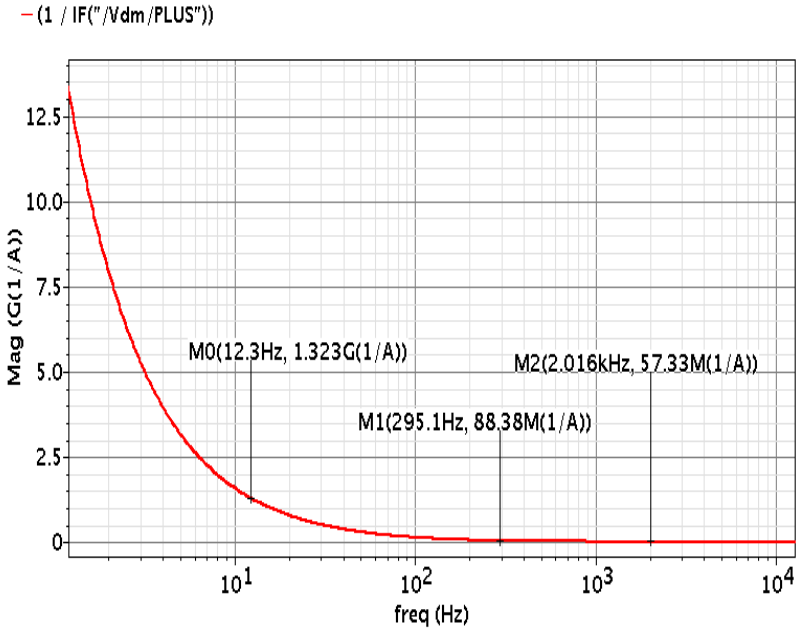

Figure 14: Differential mode input impedance of OTA with respect to frequency

Having very high input impedance helps to mitigate effect of gain mismatch from offsets in electrode impedances. It also reduces effect of loading from ECoG electrode to input of transistors. From fig 9 we can see the 3 dB bandwidth is matches very close to system requirement from 15 Hz – 270 Hz. Fig 10 shows a flicker noise corner frequency close to 126 Hz which is close to mid-band frequency. This gives the complete picture of noise distribution across the BW and shows that flicker noise effect is very significant for such low frequency application. When integrating over a BW of 15 Hz to 10 KHz, input referred voltage noise is 10.24 uV_{rms} which yields an NEF of **2.71** and correspondingly PEF of **2.94**. Large PSRR and CMRR help to get rid of supply and common mode noise. It also becomes crucial in this application due to significant contribution of 60 Hz noise falling in band of operation. The power distribution among various blocks is 524 nA for Main OTA block, 0.097 nA for Common mode sensing block and 5.7 nA for CMFB amplifier yielding a total of 211 nW (simulated) power dissipation for 0.4 V supply. Measured result showed very close resemblance to simulated result with 216 nW power measured for single amplifier unit. This ultra-low power measurement was done with help of source-measure unit (SMU).

3.4 Layout

Fully differential topology is susceptible to mismatch if layout is not done carefully. Care was taken in layout to provide perfect symmetry of signal path as well as all the transistors in differential configuration. Other well know techniques includes use of multiple fingers for distribution of gate, use of guard rings for NMOS and PMOS structures

which are in signal path or susceptible to substrate noise. Use of guard rings also prevents latch up and is strongly advised in low power digital circuitry.

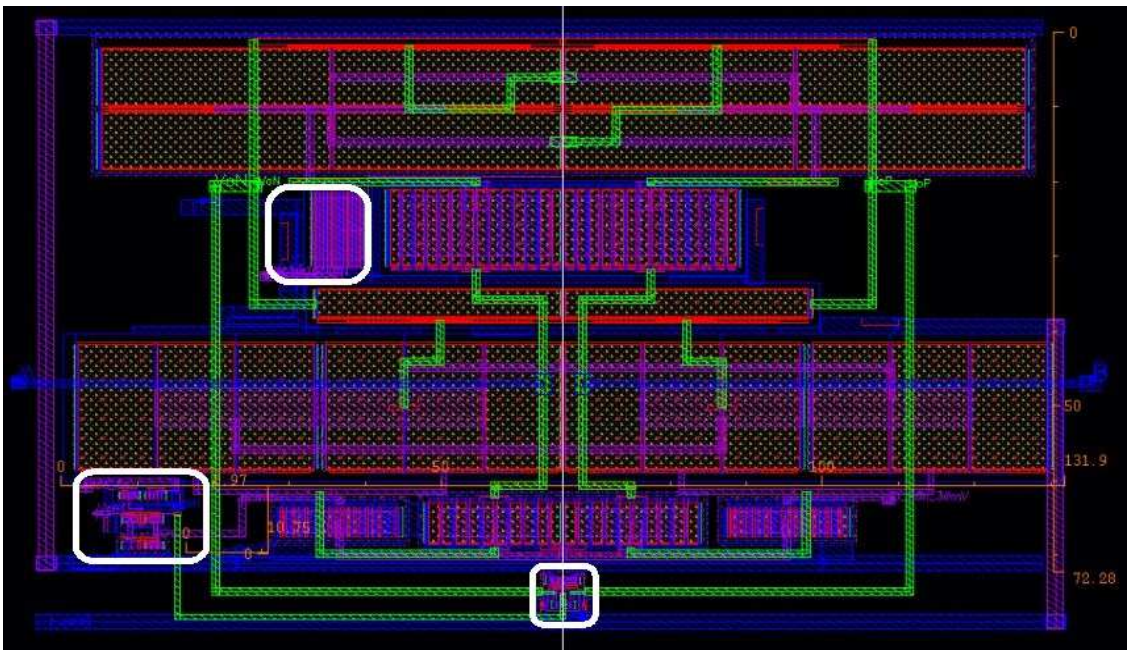

Figure 15: Layout of OTA without capacitive feedback.

In Fig 15, the white box shown center bottom is the CM sensing circuit and other two white boxes depict placement of CMFB amp and biasing circuitry which do not need to be symmetric to rest of the circuit. From green metal paths (M3 layer) it is evident that there is perfect symmetry for differential operation. Chip area for Fig 15 is 72 um x 131 um.

Fig 16 shows the placement of capacitive feedback. Total area consumed by a single OTA is therefore 284 um x 157 um. Use of pseudoresistors helps to keep area of on-chip capacitors low such that 64 channels can be integrated in a very small area of 5.62 mm^2 (excluding pads).

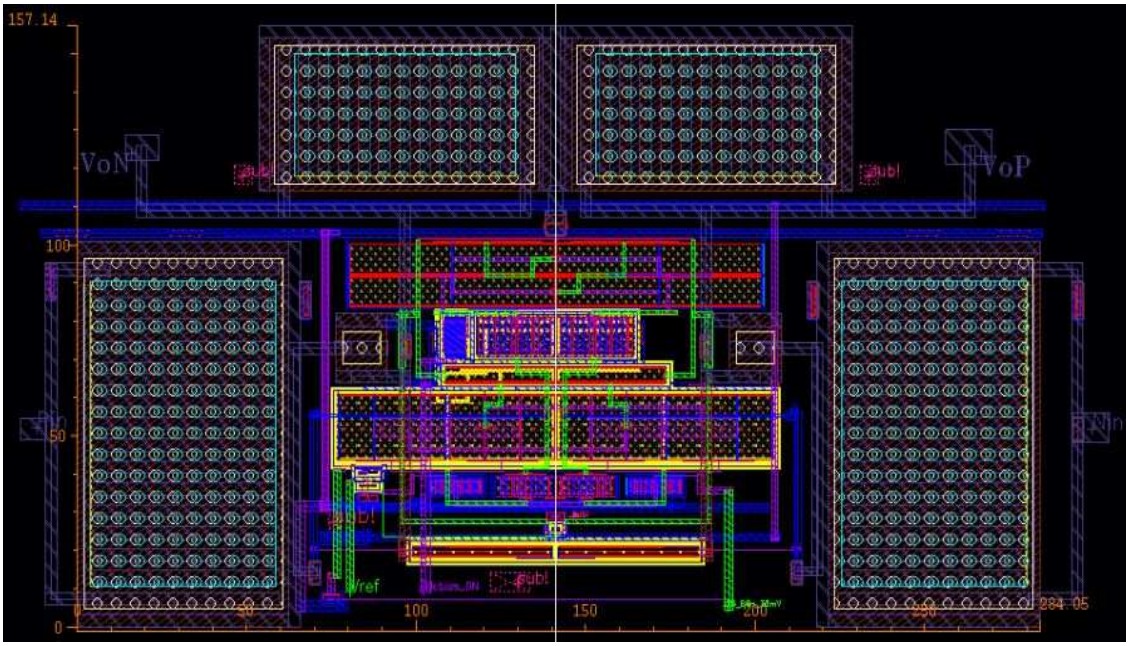

Figure 16: Layout of OTA with feedback

Fig 17 shows layout of complete chip including 64 ULP OTA shown in white box and digital circuitry used to control analog multiplexer in pink box. In the bottom corner we have a break-out circuit of a single amplifier with feedback and on the bottom right we have break-out circuit of open-loop amplifier for debugging and measurement purposes.

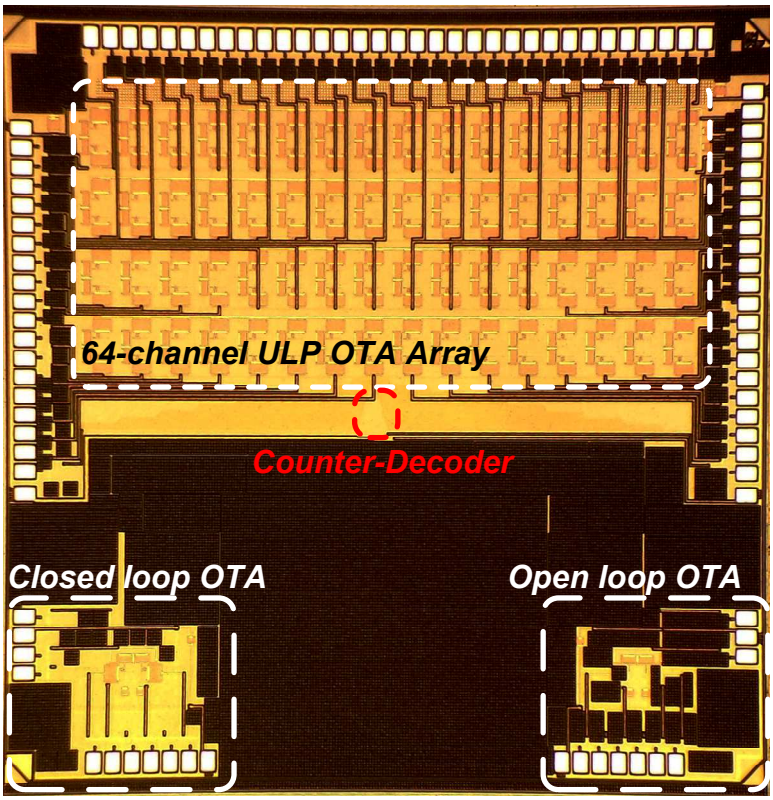

Figure 17: Complete Chip Micrograph

CHAPTER 4: Measurements

The chip was fabricated in IBM 130 nm CMOS process and has a total of 96 pins including two break-out circuits as shown in Fig 16. Both electrical and human measurements were desired from this tape-out which requires packaging and custom PCB board for a field trial. In all measurements were carried out using die-probing for electrical measurements as well as PCB for complete measurements. In this chapter we will discuss in detail all the considerations for in-vitro and in-vivo measurements of the design.

4.1 Packaging and PCB Design

Considering a 4mm x 4mm fabricated die and 96 pads, a 100 pin QFN package is apt for this purpose. It provides both, a small area and lower complexity for PCB compared to Dual inline packages (DIP) or Ball Grid Array Packages (BGA). It is advisable to use protective measures from ESD environment for sensitive designs in advanced CMOS technologies. Care should be taken during wire-bonding that the wire bond must be done at package first and pads on die later. The bonding diagram is shown in appendix.

For PCB, we used a two board solution. First one, the main board comprises of the main chip with QFN package as well as peripheral components for biasing and tuning circuitry for the ULP OTA array and break-out circuits. Most of the passive components used are surface mount devices (SMD) which provide better performance in presence of environmental noise and interferences. Same package for all passive SMD component (standard 0805) was used which makes rapid changes and debugging easier. The main board is a 4 layered board with two internal layers used as ground and supply planes and

outer layers used as signal layers. A large unbroken ground plane helps in providing a strong ground which may vary for some high speed and mixed signal applications where separating analog and digital ground is highly recommended. A detailed schematic and 3-D image of both the boards is added in appendix. Peripheral device mainly comprise of bias circuitry of main chip namely a regulated supply of 0.4 V, tunable reference voltage generation for CMFB reference voltage and tunable bias current sink for properly biasing the circuit in desired region of operation. With help of a different set of bias conditions at 1.2 V supply we can also bias the circuit in SI region of operation. This extra degree of freedom helps in debugging of the test chip.

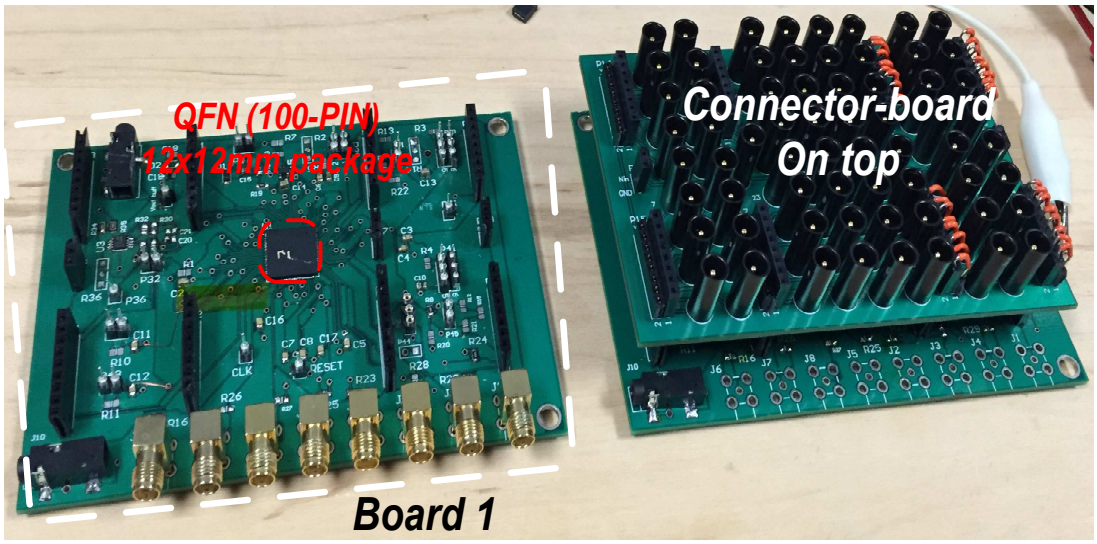

Figure 18: Picture showing both PCB boards stacked and the packaged IC

Second board is a connector board and comprises mainly of 1.5 mm touch proof connectors used for EEG and ECoG connections. This board is responsible to connect the inputs from 64 channel ECoG micro-grid in a hospital setting (in-vivo) to input of our

amplifiers. This board sits exactly on top of main board with help of long 8-pin headers providing enough headroom to access the main board and avoid contact from open header pins.

4.2 In-Vitro and In-Vivo measurements

OTA has large output impedance by its definition. When operating in WI region, this impedance will become orders of magnitude larger due to very low current levels. Thus, for driving next stages (probably ADC) a buffer is required. The input impedance of the buffer should be much larger than OTA output impedance to avoid any loading effect on gain. Buffer can be designed on-chip (which can be future work of this project). For the scope of this thesis, an industrial instrumentation amplifier has been used as buffer stage. It is worth mentioning that input impedance of most instruments like oscilloscope is not higher than 1 MΩ compared to relative output impedance of the amplifier close to 35 MΩ. Non-ideal contribution of measurement instruments on the final measured responses should also be taken into account. Initially, all DC voltages were measured and were found to be working correctly. It was particularly important to get accurate measurements for power and check the functionality of the CMFB circuit with the new topology. CMFB was found to be stable and the output voltage could be set at $V_{DD}/2$ by adjusting reference voltage. The relative change in reference voltage showed very good linearity to the output voltage with some offset ranging from 40 mV to 50 mV part-to-part and up-to 80mV on the whole amplifier array with multiplexer as shown in fig 19.

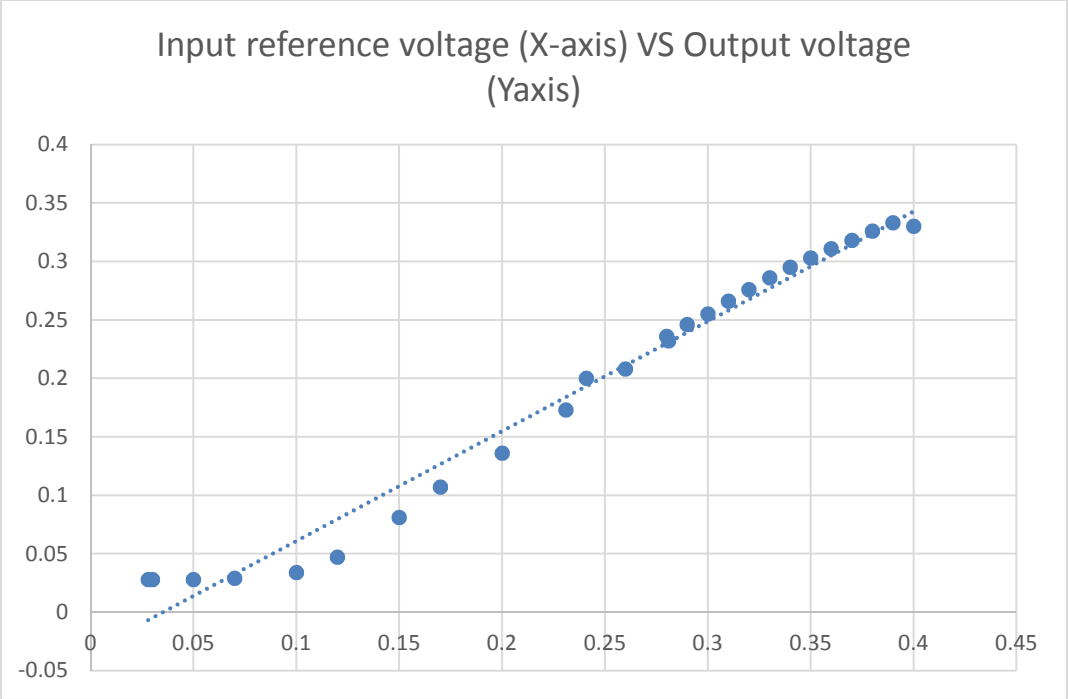

Figure 19: Transfer curve showing linearity and range of CM Sensing block

Due to low frequency range of circuit operation, 60 Hz interference is quite significant, and if not removed will make the measurement almost impossible. Shielding of circuit and cables alongside with using sharp notch filter at 60 Hz may be necessary to deal with this issue. Fig 20 shows results of an experiment done in lab environment for EMG recording on a volunteer. Two consecutive channels of the multiplexer were used where one channel was fed EMG signal. We can see the EMG signal recorded where there was no muscular activity for first 10 seconds (X axis – time, Y axis – input signal post processing) and the three consecutive arm reflexes with some interval shown by the peaks on the top channel. In the complete chip system topology, the negative terminal of all amplifiers is connected together to a common reference and positive terminal takes input from different input signals for ECoG/ EEG or EMG.

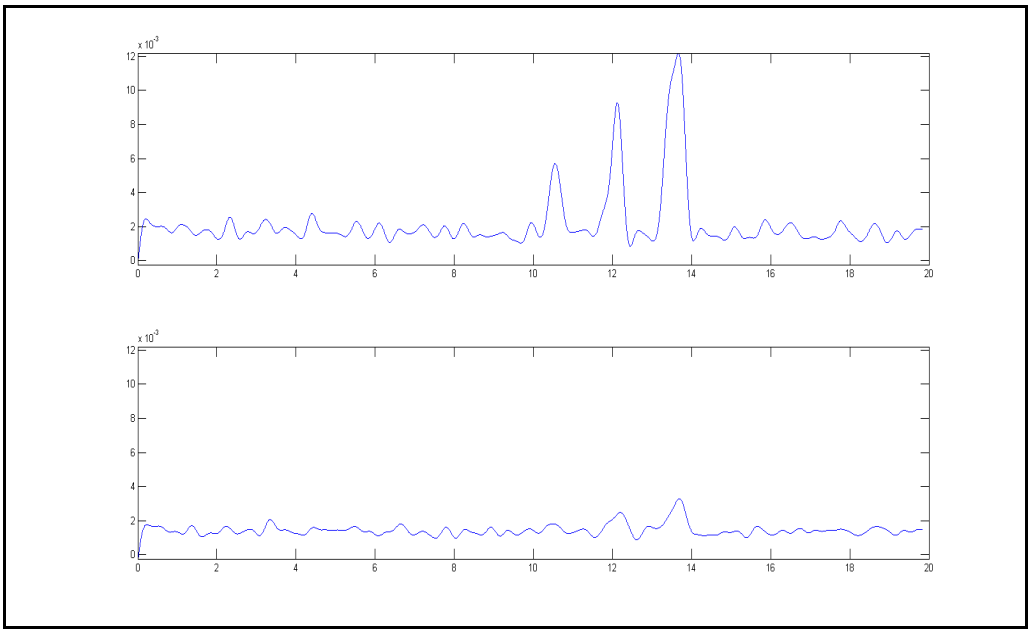

Figure 20: In-Vivo experiment for EMG

We can see some effect of the input channel onto the next empty channel in Fig 20 bottom plot. This accounts from combination of crosstalk from board and chip as well a common reference being fed to all channels. Measures can be taken in future design to mitigate cross-talk from some layout techniques. Fig 21 shows the measurement setup of the complete OTA MUX array in a hospital environment (Intensive care unit-ICU) at Rancho Los Amigos National Rehabilitation Center. Signals are taken from ECoG mini grid implanted in patient's skull (for seizure monitoring). It is constantly being recorded by the hospital system and we extract the signal is parallel to their system. The DUT is shown kept inside a custom made faraday cage from aluminum base. For this particular measurement we could not recover the ECoG signal and could get only up-to 44 % correlation in one of the visits. This can be accounted for a large component of 60 Hz present in the environment and missing ground connection from the patient as it was being used by the hospital system and could not be determined to be safe to connect to our system ground.

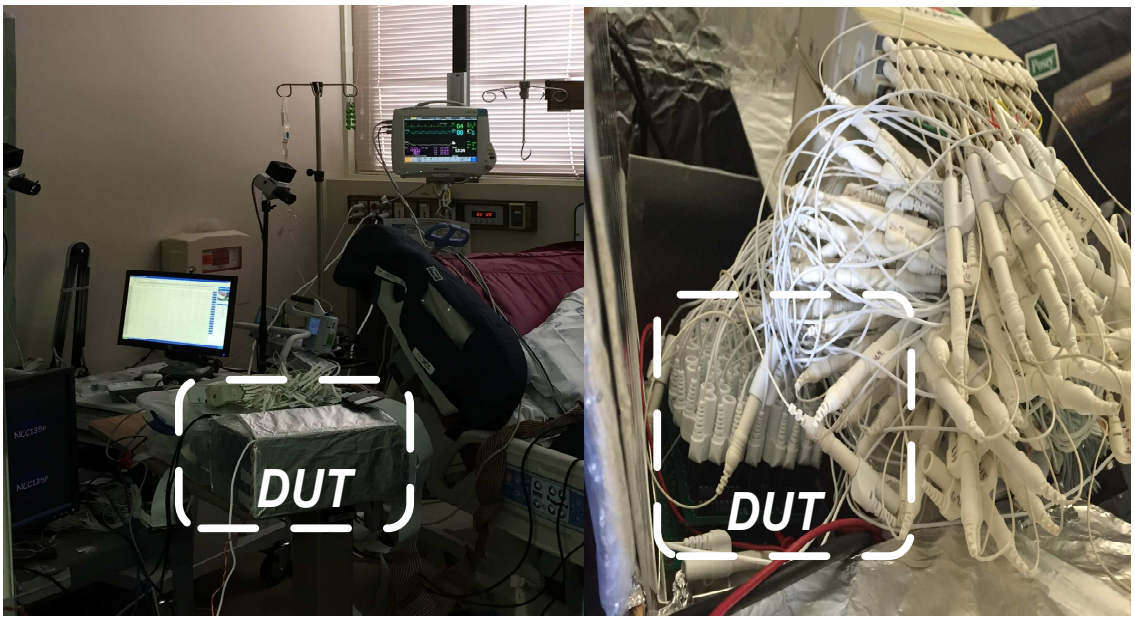

Figure 21: Device Under Test (DUT) In-Vivo measurements for ECoG

Although complete ECoG measurements are not shown here, we were able to detect EEG in an experiment shown in Fig 22. EEG has signal levels (10 – 20 uV) an order of magnitude lower than ECoG (50-100 uV) [18]. EEG was sampled at 500 Hz from one occipital electrode (Oz in the 10/10 EEG system [19] with a frontal reference electrode at AFz) on a healthy human subject while his eyes were opened and closed at different time intervals shown by red and blue color in fig 22. This shows occipital alpha rhythm in frequency band of 8 – 12 Hz which is prominent in humans when awake with closed eyes and shows clear signs of reduction when eyes are open [20]. Fig 22 shows visible difference in alpha band for these two activities with a difference of 10 dB/Hz in power spectral density plot.

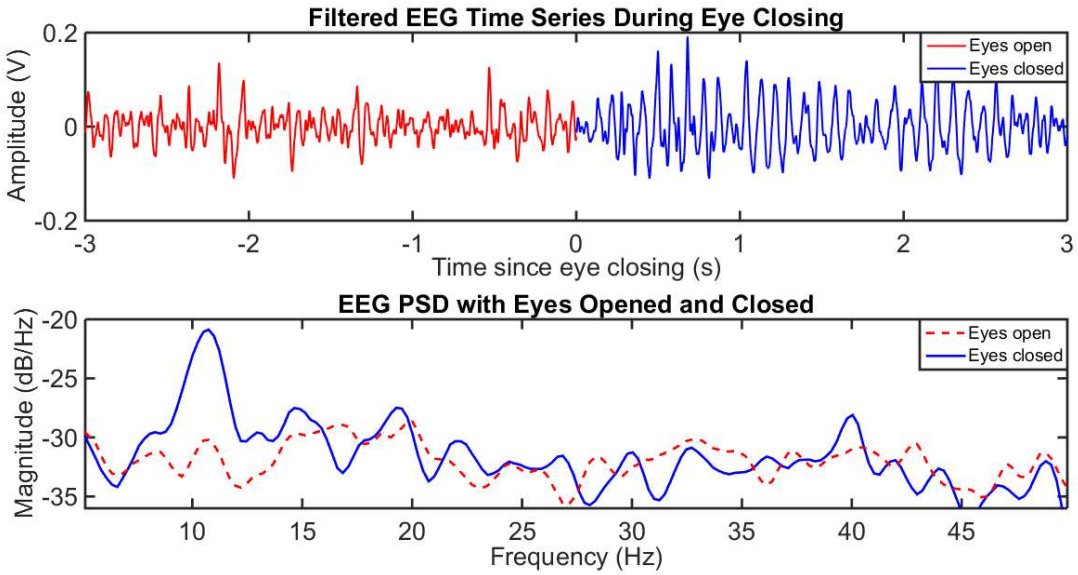

Figure 22: Time series and Power Spectral density (PSD) Plot for EEG

SUMMARY AND CONCLUSION

In this research, a novel OTA operating in WI region have been proposed. Design specifications were based on properties and requirements of ECoG signal and environment. A brief overview on WI region of MOS was given, describing EKV model of MOSFET, important challenges and design considerations when operating in this mode. OTA is consists of a complementary NMOS-PMOS input differential pair with positive feedback for g_m enhancement, CMFB circuitry with linear wide range of operation for low supply voltage and diode connected MOS pseudo-resistor. An array of 64 amplifiers alongside an analog multiplexer have been designed and fabricated in IBM 130nm CMOS process. 100 pin QFN package and PCB have been designed and fabricated for electrical and human measurements of the system. OTA consumes 216nW (Measured) from 0.4 supply voltage

and integrating from 15Hz to ~500 Hz (BW of amplifier), input referred voltage noise of 3.25uVrms (simulated) which yields NEF of 3.84 and PEF of 5.91. The measured gain and BW closely matches the simulation results and design functionality is shown for actual human signals with detection of peculiar alpha waves from EEG of human subject.

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APPENDIX

The appendix includes images of the complete die 4 mm x 4 mm submitted for fabrication fig 23, bonding diagram for packaging the die in a 100 pin 12 mm x 12 mm QFN package in fig 24 and 3-D view images of the custom PCB board designed to house the package and perform bench top and human measurements in fig 25, 26.

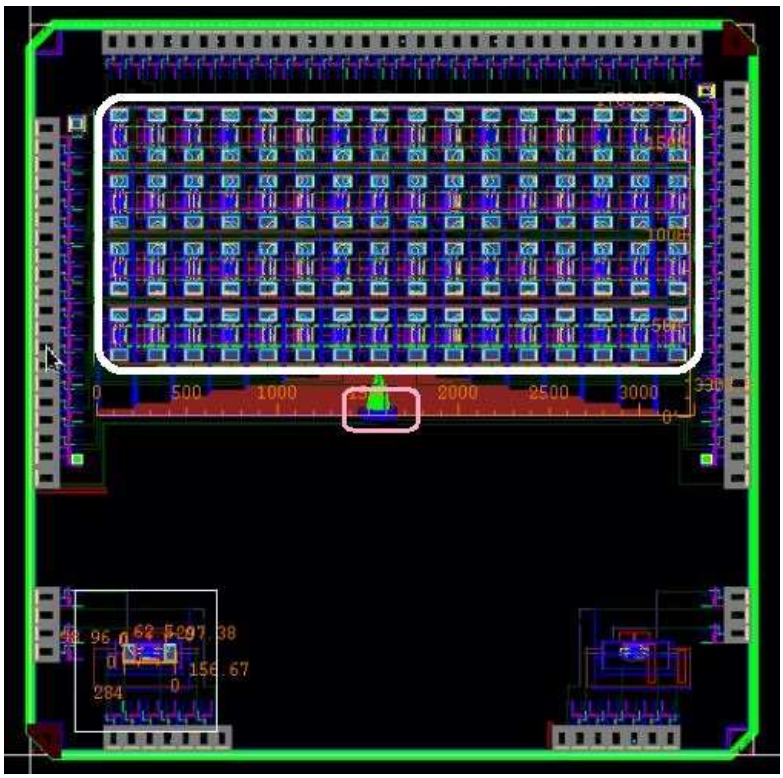

Figure 23: Final layout sent for fabrication. It comprises of array of 64 ULP OTA, analog multiplexer and digital circuitry associated with channel selection.

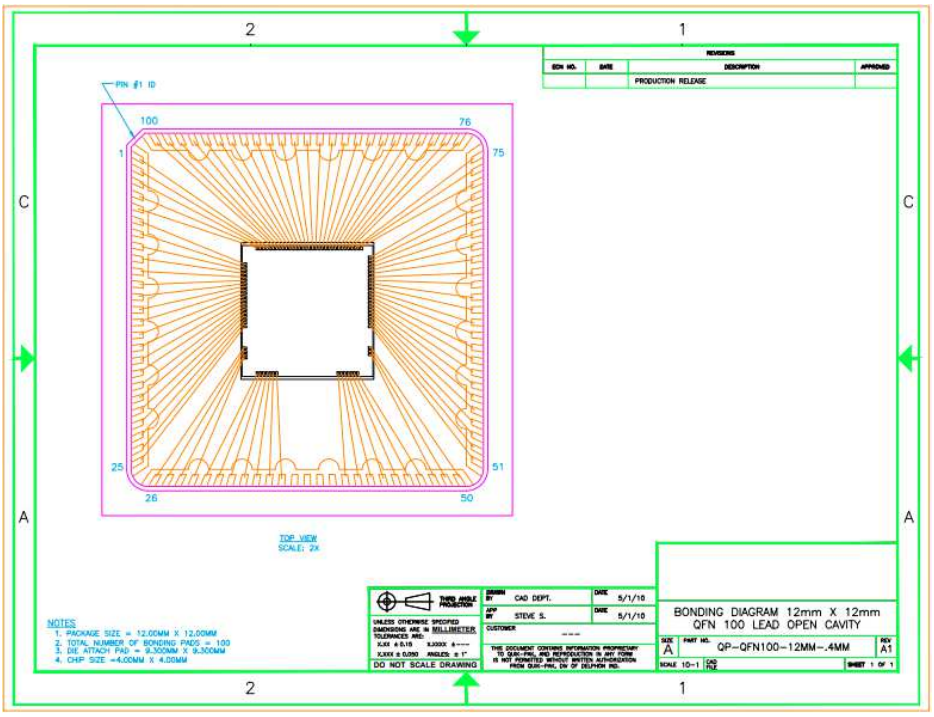

Figure 24: Bonding diagram for packaging a 100 Pin QFN package

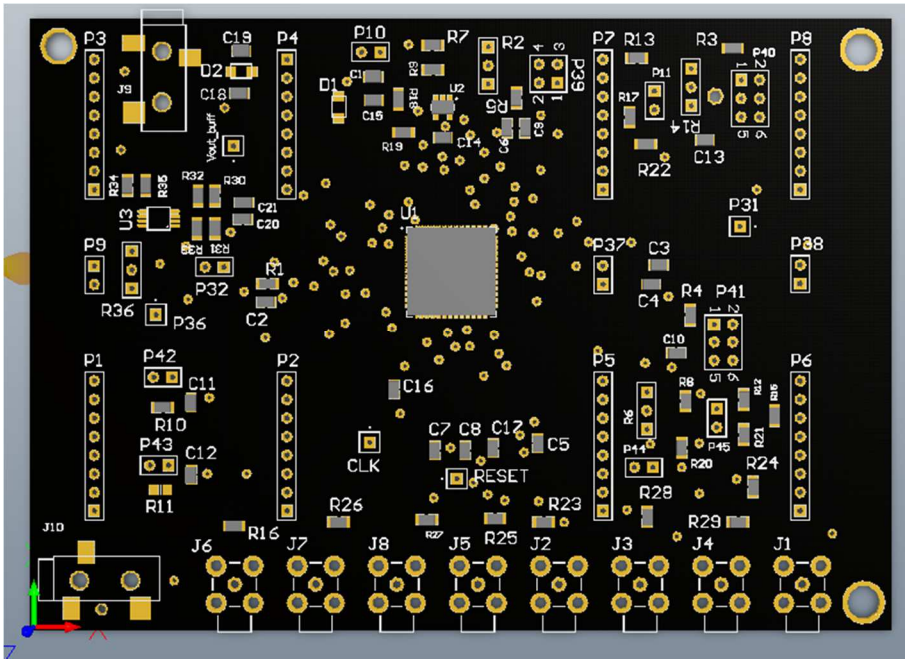

Figure 25: 3-D image of main PCB board with QFN packaged chip and peripheral components

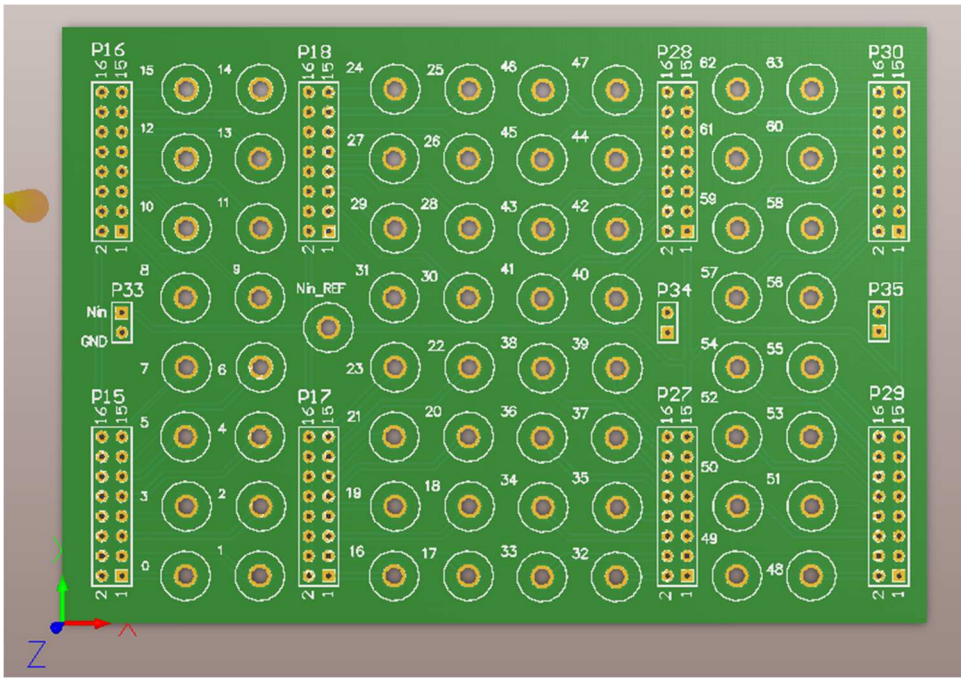

Figure 26: 3-D image of connector PCB board for receiving input from ECoG/EMG/EEG system