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Development of Single Electron Transistors as sensitive charge sensors for impurity spin quantum bits in silicon

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Single electron transistors (SET) are sensitive electrometers [1] that promise to allow single spin measurements through spin to charge conversion schemes [2]. We are developing test devices that integrate single dopant atoms with readout SETs in order to gain access to the physics of coherent spin manipulation of individual donor atoms in silicon [3]. Electron spin coherence times for P doped Si are ~60 ms at 7°K [4], and single spin device physics can become accessible at LHe temperature for silicon SETs with charging energies $E_c=e^2/2C>3.4$ meV=10 k_BT (with C, junction capacitance, T, temperature and k_B, Boltzmann constant). Here, we describe processing and electrical properties of SET pairs in silicon on insulator (SOI). Silicon based quantum wires are defined using the negative resist hydrogen silsesquioxane (HSQ) together with an organic resist in a bi-layer electron beam lithography process. SEM images in fig. 1 show wire mask structures after HSQ development. Si-nanowires (30 nm thick) with widths from ~11 nm to 30 nm were formed in an HBr/Cl_2 etch. In fig. 2, features less than 15 nm wide showed unstable wire width because of some distortions in the organic resist layer after removal of the HSQ hard mask. We have characterized SET structures at 4.2° K with the goal to correlate the topographical structure with electrical properties. We note that the Si-wires shown here are undoped, and nanowire size reduction by oxidation was not applied, due to direct lithographic access to features around 15 nm. Coulomb blockade is expected to result from tunneling junctions formed between the undoped wires and the highly n-doped source and drain electrodes. In fig. 3 (left), we show I-V curves for an SET with a 30 nm wide Si-wire with a total junction capacitance10 aF, a tunneling resistance ~0.3 MΩ and a charging energy of 8 meV. The SET with a 14 nm wide wire (right) had a capacitance of 10 aF and a tunneling resistance of 40 MΩ with E_c=10meV. Coulomb blockade is clearly visible for the SET with the 14 nm wide Si-wire. Modulation of the source drain current as a function of gate voltage is shown in fig. 4 for an SET with a 30 nm wide Si-wire. Here, the gate was placed 100 nm away from the Si-wire and the gate capacitance was only 0.13 aF. Still, a current modulation of about 5 % was achieved. In our presentation, we will discuss process optimization strategies for fabrication of SET pairs in light of the requirements for utilization of SETs as charge sensors in spin to charge conversion schemes for single electron spin readout.

References

[1] K. K. Likharev, IBM J. Res. Develop. Vol.32, p.144, 1989
[2] B. E. Kane, Nature 393, 133 (1998); B. E. Kane, et al., Phys. Rev. B 61, 2961 (2000)
[3] T. Schenkel, et al, J. Appl. Phys. 94, 7017 (2003)
[4] A. M. Tyryshkin, et al., Phys. Rev. B 68, 193207 (2003)

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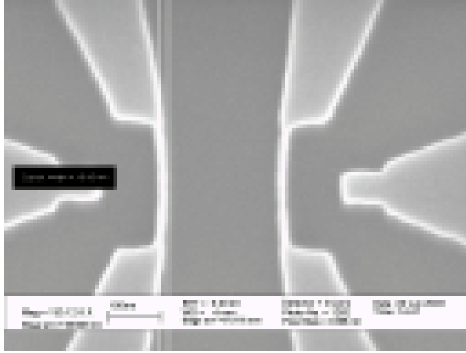


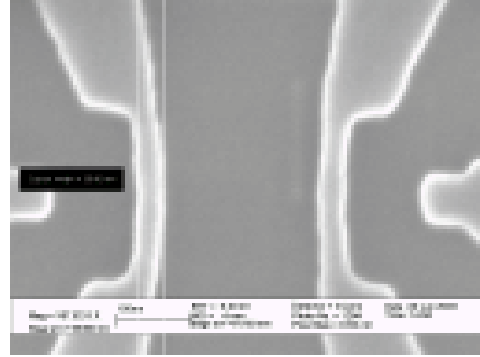
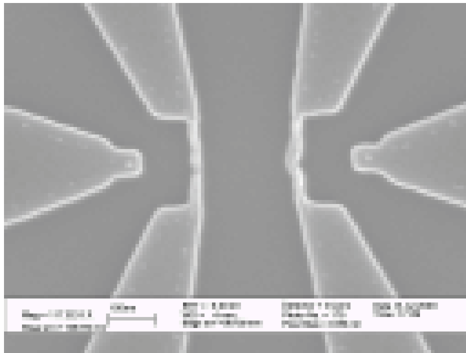


Figure 1: SEM images of SET patterns with 15.8 nm (left) and 35 nm (right) wide wires formed in HSQ.



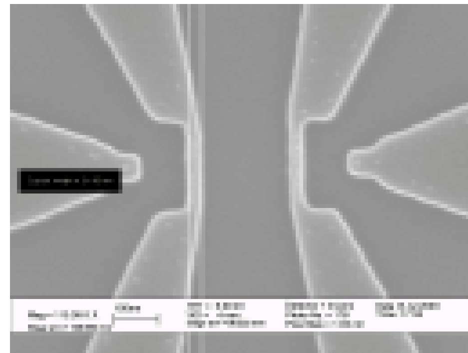
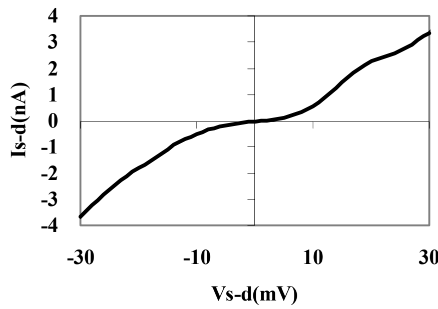


Figure 2: 14 nm (left) and 30 nm (right) nanowire patterns transferred into silicon by HBr/Cl_2 plasma etching and resist removal.



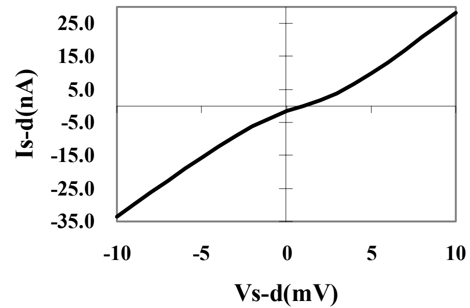


Figure 3: Source-drain current, I_{sd}, as a function of source drain voltage, V_{sd}, for SETs with a 14 nm (left), and 30 nm (right) wide silicon wire.

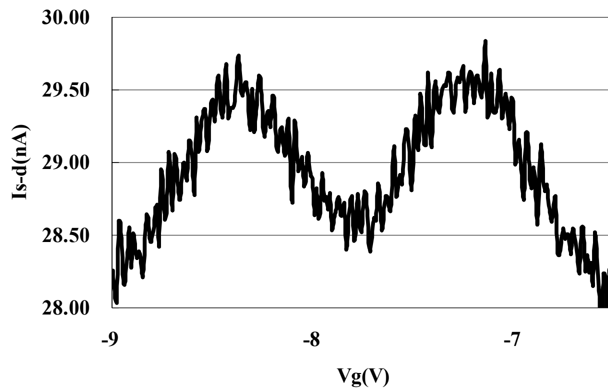


Figure 4: Source drain current modulation as a function of gate bias, V_g, for an SET with a 30 nm wide silicon wire. Here, the source drain bias was set to 10 mV.