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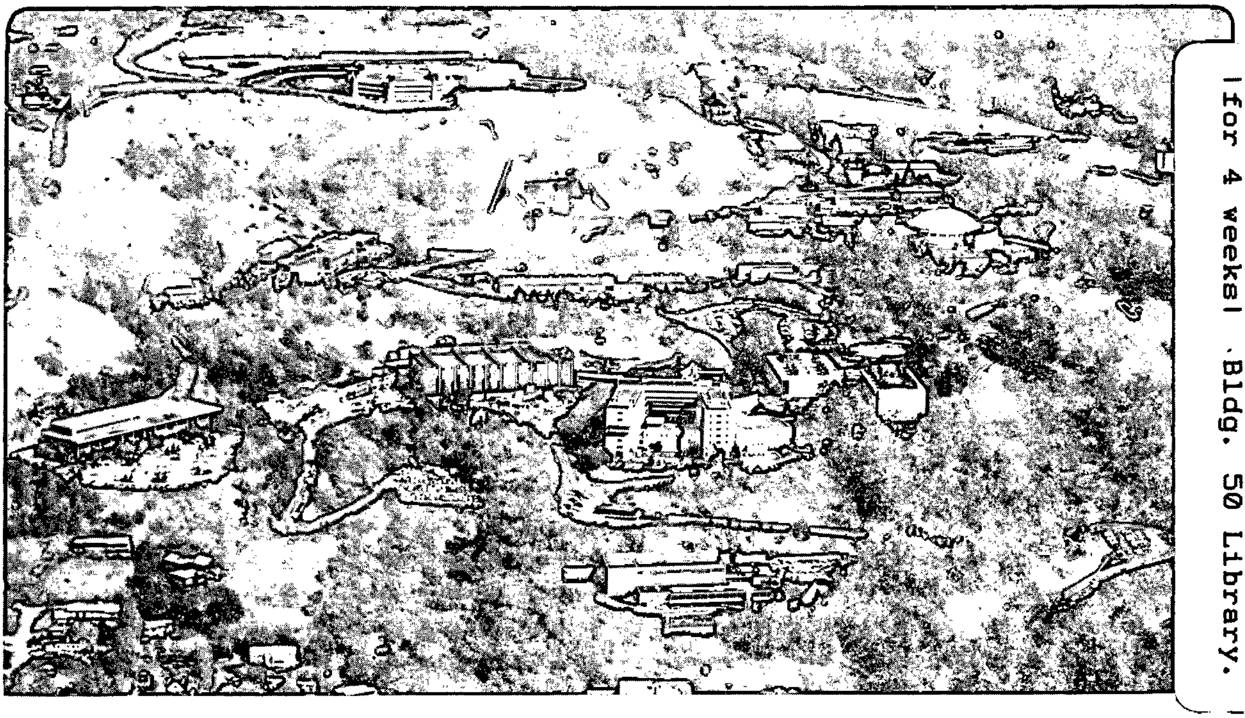

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# THE SIXTEEN CHANNEL CAMAC CONSTANT FRACTION DISCRIMINATOR FOR APEX

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## ABSTRACT

We report on the construction and the performance of a sixteen channel constant fraction discriminator (CFD) for the Atlas Positron Experiment (APEX). We have used an integrated circuit (IC), recently introduced commercially, which contains all the electronic building blocks needed to construct a CFD. We have placed 16 channels of CFD into a CAMAC module. An important feature is the time to charge converter (TQC) that we have included for every CFD channel. Its calibration constant is controlled via CAMAC. The TQC allows the use charge sensitive analog to digital converters (QDC) for timing measurements. Results for CFD walk, resolution and crosstalk as well as for TQC linearity will be presented.

## INTRODUCTION

The ATLAS Positron Experiment (APEX) at the Argonne Tandem Linear Accelerator System (ATLAS) is designed to look for electron-positron pairs emitted in heavy-ion reactions, e.g. Uranium on Uranium at the Coulomb barrier. In similar experiments at the UNILAC at GSI in Darmstadt Germany peaked structures have been found in the positron energy spectra. The nature of these structures is not well understood. APEX is designed to investigate these peaks with better detection efficiency and resolution to contribute to the understanding of the source of these phenomena.

APEX[1] uses a set of coils to generate a homogeneous magnetic field to transport positrons and electrons from the target to two sets of 216 silicon detectors on opposite sides of the target. The two sets are arranged in an hexagonal cylinder, and they are surrounded by two sets of 24 NaI(Tl) scintillator bars to detect the annihilation gamma rays from the positrons stopping the in the silicon detectors. These bars are readout by photomultiplier tubes (PMT) at both ends. The PMTs designed for operation in magnetic fields (Hamamatsu R2490). In addition there is a set of 24 large area position sensitive avalanche detectors at 20° - 70° with respect to the bean direction to detect the scattered beam and recoiling target ions in kinematic coincidence. The experiment is triggered by a coincidence of two NaI(Tl) bars 180° apart.[2] See Fig. 1.

## ELECTRONICS

The block diagram for the signal processing for the silicon detectors is shown in Fig. 2. Since the experiment depends on good time resolution (less than 2ns) and good energy resolution (less than 5keV FWHM), the large number of electronics channels (432) prompted us to develop a fast-slow preamplifier[3,4] a shaping amplifier, a peak detector-stretcher (called Peak to FERA Converter PFC) and a 16 channel constant fraction discriminator. Presently the preamplifier design is being finalized, and production should start soon. The Shaper and PFC are in the prototype stage. The design of the 16 channel constant fraction discriminator is finished and will be described in this paper.

## DESIGN

The design of the CFD is based on ideas previously published[5] and uses fast comparator integrated circuits. As shown in Ref 5 the space available in a CAMAC module permits only 8 channels on a board if standard IC are used. The company Analog Devices has introduced a "rigid disk data qualifier" IC, whose internal logic contains all the building blocks for a CFD, i.e. comparators, coincidences and two one shots, so that one has only to provide the input network and the ECL drivers to the outside world. This IC is the AD891, and it comes in a 14 pin dual inline plastic (DIP) package[6]. The schematic of the CFD is given in Fig. 3. The input network uses plug in headers to define the trigger fraction and lumped constant delay lines with five taps as the constant fraction delay. The stripline impedance at the inputs is 75Ω, and we use a resistor network to match this to the input impedance of 50Ω or 100Ω by selecting the proper parallel termination. Since the impedance of the delay line was chosen to be 100Ω, the resistor net work is determined by the fraction wanted. At the input we couple, via a diode, a test pulse generated on the board. The thresholds are determined by 16 8 bit DAC. We have used DAC IC from which we can read back the set thresholds. The dead time and output pulse width are determined by connecting resistors to ground from the corresponding pins. We found that the variations in the internal reference voltage of the AD891 lead to large variations in the times at the upper end of the range. We have therefore connected the network that determines the times to a +5V reference voltage. This makes the selection of IC for reference voltage unnecessary. We have tried time ranges from 25ns to 250ns and 50ns to 1μs. The resolution for the settings is 4 bit. The output of the AD891 passes to a 3 input NAND gate, where the other two input signals are a common veto, and an individual mask controlled via CAMAC. From there the signal goes to a set of ECL line drivers (logic pulses) and the time-to-charge converters. These are CAMAC controlled current sinks with a range from 0 to -10mA. They can be switched via a jumper to provide fast NIM level signals i.e. 16-mA current sinks. The current sinks can be used to generate time spectra with charge-sensitive ADC's. To do this one feeds the current source to the linear input and a logic signal to the gate input of the QDC. If one arranges the timing such that the leading edge of the current pulse lies within the gate time window, and the trailing edge of the gate pulse lies within the current pulse time window, the charge registered in the QDC is the time between the leading edge of the current pulse and the trailing edge of the gate pulse multiplied by the current. The advantages of this "overlap" method have been discussed by Braunsfurth, et al[7]. This particular implementation was suggested by T. Friese[8].

In addition we generate a OR output and a multiplicity output for trigger generation. The veto input can be used to construct a stand alone TQC with this unit.

The circuit itself is built on a four layer board and uses 34 pin .1 inch center connectors for the signals, except for veto, OR, Test and Multiplicity, which use LEMO connectors.

## PERFORMANCE

The range for the threshold voltage is -50 mV to -1V with 8 bit resolution. The range for the dead time and the output pulse width is 25 ns to 250ns with 4 bit resolution. A mask with 16 bits is used to enable each individual channel. The TQC range is 0 to 10mA with 8 bit resolution. The internal test pulse generator can be triggered from the front panel with a fast NIM signal, or via CAMAC.

Walk and resolution of the CFD have been tested with a pulser with 5ns rise and fall times and 20ns width. The constant fraction delay was 10ns, and the fraction 30%. The measurements show a walk of less than ±200ps from 100mV to 5V, and resolution of less than 50ps.

The crosstalk between adjacent channels is less than 5%, and depends very critically on proper termination and cabling.

The deviation from linearity of the TQC is less than ±200ps from a straight line fit. See fig. 4. Using up to 160 feet of twisted pair cable between the TQC and the QDC did not noticeably affect time resolution and linearity, making it easy to delay the signal used for timing to accommodate the delays in generating triggers, i.e. the gates to the QDC.

## CONCLUSION

Advances in I.C. technology have enabled us to build a very high density constant fraction discriminator, which will be used for several detector types in the APEX experiment, i.e. silicon detectors, NaI(Tl) scintillation detectors, and avalanche detectors. The inclusion of the time to charge converter simplifies the electronics for APEX very much since now only one type of QDC can be used.

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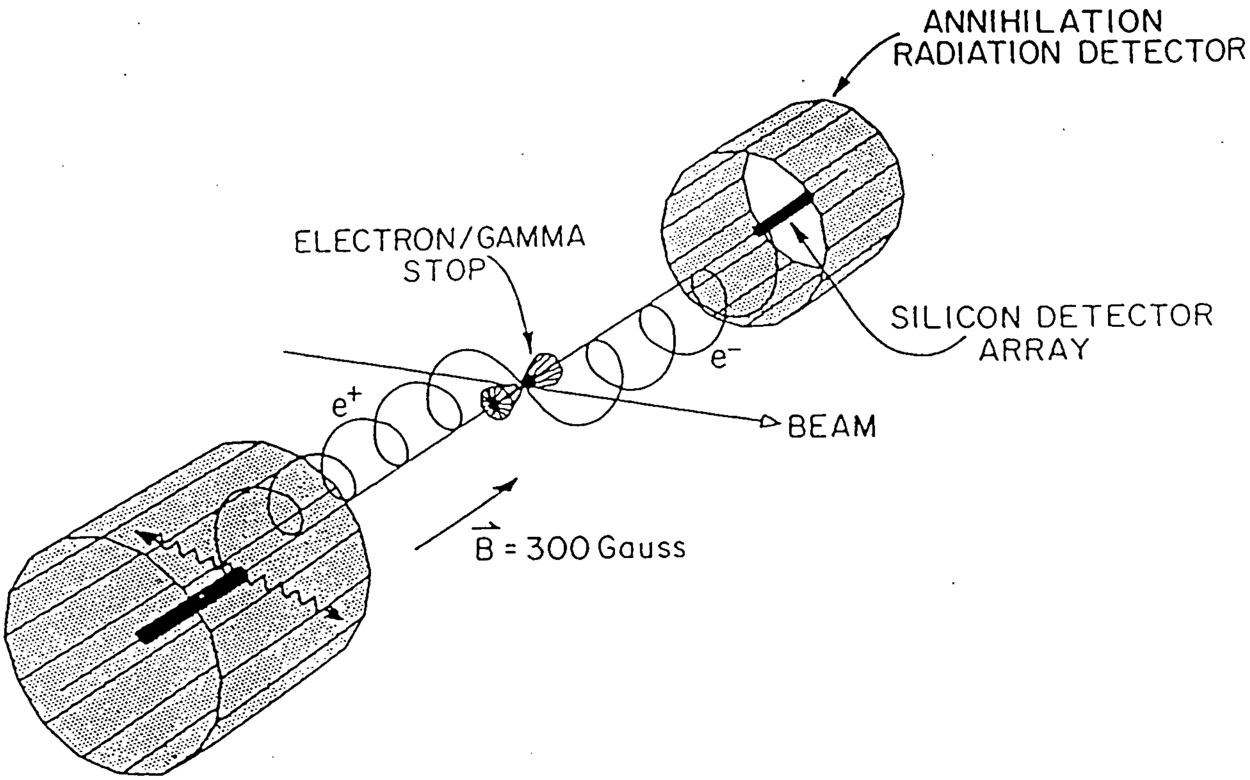
## FIGURE CAPTIONS

Fig. 1 Schematic illustration of the APEX apparatus. Major components are labelled. For the sake of clarity the heavy ion detectors have been omitted.

Fig. 2 Block Diagram of the Silicon Detector Electronics

Fig. 3. a. Constant Fraction Discriminator: Input section one channel
b. Constant Fraction Discriminator: Output section

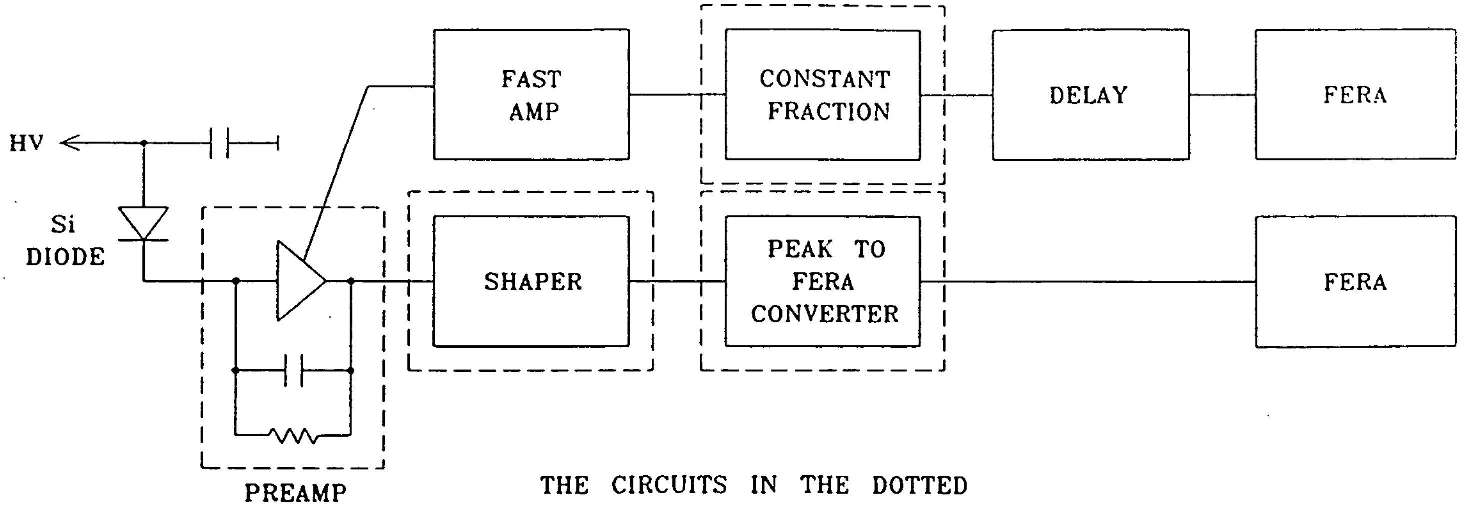
Fig. 4. Deviation from Linearity for the TQC output. The points are spaced 10ns apart.



Schematic illustration of the APEX apparatus. Major components are labelled. For the sake of clarity the heavy ion detectors have been omitted.

Figure 1

# SCHEMATIC OF THE SILICON DIODE ELECTRONICS



THE CIRCUITS IN THE DOTTED BOXES ARE BEING DEVELOPED.

Figure 2

# CONSTANT FRACTION INPUT SECTION, ONE CHANNEL

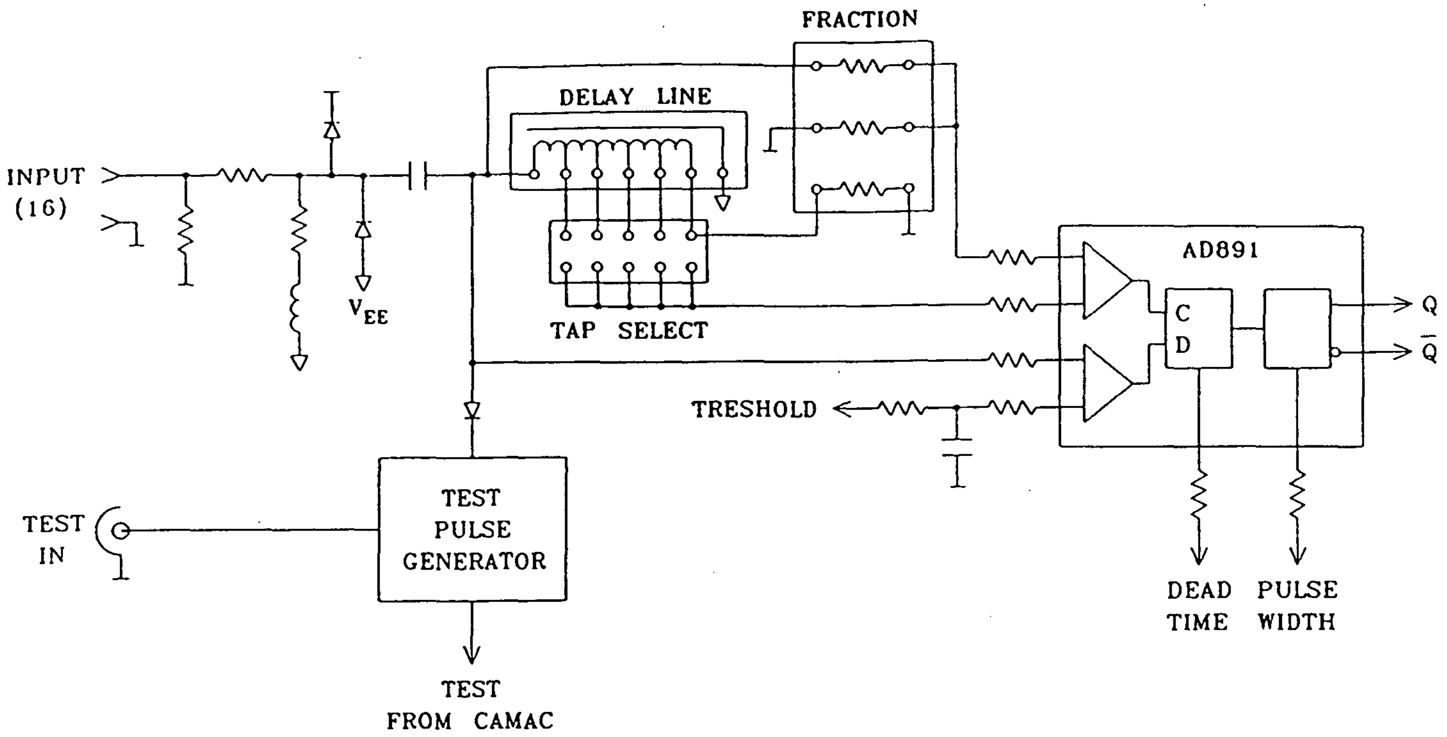


Figure 3a

# CONSTANT FRACTION OUTPUT SECTION

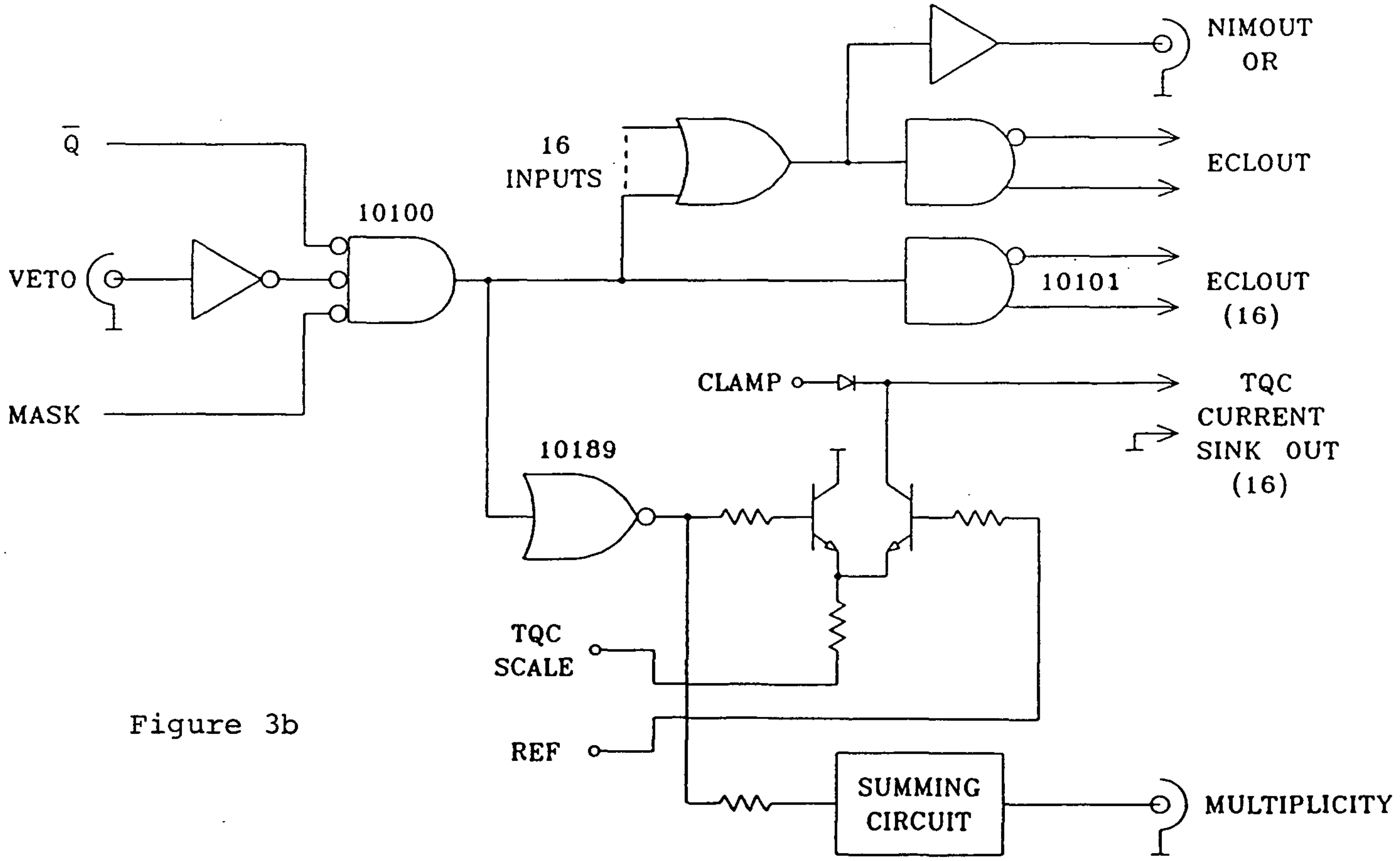


Figure 3b

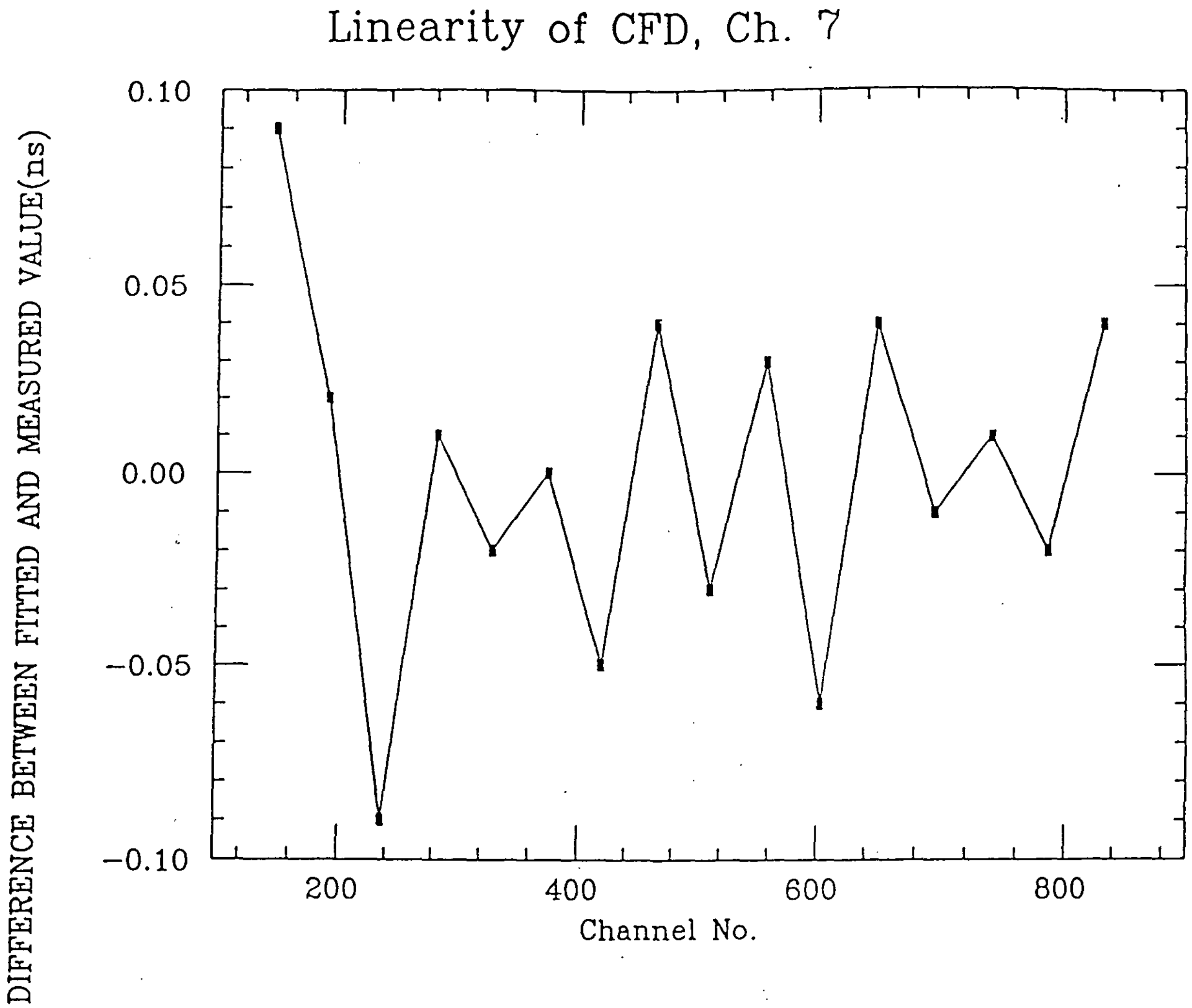

Linearity of CFD, Ch. 7
0.10
0.05
0.00
−0.05
−0.10
200
400
600
800
Channel No.
DIFFERENCE BETWEEN FITTED AND MEASURED VALUE(ns)

Figure 4