Photonic Integrated Circuits for Optical Sensing and Communication

By

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DISSERTATION

Submitted in partial satisfaction of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

Electrical and Computer Engineering

in the

OFFICE OF GRADUATE STUDIES

of the

UNIVERSITY OF CALIFORNIA

DAVIS

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2023

To my family members and my friends

ACKNOWLEDGEMENTS

Pursuing a Ph.D. has been a long, unforgettable, and fruitful experience. I want to thank my advisor, Distinguished Professor S. J. Ben Yoo, who has provided me with constant support and inspiring guidance since 2016. His knowledge and insight in the integrated photonics area guided my research. More importantly, his hardworking attitude and well-organized habits set a standard for an excellent researcher.

I want to thank my dissertation committee members, Prof. J. Sebastian Gomez-Diaz and Prof. Weijian Yang, for providing guidance and advice on my dissertation.

I want to thank everyone in the Next Generation Networking and Computing Systems (NGNCS) group. Kuanping Shang was my mentor in my first year. His careful training in photonic device design and fabrication built my foundation in photonics research. I want to thank Yu Zhang for giving me enlightening guidance. His comments and advice helped me accomplish many research tests, and he shows an excellent example of teamwork. I want to thank Mathias Prost and Tiehui Su for their photonic device characterization training, Siwei Li for the development of the flip-chip bonding process, Yi-chun Lin for his help on photonic integrated chips characterization, and Hongbo Lu for his research work in the ERON project. I also want to thank Chuan Qin, Shaoqi Feng, Guangyao Liu, Gengchen Liu, Kaiqi Zhang, Mingye Fu, Hang Su, Yujia Zhang, Jingwei Wan, Zhennan Wu, Zhixing Lin, Rijuta Ravichandran, and Yiting Jin for their help and encouragements.

I also want to thank my friends who helped me in the nanolabs, including Xiaoer Hu, Zeying Ren, Qianyi Xie, and Hanbin Song, for their advice and accompanying. I want to thank all my

friends who helped me through the seven years, including Qiutong Jin, Xuan Ding, Xiaoyu Yang, and Wenjin Pei.

I want to appreciate all staff in UC Berkeley Marvell Nanofabrication Laboratory and Center for Nano-MicroManufacturing, including Dave Taosaka, Allison Dove, Richelieu Hemphill, Ryan Rivers, Sam Tsitrin, Jay Morford, Jason Chukes, Joanna Bettinger, Daniel Martinez, Ryan Anderson, Chan Kim, Vishal Narang, and Paula Lee.

Finally, I want to thank my family for their love and support. My parents and grandparents supported me unconditionally during my Ph.D. study. I want to thank Kaiyi Wu, Hong Yang, and Ziyao Guo for their encouragement.

ABSTRACT

Photonic integrated circuits (PICs) are widely used in various applications, such as optical sensing, computing, and communication, thanks to the development of multiple photonic components, including light sources, waveguides, couplers, splitters, combiners, multiplexers, detectors, and modulators. Many material platforms can be employed for PICs. Silicon photonics taking advantage of the mature complementary metal-oxide-semiconductor (CMOS) fabrication technology stands out as a good choice. Silicon-on-insulator (SOI) platform is attracting more interest since it is CMOS compatible, cheap, and scalable. Silicon nitride (Si_3N_4) platform is also CMOS compatible and can be a supplementary and substitution of the Si platform in some cases, especially when low propagation and high scalability are required. Complex integrated photonics systems usually require the integration of many platforms.

The explosive growth of the demands for sensing and data transferring drives the development of integrated photonics. For example, future autonomous vehicles require low-cost, high-performance light detection and ranging (LIDAR) systems. Optical interconnects are proposed and being explored for modern high-performance computing (HPC) systems. Modern astronomy needs a small size, weight, and power consumption optical sensing system to significantly reduce the cost. Integrated photonics are continuously being explored and developed for higher performance and lower cost.

This dissertation presents the development of PICs for optical imaging and communication. Chapter 1 introduces integrated photonics and briefly introduces all the works in this dissertation. Chapter 2 presents our multi-layer Si_3N_4 platform, including the device design, simulation, fabrication, and measurement. This chapter experimentally demonstrates our multi-layer Si_3N_4

platform. Chapter 3 proposed and demonstrated a low-loss and broadband optical interposer for large-scale integration. The interposer includes low-loss inter-chip couplers and can be extended to a wafer scale, which shows great potential for large-scale heterogeneous integration for modern sensing and communication systems.

Chapters 4 and 5 discuss the segmented planar imaging detector for electro-optic reconnaissance (SPIDER) realized by PICs for astronomy. The SPIDER uses interferometric imaging based on PICs and can significantly reduce the size, weight, and power consumption compared to traditional bulk optical devices. Chapter 4 presents a SPIDER imager formed by many chips and a high-resolution SPIDER imaging achieved using a wafer-scale fabrication technique. Chapter 5 presents a surface-coupled SPIDER imager based on a broadband surface coupler.

Chapter 6 investigates the PICs for an elastic RF-optical network. The PICs are based on our multi-layer Si_3N_4 platform and include arrayed waveguide grating (AWG), multi-mode interferometer (MMI), and thermal phase shifters. The PICs show the capability of generating optical signals for RF-beam forming.

Chapter 7 summarizes the dissertation.

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Chapter 1 Introduction

1.1 Overview of photonic integrated circuits

The invention of fiber optics communication in the 1970s [1]-[3] and integrated circuits (IC) in the 1950s built the foundations of integrated photonics. By integrating photonic devices (including lasers [4]-[6], modulators [7],**Error! Reference source not found.**, amplifiers [9], light-emitting diodes [10], waveguides [11]-[14], multiplexers [15], splitters [16], combiners, and detectors [17] on chips, the optical signal can be generated, transmitted, processed, and detected using photonic integrated circuits (PICs). Compared to traditional bulk optical devices, the PICs significantly improve the cost and performance of the optical systems by minimizing the size, weight, power consumption, and device fabrication cost, thus offering excellent solutions for modern sensing, communication, and computing systems.

An electron is a fermion with electron spin 1/2, while a photon is a boson with spin one, so photons do not obey the Pauli exclusion principle. During transmission, the photons move at the speed of light with almost no interference between photons, which allows dense wavelength division multiplexing (DWDM) [18], while electrons move at a low speed, and the electrons will repel each other. As a result, signals that carry information transmit lower loss and higher bandwidth in PICs than in ICs. Besides, natural and manual light sources exist everywhere, providing an excellent sensing and imaging stage.

Waveguides are one of the most essential elements in integrated photonics. Waveguides in integrated photonics usually consist of a core material with a higher refractive index and a cladding material with a lower refractive index. The waveguide platform can decide the index contrast, material loss, fabrication difficulties, and capability to generate or modulate optical

signals of all its devices. PICs can be fabricated on many platforms, here are the leading platforms in integrated photonics:

- III/V material: InP-based platforms are excellent in fabricating active devices, including lasers [19] and detectors [20], for their direct band. GaAs's high electron mobility enables high-speed devices such as modulators [21]. The platform is challenging to scale up due to its high propagation loss and fabrication difficulties.
- Silica: The Silica platform [22] uses doped Silica as the waveguide core material. Silica waveguides have a low refractive index that supports a low-loss transmission while suffering from a large device footprint since the bending radius in the silica platform is large. The silica platform can achieve high-performance passive devices such as filters and AWGs [23]-[24]. Meanwhile, it is not suitable for active devices.
- Lithium niobate: The thin film lithium niobate (TFLN) platform [25]-[30] is used for fabricating high-performance modulators [31],[33] and is suitable for nonlinear optical devices [34]. However, it is hard to fabricate thin-film lithium niobate on top of CMOS chips since the TFLN fabrication technology is not as mature as silicon. The stress and thermal budget limit the fabrication of TFLN devices. Besides, the TFLN also suffers from the absence of photo generation capability, so it requires an external light source.
- Silicon-on-insulator (SOI): Silicon photonics are built on the SOI platform [35], which has high core-to-cladding refractive index contrast. The high confinement of the Si/SiO_2 waveguide allows the Si platform to achieve passible optical devices in a small footprint. The carrier injection/depletion in Si enables modulators on the Si platform [36],[37]. Silicon photonics can utilize the mature CMOS fabrication technology and can be directly integrated with CMOS devices. Meanwhile, Ge can be epitaxially grown on Si

for fabricating photodetectors and modulators [38]. However, the indirect band of Si makes it challenging to fabricate light sources such as lasers.

- Silicon nitride: Silicon nitride platform [39] is also CMOS-compatible and can utilize CMOS fabrication technology. The refractive index contrast in the SiN/SiO_2 platform is between the Si and silica platforms, so its device footprint is also between the two platforms. The Silicon nitride platform can support passive devices but is not suitable for active devices since it is a dielectric. Besides, silicon nitride is widely used in nonlinear optics.
- Germanium. Germanium is a group IV material heavily used in silicon photonics for multiple reasons [40]-[42]. High-quality crystalized germanium can be epitaxially grown on top of a single crystallized silicon layer using an ultrahigh-vacuum chemical vapor deposition (UHV-CVD), and this growth can be a selective growth in which Ge is only grown in a designed trench [43]-[45]. Rapid-melting growth is also used for Ge deposition. Germanium is widely used in silicon photonics foundries for photodetectors [46]-[49] and electro-absorption modulators (EAM) [50],[51]. Ge laser is developed since the band structure of Ge can be engineered using proper doping and tensile strain engineering [52],[53]. Furthermore, Ge is transparent in medium wavelength infrared (MWIR) to enable long-wavelength applications [54],[55].
- Polymer: The polymer platform includes many materials, such as PMMA [56]. The polymer platform usually has a low fabrication cost and high flexibility but cannot stand processes, including annealing, O_2 plasma cleaning, and wet chemical cleaning. Besides, the polymer devices will degrade during aging.

The above information shows that none of the platforms can cover all the applications of integrated photonics, so complex optical systems may require the integration or packaging of many platforms.

1.2 Large-scale heterogeneous photonic integrated systems

The growing demand for high throughput communication and sensing requires large-scale heterogeneous photonic integrated systems [57]. Compared to most of the electronic integrated circuits built on the Si platform, complex electrical and optical systems may not be achieved on a single platform. For example, a modern communication system requires optical signal generation, modulation, routing, multiplexing/demultiplexing, amplification, and transmission on the transmitter side. Besides, electrical signals for controlling and monitoring are also necessary. The systems must use the packaging or integration of many platforms since none of the platforms can support all the building blocks individually. Besides, the heavy data traffic in data centers requires communication in many channels simultaneously. Co-packaged optics (CPO), which contains the heterogeneous integrations of multiple chips onto one substrate, is explored to increase bandwidth and energy efficiency.

Another approach for increasing the integration density is using multi-layer structures, which stack multiple devices vertically to increase the device density several times. The multi-layer devices require inter-layer coupling and isolation so the layers can work independently with connections.

Optical sensing is another area that requires large-scale heterogeneous optical systems. Light for detection and ranging (LIDAR) [58] provides 3D sensing for many applications, such as autonomous cars. The performance of the LIDAR usually improves with increasing the aperture size to support higher optical throughput. In optical imaging, the imaging system's resolution is

usually decided by the size of the aperture, so a large scale is required to achieve high imaging quality.

Si and silicon nitride platform plays an essential role in the large-scale heterogeneous photonic integrated system for the following reasons:

- Low propagation loss: The low propagation loss in Si and silicon nitride platforms allows signal routing on a large scale. Especially, the Si_3N_4 waveguide can achieve a down to 0.1dB/m loss, which is negligible when routing on 6-inch wafers.
- Low coupling loss: Si and silicon nitride platforms can support many surface/edge couplers, such as inversed taper, sub-wavelength grating edge couplers, and grating couplers.
- Capability of supporting optical devices: Si and silicon nitride platforms can achieve almost all optical devices except for high-performance light sources.
- CMOS compatibility. The Si and silicon nitride platform can be fabricated using the mature CMOS foundry, which can support 12-inch wafers. Besides, the electrical ICs are directly fabricated on the same wafer.
- Germanium epitaxial growth: Germanium can be epitaxially grown or deposited onto the Si for realizing high-speed electron absorption modulators and photodetectors.
- Flexibility on multi-layer fabrication: The silicon and silicon nitride can support inter-layer couplers. Utilizing wafer bonding and smart cut technology, multiple Si layers can be transferred to the top of another wafer. Silicon nitride can be directly deposited on top of a wafer. Si and silicon nitride layers can be integrated into one wafer using CMOS-compatible fabrication technology.

- III/V compatibility: III-V materials can be heterogeneously integrated into silicon photonics chips using direct wafer bonding or adhesive wafer bonding to realize lasers, modulators, and detectors. Due to the lattice constant mismatch between silicon and III-V materials, the epitaxial growth of high-quality III-V materials on silicon is complex and can introduce defects such as threading dislocations, micro-cracks, and anti-phase domains. Progress on quantum dots offers solutions for high-performance lasers on Si substrate.

The dissertation first introduces our multi-layer silicon nitride platform and its application. Design methodology, fabrication techniques, and measurement techniques are discussed and verified.

1.3 Low-loss and broadband wafer-scale optical interposer

Optical interposer to support many function blocks with electrical and optical connection brings a solution for complex electro-optics integrated systems [59], such as large-scale light detection and ranging (LIDAR) [60] with large emitting aperture area occupation, and high-performance computing (HPC) systems assisted by optical interconnect. Such systems require the optical interposer to have large-scale, high integration density, high throughput, high energy efficiency, and low packaging difficulty.

A critical component in the optical interposer is the inter-chip coupler, which couples light between the interposer and packaged chips for supporting a high-efficiency signal transfer between elements under achievable packaging quality, with enough bandwidth to support applications. Inter-chip couplers based on gratings typically suffer from a high coupling loss and narrow bandwidth. Polymer waveguides offer a low-loss and broadband inter-chip coupler

solution at the cost of low reliability and temperature tolerance. In this chapter, we use evanescent coupling between chips, which uses the same principle as the inter-layer coupler presented in Chapter 2. A low-loss compact silicon nitride platform enables low-loss and broadband transition for inter-chip coupling due to the low index contrasts between the core and cladding material, which brings excellent potential to the optical interposer. Another concern of the interposer is to enlarge the interposer to a large scale with acceptable cost and yield. Die size in traditional CMOS fabrication using projection lithography is limited by the exposure region. On the other hand, contact lithography can expose the whole wafer in one shot, but it has limited quality, uniformity, and minimum feature size.

This dissertation will present a low-loss broadband inter-chip coupler with high packaging tolerance to support applications from 1200nm to 1600nm wavelength and a wafer-scale energy distribution for large-scale integration.

1.4 Large-scale PICs for optical interferometric imaging

Interferometry retrieves images from the interference of superimposed waves and is widely used in fiber optics, astronomy, and spectroscopy. Interferometers for interferometry require sampling from input signals and reconstructing images from the interference visibility [62]. The recent development of the Segmented Planar Imaging Detector for Electro-optical Reconnaissance (SPIDER) imager utilizes multi-layer Si_3N_4 photonics integrated circuits (PICs) to reconstruct images with a smaller size, weight, and power compared to traditional optical telescopes with a similar resolution. The SPIDER system has multiple baselines to sample the image of objects in the Fourier domain and reconstruct the image based on the measured interference fringes. The length and number of the baseline set a hardware limitation on the image quality of a SPIDER imager. Thus, large-scale integration is required for high-resolution SPIDERs.

Our 1st demonstrated SPIDER systems use a single PIC with a 22mm×22mm chip size, which can only get and process information from one dimension at a time. For imaging, we need to rotate the PIC to extract data from a two-dimensional plane, which limits the imager's latency and stability. Our new SPIDER system uses a 21 PICs system to achieve real-time imaging by placing the PICs in a radian shape. Besides, we explore the route to extend our imager to a wafer scale for high-resolution imaging.

This dissertation presents a SPIDER imaging system with multiple chips for achieving imaging in real time. Furthermore, we present an ultra-large SPIDER imager for high-resolution interferometric imaging.

1.5 Surface-coupled SPIDER imager

The 1st generation of the SPIDER imager uses edge coupling, which significantly limits the position of all the optical inputs since all of them must be arranged along almost one axis. Surface couplers provide great potential for the SPIDER since the baselines can be arranged in a 2D plane and collect singles in many directions using a single wafer at one time. However, traditional surface couplers based on gratings have limited bandwidth, so they cannot lead to broadband detection. We propose and design the 1st and 2nd version of the broadband surface coupler based on a 45° mirror for the broadband imaging applications. The mirrors are fabricated by a Si anisotropic wet etching and can achieve wafer-scale uniformity. As a proof-of concept demonstration, we design surface-coupled SPIDER PICs by replacing the optical inputs of the 1st generation SPIDER PICs with surface couplers. By integrating the surface coupler with the SPIDER imager, we can achieve a surface-coupled SPIDER imager, which significantly extends the flexibility and capabilities of the SPIDER imager.

In this dissertation, we present a surface-coupled SPIDER imager using a broadband surface coupler. The fabrication of the SPIDER imager is in wafer-scale, which shows a great potential for a wafer-scale surface-coupled SPIDER imager.

1.6 PICs for an elastic RF-optical network

The progress in RF photonics and radio over fibers offers low-cost, low latency, and energy-efficient solutions for the next-generation communication system [63], [64]. One critical issue in communication is how to generate multiple spatial beams in mmWave from a single-phased array antenna. Our previous work proposes an Elastic RF-optical Networking (ERON) architecture for a flexible 5G RF photonics integrated system. The distributive units (DUs) in ERON include all base-band units (BBU) and digital-to-analog converters (DAC) resources. The remote-antenna units (RUs) in ERON are solely responsible for mmWave beamforming and generation.

This dissertation presents the 1st and 2nd generation of PICs for the RU in the ERON architecture and demonstrates a mmWave two-beam spatial-division multiplexing (SDM) system from a single patch phased array antenna (PAA). The PICs are fabricated on the multi-layer silicon nitride platform.

1.7 Organization of the dissertation

The dissertation will present and discuss integrated photonics for communication and sensing. Chapter 2 introduces the PICs platform, including component design/simulation, layout, fabrication, and characterization. Chapter 3 presents the silicon photonics interposer for large-scale heterogeneous integration. Chapter 4 presents PICs for high-resolution interferometric imaging, including device design, layout, fabrication, and characterization. Chapter 5 investigates the surface-coupled SPIDER imager using a broadband surface coupler. Chapter 6

discusses PICs based on a multi-layer silicon nitride platform for realizing multi-beam forming in ERON architecture.

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Chapter 2 Design, Fabrication, and Characterization of Multi-Layer Silicon Photonic Devices

2.1 Silicon nitride platform overview

This chapter presents an overview of the multi-layer silicon nitride platform, including the design, simulation, fabrication, and characterization of the components.

The development of silicon photonics offers low-cost and high-performance solutions for communications, sensing, and computing [65]. Typical silicon photonics devices are built on a silicon-on-insulator (SOI) platform [66], so silicon photonics can benefit from the mature semiconductor fabrication technology and be integrated with CMOS. The relatively large refractive index difference between silicon and silicon dioxide at around 1550nm wavelength ensures relatively high optical confinement of the optical mode inside the silicon waveguide core, which makes silicon photonics devices on the SOI platform compact but sensitive to fabrication errors. Silicon has semiconductor properties that enable carrier-concentration-based plasma electro-optical tuning on active silicon photonics devices [67], such as modulators and switches [68]. At the same time, its indirect band makes it difficult to make light sources and high-performance photodetectors on silicon. Heterogeneous integration of other materials introduced to silicon photonics, such as silicon nitride, III-V materials, germanium, and lithium niobate, add diverse capabilities to silicon photonics integrated systems. Silicon nitride is one of the most widely used materials in silicon photonics for its unique properties. The refractive index of the standard stoichiometric silicon nitride is 1.99 at 1550nm wavelength, which is lower than the refractive index of silicon (3.48).

The relatively small refractive index difference between the core material and the silicon dioxide cladding (n_{sio2}=1.44 at 1550nm wavelength) on the silicon nitride waveguide leads to a relatively low optical confinement factor compared to silicon waveguide counterparts. Figure 1 (a) and (b) show the schematics of a silicon waveguide and a silicon nitride waveguide with dimensions marked on the plots. The core material is fabricated into a rectangle in the cross-section view and surrounded by silicon dioxide cladding. The fundamental TE mode of the waveguides is simulated using finite difference analysis algorithms from the Lumerical FDE solver, as shown in Figure 1 (c) and (d). The simulation area is 5μm × 5μm to ensure the boundaries will not influence the waveguide mode. The simulated mode shows that compared to silicon waveguides, silicon nitride waveguides can have a larger mode size and less confinement factor. Although the mode size, mode shape, and confinement factor of both silicon and silicon nitride waveguides can be engineered according to their applications, silicon nitride waveguides are usually more suitable when a low confinement factor is required.

The use of silicon nitride in photonic integrated circuits (PICs) leads to the following advantages and applications:

- High fabrication error tolerance. Silicon nitride devices are less sensitive to fabrication imperfection, including dimension changes and side wall quality than silicon devices due to their low refractive index contrast, than Si platform. Figure 2 indicates the relationship between the waveguide width and the effective index of the fundamental TE mode. Silicon waveguide's effective index is more sensitive to the waveguide width than silicon nitride.
- Low optical transmission loss [69]. Silicon nitride waveguides usually have a lower loss when the silicon nitride is deposited by low-pressure chemical vapor deposition (LPCVD)

compared to silicon waveguides. When plasma-enhanced chemical vapor deposition (PECVD) is used on deposition, the loss depends on the tuning of the deposition recipe and post-treatment like annealing. Usually, a silicon nitride waveguide made by PECVD will be higher than a LPCVD one but still lower than a silicon waveguide [70],[71].

- Large transparency window. Silicon nitride is transparent in visible light wavelength, while silicon absorbs light below 1.1μm wavelength. So, the silicon nitride platform is widely used in visible spectrum devices [72].
- High optical power tolerance. Some of the silicon photonics devices require high optical power, especially for sensing and nonlinear optics, where a silicon nitride platform is used. Silicon has multi-photo absorption in near-infrared wavelength, which brings high loss and temperature on a working silicon device with high power [73].
- Large mode size. Silicon nitride waveguides have a low confinement factor, so they can expand the beam to a large size with a small numerical aperture (NA). This property leads to high-performance edge couplers [74] to a standard SMF-28 fiber and couplers for free space optics. The large mode size of the silicon nitride waveguide also allows light to transmit from the silicon nitride layer to another layer through a large gap (0.5-2μm) with a low loss (less than 1dB).
- Fully CMOS compatible. Silicon nitride is a dielectric already being used in CMOS foundry, and it can use the well-developed CMOS fabrication technology and will not introduce ion contaminations. Besides, the silicon nitride, including annealing, can stand the CMOS-compatible temperature in CMOS fabrications.

- Nonlinear properties [75],[76]. Silicon nitride can accommodate high power with low optical loss, making it suitable for nonlinear optics. Silicon nitride platforms can make nonlinear optical devices, including optical frequency comb (OFC).
- Flexibility on multi-layer fabrication. The high-quality SOI wafers are fabricated by SmartCut technology [77], in which the top silicon layer is bonded from another wafer. Multi-layer silicon structure requires multiple times of wafer bonding, which brings high price and low yield. A silicon nitride multi-layer platform can be fabricated by depositing a silicon nitride layer on a planarized silicon dioxide surface using LPCVD or PECVD [39],[78].

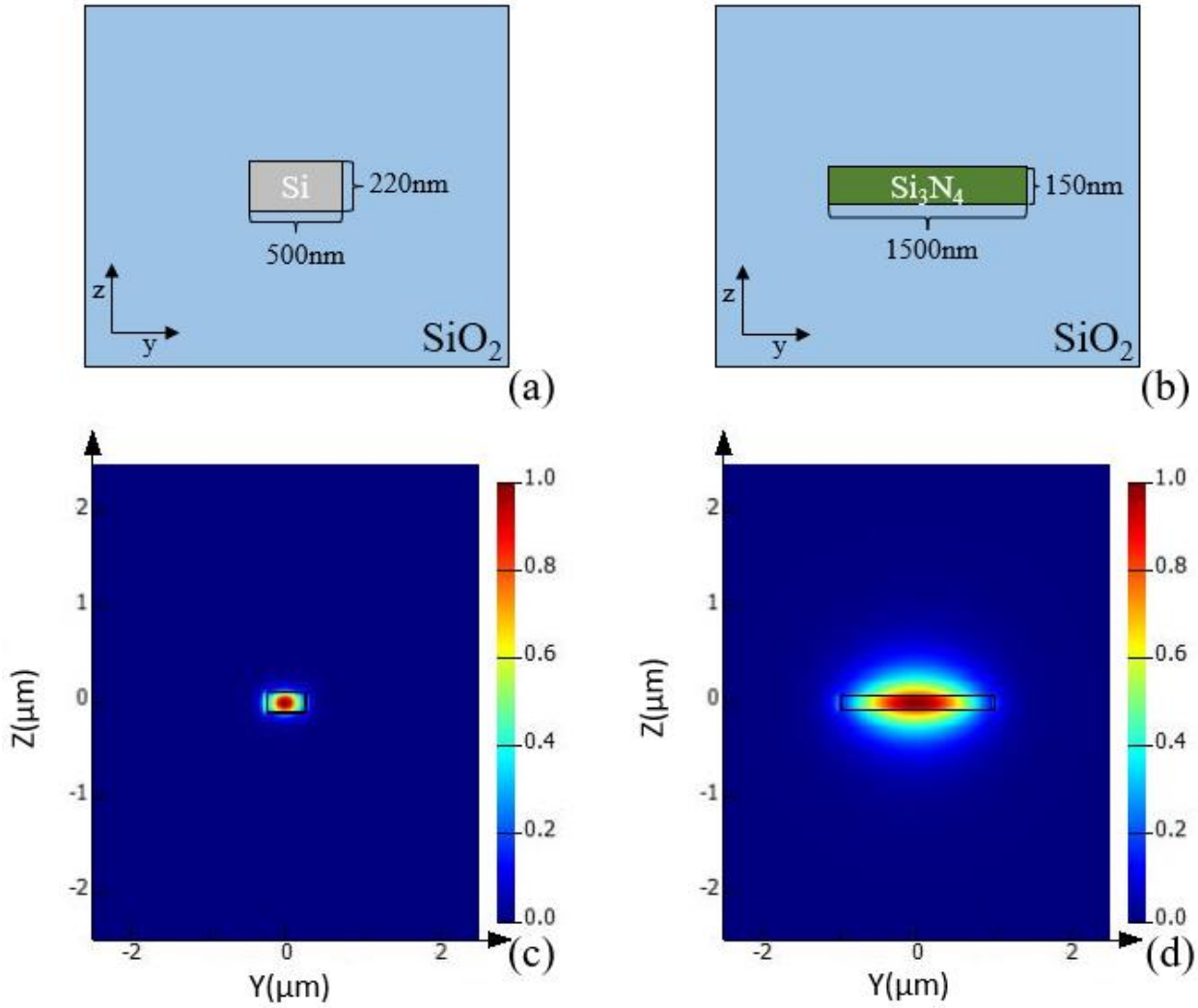


Figure 1 (a) The schematic of a typical silicon waveguide embedded in silicon dioxide at cross-section view. The thickness of silicon is 220nm, and the width of the silicon is 500nm. (b) The schematic of a typical silicon nitride waveguide embedded in silicon dioxide, at cross-section view. The thickness of silicon is 150nm, and the width of the silicon is 1500nm. (c) and (d) the simulated fundamental TE mode in (a) and (b), respectively. The simulation area is 5μm by 5μm.

Silicon nitride photonics are suitable for making passive devices with high performance. Dimension-sensitive integrated photonic devices like arrayed waveguide grating (AWG) [79]-[81] benefit from the high fabrication error tolerance and low loss from the silicon nitride platform to achieve low crosstalk, low insertion loss, and high wavelength accuracy. As a result, the silicon nitride AWGs usually have better performance than silicon AWGs. Silicon nitride

ring resonator and disk resonator have high-quality factor (Q) when it uses proper design and fabrication [82],[83].

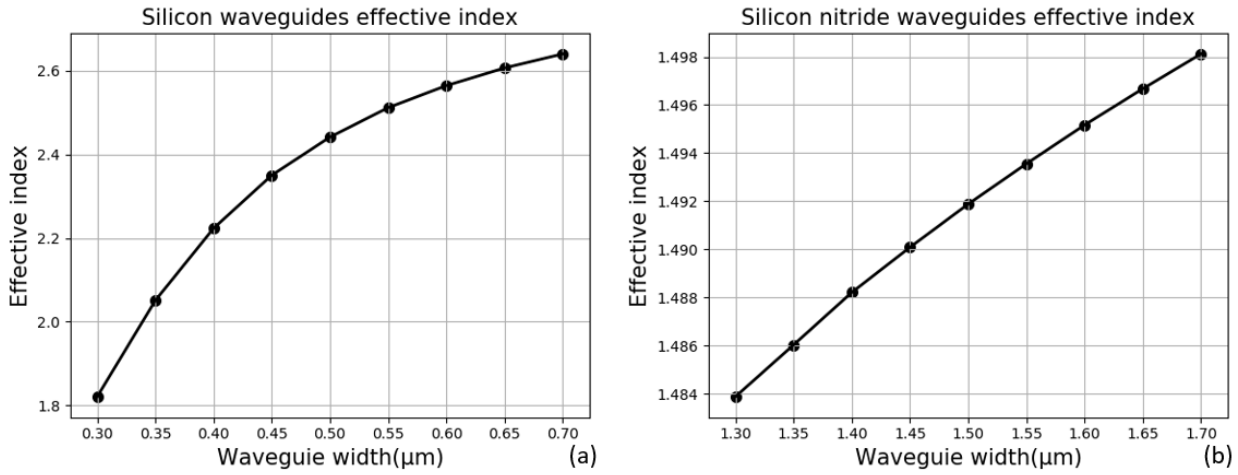


Figure 2 (a) Effective index of a silicon waveguide with 220nm core thickness with varying waveguide width (around 0.5μm). (b) The effective index of a silicon nitride waveguide with 150nm core thickness with varying waveguide width (around 1.5μm). Lumerical FDE simulates the effective index.

2.2 Silicon nitride devices simulation and layout

Simulation has become an essential tool for device design, optimization, and analysis thanks to computing technology advances. Although all classical electromagnetics problems can be calculated by solving Maxwell's equations, the computing capability sets limitations on extensive device simulations, which brings the importance of applying proper approximations to simplify the calculations.

The finite-difference time-domain (FDTD) method directly solves Maxwell's equations using a grid-based method to simulate the transmission photonics devices, demonstrated by Kane Yee in 1966 [84],[85]. The simulation accuracy and cost depend on the grid size in space and time. The

FDTD simulation can use a pulse as an excitation to get a broadband response of a system. We use commercial software Lumerical FDTD to perform 3D FDTD simulation. The FDTD method takes a long time to simulate resonance structures such as high Q ring resonators.

The finite element method (FEM) is a method to solve partial differential equations by dividing an extensive system into small finite elements [86]. The FEM simulation can simulate the time-harmonic response of a linear system with a single frequency. FEM simulation usually takes longer than FDTD when the simulation dimension on each axis is more significant than a few times the wavelength unless the system requires a long time to achieve a steady state. For simulating the transmission spectrum of a device, we need to repeat the simulation for each frequency we need in the spectrum.

The beam propagation method (BPM) solves simplified Maxwell's equations, assuming the optical beam transmits near one axis by removing the fast-varying terms [87]. The approximation in BPM enables a fast simulation as a cost of accuracy. The BPM can give results with unacceptable accuracy when the beam is transmitted with a large angle from the central axis in the simulation.

Most of the simulation tools and algorithms for silicon photonics and RF circuits can be used directly in silicon nitride device simulation since they solve Maxwell's equations. However, the low confinement of the silicon nitride devices brings extra difficulties by expanding the simulation area. Silicon nitride devices usually have a larger footprint than silicon devices to realize a similar function, and the large mode size on silicon nitride devices requires more space around the devices to accommodate the whole working area. In practice, it is impossible to optimize a large silicon nitride device like AWG using FDTD or finite element method (FEM)

from a basic modal because of the size and complexity of such a device. We first design a basic design using the analytic method, which must be finished first to simplify the simulation and then perform a full-size device simulation to verify and optimize the design. Since silicon photonics devices' dimensions are usually larger than a few times the wavelength, 3D FDTD simulation is preferred over FEM to minimize the simulation time and memory consumption.

2.3 Multi-layer silicon nitride platform

2.3.a Multi-layer silicon nitride platform

The multi-layer silicon nitride platform integrates multiple devices on a high-density chip by arranging them into multiple vertical function layers. Each function layer can work independently, which requires low crossing loss and crosstalk between the two layers. A loss interlayer coupler allows light to transmit through any of two function layers. Besides, the multi-layer silicon nitride platform can also be integrated with other platforms, such as SOI, silica, thin film lithium niobate and III-V platforms [92]-[94].

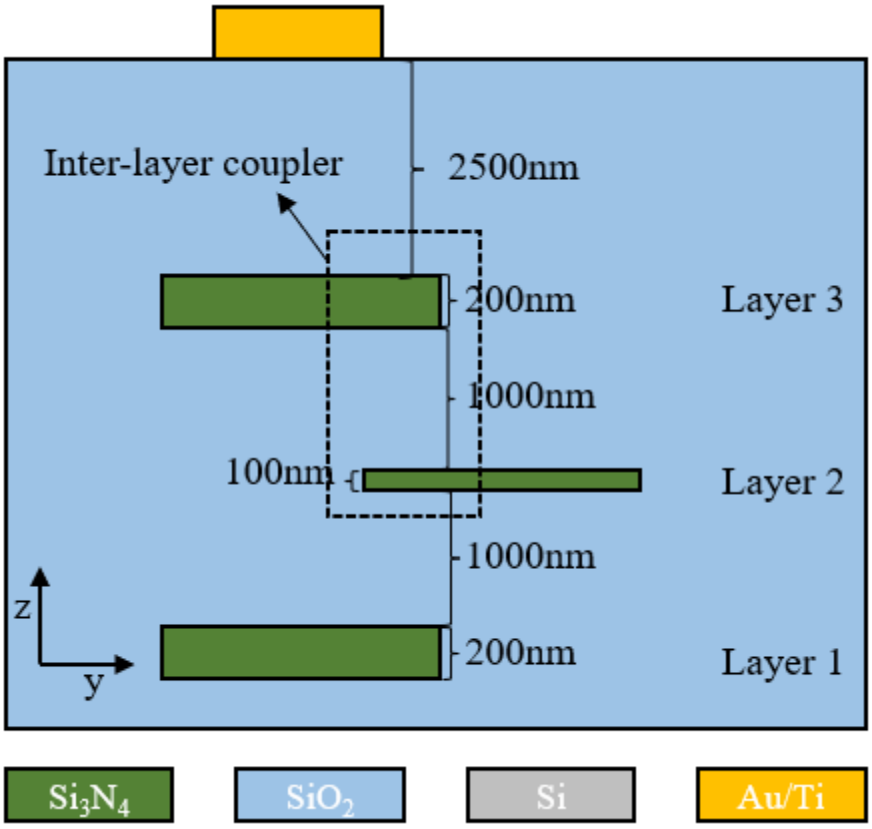


Figure 3 Diagram of the multi-layer silicon nitride platform. The silicon nitride platform consists of 3 layers and one metal layer for thermal tuning. Layer 1 and 3 are function layers, while layer 2 is a transition layer.

Here, we introduce one of our standard silicon nitride platforms, shown in Figure **3**. The platform is fabricated on a 6-inch silicon substrate with silicon dioxide as cladding material and silicon nitride as core material. Layer 1 and 3 are function layers with 200nm thick silicon nitride core. A transition layer with 100nm thickness is added into the middle of the two function layers to enlarge the gap between them while keeping the gap between 2 adjacent layers at 1μm. The gap between the two function layers is around 2100nm, optimized by minimizing the sum of the inter-layer coupling loss and inter-layer waveguide crossing loss—the top cladding with 2.5μm thickness to isolate the metal layer and the silicon nitride layers. The metal layer uses Au to tune the silicon nitride devices thermally. During fabrication, a 20nm Ti is deposited before the Au to

maintain the adhesion between the Au on top of the silicon dioxide. Since the heating occurs at the top surface, the thermal phase shifters in the platform usually use waveguides in the top layer to maximize the tuning efficiency.

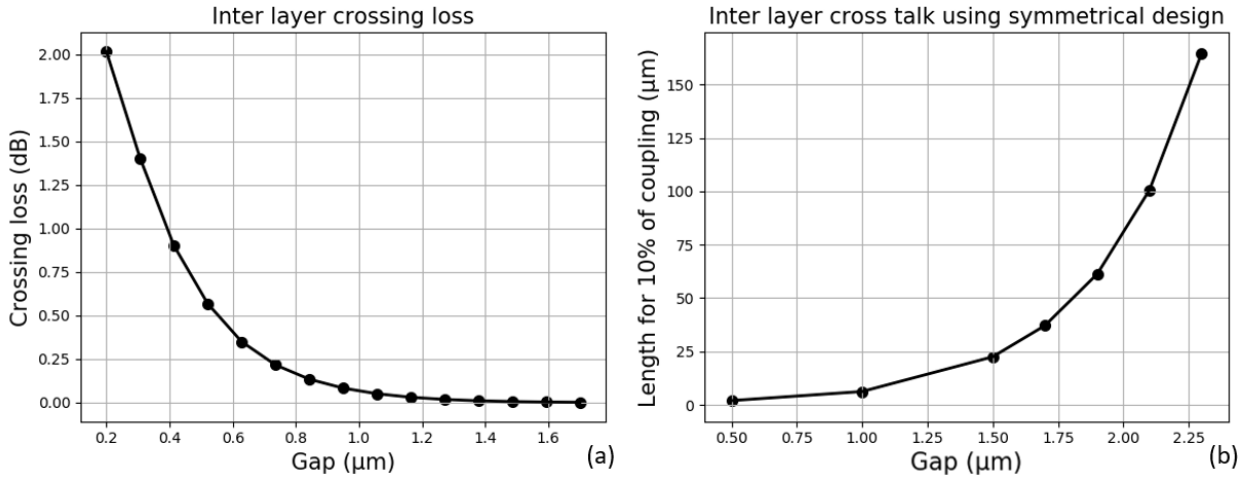


Figure 4 (a) Inter-layer crossing loss with varying gap thickness. The waveguides at the 2 layers have 200nm waveguide thickness and 2µm width. (b) Inter-layer crosstalk with varying gap thickness. The waveguides at the 2 layers have 200nm waveguide thickness and 2µm width and overlap with each other. The y-axis shows the length of 10% of crosstalk between the two layers.

The inter-layer crossing loss and crosstalk are simulated, as shown in Figure 4. In this simulation, the waveguide width for both layers is 2µm. The crossing loss is simulated using the FDTD method, assuming all crossings are at 90 degrees. During simulation, we cross the waveguides in two layers multiple times and calculate the average insertion loss. The crossing loss is negligible when the gap is higher than 1.5µm, demonstrating optical isolation between the two layers. The inter-layer crosstalk is calculated, assuming the two waveguides perfectly overlap with each other. At a 2.1µm gap, it takes 100µm to couple 10% of the energy to another layer, which indicates that the waveguides using the same design should avoid overlapping in a long range. Asymmetrical design can significantly reduce the interlayer cross talk, in which the waveguide width on the two layers is different.

2.3.b Low-loss inter-layer coupler

A low-loss inter-layer coupler based on evanescent coupling, demonstrated by Kuanping Shang [39], allows light to transmit light through different layers [88]. Inter-layer couplers based on gratings [89],[90] and vertical directional couplers[91] are also explored. The grating couplers typically have a higher than 3dB coupling loss and a less than 60nm bandwidth. The vertical directional coupler can achieve an around 0.19dB loss, but the bandwidth is also limited. Besides, the coupling efficiency of the inter-layer coupler at a certain wavelength highly depends on the gap thickness. The inter-layer coupler we proposed have a low coupling loss, large bandwidth, and high robustness against fabrication imperfections.

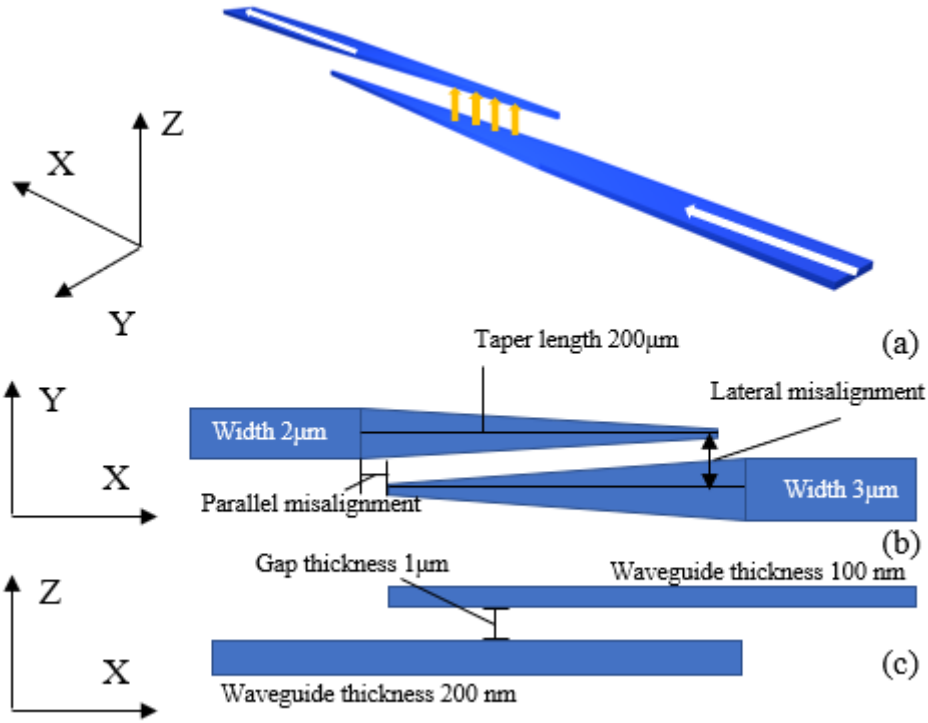


Figure 5 (a) 3D diagram of the inter-layer coupler. The white arrows indicate the light transmission through the waveguides, and the yellow arrows indicate the light transmission through the two waveguides evanescently. (b) Top view of the interlayer coupler. (c) Cross-section view of the inter-layer coupler [39].

Figure **5** (a) shows the diagram of the inter-layer coupler, which consists of a pair of inverse tapers on the two layers that overlap in opposite directions. During transmission, the light will be expanded with the narrowing of the waveguide at the input inverse taper and be coupled into the output taper gradually. Around the end of the input taper, the input waveguide width is too short to support an eigen mode while the light is transmitted through the output waveguide mode. Ideally, the taper end width should be as small as possible, not only to make sure that no waveguide mode is supported at the end of the taper but also because part of the light will be reflected at the beginning of the output taper due to the discontinuity of the waveguide. A large taper end width will cause reflections and result in an extra loss when the gap is short. In applications, the taper end width is limited to the minimum feature size that the fabrication process can achieve, which is usually defined by lithography. We use the ASML^{TM} PAS 5500 300 deep-UV lithography stepper in UC Berkeley Marvell Nanolab, and a minimum 250nm feature is achievable in this facility. Figure **7** (b) shows an SEM photo of a fabricated silicon nitride inverse taper to show our fabrication capabilities. We use 250nm taper end width in the following design, simulation, and fabrication of the interlayer coupler to meet our fabrication capability. Another fabrication error that needs to be considered is the misalignment between multiple times of lithography.

Figure 8 shows the influence of the extra loss from the misalignment. It needs to be noticed that in inter-layer coupler design, a proper offset at the parallel direction can reduce the loss, especially at long tapers. The ASML^{TM} PAS 5500 300 deep-UV lithography stepper we use can achieve less than 60nm misalignment, so this extra loss is usually not considered during fabrication.

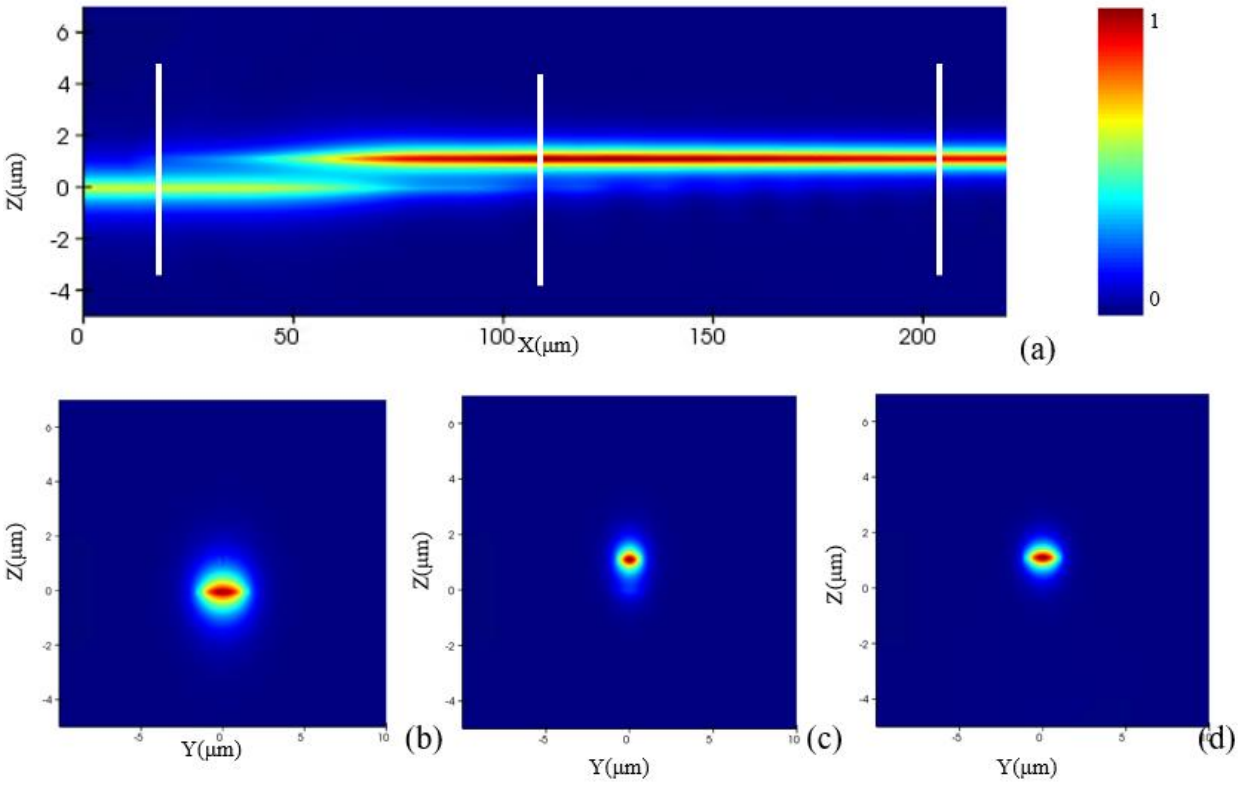


Figure 6 (a) Simulated inter-layer coupler at the XoZ plane. The input waveguide has a 100nm thickness and 3μm width. The output waveguide has a 200nm thickness and 2μm width. The inter-layer coupler has a 1μm gap. The three whit lines denote the beginning of the output taper, the middle of the tapers, and the end of the output taper, whose cross-section view of the E-field at YoZ plane (in Figure 5) is shown in (b), (c), and (d), respectively.

In the silicon nitride platform we proposed, the inter-layer transition of the light happens only between a function layer and a transition layer, which have 200nm and 100nm thick silicon nitride waveguide core thickness, respectively. Figure **6** shows the simulated E-filed from a working inter-layer coupler, from a transition layer to a function layer. The taper length is 200μm since a sharp change in the waveguide width may excite high-order modes and bring extra loss and uncertainty to the coupling. The optical signal incident from the input waveguide is coupled into the output taper evanescently through the 1μm gap and confined into the fundamental mode of the output waveguide with almost full energy. The relationship between the coupling efficiency and the gap thickness is simulated and shown in Figure **7** (a). The reflection at the

beginning of the output taper contributes a little to the total loss when the gap is below 1μm. Limited by the mode size conversion capability of the silicon nitride taper, the coupling loss becomes high when the gap is above 1.4μm. The coupling loss when the gap is high (>1.4μm) can be further minimized by enlarging the taper length. Figure 9 (a) shows the relationship between the coupling loss and the taper length at a 1.4μm gap, suggesting that the taper length design is a tradeoff between the coupling loss and the footprint. The parallel offset usually requires optimization when the taper length is high.

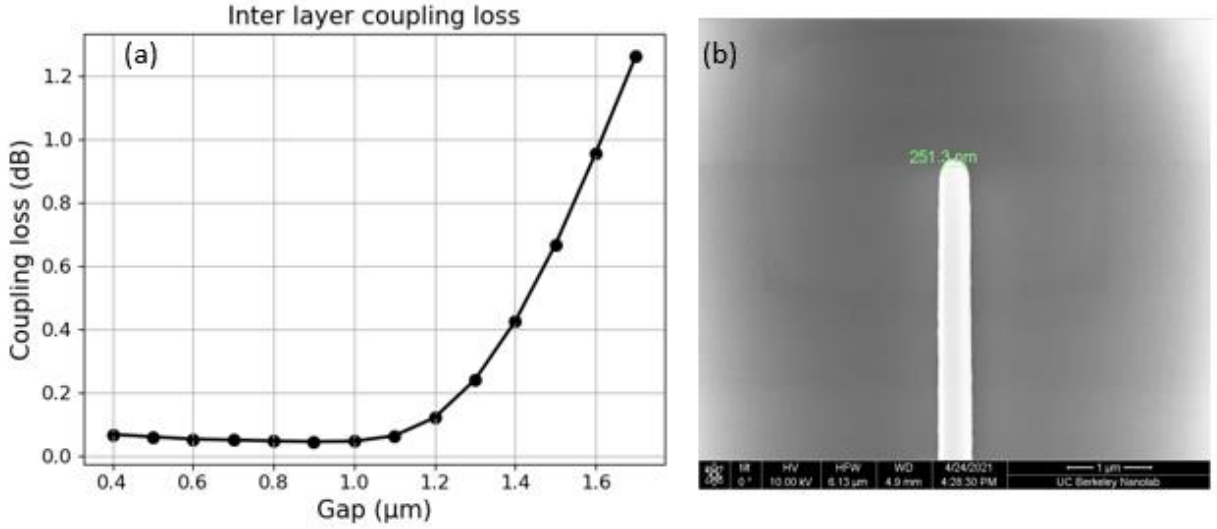


Figure 7 (a) Simulated inter-layer coupling loss with varying gap thickness. The input waveguide has a 100nm thickness and 3μm width. The output waveguide has 200nm thickness and 2μm width. (b) An SEM photo of the inter-layer coupler at the end of the taper.

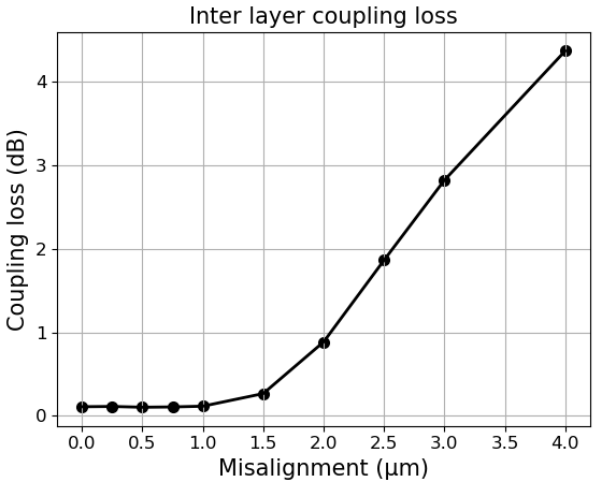


Figure 8 (a) Simulated inter-layer coupling loss with varying lateral misalignment. The input waveguide has a 100nm thickness and 3μm width. The output waveguide has 200nm thickness and 2μm width. The inter-layer coupler has a 1μm gap and 200μm taper length.

The silicon nitride platform requires optimization in different working scenarios. As the increasing of the gap thickness between a function layer and a corresponding transition layer, the gap between the two function layers increases twice faster and results in lower crossing loss and crosstalk, while the inter-layer coupling loss becomes higher. In the diagram proposed in Figure **3**, the crossing is much below 0.05dB per crossing, so it is almost negligible, and the inter-layer coupling loss is below 0.1dB per coupling. The crosstalk between the two function layers can be high when two devices overlap perfectly. However, this crosstalk can be significantly reduced by carefully routing and positioning devices on different layers and using asymmetrical design. The total loss from the waveguide crossings and the inter-layer couplings can be calculated once the layout is finished, so it can be minimized by adjusting the gap thickness. The inter-layer coupling loss can be reduced by using a longer taper when the gap is high (>1.4μm, at 1550nm wavelength), as a scarify to the footprint. If extremely low crossing loss or crosstalk is required, we can add more than one transition layer. Crosstalk can be almost zero when the gap is about 1.6μm, while an almost zero crosstalk at any condition requires a much higher gap thickness.

Figure 9 (b) shows the inter-layer crosstalk at high gap thickness. Crosstalk abruptly drops when the gap thickness is above 5μm when the two function layers are perfectly isolated from each other. The 5μm gap requires 3-4 transition layers between the function layers, which brings a large footprint and an extra coupling loss.

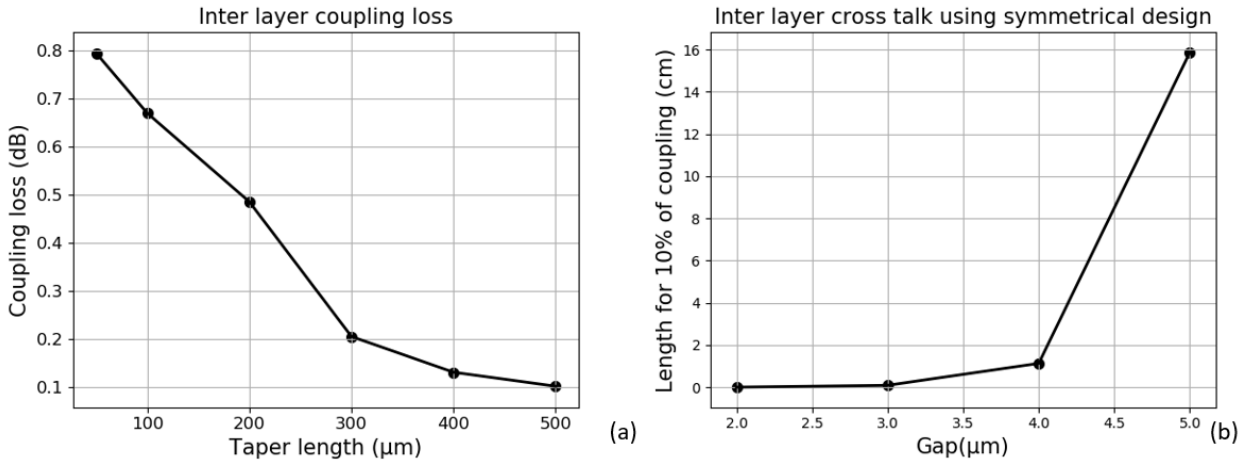


Figure 9 (a) Simulated inter-layer coupling loss with varying taper length. The input waveguide has a 100nm thickness and 3μm width. The output waveguide has 200nm thickness and 2μm width. The inter-layer coupler has a 1.4μm gap. (b) Simulated inter-layer crosstalk using the same waveguide as (a).

2.3.c Multi-layer silicon nitride platform fabrication

The fabrication of the multi-layer silicon nitride platform requires four fabrication steps: deposition, lithography, etching, and CMP. In this section, we present the techniques and tools for each step. The multi-layer silicon nitride platform can be fabricated on top of multiple substrates if a thick silicon dioxide bottom and top cladding presence with enough thickness to isolate the silicon nitride waveguides can be fabricated on top of the wafers, and the fabrication facility can support such fabrication. We use a 6-inch silicon wafer to fabricate our multi-layer silicon nitride platform, and we perform a 120^{o}C piranha bath as an initial cleaning step.

The multi-layer silicon nitride platform needs silicon nitride and silicon dioxide deposition. The silicon nitride can be deposited using LPCVD or PECVD. The deposition temperature of silicon nitride using LPCVD can be higher than 700^{o}C (we use 800^{o}C), so the thermal budget must be considered for fabrication involved with CMOS devices. Stoichiometric silicon nitride deposited by LPCVD possesses a large tensile stress of around 1000MPa, which usually causes cracking when the film thickness exceeds 400nm. An alternative to the LPCVD is PECVD silicon nitride, which can be deposited at less than 400^{o}C but with more impurities and defects, which introduces a higher waveguide propagation loss. The PECVD can deposit nonstoichiometric silicon nitride using an imperfect deposition process, which causes a deviation between the simulated and experimental device performance. We used LPCVD to deposit silicon nitride for higher device performance.

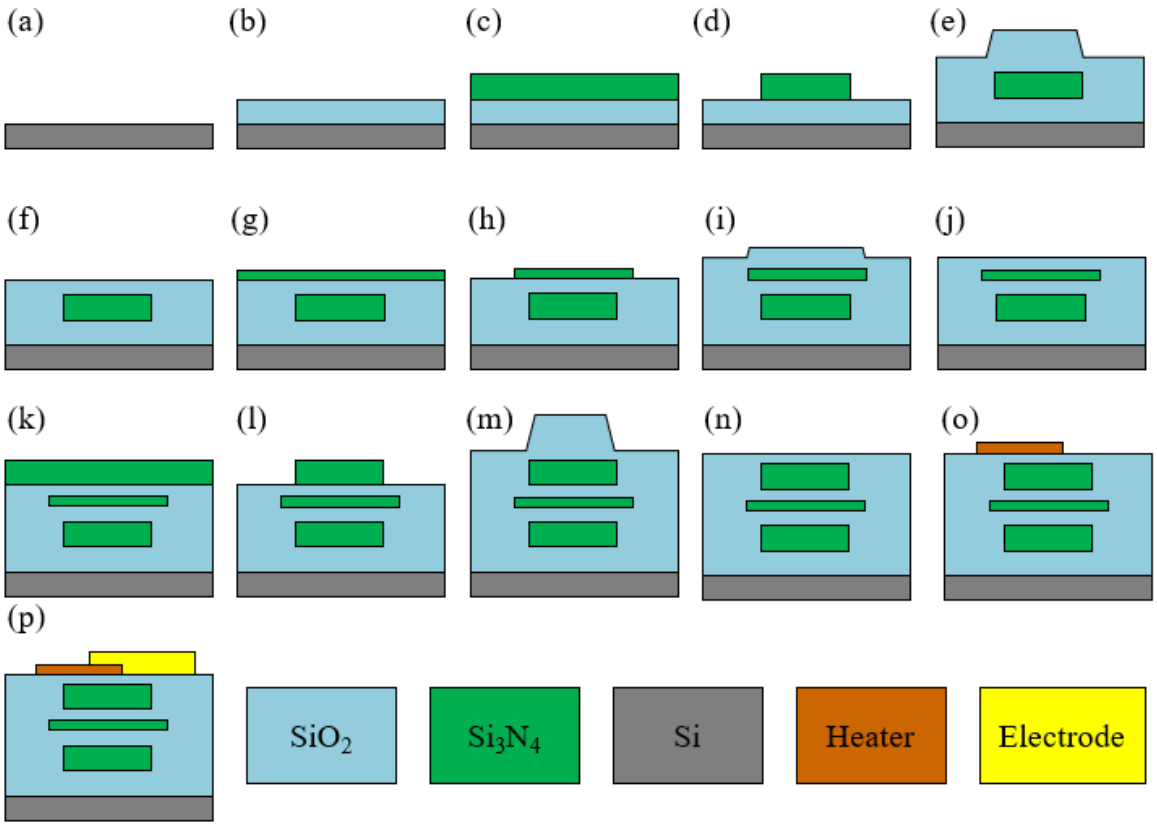


Figure 10 Fabrication process flow of the multi-layer silicon nitride platform. (a) Initial wafer cleaning for 6-inch wafers. (b) Thermal oxidation. (c) The bottom layer is 200 nm Si3N4 deposition. (d) 500 nm Si3N4 patterning by lithography and etching. (e) First inter-layer SiO2 deposition. (f) CMP. (g) The transition layer 100 nm Si3N4 deposition (h) 100 nm Si3N4 patterning by lithography and etching. (i) Second inter-layer SiO2 deposition. (j) CMP. (k) The top layer 200nm Si3N4 deposition. (l) 200 nm Si3N4 patterning by lithography and etching. (m) Top cladding SiO2 deposition. (n) CMP. (o) 20nm Ti / 100 nm Au metal heaters fabrication using metal lift-off. (p) 20 nm Ti / 800 nm Au metal electrodes fabrication using metal lift-off.

Figure 11 Surface roughness measured by atomic force microscope (AFM) (a) thermal oxide. (b) LTO after deposition, (c) LTO after deposition, and (c) LTO after CMP.

The silicon dioxide can be deposited by LPCVD and PECVD. The silicon dioxide LPCVD can deposit low-temperature oxide (LTO) and high-temperature oxide (HTO) using different deposition conditions. The LTO uses silane and oxygen to deposit silicon dioxide under 400~450^{o}C, while the HTO uses dichlorosilane and nitrous oxide to deposit silicon dioxide under 800~900^{o}C. The HTO is denser and has a lower wet etching rate under HF etching compared to

LTO. The PECVD silicon dioxide deposition can be used under 400^{o}C temperature while inducing more impurities and defects. Except for deposition, silicon dioxide can also be produced by oxidizing silicon substrate using dry oxidation (using oxygen) or wet oxidation (using vapor water). The silicon dioxide produced by oxidation typically has a better quality than the deposited silicon dioxide. After material deposition, N_2 annealing improves the quality of the silicon dioxide and silicon nitride quality by making the materials denser and removing N-H and O-H bonds. The surface roughness of the silicon dioxide also influences the waveguide performance. Our fabrication results show that the surface roughness after wet oxidation on a new Si wafer with less than 6μm thickness is smooth enough to exceed our AFM measurement capability. In contrast, HTO and LTO can induce a higher roughness (typically a few nanometers) while HTO is smoother than LTO when using the same thickness. More measurement result is shown in later chapters.

The deposited silicon nitride is patterned according to a mask layout using lithography and etching. Lithography includes photoresist coating, exposure, and development. We mainly use ASML DUV stepper model 5500/300c for exposure, which uses 248nm wavelength laser to resolve a minimum of around 250nm feature size using proper photoresist. The stepper achieves a 60nm misalignment between many exposures using sets of alignment marks that are fabricated on the wafers. We use all automatic machines for photoresist spin coating and development. We perform the silicon nitride etching in an inductively coupled plasma (ICP) etching system with a combination of C_4F_8 and H_2 gas, followed by a photoresist removal using an O_2 plasma etching under 250^{o}C. We then cleaned the wafer using a 120^{o}C piranha bath.

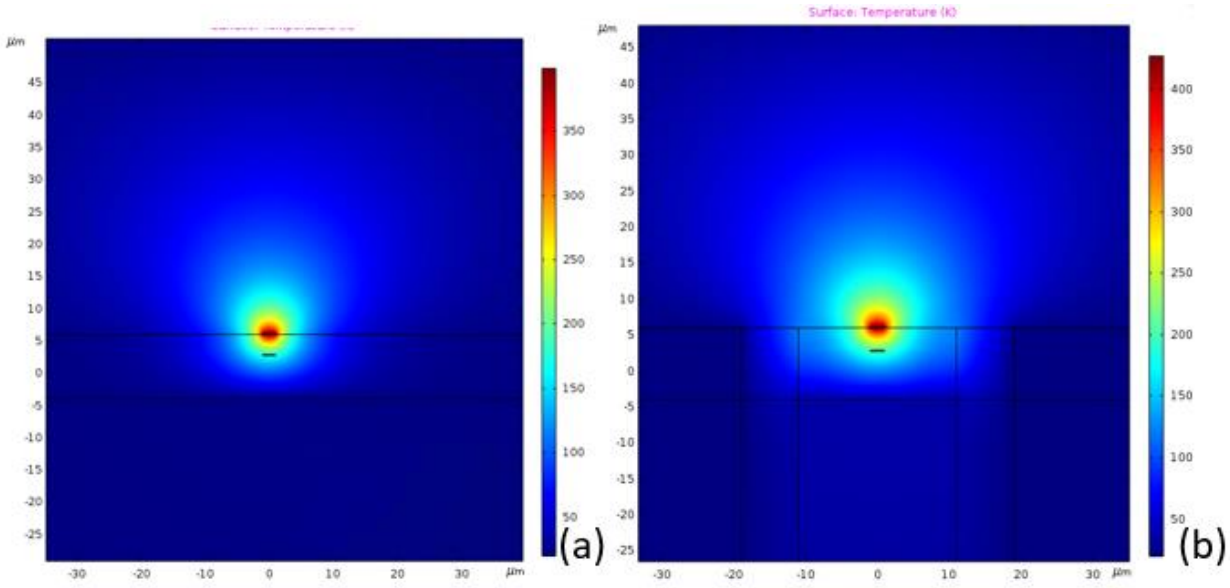


Figure 12 Thermal simulations of the single-layer silicon nitride waveguide using the same input thermal power. The room temperature is 20°C. (a) No thermal trench. The center of the silicon nitride has 176°C temperature. The temperature at 30μm away from the waveguide is 23°C. (b) Two thermal trenches at the left and right of the waveguide by 8μm. The center of the silicon nitride has 200°C temperature. The temperature at 30μm away from the waveguide is 20.4°C.

Here, we present a tri-layer silicon nitride platform fabrication process, as shown in Figure 10. The multi-layer silicon nitride platform is fabricated by stacking multiple silicon nitride layers on one wafer to increase the device's density. The bottom cladding is fabricated using a wet oxidation since the thermal oxide has a high quality and a lower surface roughness compared to the LTO deposited at 450°C, as indicated in Figure 11 (a) and (b). A 200nm silicon nitride is then deposited on top of the bottom cladding using LPCVD at 800°C and then patterned according to the layout we designed by lithography and etching. An LTO layer is deposited on top of the silicon nitride devices as a top cladding. The top surface after the LTO deposition will be conformal with the silicon nitride waveguides and have a high surface roughness, so we planarized the top surface using chemical-mechanical polishing (CMP). Figure 11 (d) shows the surface roughness of the silicon dioxide after the CMP, with all structures removed. It needs to be noticed that an LTO surface after CMP still has a higher surface roughness compared to the

roughness of a silicon dioxide surface fabricated by a wet oxidation process on a silicon wafer, so the top layer devices have a higher propagation loss compared to the first layer. After CMP, the top surface is ready for the fabrication of the next layer, and the second layer will be fabricated using the same process as the first layer fabrication (Figure 10 (c) to (f)). The multi-layer structure is fabricated by repeating the single-layer fabrication process with a different layout and silicon nitride thickness.

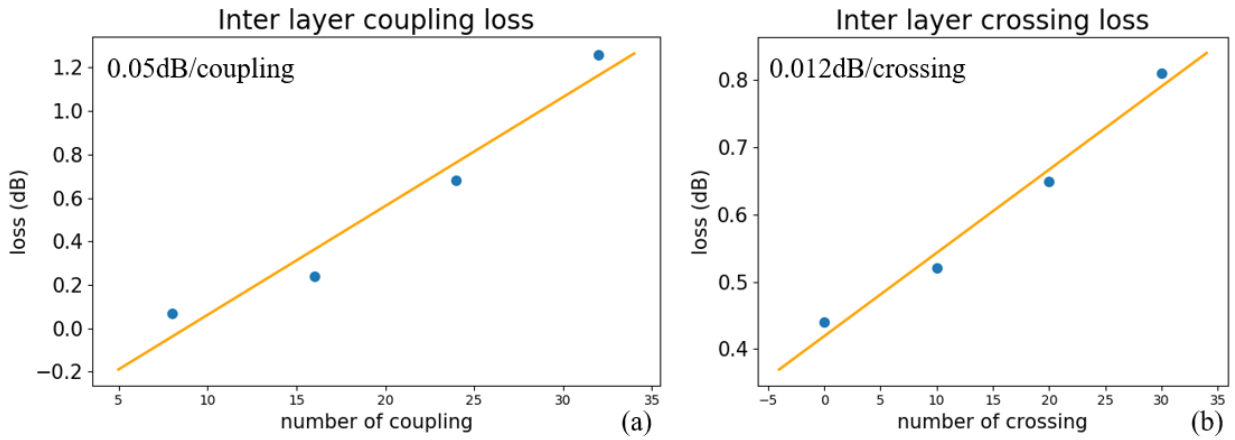


Figure 13 (a) Measured inter-layer coupling loss. (b) Measured inter-layer crossing loss.

Metal layers can be fabricated on top of the silicon nitride platform for thermal tuning. Here, we take a two-layer metal fabrication as an example. After the top cladding planarization, we deposit and pattern the 20 nm Ti and 100 nm Au using electron-beam evaporation and lift-off, followed by 20 nm Ti and 800nm Au. The Ti is to enhance the adhesion between silicon dioxide and gold. Figure **12** shows the simulated thermal tuner on a single-layer silicon nitride waveguide with bottom and top cladding, assuming a constant of thermal power is fed into the metal heater above the top surface. Since the thermal conductivity of single-crystalized silicon is about two orders of magnitude higher than that of silicon dioxide, the bottom silicon dioxide thickness has a major impact on the efficiency and thermal crosstalk. Etching trenches into silicon substrate around the waveguide with thermal tuning is an effective way to further improve the performance of the

heater, as indicated in Figure **12**. Trenches are etched into the Si by 100μm around the heaters for thermal isolation. Since thermal resistance of the SiO_2 is larger than that of the Si, a thick bottom cladding also helps on improving the heaters' performance.

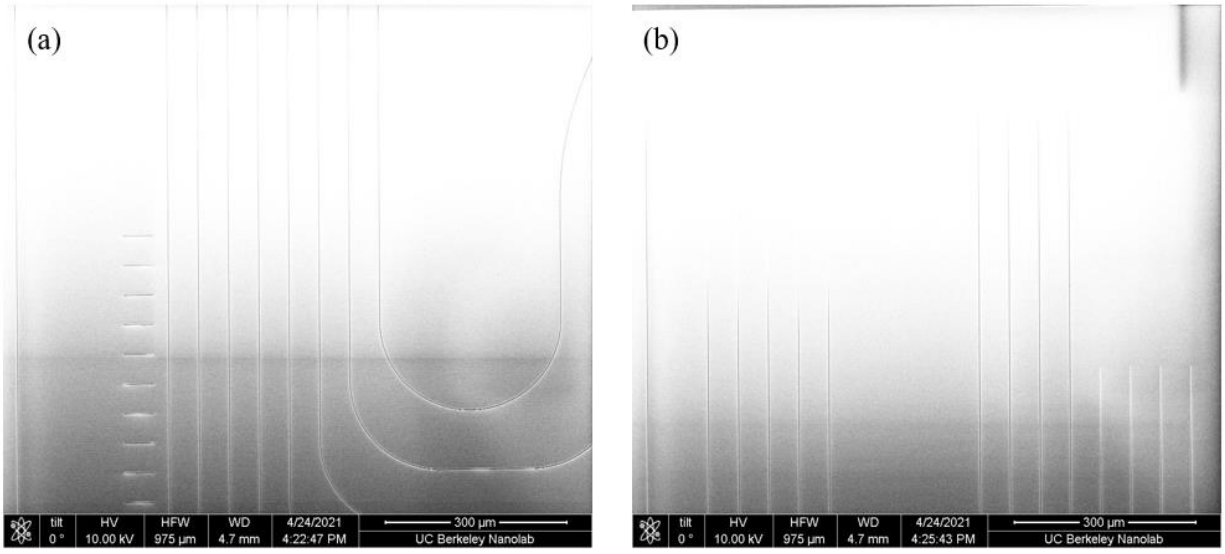


Figure 14 SEM photo of the silicon nitride waveguides on one layer.

We demonstrate our silicon nitride platform by measuring the inter-layer coupling loss and the inter-layer crossing loss on a fabricated device. On these devices, arrays of waveguides with different numbers of inter-layer coupling and inter-layer crossing are designed so the loss can be calculated through linear regression. The 0.05dB inter-layer coupling loss and the 0.012dB inter-layer crossing loss in Figure **13** show that our design can work with highly efficient coupling and good isolation between two function layers. Figure **14** shows SEM photos of a fabricated silicon nitride layer. After a second layer fabrication, the waveguides at the first layer will be covered by cladding and cannot be observed by SEM.

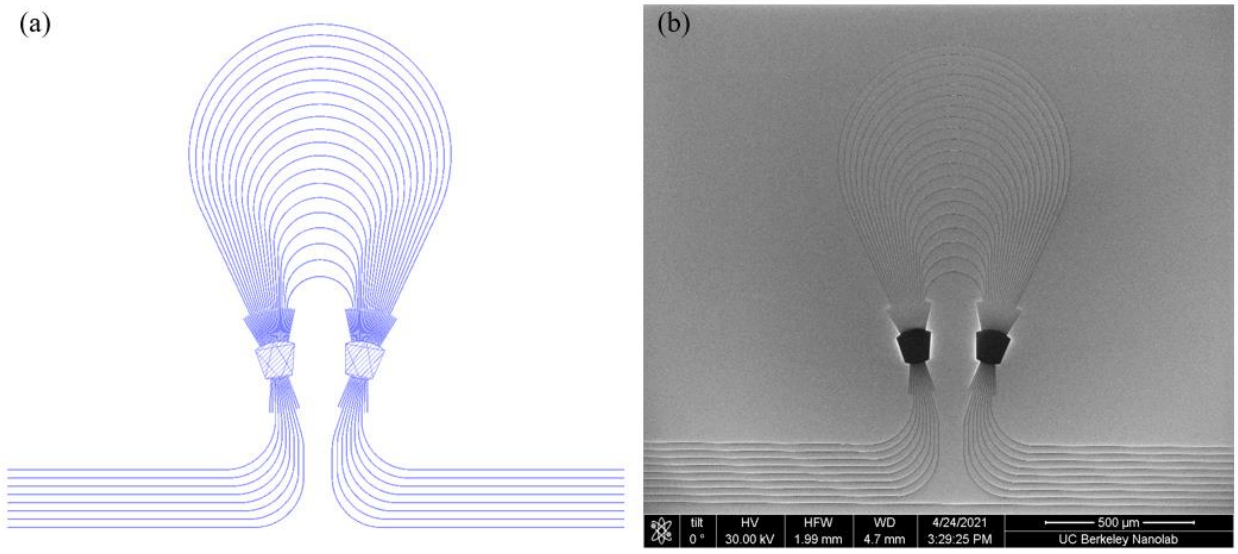
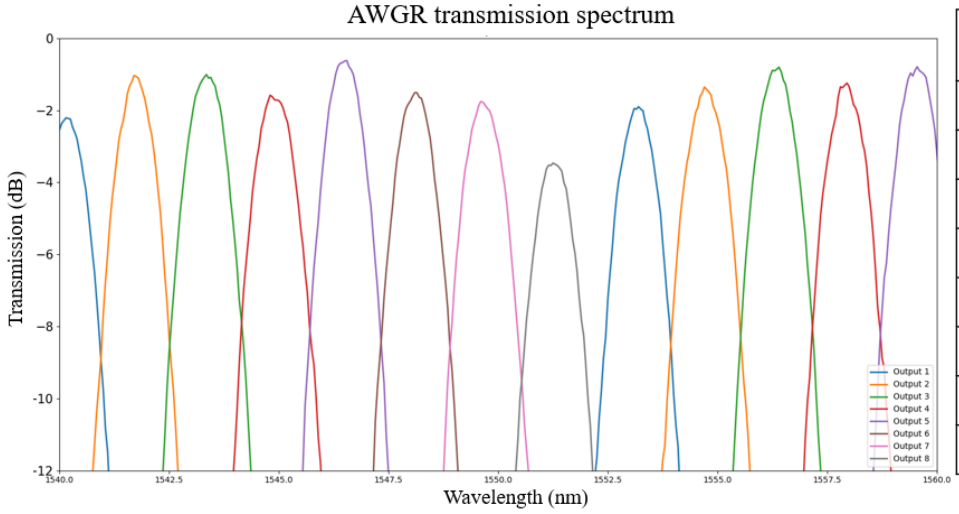


Figure 15 (a) Layout of the 8×8 200GHz channel spacing AWG and (b) SEM photo of the 8×8 200GHz channel spacing AWG after waveguide patterning.

We design and fabricate an 8×8 200GHz channel spacing arrayed waveguide grating routers (AWGRs) with the layout presented in Figure 15 (a) to demonstrate our silicon nitride devices fabrication. The AWGR is designed and measured by Jingwei Wan. The fabrication started with a commercial silicon wafer with 6μm thermal oxide on top. We deposited a 200nm silicon nitride using LPCVD. Our lithography and etching process patterned the AWGR layout accurately to the silicon nitride layer, with an SEM photo shown in Figure 15 (b). The AWGR has a minimum 250nm feature size to meet the limitation of our commercial ASML DUV stepper. Then, we deposited LTO as the top cladding material.

Figure **16** shows the measured transmission spectrum of the AWGR using our home made OVNA system, calibrated to a straight reference waveguide. The AWGR has a 199.11GHz average channel spacing and a 1.66dB average insertion loss with 0.82dB standard deviation on every port. The measurement results demonstrate our capability of fabricating large-size and complex structures on a silicon nitride layer.



Output #	Wavelength (nm)	Maximum (dB)
1	1540.15	-2.21
2	1541.7	-1.03
3	1543.38	-1.01
4	1544.8	-1.58
5	1546.55	-0.68
6	1548.1	-1.51
7	1549.6	-1.76
8	1551.25	-3.46

Figure 16 Measured 8×8 200GHz channel spacing AWGR transmission spectrum.

The multi-layer silicon nitride platform can be further improved by optimizing the waveguide fabrication process. The waveguide propagation loss can be reduced by optimizing the Si_3N_4 etching recipe, the photoresist reflow process and post etching cleaning process.

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Chapter 3 Low-loss and broadband optical interposer for large-scale integration

3.1 Diagram of the low-loss electrical and optical interposers

This chapter presents the demonstration of a low-loss, broadband optical interposer, a wafer-scale fabrication process and a broadband surface coupler based on a 45^{o} mirror.

Silicon photonics' advantages offer new possibilities for many applications, while other materials and platforms can compensate for its different disadvantages. For example, the indirect band of silicon makes it impossible to make high-efficiency laser and detector and raise the loss at high transmission power. A complex integrated optical system usually requires combining devices using multiple materials to optimize its performance.

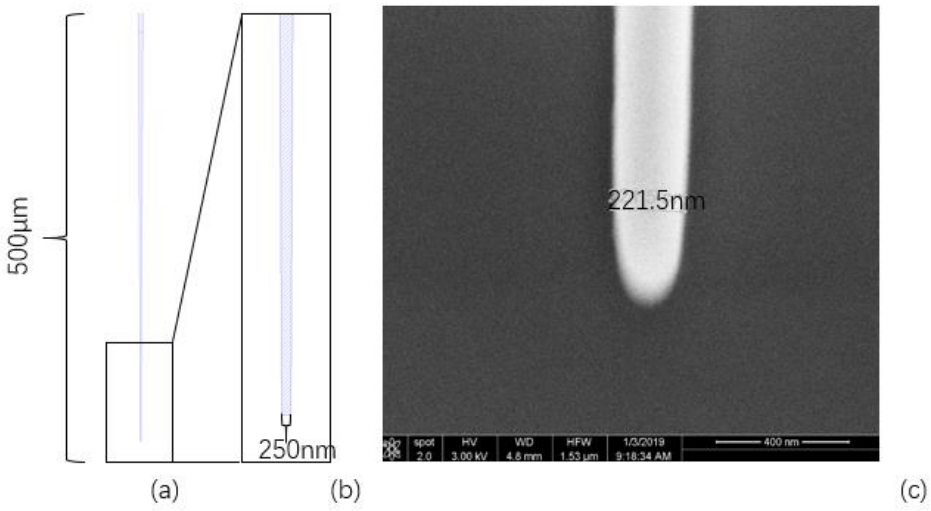

Figure 17 (a) A layout for an inverse taper coupler with 500µm taper length. (b) An SEM photo of the inverse taper coupler with 250nm taper end width and 100nm thickness.

A complex photonics integrated circuit may require devices from many materials. For example, a high-performance optical transceiver has CMOS control circuits, silicon multiplexer/demultiplexer and routing, III-V lasers, TFLN or III-V modulators, and Ge

photodetectors on a large scale. Although some of the devices can be integrated using epitaxial growth, multi-layer fabrication, wafer bonding, and other methods, integration of all components heterogeneously onto one wafer brings low yield and high cost due to fabrication difficulties. Interposers with many dies packaged together become a feasible solution for large-scale heterogeneous integration [95]-[97]. In our diagram, multiple building blocks are packaged onto an interposer (using flip-chip bonding) with optical and electrical connections so the fabrication of each component can be finished individually. Electrical connections can be achieved by simply attaching metal pads on the two chips together, while optical coupling requires high-efficiency chip-to-chip couplers.

Coupling efficiency is one of the most important parameters in interposer design [98],[99]. We use a silicon nitride platform to design and fabricate our interposer since it has a large mode size (shown in Figure 1), a low transmission loss (<0.1dB/cm) and compatibility with other platforms. Besides, the high-power capacity allows silicon nitride waveguides high power for many chips. Inverse taper couplers, as shown in Figure **5**, are used for chip-to-chip coupling. The inverse taper couplers' working principles are identical to the inter-layer coupler we described. However, misalignment during packaging becomes our major concern since most commercial flip chip bonders can only achieve less than 2.5μm alignment accuracy [100]. As discussed in Chapter 2, the inverse taper coupler can be optimized using a longer pair of tapers. We use 100nm thick silicon nitride and 500μm/1000μm taper length as a tradeoff between performance and footprint. The main design goal is to minimize the coupling loss under achievable misalignment. Table 1 shows the comparison between three different chip-to-chip couplers, including grating couplers, butt couplers, and inverse taper couplers. We chose the inverse taper couplers as our chip-to-chip coupler for their high bandwidth, polarization independence, and large misalignment tolerance.

Grating couplers have a limited bandwidth and usually work for a single polarization unless complex designs are applied [101]-[105]. So, grating couplers are usually not used in broadband detections and communications. The butt coupling is one of the simplest couplers for supporting a large bandwidth for TE and TM polarizations. Still, the coupling loss will abruptly increase with the increase of the misalignments [106].

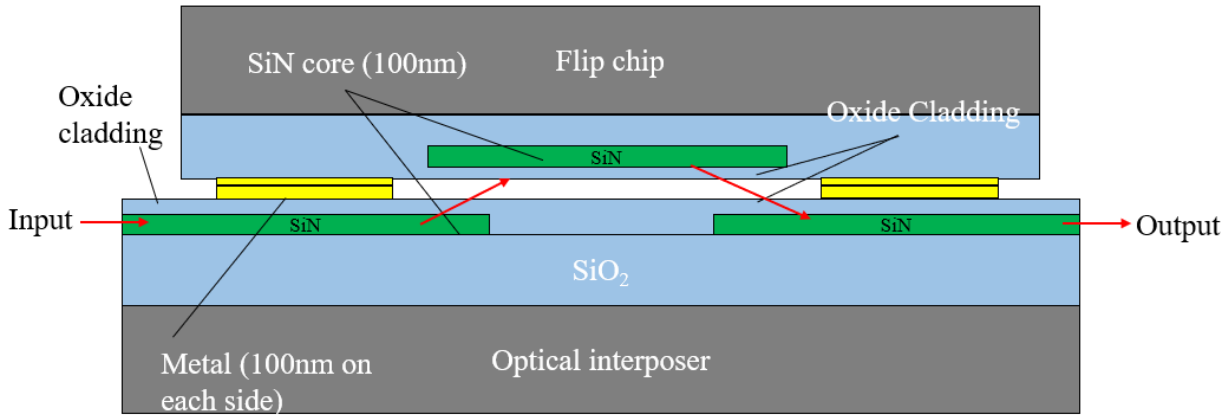

Figure 18 Diagram of the optical interposer. Red arrows indicate the light propagation directions.

Table 1 Comparison between different couplers for chip-to-chip coupling.

	Grating coupler	Butt coupler	Inverse taper coupler
Coupling loss	High (>3dB)	Low(<3dB)	Low(<1dB)
Misalignment tolerance	High(>2μm)	Low(~1μm)	High(>2μm)
Fabrication difficulty	Complex	Simple	Simple
3dB bandwidth	Low(<80nm)	High(>800nm)	High(>800nm)
Polarization dependence	High	Low	Low

Figure 18 shows the diagram of our optical interposer for a proof-of-concept demonstration. We perform an Au-to-Au thermal compressive flip-chip bonding for packaging the flip chip onto the interposer chip to enable the evanescent coupling between the two chips. We optimize our design at TE mode, around 1550nm wavelength. Figure 19 shows the simulated coupling loss at different oxide cladding thicknesses and air gap thicknesses. It must be noted that the air gap thickness is the sum of the metal thickness on the two chips, and the total gap thickness is the sum of the two oxide claddings' thickness and the air gap thickness. We can observe that all the

simulated coupling loss is below 0.5dB when there is no misalignment. However, the misalignment tolerance decreases with the increase of the gap thickness. The misalignment tolerance for less than 3dB coupling loss is less than 2.5μm in the simulated loss in Figure 19, which meet the capability of most commercial flip chip bonder. Besides, the coupling loss can be less than 0.5dB if less than 1.5μm misalignment is achieved, which means that under high bonding accuracy, many chips on the interposer can have almost the same input power. The bandwidth of the chip-to-chip coupler is shown in Figure 20. The misalignment can be further reduced by using a longer taper length, as indicated in Figure 21, while a longer taper length can increase the footprint and the transmission loss. In our proof-of-concept demonstration, we use 500μm/1000μm taper length as a tradeoff.

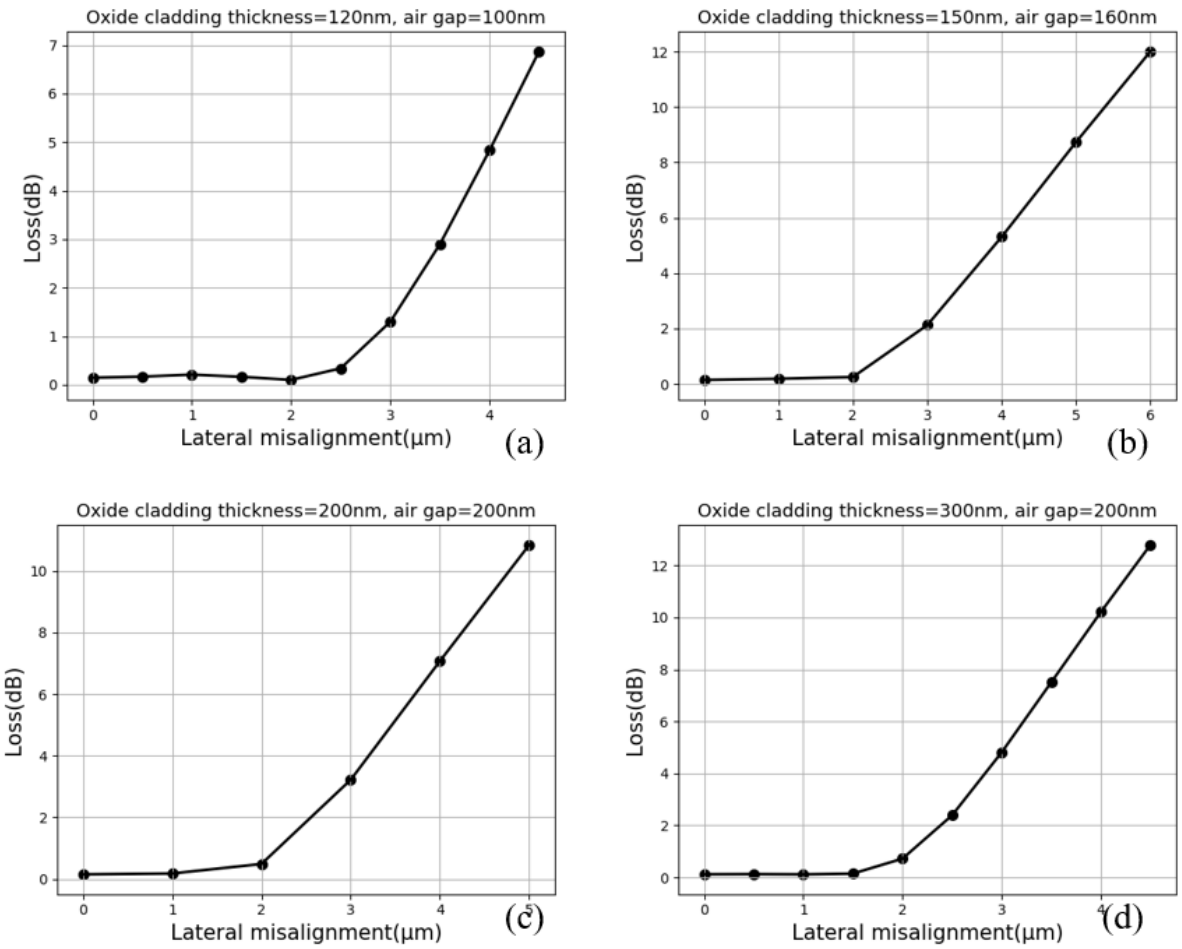

Figure 19 Coupling loss of the chip-to-chip coupler with 500μm taper length with a varying lateral misalignment at TE mode and 1550nm wavelength. (a) The oxide cladding is 120nm on each side, and the air gap is 100nm. (b) The oxide cladding is 150nm on each side, and the air gap is 160nm. (c) The oxide cladding is 200nm on each side, and the air gap is 200nm. (d) The oxide cladding is 300nm on each side, and the air gap is 200nm.

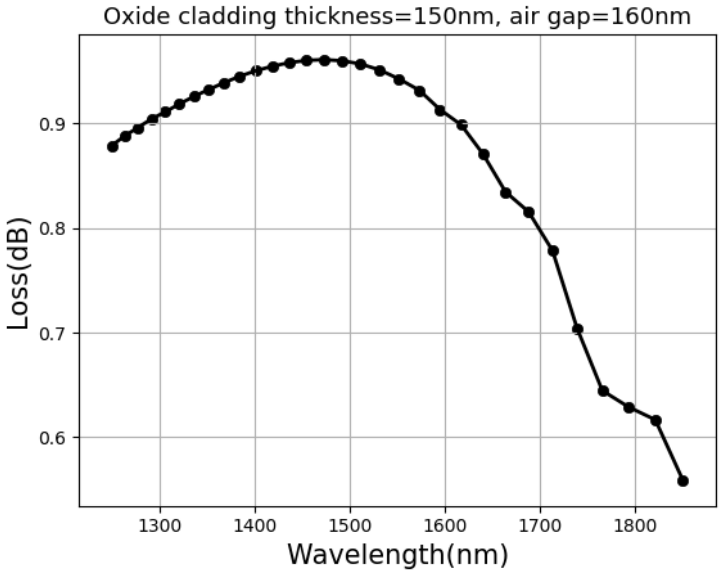

Figure 20 Bandwidth of the chip-to-chip coupler with 500μm taper length at TE mode.

The fabrication process of the interposer in Figure 22 is very similar to single-layer silicon nitride devices. After CMP, 200-300nm silicon dioxide was left on top of the silicon nitride waveguide. Ti/Au is evaporated on top of silicon dioxide and patterned by metal lift-off for electrical connection and thermal compression bonding.

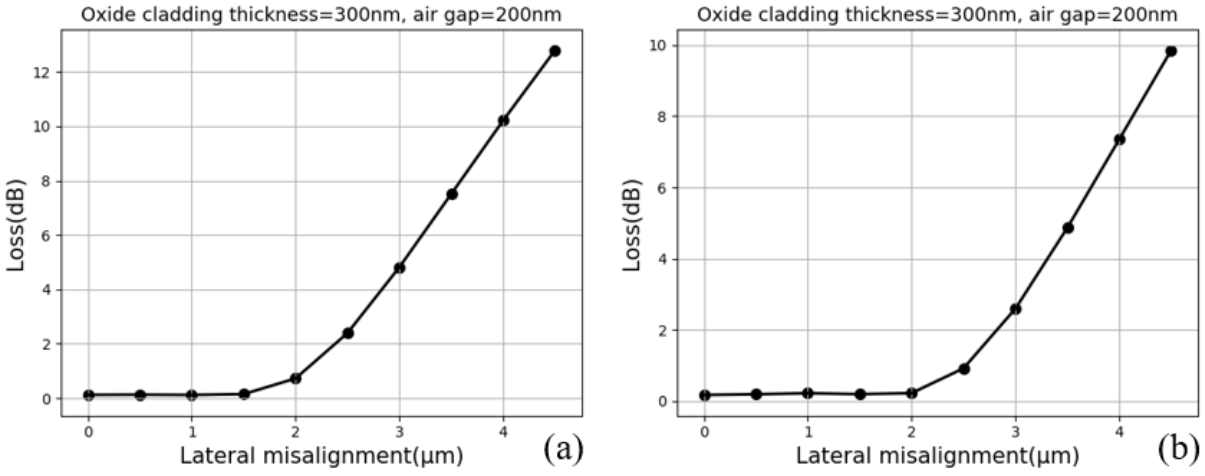

Figure 21 Coupling loss of the chip-to-chip coupler with a varying lateral misalignment at TE mode and 1550nm wavelength, with (a) 500μm taper length and (b)1000μm taper length.

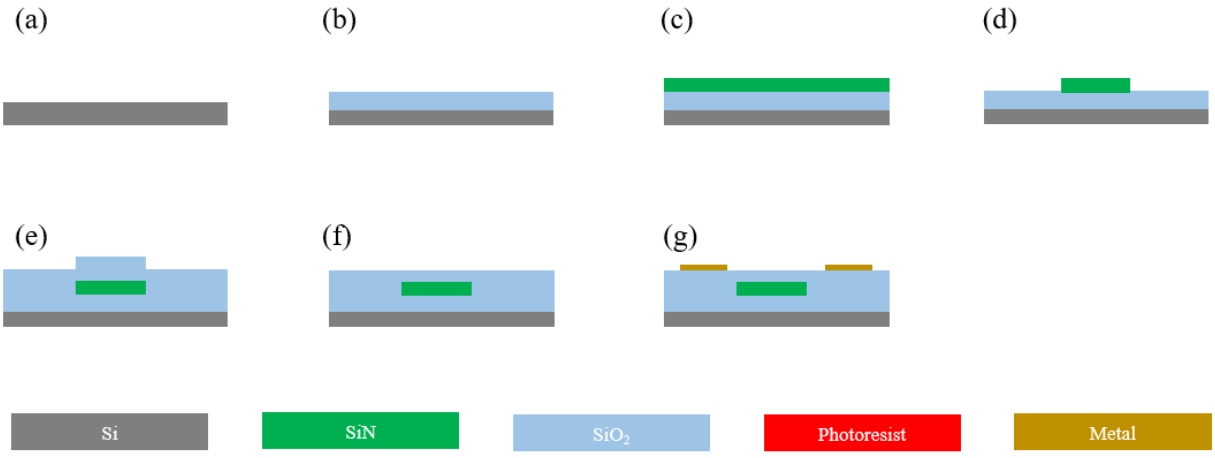

Figure 22 Fabrication process of the optical interposer. (a) Initial wafer cleaning. (b) LTO deposition or thermal oxidation. (c) Silicon nitride LPCVD. (d) Waveguide patterning using lithography and etching. (e) LTO deposition. (f) CMP. (g) Metal patterning using metal lift-off.

In our proof-of-concept demonstration, we used the layout in Figure 23. Waveguides on the two chips are arranged using different periods for introducing different lateral offsets. Metal pads on the chips are for alignment and bonding. The alignment marks are fabricated on the metal and silicon nitride layers, with the design shown in Figure 24. Alignment marks on the interposer and the flip chips are complementary, so during bonding, we can align the two chips by overlapping the center of the marks on the two chips together. Figure 25 (a) and (b) show the interposer chip and the flip-chip diagram at the front view and side view, respectively.

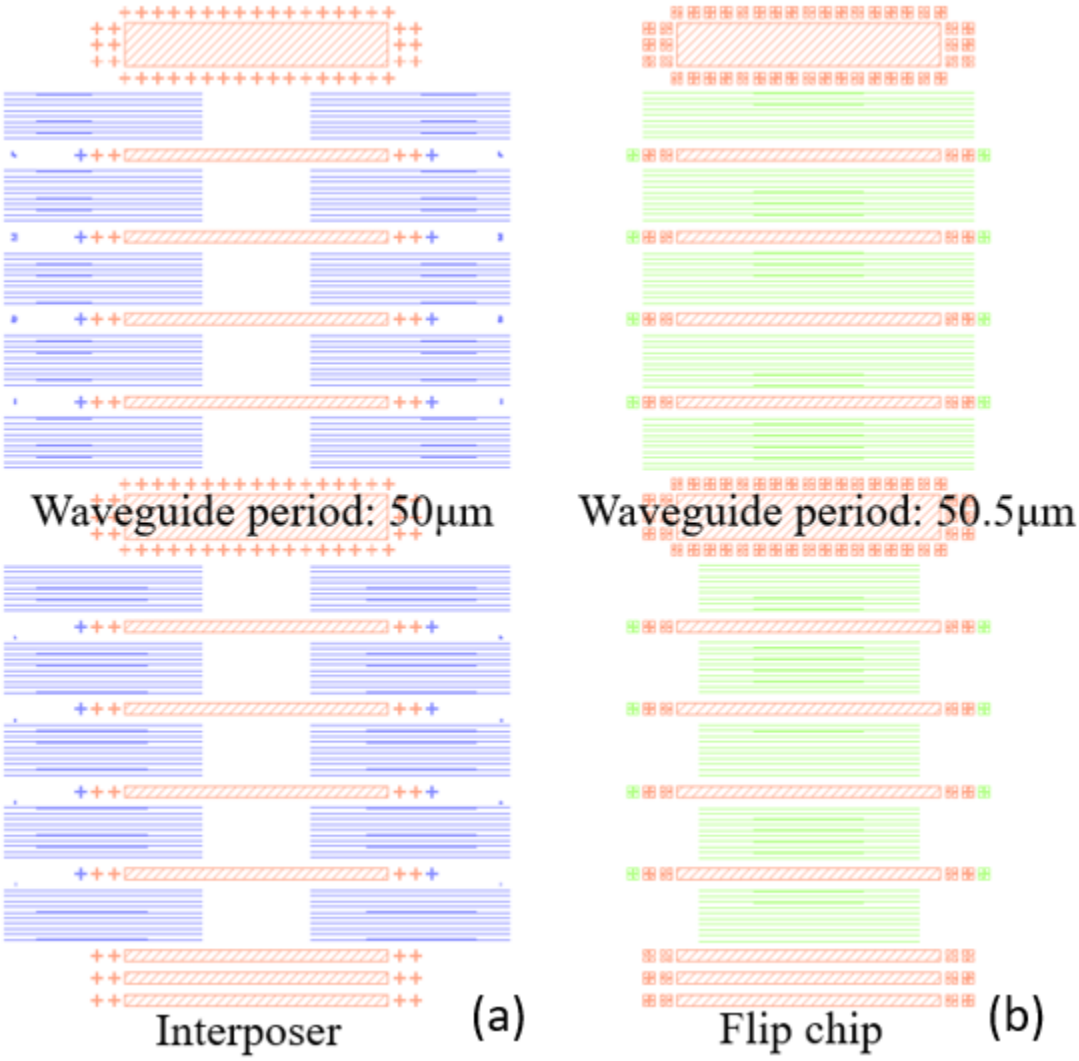

Figure 23 (a) Layout of the interposer. The blue structures are on the silicon nitride layer. (b) Layout of the flip-chip. The green structures are on the silicon nitride layer. Orange structures on both layouts show the metal layer.

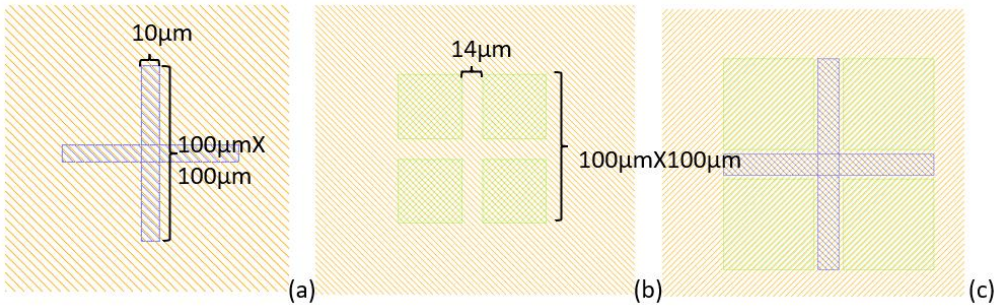

Figure 24 Alignment marks on the (a) interposer and (b) flip chips. (c) Overlay of the alignment marks on both chips.

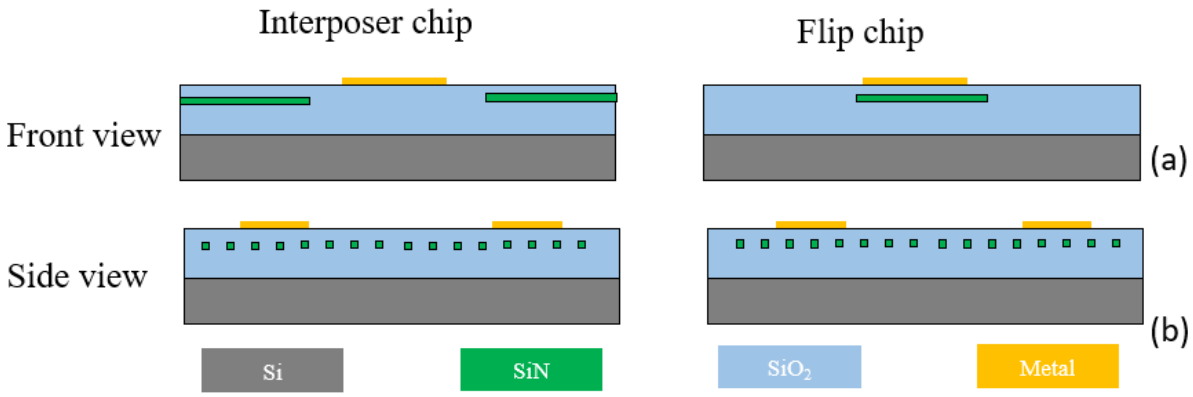

Figure 25 Diagram of the interposer chip and the flip chip. (a) Front view. (b) Side view.

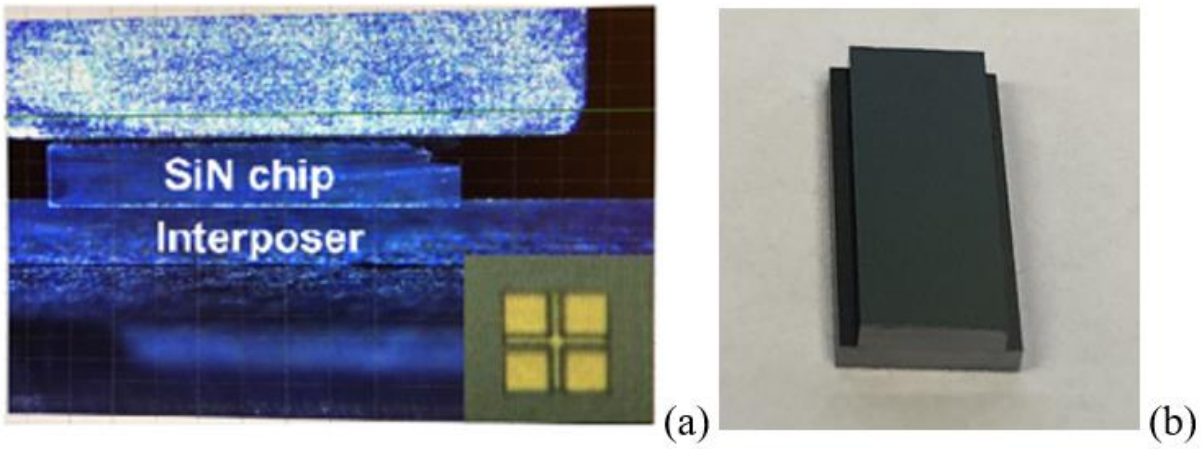

Figure 26 (a) Photo of flip chip bonding. The small figure at the bottom right illustrates the alignment of flip-chip bonding. (b) Photo of the bonded chips.

After the wafer-level fabrication, the whole wafers are diced into individual dies. In sequence, the dies are cleaned using ultrasonic cleaning under acetone, methanal, IPA, and DI water. We use FINETECH® lambda flip chip bonder to perform our flip chip bonding. The machine's light splitting and combining system allows us to observe the overlapping between the two chips before we put them together and achieve a less than 3μm misalignment. The metal arm on the flip chip bonder will place the flip chip onto the interposer chip according to the position guided

by alignment, as shown in Figure 26 (a). The bonded chip is shown in Figure 26 (b). Figure 27 shows the measured chip-to-chip coupling loss, with 500μm and1000μm taper lengths, respectively. The measured chip-to-chip coupling loss is calibrated to a reference straight waveguide on the interposer. Due to the reflections in the measurement system, especially between the fiber to the chip, we observed a around 1dB fluctuation on the measured spectrum. The error bar in Figure 27 denotes the fluctuation. The 3dB offset is ±2μm for 500μm taper and ±3μm for 1000μm taper. Besides, the coupling loss is near zero at its minimum, where the lateral offset compensates for the lateral misalignment during bonding. The measurement results show our chip-to-chip coupler can achieve low-loss coupling at achievable accuracy.

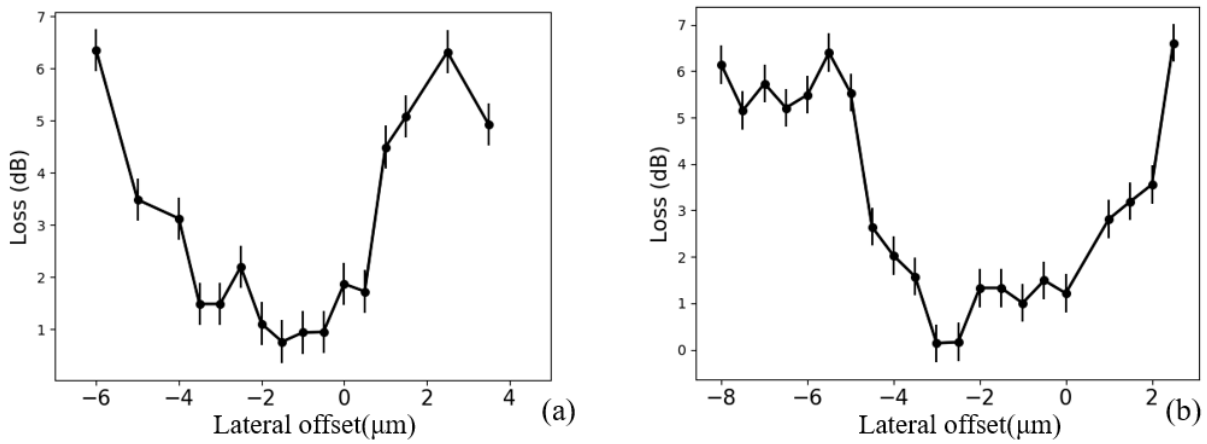

Figure 27 Measured chip-to-chip coupling loss (a) with 500μm taper length and (b) with 1000μm taper length.

3.2 Low-loss and broadband optical interposer for large-scale integration

In this section, we design, fabricate, and demonstrate a low loss, high misalignment tolerance, and broadband optical interposer for large-scale integration of many chips using thermal compression flip-chip bonding. The optical interposer uses inter-chip couplers with 0.54dB

coupling loss and ±3.53μm 3dB misalignment tolerance based on a wavelength-insensitive evanescent coupling to support applications in both O-band and C-band.

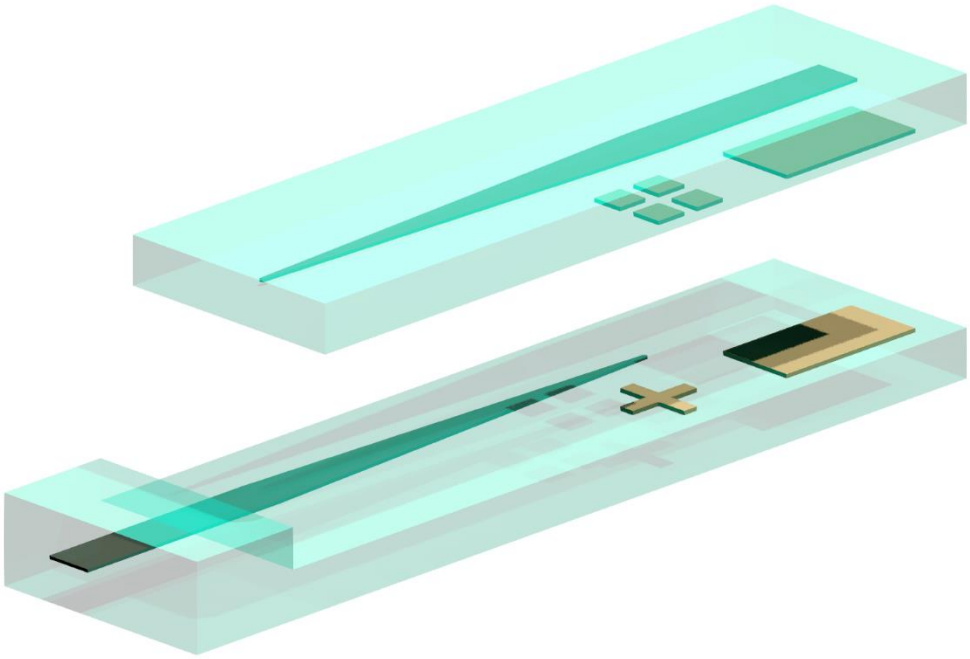

Figure 28 Schematic of the inter-chip coupler. Alignment marks and bonding pads are on the surface of the two chips. The Orange arrows denote the beam propagation direction. The black arrow denotes the chip movement direction during flip-chip bonding.

The inter-chip coupler requires broadband, low loss, and high packaging tolerance. A conventional flip-chip bonding process can achieve a ±0.5μm misalignment after placement, and it could greatly increase after the bonding. The optical coupling efficiency could be impaired under such misalignment, so our design goal is to minimize the inter-chip coupling loss under an achievable post-bonding misalignment.

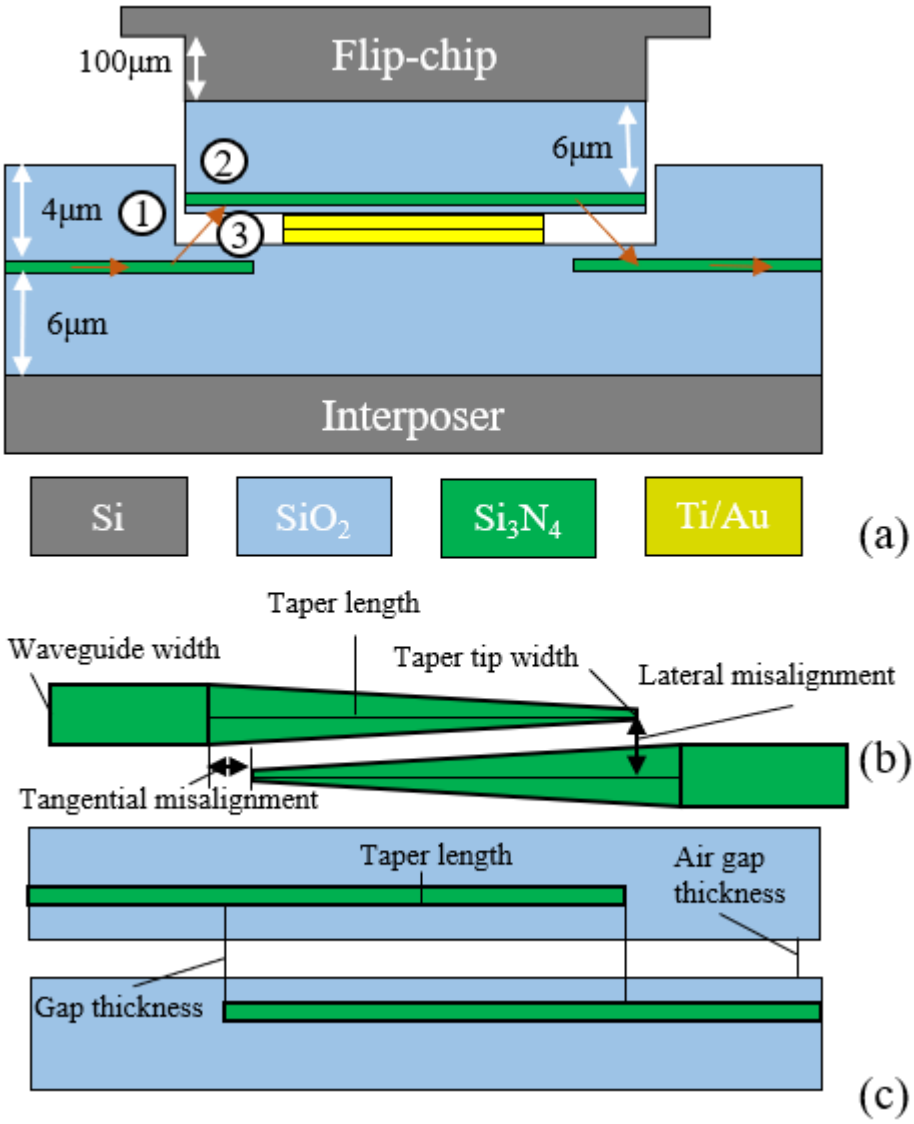

Figure 29 (a) Diagram of the flip-chip and Interposer packaging. The numbers denote:1. Air trench crossing loss, 2. flip-chip crossing loss, and 3. coupling loss. (b) Top view and (c) side view diagram of the inter-chip coupler.

We use the wavelength-insensitive evanescent coupling on the Si_3N_4 platform to efficiently couple light between chips. We utilize its low propagation loss, large transparency window, and large mode size, brought by the low refractive index contrast on Si3N4/SiO2 waveguides. We design a low-loss broadband inter-chip coupler using a pair of Si_3N_4 inversed tapers embedded in SiO2 cladding for optical transmission and metals for bonding, alignment, and electrical

connection on the two chips, as presented in Figure 28. During transmission, the optical beam transmitted in one Si_3N_4 waveguide is expanded by the inversed taper and coupled to the other taper evanescently. We performed Au-to-Au flip-chip thermal compression bonding to package the silicon photonics chips to the interposer guided by the alignment marks on the Au layer.

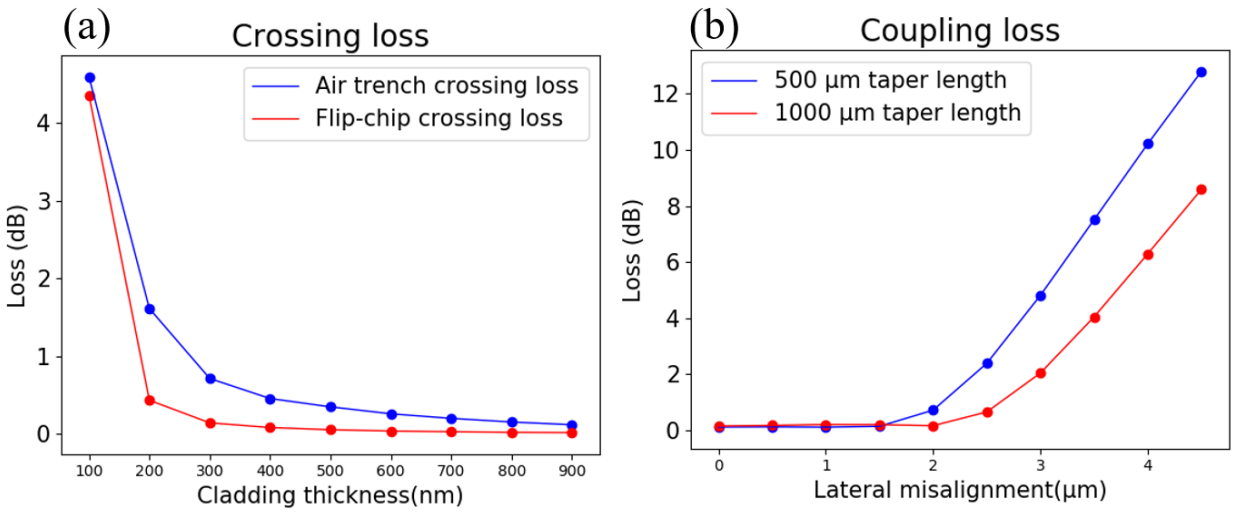

Figure 30 (a)Simulated crossing loss, (b) Simulated coupling loss.

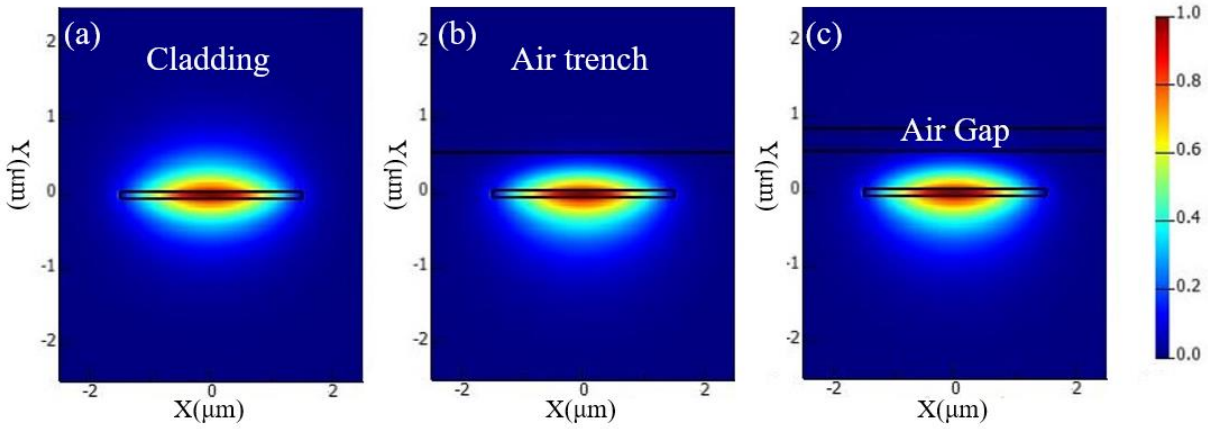

Figure 31 (a), (b), and (c) are simulated mode profiles with full cladding, with 500nm silicon dioxide cladding, and with a 200nm air gap, respectively.

We design a test structure with straight waveguides to measure the coupling loss of the inter-chip coupler, as shown in Figure 29 (a). The inter-chip coupler has a > 50μm longitudinal misalignment (presented in Figure 29 (b)) tolerance, so only lateral misalignment is considered

in this work. The test structure includes an array of the inter-chip coupler with a variable offset to measure the coupling loss and the misalignment tolerance. The top cladding thickness was reduced to around 500nm at the coupling region to enhance the coupling efficiency. The flip-chip is plugged into the trench on the interposer during packaging. We design the 100nm silicon nitride thickness and a 1000μm taper length as a trade-off between the misalignment tolerance and device footprint. The total optical loss between the interposer and the flip-chip comes from 1. air trench crossing loss, 2. flip-chip crossing loss, and 3. coupling loss. Crossing loss induced by mode discontinuity (as shown in Figure 31 (a)-(c)) decreases with the increase of the interposer exposed cladding thickness and the air gap thickness shown in Figure 29 (c). The simulated crossing loss in Figure 30(a) indicates that the air trench loss dominates the total crossing loss. Figure 30 (b) indicates the misalignment tolerance increase with the increase of the taper length. Hence, we design the 100nm silicon nitride thickness and a 1000μm taper length as a trade-off between the misalignment tolerance and device footprint. We designed a 500nm interposer exposed cladding thickness and a less than 100nm flip-chip cladding thickness as a trade-off between the total inter-chip loss and lateral misalignment tolerance. The waveguide width is 3μm, and the tip width of all the inversed tapers is 250nm, limited by the minimum feature size of our ASML^{TM} PAS 5500 300 deep-UV lithography stepper. The air gap thickness is determined by the sum of the two metal thicknesses on the two chips, which is 200nm in this work. The two bonded metal pads enable an electrical connection between the bonded chips and the interposer.

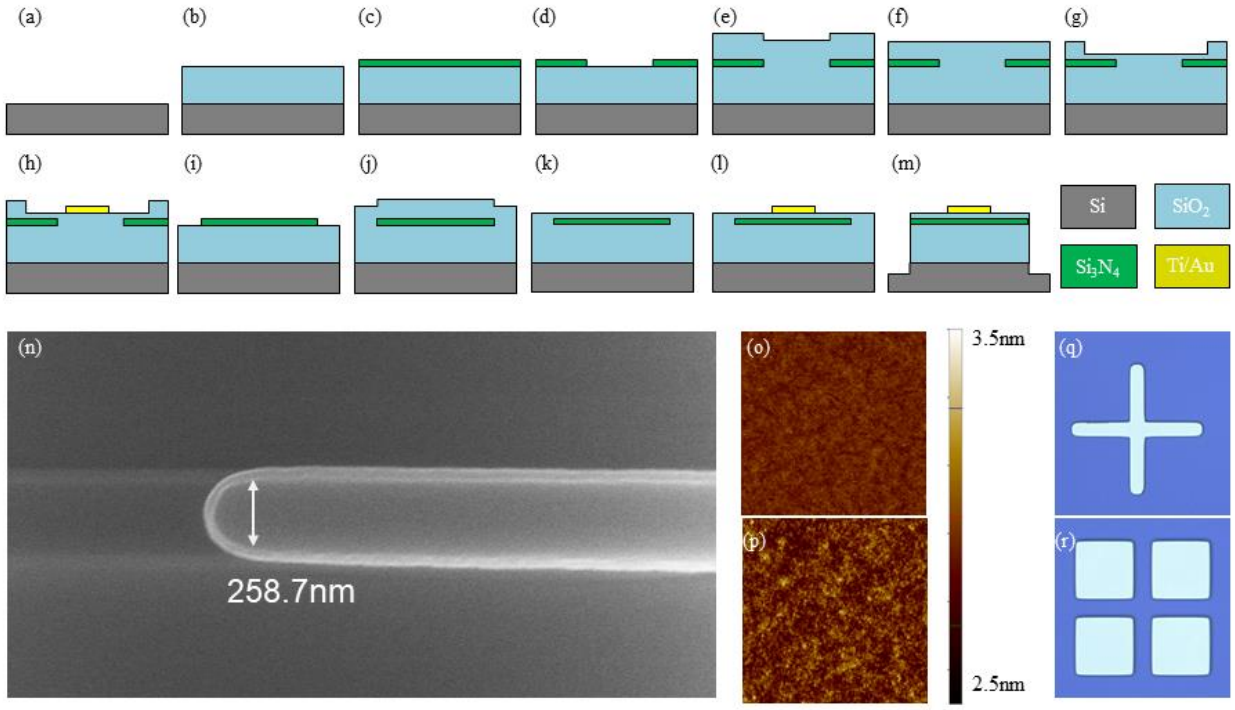

Figure 32 Fabrication flow chart of (a) initial wafer cleaning; (b) thermal oxidation; (c) Si_3N_4 deposition; (d) interposer Si3N4 lithography and etching; (e) interposer LTO deposition; (f) interposer CMP; (g) interposer LTO lithography and etching; (h) interposer Ti/Au lift-off; (i) flip-chip Si3N4 lithography and etching; (j) flip-chip LTO deposition; (k) flip-chip CMP; (l) flip-chip Ti/Au lift-off; (m) deep LTO/Silicon etching, (n) SEM photo of a patterned Si3N4 taper, at the tip, (o) AFM measurement of the SiO2 surface after CMP, (p) AFM measurement of the SiO2 surface inside the LTO trench after step (g), (q) and (r) microscope photo of the alignment marks on the interposer and the flip-chip, respectively.

Figure 32(a)-(m) shows the fabrication flow chart of our interposer and the flip-chip. The interposer and the fabrication start with an initial wafer cleaning on a 150mm silicon wafer using a 120^{o}C piranha solution. We perform wet oxidation under 1050^{o}C to get 6μm SiO_2 bottom cladding. We then deposited stoichiometry Si_3N_4 using low-pressure chemical vapor deposition (LPCVD). The interposer and flip-chip waveguide design are patterned onto the Si_3N_4 layer using lithography and etching, as presented in Figure 32 (n). We deposited a 4μm low-temperature oxide (LTO) on the interposer wafer using LPCVD as the top cladding, followed by a chemical mechanical polishing (CMP). The polished surface has an average 0.2nm surface

roughness, measured by atomic force microscopy (AFM), as shown in Figure 32 (o). We etch the trench on the interposer using inductively coupled plasma (ICP) etching with low surface damage since the roughness on the trench surface will induce scattering loss because of local discontinuity. The etched surface roughness is 0.5nm, as shown in Figure 32 (p). On the flip-chip, we deposit a 350nm LTO on top of the patterned Si_3N_4 layer, and we remove ~250nm LTO by CMP to ensure the flip-chip cladding thickness is around 100nm. Using lift-off, we patterned 20nm Ti and 80nm Au on top of the interposer and the flip-chip wafers. Figure 32 (q) and (r) present the alignment mark microscope photos on the interposer and the flip-chip, respectively. We perform a SiO_2/Si deep etching process to make the flip-chip accommodated by the trench on the interposer during packaging and expose the edge of the waveguides on the interposer chip.

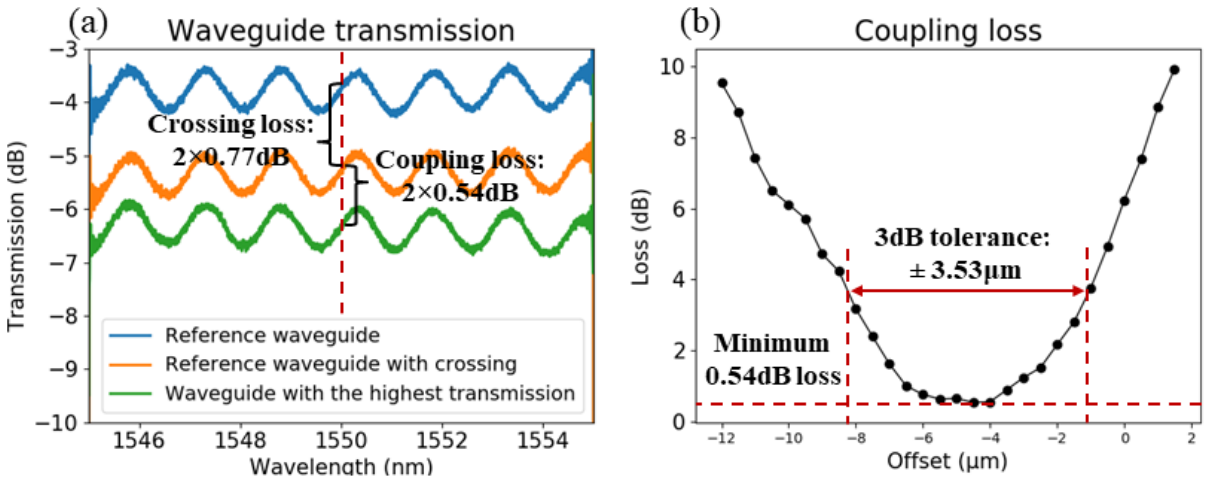

Figure 33 (a)Measured transmission of the reference waveguides and the inter-chip coupler with the highest transmission around 1550nm wavelength and (b) measured inter-chip coupling loss as a function of the offset at 1550nm wavelength.

The diced chips are then cleaned, and flip-chip bonded together using a thermal compression bonding with a 400°C temperature, 3N force for 10min. After bonding, we anneal the bonded chips under 350°C for an hour.

We measure the crossing loss and the coupling loss on the fabricated devices using single-mode lensed fibers as input and output at TE mode, around 1550nm wavelength. The measured result shows a 0.77dB total crossing loss, as indicated in Figure 33 (a), by averaging the two crossings on a reference waveguide (shown in Figure **33** (a)). The 0.54dB minimum inter-chip coupling loss in Figure 33 (a) occurs when the offset on an inter-chip coupler compensates for the flip-chip bonding misalignment. The inter-chip coupling loss at variable offsets in Figure 33 (b) shows a ±3.53μm 3dB tolerance. The post-flip-chip bonding misalignment is estimated to be 5μm.

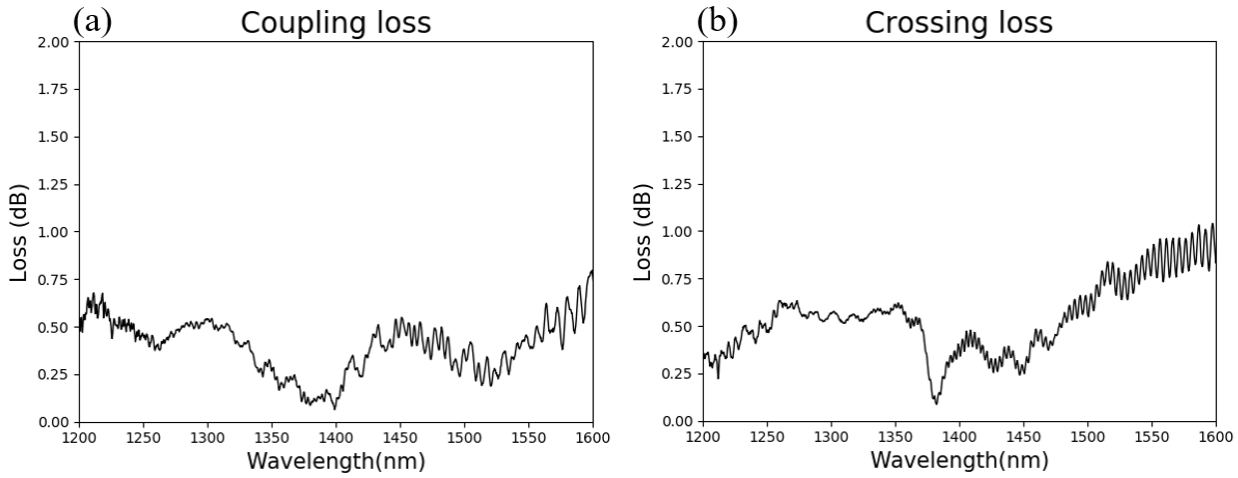

Figure 34 (a)Measured broadband coupling loss and (b) measured broadband crossing loss.

Figure 34 shows the crossing and coupling loss from 1200nm to 1600nm wavelength. We use a broadband light source, a polarization beam splitter (PBS), and a lensed polarization maintaining (PM) fiber with a calibrated rotation angle to couple light into the devices at fundamental TE mode. The output light from the devices is then coupled into a lensed PM fiber and measured by an optical spectrum analyzer (OSA). The coupling loss is measured at the -5μm offset, which shows the inter-chip coupling loss is wavelength insensitive in the designed bandwidth when the misalignment is near zero. The mode size at the C-band is larger than that of the O-band with the

same waveguide configuration, which induces a higher crossing loss. The measured crossing loss and coupling loss show our optical interposer can support applications in both C-band and O-band.

3.3 Large-scale integration using optical and electrical interposer

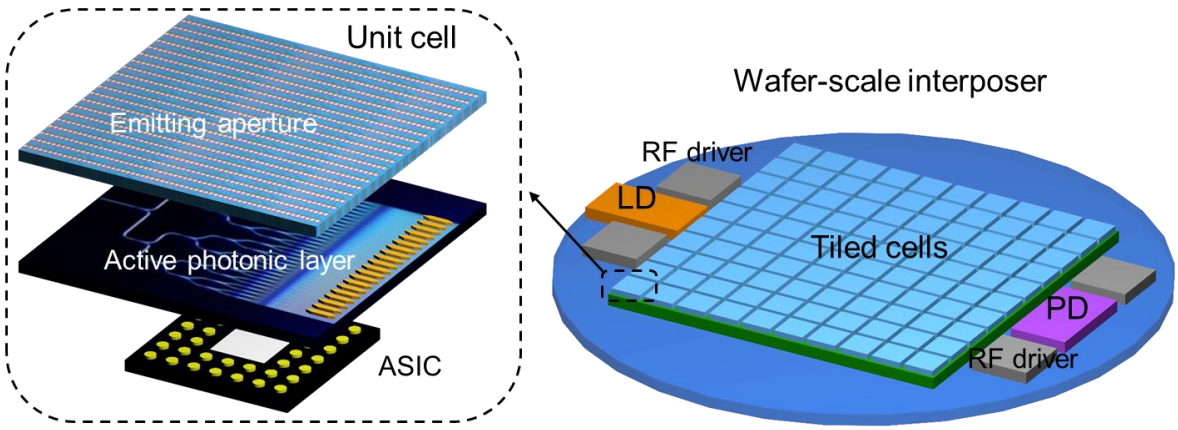

Figure 35 Schematic of a wafer-scale LIDAR system consisting of unit cell-based 3D silicon photonic chips tiling on an interposer.

A complex integrated electrical and optical system may require the integration of multiple dies on multiple platforms in a wafer-scale interposer (WSI) [107]. Figure 35 shows a schematic of a wafer-scale LIDAR system consisting of 10×10-unit cells packaged onto a wafer-scale interposer with electrical and optical connections. Each unit cell is fabricated individually and consists of an optical phased array (OPA) controlled by the electronic application-specific integrated circuit (ASIC) attached at the bottom. In this section, we demonstrate our capability of wafer-scale fabrication. Besides, we design and fabricate a wafer-scale grating array by replacing the inversed taper with the grating so we can observe the light emission from the top as a proof-of-concept demonstration.

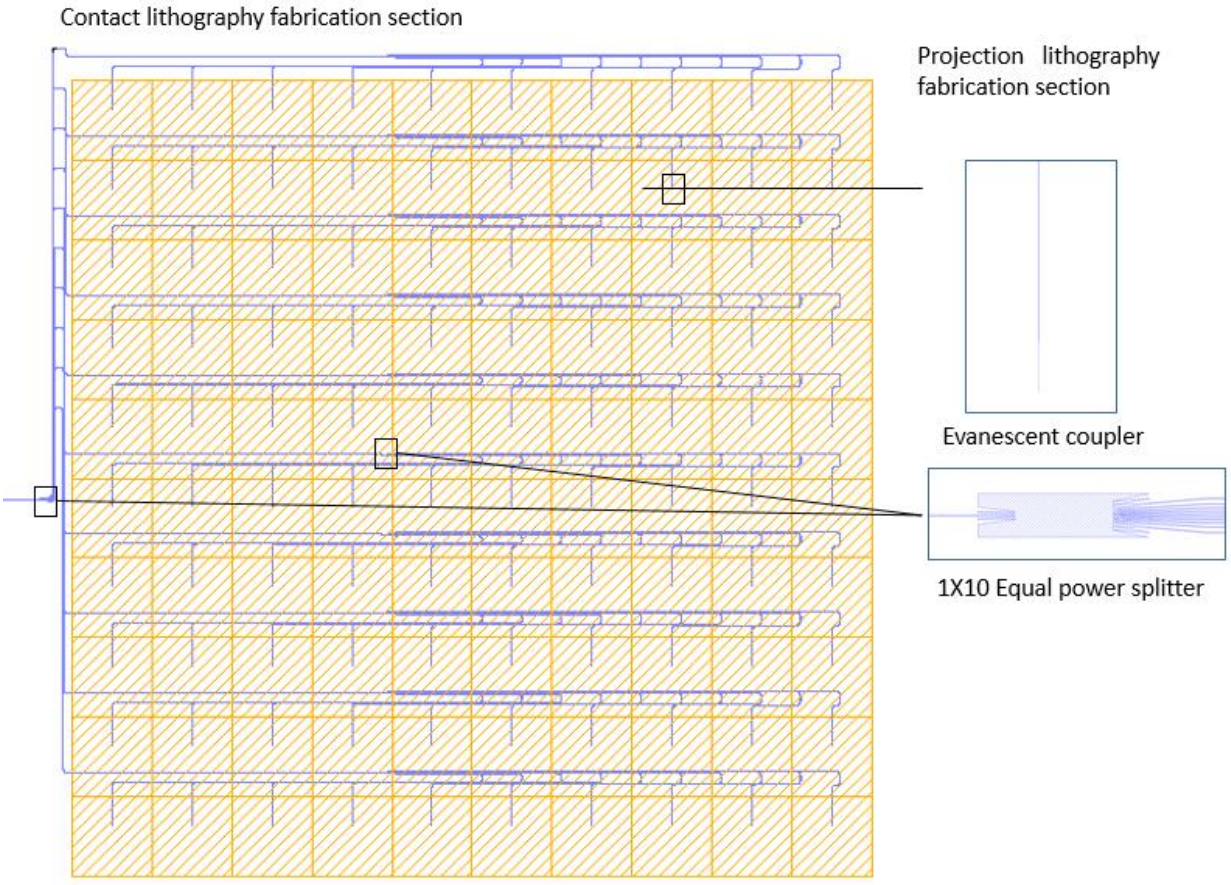

Figure 36 The layout of a wafer-scale interposer. The size of the tiles is 10 cm x 10 cm. The Waveguide section is patterned by contact lithography. An equal power splitter and

inverse taper coupler are stitched onto the wafer by projection lithography with high resolution (<250nm).

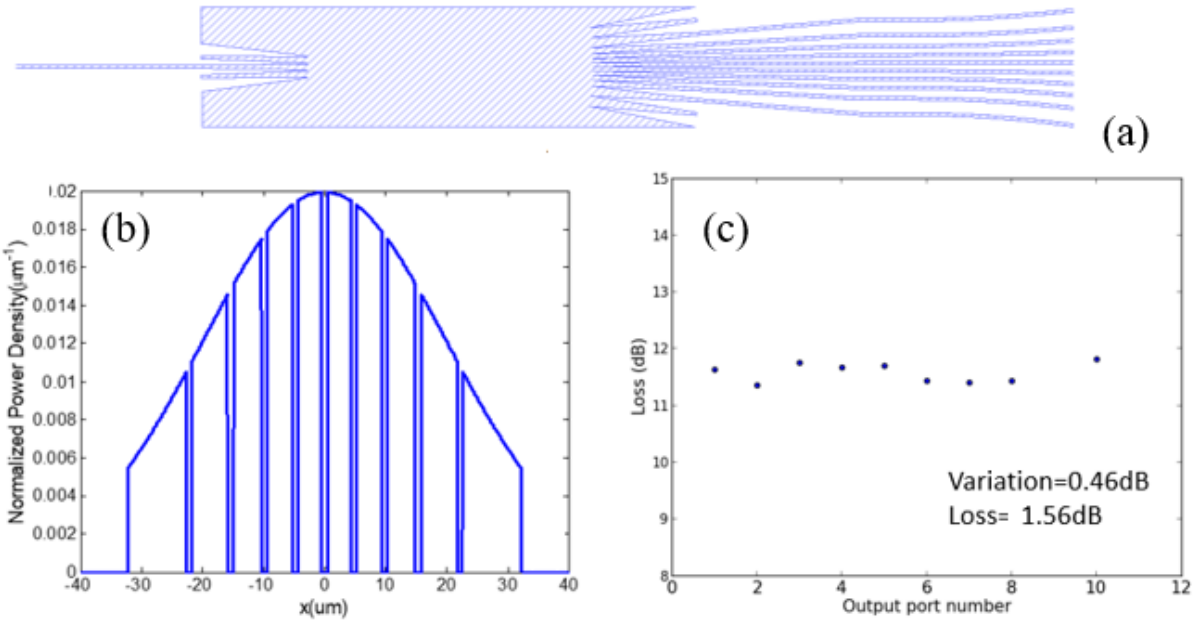

Figure 37 (a) Layout of the equal power splitter. (b)The simulated output width and power. (c) The measured output power.

The WSI needs to deliver the power to each silicon photonic unit cell-based tile with uniform power and phase to ensure the large coherent aperture operation and mitigate the system sensitivity to pathlength-dependent loss and phase errors. Figure 36 shows the layout of the WSI with equal power splitting and a length-matched design of 10 ×10 tiles. Power from the external laser will be evenly distributed to each tile through a cascaded 1×10 equal power splitter (shown in Figure 36) and then evanescent coupled to the silicon photonic unit cell above. The total waveguide length to each tile from the laser input is fixed at 15 cm, which gives less than 1.5 dB loss with the SiN core thickness of 100 nm. Figure 37 shows the layout of the equal power splitter (EPS) to divide the input power to 10 ports uniformly. The EPS is designed by varying the output width of each port on a star coupler to achieve an equal power splitting, as indicated in Figure 37 (b). The output aperture width is tapered from center to edge to ensure the same

amount of power is captured from the Gaussian profile in the free propagation region. Our calculated result suggests a ~ 1dB from the splitter with power variation between the ports to be less than 0.1 dB. We fabricated a single equal power splitter for testing and showed its measured performance in Figure 37 (c). The average insertion extra loss is 1.56dB, with 10dB systematic loss. The 0.46dB loss variation on each port shows a uniform power splitting. The EPS in this section is designed by Kuanping Shang.

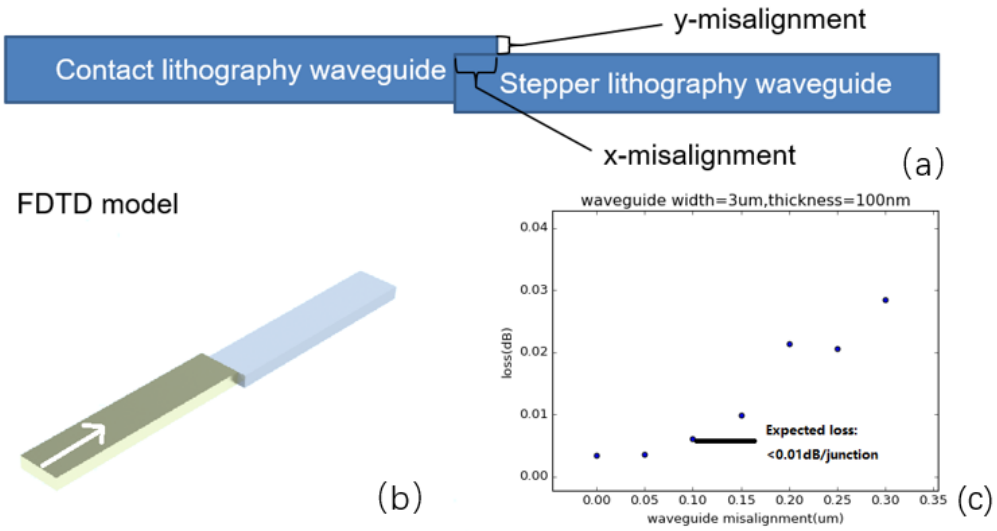

Figure 38 (a) Diagram of waveguide stitching. (b) FDTD modal of waveguide stitch. (c) The extra loss brought by waveguide mismatching.

We develop a wafer-scale fabrication technique by combining projection lithography and contact lithography. Contact lithography can expose an entire 6-inch wafer at one time of exposure but can only achieve a down to 1μm minimum feature size. Our projection lithography gives a 250nm minimum feature size, but the exposure area is limited to a 22mm×22mm area, using the ASML 5500/300 DUV stepper. In our fabrication process, we first pattern the routing waveguides and six alignment marks using contact lithography and etching while preserving the area for the devices that have small <1μm) feature sizes, such as EPS, inversed tapers, and

gratings. Then, we use projection lithography to expose devices with small features guided by the alignment marks and butt connect the devices to the routing waveguides. The waveguide mismatch presented in Figure 38 (a) induces a waveguide mismatch loss with a simulated result shown in Figure 38 (c). We place vernier rulers in the stitching area to check for the mismatch. Figure 40 (b) shows an SEM picture of a vernier ruler, in which the projection lithography fabricates the left side while the contact lithography fabricates the right side. The misalignment between the two times of lithography is mainly decided by the quality of the alignment marks, which can be less than 60nm if the alignment marks are ideal. We practically achieved ~100nm misalignment by optimizing the contact lithography process, which induced a negligible insertion loss at the connections.

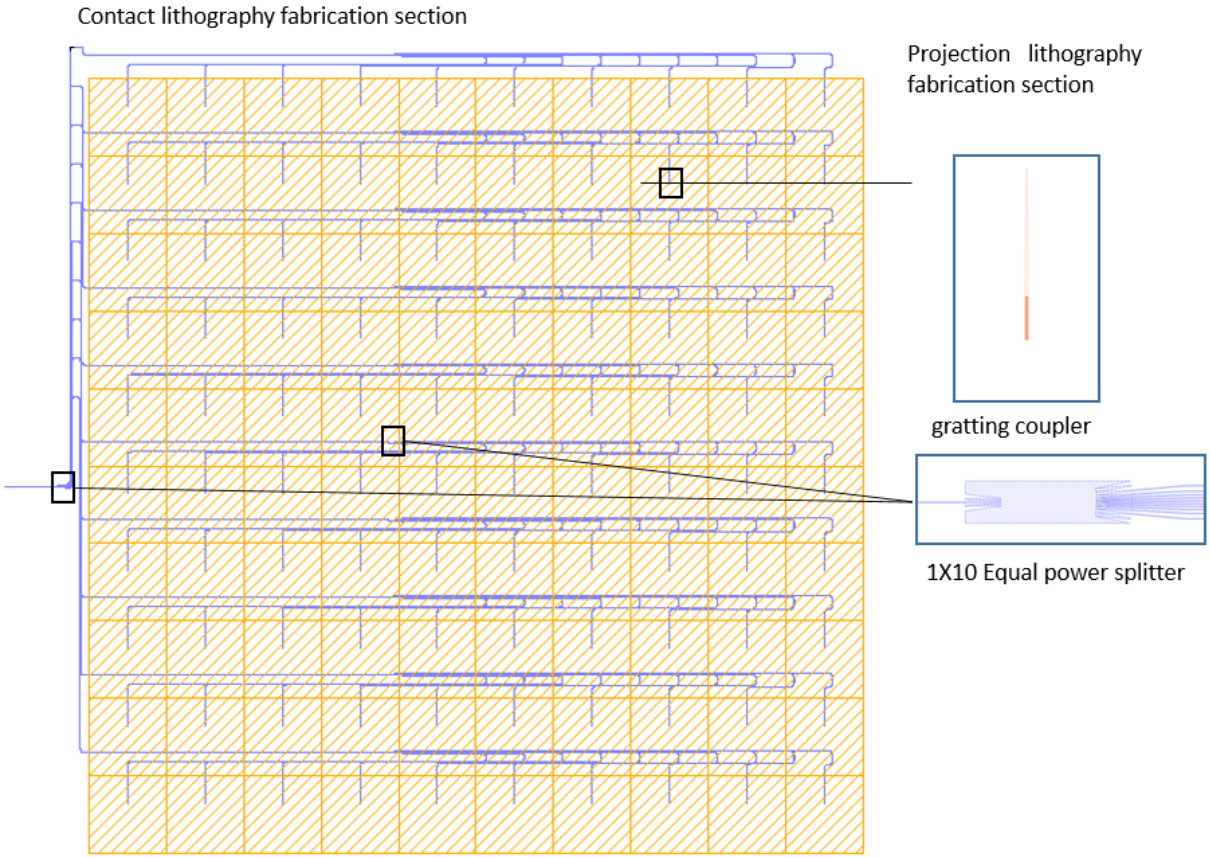

Figure 39 The layout of a wafer-scale grating array.

Due to the fabrication difficulties of the flip-chip bonding on a 150 mm wafer, we fabricate a wafer-scale grating array as a proof-of-concept demonstration, with the layout shown in Figure 39. This layout uses the same design as our WSI in Figure 36 except for changing the evanescent couplers to grating couplers so we can observe the outcoming light using an IR camera. Figure 41 (b) shows the simulation of the grating couplers. Besides, we demonstrated our waveguide stitching and uniform power distribution. Figure 40 shows the SEM photos after the waveguide etching (including photoresist removal). We place pairs of vernier rulers to measure the misalignment between the projection lithography and contact lithography. Figure 40 (b) and (c) shows the waveguide stitching with less than 100nm misalignment. Figure 40 (d) and (f) shows the SEM photos of the equal power splitter and the gratings, proving our capability to fabricate small features. The grating at the terminals has a 1.2μm period and a 50% duty cycle using a fully etched process with almost 50% of the optical power coming to the top. The 100nm thickness of the Si_3N_4 platform maintains a weak emission.

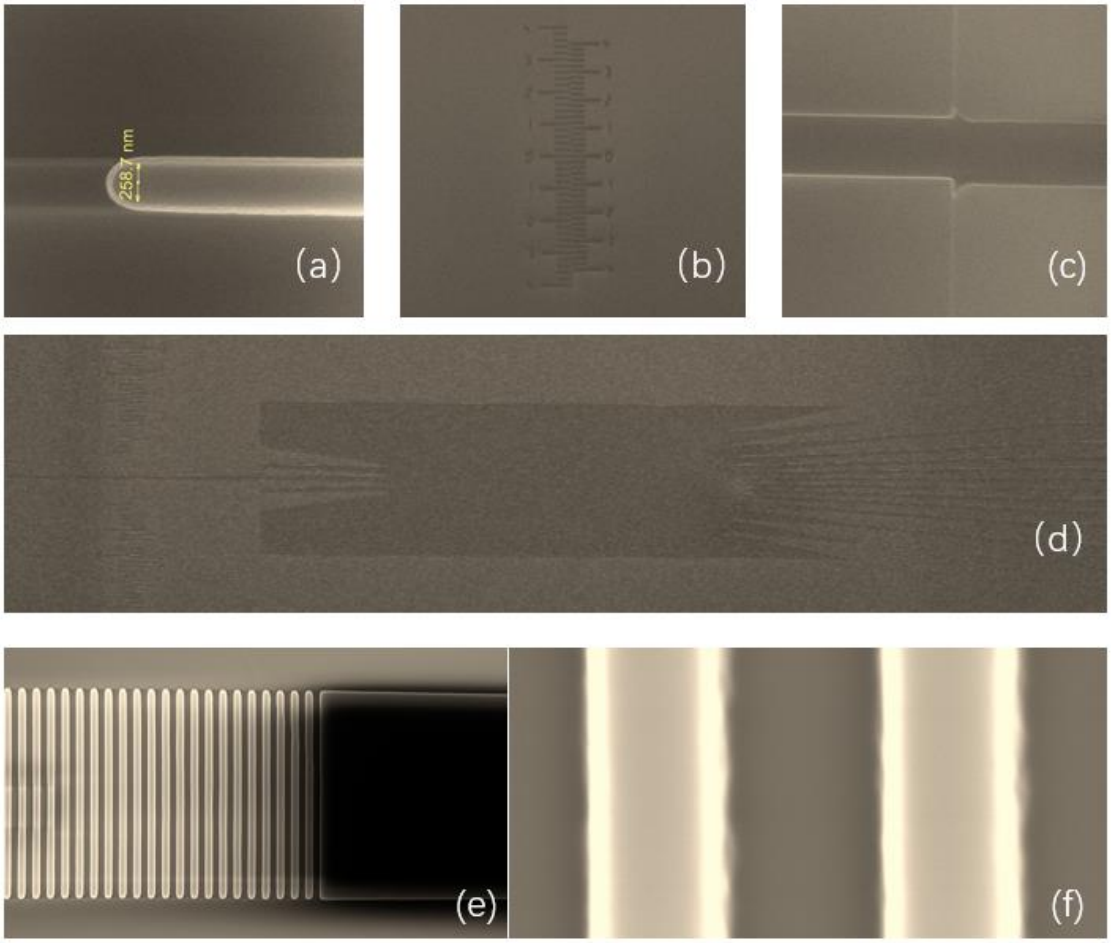

Figure 40 SEM photo on the wafer-scale grating array. (a) Inverse taper coupler tip end. (b) Vernier ruler for measuring stitching misalignment. Smaller than 100nm is observed on the ruler. (c) Waveguide stitching section. The waveguide width is 3μm. The left part is patterned by projection lithography, while the right part is patterned by contact lithography. (d) Equal power splitter. (e) Grating and bus waveguide. The width of the bus waveguide. The grating has a pitch of 1.2μm and a 50% duty cycle. (f) Zoom in a photo of the grating. About 50% of the duty cycle is achieved by adjusting lithography energy.

The wafer scale grating array is measured using an IR camera on top. We sample a 3×4 array and show the images in Figure 41 (a). We measure the power in the red boxes, and the normalized energy in Figure 41 (c) shows a uniform power distribution.

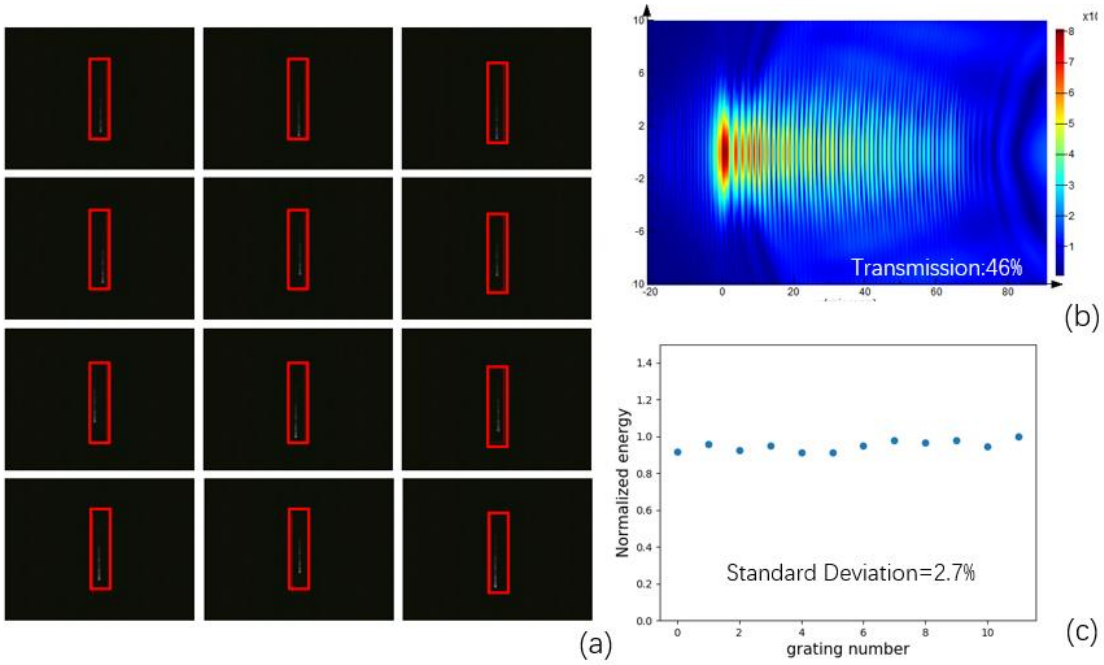

Figure 41 (a) Wafer-scale grating array measurement results sampled at the center of a 150mm wafer. (b) Simulated grating pattern. (c) Normalized output power in (a). Only energy in the red box is calculated to minimize noise.

The future works should be achieving a wafer-scale packaging for a full demonstration of the

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Chapter 4 PICs for Optical Interferometric Imaging

4.1 Overview of the interferometric imaging

This chapter presents the principles of optical interferometric imaging, followed by the fabrication and measurement of the PICs for the imaging. Furthermore, this chapter presents large-scale PICs for high resolution interferometric imaging, including design, fabrication and characterization.

Traditional optical telescopes use lens systems for imaging [109],[110]. The angular resolution of a telescope θ is:

$$\theta = 1.22\frac{\lambda}{D}$$

D is the diameter of the lens aperture, which indicates the lens size needs to increase for a higher resolution. The large-scale optical components limit the scale of traditional optical telescopes.

Interferometric imaging [111]-[113] reconstructs images using the interference of light waves from a scene using the Van Cittert-Zernike theorem [114],[115]. Segmented planar imaging detector for electro-optical reconnaissance (SPIDER) [116]-[119] is an interferometric imaging system using photonic integrated circuits to significantly reduce the Size, Weight, and Power (SWaP) compared to a traditional imaging system with the exact resolution by a factor of 10×~100×. Optical signals from free space are coupled into the PICs through lenslet arrays and be processed using on chip devices, and then be converted to electrical signals using photodetectors for imaging reconstruction. The SPIDER system has multiple baselines to sample the image of objects in the Fourier domain and reconstruct the image based on the measured

interference fringes. The length and number of the baseline set a hardware limitation on the image quality of a SPIDER imager [120],[121].

Figure 42 (a) shows the diagram of the interferometric imaging using one baseline. The light source is placed far from the imaging system to ensure that the light on the imaging system is a far field. The imaging system collects light from 2 apertures with a B distance. The incident light from the two apertures goes through 2 delay lines with D_1 and D_2 delay lengths and is then mixed using a 2×2 coupler. We convert the mixed optical signals into electrical signals using balanced detectors. Considering the electrical field at the detectors are:

$$E \propto e^{j\omega t}\left(e^{-jk(\overrightarrow{LB}+\overrightarrow{D_2})} + e^{-jk\overrightarrow{D_1}}\right)$$

The current given by the detectors is:

$$I \propto 2 + 2\cos\left(k(\overrightarrow{LB} + \overrightarrow{D_2} - \overrightarrow{D_1})\right)$$

We define the visibility function as:

$$abs(V) = \frac{I_{max} - I_{min}}{I_{max} + I_{min}}$$

V represents the visibility function. By applying an inverse Fourier transform of the fringes using the measured complex visibility of many baselines with different lengths, we can reconstruct the brightness distributions of the source.

We present a diagram of the interferometric imaging using PIC in Figure 42 (b) with one baseline. Light from free space is coupled into the optical inputs on the PICs through a lenslet array to maximize the coupling efficiency. We use on-chip phase shifters to tune the effective length on each waveguide. We achieve the optical mixing using a 2×2 coupler routed to optical

outputs so the light can be converted to electrical signals using a linear detector array. We use a path-length-match design on a pair of waveguides in one baseline. The data from the linear detector array is used for imaging reconstruction.

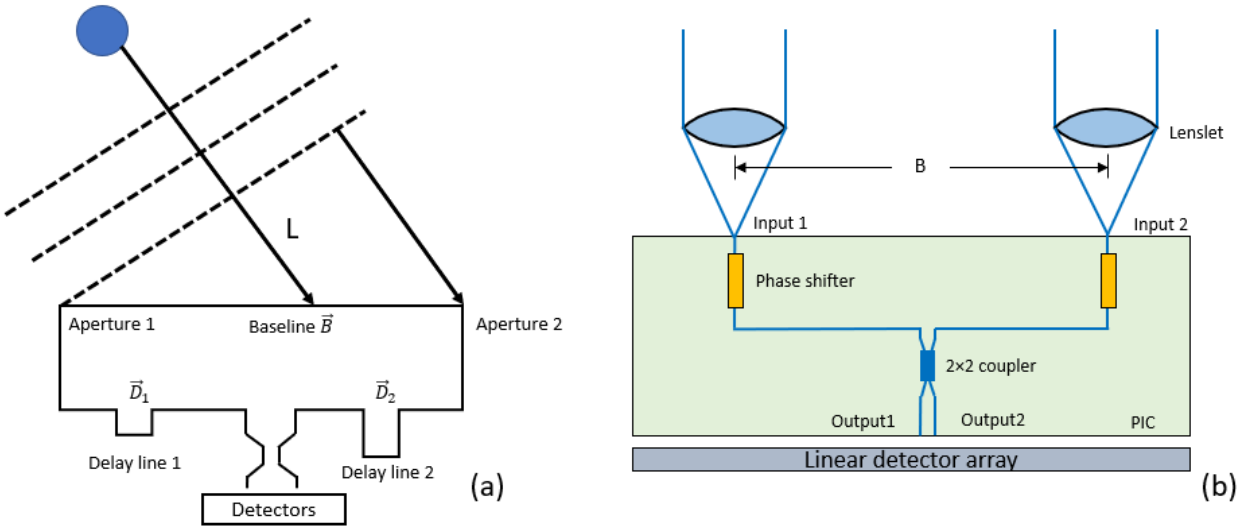


Figure 42. (a) Interferometric imaging diagram. (b) PICs diagram in SPIDER system.

4.2 Platform and devices for SPIDER

The SPIDER chips use a multi-layer silicon nitride platform for the following reasons:

- Supports relatively low propagation loss compared with other material platforms (e.g. silicon),
- Covers a broad transparency window across the 600 - 1700nm spectral band,
- Realizes low-loss and low-crosstalk broadband AWGs, and
- Supports high-density photonic integration.

We used a 150nm thick silicon nitride as a tradeoff between the propagation loss and the footprint of our devices. To further reduce the propagation loss, we developed the process flow in Figure 43, which uses an amorphous Si hard mask to improve the side wall quality. The low

loss waveguide process is developed by Shaoqi Feng and Guangyao Liu. A bottom anti-reflection coating (BARC) is coated onto the wafer to resolve down to 250nm minimum feature size from the stepper by decreasing the reflection from the top surface of the wafer. Different exposure energy is tested to get an accurate feature size for bright regions (tip of an inversed taper) and dark regions (AWGs I/O). The AWGs lithography requires a high exposure power to separate the I/O of Rowland circles, while it could overexpose the tip of an inversed taper. Figure 44 (c) shows an example of a patterned photoresist with an optimized energy for both bright region and dark region density [122]. After amorphous silicon hard mask etching, the photoresist is removed by an oxygen plasma etching. We used the STS-OXIDE MPX APS inductively coupled plasma (ICP) etching system for the silicon nitride etching, which can achieve 4:1 selectivity between amorphous silicon to silicon nitride. Typically, we deposited 80nm amorphous silicon for 150nm silicon nitride etching and over-etching. The remaining amorphous silicon hard mask after the waveguide patterning is oxidized using wet oxidation and will become a part of the cladding. In our multi-layer process, after the Figure 43 step (h), the top surface will be planarized using CMP for the fabrication of the next layer.

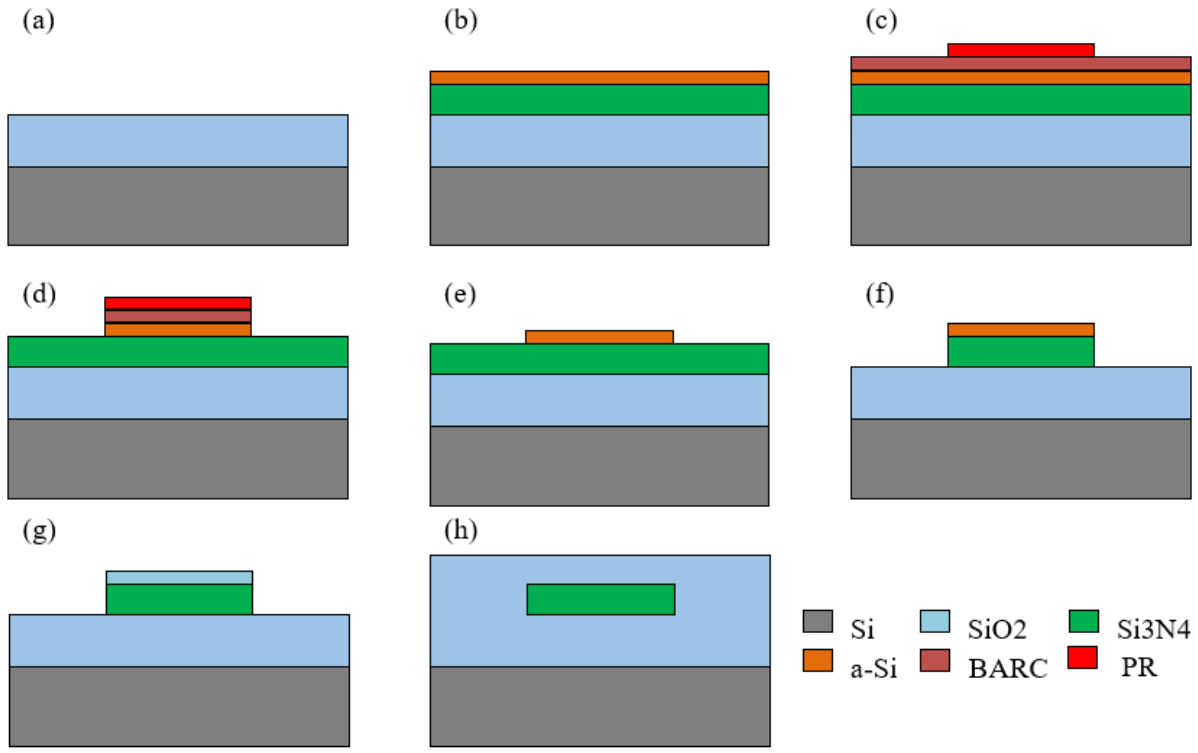


Figure 43 Fabrication process of the low-loss silicon nitride waveguide (a) Wet oxidation. (b) Silicon nitride and a-Si deposition. (c) Lithography. (d) BARC and a-Si hard mask etching. (e) Photoresist removal. (f) Silicon nitride etching. (g) Wet oxidation. (h) LTO deposition.

The waveguide propagation loss and bending loss are measured using the structures shown in Figure 45. We used a 150μm bending radius as a tradeoff between the device footprint and the bending loss. The propagation loss is measured using a set of spiral waveguides with different lengths, while the measured loss is shown in Figure 46. Our low-loss waveguides process achieves a 0.09dB/cm propagation loss and 0.285dB/circle bending loss. We fabricated and tested one broadband AWG (Designed by Dr. Okamoto) with about 30nm channel spacing as a process and design demonstration using the low-loss waveguide process, with a patterned AWG SEM photo presented in Figure 47. Figure 48 (a) presents the measured AWG transmission spectrum calibrated to a straight waveguide, with the center wavelength of each channel listed in Figure 48 (b) and an average of about 4dB insertion loss. The insertion loss of the AWG is

acceptable compared to other terahertz channel spacing AWGs on Silica platform[123]. Considering the longest waveguide, we have ever designed is below 20cm with less than 3 circles bending, the low loss waveguide process satisfies the requirement of our SPIDER PICs.

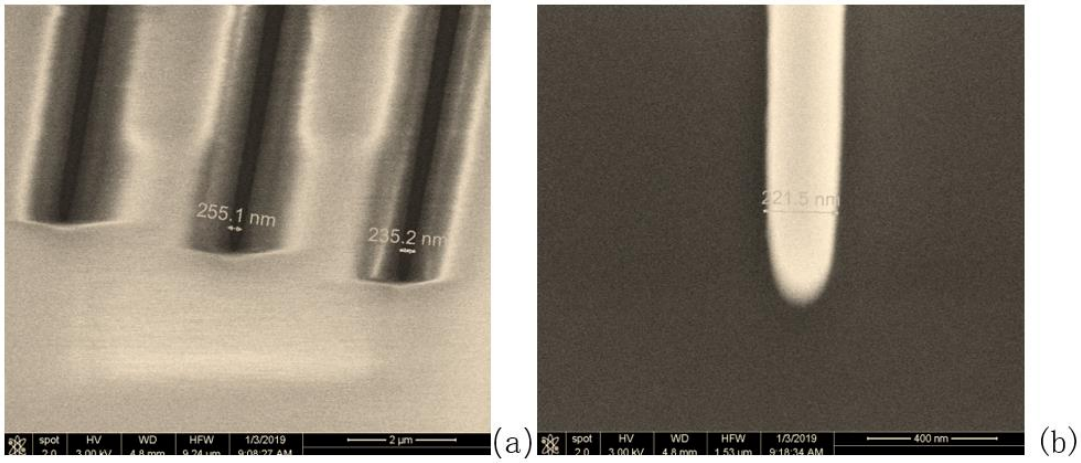


Figure 44. SEM photo of the patterned photoresist using a 15mJ/cm^2 (a) at the AWG and (b) at the tip of the inversed taper.

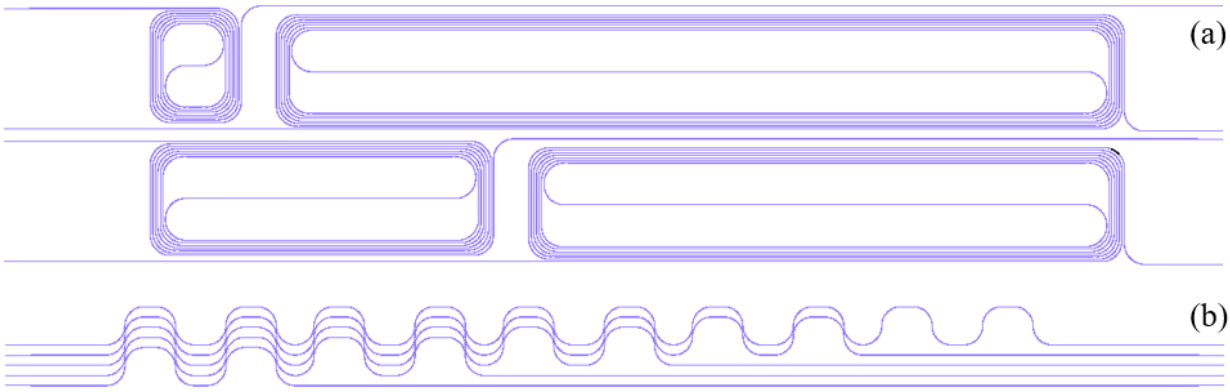


Figure 45 Layout of the silicon nitride test structures. (a) Propagation loss testing structures. (b) Bending loss testing structure.

Our SPIDER PICs use multi-layer platforms to increase the integration density. Except for 150nm Si_3N_4 layers, we use 50nm Si_3N_4 layers as transition layers. The 50 nm Si_3N_4 layers use

the same waveguide fabrication process, except the hard mask thickness for 50nm Si_3N_4 waveguides is 30nm.

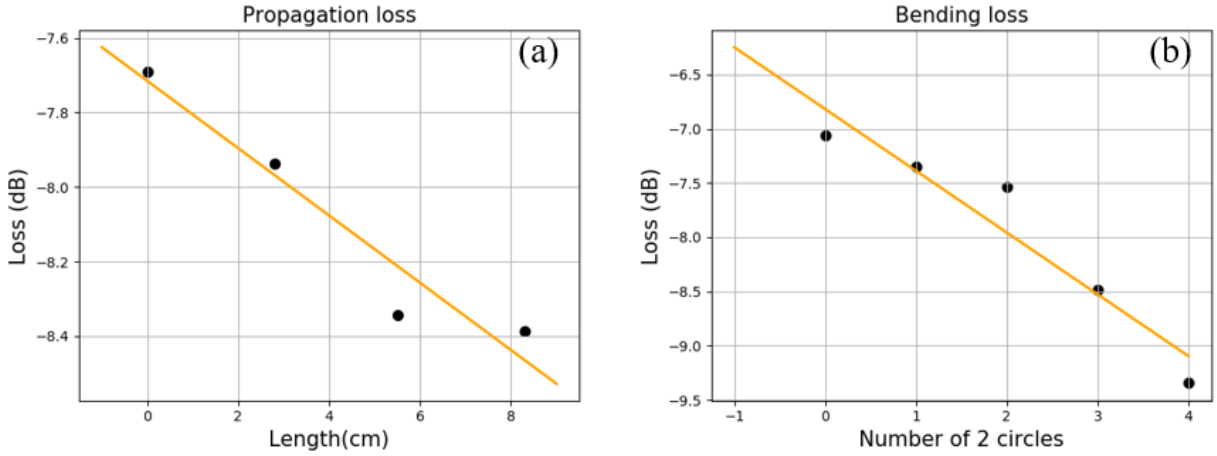


Figure 46 (a) Measured propagation loss. (b) Measured bending loss. One circle means the waveguide bend with 90^o for four times.

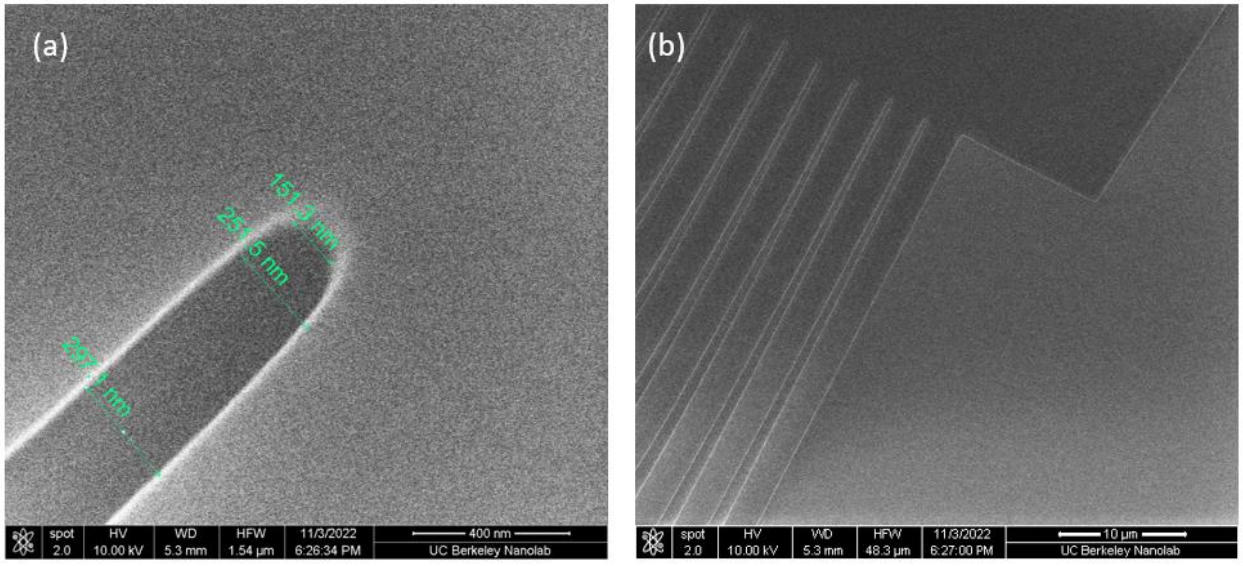
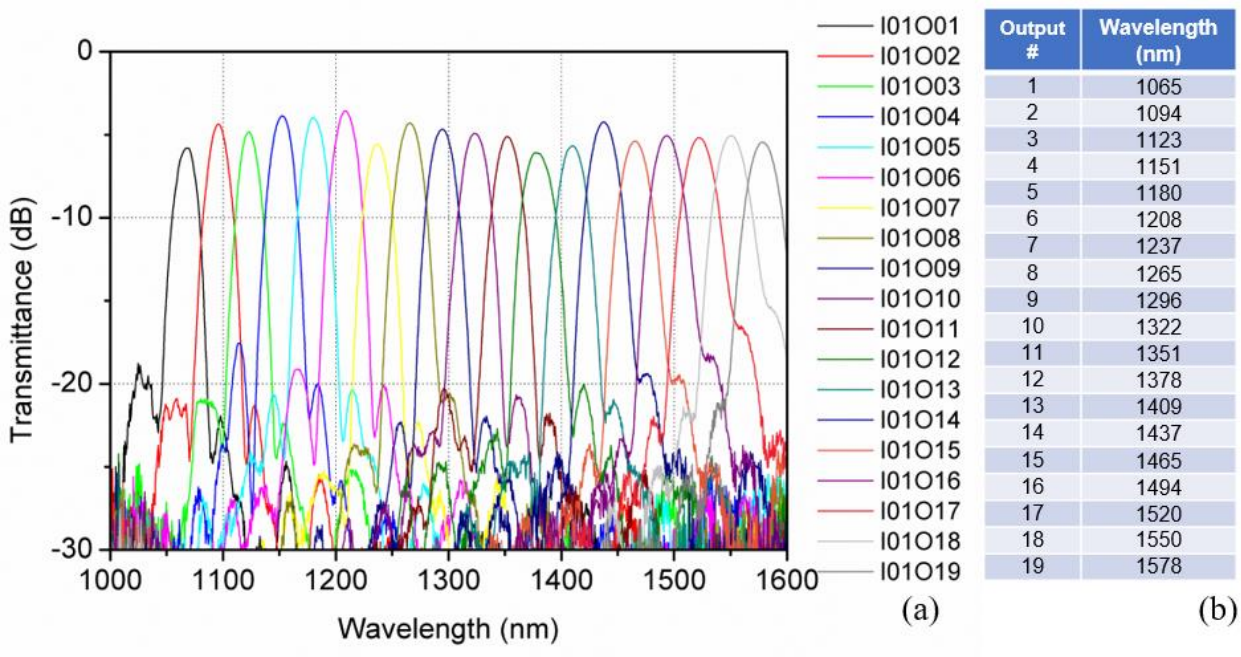


Figure 47 SEM photo of the patterned AWGs (a) gap between 2 inputs and (b) input region.



Output #	Wavelength (nm)
1	1065
2	1094
3	1123
4	1151
5	1180
6	1208
7	1237
8	1265
9	1296
10	1322
11	1351
12	1378
13	1409
14	1437
15	1465
16	1494
17	1520
18	1550
19	1578

(b)

Figure 48 (a) Transmission spectrum of the AWG (b) Channel center wavelength.

4.3 Optical interferometric imaging using a multi-chip system

The first generation of the SPIDER PICs is based on a 3-layer silicon nitride platform for optimizing size and loss. Figure 49 shows the cross-section of the 3-layer waveguide structure.

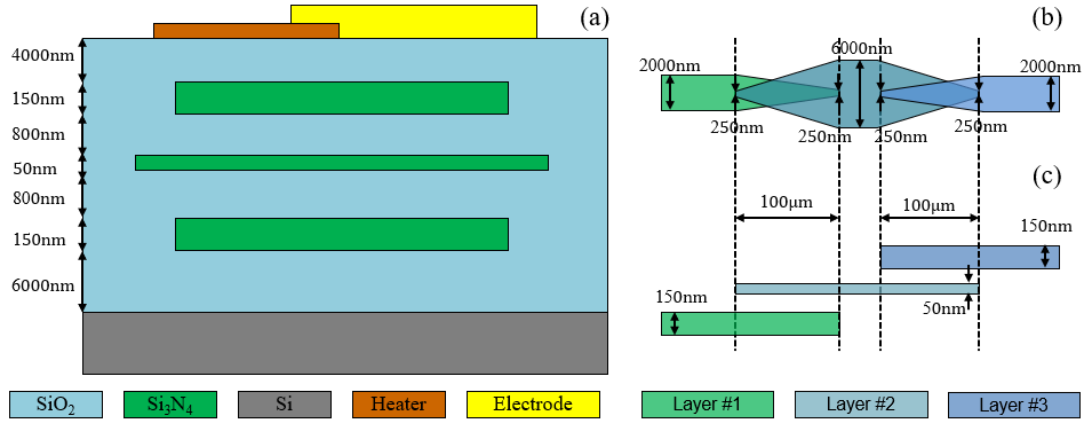


Figure 49 (a) Cross-section view of the 3-layer Si_3N_4 waveguide structure. (b) and (c) Top-down and cross-section view of the inter-layer coupler in the 3-layer Si_3N_4 waveguide structure.

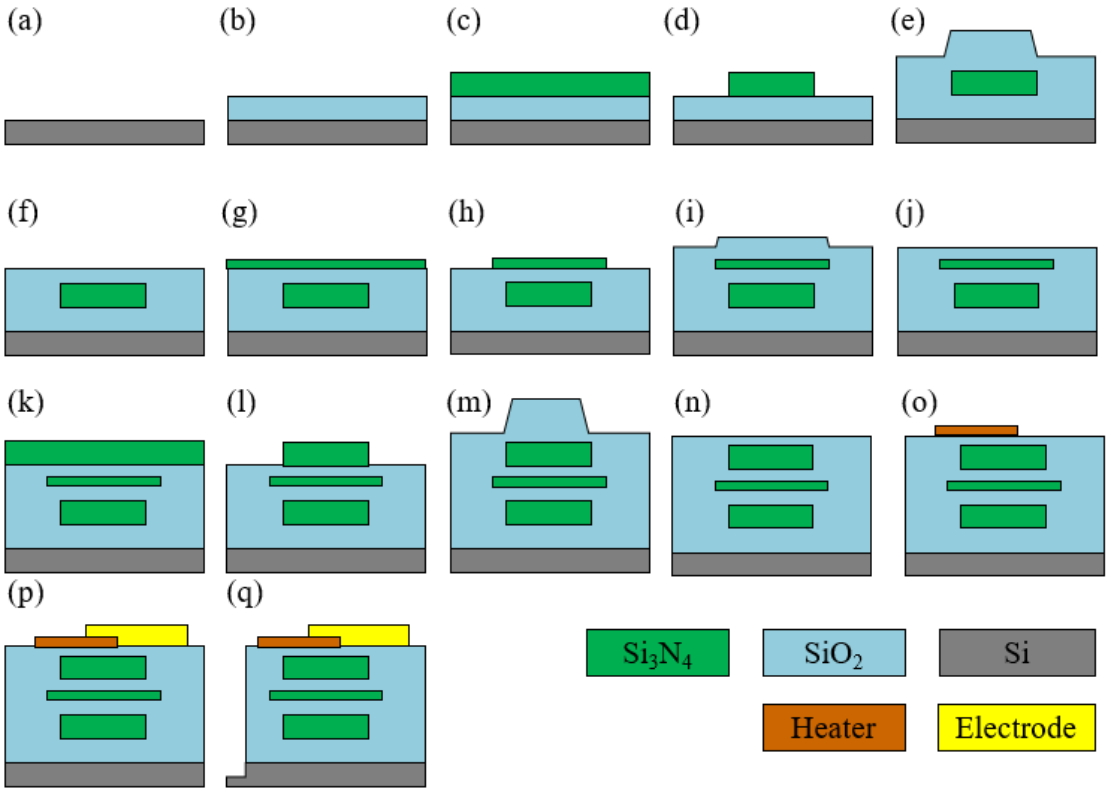


Figure 50 Fabrication process flow of the SPIDER PICs. (a) Initial wafer cleaning for 6-inch wafers. (b) Thermal oxidation. (c) The bottom layer 150 nm Si_3N_4 deposition. (d) 150 nm Si_3N_4 patterning by lithography and etching. (e) First inter-layer SiO_2 deposition. (f) CMP. (g) The middle layer 50 nm Si_3N_4 deposition (h) 50 nm Si_3N_4 patterning by lithography and etching. (i) Second inter-layer SiO_2 deposition. (j) CMP. (k) The top layer 150nm Si_3N_4 deposition. (l) 150 nm Si_3N_4 patterning by lithography and etching. (m) Top cladding SiO_2 deposition. (n) CMP. (o) 20nm Ti / 100 nm Au metal heaters fabrication using metal lift-off. (p) 20 nm Ti / 800 nm Au metal electrodes fabrication using metal lift-off. (q) silicon dioxide and silicon deep etching.

The bottom (layer #1) and top (layer #3) layers are 150nm silicon nitride device layers to accommodate devices for routing, mixing, thermal phase shifter, and demultiplexing so the density of the chip is expanded by a factor of 2, compared to a single layer device. The middle layer uses 50 nm Si_3N_4 waveguides for optical I/O and interlayer transition. The metal layer for thermal phase tuning is fabricated on top of the PICs. The inter-layer optical transition is achieved by using the inverse-taper coupler, as shown in Figure 49 (b) and (c). The tapering width is from 2μm to 250nm, limited by the minimum line width of our lithography. The optical signal from the bottom to the top layer will first be coupled to the middle layer and then coupled

to the top layer. The gaps between each Si_3N_4 layer are 800nm to have a low interlayer coupling loss, while the bottom and top layers are isolated from each other. The two metal layers are on top of the 3rd waveguide layer top cladding for thermal phase tuning. All the thermal phase shifters use 3rd layer waveguides and the heater layer for heating. The heater layer uses 20nm/100nm Ti/Au, and it connects to a 20nm/800nm electrode. The gap between the 3rd waveguide layer and the heater layer is about 4μm to maximize thermal efficiency while preventing any disturbance above the silicon dioxide cladding (especially metals).

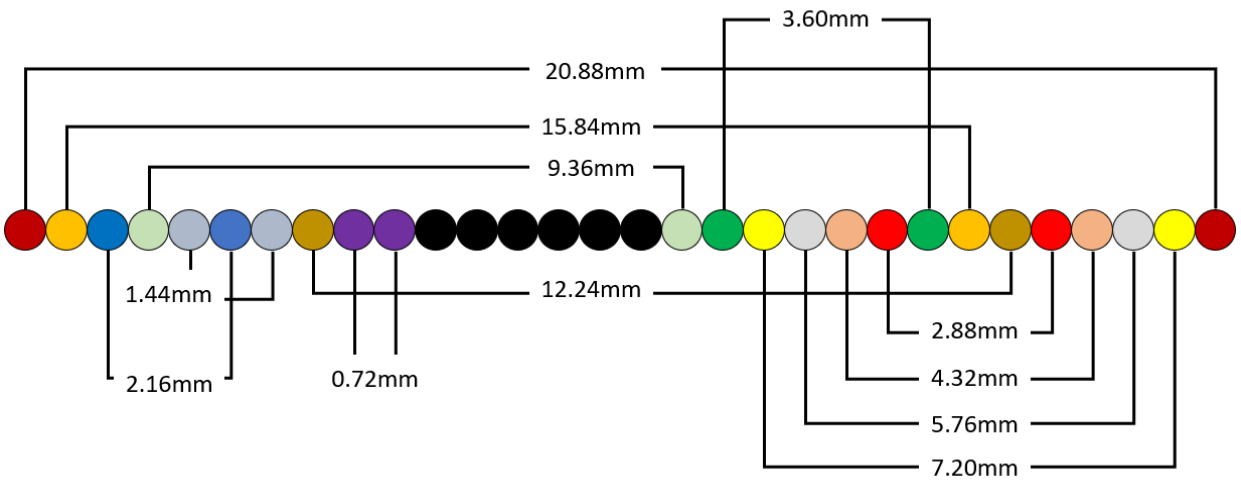


Figure 51 Baseline configuration in the SPIDER PICs designed by Lockheed Martin.

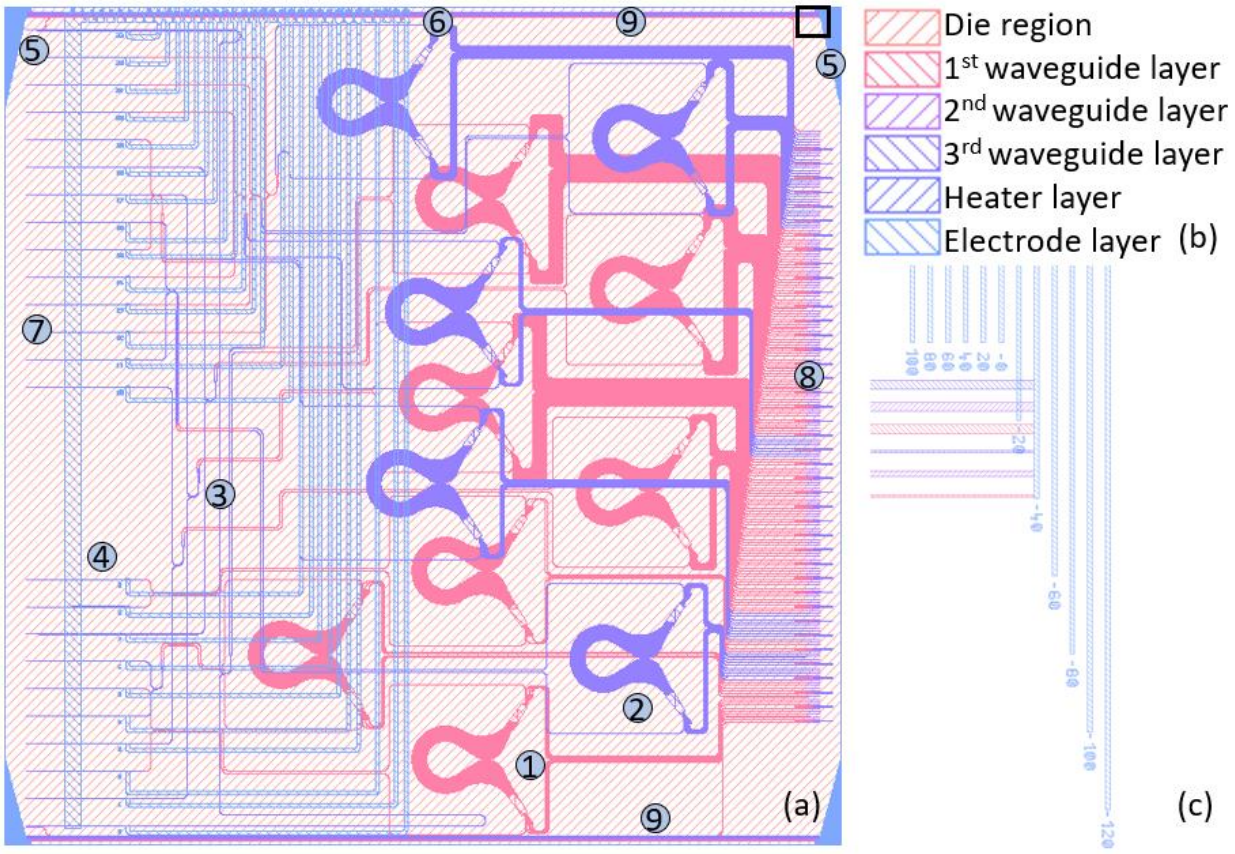


Figure 52 (a) Layout of the SPIDER PICs. Elements are denoted with numbers: 1. AWGs at the first waveguide layer. 2. AWGs at the third waveguide layer. 3. MMI. 4. Thermal phase shifter. 5. Metal ruler for polishing. 6. Electrode I/O. 7. Optical inputs. 8. Optical outputs. 9. Test waveguides. (b) Colors for different layers. (c) Metal ruler for polishing in the black box at the top right corner of (a).

The SPIDER PICs are fabricated on a 6-inch silicon wafer using ASML^{tm} PAS 5500 300 deep-UV lithography stepper technology. Fig. 2 shows the whole fabrication process flow. The bottom cladding is fabricated using a long-time thermal oxidation. In every layer fabrication process, a Si_3N_4 layer will first be grown using Low-Pressure Chemical Vapor Deposition (LPCVD) at 800^{o}C. Then, optical devices are patterned using lithography and etching. A low-temperature oxide (LTO) layer is deposited on top of the patterned Si_3N_4 layer as an inter-layer gap. The top of the LTO will then be planarized by a chemical mechanical polishing (CMP). The polished top surface is ready for the fabrication of the next layer. After the top cladding planarization, we

deposit and pattern the 20 nm Ti and 100 nm Au using electron-beam evaporation and lift-off, followed by 20 nm Ti and 800nm Au. The optical inputs and outputs are exposed using side wall polishing.

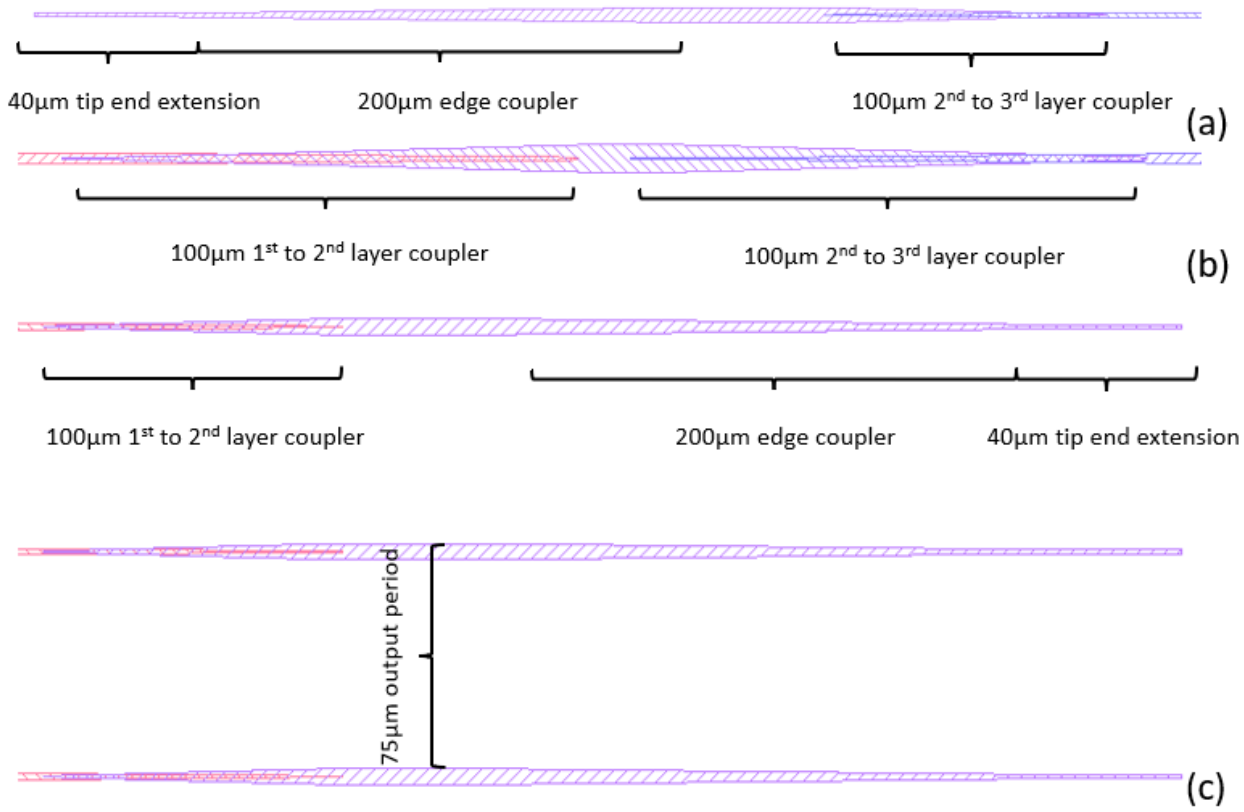


Figure 53 Layout of the SPIDER PICs. (a) Optical input, (b) inter-layer coupler, and (c) output array.

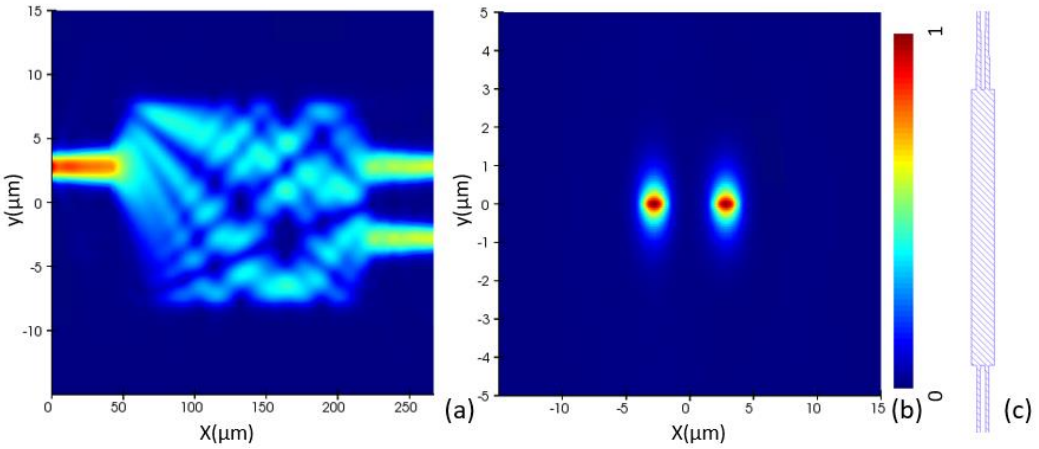


Figure 54 Simulated E field plot of the MMI at 1500nm wavelength. (a) Top view and (b) Cross section view at the end of the outputs. (c) Layout for the MMI.

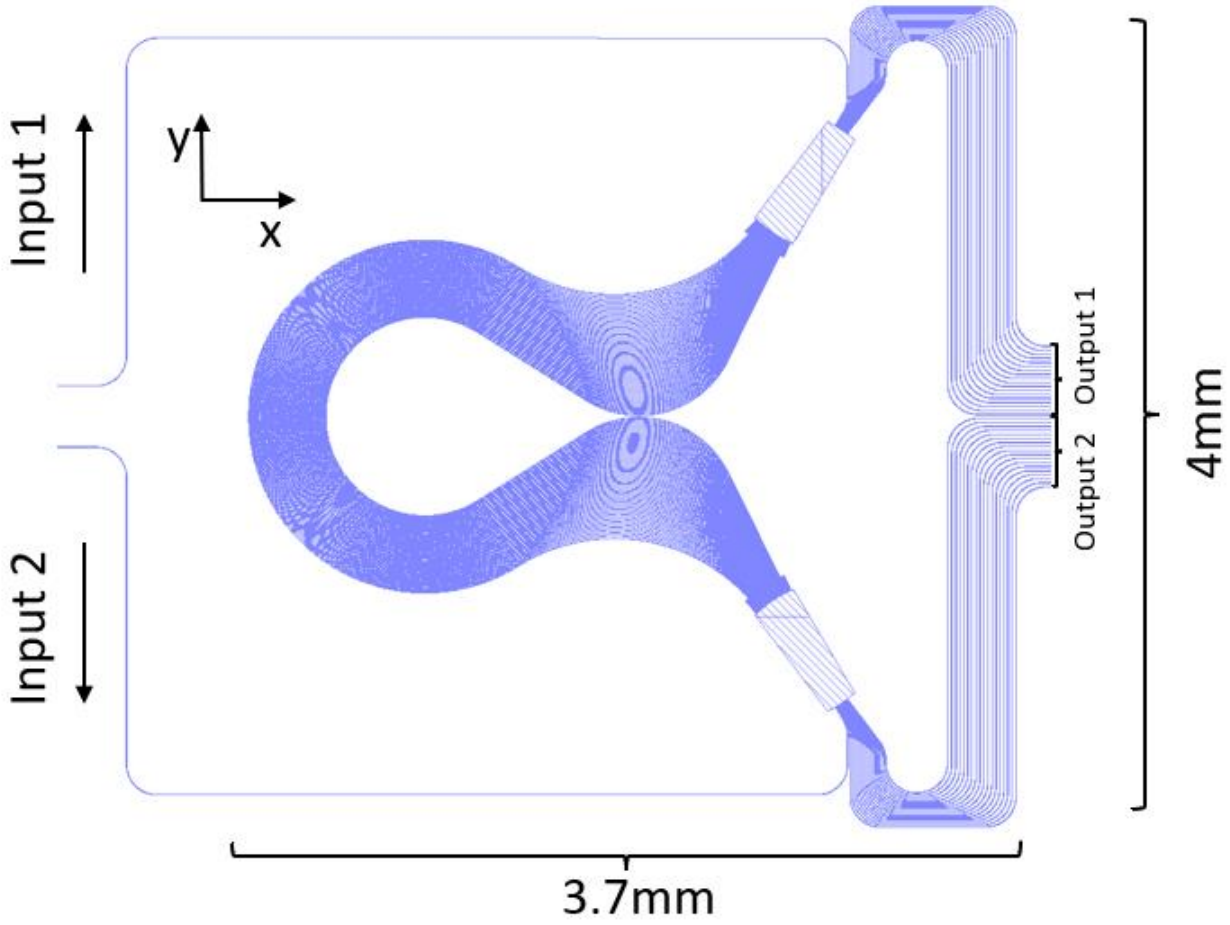


Figure 55 Layout of the broadband AWG.

Table 2 Simulated inter-layer coupling loss between a device layer and the transition layer, with different taper lengths and gap thickness.

Gap(μm) / Taper length(μm)	0.8	1	1.2	1.4
100	0.033dB	0.337dB	0.260dB	1.337dB
200	0.068dB	0.089dB	0.034dB	0.037dB
300	0.104dB	0.090dB	0.062dB	0.115dB
400	0.092dB	0.098dB	0.041dB	0.088dB

Tiehui Su and Guangyao Liu designed the layout shown in Figure 52 to accommodate all elements inside a 22mm×22mm region, which is the size limitation of our ASML 5500/300 DUV stepper at one time of exposure. The 2×2 optical signal mixing is realized using MMI (designed by Tiehui Su) presented in Figure 54 (c). The MMI has a 187μm box length and 16μm box width. The inputs and outputs are tapered to 3μm when it connects to the MMI box. Figure 54 (a) and (b) show the simulated E-field plots at 1500nm wavelength. The insertion loss and the power splitting ratio will shift with the varying wavelength, which leaves us room for further improvement of the bandwidth of the 2×2 couplers. All optics inputs are at the left side of the chip for experiment convenience. During imaging, a lenslet array will be placed on top of the optical inputs, which limits the spacing between the adjacent two inputs to higher than 700μm. The input signal is then transmitted into the 3rd layer using the layout presented in Figure 53 (a). The output signal is detected using a linear photodetector, so the optical outputs with the layout shown in Figure 53 (c) are arranged into an array with a 75μm period centered at the right side of the chip. Both inputs and outputs use the same edge coupler design. The edge couplers have a 200μm length taper on the 50nm Si_3N_4 layer with a 40μm extension at the end of the taper to have a buffer region for side wall polishing. Figure 53 (b) presents the layout of 2 length inter-layer coupler that can transmit the light from the bottom layer to the top layer. The 100μm taper

length is decided by minimizing the device footprint with a low coupling loss (below 0.5dB) using the simulated coupling loss shown in

Table 2. Straight waveguides for testing and references are placed on the top and the bottom of the chip.

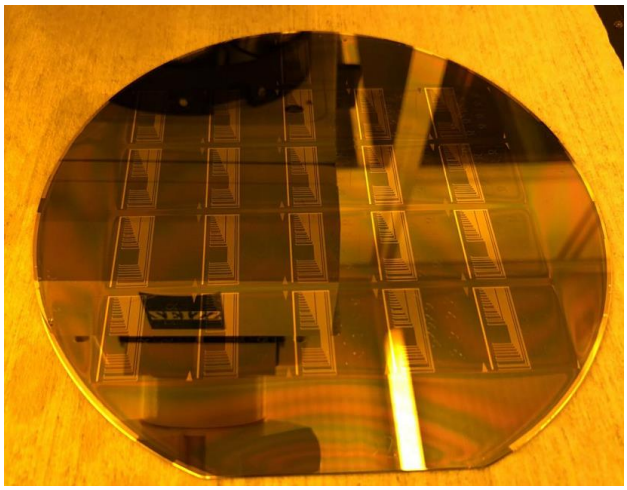


Figure 56 Photo of the fabricated SPIDER PICs wafer.

After the chip fabrication, including the wafer dicing, we use a mechanical polishing process to make the input and output facet smooth, which results in a lower and more consistent coupling loss. Four metal rulers for guiding the polishing are designed on the four corners of the chip, and the zero point on the ruler marks the tapered end. Considering the 40μm tip end extension, the polishing is targeted to stop at the -20μm position.

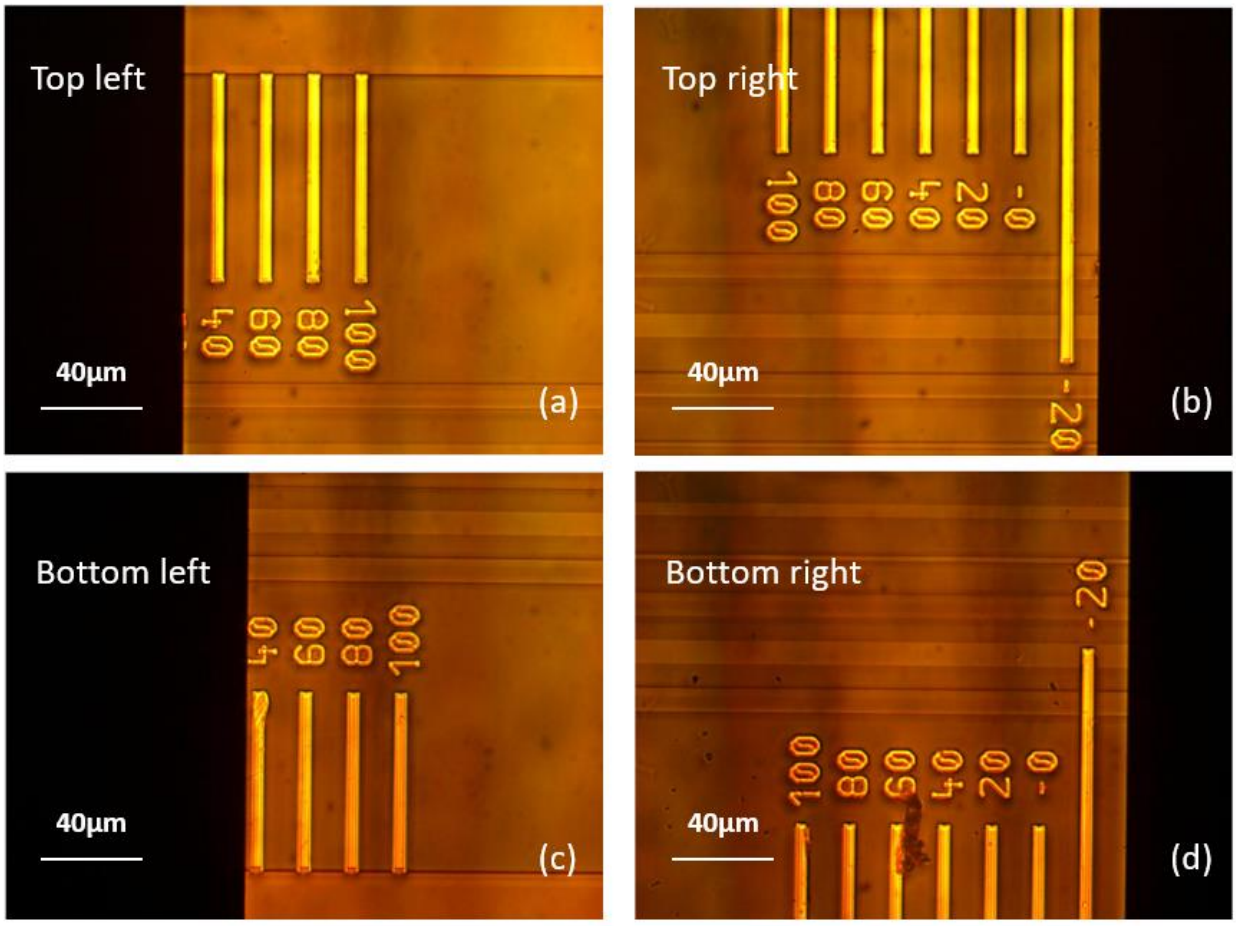


Figure 57 Microscope photo of the PICs corners after polishing. (a) Top left corner, (b) top right corner, (c) bottom left corner, and (d) bottom right corner.

To further improve the device density, we reuse the two sides of the broadband AWG, as shown in Figure 55. The broadband AWG we use has a 3.7mm×4mm device size, including the inputs and outputs, and it is symmetrical along the center x-axis. The AWG has 19 optical I/O on each side with 3.3 THz channel spacing. We use the first I/O on each side as inputs and the rest 18 I/O as outputs, so one AWG works as two 18 channel 3.3THz DEMUX. The input optical signal from input one will be split according to its wavelength and routed to output 2. By using the multi-layer process and the proper configuration of AWG, we process the optical signal from up to 24 channels with 12 AWGs in 2 device layers. For measurement and data processing

convenience, some of the outputs of the AWGs are not needed and are not connected to the chip output.

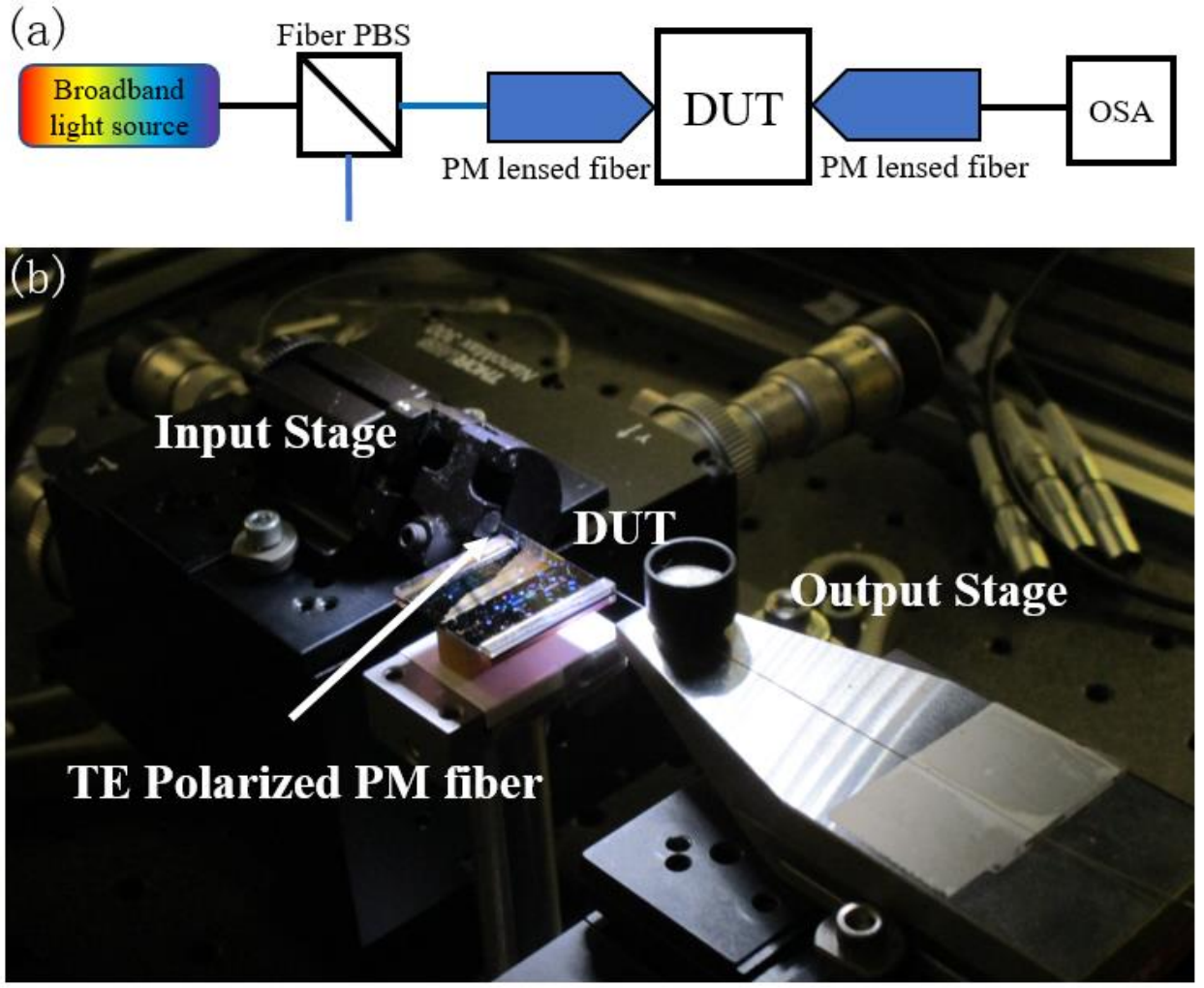


Figure 58 (a) Diagram of the PICs measurement setup. (b) Photo of the measurement setup with a device under testing (DUT).

We fabricated three SPIDER PIC wafers, and one of them is shown in Figure 56. There are a total of 20 dies on one wafer, and the four dies on the corner of the wafer can have poor quality and will not be tested. The rest part of the wafers is diced into 22mm×22mm dies and polished to get smooth sidewalls. Figure 57 shows the microscope photos at the four corners of one die after polishing. The top views show the chip polishing is smooth, and no obvious tilt angle is observed

on both sides. The right-side polishing stops between -20μm to -40μm, and the left-side stops between 20μm to 40μm.

A total of 21 dies are required to make the multichip imaging system, and each die in the system is tested using the measurement setup shown in Figure 58 (a) and part of its photo shown in Figure 58 (b). We use a commercial broadband laser (NTK COMPACT) as the light source and use a calibrated PBS with PM fiber to make sure that the input optical signal to the chip is in TE mode. The output signal is then measured by an optical spectrum analyzer (OSA). The whole measurement setup has a working bandwidth that covers from 1100nm to 1700nm wavelength. The total insertion loss includes the waveguide propagation loss, inter-layer coupling loss, AWG insertion loss, inter-layer coupling loss, and MMI loss. The total insertion loss is higher when the wavelength comes away from 1550nm wavelength since the MMI and waveguides are optimized around 1550nm wavelengths. The waveguides on the 3rd waveguide layer can have a higher propagation loss compared to the 1st waveguide layers since the 3rd layer uses a polished LTO as the bottom cladding, which has a lower quality and a higher surface roughness compared to the silicon dioxide from wet oxidation at the bottom.

We present another 6 AWGs' transmission spectrum in Figure 59. The measurement results show a high robustness in our device fabrication. We observed the AWGs work as demultiplexer at the desired wavelength and there are a variation of insertion loss and channel center wavelength of different AWGs. The variation comes from the imperfect fabrication mainly in the following aspects: (1) nonuniform CMP, (2) nonuniform Si_3N_4 layer deposition, (3) particles or other damaging on waveguides, (4) nonuniform etching profile. Those imperfections can cause variation on the loss and effective index of the waveguides and eventually result in the variations.

The measurement spectrum in this Chapter is finished by me, Guangyao Liu and Junjie Hu.

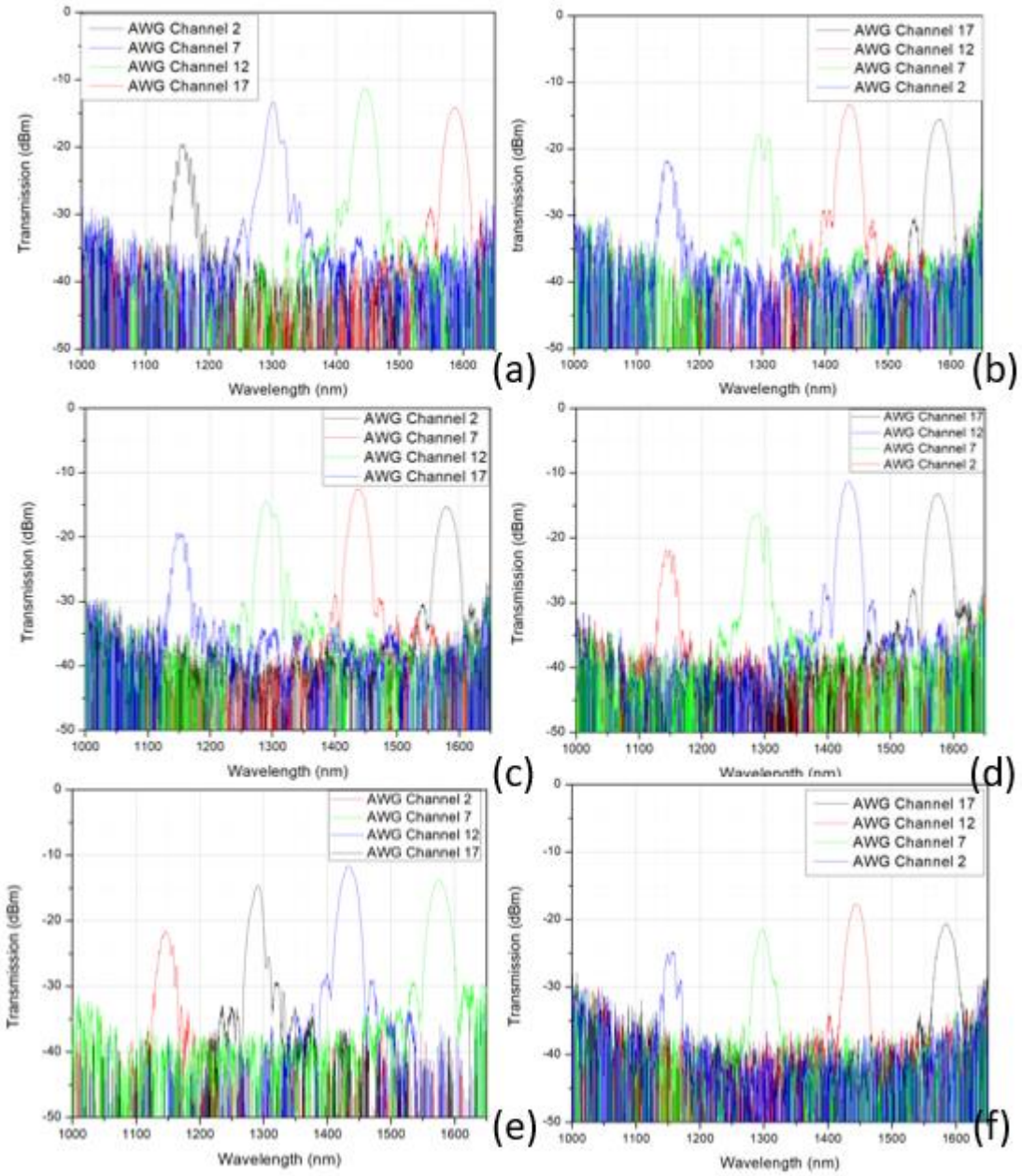


Figure 59 Transmission spectrum of 6 AWGs at six chips, calibrated to the straight waveguide at the same layer.

4.4 Large-scale Si3N4 Integrated Circuit for High-resolution Interferometric Imaging

The SPIDER system has multiple baselines to sample the image of objects in the Fourier domain and reconstruct the image based on the measured interference fringes. The length and number of the baseline set a hardware limitation on the image quality of a SPIDER imager. Especially, the maximum baseline determines the resolution of the imager. The goal of the SPIDER SuperPIC project, which is the second generation of the SPIDER chips, is to greatly increase the scale and the combination of the baselines. Our group previously demonstrated 12-baseline 22×22*mm* Si_3N_4 PICs while the chip size is limited by the ASML 5500/300 DUV stepper. We extend the die size by stitching multiple exposure areas [124].

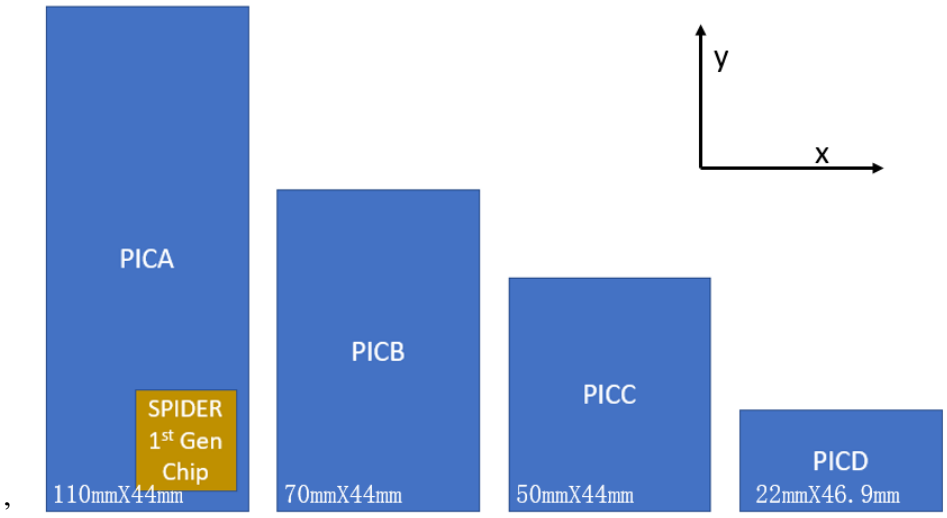


Figure 60 Relative size of the SuperPIC PICs. The yellow square shows the size of the first-generation chip with a 22mm-by-22mm size.

In the SuperPIC project, we designed and fabricated 4 PICs with a biggest 110mm×44mm size and 32 baselines for a high-resolution SPIDER imager with 1200nm~1600nm working wavelength, which improves the maximum baseline length from 20.88mm to 98.778mm. We use a wafer-scale fabrication process that uses image stitching to overcome the size limitation of the

stepper at one exposure. We name the 4 PICs as PICA, PICB, PICC, and PICD with an order of size. Figure 60 shows the relative size of the 4 PICs compared to the first generation of the SPIDER chips. All the optical I/O are on the edge of the y direction and have a similar chip length along the x direction for minimizing the packaging difficulty. The PICD is extended from the first generation of the SPIDER chip with a cross-section view diagram shown in Figure 61 (b), and it is longer than the other PICs to minimize the design difficulty.

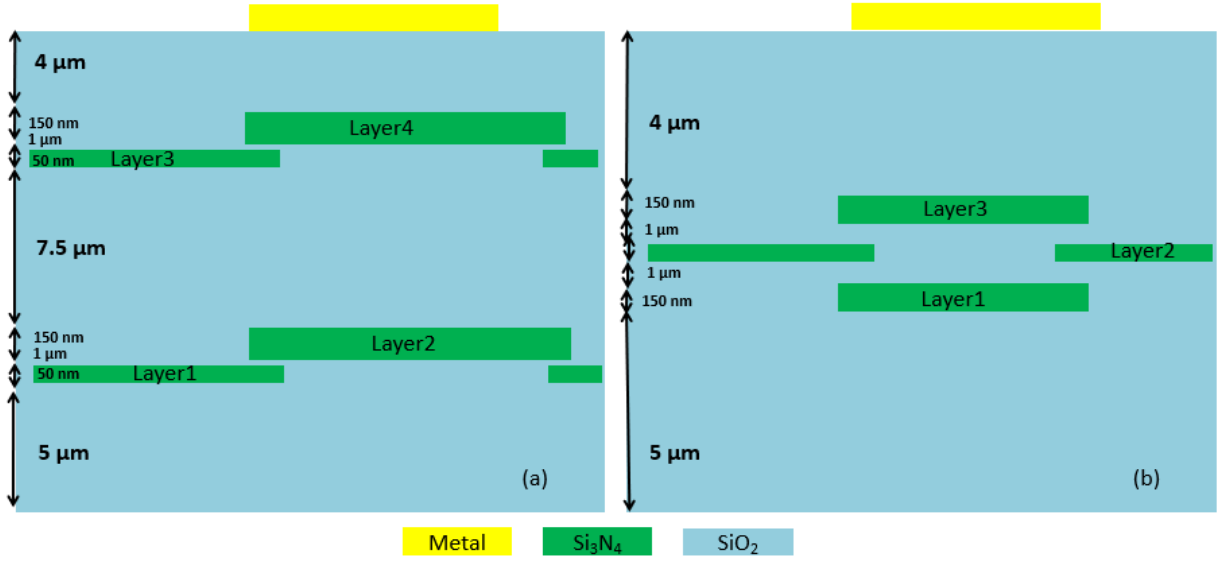


Figure 61 Cross-section view diagram of the SuperPIC PICs. (a) PICA, B, and C. (b) PICD.

PICA, B, and C have similar designs but different baseline lengths. We take the PICA design as an example. The PICA have the diagram shown in Figure 62 (a), which consists of pairs of waveguide with path length-matching, thermal phase shifter, 2×2 multimode interferometers(MMI), and arrayed waveguide gratings (AWGs) while all elements support the whole working bandwidth. The PICA, B, and C are built on a 4-layer Si3N4 platform, as shown in Figure 61 (a), for capturing and processing light with high density. The whole PICs are

fabricated on silicon substrates. Vertically, the Si3N4 layers are split into the bottom sets and the top sets with 7.5μm silicon dioxide in between, which isolate the two sets of layers to enlarge the integration density by a factor of 2. Each set includes a 150nm Si3N4 layer for optical signal routing and process and a 50nm Si3N4 layer for optical input/output and waveguide crossing. Table 3 shows the simulated waveguide crossing loss at the 50nm Si3N4 layer with different waveguide width. Our standard waveguide design uses 2μm width in the 150nm Si3N4 layer and 5.5μm in the 50nm Si3N4 layer. As a comparison, the simulated waveguide crossing loss on the 150nm layer is 0.26dB, while the inter-layer crossing loss with a 1μm gap is around 0.5 dB. We use 5.5μm as the 50nm Si3N4 waveguide width as a tradeoff between waveguide crossing loss and propagation loss. Broadband inter-layer couplers with below 0.5dB coupling loss in the working bandwidth ensure the connections in a set. Two metal layers are fabricated on top cladding to tune the thermal phase shifters in the top set. The input and output facets of the PICs are exposed using a silicon deep etching technique due to the difficulty of polishing such big chips.

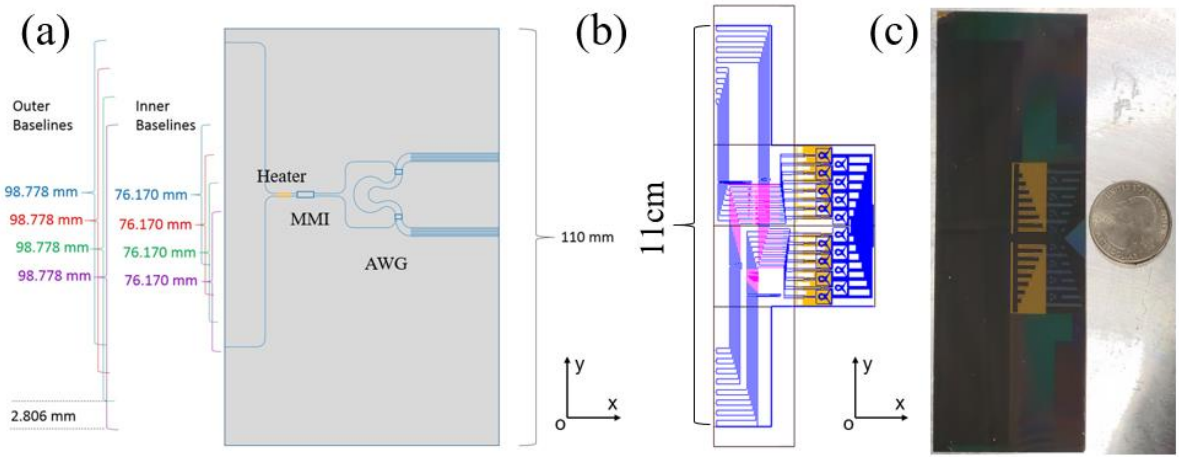


Figure 62 (a)Top view of the Si3N4 PICs with baseline length and locations. (b) The layout of the Si3N4 PICs. (c) A photo of the PIC.

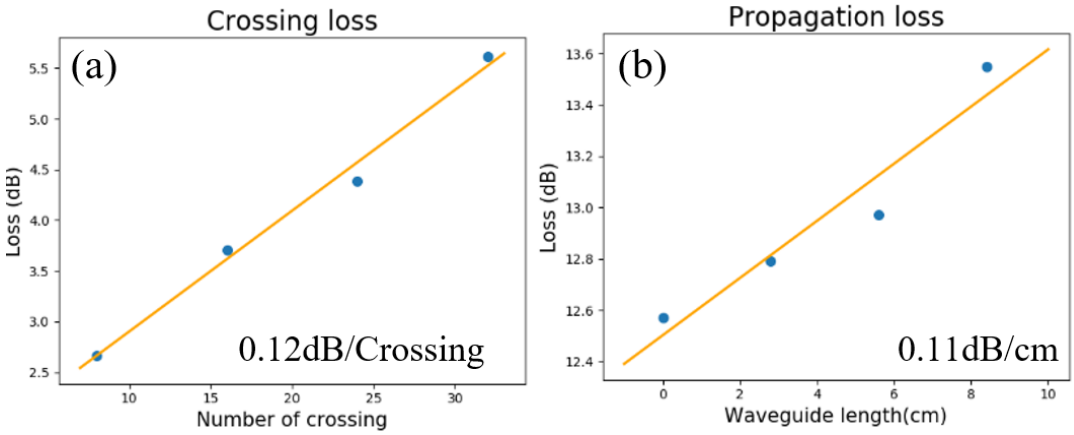


Figure 63 (a)Measured waveguide crossing loss on 50nm Si3N4 layers. (b) Measure waveguide propagation loss on 150nm Si3N4 layers.

Broadband light from the two optical inputs in one baseline will be routed into its MMI through a phase-matching design realized by making all elements the same on the two routes, including the length of the waveguides on each layer, number of waveguides bending, number of waveguides crossing and number of the inter-layer coupling. Figure 67 (b) and (c) shows that we use dummy waveguides to ensure the path length matching. The optical signals are mixed in the MMIs and demultiplexed at 3.3THz channel spacing AWGs into 18 wavelength channels while only 14 channels are in the working bandwidth (1200nm~1600nm). The optical signal with a single wavelength at each waveguide will be detected by an off-chip linear detector array and processed by an image reconstruction algorithm. Figure 62 (b) shows the layout of the PICs, including a routing region on the left and an AWG engine on the right. The bottom and top sets are highly overlapped vertically with optical isolation to accommodate 32 AWGs in one PIC. The total length of the chip is 11cm long in the Y direction. All the optical outputs are routed to a 12mm length region at the right side of the chip for detection. During fabrication, the whole layout is split into 8 22×22mm tiles to meet the maximum image size of our stepper and stitched together during exposure with lower than 60nm misalignment, which introduces a lower than 0.05dB loss per tile.

The routing region of the PICA has six tiles on each layer, and the AWG engine has two tiles. The two AWG engine tiles are mirrored with each other. All the waveguide crossings happen at 50nm Si3N4 layers to minimize the loss, with measured waveguide crossing loss indicated in Figure 63 (b). There are 23 waveguide crossings on one route, so the total crossing loss is below 3dB. We use the low-loss Si3N4 waveguides fabrication process with propagation loss of 150nm Si3N4 waveguides shown in Figure 63 (c) to achieve a low loss (below 2dB) optical routing in wafer-scale, considering the longest route on the PICs is below 13cm. The edge of the dies is exposed using a deep etching technique. Figure 62 (c) shows a photo of one PIC with a quarter dollar as a reference.

The fabrication process of the SuperPIC PIC PICA, B, and C are presented in Figure 64. 4 silicon nitride layers, two metal layers, and one deep etching layer are fabricated on top of a 6-inch silicon substrate. The wafer is firstly cleaned using a 120^{o}C piranha bath and then followed by an LPCVD silicon nitride deposition. After the silicon nitride layer patterning using lithography and etching, we deposit LTO as the interlayer cladding material. We use CMP to planarize the LTO surface so that the wafer is ready for a 2nd silicon nitride layer fabrication. Inter-layer gap thickness is controlled by adjusting the deposited LTO thickness and the time duration for CMP. We fabricate four silicon nitride layers by repeating the previous steps. After the top cladding planarization, we patterned metal heaters and electrodes using metal lift-off. The optical inputs and outputs are exposed using a silicon deep etching [125]. Due to the difficulty on etching a 20μm SiO_2, we used a 11μm photoresist as the mask material, which has a 1:2.6 photoresist: SiO_2 selectivity. The fabrication work in this section is finished by me and Rijuta Ravichandran.

The cladding thickness between the 2nd silicon nitride layer and the 3rd silicon nitride layer is about 7.5μm, which can cause wafer expansion and impair the inter-layer alignment accuracy. We fabricated alignment marks on the 3rd silicon nitride layer, which are aligned to the alignment marks on the 1st layer to guide the fabrication after the 3rd layers.

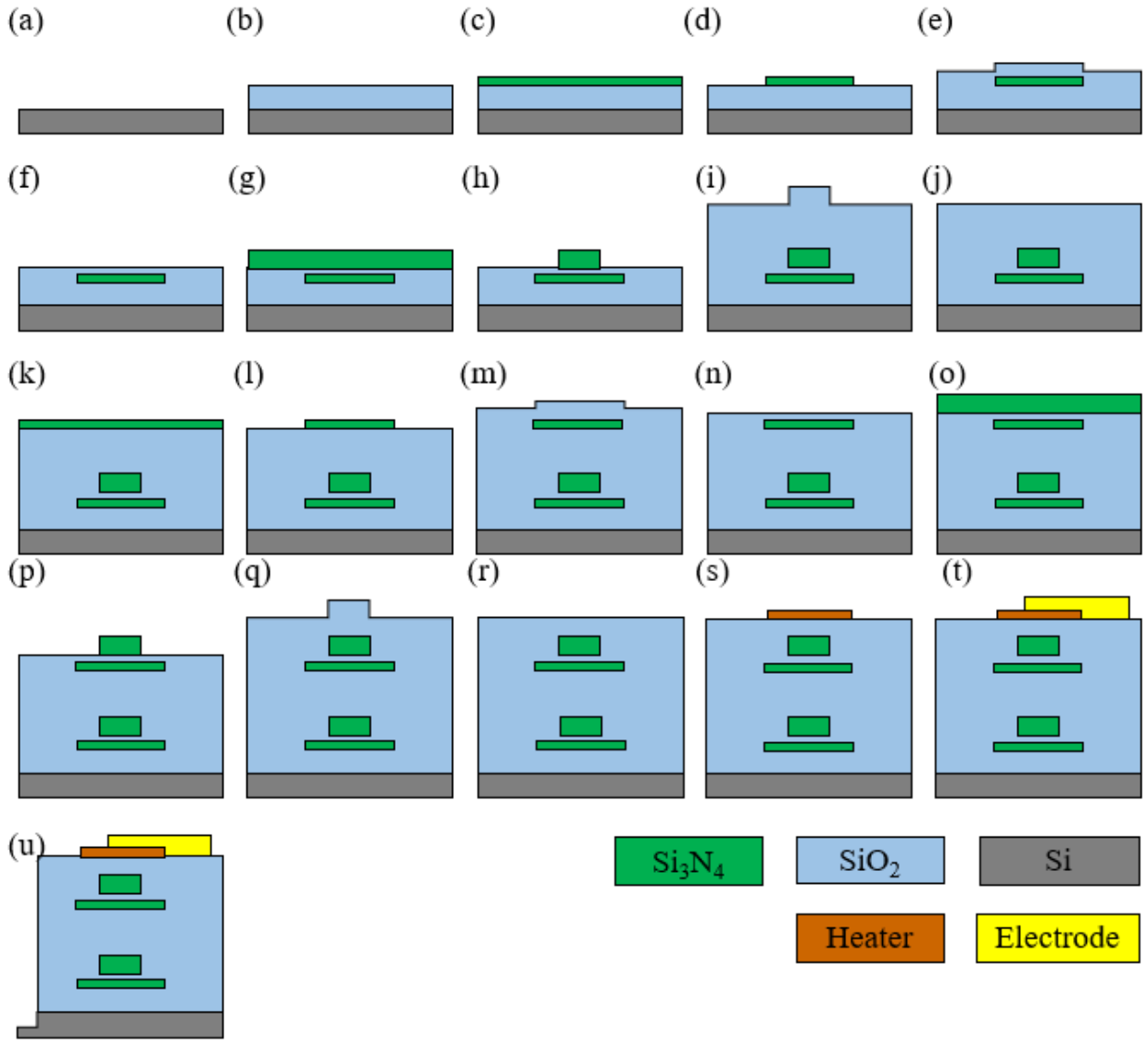


Figure 64 Fabrication process of the SPIDER SuperPIC PICA, B and C. (a) Initial wafer cleaning for 6-inch wafers. (b) Thermal oxidation. (c) The 1st layer is 50 nm Si3N4 deposition. (d) 50 nm Si3N4 patterning by lithography and etching. (e) First inter-layer SiO_2 deposition. (f) CMP. (g) The 2nd layer 150 nm Si3N4 deposition (h) 150 nm Si3N4 patterning by lithography and etching. (i) Second inter-layer SiO_2 deposition. (j) CMP. (k)

The 3rd layer 50nm Si3N4 deposition. (l) 50 nm Si3N4 patterning by lithography and etching. (m) Inter-layer SiO_2 deposition. (n) CMP. (o) The 4th layer 150nm Si3N4 deposition. (p) 150 nm Si3N4 patterning by lithography and etching. (q) Top cladding SiO_2 deposition. (r) CMP. (s) 20nm Ti / 100 nm Au metal heaters fabrication using metal lift-off. (t) 20 nm Ti / 800 nm Au metal electrodes fabrication using metal lift-off. (u) silicon dioxide and silicon deep etching.

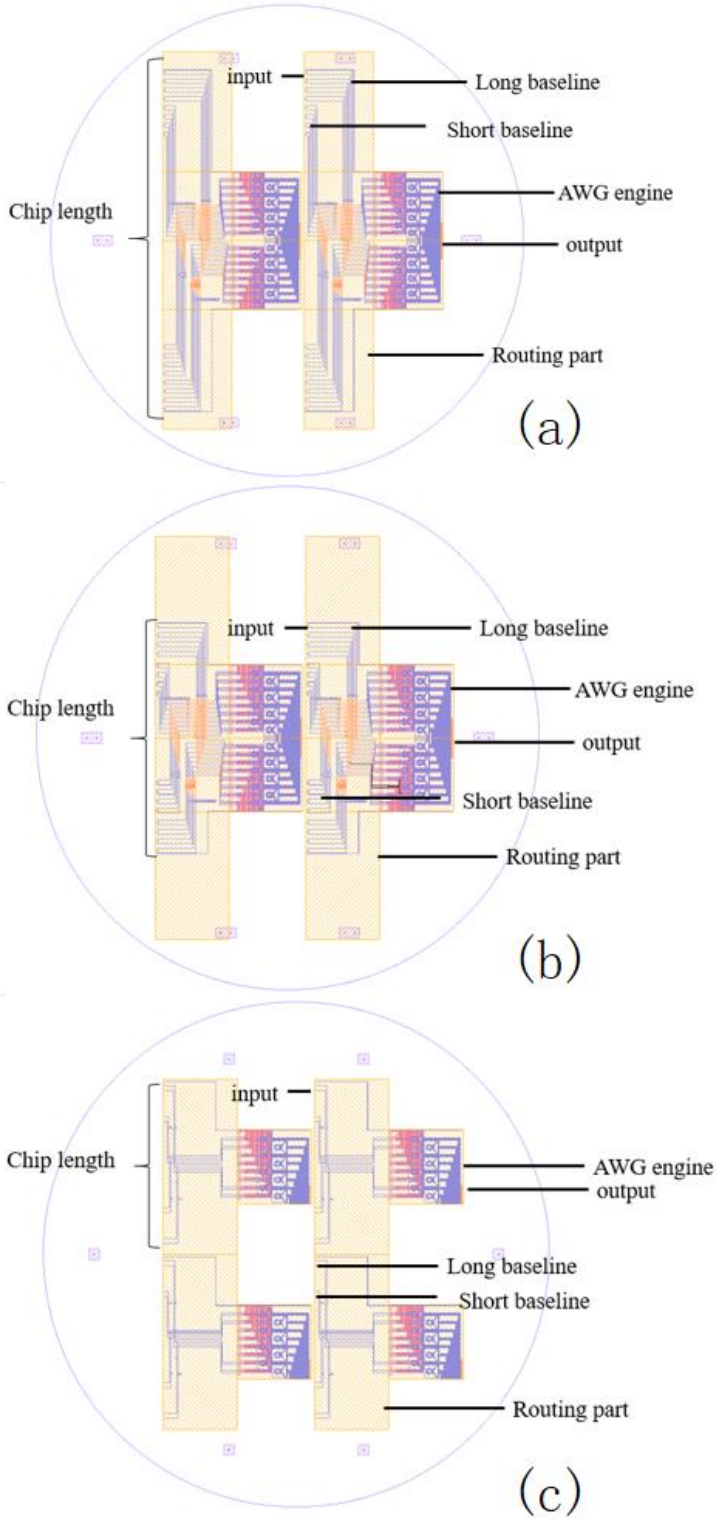


Figure 65 Layout of the SuperPIC PICs. (a) PICA, (b) PICB and (c) PICC. The blue circles show the size and location of 6-inch wafers. Yellow boxes show the size and location of the dies. Purple boxes around the edge of the dies are alignment marks region.

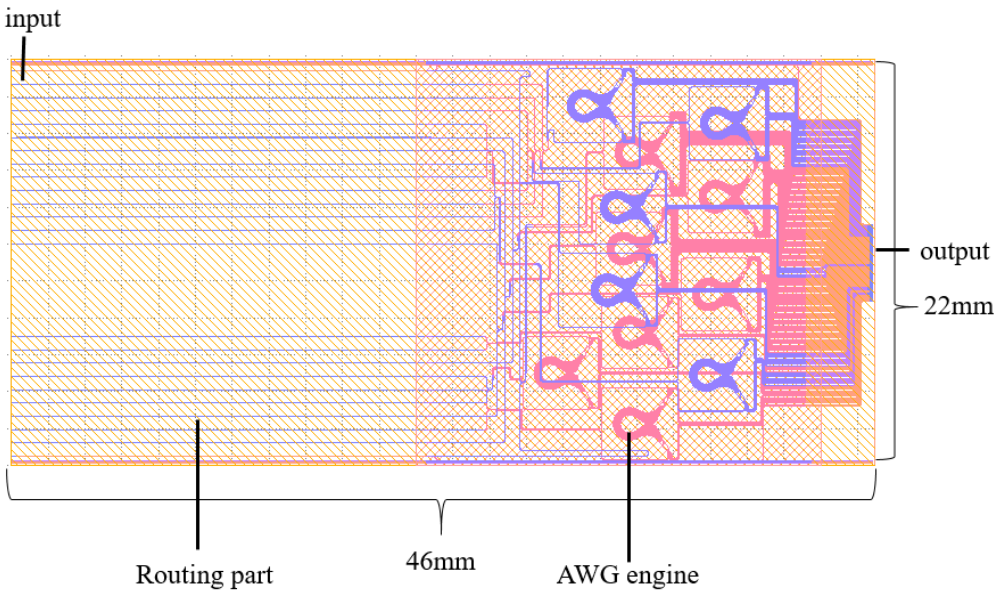


Figure 66 Layout of the PICD.

Table 3 The designed parameters and testing results of the fabricated 1×2 MMIs.

Waveguide width (μm)	3	3.5	4	4.5	5	5.5	6
Loss/cross (dB)	0.2	0.2	0.03	0.05	0.05	0.07	0.12

Figure 65 shows the layout of the SuperPIC PICA, B, and C presented in a six-inch wafer. The number of dies a six-inch wafer can accommodate for PICA, B, and C are 2, 2, and 4, respectively. The AWG engine designs for PICA, B, and C are the same (except for PICC, which has only half of the AWG engine) for minimizing the mask cost. The purple boxes around the edge contain alignment marks for inter-layer alignment. There are three pairs of alignment marks in layer 1 and 3 pairs of alignment marks in layer 3. Although only one pair of alignment marks is required for alignment, we place many alignment marks on different layers as backups since the wafer bowing, expansion, and edge damages sometimes impair the accuracy of alignment. We also placed vernier rulers, shown in Figure 67 (a), at the edges between two adjacent tiles.

Figure 66 shows the layout of the PICD. The design goal of the PICD is to extend the size of the first generation of the SPIDER chip so that all the PICs have similar chip lengths. The PICD layout is split into three tiles, including one tile for input extending and another tile for output routing. The AWG engine for PICD has a similar design compared to the 1st generation SPIDER PICs.

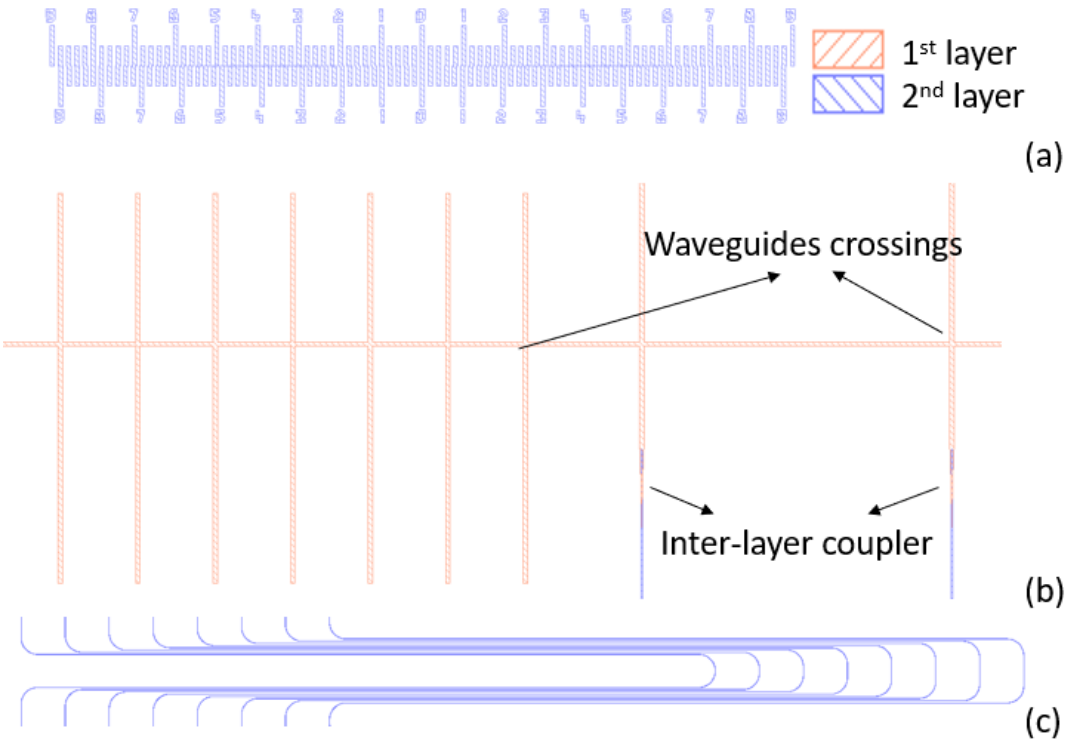


Figure 67 Layout of the Super PICs PICA at the bottom set. (a) Vernier ruler for alignment between tiles. (b) Waveguide crossings and inter-layer couplers. (c) Waveguides for path length matching.

Figure 68 (a) shows the experimental setup diagram for SuperPIC PICs measurement, which is the same as the measurement setup for 1st generation SPIDER PICs except all the stages and holders are large enough to measure dies with up to 110mm×44mm size at the fundamental TE mode. Figure 68 (b) shows the transmission spectrum from one optical input of a baseline at 15 different output channels calibrated to a reference waveguide at the bottom set. The measurement

results show the demultiplexing capability of the AWGs and waveguide continuity at the edges of the tiles. Figure 69 shows the measured transmission spectrum of the PICB, C, and D at the bottom and the top sides, respectively. The measurement results show that our SuperPIC PICs can collect and process the light for interferometric imaging. The chip characterization is finished by me and Yujia Zhang.

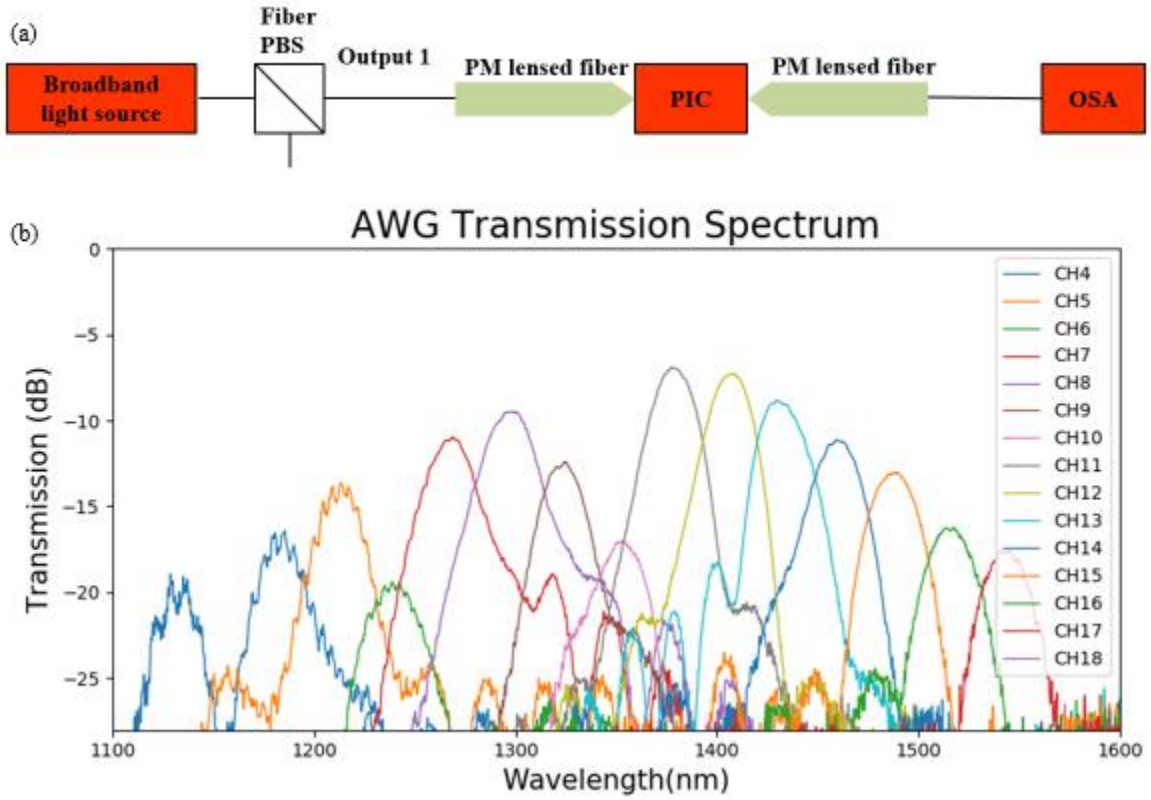


Figure 68 (a)Diagram of the PICs measurement setup. (b)Measured waveguide crossing loss on 50nm Si_3N_4 layers. (c) Measure waveguide propagation loss on 150nm Si3N4 layers. (d)Measured 3.3THz AWG transmission spectrum.

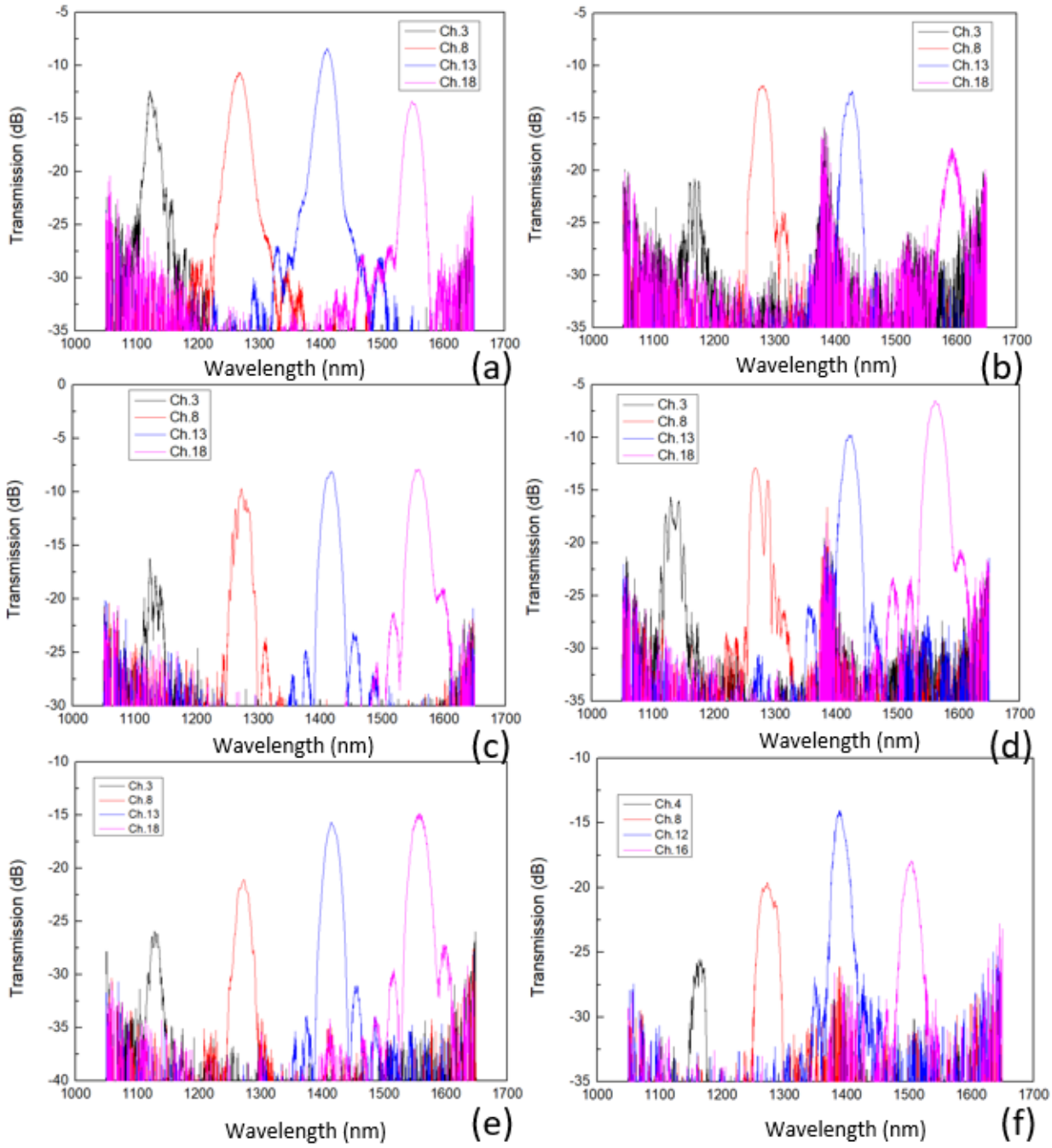


Figure 69 Transmission spectrum of the SuperPIC PICs (a) PICB bottom set, (b) PICB top set, (c) PICC bottom set, (d) PICC top set, (e) PICD bottom set and (f) PICD top set.

Future work includes (1) the fringes measurement using the high-resolution SPIDER imager and (b) high-resolution imaging experiments.

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Chapter 5 Surface-coupled SPIDER Imager

5.1 1st version of the surface coupler

This chapter presents the 1st and 2nd version of the surface coupled based on 45o mirrors. Furthermore, we present a surface-coupled SPIDER imager based on a broadband surface coupler, including the device design, simulation, fabrication, and characterization.

Our SPIDER imaging PICs in Chapter 5 use edge coupling, in which the optical inputs are limited to almost only one dimension. As a result, 2D imaging requires multiple PICs or rotating a single PIC. Using a surface coupler, we can arrange all the optical inputs in a 2D domain and achieve real-time imaging using a single PIC, significantly increasing the systematic simplicity and flexibility. Traditional surface couplers [126] based on gratings have a less than 100nm 3-dB bandwidth around 1550nm wavelengths. They are sensitive to light polarization, which sets a limitation on the performance of our imager.

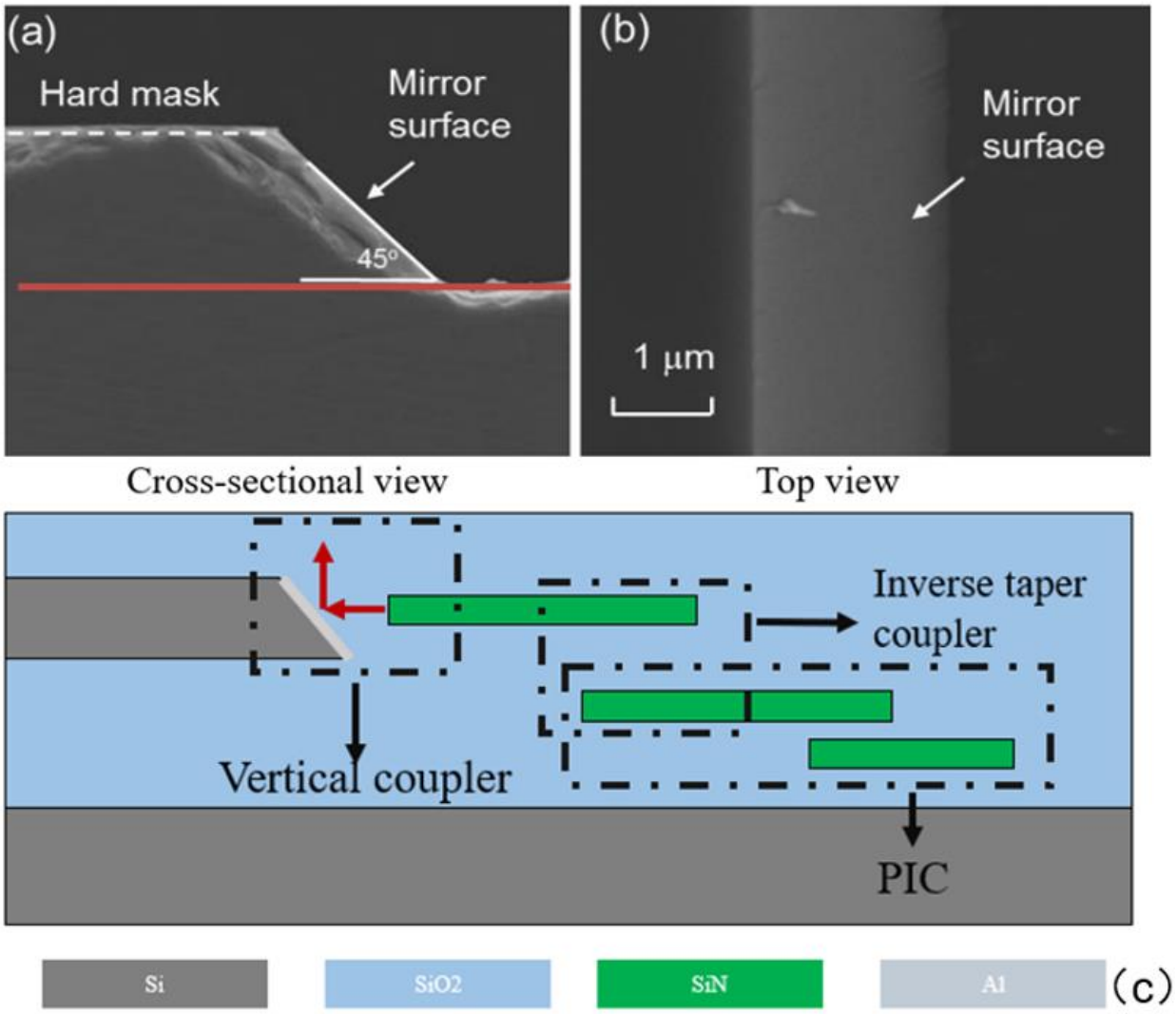

Figure 70 Diagram of the surface coupler based on a 45° mirror. The surface coupler is fabricated on (a)Side view of silicon 45° wet etching. (b) Top view of silicon 45° wet etching. (c) Diagram of the surface coupler based on a 45° mirror. The surface coupler is fabricated on top of a PIC. Light transmits in and out through the surface coupler and is coupled into the PIC by the inverse taper coupler.

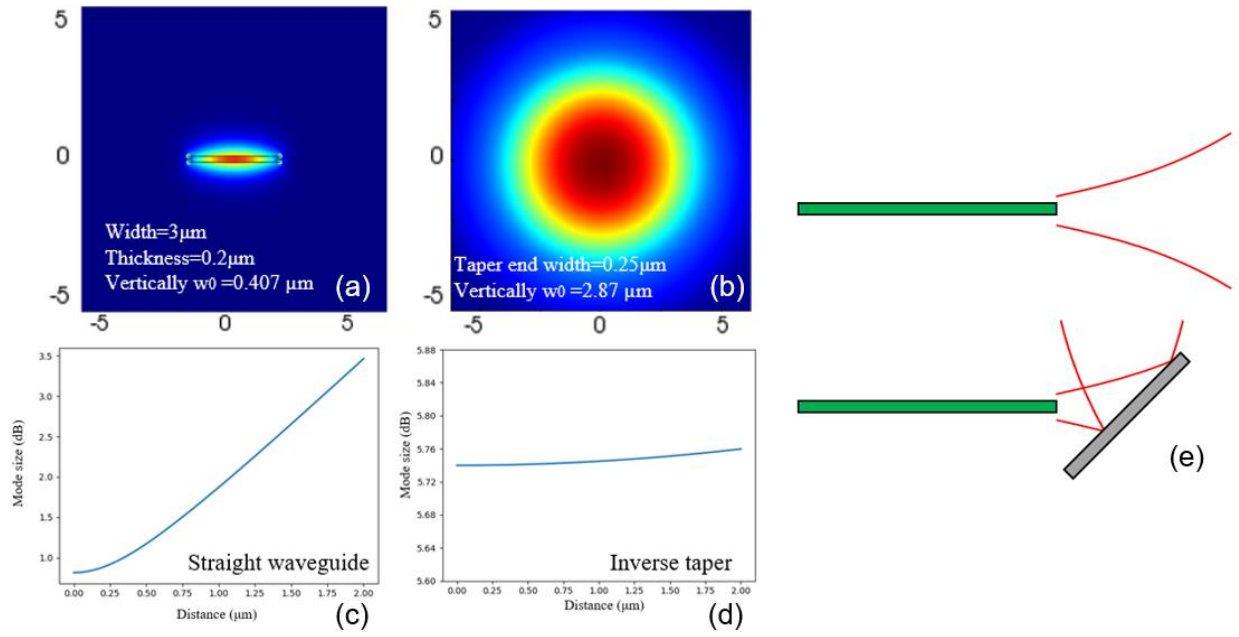

Figure 71 (a) Mode profile of a silicon nitride waveguide without taper. (b) Mode profile of a silicon nitride waveguide with taper. (c) and (d) Output mode size in vertical direction with the variation of the distance. (d) Diagram of the surface coupler with the silicon nitride waveguide.

In this section, we present a broadband, polarization-independent, and high-efficiency surface coupler for optical signal coupling, imaging, and detection[108]. The surface coupler is based on a 45^o mirror fabricated by anisotropic etching of single crystallized silicon, as shown in Figure 70 (a) and (b). The mirror structure in Figure 70 (a) and (b) are fabricated by Yu Zhang. Figure 70 (c) shows the diagram of the surface coupler. In our surface coupler based on the 45^o mirror, we use a thin layer of metal deposited on top of the silicon 45^o slope to achieve the light reflection. Optical signal coupled between the surface coupler and the PIC through inversed taper couplers. Traditionally, the surface coupling on PICs is achieved using grating couplers. Table 4 shows the comparison between the grating coupler and the 45^o mirror. The optical signal is transmitted through the surface coupler through reflections, so it is less sensitive to wavelength and polarization compared to the grating coupler. Besides, the grating couplers have difficulties in coupling the light vertically to the top, which limits large-scale 2D packaging, while our

mirror is guaranteed to be 45^{o} limited by the single crystallized Si crystal structure. We designed the surface coupler using the 45^{o} mirror for the following applications:

- SPIDER imager
- High density 2D packaging (fiber-to-chip, VCSEL)
- Vertical surface coupling
- High bandwidth connection
- Broadband detection
- Dual-polarization connection and detection
- Chip-to-photodetector coupling

The fabrication process of the surface coupler is shown in Figure 72. The silicon layer on a silicon-on-insulator (SOI) wafer is bonded onto a wafer with photonic devices for thin film transfer. The surface coupler is then fabricated on the top silicon layer. The mirror size of the surface coupler is mainly decided by the silicon thickness on the bonded SOI wafers. With the increasing of the silicon thickness, the reflectance and efficiency of the surface coupler also increase, as a cost of fabrication difficulty and coupling loss at the inversed taper coupler. As a proof-of-concept demonstration, we designed the photomask in Figure 73 (a) and (c) to fabricate a surface coupler using a 500nm Si device layer, as shown in Figure 73 (b). Our hard masks for wet etching are designed to be many rectangular structures, so after silicon anisotropic wet etching, we will get silicon blocks with four 45^{o} side walls. The waveguides with 200nm thickness are placed next to the mirror to enhance the reflectance. We deposited aluminum on the slope that faces the waveguide using E-beam evaporation and lift-off.

Figure 71 (a) shows the mode profile of a Si_3N_4 waveguide. The mode is confined by the waveguide during transmission and will expand after it transmit out of the end of the waveguide, as presented by Figure 71 (e). Figure 71 (b) shows a simulated mode profile when we use an inverse taper to expand the beam. We can observe that an inverse taper makes the mode to be round and match better to a SMF-28 waveguide than the waveguide mode. Besides, the mode expansion after the inverse taper is less significant than a straight, as shown in Figure 71 (c) and (d). However, a large mode size sets a requirement to the height of the mirror. Otherwise, part of the optical energy will not be reflected by the mirror and will result in an extra insertion loss.

Table 4 Comparison of the 45° mirror and the grating coupler.

Performance factors	45° mirror	Grating coupler
Bandwidth	Wide	Narrow (typically below 80nm)
Polarization dependence	Low	High
Coupling angle	Sensitive to mirror angle	Sensitive to design and fabrication
Structure	Simple 3D structure	Complex 2D structure
Fabrication sensitivity	High tolerance	Low tolerance

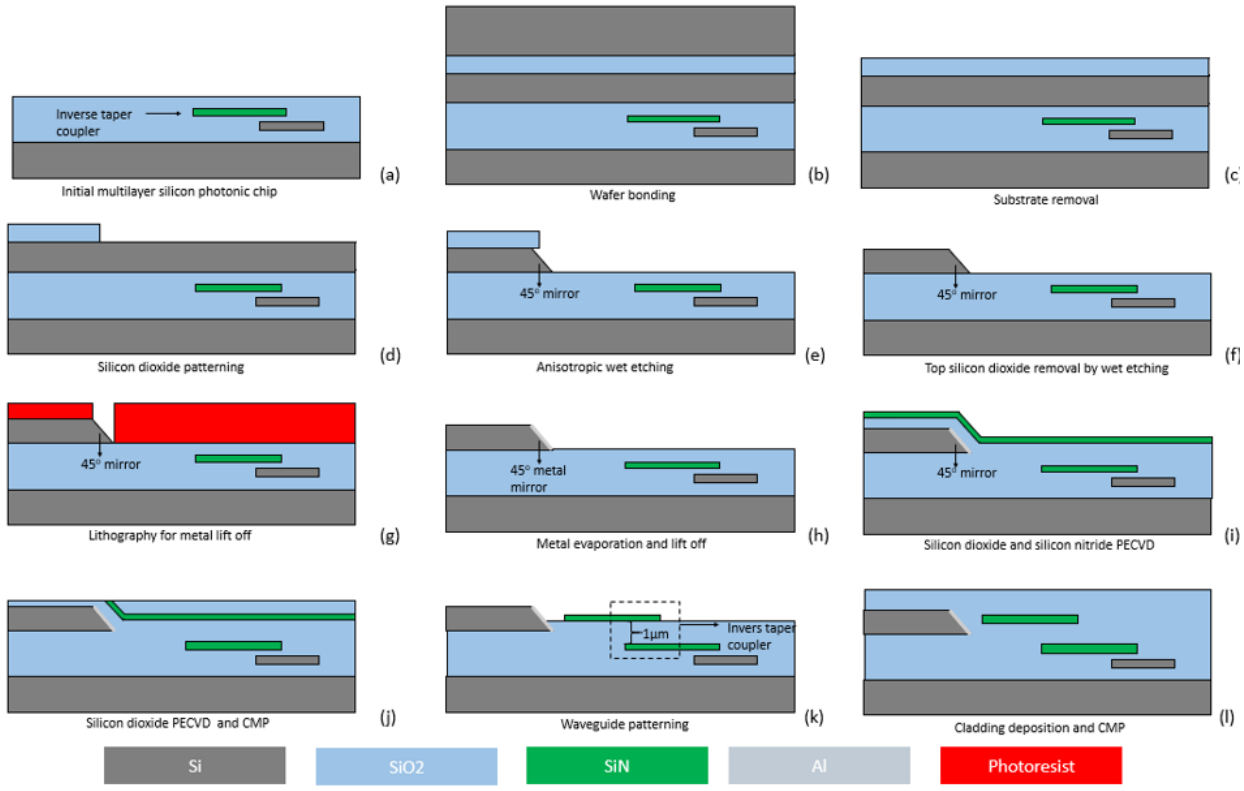

Figure 72 (a) Substrate silicon photonics integrated chip top surface planarization. (b) SOI wafer bonding. (c) Substrate removal by grinding. (d) silicon dioxide patterning. (e) 45° anisotropic wet etching. (f) Top silicon dioxide removal by wet etching. (g) Lithography for the metal mirror. (h) Metal evaporation and lift-off. (i) Silicon dioxide and silicon nitride PECVD. (j) Silicon dioxide PECVD and CMP. (k) Waveguide patterning. (l) Cladding deposition and CMP.

A SiO_2 hard mask is used for the Si anisotropic wet etching. The hard mask is patterned using lithography and etching and is designed to expose the 45°C side walls. The silicon wafer with patterned SiO_2 hard mask will be etched in 9% KOH solution at 70°C with 100ppm triton X-100 to form 4 45° slops. During etching, we use a pump to circulate the solution to make the etching more uniform. The measure Si etch rate is 56nm/min. Figure 74 (a) and (b) shows the SEM photos of the silicon block after the anisotropic etching. The remaining SiO_2 hard mask looks bright in the SEM photo since it is an isolator and is removed using an HF etching to expose the 45° sidewalls, and the Si block is partially buried under the hard mask. Figure 74 (c) and (d)

shows the SEM photo of the silicon block. The four slopes are around 500nm and will be a little bit shorter (by around 20nm) because of the overarching in the KOH solution. We perform an AFM measurement to verify the angle of the slops, an indicated in Figure 76 (a). The angle we measured is 44.4^{o} since the measurement is not perfectly perpendicular to the mirror. The silicon dioxide bottom cladding is measured to be 0.145nm, as shown in Figure 77 (b), which is smooth enough for our waveguide fabrication. Then, a thin layer (70nm) of Al is deposited on the mirror using lift-off. Figure 75 shows the SEM photo of the silicon block after the metal lift-off. The meal structure is designed to cover part of the top of the Si blocks to enlarge the fabrication tolerance and enhance the reflection. Figure 77 (a) shows the roughness of the Al measured by an AFM. Figure 76 (b) shows the AFM measurement of the Al mirror, which has a 44.6^{o} angle. The measurement result shows the metal evaporation is conformal and will not change the angle of the 45^{o} slope.

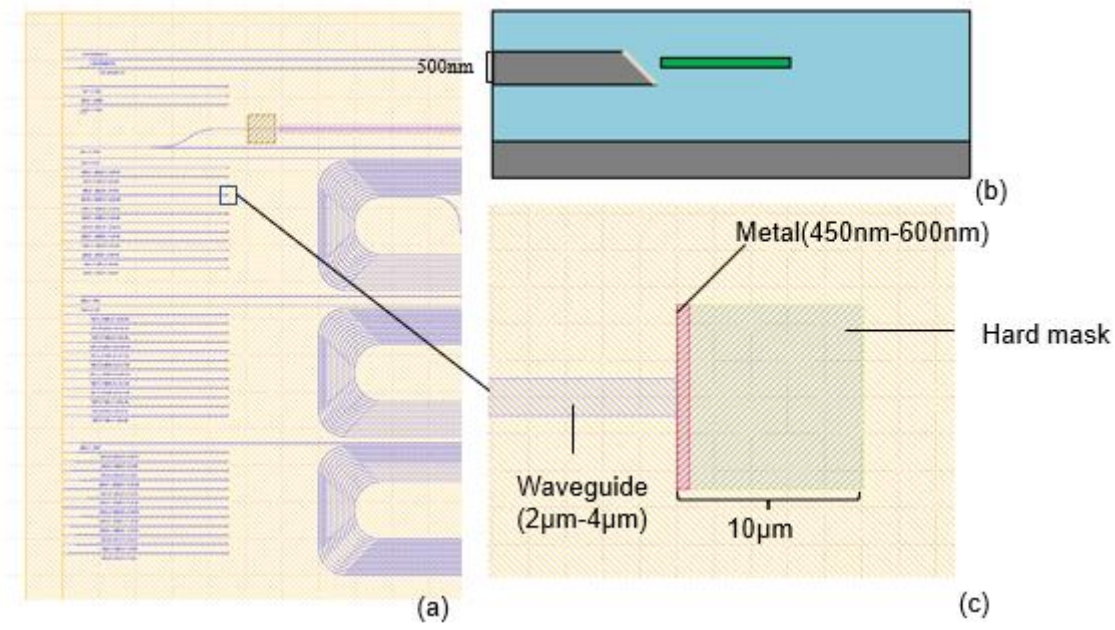

Figure 73 (a) and (c) Mask layout of a proof-of-concept demonstration of the surface coupler. (b) Diagram of the surface coupler proof-of-concept demonstration.

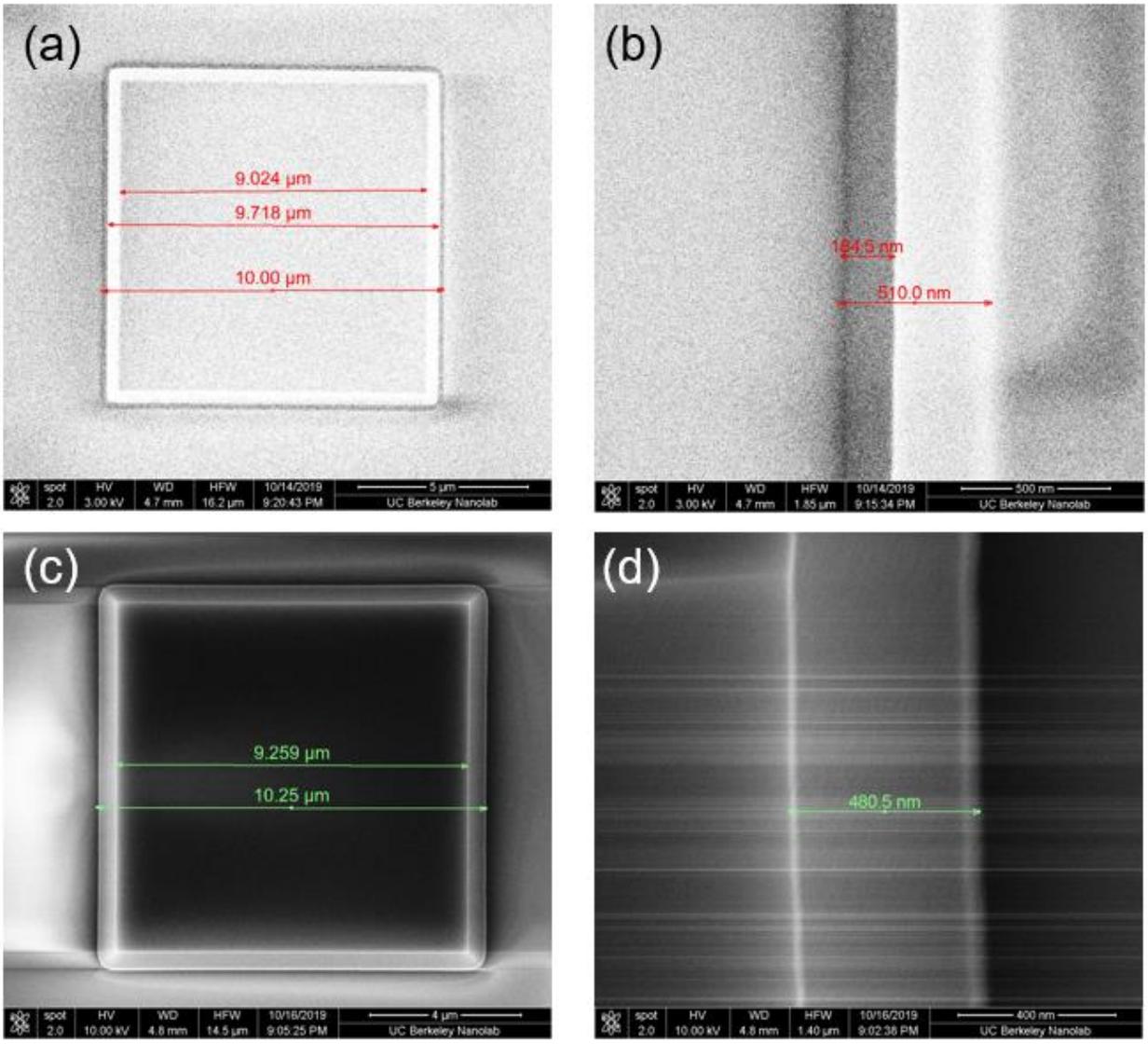

Figure 74 (a) and (b) SEM photos of the silicon block after Si anisotropic etching. (c) and (d) SEM photos of the silicon block after the hard mask removal.

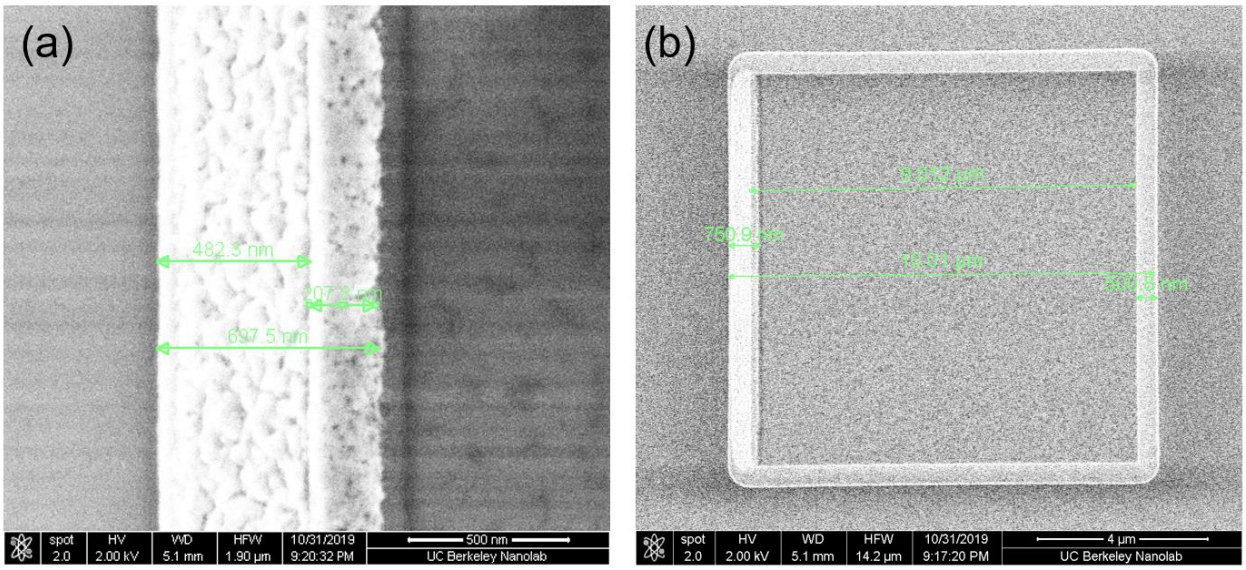

Figure 75 SEM photos of the silicon block after metal deposition. (a) A Zoom-in photo, and (b) A Zoom-out photo.

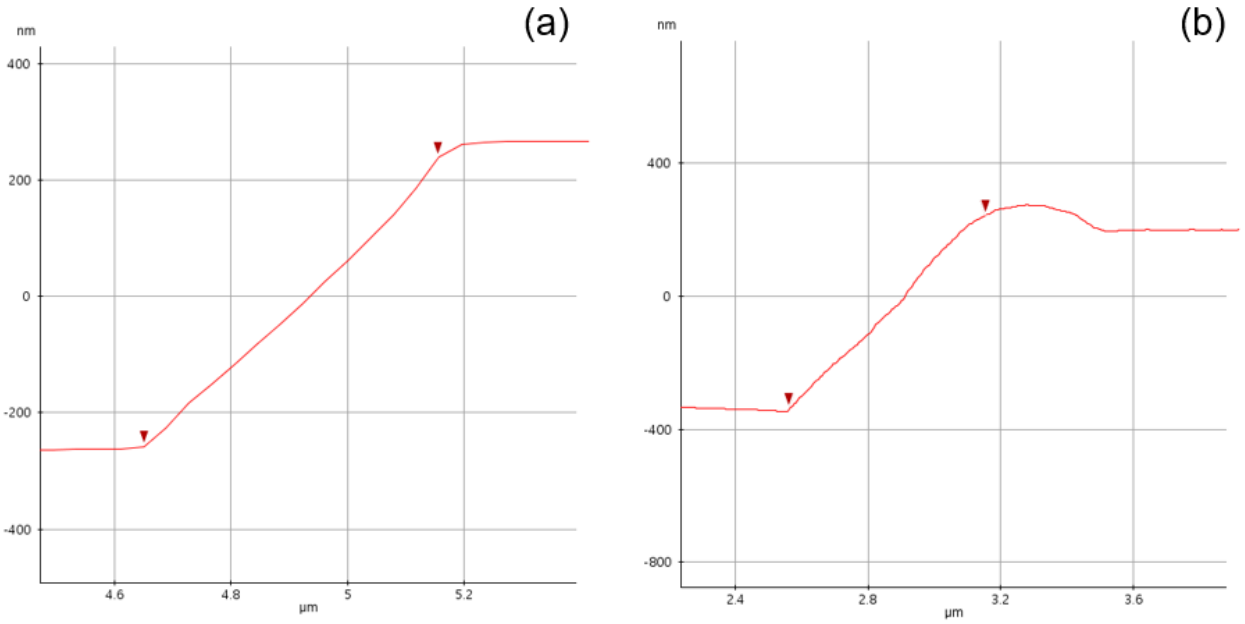

Figure 76 AFM photo of the 45° slope (a) after hard mask removal and (b) after deposition. The angles between the two cursors in (a) and (b) are 44.4 and 44.6 degrees, respectively.

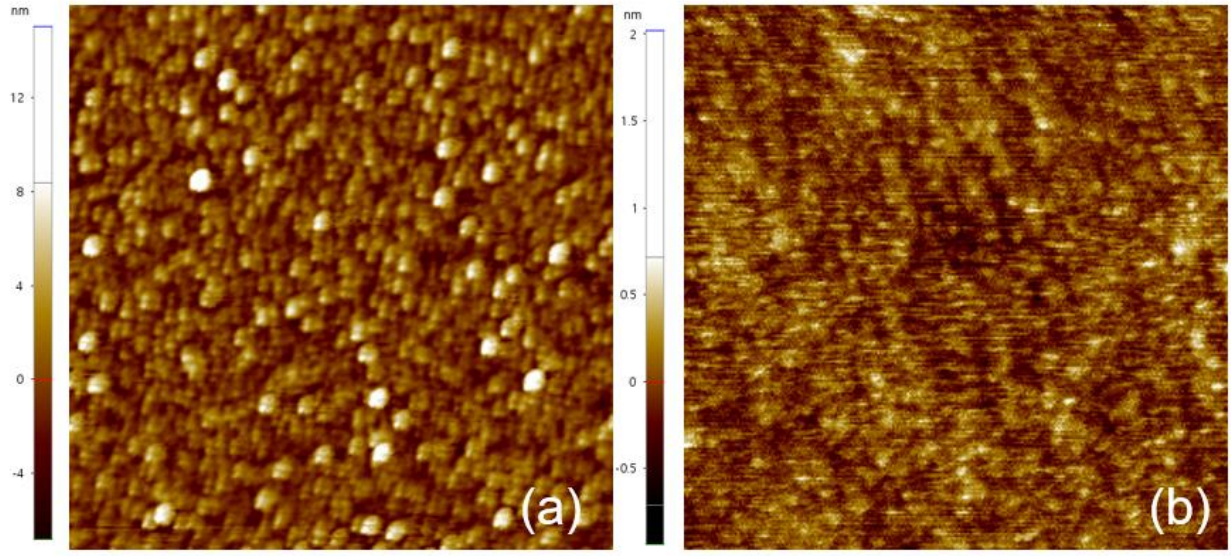

Figure 77 (a) AFM photos of the deposited Al, with 1.619nm surface roughness. (b) AFM photo of the SiO_2 bottom cladding after hard mask removal, with a 0.145nm surface roughness.

Since Al has an around 660°C melting point, it cannot stand the LPCVD Si_3N_4, which is deposited around 800°C. We used PECVD Si_3N_4 and SiO_2 as the cladding and core materials. The PECVD Si_3N_4 waveguide typically has a higher propagation loss compared to LPCVD Si_3N_4, so in our integration design, we use an additional Si_3N_4 layer for the surface coupler instead of integrating all devices into the surface coupler waveguide layer. We first deposited SiO_2 as the bottom cladding and then deposited the 200nm Si_3N_4 core layer. The SiO_2 layer thickness is optimized for making the Si_3N_4 waveguide to be the middle of the mirror. The Si_3N_4 layer is then patterned using lithography and dry etching. We optimized the photoresist coating process to make sure that our design is transferred to the Si_3N_4 layer accurately. Figure 78 (a) shows the zoom-in SEM photo of the Si_3N_4 waveguide after the dry etching. The metal mirror is embedded under the SiO_2 bottom cladding, and the end of the waveguide touches the slope by 175.9nm for two reasons: 1. The metal we deposited is larger than what we designed because the E-beam evaporation is not ideally perpendicular to the Si wafer. We designed a 600nm width metal

mirror and got 697.5nm checked by SEM. 2. The SiO_2 bottom cladding deposition will enlarge the slope. The measured slope is 634.8nm, while the Si bock has a 480.5nm slop. We designed waveguide arrays with 4μm pitch to further investigate the density limitation of the surface coupler, and our fabrication result shown in Figure 78 (b) indicate that our surface coupler can achieve a high density with a small footprint. We then deposited SiO_2 top cladding using PECVD and then flattened the top surface using CMP. We expose the edge of the waveguides using a DRIE process.

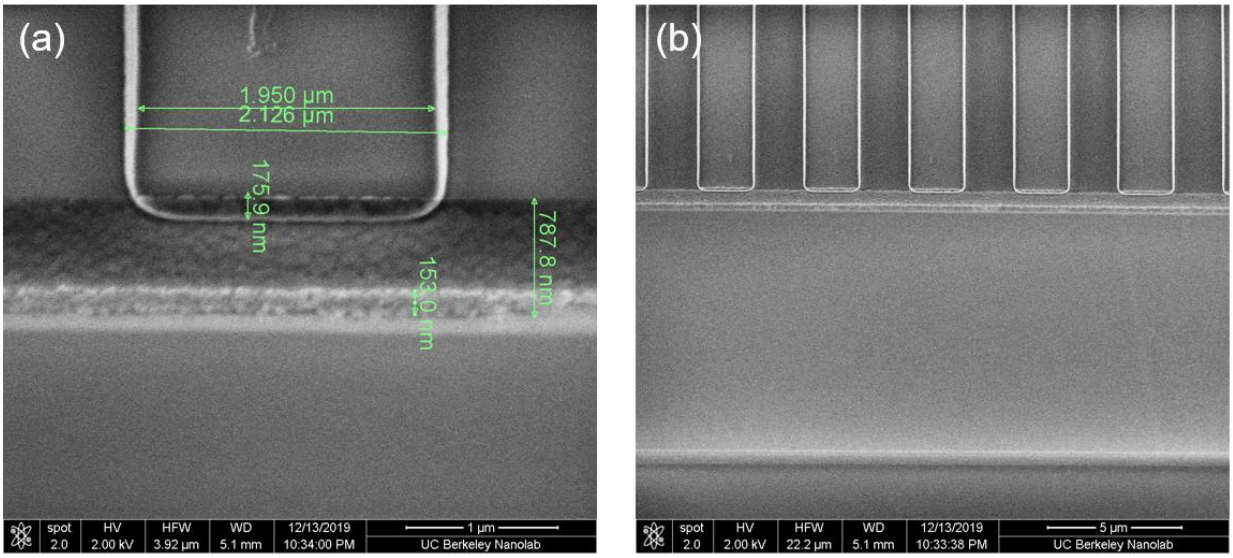

Figure 78 SEM photo of the silicon nitride waveguide at the mirror (a) zoom in and (b) zoom out.

Figure 80 (a) shows the simulated transmission of the surface coupler at the fundamental TE mode using the FDTD method. The transmission is measured above the SiO_2 top cladding. We measured the surface coupler using our homemade OVNA, with the measurement setup and the chip shown in Figure 79. The chip is first cleaned using Acetone, IPA, and DI water to expose a clean top surface. The input light is calibrated to fundamental TE mode and coupled into the chip using a lensed fiber (the coupling loss here is measured using a reference waveguide). We then used a lensed fiber with a 2.5μm beam waist to measure the output of the surface coupler from

the top of the chip. Figure 80 (b) shows the coupling loss of the surface coupler, which shows a 5.2dB coupling loss. We then measured waveguide arrays on the chip with 28 waveguides using one input and an MMI tree to equally split the power into 32 waveguides with 4μm pitch (4 waveguides on the two sides are used for calibration). Figure 80 (c) shows the photo of the waveguide array measured using an IR camera from the top of the chip. We observed one of the reflectors is dark and all the others can be observed. We estimate the dark reflector is damaged during fabrication, limited by our fabrication yield.

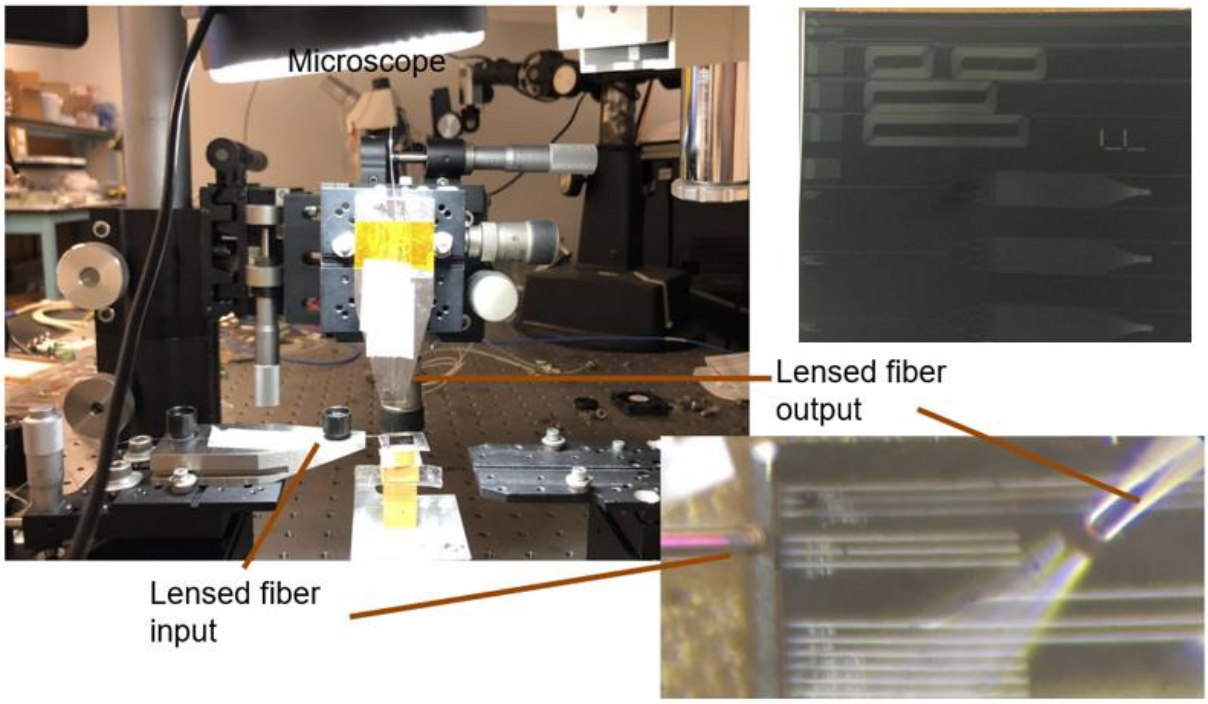

Figure 79 Measurement setup of the surface coupler. The photo of the chip is shown at the top right corner.

Traditional chip to SMF-28 fiber grating couplers can achieve a 2.64dB coupling loss with an around 67nm bandwidth [126]. Our 1st version of the surface coupler introduces a much higher coupling loss even to a lensed fiber. The advantage of our surface coupler is the large bandwidth,

as simulated in Figure 80 (a). The measured coupling loss is higher than the simulated loss of the mirror due to the mode mismatch. To further optimize the performance of the surface coupler, we need to improve our design and fabrication in the following aspects:

1. Enlarge the mirror size to enhance the reflection. Besides, a large mirror will also make the surface coupler more insensitive to polarization since the TM mode size in the Si_3N_4 waveguide is usually larger than the TE mode size.
2. Using a spot size converter (such as an inversed taper structure) to expand the input/output beam to match well with standard single-mode optical fibers. The large spot size must fit the size of the mirror to avoid large loss during reflection.
3. Improve the mirror smoothness by optimizing the Si anisotropic wet etching recipe.
4. Improve the mirror smoothness by optimizing the metal deposition and post-annealing recipe.

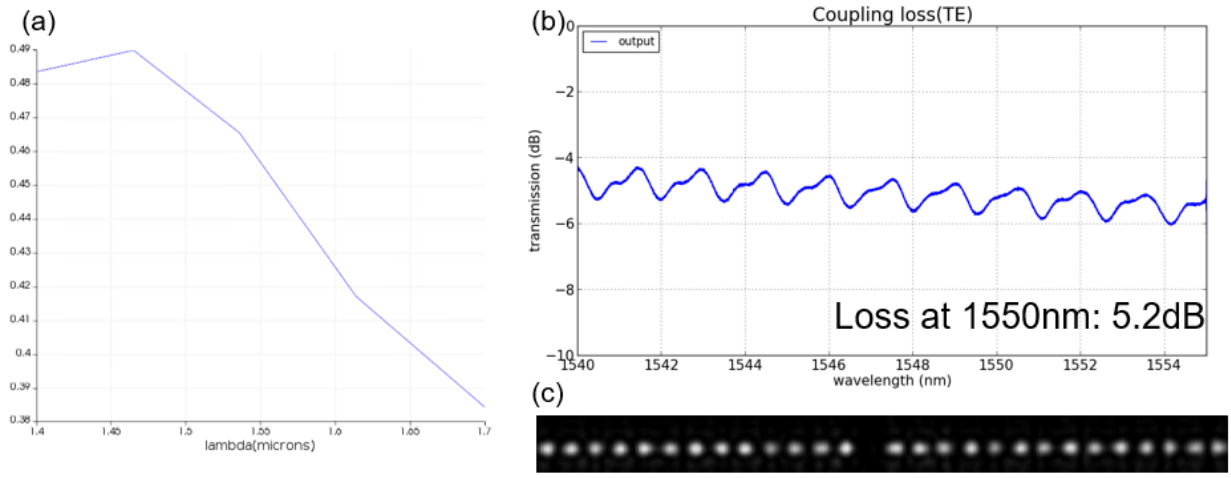

Figure 80 (a) Simulated transmission of the surface coupler. (b) measured coupling loss of the surface coupler to a lensed fiber. (c) Photo of the reflector arrays.

5.2 2nd version of the surface coupler.

Our progress on the surface coupler using a 1st version of the surface coupler shows excellent potential for a broadband and polarization-insensitive surface coupler. To further improve the performance of the surface coupler, we propose a 2nd version of the surface coupler with the diagram shown in Figure 81, using a pyramid air void inside the SiO_2 cladding. In this diagram, the Si block is removed after the deposition of the top cladding using an anisotropic etching method and forming a 45° mirror at the SiO_2/air interface. Considering the critical angle of the SiO_2/air interface is 44°, the light from the waveguide will be reflected to the top surface by total internal reflection, considering the light propagates along the x direction. The silicon nitride waveguide uses a taper structure to increase the beam size and decrease the numerical aperture of the surface coupler to fit an SMF-28 fiber. Compared to the 1st version of the surface coupler, the 2nd avoids the metal mirror so that the roughness from metal deposition is avoided. Besides, the absence of metal allows us to use high-temperature processes such as annealing at 1050°C, dry/wet oxidation, HTO deposition, and LPCVD Si_3N_4 deposition without considering the metal melting and diffusion.

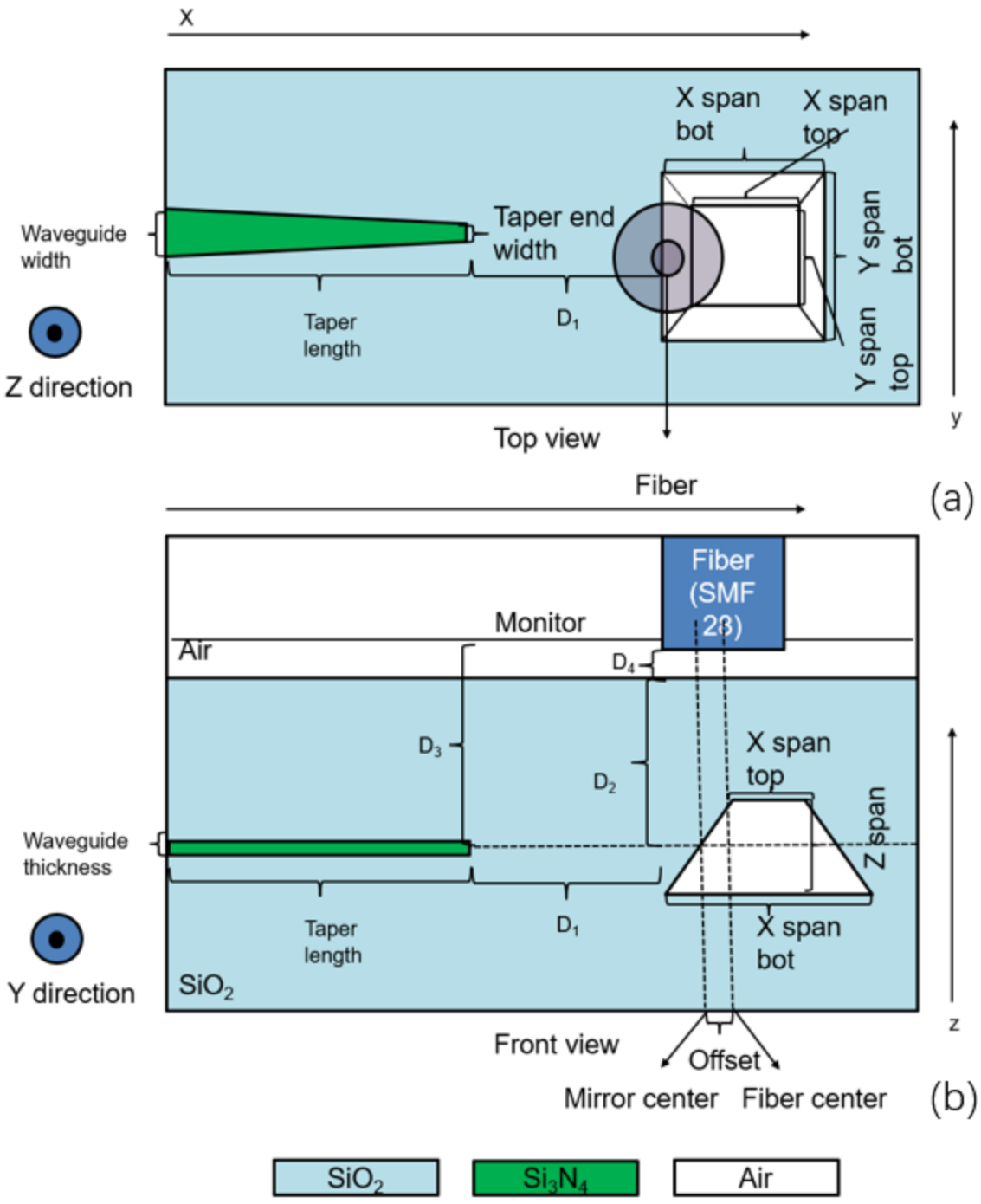

Figure 81 Modal of the 45-degree mirror simulation. (a) To view and (b) front view, respectively. Light comes from the left side in the silicon nitride waveguide, which is transmitted and expanded through a tapered waveguide and is reflected by a 45-degree mirror.

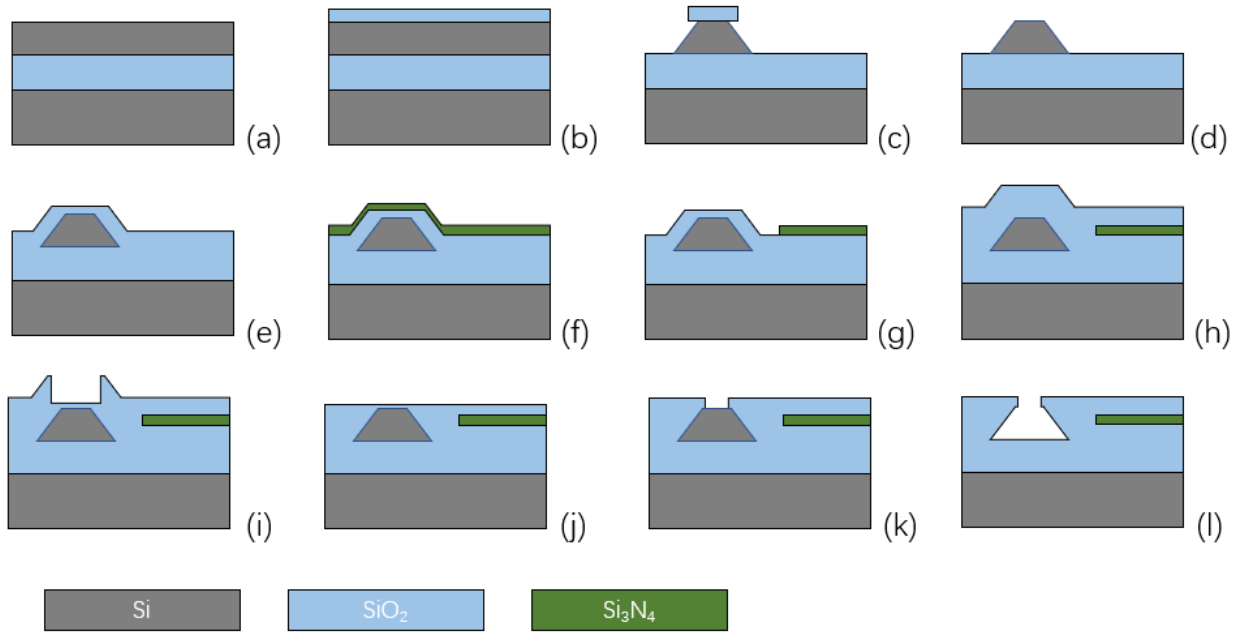

Figure 82 Fabrication process of the surface coupler. (a) SOI wafer cleaning. (b) SiO2 hard mask deposition. (c) 45-degree anisotropic wet etching. (d) SiO2 hard mask removal using BOE wet etching. (e) SiO2 bottom cladding deposition. (f) Si3N4 deposition. (g) Si3N4 waveguide patterning using lithography and dry etching. (h) SiO2 top cladding deposition. (i) Inverse etching for CMP. (j) CMP. ((k) Silicon dioxide window opening using lithography and dry etching. (l) XeF_2 etching.

Figure **82** shows the fabrication process of the 2nd version of the surface coupler. The fabrication process starts with a SOI wafer cleaning. The SiO_2 hard mask is then deposited on top of the wafer using LPCVD and then patterned by lithography and etching. The SiO_2 hard mask after patterning is composed of many rectangles and every rectangle will define a Si pyramid after the Si anisotropic wet etching. The silicon layer is etched using the 45^o anisotropic wet etching (in Chapter 3) to form pyramid structures, followed by hard mask removal. We deposited SiO_2 as the bottom cladding and Si_3N_4 as the waveguide core using LPCVD. The deposition is carefully controlled so that the Si_3N_4 waveguide is located at the center of the mirror. After the waveguide

patterning, we deposit the SiO_2 top cladding and flatten the top surface using CMP. We etch through the top cladding into the Si pyramid after the top surface flattening using lithography and dry etching.

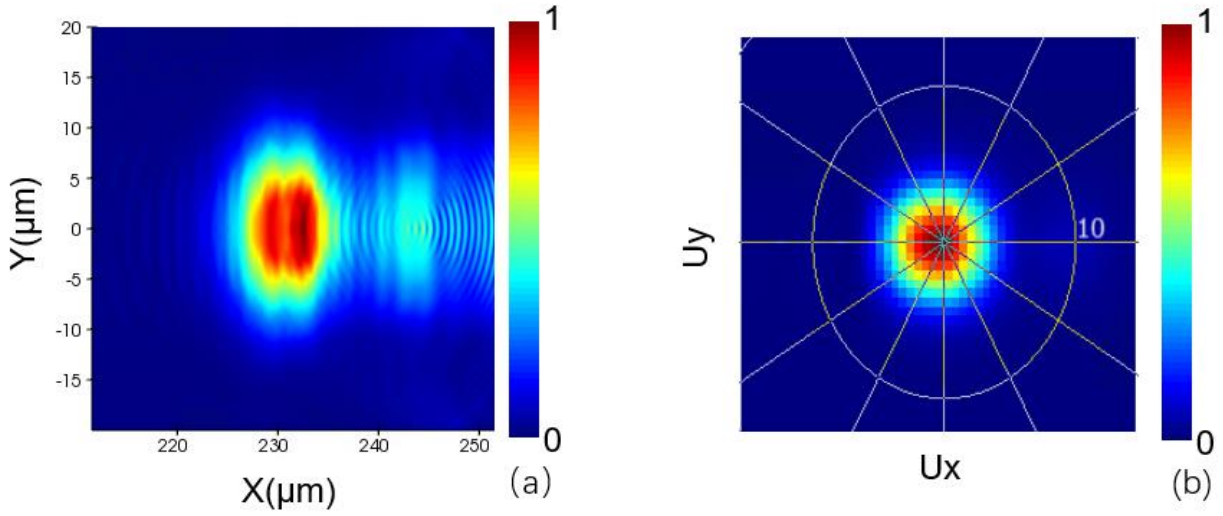

Figure 83 Simulated mode profile inside the fiber input (top view). (a) near field and (b) far-field.

At last, the Si pyramid is removed using an isotropic XeF_2 etching 135[128]. The critical step in the coupler fabrication is the waveguide lithography since the photoresist spin coating is non-uniform when a high block exists. Our photo-resistant coating includes a 60nm BARC followed by a 430nm UV210-0.3 to fabricate our 250nm Si_3N_4 taper tip. In our lithography test, our fabrication process cannot lead to a high yield over the whole 6-inch wafer with a large size Si block. One method is to minimize the size of the Si blocks in the x and y direction while it is large enough to reflect light, and so the Si block we design becomes a pyramid structure. We also optimized the photoresist spin coating process to further improve the yield.

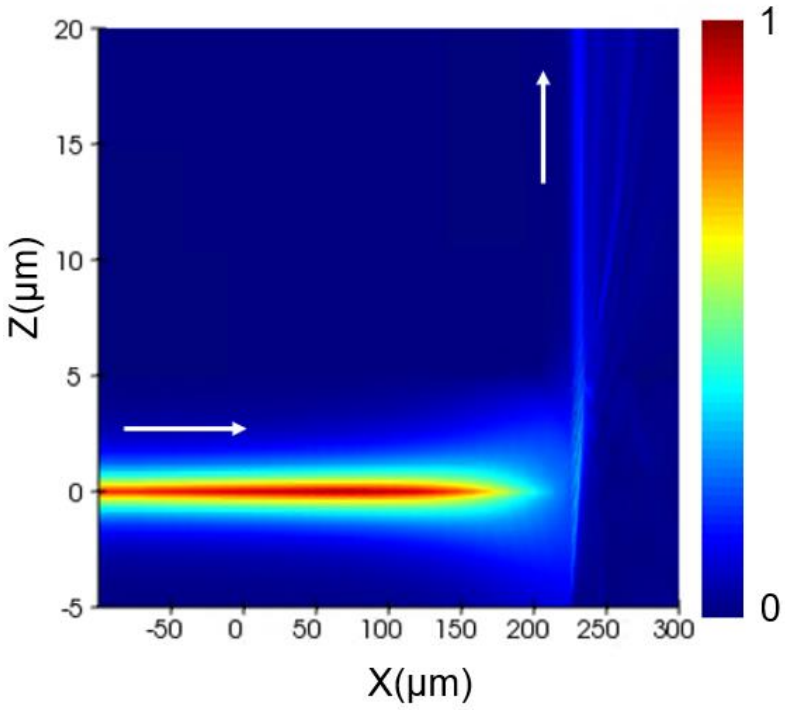

Figure 84 Simulated mode profile inside the fiber input (cross-section view). White error denotes the beam transmission direction.

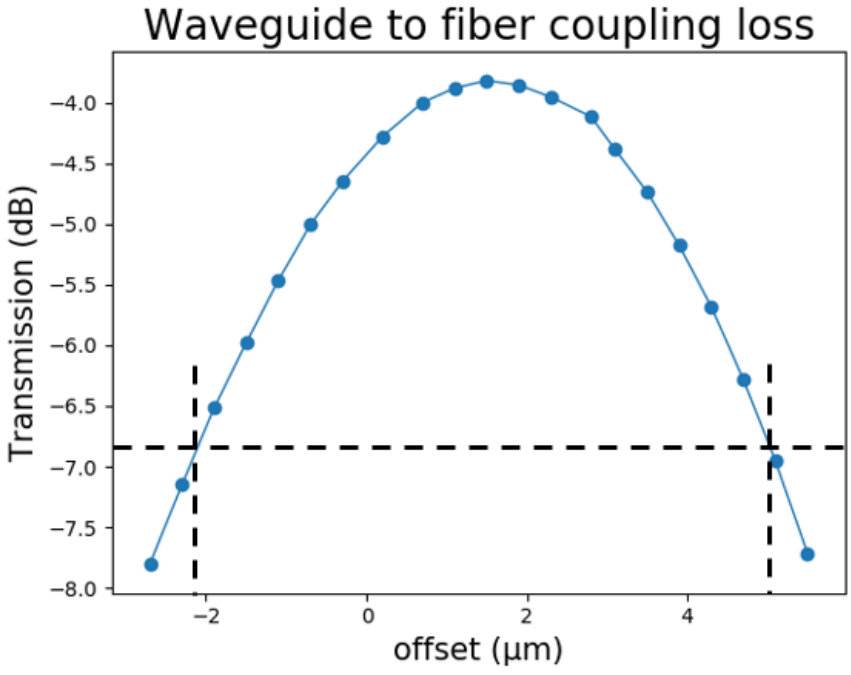

Figure 85 Simulated transmission from the waveguide to the fiber versus variable offset at x direction using the following parameters: D1=5μm, D2=5μm, and D4=0μm. Z span

is 10μm, and the waveguide thickness is 50nm. The taper end width is 250nm. The taper length is 100μm. The highest transmission is -3.82dB. The 3dB tolerance is around 7μm.

To further optimize our design, we simulated the waveguide to fiber coupling loss at the fundamental TE mode in our surface coupler using the FDTD method, as shown in Figure 85. The simulation result shows a 3.82dB minimum coupling loss when we use a 10μm Z span and 50nm waveguide thickness. We assume the fiber matches the position of the waveguide in the y direction during simulation. The loss comes from the mode mismatch between the expanded waveguide mode and the mode distortion after reflection. Figure 83 shows the simulated mode profile inside the fiber input from the top, and Figure 84 shows the simulated beam transmission along the waveguide and the mirror. We can observe that most of the energy transmits to the top while a small proportion of the light goes along the mirror (45^o to the top). When the optical signal transmits after the end of the Si_3N_4 taper, the NA becomes lower than the waveguide mode while it still expands during transmitting. As a result, part of the optical signal will not be reflected and will be refracted to the right side of the mirror. According to Fresnel equations, the incident angle will be almost 45^o, so part of the light will appear on the right side of the main mode [129]. The simulation result in Figure **85** shows a good fitting between the waveguide mode and the fiber mode after the reflection at the SiO_2/air mirror and has the potential to achieve a broadband and polarization-independent surface coupler. Our first demonstration uses 50nm waveguide core thickness to minimize the coupling loss at the fundamental TE mode.

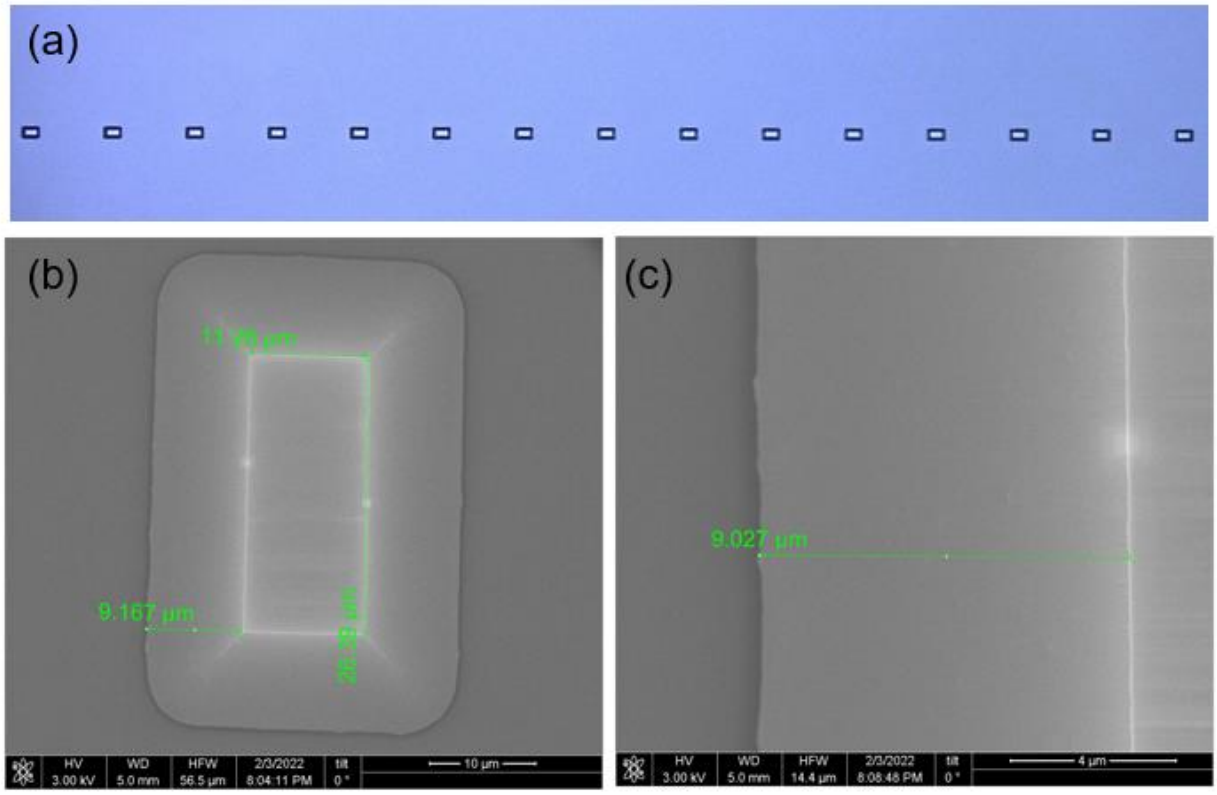

Figure 86 (a) Microscope photo of the Si pyramid blocks. (b) and (c) SEM photos of the Si pyramid blocks.

We start the fabrication from a SOI wafer with a 10µm Si device layer and 1µm buried oxide using the fabrication process presented in Figure 82. The SOI wafer is cleaned and then covered with an HTO hard mask. Then, the hard mask is patterned using lithography and etching. We used the same KOH etching recipe as the 1st generation surface coupler with an extended time duration to fully etch 10µm of Si. The remaining hard mask is then removed using an HF etching. Figure 86 (b) and (c) show the SEM photos of the Si after the hard mask removal. We can observe that the mirror after etching is smooth and shorter than the Si block thickness induced by over-etching from the bottom of the 45^{o} slope. Over-etching on the Si blocks will decrease the mirror width since more of the slop at the bottom will be etched. We placed many Si pyramid blocks with a 200µm period.

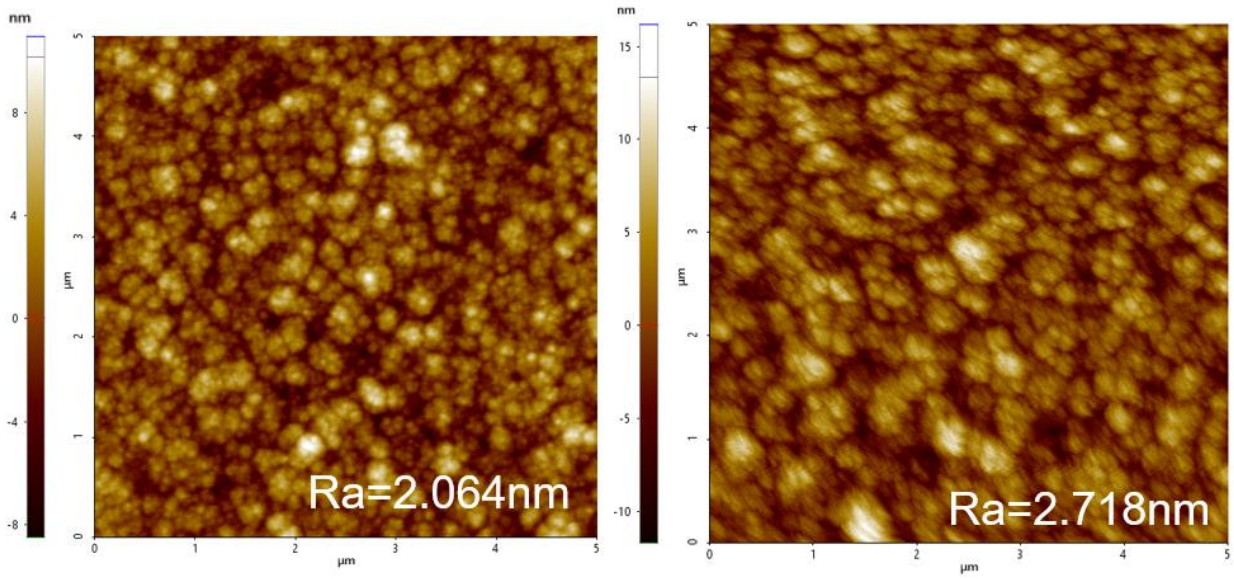

Figure 87 (a) AFM photos of a 5μm HTO. (b) AFM photo of a 5μm LTO.

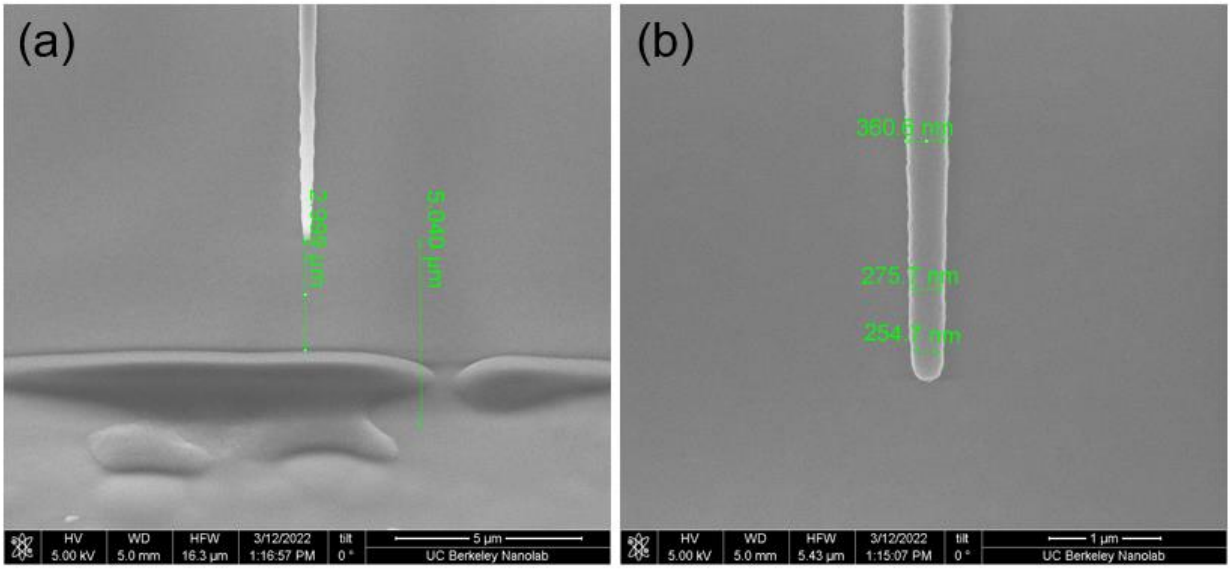

Figure 88 (a) and (b) SEM photo of the inversed taper after waveguide lithography.

After hard mask removal, we need to deposit 5μm of SiO_2 as the bottom cladding. Because we cannot do CMP inside the trench without damaging the Si block, we used HTO to minimize the surface roughness induced by the long-time deposition at the cost of deposition time. Figure 87 (a) and (b) show the AFM photos of the HTO and LTO after 5μm deposition. The measured

deposition rate is 228nm/hour and 750nm/hour, respectively. We then deposit a 50nm Si on top of the bottom cladding.

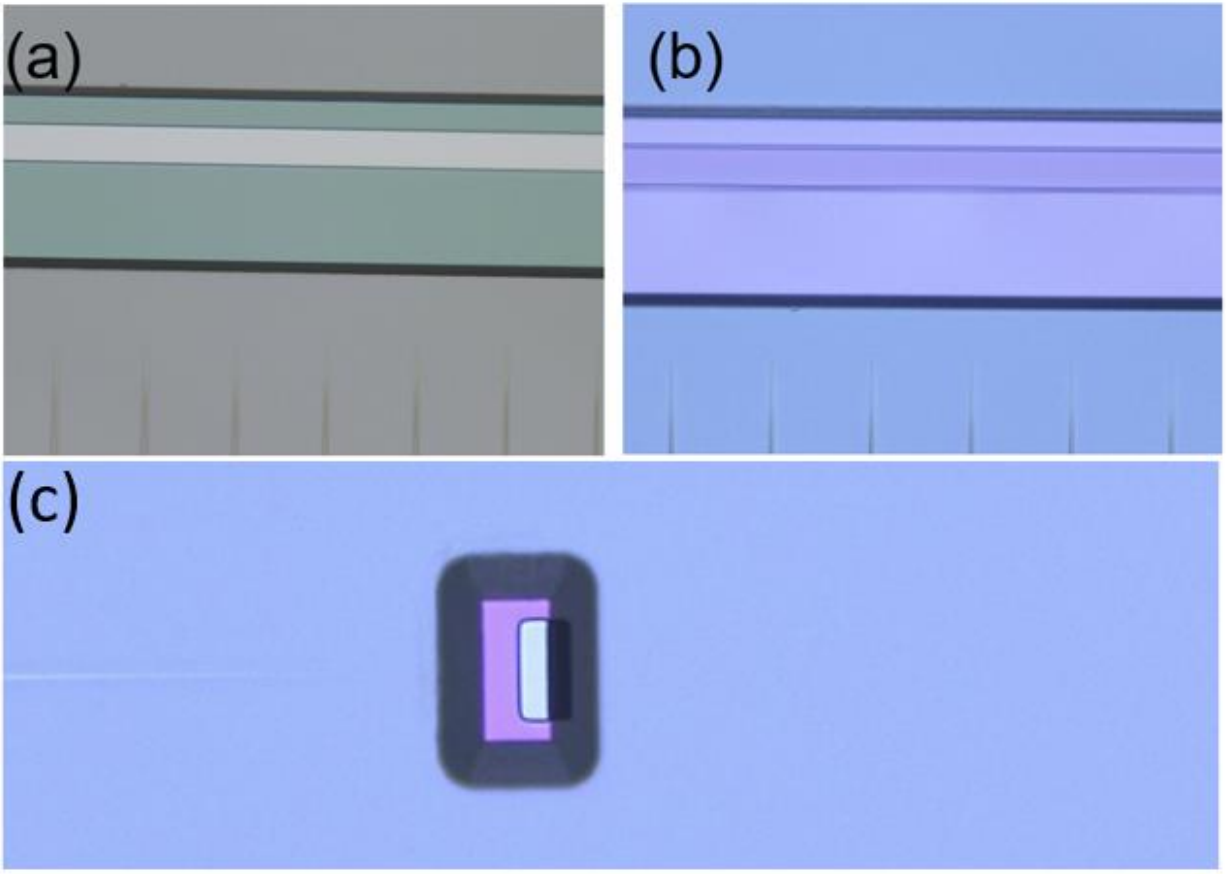

Figure 89 (a) Microscope photo before the Si removal. (b) Microscope photo after the Si removal. (c) Microscope photo of the pyramid voided with Si_3N_4 taper.

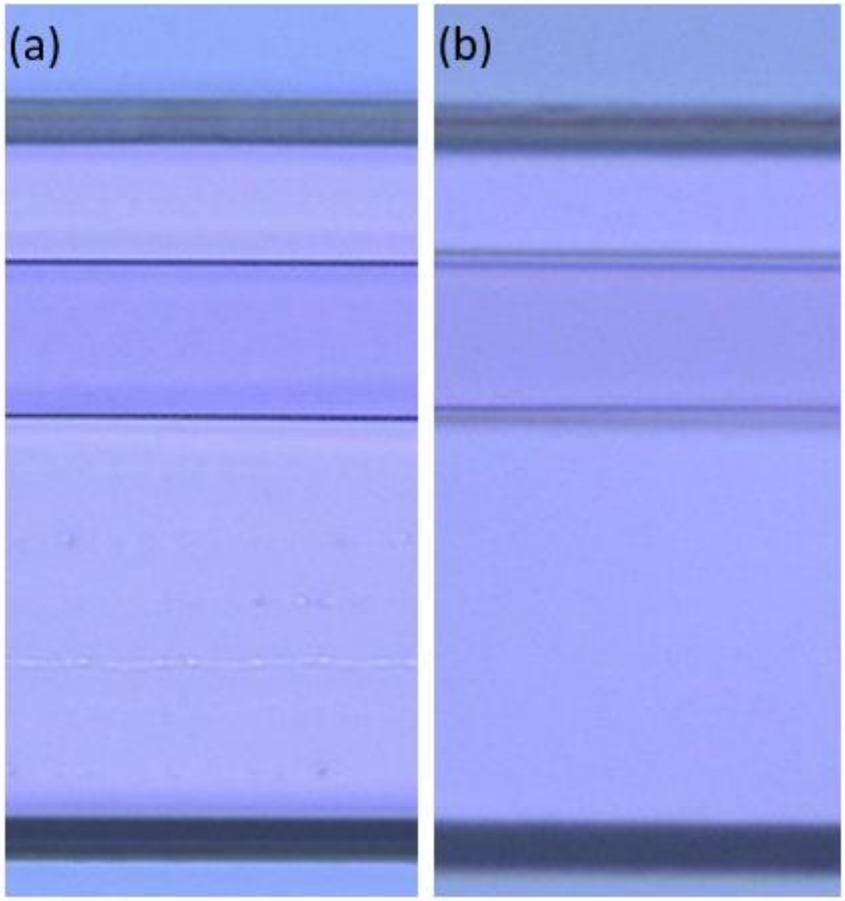

Figure 90 Microscope photo of the SiO_2 membrane (a) before HF cleaning and (b) after HF cleaning.

We optimize our photoresist spin coating process to expose inversed taper with the presence of the 10μm height Si block. We use a BARC coating with a 3750rpm spinning speed and a 430nm DUV photoresist. During coating, we apply an extra amount of photoresist to ensure all the valleys are covered. The nature of the photoresist spin coating makes the photoresist coating on the hills to be non-uniform. During exposure, we expose all the regions on and around the silicon block to remove all the Si_3N_4 on the Si pyramid blocks. Figure 88 shows the inversed taper after lithography. The end of the taper is designed to be 5μm away from the bottom of the SI blocks with a 250nm taper end width. The clear photoresist pattern shows our process can transfer our

pattern correctly to the Si_3N_4 layer. The top cladding is then deposited and flattened. Figure 89 (c) shows the waveguide with a Si pyramid after the top cladding polishing.

We then develop the Si removal process to form the mirror. Figure 89 (a) shows a microscope photo of a-Si block (green rectangle) under SiO2 cladding, with two 45^o slopes on the north and the south side. The rectangles on the Si blocks are a via that etch until the Si. We used a 30-minute XeF_2 etching followed by a 10s 10:1 49% HF dip to remove the Si and clean the SiO2 surface. Figure **90** shows the SiO_2 membrane before and after the HF dip. We can observe that HF cleaning removed most of the residue particles on the membrane. Figure 89 (b) shows the microscope after etching. The Si underneath is removed, and the SiO_2 membrane is formed on the top surface. The fabrication result shows the SiO_2 membrane can exist and support itself after the Si removal and form a mirror. Figure 89 (c) shows the photo of the fabricated surface coupler.

5.3 Surface-coupled SPIDER Imager

Our 2^{nd} version of the surface coupler shows great potential for broadband imaging. By combining the surface coupler with our SPIDER PIC, we can achieve a wafer-scale normal incident SPIDER imaging to achieve real-time imaging using a single wafer. In this section, we propose and demonstrate the integration of the SPIDER imager with the 2^{nd} version of the surface coupler.

We proposed the surface-coupled SPIDER imaging photonic integrated circuits (PICs) with the diagram shown in Figure 91. The new imaging PICs are composed of five silicon nitride layers and two metal layers using the layout shown in Figure 92 and the baseline configuration in 1^{st} generation SPIDER PIC. After the fabrication of the silicon nitride layers and the metal layers, we etch a through via the silicon block and remove the silicon using XeF2 dry etching to form air

to the silicon dioxide reflectance surface. As a proof-of-concept demonstration, we designed the surface-coupled SPIDER imager by changing the optical input of the 1st gen SPIDER PICs into the surface coupler, as shown in Figure **92**. Layer 1 includes only the waveguides and taper couplers at the surface coupler to avoid the high propagation loss due to the bottom cladding roughness. Layer 2 is a transition layer that transmit the incoming light to the upper layers. The optical circuit in the 1st gen SPIDER PICs are arranged into layer 3-5 in the surface-coupled SPIDER PICs.

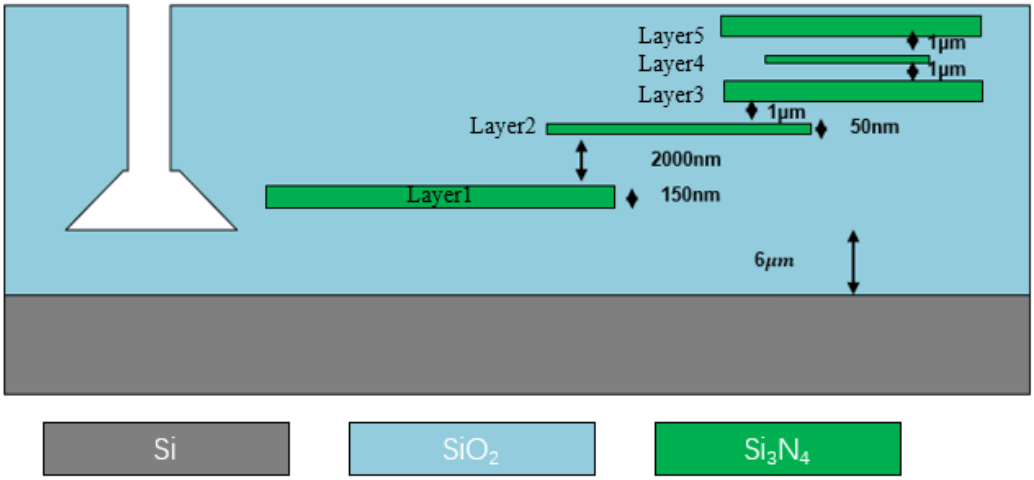

Figure 91. Diagram of the SPIDER imaging PICs using the surface coupler based on 45° mirrors.

Figure **94** presents the fabrication process of the surface-coupled SPIDER imager. Our fabrication started from a SOI wafer with 5.5μm thickness, and we fabricated the surface coupler first. We first fabricate the Si pyramids and the waveguides for the surface coupling. After the surface planarization in step 4, we fabricate another 4 layers using our multi-layer Si_3N_4 process. Two metal layers for thermal tunning are fabricated on the flattened top surface using a lift-off process. Then we perform a 10μm depth SiO_2 dry etching to expose the output waveguides and the Si pyramids at the same time. The final step is to release the Si pyramids using an XeF_2 dry etching.

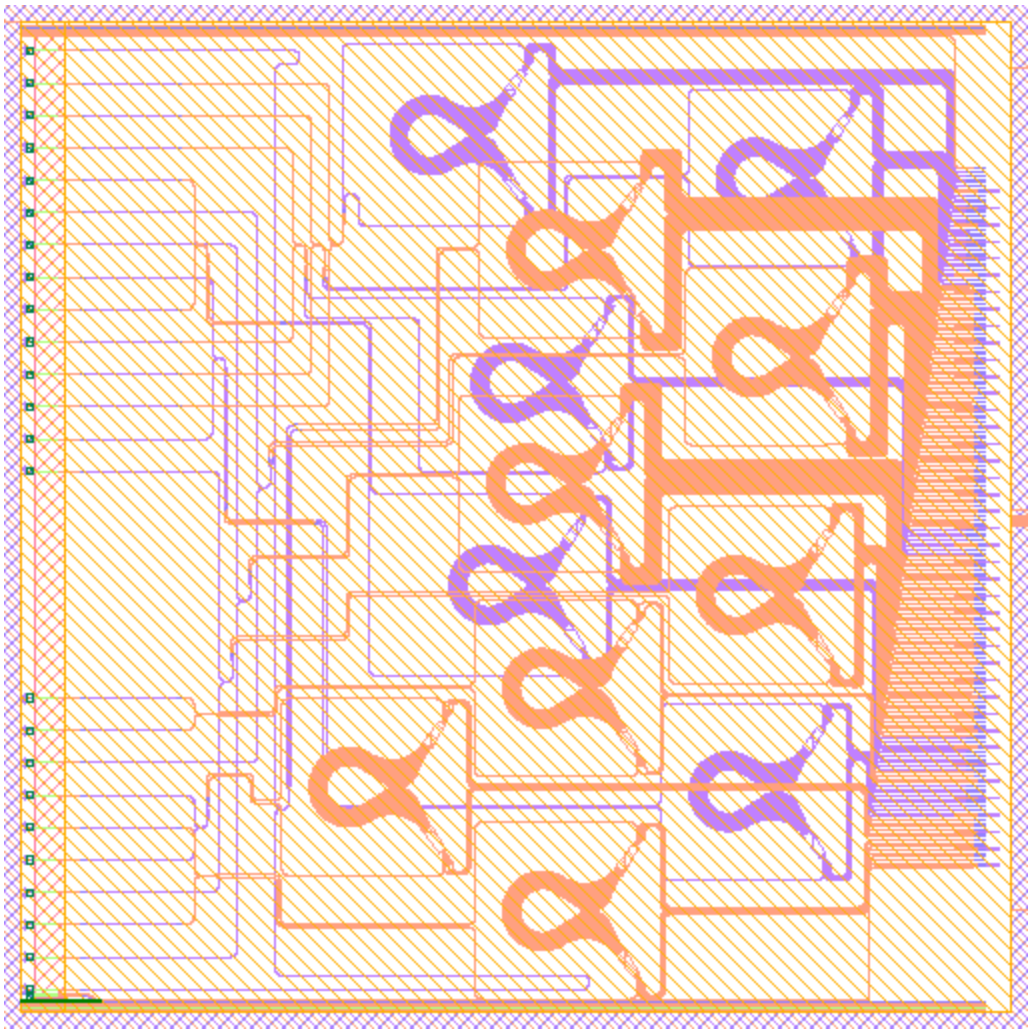

Figure 92. The layout of the PICs for interferometric imaging.

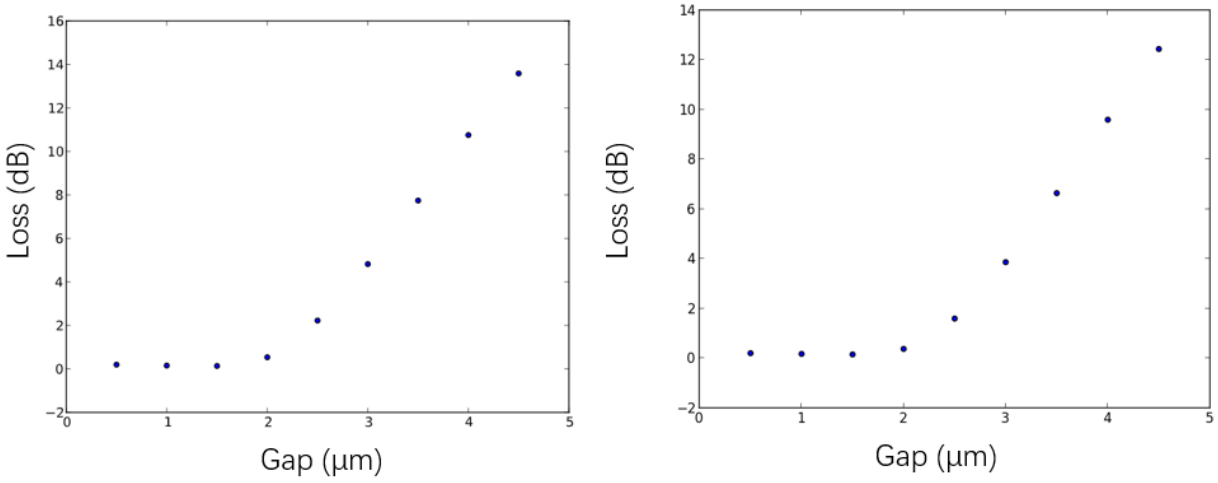

Figure 93. Simulated coupling loss of a pair of inter-layer couplers with (a) 300μm taper length and (b) 500μm taper length. The waveguides on the two layers have 150nm and 50nm thicknesses, respectively.

The coupling between the bottom two silicon nitride layers (layer 1 and layer 2) must overcome a 2-3μm silicon dioxide gap since the pyramid structures will occupy space and block the CMP during fabrication. The pyramid structures have a 5.5μm height as a trade-off between the fabrication difficulty and the device performance. A larger pyramid height can enhance the reflection at the 45-degree mirror and improve the beam size. However, a larger pyramid height will make it difficult to couple the light to another layer since the inverse taper coupler must work when the gap is higher than half of the pyramid height. For analyzing the behavior of the interlayer coupler at high gap thickness, we perform a simulation in Figure 93. The simulated results show that the coupling loss significantly rises when the gap is above 2μm, while the loss will be lower if a long taper is applied. Table 5 shows a more detailed simulation of the inter-layer coupling loss. The simulated results show that a less than 2.5μm gap is required for achieving less than 3dB loss. We chose a 500μm taper length for the inter-layer coupler as a trade-off between the footprint and the coupling loss. To further improve the inter-layer coupling, we design a fabrication process, as shown in Figure 95, to minimize the gap between layer 1 to layer 2. Considering our silicon block height is 5.5μm ±0.5μm, the planarized surface could have an around 3μm distance to the silicon nitride waveguide when the silicon block remains undamaged during CMP while taking the CMP non-uniformity into consideration. We patterned the silicon dioxide surface using lithography and an inductively coupled plasma (ICP) etching with an optimized etching step for low surface damage during etching. After an 800nm depth trench etching, the top surface inside the trench achieves a 1nm roughness on average, measured by an atomic force microscope (AFM). Then, we deposit a 50nm silicon nitride on top of the surface using Low-pressure chemical vapor deposition (LPCVD). We patterned the silicon

nitride layer using lithography and etching, while silicon nitride residue can present on the side walls of the trench, introducing a slight optical scattering. After the 2nd layer of silicon nitride patterning, we flatten the top surface using a second LTO deposition and CMP, and the top surface is then ready for the multi-layer silicon nitride platform fabrication. We successfully achieved a less than 2.5μm inter-layer gap using the process.

Table 5 Interlayer coupling loss from a pair of inverse taper couplers. The waveguides on the two layers have 150nm and 50nm thicknesses, respectively.

Gap/Taper length(μm)	300	400	500	600	700
2	1.20dB	0.76dB	0.67dB	0.46dB	0.19dB
2.25	2.58dB	1.93dB	1.32dB	1.12dB	0.81dB
2.5	4.36dB	3.55dB	2.71dB	2.38dB	1.98dB

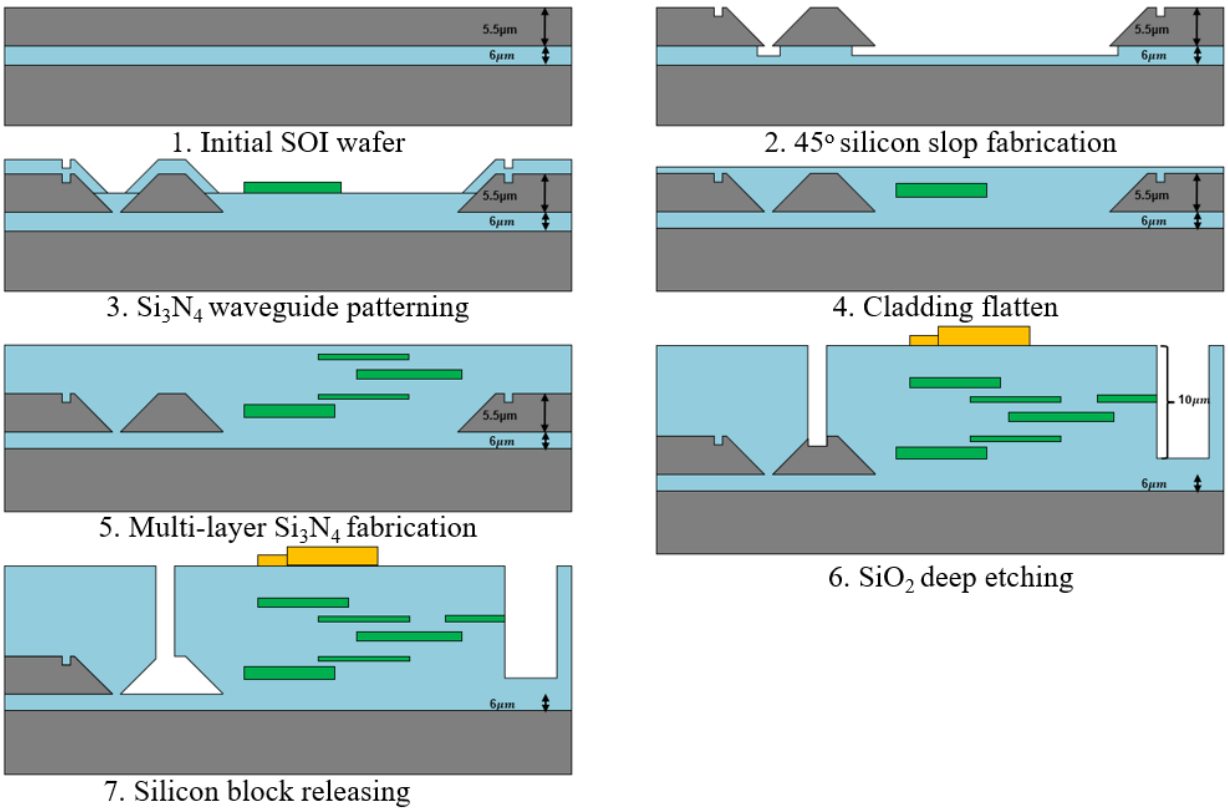

Figure 94. The fabrication process of the SPIDER imaging PICs using the surface coupler.

Figure 96 presents the microscope photos of the silicon blocks after the final surface CMP. Due to the non-uniform photoresist coating during the 1st Si_3N_4 layer fabrication, we observed some non-uniformity on top of the silicon blocks. The square around the silicon block is the edge of the trench mentioned in Figure 95. The two silicon nitride alignment marks are shown on the left side of the silicon block for guiding the lens. Figure 97 shows the overlapping of the two AWGs and routing waveguides. The multi-layer structure ensures that the waveguides on the two layers are isolated at the device region. Figure 98 shows the photo of the surface-coupled SPIDER imager.

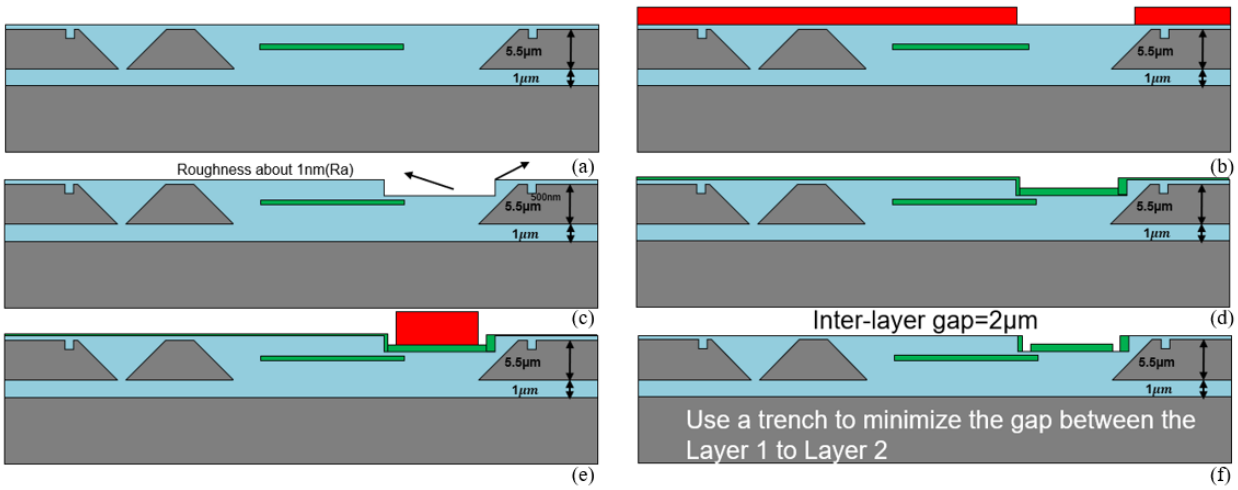

Figure 95. Fabrication process for the 2nd silicon nitride layer.

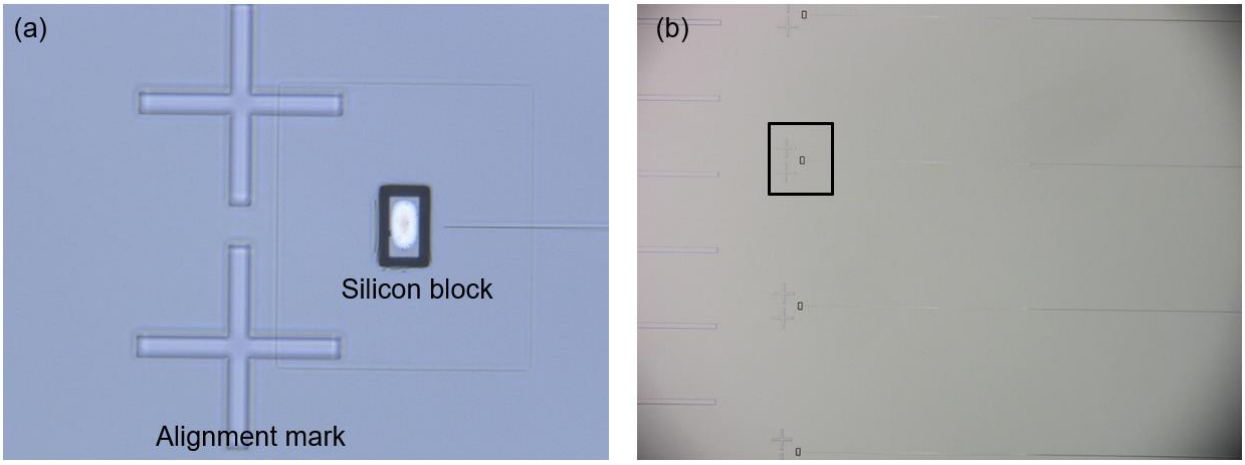

Figure 96. Microscope photo of the (a) Zoom in and (b) Zoom out photo of the silicon block with waveguides.

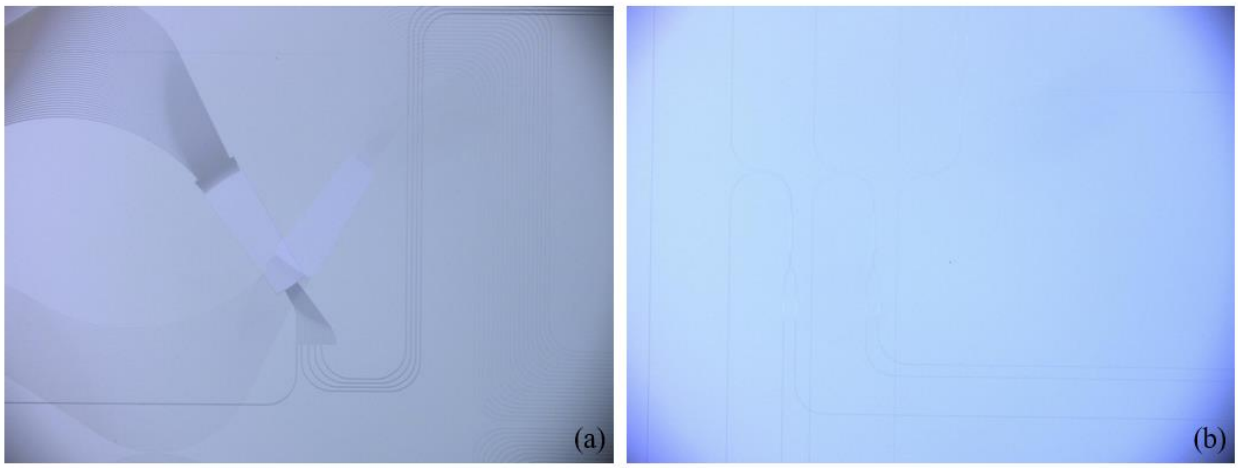

Figure 97. Microscope photo of the (a) AWGs and (b) routing regions.

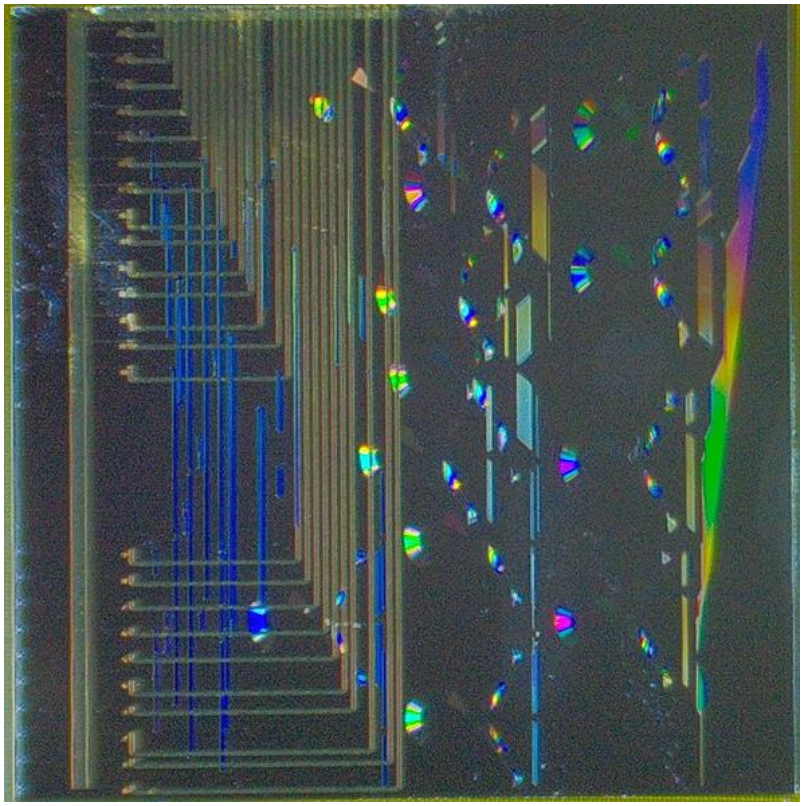

Figure 98. Photo of the SPIDER imager using a surface coupler.

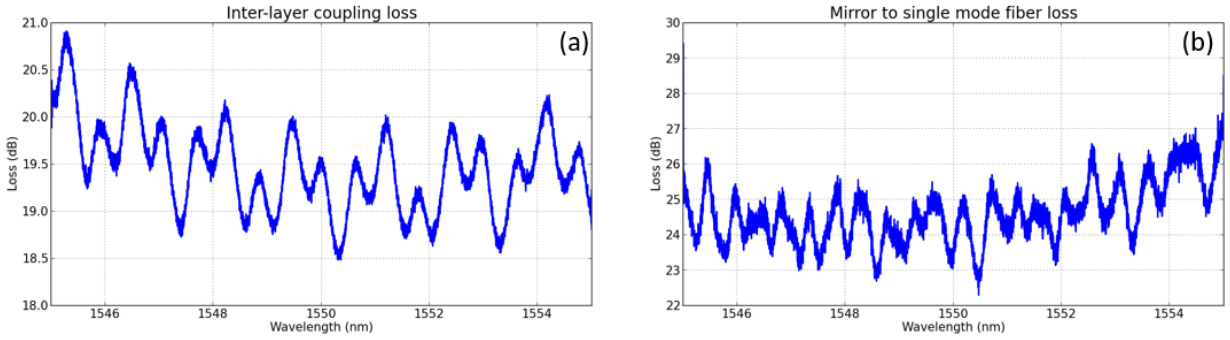

Figure 99. (a) Measured inter-layer coupling loss and (b) measured coupling loss of the surface coupler to a cleaved single-mode fiber.

We characterize the chip using our homemade OVNA system with an erbium-doped fiber amplifier (EDFA). The OVNA system measures the spectrum between 1545nm to 1555nm wavelengths. The measured total inter-layer coupling loss from layer 1 to layer 5 is around 19.53dB, as shown in Figure 99 (a), which is higher than the simulated value. The extra loss could come from: 1. Imperfect gap thickness control, 2. Coupling loss between layer 1 to layer 2

and 3. High surface roughness in layer 1 and 2. We then verify our mirror by using a cleaved single-mode fiber on the top of the surface coupler as optical input, while the waveguide output is designed at the side of the chip, using edge coupling. Figure 99 (b) shows the measured coupling loss. The loss is around 23.3dB since the surface coupler is not optimized for fiber coupling. We further measure the AWG transmission spectrum using a surface coupler as input. The light coupled into the chip and propagated through a 2×2 MMI and an AWG. Limited by the bandwidth of our OVNA system, we cannot measure the entire transmission spectrum of the AWG, which includes wavelengths from 1100nm to 1600nm. W measured four channels around 1550nm wavelength. We can observe that the Chanel 18 and 17 can transmit light, which matches our AWG spectrum (presented in Chapter 4). The measurements show that our device can receive normal incident light and transmit the light.

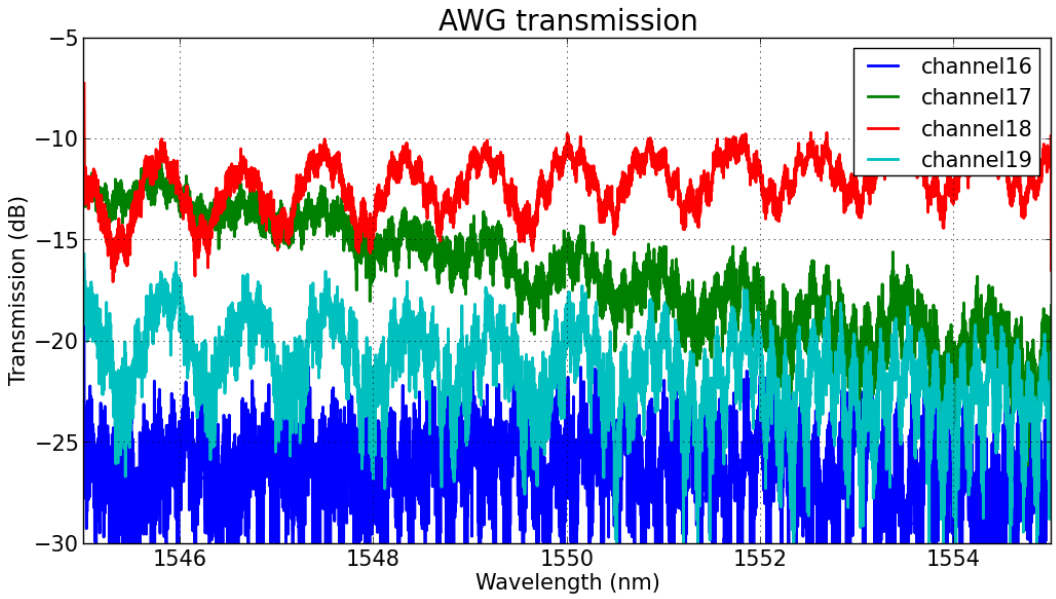

Figure 100. Measured AWG transmission spectrum.

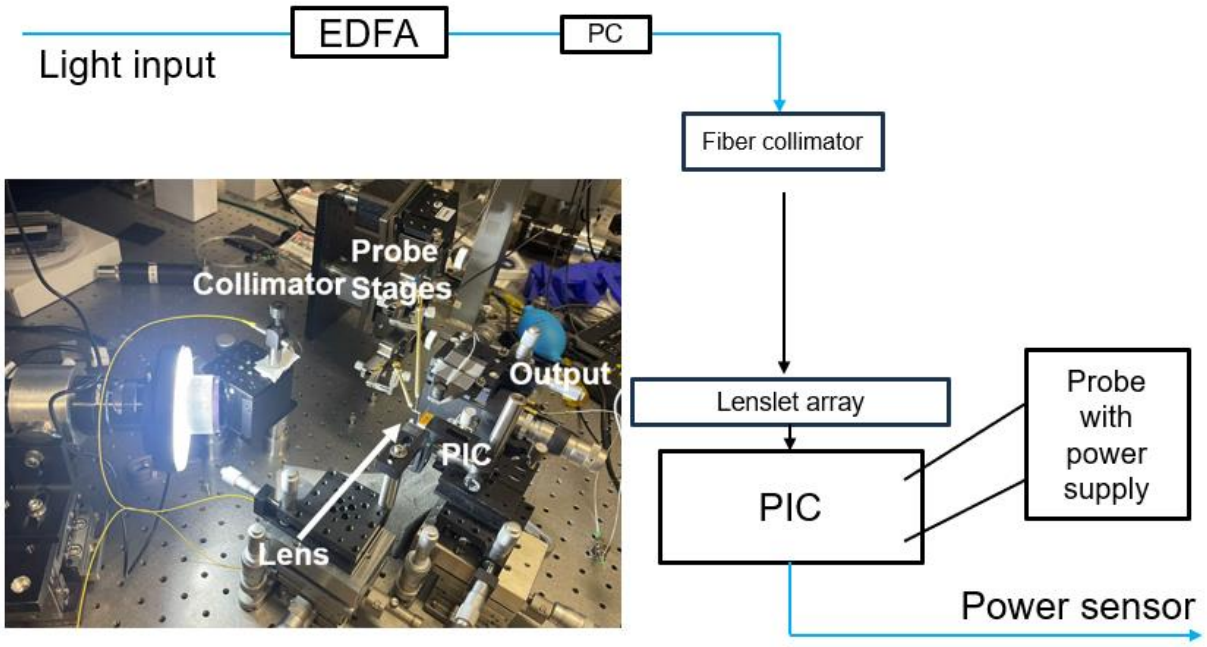

Figure 101. Photo and schematic of the fringe measurement setup.

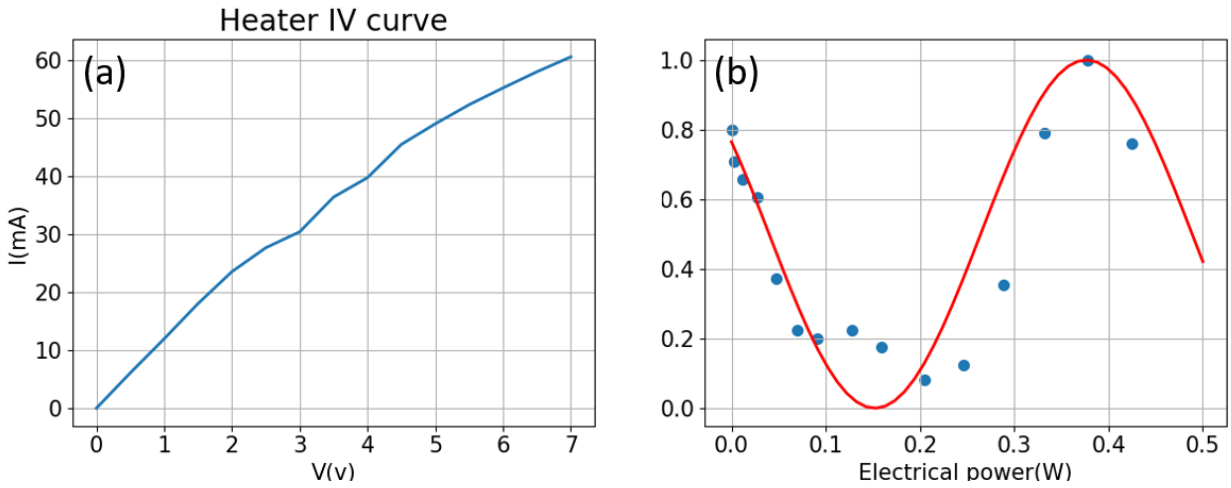

Figure 102. (a) Measured IV curve of the heater and (b) measured fringe at 1550nm wavelength.

We measured the fringe of the surface-coupled SPIDER imager using the setup shown in Figure **101**. Light from a tunable laser (fixed at 1550nm wavelength) is amplified using an EDFA. Then, we use a polarization controller to ensure that the light is coupled to our chip at the TE mode. The light from the fiber goes through the fiber collimator and is focused onto the surface couplers on the PICs using the lenslet array. We measured a baseline with a 2.16mm length. Our

fiber collimator has a 3.54mm beam waist and the collimated beam is aligned to the chip so that the two surface couplers in one baseline can receive light simultaneously. The output light goes into a single-mode fiber and is measured by a power sensor. We used two probes with positioners to control the electrical power applied on one arm of the baseline. Figure **102** (a) shows the IV curve of the heater. The curve becomes nonlinear at high voltage since the metal's resistance rises with the temperature increase. Figure **102** (b) shows the measured fringe at 1550nm wavelength, with a sinusoidal fitting. The measured result shows that our SPIDER imager can receive, propagate, and process the normal incident light and thus have the potential to perform interferometric imaging.

Our surface-coupled SPIDER imager can be improved on the following aspects:

- The coupling efficiency of the surface coupler can be greatly reduced using a large mirror, which requires the fabrication to start on SOI wafers with a thicker device layer thickness.
- The mirror quality can be improved using an HF dip. But the HF can etch the adhesion layer of the metal layer. We can use a hard mask layer for metal protection to perform the HF dip.
- The inter-layer coupling loss can be significantly reduced by minimizing the gap thickness, which requires more transition layers.
- The surface roughness of the SiO_2 cladding can be improved using a high temperature reflow.
- The propagation loss can be reduced by optimizing our waveguide process.

Future work will be the imaging experiment and the optimization of the device insertion loss.

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Chapter 6 PICs for an elastic RF-optical network

6.1 Overview of the elastic RF-optical network

This chapter presents the PICs for elastic RF-optical network, including device design, fabrication and characterization.

New photonic and RF technologies are becoming increasingly important in enabling the next generation 5G communication system [130]-[134]. Radio over fiber [135]-[137] is a promising candidate in wireless networks. For providing high bandwidth and throughput, mmWave beamforming and steering are raised and studied [138]-[141]. By putting more function blocks in the centralized optical system, the cost of a base station is significantly reduced. ROF is also suitable for centralized management, like software-defined networking (SDN) [142]-[144]. ROF is realized by combining photonics and RF technologies. Recent progress in integrated optics makes compact, low-cost, high-density photonic integrated chips (PICs) offer a new solution to radio over fiber technology. Our group proposed an Elastic RF-Optical Networking (ERON) architecture for achieving a 5G RF-Photonics system.

We first discuss the architecture of the ERON photonic-processing unit (PPU) on the system level. The based architecture is shown in Figure 103. In the Radio over fiber architecture, a signal is generated and modulated in a central office and is connected to every base station. A centralized structure enables high-efficiency central management, which is suitable for software-defined networking (SDN). The base station combines the input signal with a local signal, which has a slight frequency difference from the original signal, and then turns the signal into an RF signal. Furthermore, for implementing beamforming and SDM, we need to split the signal and

add a phase tune on each channel to realize beam steering. We will discuss the basic ERON PPU, which can meet the minimum requirement of optical signal processing, as a demonstration.

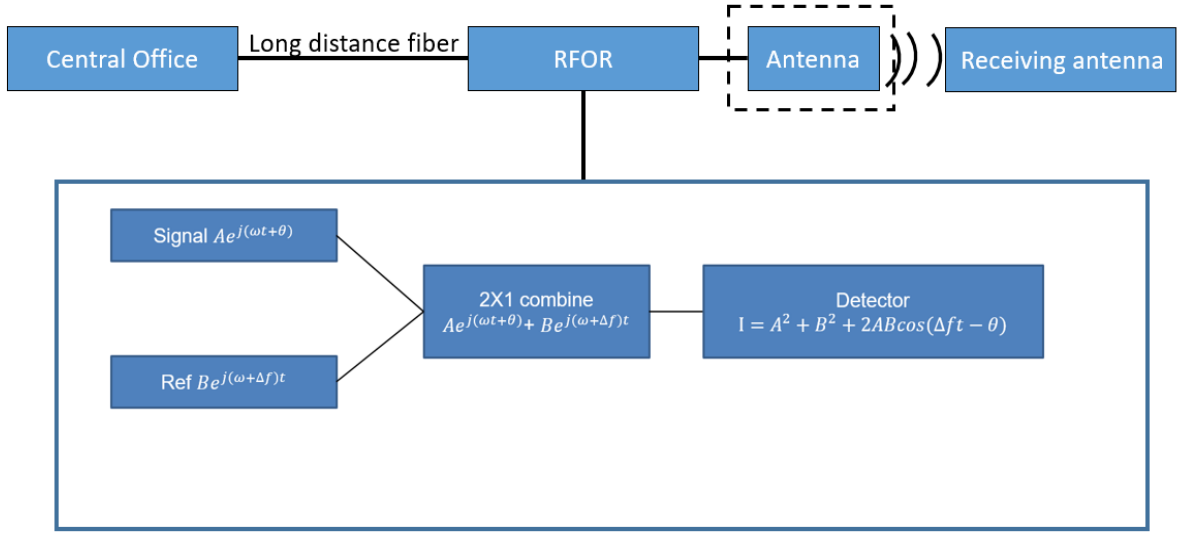

Figure 103 Diagram of ROF and ERON PPU. Signals are generated and modulated in the central office and propagate along a long fiber, like any long-distance fiber communication system. RFOR receives an input signal, combines it with a local signal, and turns it into an RF signal. The function of an antenna can be integrated into the RFOR.

The most basic function of RFOR is wave combining. The input optical signal is:

$$Ae^{j(\omega t+\theta)}$$

We can modulate the amplitude on A and phase (θ). The reference optical signal is:

$$Be^{j(\omega+\Delta f)t}$$

Δf is in RF frequency. With a 2X1 combiner, we can get the following combined signal:

$$Ae^{j(\omega t+\theta)} + Be^{-j(\omega+\Delta f)t}$$

Our photodetector can only detect the intensity of the light signal. By carefully choosing Δf, we can get a Δf frequency output:

$$I = A^2 + B^2 + 2ABcos(\Delta ft - \theta)$$

Since the B is known as A from the DC term of I, when we convert the output signal into electrical signals using detectors, we get an RF signal with Δf frequency and θ phase shift. The intensity of the RF signal is proportional to 2AB. If we can generate many RF signals with a proper phase difference between each other, we can use the RF signals to drive a phased array antenna (PAA) and generate one RF beam in a certain direction. By mixing multiple beams in the optical domain and using a proper RF filter, we can generate multiple RF beams using one antenna.

We propose a PPU to generate optical signals for multi-beam forming. The PPU requires optical devices, such as wavelength-dependent demultiplexers, to split the input signal and phase shifters to add a phase change on each channel. We use silicon photonics integrated circuits as the PPU in the ERON system for a low optical loss and crosstalk, which is critical as the number of the PIC elements scales up.

In this Chapter, Hongbo Lu proposed the ERON architecture and worked on the beam forming experiment. I did device design, fabrication and characterization.

6.2 Elements design of the PICs

The ERON PPU is realized using multiple-layer Si_3N_4 platforms with 1 ×2 coupler, demultiplexer, and waveguides routing. The section illustrates the design, fabrication, and measurement of the elements for ERON PPU. The designs in this section use 1550nm wavelength and fundamental TE mode. All the devices in this section use a 200nm silicon nitride device layer embedded in silicon dioxide cladding.

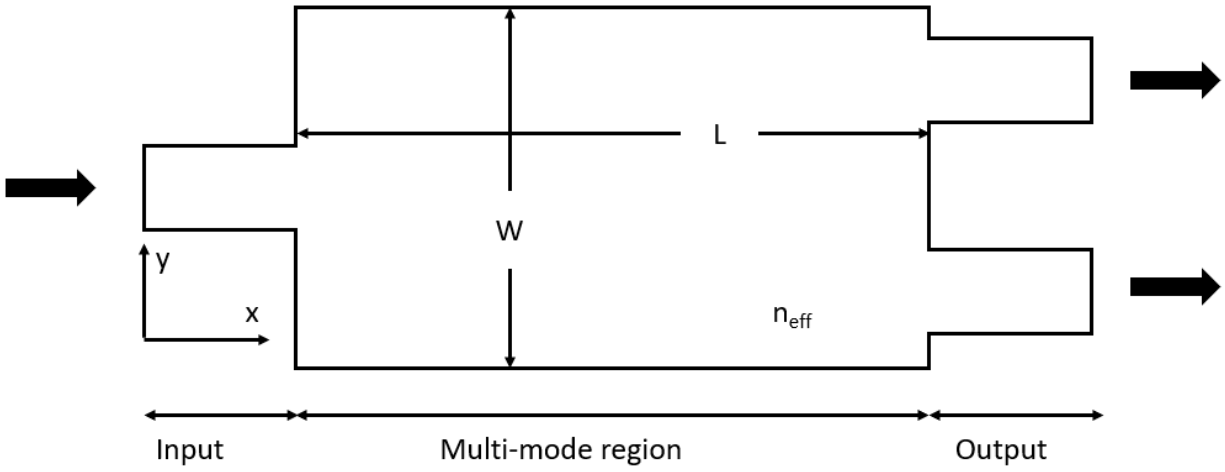

Figure 104 2D schematic of a 1×2 MMI. Black arrows denote the beam transmission.

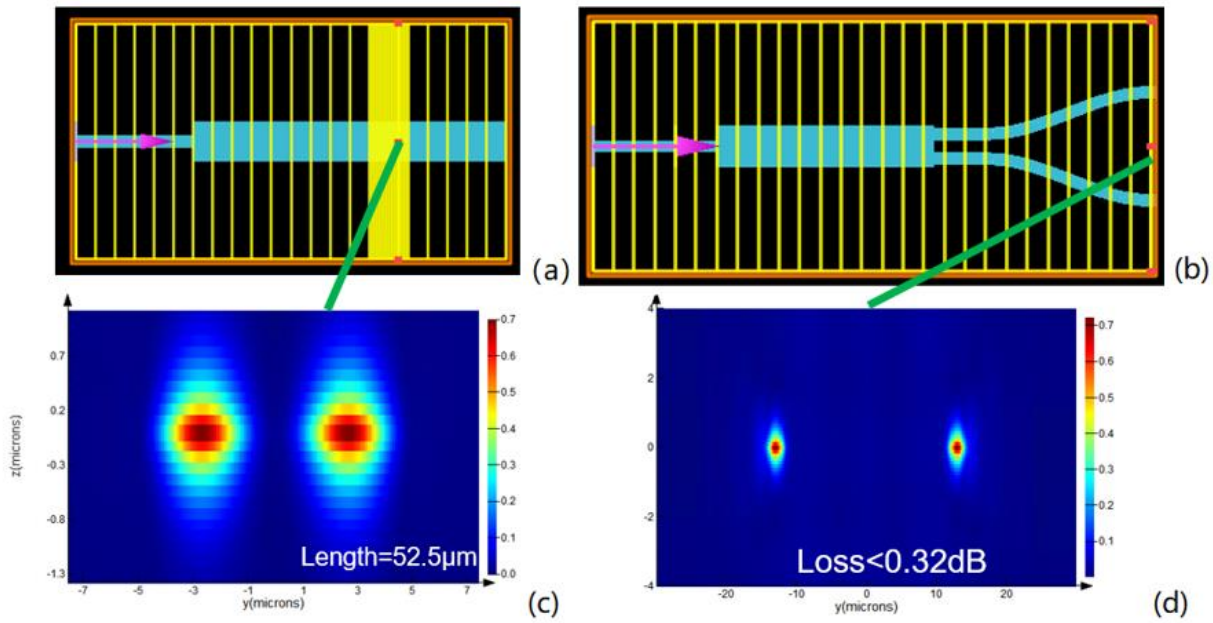

Figure 105 (a) and (b) are simulation models of MMI. (c) and (d) are simulation results of (a) and (b), respectively. The green line denotes the position of the field monitor. The focal length in (b) and (d) is 52.5μm. The width of the multimode region is 10μm. All simulation is at 1.55μm wavelength.

We use 1×2 multimode interferometers (MMIs) [145]-[147] as the 1×2 couplers for ERON PPU for their high efficiency, large bandwidth, and high fabrication error tolerance. The symmetrical structure of 1×2 MMIs decides no matter how much the wavelength shifts, the output power at the two outputs is always equal. The MMI we designed in this section has a minimum 300nm

feature size, and the fabrication imperfection will not influence the power splitting ratio between the two outputs if the imperfection influences uniformly on the MMI since the fabrication imperfections usually come from an under/over exposure and imperfect etching profile [148].

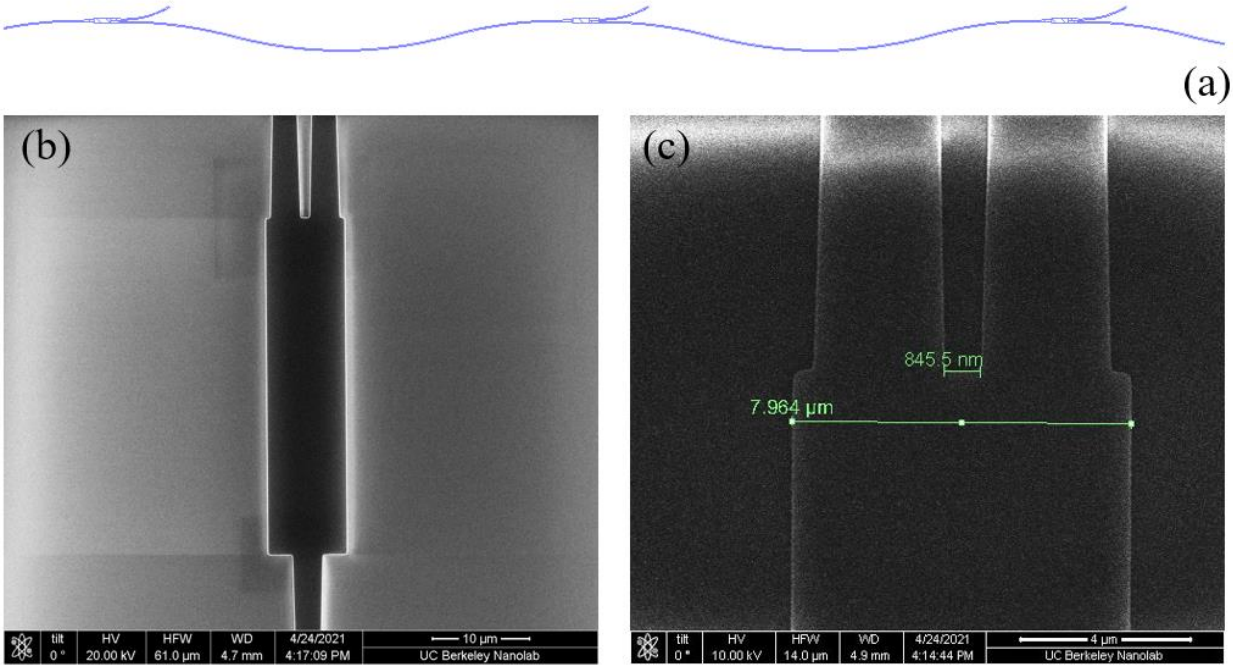

Figure 106 (a) Layout of an MMI tree with 3 MMIs. (b) SEM photo of an MMI after device patterning. (c) Zoom in SEM photo of an MMI after device patterning.

Here, we discuss two other options for the 1×2 coupler, including "Y" brunches and direction couplers. "Y" brunches can support a uniform power splitting in a large bandwidth with a low insertion loss and can require a below 250nm minimum feature size without a unique shape design, which cannot be fabricated using our projection lithography tool [149]. Recent progress on optimization and inversed design offers new solutions for fabrication low loss "Y" brunches with achievable minimum feature size at the cost of design difficulty and fabrication sensitivity.

1×2 directional coupler can achieve the same function with a higher than 500nm minimum feature [150],[151]. However, 1×2 directional couplers usually have a limited bandwidth.

Especially when the wavelength shift or the fabrication imperfection occurs, the energy splitting ratio will not be 50/50 since a 1×2 directional coupler's unsymmetrical structure.

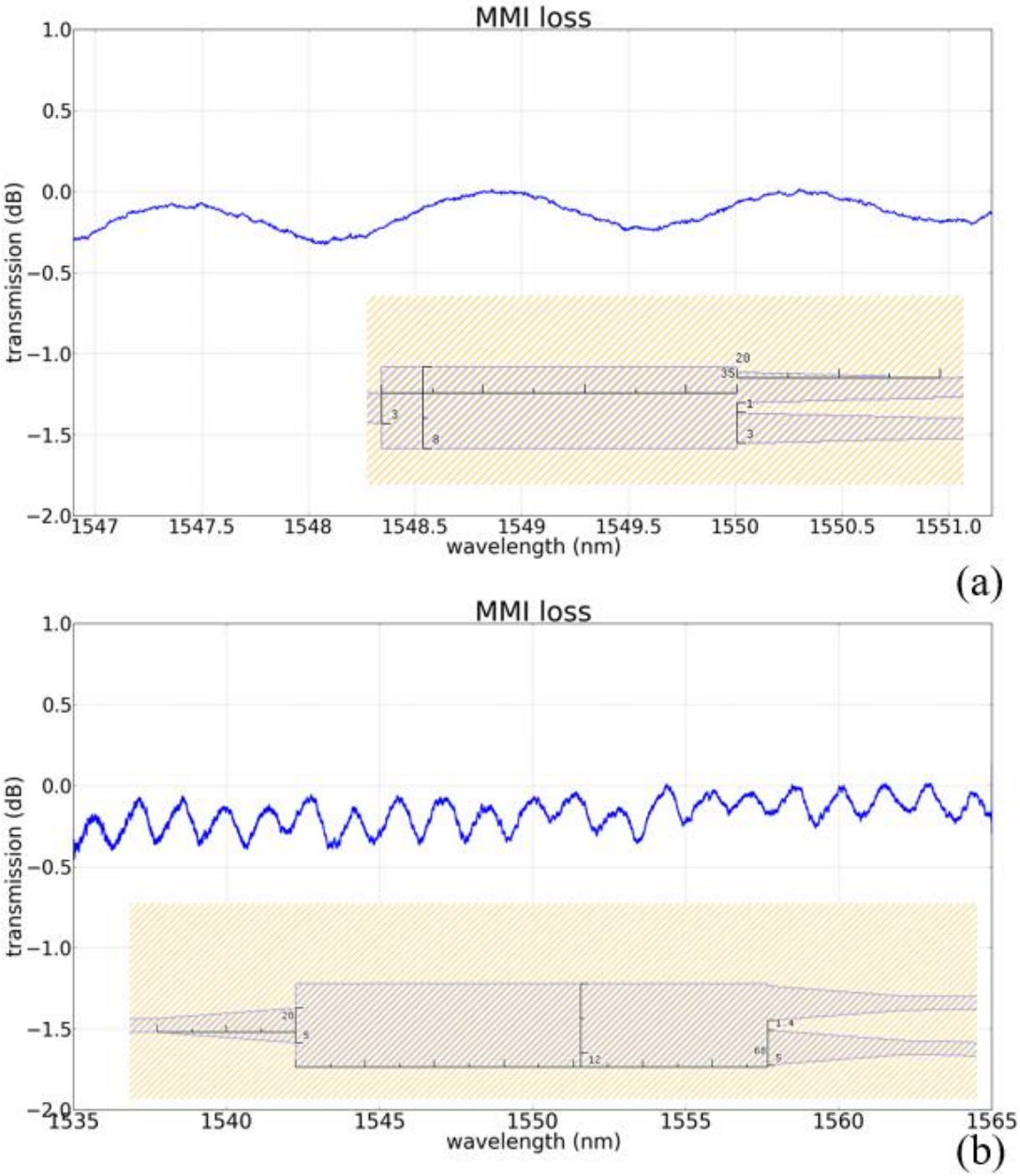

Figure 107 Measured MMI insertion loss with the layout. (a) Small size design and (b) large size design

We design the MMI using the steps method: 1. Mathematical calculation. 2. FDTD simulation. 3. Test devices fabrication and measurement. Figure **104** denotes the 2D schematic of a 1×2 MMI. One optical input is placed at the center of the waveguide. The input optical signal will transmit to the multimode region and excite high-order modes. After propagation with length L_{3dB} in the multimode region, the self-imaging property of the MMI will cause two symmetrical modes. We add two outputs to guide the two modes to 2 waveguides. The propagation constant β_m in the multimode region is calculated as:

$$\beta_m \approx kn_{eff} - \frac{(m+1)^2\lambda}{4n_{eff}W^2}\pi$$

$$k = \frac{2\pi}{\lambda}$$

In the function, we denote the effective index of the multimode region to be n_{eff}, the wavelength of the propagation optical beam to be λ, the width of the MMI to be W, and the m to be the mode number. After transmission through the multimode region with a characteristic length L_{π}, the two lowest modes will have a π phase difference. The L_{π} is expressed as:

$$L_{\pi} = \frac{\pi}{\beta_0 - \beta_1} \approx \frac{4n_{eff}W^2}{3\lambda}$$

With propagation constants, spacing is:

$$\beta_0 - \beta_m \approx \frac{m(m+2)\pi}{3L_{\pi}}$$

The transmission of the optical beam in the multimode region is considered to be a superposition of the multi modes. With the amplitude coefficient of each mode in the multimode region denoted by $c_{m,}$ we denoted the input waveguide mode as:

$$\emptyset(y,0) = \sum_{m} c_m \varphi_m(y)$$

By taking the phase of the fundamental mode as a common factor out of the sum, we get:

$$\emptyset(y,x) = \sum_{m} c_m \varphi_m(y) exp[j(\beta_0 - \beta_m)x]$$

With propagation constants, spacing is expressed as a function of L_π and m. We calculated the lowest length for forming two-fold images (L_{3dB}) as follows:

$$L_{3dB} = \frac{L_\pi}{2} = \frac{2n_{eff}W^2}{3\lambda}$$

From the equation, we find with each W comes a corresponding L to make the MMI a 1×2 coupler if the high order modes are corrected exited in the multimode region. In the 1×2 MMI design, each box width can lead to a certain design with an optimized insertion loss, and with the increasing of the box width, its optimized design has a larger device footprint and bandwidth. The design goal is to minimize device size when the bandwidth is large enough. Besides, the MMI design needs to meet the minimum feature size requirements of the nanofabrication process. The n_{eff} can be calculated by the waveguide mode derivation or waveguide mode simulation using Lumerical MODE.

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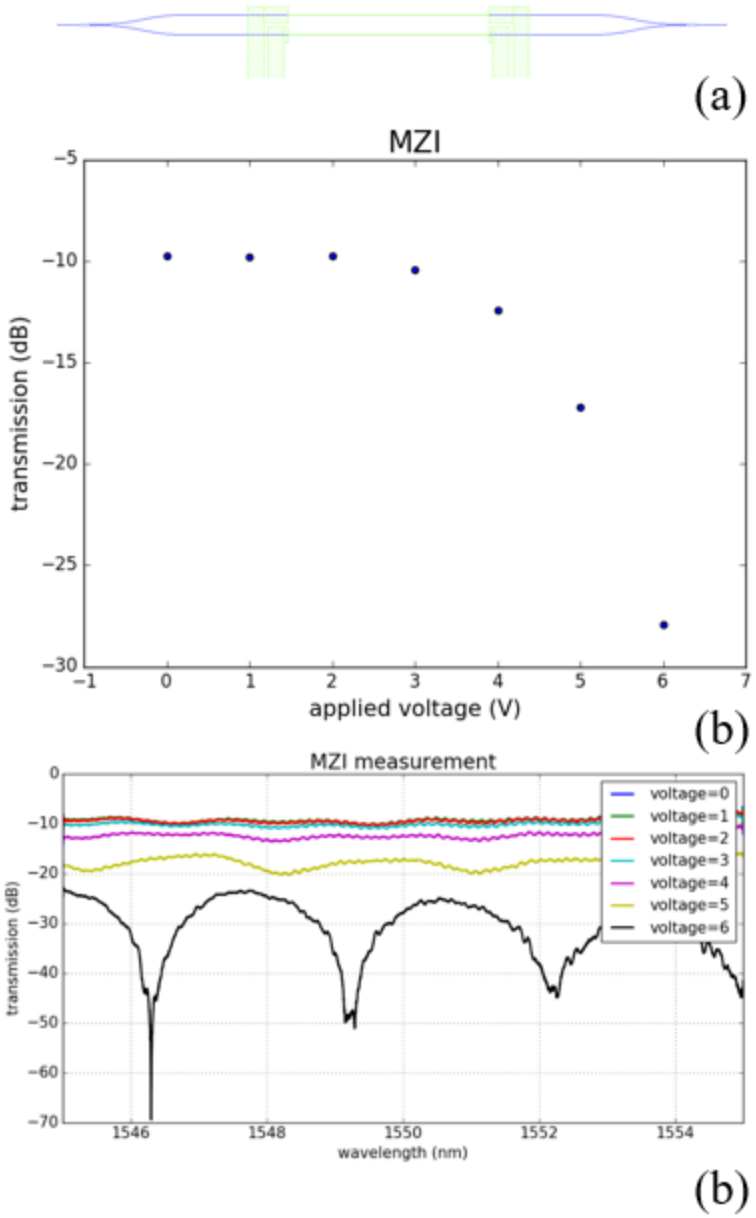


Figure 108 (a) Layout of an MZI. Blue structures are waveguides, and green structures are metal for heating and controlling. (b) Measured MZI transmission with a variable applied voltage at 1550nm wavelength, calibrated to a fiber-to-fiber loss. (c) Measured MZI transmission spectrum with a variable applied voltage around 1550nm wavelength, a fiber-to-fiber loss.

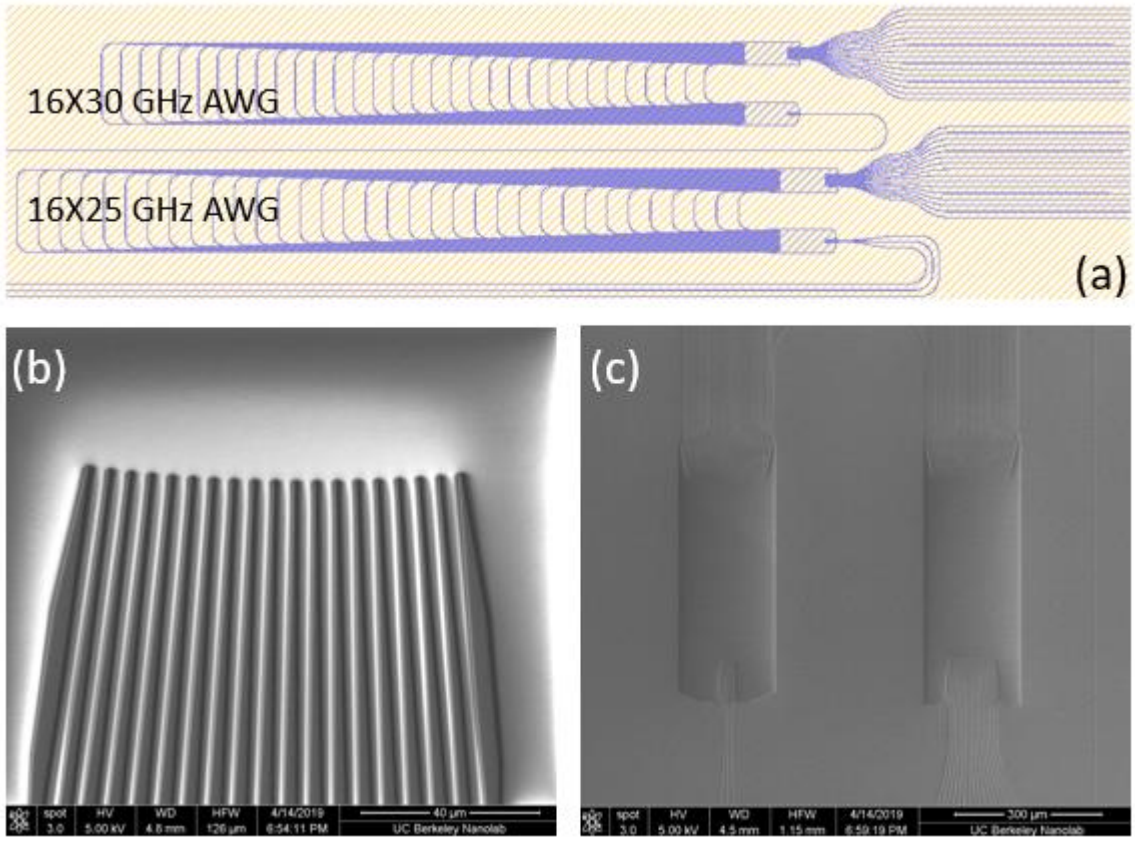
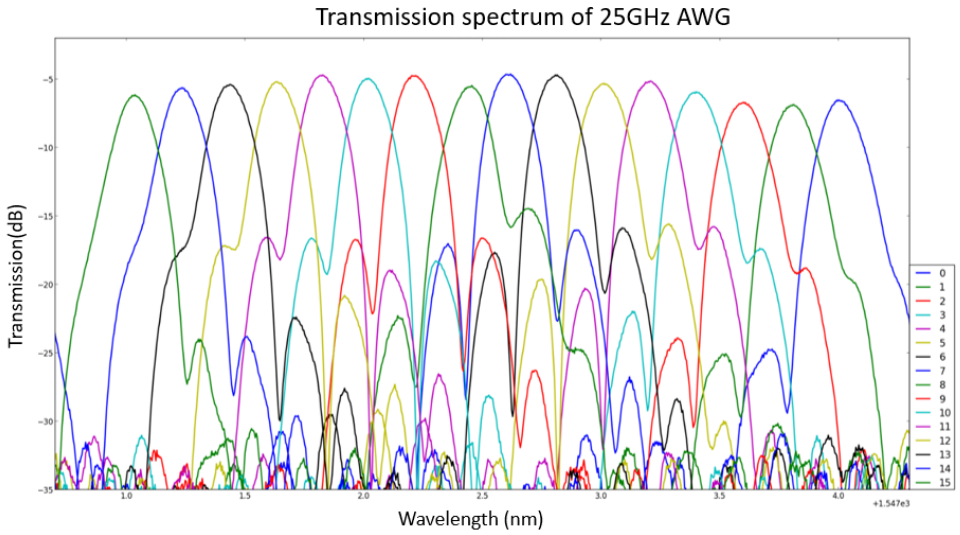


Figure 109 (a) Layout of a 16-channel, 25GHz channel spacing AWG and layout of a 16-channel, 30GHz channel spacing AWG. (b) SEM photo of the AWG after photoresist patterning. (c) SEM photo of the AWG after device patterning.

We then perform a full-size FDTD simulation to optimize the device design. Due to the existence of the Goos-Hanchen shift [152], the simulated L_{3dB} is usually larger than the calculated value. During simulation, we optimize the input and output taper length, width, and location to minimize the transmission loss. Figure 43 shows the FDTD simulation model and results of one MMI example. Firstly, we use the design parameters from the mathematical calculation as guidance. We make the box of the MMI much larger than the predicted value (and end after the end of the simulation area to eliminate the influence from the reflection at the end of the box). We find that at a certain distance (52.5μm in Figure 43(a)), the E-field is self-imaged into two separate modes, as shown in Figure 43(c). Then we use the length we got from Figure 43(a) as

the MMI box length and redo the simulation with added outputs centered at the mode center in Figure 43(c), as presented in Figure 43(b) and (d). The simulated results show a 0.32dB insertion loss. The actual transmission on one output port will be 0.32dB plus 3.01dB, which is the systematic loss from the 50% power splitting. The design can be further improved by optimizing the box length, input taper design and the outputs taper design.

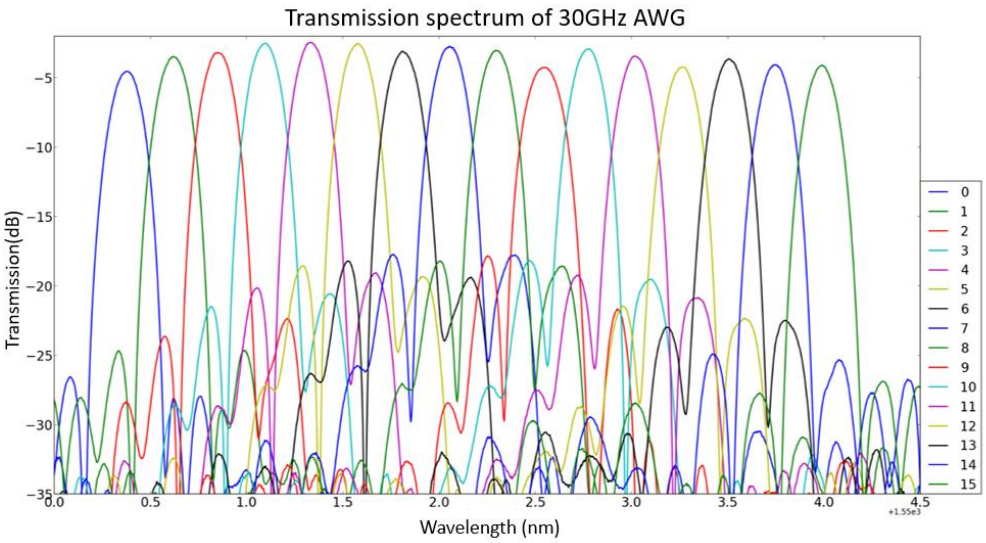


Output #	Wavelength (nm)	Maximum (dB)
1	1548.04	-6.12
2	1548.23	-5.59
3	1548.43	-5.36
4	1548.64	-5.20
5	1548.83	-4.67
6	1549.03	-4.92
7	1549.22	-4.71
8	1549.45	-5.54
9	1549.62	-4.58
10	1549.81	-4.76
11	1550.01	-5.26
12	1550.21	-5.12
13	1550.45	-5.89
14	1550.6	-6.67
15	1550.81	-6.84
16	1551.01	-6.60

Figure 110 Transmission spectrum of the 16 channel, 25GHz channel spacing AWG calibrated to a straight waveguide, with center wavelength and insertion loss of each channel shown on the right side.

To demonstrate and improve the MMI designs, we fabricate and characterize the MMIs using the low-loss waveguide fabrication process in chapter 4. We use an MMI tree, as shown in Figure 106 (a), to improve the accuracy of the insertion loss measurement by averaging the loss from many MMIs. Figure 106 (b) and (c) shows top-view SEM photos of an MMI after device patterning with the layout presented in Figure 107 (a), using an optimized lithography energy density. The low-loss waveguide fabrication process patterned the design accurately with a smooth side wall according to its device layout. After the top cladding deposition, the input and output facets are exposed using a silicon deep etching technique so that the dies after dice do not

require side wall polishing. The fabricated devices are measured using our OVNA system around 1550nm wavelength. Figure 107 presents the insertion loss of 2 MMI designs after averaging according to its layout. The matching of the simulated and measured data demonstrate our design. The measurement results demonstrate low loss 1×2 coupler designs. The ERON PPU diagram decides that the whole PICs only work within 3nm around 1550nm wavelength, so we choose the MMI design in Figure 107 (a) for our ERON PPU for its small footprint.



Output #	Wavelength (nm)	Maximum (dB)
1	1550.38	-4.46
2	1550.62	-3.43
3	1550.85	-3.16
4	1551.10	-2.50
5	1551.33	-2.43
6	1551.58	-2.50
7	1551.8	-3.07
8	1552.05	-2.7
9	1552.29	-2.92
10	1552.54	-4.25
11	1552.77	-2.90
12	1553.02	-3.33
13	1553.26	-4.17
14	1553.51	-3.54
15	1553.75	-4.04
16	1553.99	-4.04

Figure 111 Transmission spectrum of the 16 channel, 30GHz channel spacing AWG calibrated to a straight waveguide, with center wavelength and insertion loss of each channel shown on the right side.

Using the 1×2 MMI, we designed a Mach–Zehnder interferometer (MZI) to characterize the performance of our thermal phase shifter. The MZI is composed of 2 MMIs and metal heaters. The metal heaters are fabricated on top of the waveguide's layers by 2.5μm using a lift-off process. The metal heaters are 1mm long and fabricated on top of the two arms in the MZI, while only one will be tested simultaneously. We used two probes to apply voltages onto the MZI. After applying voltages onto the heater above the lower arm, the refractive index of the silicon

nitride core will slightly change and induce a phase difference ($\Delta\emptyset$) between the two arms, so after the optical signal mixing on the second MMI, the output power is:

$$p = cos^2(\frac{\Delta\emptyset}{2}) \qquad (1)$$

Figure 108 (b) and (c) shows the transmission of the MZI with a variable applied voltage calibrated to a fiber-to-fiber loss. We can observe the decrease of the transmission with the increase of the applied voltages, which shows that our phase shifter can change the phase in waveguides.

We designed small channel AWGs for ERON PPU demultiplexers using our homemade AWG design tool. The ERON PPU diagram decides that the demultiplexer channel spacing equals the RF signal frequency, which introduces a danger for high crosstalk between the channels. We design a 16-channel, 25GHz channel spacing AWG and layout of a 16-channel and 30GHz channel spacing AWG as presented in Figure 109 (a). The 25GHz AWG is designed by Kuanping Shang[153]. We verify the AWG design by fabricating test chips. Figure 109 (b) and (c) shows SEM photos of the 25GHz channel spacing AWG during fabrication. Figure 110 and Figure 111 show the transmission spectrum of the 2 AWGs calibrated to a straight waveguide. The 25GHz AWG has a 5.48dB average insertion loss on each channel with 0.76dB standard deviation on each channel, and it has a 13.3dB average crosstalk. The 30GHz AWG has a 3.34dB average insertion loss on each channel with a 0.67dB standard deviation on each channel, and it has an 18.44dB average crosstalk. The measurement results show that the AWGs can work as demultiplexers for ERON PPU. But with a smaller channel spacing, it usually comes with a larger crosstalk between channels. Besides, a small channel spacing AWG usually has a large

device footprint. The 25GHz channel spacing AWG in this section has a 7.2mm×0.8mm device size, which also introduces a high requirement for fabrication uniformity.

6.3 1st generation ERON PPU

In this section, we present the 1st generation of ERON PPU, which includes the most basic functions for ERON, including phase shifting and optical signal mixing. The ERON system uses commercial PDs to generate 24GHz mmWave frequency signals. The signal demultiplexing and EO conversion are realized using commercial devices. Figure 113 shows the diagram of the 1st generation ERON PPU. For solving the waveguide crossing between signal waveguide and reference waveguide, we use a two two-layer architecture. The bottom and the top layer have the same 200nm Si_3N_4 thickness and receive the reference signal and the users signal, respectively. The waveguides on both layers have a 3μm width. The gap between the two layers is 700nm.

Figure 112 shows the 200μm length inter-layer coupler design. Figure 113 (b) shows the layout of the PPU. Signal waveguide and reference waveguide are separated into two layers for waveguide routing. In each layer, the input signal is split into four channels by an MMI tree. The bending radius of the waveguides is 100 μm to optimize the tradeoff between the footprint and the bending loss. The user's signal after the 1×4 splitting will be connected to a phase shifter array and mixed with the reference signal from the bottom layer. We optimize the performance of the phase shifters on the PPU by minimizing the gap between the metal layer and the 2nd silicon nitride layer and using a longer metal heater.

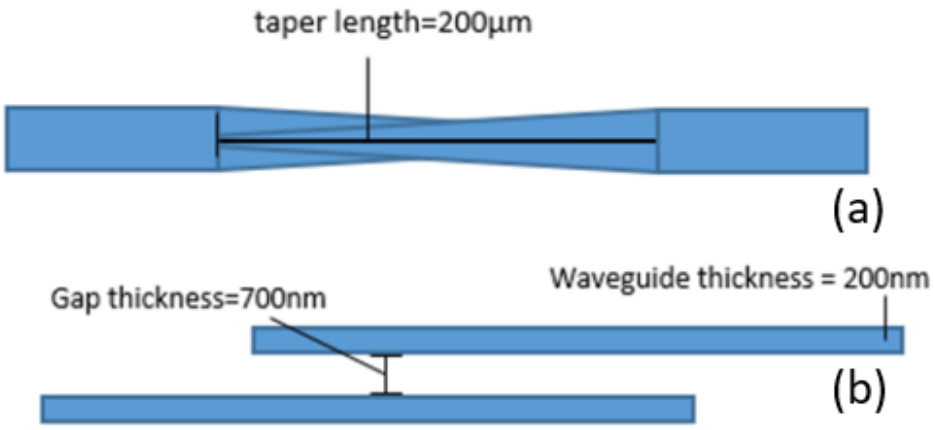


Figure 112 Diagram of the inter-layer coupler (a) top view and (b) cross-section view.

Figure 114 shows the fabrication process of the 1st ERON PPU, which is our standard multi-layer Si_3N_4 platform fabrication with a specific Si_3N_4 thickness and gap thickness. One metal layer is fabricated on the top surface for thermal tuning, as shown in Figure 115 (a). Figure 115 (b) shows the microscope photo of the fabricated chip. Figure 115 (c) and (d) show the beam transmitting and splitting in each layer using red light as indicators.

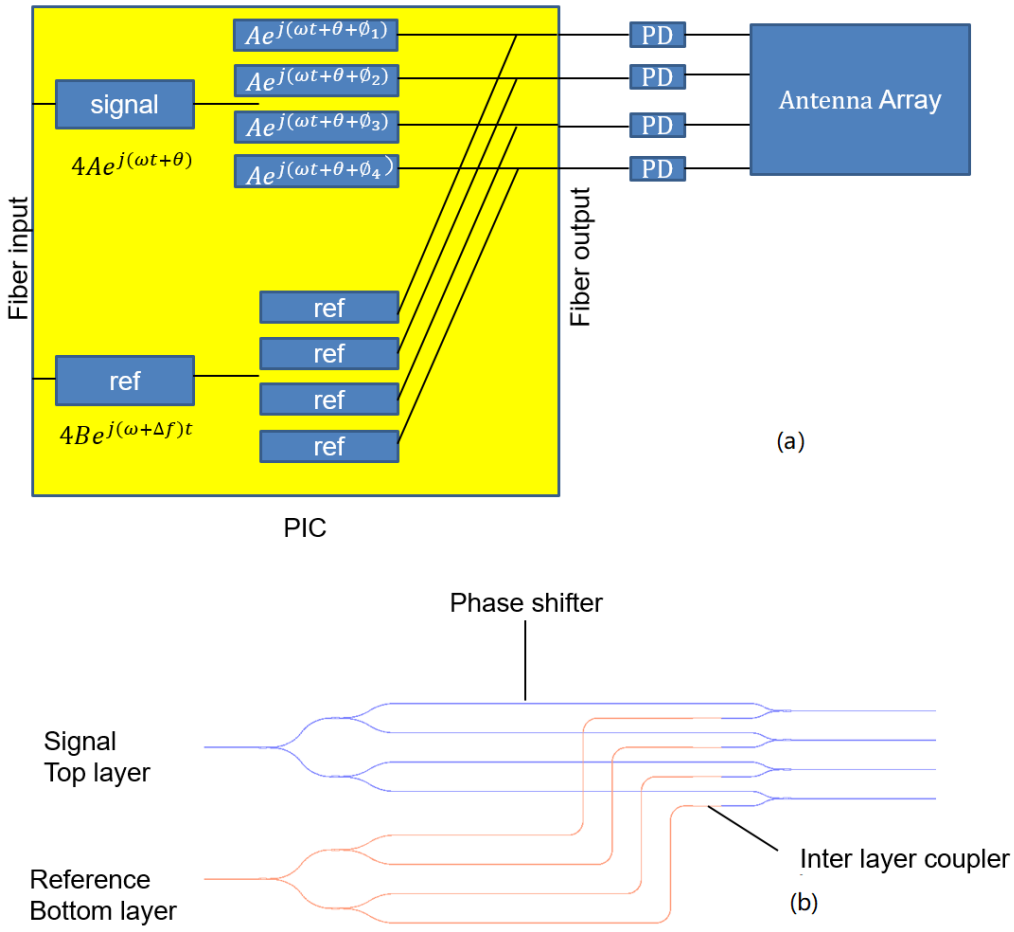


Figure 113 (a) Diagram of the 1st generation ERON PPU. Input wave is coupled into the PIC with fiber array and split into four channels, for both signal channel and reference channel. A tunable phase shift is added to each signal channel. Then, each signal channel is combined with a corresponding reference channel, coupled out to the output fiber array, and connected to the photodetector (PD). The optical signal is converted to an electrical signal and fed into an antenna array to realize beamforming. (b) Layout of the basic ROFR. The incident wave is split into four channels via a 3 1X2 splitter. Signal and reference channels are in two layers to realize wavelength crossing. An inter-layer coupler enables communication between the two layers.

We performed the mmWave beamforming experiments using the system presented in Figure 116 with the PPU. The optical signal is generated in the distributive unit (DU) located at UC Davis Kemper Hall 2230 and then transmitted to Kemper Hall 131. We first combined a 1551.74nm laser and a 1550.74nm laser and modulated the combined signal using a commercial Mach-Zehnder modulator (MZM). Each laser will generate a user signal and a reference signal. Then,

two optical tones with 24GHz frequency spacing are generated and act as the signal tone and the reference tone, respectively. The signal tone is then selected and modulated by an IQ modulator using the electrical signal from an electrical arbitrary waveform generator (EAWG). The combined user signal and the reference signal after the AWG is then amplified using an EDFA and transmitted to the remote unit (RU) Kemper Hall 131. In the 1st generation ERON PPU, we use a commercial wave selective switch (WSS) as demultiplexers. One pair of user signals and reference signals is guided and coupled into one PPU using a fiber array. The processed optical signal from PPUs is amplified and detected using a photodetector array, which can generate RF signals up to 40GHz. Vpi measurement and mmWave beamforming measurements are performed using the setup presented in Figure 116(b) and (c), respectively. The Vpi measurement is first performed using a real-time scope. Then, we switch to the beam pattern measurement, which uses a single patch phased array antenna (PAA) as the transmitter and a horn antenna as the receiver. The horn antenna is about 1 meter away from the PAA during measurement, and its received signal will be connected to an RF analyzer to measure its RF power. The single beam antenna gain is 16.4 dBi.

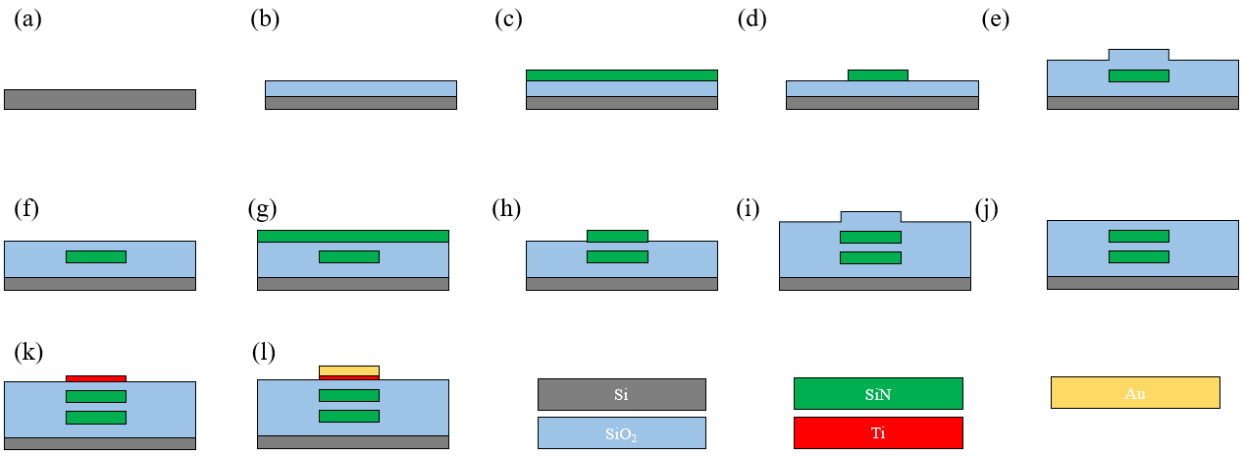


Figure 114 Fabrication flow chart of ERON device. (a) Starting 6 in silicon wafer. (b) Wet thermal oxidation. (c) 200nm thick Si3N4 first layer LPCVD. (d) Si3N4 first layer

lithography and etching. (e) LTO inter-layer deposition. (f) CMP. (g) 200nm thick Si3N4 second layer LPCVD. (h) Si3N4 second layer lithography and etching. (i) LTO top cladding deposition. (j) CMP. (k) Ti evaporation and lift-off. (l) Au evaporation and lift-off.

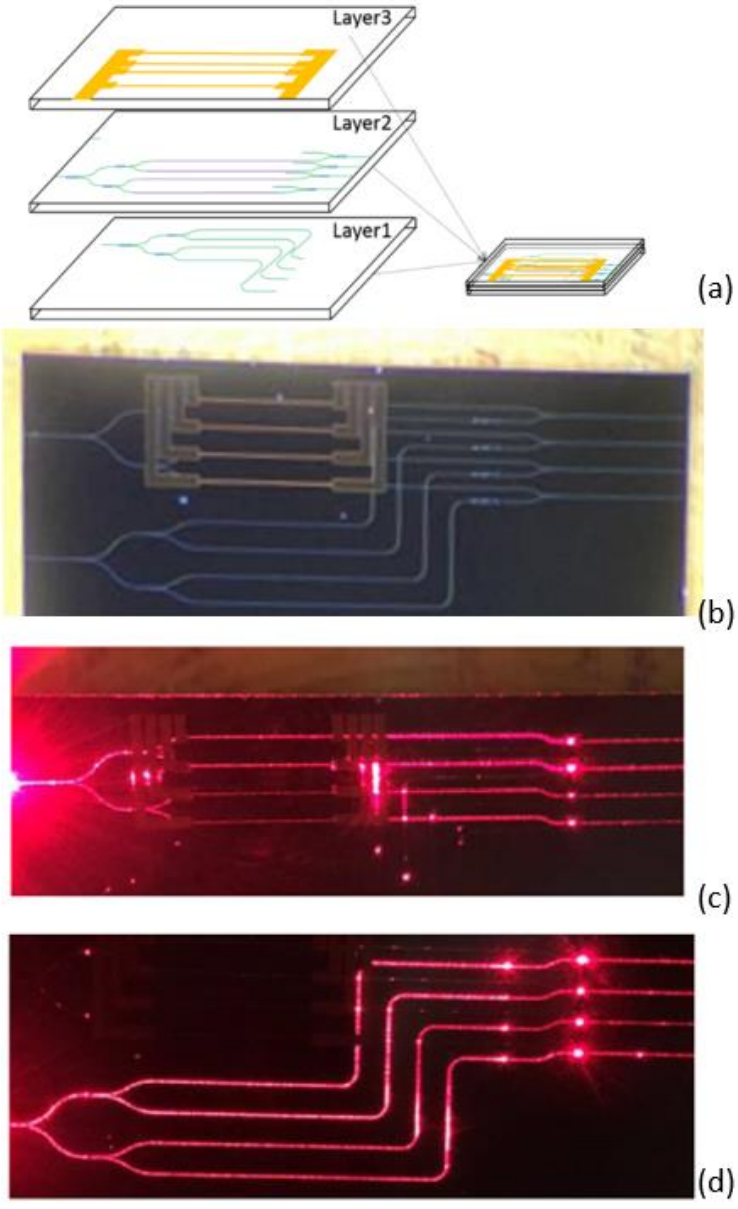


Figure 115 (a) Each layer design layout of the SiN PIC for ERON PPU. Yellow: Metal wire and pad. Purple: Optical phase shifter. Blue: MMI optical coupler. Green: SiN optical waveguide. (b) Photo of the fabricated chip (c) and (d) photo of PIC with red light coupled into, at signal and reference layer, respectively

We first perform the Vpi measurement, which gives us the characterization of the phase shifters. Figure 117 (a) shows the phase change at a variable applied voltage. We measure 3 phase shifters on one chip, and the measurement results show that they have almost the same Vpi, about 2.5V. The phase shifters have an around 77Ω resistance and 81mW for a π phase shift.

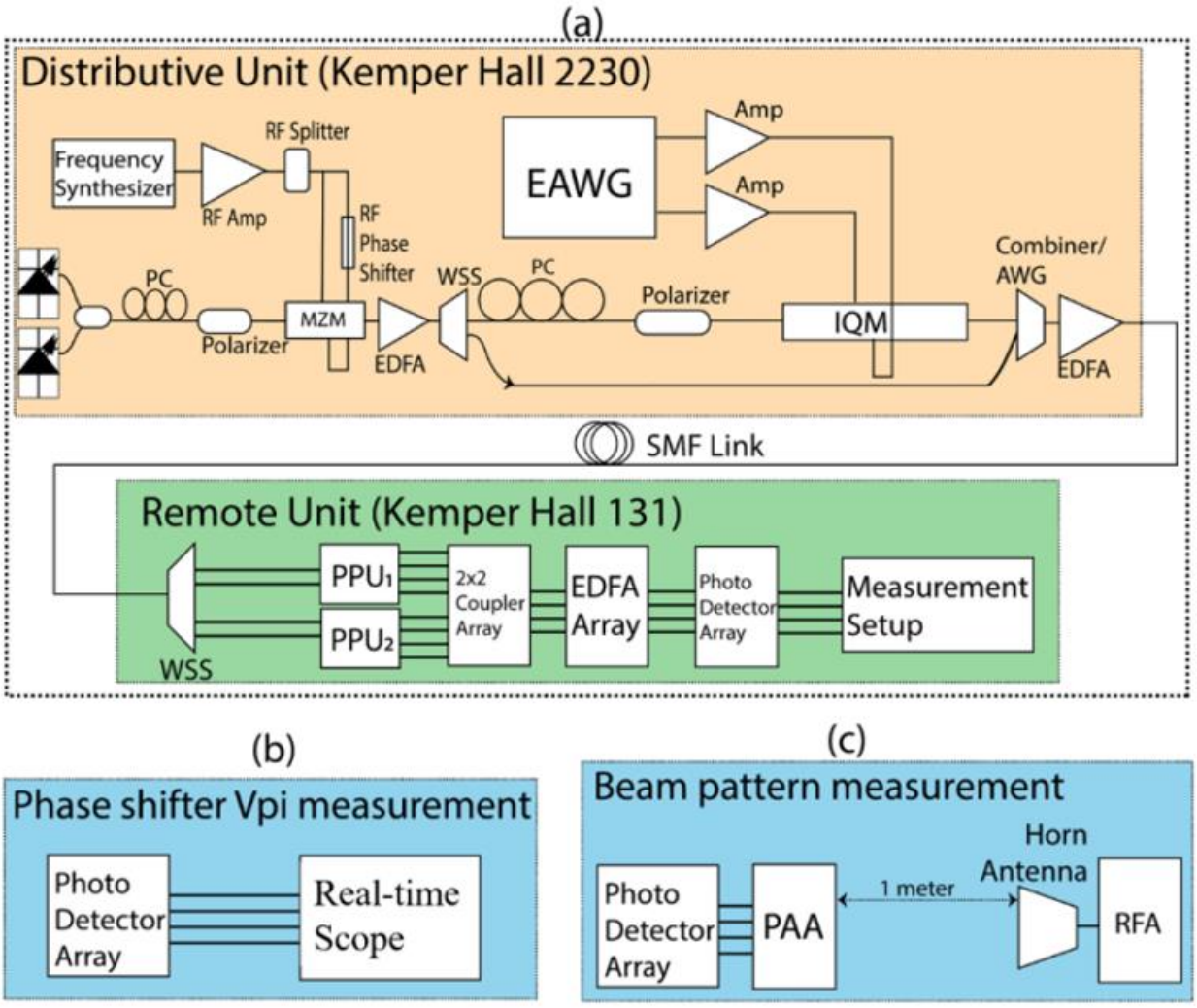


Figure 116 (a) The ERON DU-RU experimental setup. (b) The phase shifter measurement setup. (c) The far-field beam pattern measurement setup.

The beamforming pattern is then measured based on the parameters from the phase shifters. Figure 117 (b) presents the measured dual beam forming. We generated the two RF beams with their far-field denoted using blue and orange lines in Figure 117 (b), respectively. The blue line shows the far field RF beam generated by the 1550.74nm laser with no applied voltages on its phase shifter, so it is centered at 0 degrees. The orange line shows the far field RF beam generated by the 1551.74nm with phase shifter that makes the RF beam centered at -25-degree direction. We combined the outputs of the two lasers to generate the two beam signals from a single antenna, and the generated RF signal is shown in Figure 117 (b) using a black line. The beamforming result shows that our 1st generation ERON PPU can generate multiple beams using the ERON scheme.

We measured the optical front-end BER as a function of the OSNR at the RU.

The transmitted signals have 1-GHz bandwidth QPSK or 16-QAM modulation format, and both modulation formats can achieve error-free results with a 7% FEC overhead. The system we propose can achieve an 8-Gbps data rate mmWave communication.

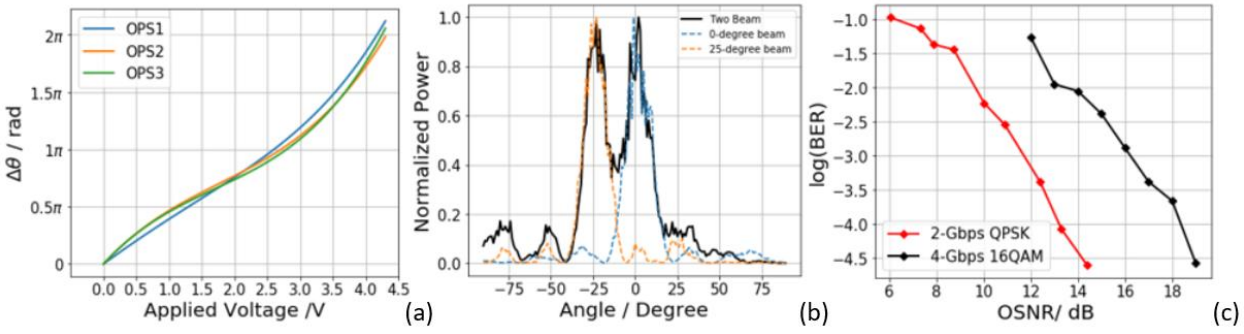


Figure 117 (a) Measured phase change as a function of the applied voltage of the phase shifter. (b) Measured far-field beam pattern from a single PCB phased array antenna at 24

GHz. (c) Measured optical front-end BER as a function of the OSNR for 1-GHz QPSK and 16-QAM signal.

6.4 2nd generation ERON PPU

For further improving the cost and scale of the PPU, we propose the 2nd generation ERON PPU with the diagram shown in Figure 118. The yellow region denotes the PICs for signal processing. The 2nd generation ERON PPU can support a 1×8 elements PAA with two mmWave beams using one chip. We integrated the 25GHz channel spacing AWG in chapter 5.2 on the PICs for demultiplexing. The PPU can process two signal channels, and each channel includes a user signal and a reference signal. The two user signals and three reference signals transmitting in a single-mode fiber will first be coupled into the chip and demultiplexed based on its wavelength. Each signal is equally divided into eight waveguides. The user signals will be thermally tuned and combined with its reference signals. The eight waveguides for one signal channel are then combined with the other signal channels and coupled into 8 PDs using a fiber array. During each 2×1 combining, there will be a 3dB systematic loss, which adds 6dB intrinsic loss on each signal.

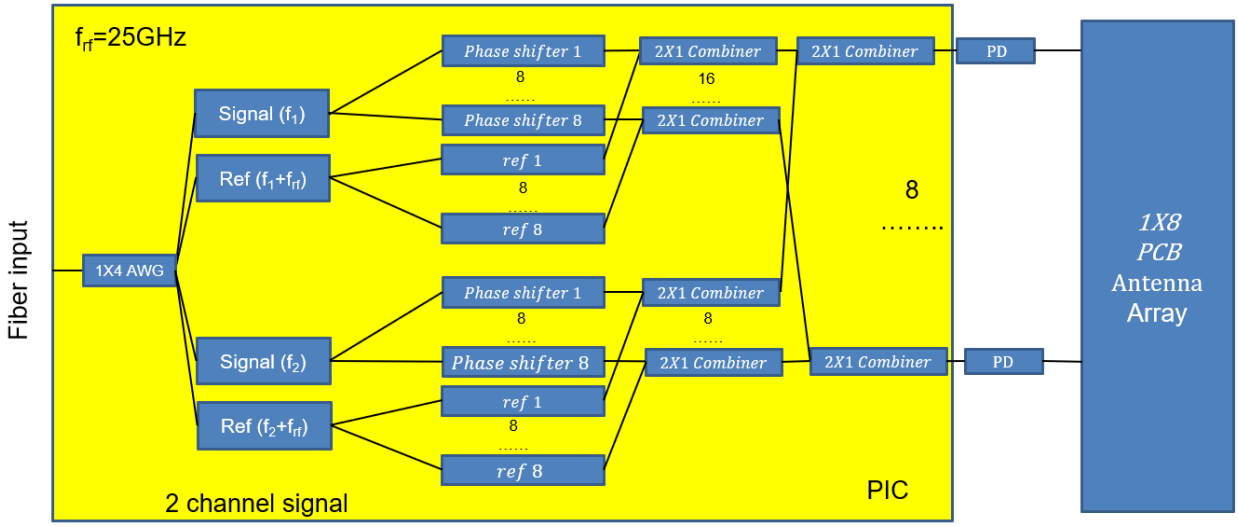


Figure 118 (a) Diagram of the 2nd generation ERON PPU. 4 signals, including two user signals and three reference signals with different wavelengths, are combined and coupled into the PIC using a single mode fiber. One signal and its adjacent reference form a signal channel. The four signals are demultiplexed, and then each signal is split into eight

waveguides for both signal channel and reference channel. A tunable phase shift is added onto each signal waveguide. Then, each signal is combined with its corresponding reference channel. Then the 2 signal channels will be combined into eight waveguides and connected to PDs using a fiber array. The optical signal is converted to an electrical signal at the PD and fed into an antenna array to realize beamforming.

The diagram of the 2nd generation PPU denotes that each waveguide could cross other waveguides by a maximum of 14 times. We use a three-layer structure in Figure 119 for minimizing the waveguide crossing loss. By adding a 100nm $S_{i3}N_4$ transition layer, we isolate the 2 200nm device layers. We use 2μm width waveguides on the device layers, guided by the simulated waveguide inter-layer crossing loss in Figure 120 (a). The simulated inter-layer coupling loss is shown in Figure 120 (b), which suggests that the coupling loss is below 0.25dB if the gap thickness is below 1.2μm. We use 1μm gap thickness as a tradeoff between the waveguide crossing loss and the coupling loss.

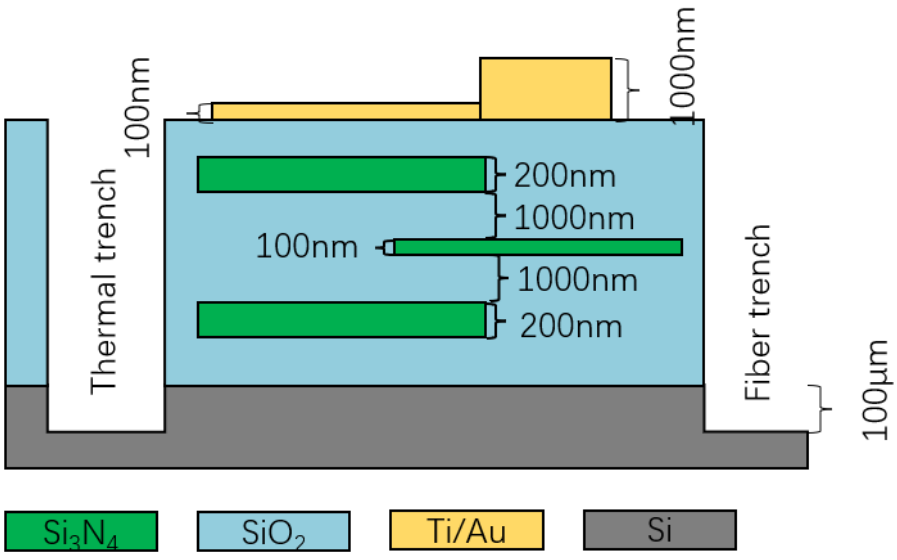


Figure 119 Diagram of the 2nd generation ERON PPU platform. The silicon nitride platform consists of 3 silicon nitride layers and two metal layers for thermal tuning. Layer 1 and 3 are function layers, while layer 2 is a transition layer. Trenches for accommodating fibers and thermal isolation are fabricated on the wafer using a silicon deep etching.

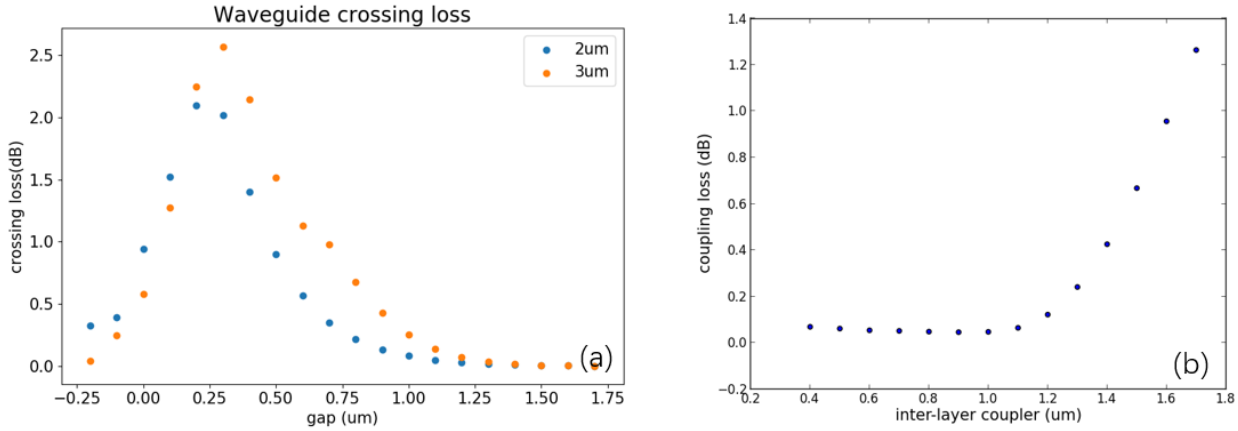


Figure 120 (a) Simulated waveguide crossing loss as a function of gap thickness with different waveguide widths. (b) Inter-layer coupling loss as a function of gap thickness.

To further optimize the performance of the thermal tuning, we added thermal trenches between the phase shifters for thermal isolation. We design a deep etching layer to fabricate trenches with more than 100μm depth. The same deep etching layer is also used for exposing the optical I/O facets. A heater layer (100nm Au) and an electrode layer (1000nm Au) are fabricated on the top surface to decrease the heating on the electrodes.

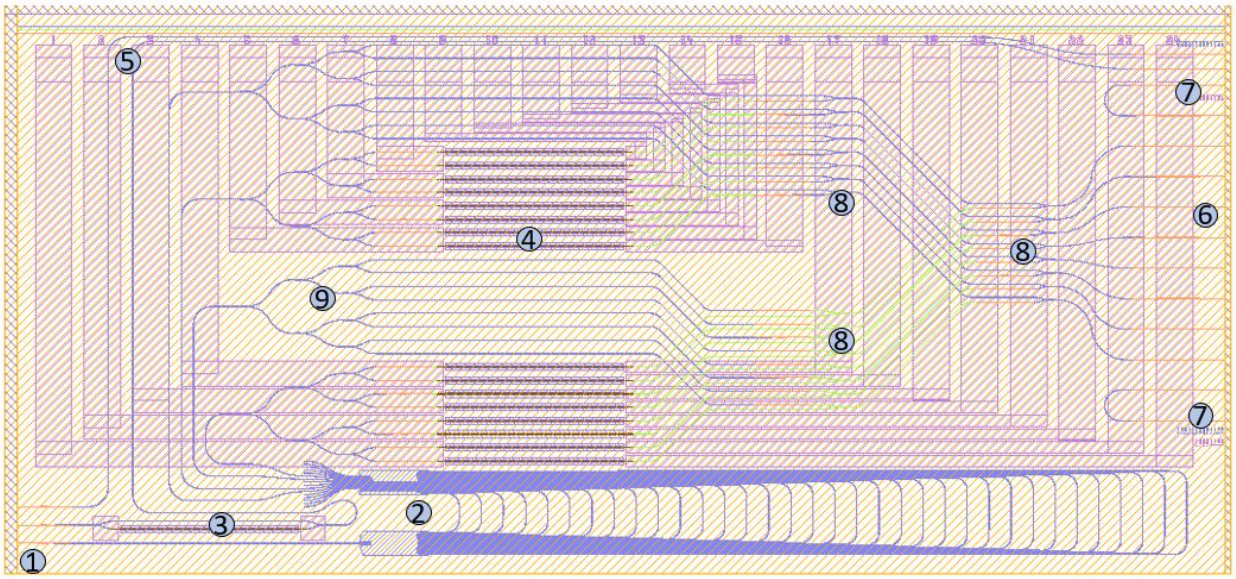


Figure 121 Layout of the 2nd generation ERON PPU. Elements are denoted with numbers: 1. Optical input, 2.25GHz channel spacing AWG, 3. test MZI, 4. thermal phase shifters, 5. electrodes, 6. optical outputs, 7. reference loops, 8. 2×1 combiner, and 9. MMI tree.

Figure 121 shows the layout of the 2nd generation ERON PPU, with elements denoted. We added one test MZI on the chip for phase tuning calibration. The user signals and reference signals are first demultiplexed by the AWG and are split equally into 8 waveguides using the MMI tree in Figure 2 (b). The user signals are routed to the top layer for phase tuning, as shown in Figure 122. Figure 123 presents the layout of the waveguides and the metal layers. Since the bottom device layer has a lower waveguide propagation loss, and the top device layer has a higher thermal tuning efficiency, we arrange most of the functional devices in the bottom layer while the thermal phase shifter is on the top. All the electrodes are connected to one side of the chip for packaging.

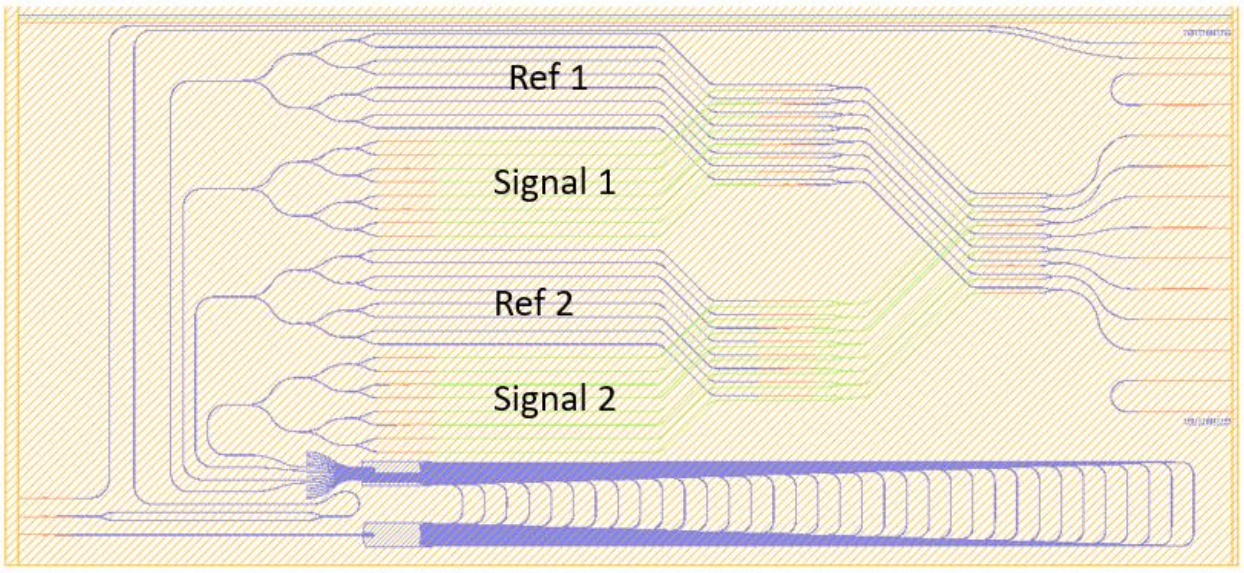


Figure 122 Layout of the 2nd generation ERON PPU at waveguides layers.

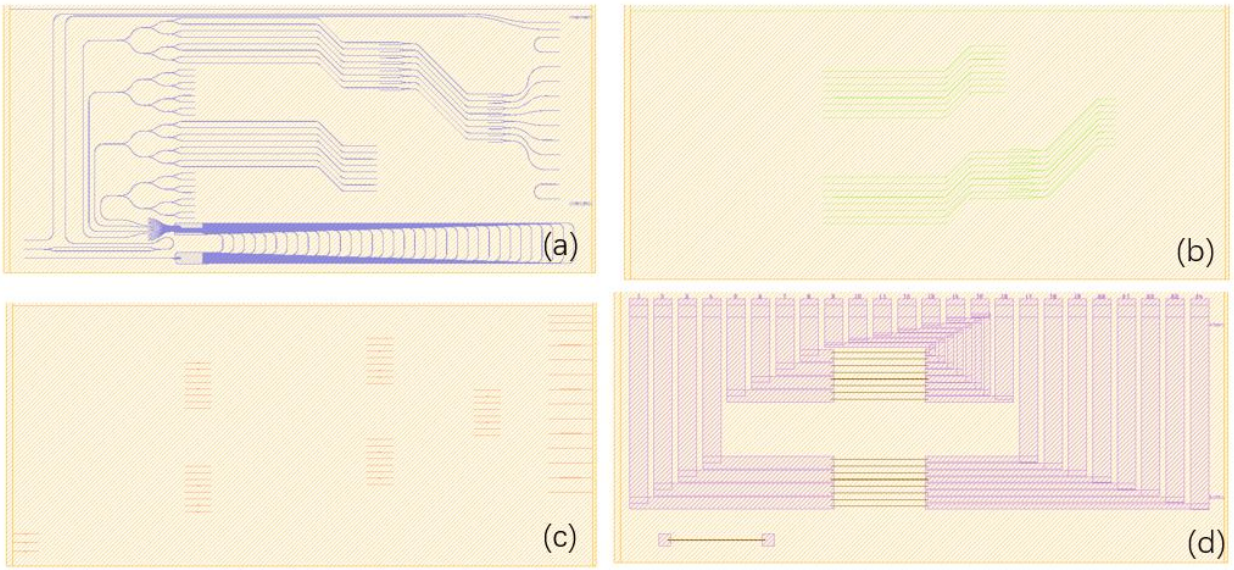


Figure 123 Layout of the 2nd generation ERON PPU (a) layer 1, (b) layer 2, (c) layer3, and (d) 2 metal layers.

We add two reference loops at the output facet. All the outputs and I/O of the reference loops have a 250μm spacing to accommodate a fiber array with the same pitch. The reference loops are used for measuring the coupling loss between the edge couplers to the fiber array and helping the fiber array to chip alignment. Two 20μm wide thermal trenches are placed around a waveguide

covered by the metal heater, with an 8μm distance to make sure the trenches will not influence the waveguide performance, as presented in Figure 124. Figure 125 shows the SEM photo of the patterned silicon nitride devices at the 1st layer using a calibrated lithography energy. Figure 126 shows the assembled microscope photo of the 2nd generation ERON PPU before the deep etching. Thermal tranches after deep etching can be clearly observed in Figure 127 (b).

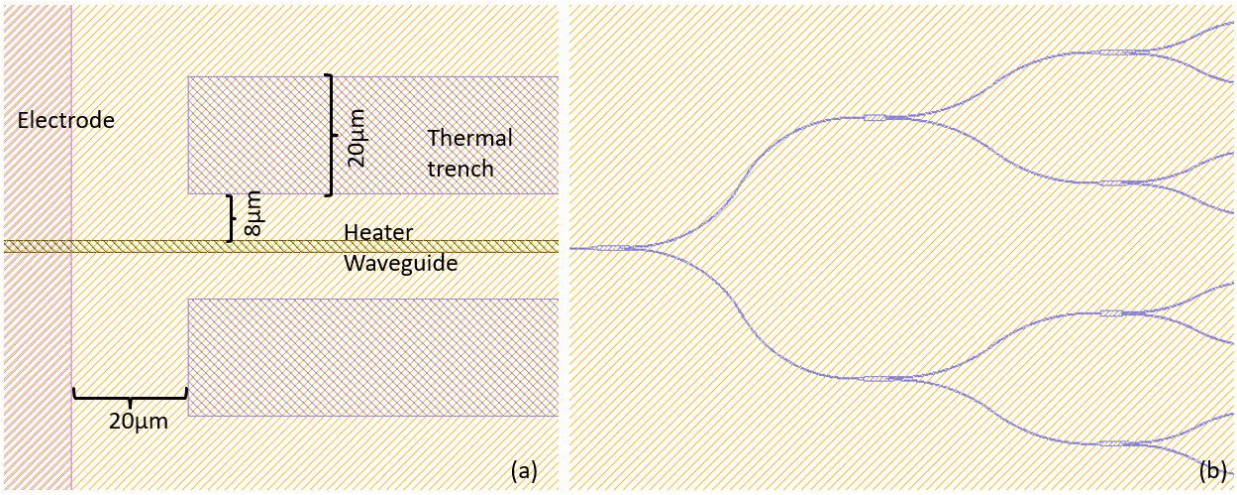


Figure 124 Layout of the 2nd generation ERON PPU (a) thermal trenches and heaters. (b) MMI tree.

We measured the 2nd generation ERON PPU using our homemade OVNA. Single components, such as MMIs and inter-layer couplers, are evaluated using on-chip test structures. Figure 128 shows the transmission spectrum of 7 cascaded MMIs. The insertion loss of a single MMI is the average from the cascaded MMIs minus 3.1dB systematic loss, which is 0.087dB around 1550nm wavelength. To further understand the performance of the 3-layer silicon nitride platform, we measured two waveguide crossing losses when the bus waveguide is on the 1st and the 2nd layers, respectively. The waveguide crossing loss presented in Figure 129 shows a higher loss when the bus waveguide is on the top layer, which can be induced by an imperfect CMP.

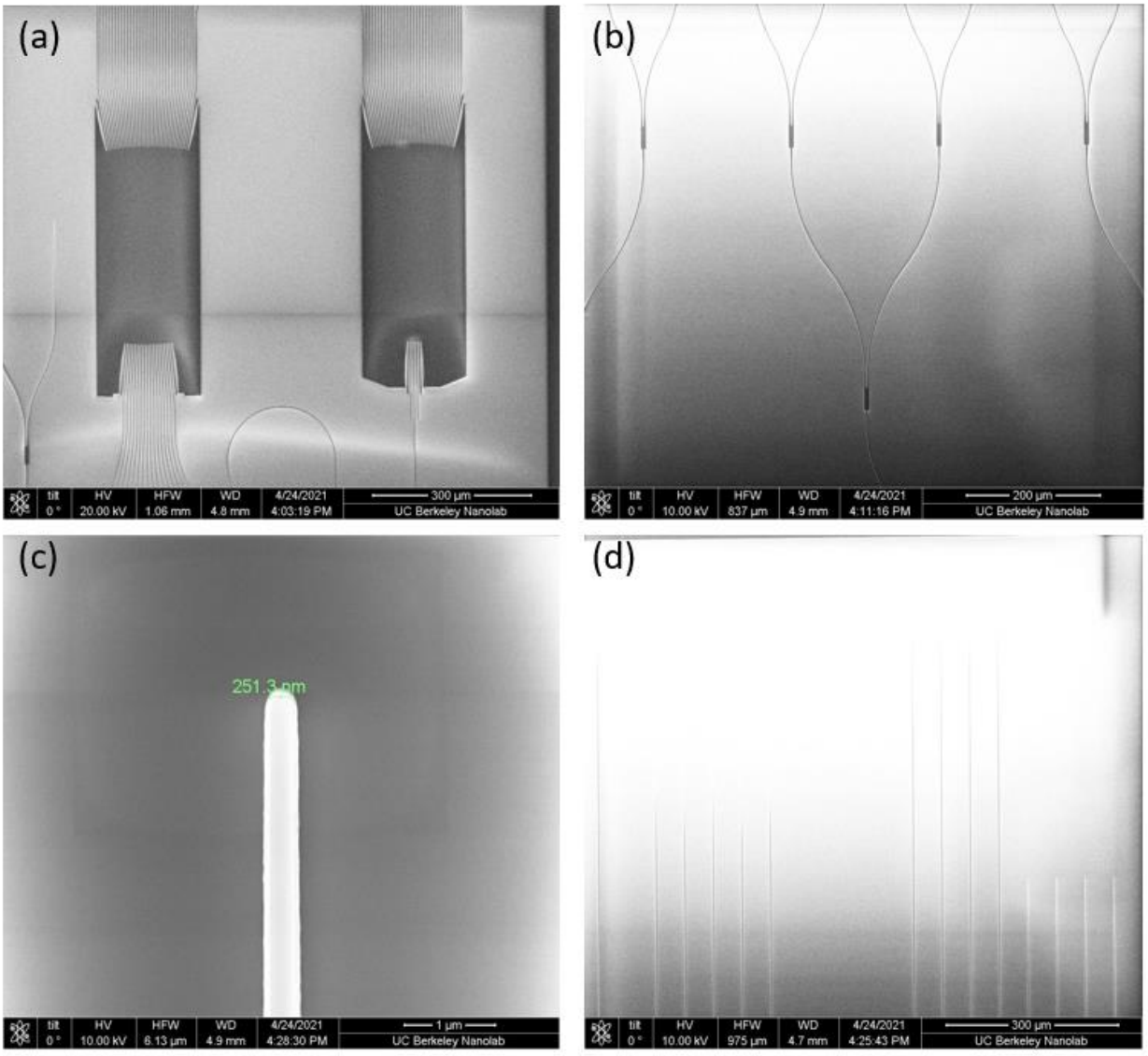


Figure 125 SEM photos of the 2nd generation ERON PPU after device patterning. (a) AWG, (b) MMI tree, (c) inter-layer coupler, and (d) waveguides.

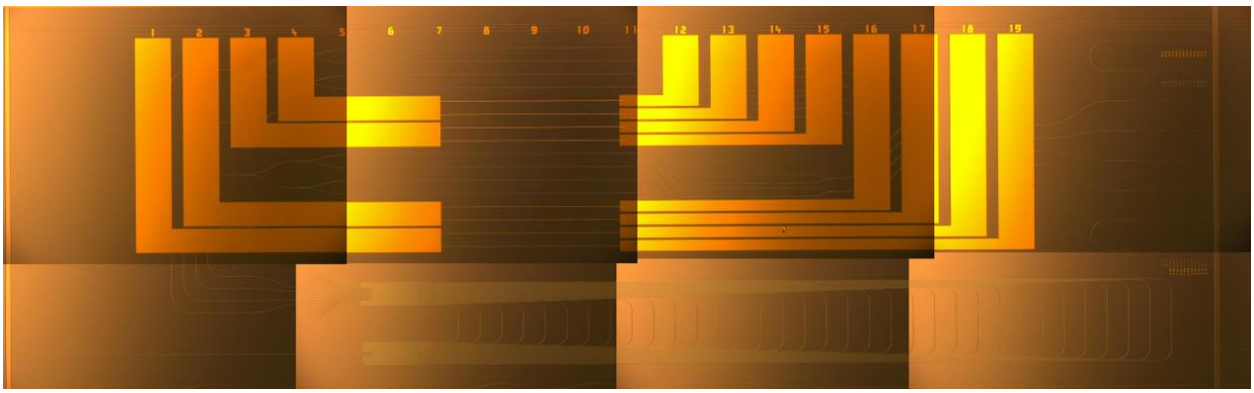


Figure 126 Assembled microscope photo of the 2nd generation ERON PPU.

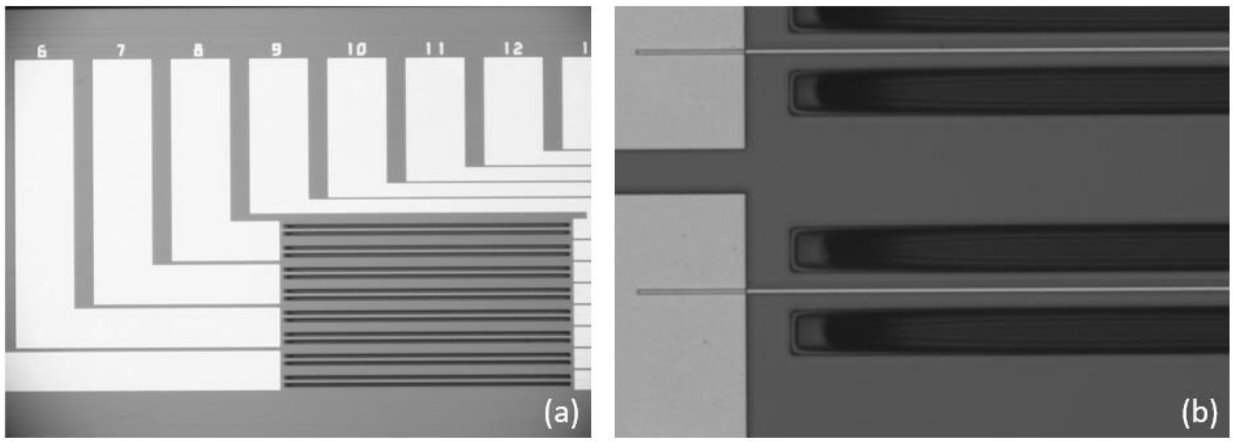


Figure 127 Microscope photo of the 2nd generation ERON PPU. (a) Metals and thermal trenches and (b) zoom-in photo of the thermal trenches.

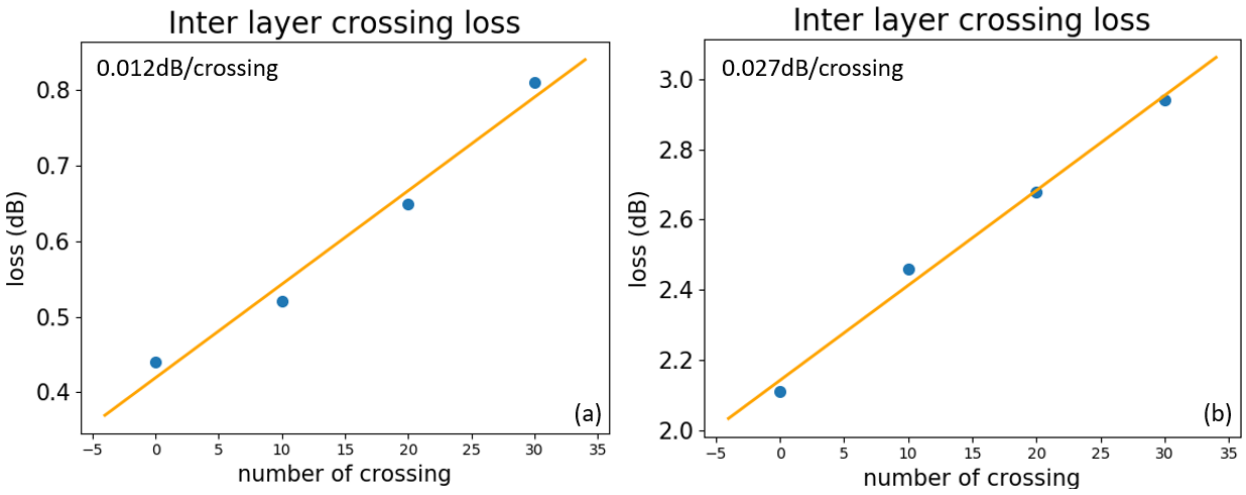


Figure 128 Transmission spectrum of an MMI tree with seven cascaded MMIs calibrated to a straight waveguide.

Figure 129 Inter-layer waveguide crossing loss when the bus waveguide is at (a) layer one and (b) layer 2.

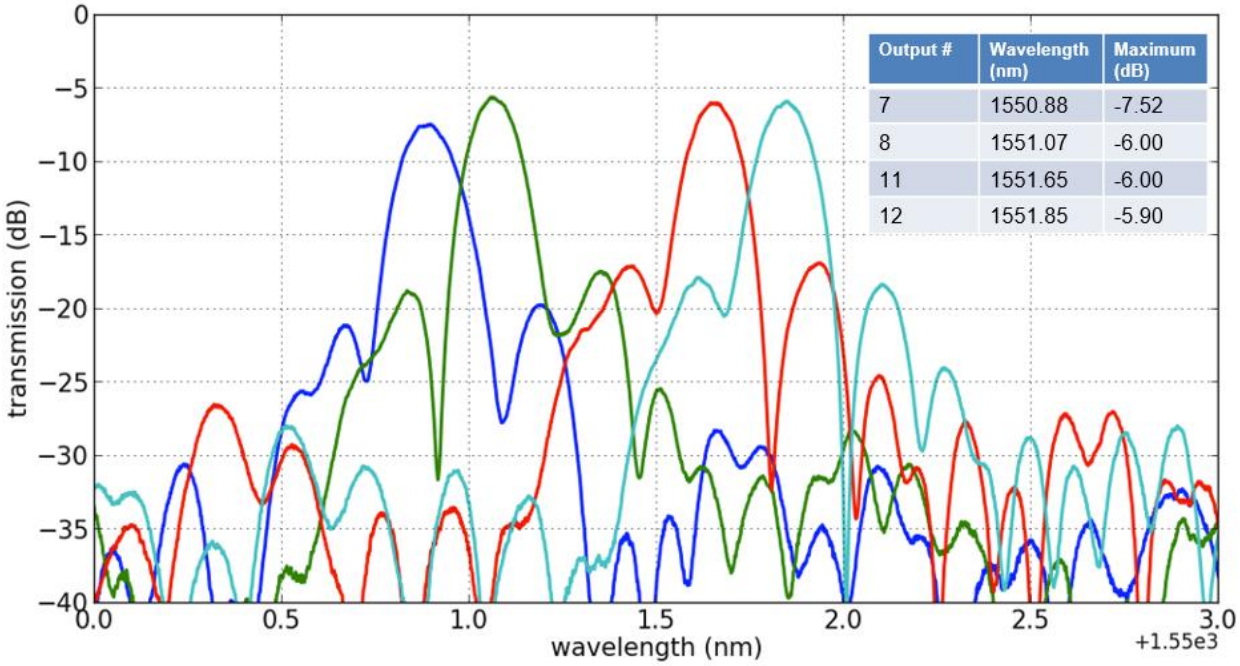


Figure 130 Transmission spectrum of the 2nd generation ERON PPU at four outputs.

Future work includes the RF beam forming experiment using the 2nd generation ERON PPU.

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Chapter 7 SUMMARY

The dissertation explored silicon photonic devices and systems in design, fabrication, and characterization on Si and Si_3N_4 platforms. The platform offers new solutions for optical sensing, computing, and communication. Chapter 2 investigates the multi-layer Si_3N_4 platform from the waveguide and device design methodology, including physics and simulation methods, followed by the low-loss Si_3N_4 devices fabrication technique using the assistance of a-Si hard mask. The deposited stoichiometric Si_3N_4 can be fabricated into Si photonic devices with a flexible thickness, width, and low propagation loss. The fabrication technique can accurately transfer large-scale silicon photonic devices to the Si_3N_4 core layer, verified by measurement data.

Furthermore, we present the multi-layer Si_3N_4 platform, including inter-layer coupler design, inter-layer crossing loss, and crosstalk analysis. We present the fabrication process and robustness of the multi-layer Si_3N_4 platform. The multi-layer Si_3N_4 platform can accommodate low-loss and CMOS-compatible Si photonic devices with a high integration density by overlapping devices vertically. The inter-layer coupling loss, crossing loss, and crosstalk are discussed for reducing the interference between layers. The flexibility and low propagation loss on the Si_3N_4 offers an excellent opportunity to realize large-scale Si photonic devices with many functional blocks.

Chapter 3 presents the elements of the optical interposer, including a low-loss, high misalignment tolerance, polarization-insensitive, and broadband inter-chip coupler for optical connection between the chip and the interposer, with design, simulation fabrication, and measurement results. During packaging, the individual dies are flip-chip bonded onto the interposer using thermal compressive bonding. The inter-layer coupler can achieve a 0.54dB

coupling loss and a ±3.53μm 3dB tolerance and can support coupling between 1.2μm wavelength to 1.6μm wavelength. Meanwhile, we develop a wafer-scale fabrication technique by combining projection and contact lithography, which enables a wafer-scale optical power distribution. The fabrication technique supports waveguide routing on an entire 6-inch wafer and can support structures with a down to 250nm feature size. We demonstrate a wafer-scale optical equal power distribution utilizing equal power splitters and a path-length matching design. At the terminals of the distribution, we pattern gratings so that the distribution can be observed and measured on top of the wafer.

Chapter 4 illustrates the design, fabrication, and measurement of the SPIDER imager. The SPIDER imagers use integrated silicon photonic devices to achieve interferometric imaging with a smaller size, weight, and power consumption than traditional imaging systems, which use bulk optic devices such as lenses. We use the multi-layer Si_3N_4 platform for its low propagation loss, large transparency window, and capability to support high-performance AWGs. We present a SPIDER imaging system using multiple chips for imaging. Furthermore, we improve the resolution of the SPIDER imaging system by enlarging the integrated chips into wafer-scale utilizing an image stitching technique. The size of the wafer limits the most extended baseline, and the die size for the largest PIC is 110mm×44mm.

Chapter 5 investigates the surface-coupled SPIDER imager based on a broadband surface coupler. We propose and demonstrate the 1st and 2nd version of the broadband surface couplers based on 45^{o} mirrors. The mirrors are fabricated using a silicon anisotropic wet etching, and their angle is decided by the crystal structure of single-crystalized silicon. The mirror reflects the light to the top surface vertically for surface coupling. Based on the surface couplers, we design,

fabricate, and characterize the surface-coupled SPIDER imager. The imager shows an excellent potential for large-scale, high-resolution, and broadband imaging.

Chapter 6 illustrates the 1st and 2nd generation PICs for elastic RF-optical networks. The elastic RF-optical network uses radio over fiber to transmit and process the optical signals with the assistance of the integrated PPUs. The PPUs can process multiple channels of optical signals for RF beam forming. The PICs include small channel spacing AWGs, phase shifters, and MMI trees for optical signal processing. We experimentally demonstrate dual beam forming using our PPUs.

APPENDIX A: LIST OF PUBLICATIONS

Publications in international journals

1. Zhang, Yu, Yi-Chun Ling, **Yichi Zhang**, Kuanping Shang, and SJ Ben Yoo. "High-density wafer-scale 3-D silicon-photonic integrated circuits." IEEE Journal of Selected Topics in Quantum Electronics 24, no. 6 (2018): 1-10.
2. Zhang, Yu, Xian Xiao, Kaiqi Zhang, Siwei Li, Anirban Samanta, **Yichi Zhang**, Kuanping Shang, Roberto Proietti, Katsunari Okamoto, and SJ Ben Yoo. "Foundry-enabled scalable all-to-all optical interconnects using silicon nitride arrayed waveguide router interposers and silicon photonic transceivers." IEEE Journal of Selected Topics in Quantum Electronics 25, no. 5 (2019): 1-9.
3. Prost, Mathias, Yi-Chun Ling, Semih Cakmakyapan, Yu Zhang, Kaiqi Zhang, Junjie Hu, **Yichi Zhang**, and SJ Ben Yoo. "Solid-state MWIR beam steering using optical phased array on germanium-silicon photonic platform." IEEE Photonics Journal 11, no. 6 (2019): 1-9.
4. Fu, Mingye, Guangyao Liu, **Yichi Zhang**, Roberto Proietti, and SJ Ben Yoo. "Monolithic silicon photonic 32x32 thin-CLOS AWGR for all-to-all interconnections." Optics Express 31, no. 10 (2023): 16623-16633.

Publications in international conferences

1. **Zhang, Yichi**, Rijuta Ravichandran, Yujia Zhang, and SJ Ben Yoo. "Large scale Si3N4 Integrated Circuit for High-resolution Interferometric imaging." In CLEO: Science and Innovations, pp. SF3J-8. Optica Publishing Group, 2023.
2. **Zhang, Yichi**, Kuanping Shang, Yu Zhang, and SJ Ben Yoo. "Low-loss wafer-scale silicon photonic interposer utilizing inverse-taper coupler." In 2018 IEEE Photonics Conference (IPC), pp. 1-2. IEEE, 2018.
3. Lu, Hongbo, **Yichi Zhang**, Yi-Chun Ling, Gengchen Liu, Roberto Proietti, and SJ Ben Yoo. "Experimental demonstration of mmWave multi-beam forming by SiN photonic integrated circuits for elastic RF-optical networking." In Optical Fiber Communication Conference, pp. Th1F-3. Optica Publishing Group, 2019.
4. Prost, Mathias, Yi-Chun Ling, Semih Cakmakyapan, Yu Zhang, Kaiqi Zhang, Junjie Hu, **Yichi Zhang**, and SJ Ben Yoo. "MWIR solid-state optical phased array beam steering using germanium-silicon photonic platform." In 2019 Optical Fiber Communications Conference and Exhibition (OFC), pp. 1-3. IEEE, 2019.
5. Fu, Mingye, Guangyao Liu, Roberto Proietti, **Yichi Zhang**, and SJ Ben Yoo. "First demonstration of monolithic silicon photonic integrated circuit 32 × 32 thin-clos awgr for all-to-all interconnections." In 2021 European Conference on Optical Communication (ECOC), pp. 1-4. IEEE, 2021.