High Power/Gain Power Amplifier Design At High Mm-wave And Terahertz Frequencies: Embedded Power Amplification

By

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Abstract

In this dissertation, a general embedding is proposed to boost the power gain of any device to the maximum achievable gain (G_{max}), which is defined as the maximum theoretical gain of the device. Using a gain-plane based analysis, two linear-lossless-reciprocal embeddings are used to perform a movement from the coordinate of the transistor to the coordinate that corresponds to G_{max}. The proposed embedding is applied to a 10μm common-source NMOS transistor, and the theoretical and simulation results are presented and compared. The properties of the embedded transistor are inspected, and the few issues in implementation are investigated and addressed. Using the proposed general embedding, an amplifier is implemented in a 65nm CMOS process with a measured power gain of 9.2dB at 260GHz, which is the highest frequency reported in any silicon-based amplifier. Then, the effect of gain and embedding of amplifying cells (amp-cell) on the output power of power amplifiers at high mm-wave and terahertz frequencies is studied. These are the frequency bands where matching loss becomes comparable to the gain of the amp-cell in most solid-state technologies. By deriving power equations of embedded amp-cell, power contours are plotted in the gain-plane and an optimum embedding is designed to maximize the output power for a desired gain. To showcase the theory, a high-frequency, high-power amp-cell, called matched-cascode, is introduced, and afterwards embedded to boost both power gain and output power. To increase the output power even further, a differential slot power combiner is introduced and its equivalent circuit is analyzed. Finally, using the embedded matched-cascode cell, and the slot power combiner, a 2x8 power amplifier is implemented in 65nm Bulk CMOS. The PA features a Psat, and OP1dB of 9.4dBm and 6.3dBm, respectively, at 200GHz, and a maximum power gain of 19.5dB.

CHAPTER 1

Introduction

High mm-wave and terahertz (THz) frequencies have found various applications in different fields from commercial to security and medicine [**1**, **5**, **7**, **8**, **10**, **21**, **28**, **32**, **41**, **55**, **57**]. In most of these applications, transceivers are the vital part of the system. One of the most important issues in transceiver design is signal amplification. Amplification is important since it improves the signal to noise ratio and data rate as well as the transceiver range. Signal amplification at submillimeter-wave and THz frequencies, however, is challenging. On the one hand, these frequencies are very close to f_{max} of active devices [**22**, **33**, **37**, **49**, **61**], meaning the available gain from the active device is low. On the other hand, high losses of input and output matching networks reduce the total power gain of the amplifier even further. Therefore, at these frequencies, the total power gain is very close to, or even less than, unity.

To address the power gain issue, designers usually unilateralize the active two-port, which is usually a single transistor, to improve stability and increase the power gain to unilateral power gain (U) of the active two-port [**9**, **11**, **23**, **26**, **30**, **39**, **40**, **59**]. Nevertheless, this technique suffers from a few drawbacks. Unilateralization may not increase the power gain very much, and in some cases, U is even less than the maximum available gain (G_{ma}) of the active two-port. Moreover, even if unilateralization improves the gain slightly in theory, the loss of passive components used for unilateralization neutralizes the gain-boosting effect of this technique.

It has been shown that maximum achievable gain (G_{max}) of an embedded active two-port is considerably higher than its U [**3**, **50**, **52**, **53**]. Hence, a promising solution to the problem of

power gain at frequencies near f_{max}, is boosting the power gain to G_{max} using an appropriate embedding. Proposed in [**52**], two different embeddings are discussed to improve the power gain by movement in a gain-plane. However, it does not provide an analytical solution to increase the power gain to G_{max}.

In this dissertation, for the first time, we propose a general embedding with its exact derivations and calculations to boost the power gain of an embedded active two-port to G_{max}. The embedding is used to create the required movement in the gain-plane, which is used to visualize the effect of the embedding. The only information that is used to find the elements of the embedding is the Y-parameters of the active two-port. Moreover, the proposed technique makes it possible to design the embedding to achieve any arbitrary power gain up to G_{max} of the active two-port. The proposed embedding is applied to a 10 μm common-source NMOS transistor in a 65 nm CMOS process with an f_{max} of 352 GHz to implement a four-stage amplifier. The amplifier features a power gain of 9.2 dB at 260 GHz that shows a significant improvement compared to the state-of-the-art.

Besides boosting the small signal gain of amplifiers at high-mmwave and terahertz frequencies, one of the key factors in improving the range of a transceiver is increasing the power it radiates, which is directly impacted by the output power of its power amplifier (PA) [**19**,**25**,**38**,**42**,**58**,**66**]. Recently achieving high maximum oscillation frequencies (f_{max}) in silicon processes has made them low-cost candidates for the implementation of transceivers at the high-end of mm-wave band [**15**, **22**, **33**, **37**, **49**, **61**]. The trade-off between the output power and operation frequency, however, stays a major challenge to overcome in PA's operating at this frequency band [**16**, **24**, **46**, **47**, **48**].

As the operation frequency gets closer to $f_{max}/2$, the available gain from transistors starts to diminish to values comparable to the loss of the matching networks [**14**, **29**, **31**, **34**, **35**, **43**, **44**, **60**, **64**, **65**]. This, as elaborated in Chapter II, not only lessens the overall gain of the PA, but also adversely affects the maximum output power of the PA with a practical

gain. Low power gain, also, adds to the number of cascaded amplifying cells (amp-cells) needed to reach a desired gain, increasing DC power consumption. From Chapter 5, we use the term amp-cell instead of A2P as it matches the context. High-voltage topologies such as cascode and stacked amp-cells are traditionally used to increase supply voltage by which the maximum output swing and hence the output power can be elevated. Nevertheless, conventional cascode amp-cells commonly suffer from large inter-cell parasitic capacitance and hence small gain at higher mm-wave frequencies [**12**]. Stacked amp-cells have even lower gain compared to cascode as the gate capacitors function as a negative voltage feedback and reduce the gain [**2**, **56**].

Power combining techniques, which mostly fall into series and parallel categories, can be used to raise the output power. Nonetheless, the former suffers from imbalanced input impedances due to parasitic capacitors between the primary and secondary of the transformer and therefore, the output power and gain drop [**62**]. The latter increases the impedance transformation ratio and the loss of the output matching network, and thus decreases the output power and gain [**13**].

We aim to maximize the output power of the PA while operating at high mm-wave frequencies. To this end, a strategy that combines system and circuit-level optimization and design, with passive power combining technique is proposed, to implement a 200GHz PA in 65nm CMOS process. This strategy can be implemented in any other technology as well. In the system-level analysis, the effect of power gain on the output power of a PA at frequencies where the gain of amp-cells becomes comparable with the loss of matching networks is explained. It is illustrated that embedding boosts both gain and output power of a PA for a minimum amplification. In the circuit-level design, the stable region of the gain plane in [**6**] is analyzed and power contours are demonstrated to find the optimum embedding that maximizes the output power for a given power gain. Then, a high-power, high-frequency amp-cell called matched-cascode with an optimized embedding is introduced to maximize the output

power for an acceptable power gain. Finally, a balanced, and wideband slot power combiner is introduced to boost the output power even further. Using the embedded matched-cascode amp-cell and the slot power combiner, a 2x8 embedded power amplifier with an output saturated power P_{sat} of 9.4dBm and gain of 19.5dB is implemented at 200GHz in a 65nm CMOS technology.

The rest of this dissertation is organized as follows. Chapter 2 gives a short review of three basic power gain definitions that are used in the rest of this dissertation. In Chapter 3, the gain-plane and its properties are studied. The embedding elements values are calculated and derived for any desired gain including G_{max}. Chapter 4 studies the practical limitations of such gain boosting. A four-stage embedded amplifier at 260GHz is presented in this chapter using the proposed embedding, and the measurement results are illustrated. Chapter 5 explains the main challenges in achieving high P_{sat} at high frequencies, as well as the impact of gain on output power in a cascaded power amplifier. Output power in embedded amplifiers is studied in this chapter. A high-power, high-frequency, matched-cascode amp-cell is introduced in Chapter 6. In this chapter, the wideband, balanced slot power combiner is discussed, and the simulation results are presented, as well. At the end of this chapter, the implementation of the PA is explained, and the measurement results are demonstrated as well as comparison with state-of-the-art. Finally, Chapter 7 concludes this dissertation.

CHAPTER 2

Basic Gain Definitions

In this chapter, we review three basic power gain definitions for a two-port, and their relationships. This review proves useful when we maximize the power gain in Chapter 3.

2.1. Maximum Available Gain (G_{ma})

Maximum available gain (G_{ma}) of a two-port is defined as the ratio of the available power from the output port of the two-port to the available power from the source. G_{ma} is achieved when the source and load impedances are conjugate matched to the input and output ports of the two-port simultaneously. Simultaneous matching is possible only when the two-port is unconditionally stable [**45**].

Fig. 2.1 shows a two-port that is active and unconditionally stable. The active two-port (A2P) in Fig. 2.1 is shown as a black box and represents any active transistor-based circuit combination throughout this paper. The simple and popular combinations are common-emitter and common-source amplifiers. For an amplifier to be unconditionally stable, the amplifier's stability measures K and Δ must satisfy $K > 1$ and $|\Delta| < 1$ conditions [**45**]. G_{ma} of an A2P can be written as a function of its parameters:

$$G_{ma} = |A| \left(K - \sqrt{K^2 - 1}\right), \quad \text{where} \quad A = \frac{Y_{21}}{Y_{12}} = \frac{Z_{21}}{Z_{12}}. \tag{2.1}$$

Fig. 2.2(a) shows G_{ma} of a 10 μm common-source NMOS transistor in 65 nm CMOS process versus frequency. Fig. 2.2(b) illustrates that G_{ma} is only defined at frequencies higher than 255 GHz in which both the stability measures are satisfied.

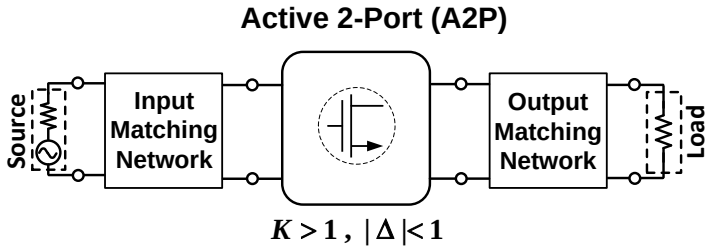
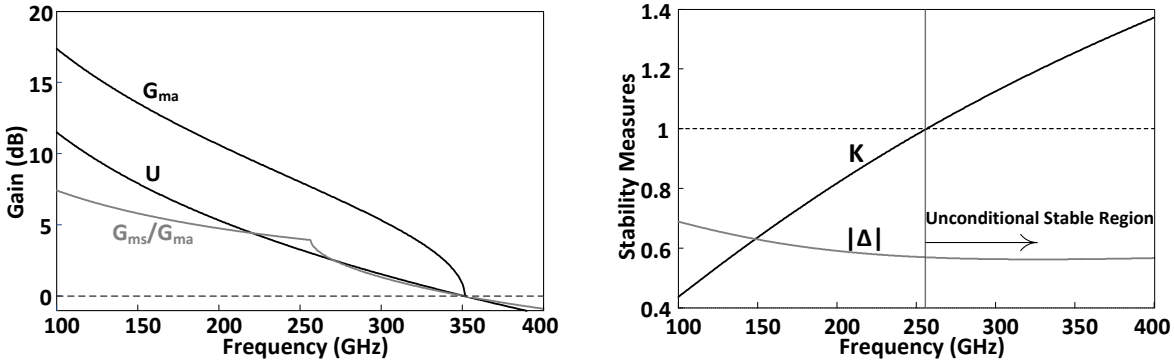


FIGURE 2.1. The conditions under which maximum available gain (G_{ma}) is defined for a two-port (an A2P here).



(a) (b)

FIGURE 2.2. Power gains and the stability measures of a 10 μm common-source NMOS transistor in 65 nm CMOS process. (a) G_{ma}, U, and G_{max}. (b) K and $|\Delta|$.

2.2. Unilateral Power Gain (U)

This power gain is defined as G_{ma} of an A2P that is unilateralized using a linear-lossless-reciprocal (LLR) embedding. Fig. 2.3 illustrates the conditions under which U is defined. U is given below as a function of the Y-parameters of the A2P:

$$U = \frac{|Y_{21} - Y_{12}|}{4(Re[Y_{11}] \cdot Re[Y_{22}] - Re[Y_{12}] \cdot Re[Y_{21}])}. \tag{2.2}$$

Fig. 2.2(a) shows U of the same 10 μm transistor. The figure depicts that U is defined even at frequencies in which $K < 1$. Moreover, U is invariant under LLR embedding [**36**].

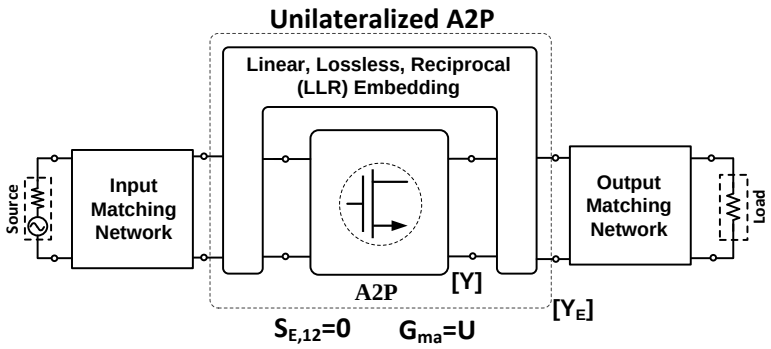


FIGURE 2.3. A unilateralized A2P. $S_{E,12} = 0$.

In other words, U is only a function of the A2P parameters and LLR embedding does not change it. Fig. 2.2(a) shows that U of the transistor is just slightly larger than its G_{ma} in a limited frequency range (271-352 GHz). In practice, the loss of the embedding reduces the power gain of the unilateralized transistor well below the theoretical U in this frequency range.

2.3. Maximum Achievable Gain (G_{max})

Maximum achievable gain (G_{max}) is the maximum G_{ma} of an LLR embedded A2P. In other words, if we embed an A2P by a tunable LLR embedding and match the input and output of the resulting two-port, as shown in Fig. 2.4, G_{max} is the maximum power gain, and is given as [**52**]:

$$G_{max} = (2U - 1) + 2\sqrt{U(U - 1)}. \tag{2.3}$$

This equation depicts that G_{max} is only a function of U and similar to U, is an inherent characteristic of any A2P. In addition, $G_{max} \approx 4U$ (6 dB larger than U) when $U \gg 1$. This can be clearly seen in Fig. 2.2(a). This difference is more important at submillimeter-wave and THz frequencies where G_{ma} and U of the A2P drop significantly. It shows that boosting the power gain to G_{max} is a promising solution to high-gain amplifier design at frequencies near f_{max}.

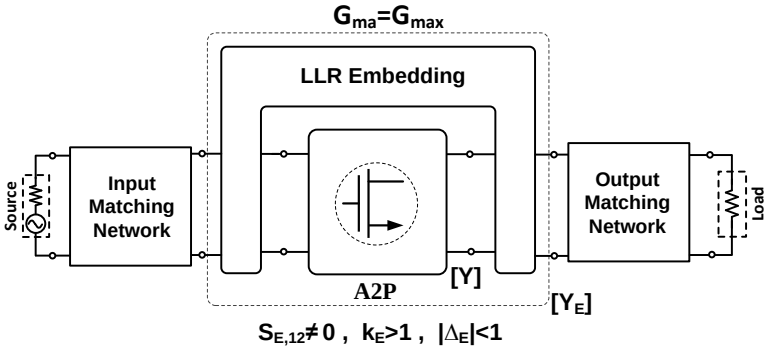


FIGURE 2.4. An LLR embedding that increases G_{ma} to G_{max}. The embedded A2P is unconditionally stable.

CHAPTER 3

T-Embedding: A General Solution to Reach G_{max}

In this chapter, a general LLR embedding called T-embedding is proposed by which G_{ma} of the LLR-embedded A2P is boosted exactly to G_{max}. To this end, G_{ma} of a two-port is described as a function of its U and A, and gain-plane is defined accordingly. LLR embedding is then interpreted as a movement in the gain-plane, and by an appropriate movement, G_{ma} is boosted to G_{max}.

3.1. Gain-Plane and Maximum G_{ma}

G_{ma} of a two-port can be written as a function of its U and A as [**52**]:

$$\frac{G_{ma}}{U} = \left| \frac{A - G_{ma}}{A - 1} \right|^2, \tag{3.1}$$

which suggests that we can change G_{ma} by changing A and/or U. To minimize the added loss to the network and to take advantage of a constant U, LLR embeddings are chosen to change G_{ma}. Thus U is constant, and the problem of finding an LLR embedding that maximizes G_{ma} can be reduced to finding an LLR embedding that changes A in such a way that maximizes G_{ma} in (3.1) to reach G_{max}. For the sake of brevity, "LLR embedding" is reduced to "embedding" in the rest of this paper.

As defined in (2.1), A is a complex number, while G_{ma} and U both are positive real numbers. Accordingly, G_{ma} of an embedded A2P is a function of two variables: the real part of A, and the imaginary part of A (U is constant). Assuming $|A| \gg 1$, (3.1) can be simplified to

$$\frac{U}{G_{ma}} = \left(Re\left(\frac{U}{A}\right) - \frac{U}{G_{ma}} \right)^2 + \left(Im\left(\frac{U}{A}\right) \right)^2. \tag{3.2}$$

The derivation of (3.2) is shown in Appendix A. This equation describes locus of a group of equi-gain circles in a plane whose horizontal axis is $Re\left(\frac{U}{A}\right)$ and vertical axis is $Im\left(\frac{U}{A}\right)$. This plane is called gain-plane. Each circle has a center at $\left(\frac{U}{G_{ma}}, 0\right)$ and a radius of $\sqrt{\frac{U}{G_{ma}}}$. These circles are plotted in Fig. 3.1 for $G_{ma} = U$, $2U$, $3U$, and an arbitrary value less than U. It will be shown that only an arc of each circle is acceptable as an equi-gain locus. Thus, the first three equi-gain circles are reduced to their acceptable arcs in Fig. 3.1. Each two-port corresponds to a coordinate in the gain-plane based on its U and A. The position of the 10 μm common-source NMOS transistor is shown in Fig. 3.1 as a black dot. Changing A by applying an embedding moves the corresponding point in the gain-plane. This interpretation will be used to boost G_{ma} to G_{max}.

The basic limitation on the equi-gain arcs is stability. To find the stable region, (3.1) can be used in conjunction with inequality $K > 1$. The boundary that represents $K = 1$ is a parabola when $|A| \gg 1$. The equation that expresses the parabola in the gain-plane is

$$\left(Im\left(\frac{U}{A}\right)\right)^2 = Re\left(\frac{U}{A}\right) + 1/4. \tag{3.3}$$

The inside and outside regions of this parabola correspond to $K > 1$ and $K < 1$, respectively. Although $|\Delta|$ satisfies the stability criteria in most practical applications, it must be checked to guarantee unconditional stability inside of the parabola.

Each circle in Fig. 3.1 is tangential to this parabola at two points. These points split each circle into two arcs: the left arc, and the right arc. Only the left arc of each circle is acceptable as a locus of equi-gain coordinates. Moving from a tangential point on an arbitrary circle, increases K from 1. Therefore, on the right arc, $K - \sqrt{K^2 - 1}$ and $|A|$ decrease simultaneously (K and $\left|\frac{U}{A}\right|$ both increase). Referring to (2.1), this simultaneous decrease, reduces G_{ma}, and hence the right arcs do not represent locus of constant G_{ma}, and hence is not acceptable.

Fig. 3.1 illustrates that as G_{ma} increases, the corresponding equi-gain arc moves to the left

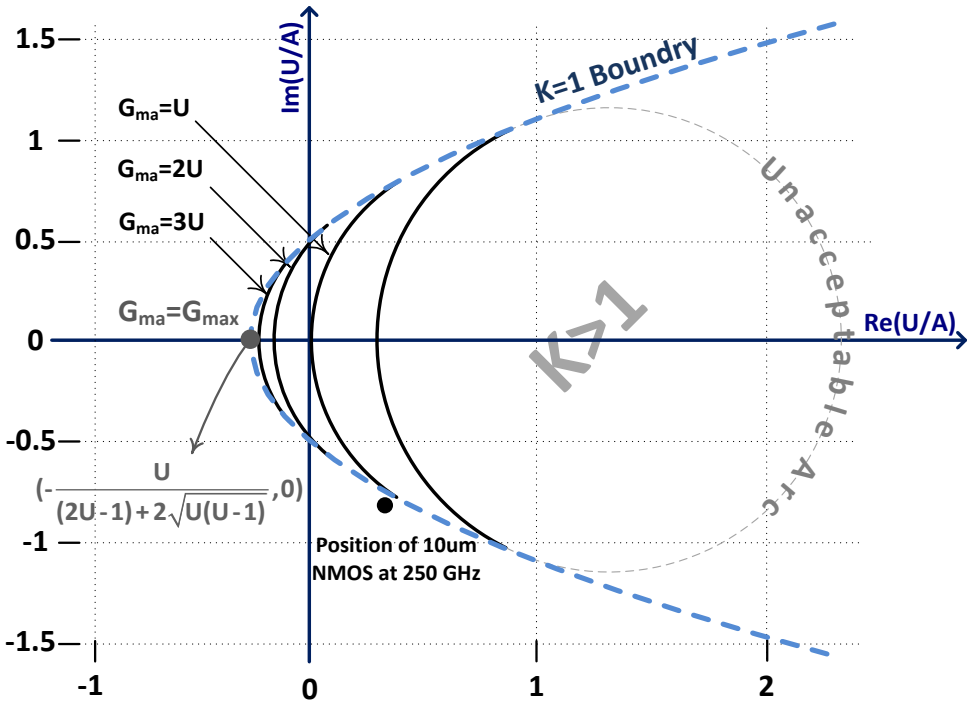
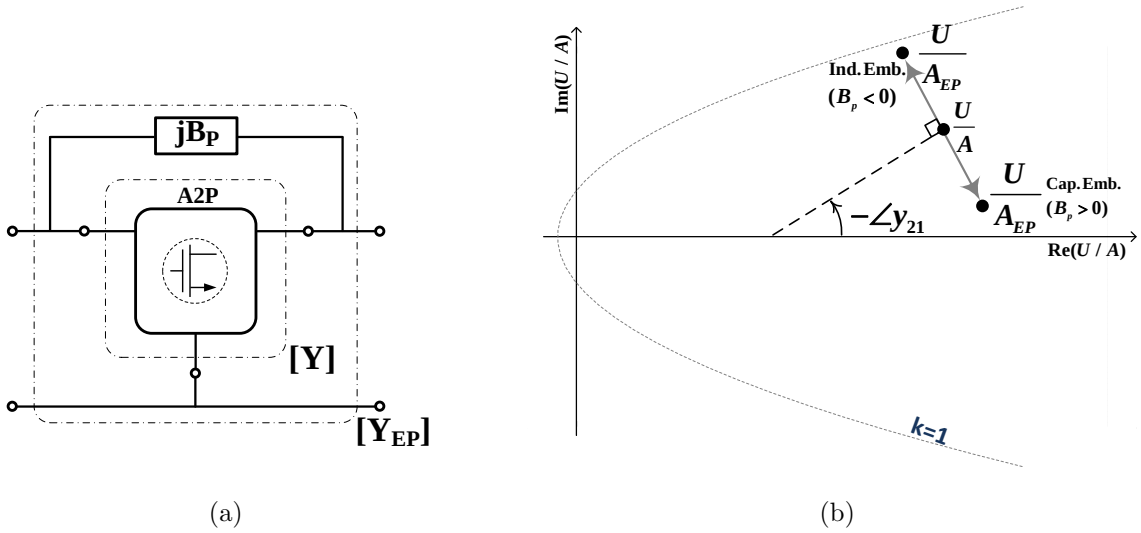


FIGURE 3.1. Gain-plane and the constant G_{ma} arcs inside of $K > 1$ region. U is constant everywhere in the gain-plane.

in the gain-plane, hence the coordinate that corresponds to the maximum G_{ma} is $\left(-\frac{1}{4}, 0\right)$ assuming $|A| \gg 1$, and is shown by a gray dot in Fig. 3.1. G_{ma} at this point is equal to $4U$, and therefore $G_{max} = 4U$. However, this number is an approximation since (3.2) and (3.3) are found assuming $|A| \gg 1$. To find the exact value of G_{max}, (3.1) should be simplified using the following two conditions at G_{max}: $Im(A) = 0$ and $K = 1$. The resulting equation is shown in (2.3), and therefore the exact coordinate of the point that corresponds to $G_{ma} = G_{max}$ is $\left(-\frac{U}{(2U-1)+2\sqrt{U(U-1)}}, 0\right)$ as shown in Fig. 3.1.

It must be noted that as the frequency increases and becomes closer to f_{max}, U and $(2U-1)+2\sqrt{U\,(U-1)}$ both decrease and become closer to unity. Therefore, as the frequency goes up, the assumption of $|A| \gg 1$ is not correct anymore, and the point that corresponds to G_{max} deviates from $(-\frac{1}{4},0)$, moves to the left, and reaches (-1,0) at f_{max}.



(a) (b)

FIGURE 3.2. (a) An A2P embedded by a parallel inductor or capacitor (b) The movements caused by these embeddings in the gain-plane.

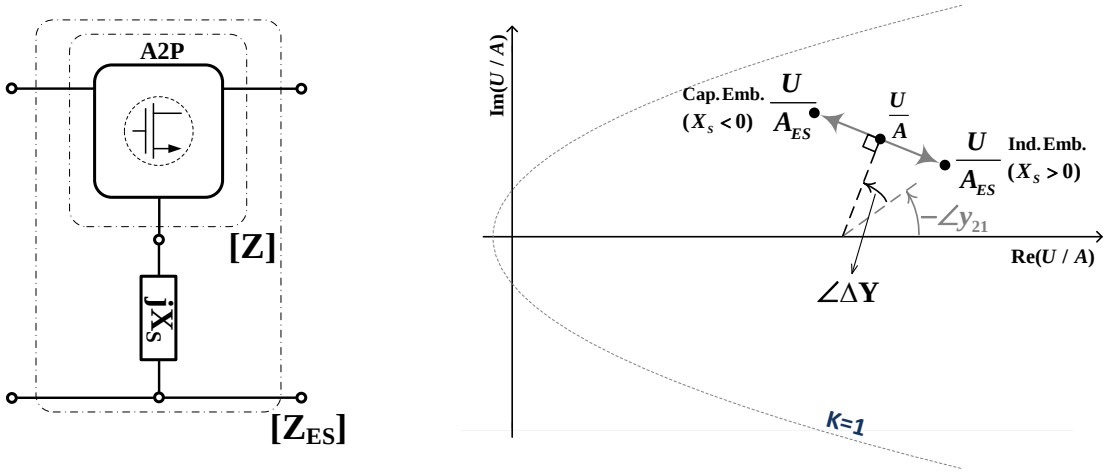
3.2. Movement in the Gain-Plane and T-embedding

After locating the exact coordinate of the point that corresponds to G_{max} in the gain-plane, the next step is finding an embedding that causes a movement from the coordinate of the A2P to that of G_{max}. This movement provides us with two numbers: one is the change in the real part of A, and the other is the change in the imaginary part of A. These two numbers will be used to find the embedding that boosts G_{ma} to G_{max}. Here, we study two embeddings, called parallel and series embeddings, and the movements that they cause.

Fig. 3.2(a) shows the parallel embedding. The embedding is done by adding a passive element with an admittance of jB_P between the input and output terminals of the A2P. It can be simply shown that

$$\mathbf{Y_{EP}} = \mathbf{Y} + \begin{bmatrix} jB_P & -jB_P \\ -jB_P & jB_P \end{bmatrix}, \tag{3.4}$$

where $\mathbf{Y}$ and $\mathbf{Y_{EP}}$ are the admittance matrices of the A2P and embedded A2P, respectively. To calculate the movement caused by this embedding, we need to find the coordinate of the



(a) (b)

FIGURE 3.3. (a) An A2P embedded by a series inductor or capacitor (b) The movements caused by these embeddings in the gain-plane.

embedded A2P. Assuming $|B_P| \ll |Y_{21}|$, the coordinate is

(3.5)

According to (3.5), for small values of B_P, the magnitude of this movement is $U \cdot \left|\frac{B_P}{Y_{21}}\right|$, and its phase is $\pm\frac{\pi}{2} - \angle Y_{21}$. For an inductive parallel embedding ($B_P < 0$), the phase of the movement is $+\frac{\pi}{2} - \angle Y_{21}$, and when it is capacitive ($B_P > 0$), the phase is $-\frac{\pi}{2} - \angle Y_{21}$. These movements are shown in Fig. 3.2(b) for an arbitrary $\mathbf{Y}$ and B_P.

Fig. 3.3(a) shows the series embedding. The embedding is done by adding a passive element with an impedance of jX_S in series with the common terminal of the A2P. $\mathbf{Z}$ (or $\mathbf{Y^{-1}}$) and $\mathbf{Z_{ES}}$ are the impedance matrices of the A2P and the embedded A2P, respectively. It can be shown that the impedance matrix of the embedded A2P is

$$\mathbf{Z_{ES}} = \begin{bmatrix} \frac{Y_{22}}{\Delta Y} + jX_S & \frac{-Y_{12}}{\Delta Y} + jX_S \\ \frac{-Y_{21}}{\Delta Y} + jX_S & \frac{Y_{11}}{\Delta Y} + jX_S \end{bmatrix}, \quad \text{where } \Delta Y \text{ is} \quad \Delta Y = Y_{11} \cdot Y_{22} - Y_{12} \cdot Y_{21}. \tag{3.6}$$

Assuming $|X_S| \ll \left|\frac{Y_{21}}{\Delta Y}\right|$, the coordinate of the embedded A2P by the series embedding in

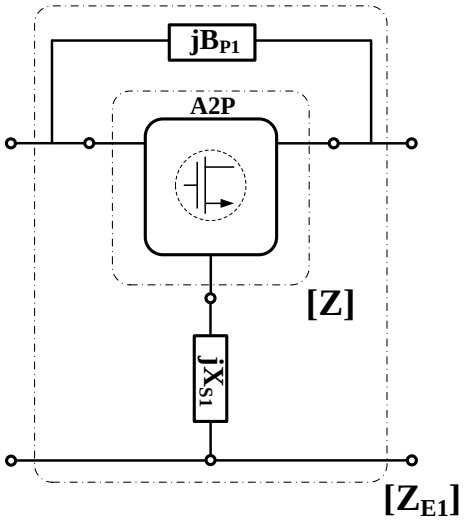
the gain-plane is

$$\frac{U}{A_{ES}} \simeq \frac{U \cdot Y_{12}}{Y_{21}} - \frac{jX_S \cdot \Delta Y}{Y_{21}} = \frac{U}{A} - \frac{jX_S \cdot \Delta Y \cdot U}{Y_{21}}. \tag{3.7}$$

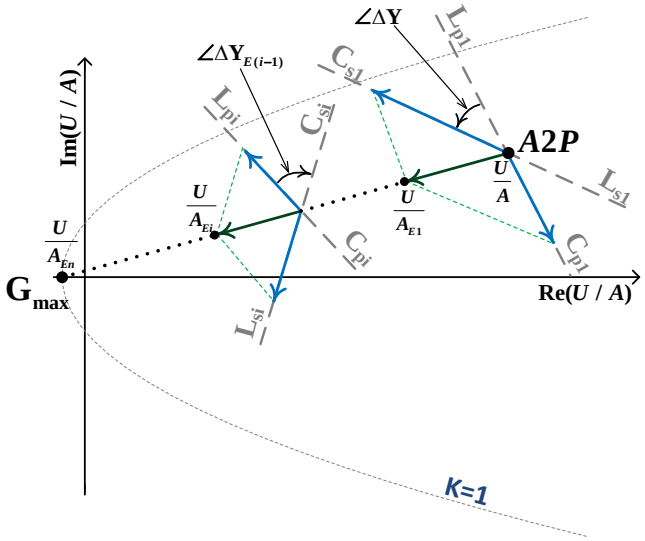
The amplitude of the movement is $\left|\frac{X_S \cdot \Delta Y \cdot U}{Y_{21}}\right|$, and its phase is $\pm\frac{\pi}{2} - \angle Y_{21} + \angle \Delta Y$. Plus and minus signs are for capacitive and inductive embeddings, respectively. These movements are illustrated in Fig. 3.3(b) for an arbitrary $\mathbf{Y}$ and X_S. The phases of the movements in this case are different from that of the parallel embedding by $\angle \Delta Y$. This phase difference makes it possible to select any arbitrary direction for the movement in the gain-plane when both parallel and series embeddings are applied to A2P. This feature proves useful when considering the fact that the coordinate of the A2P can be anywhere in the gain-plane.

The superposition of the movements caused by these embeddings results in an omni-directional movement in the gain-plane. Shown in Fig. 3.4(a) is the A2P embedded simultaneously by parallel and series embeddings, and Fig. 3.4(b) shows the movement due to these simultaneous embeddings. In Fig. 3.4(b), L and C specify whether the embeddings are inductive or capacitive, and the subscripts p and s represent whether the embedding is parallel or series, respectively. In this figure, the coordinate of the A2P is $\frac{U}{A}$, which is the starting point of the movement toward G_{max}. The figure depicts that by a correct choice of B_{P1} and X_{S1}, a small movement is feasible toward any arbitrary point in the gain-plane, including G_{max}, independent of the A2P coordinate. As shown in the figure, the embedded A2P has moved to a new point, $\frac{U}{A_{E1}}$, toward the coordinate of G_{max}.

However, these movements are relatively small to satisfy the assumptions behind our derivations. Therefore, multiple small movements should be made to reach G_{max} exactly. Fig. 3.4(b) also shows the movement due to the ith embedding. Since the starting point of this movement is different from the original A2P, the required embedding to have the same movement in the same direction will be different. This fact is graphically illustrated in this figure. For example, if the first movement needed two capacitors, the ith movement may need two



(a)

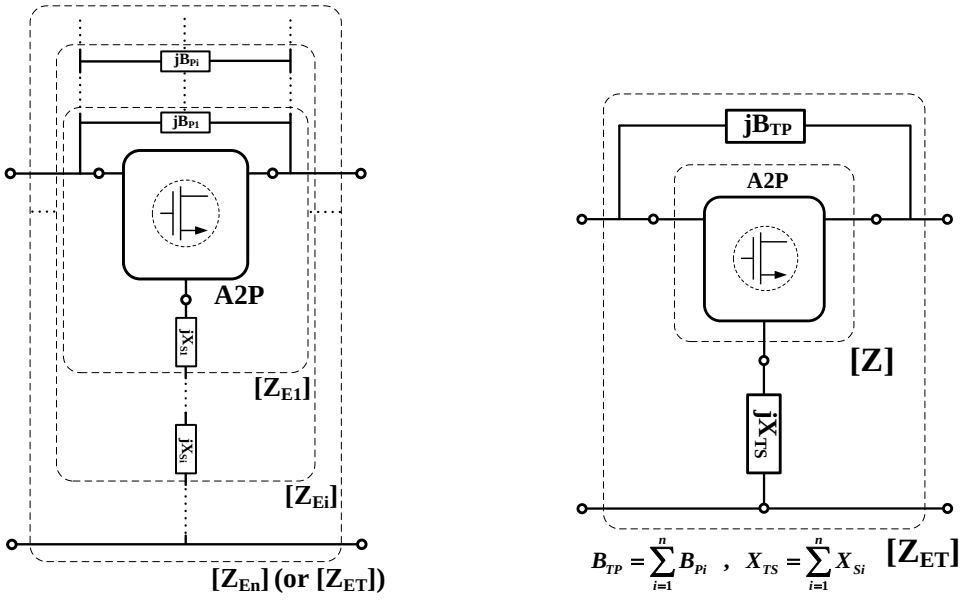


(b)

FIGURE 3.4. (a) An A2P embedded by parallel and series embeddings simultaneously. (b) The movement due to B_{P1} and X_{S1} is toward the coordinate of G_{max}. The movement can be done n times to reach G_{max}.

inductors to move toward G_{max}.

By a large number of small movements (n times), the coordinate of the starting point, the



(a) (b)

FIGURE 3.5. (a) An A2P embedded n times by parallel and series embeddings. (b) The embeddings are combined and simplified to two embedding elements B_{TP} and X_{TS}.

coordinate of A2P, can be changed to that of G_{max}. These movements correspond to n different embeddings and are shown in Fig. 3.5(a). As shown in the figure, by combining all the small embeddings we arrive at one single parallel and series passive element that boost the gain to G_{max}. B_{TP} and X_{TS} are the sum of B_{Pi}'s and X_{Si}'s, respectively. In the next section, the elements of this T-shape embedding, B_{TP} and X_{TS}, are derived as a function of the Y-parameters of the A2P.

3.3. T-Embedding: Elements Deriviation and Verification

To derive the embedding elements B_{TP} and X_{TS} shown in Fig. 3.5(b), $\mathbf{Z_{ET}}$, the impedance matrix of the final embedded A2P, is calculated using B_{TP}, X_{TS}, and the Z-parameters of the A2P. Next, A of the embedded A2P, A_{ET}, is found from $\mathbf{Z_{ET}}$. From the gain-plane, the

following conditions are required at G_{max}:

$$Re(\frac{U}{A_{ET}}) = -(\frac{U}{G_{max}}) \quad \& \quad Im(\frac{U}{A_{ET}}) = 0. \tag{3.8}$$

After applying these conditions to A_{ET}, X_{TS} and B_{TP} are obtained as:

$$X_{TS} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}, \quad B_{TP} = -\frac{R_{21} + G_{max}R_{12}}{(1 + G_{max}(Im(\Delta Z) + X_{TS}M))}, \tag{3.9}$$

where

(3.10)

$$a = (1 + G_{max})M, \quad b = (X_{21} + G_{max}X_{12})M + (R_{21} + G_{max}R_{12})N + (1 + G_{max})Im(\Delta Z),$$

$$c = (R_{21} + G_{max}R_{12})Re(\Delta Z) + (X_{21} + G_{max}X_{12})Im(\Delta Z),$$

and

(3.11)

$$\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21}, \quad M = R_{11} + R_{22} - R_{12} - R_{21}, \quad N = X_{12} + X_{21} - X_{11} - X_{22},$$

$$Z_{ij} = R_{ij} + jX_{ij} \quad \& \quad i, j = 1, 2.$$

Z_{ij} are the elements of impedance matrix of the A2P. The complete derivation of (3.9)−(3.11) is given in Appendix A. These equations show that only the Z-parameters of the A2P are used to calculate B_{TP} and X_{TS}. Although the square root term in (3.9), $b^2 - 4ac$, is positive for most transistors, for the rare cases that it is less than zero, it can be made positive using pre-embedding, which is discussed in Chapter 4.

Reaching any arbitrary G_{ma} up to G_{max} can be done using the proposed embedding as well. From a stability viewpoint, the crossing point of the equi-gain arc and the horizontal axis is targeted to reach a G_{ma}. It can be shown that to reach such a point (e.g., G_{ma}), we only need to substitute the G_{max} term in (3.9) and (3.10) with $U \cdot \left(\sqrt{\frac{U}{G_{ma}}} - \frac{U}{G_{ma}}\right)^{-1}$. The proposed technique guarantees that after embedding $K > 1$. The embedding process is independent

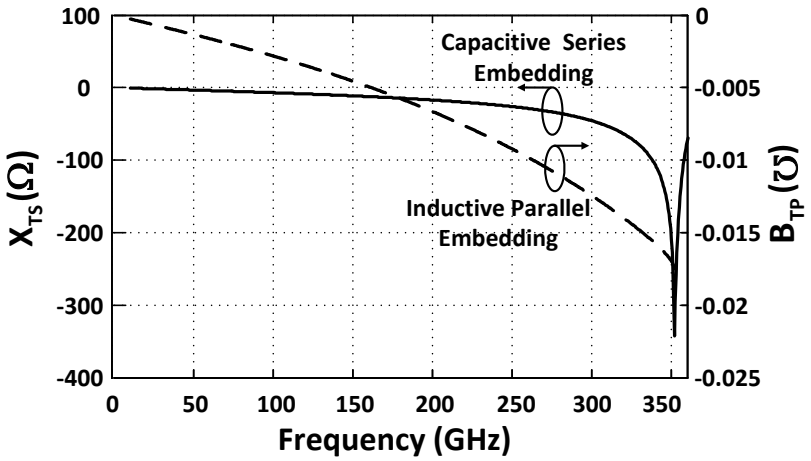
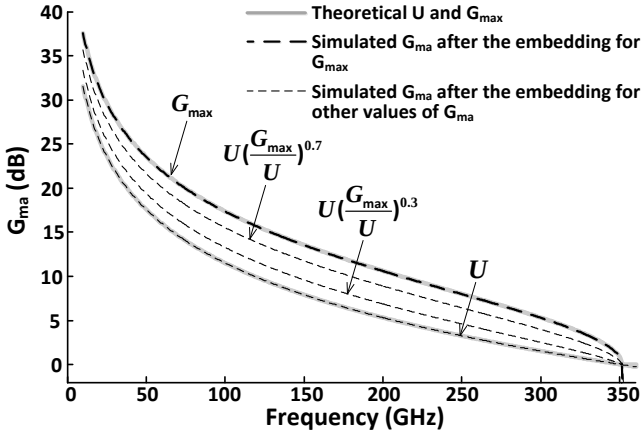


FIGURE 3.6. Calculated B_{TP} and X_{TS} for the 10μm common-source transistor to achieve G_{max}.

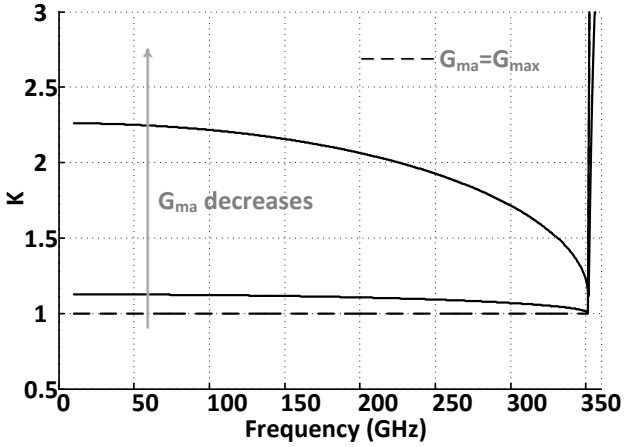
of $|\Delta|$, and it has to be less than one only after embedding to make certain the amplifier is unconditionally stable. Therefore, the value of $|\Delta|$ has to be checked after embedding. In practice, one of the two solutions in (3.9) results in an unconditionally stable amplifier. The embedding has been applied to several A2P's, including BJT and CMOS transistors with various sizes and pin arrangements. In all of these cases, $|\Delta|$ is always smaller than one.

To verify the proposed embedding, the same 10 μm common-source NMOS transistor is used as the A2P. Using its Z-parameters, the embedding elements of T-embedding, B_{TP} and X_{TS}, are calculated to reach G_{max} at all frequencies. These values are shown in Fig. 3.6. Fig. 3.7(a) shows the simulated G_{ma} of the transistor embedded by B_{TP} and X_{TS} shown in Fig. 3.6 to reach G_{max} (the thick black dashed line). It can be seen that T-embedding boosts the G_{ma} to the theoretical G_{max}. For the same transistor, and using the corresponding embeddings, G_{ma} is also boosted to U, $U \cdot \left(\frac{G_{max}}{U}\right)^{0.3}$, and $U \cdot \left(\frac{G_{max}}{U}\right)^{0.7}$. Here, for all the simulations, minus sign is selected in (3.9) as it leads to $|\Delta| < 1$. Fig. 3.7(b) and Fig. 3.7(c) show the simulated stability measures of the embedded transistors versus frequency. Circuit simulation is done to verify T-embedding properties. To perform circuit simulation, the embedding elements B_{TP} and X_{TS} are calculated at two frequencies (150

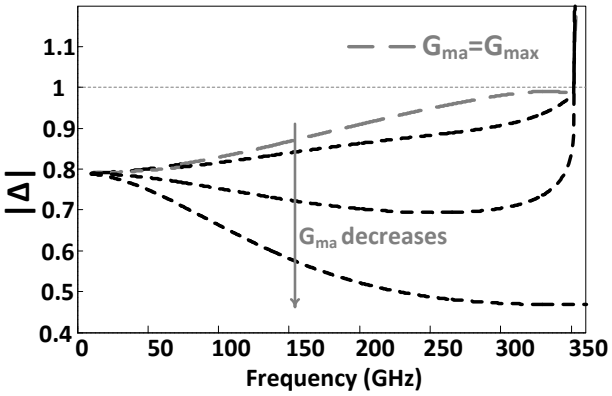
GHz and 250 GHz) for three different values of G_{ma} (U, $U \cdot \left(\frac{G_{max}}{U}\right)^{0.5}$, and G_{max}). The equivalent inductances or capacitances of B_{TP} and X_{TS} are calculated and given in Fig. 3.8. The transistor is embedded by the resulting capacitors and inductors, and G_{ma}'s of the embedded A2P's are simulated. The simulation results and the calculated values shown in Fig. 3.8 are in perfect agreement.



(a)

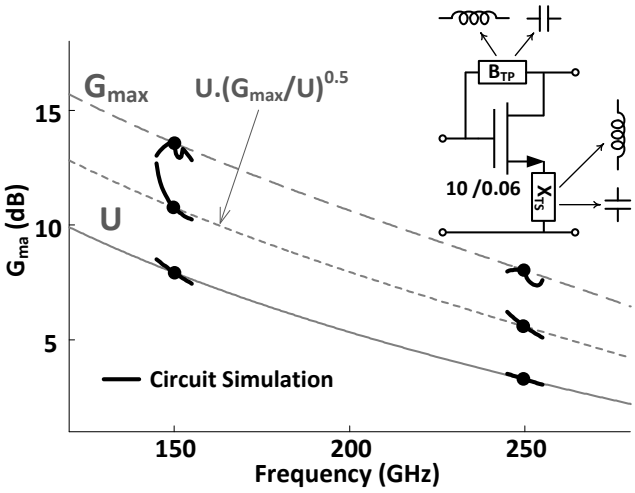


(b)



(c)

FIGURE 3.7. (a) Theoretical and simulated G_{ma}'s for the same 10 μm transistor embedded by T-embedding. (b) corresponding K's. (K of $G_{ma} = U$ is infinity) (c) corresponding $|\Delta|$'s.



Freq. \ G_{ma}	U	$U.(U/G_{max})^{0.5}$	Gmax
150 GHz	B_{TP}: L= 308.30 pH X_{TS}: L= 8.39 pH	B_{TP}: L= 245.90 pH X_{TS}: C= 175.52 fF	B_{TP}: L= 232.80 pH X_{TS}: C= 93.39 fF
250 GHz	B_{TP}: L= 127.06 pH X_{TS}: L= 5.02 pH	B_{TP}: L= 77.42 pH X_{TS}: C= 52.36 fF	B_{TP}: L= 68.95 pH X_{TS}: C= 24.32 fF

FIGURE 3.8. Theoretical and circuit simulation results comparison of three different G_{ma}'s of the same 10 μm embedded transistor at 150 GHz and 250 GHz.

CHAPTER 4

Practical Design Considerations and Implemented 260GHz CMOS Amplifier

4.1. Power Flow in a Gain-Boosted Amplifier

Fig. 4.1(a) shows a quantitative illustration of the power flow in a generic gain-boosted embedded A2P where P_f is the feedback power via the T-embedding. In such a situation, the power gain of the A2P ($P_{out,D}/P_{in,D}$) can be much smaller than the power gain of the amplifier (P_{out}/P_{in}). This is evident from the power gain derivation shown below:

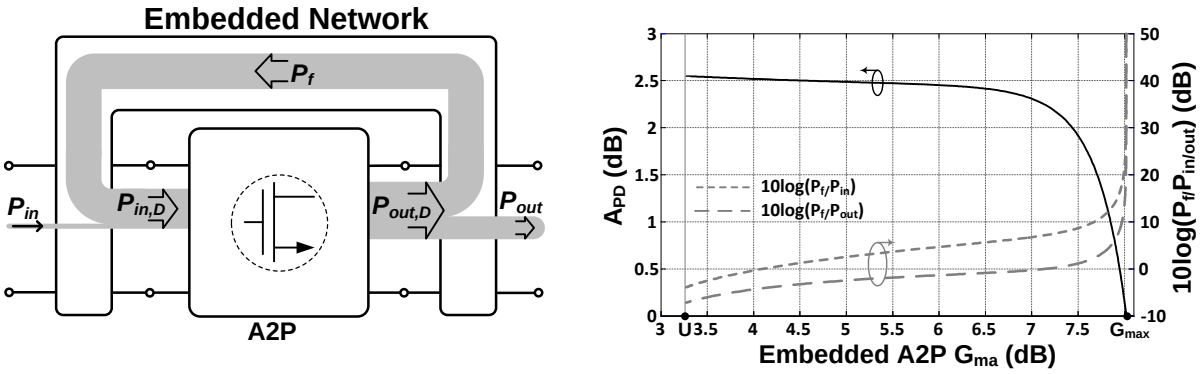
$$A_{PD} = \frac{P_{out,D}}{P_{in,D}} = \frac{P_{out} + P_f}{P_{in} + P_f} = \frac{\frac{P_{out}}{P_{in}} + \frac{P_f}{P_{in}}}{\frac{P_{in}}{P_{in}} + \frac{P_f}{P_{in}}} = \frac{G_{ma} + \frac{P_f}{P_{in}}}{1 + \frac{P_f}{P_{in}}}. \tag{4.1}$$

Here P_{in}, P_{out}, and P_f are the input power and output power of the embedded A2P, and the feedback power via T-embedding, respectively. $P_{in,D}$ and $P_{out,D}$ are the input and output power of the A2P, respectively.

In the right-hand side of (4.1), P_f and P_{in} are both positive numbers. Therefore, for any $G_{ma} > 1$, it can be simply shown that $A_{PD} < G_{ma}$. The larger the ratio P_f/P_{in} is, the bigger the difference between A_{PD} and G_{ma} will be. Simulated P_f/P_{in}, P_f/P_{out}, and A_{PD} are plotted versus G_{ma} in Fig. 4.1(b) for the same embedded 10 μm common-source NMOS transistor at 250 GHz. As G_{ma} gets closer to G_{max}, P_f/P_{in} and P_f/P_{out} increase, and at $G_{ma} = G_{max}$, they become very large. A very large P_f/P_{in} results in $A_{PD} \simeq 1$ based on (4.1), when $G_{ma} = G_{max}$. Plotted in Fig. 4.1(b), the simulated A_{PD} goes to 0 dB as it is expected. This means in practice due to high feedback power, boosting the gain to exactly G_{max} may not be feasible. This is because the high power flow in real embedding elements results in high power loss which significantly reduces the overall power gain. However, it is

practical to get reasonably close to G_{max} as shown in Fig. 4.1(b).

One may speculate that the feedback power through T-embedding network degrades the linearity of the embedded A2P by decreasing its input 1-dB compression point. However, the linearity of an embedded amplifier is a function of several parameters including the input power of A2P as well as the impedances seen by the input and output ports of the A2P. Since the proposed gain boosting technique changes the impedance seen by the input and output ports of A2P, it cannot be concluded that gain boosting necessarily degrades linearity. For example, a 10 μm common source NMOS transistor is simultaneously matched to the source and load at 260 GHz where it is unconditionally stable, and features a G_{ma} of 3.3 dB. As shown in Fig. 4.2, its simulated input and output 1-dB compression points are -8.5 dBm and -6.2 dBm, respectively. Then, the transistor is embedded using T-embedding to boost G_{ma} to 6 dB at 260 GHz. In this case, the simulated input and output 1-dB compression points are -7.95 dBm and -2.95 dBm, respectively. This shows that the linearity has improved after gain boosting, verifying that linearity does not necessarily degrade with gain boosting.



(a) (b)

FIGURE 4.1. (a) A quantitative illustration of the power flow in a gain-boosted embedded A2P. (b) the input and output powers normalized to the feedback power and A2P power gain of the same 10 μm transistor at 250 GHz.

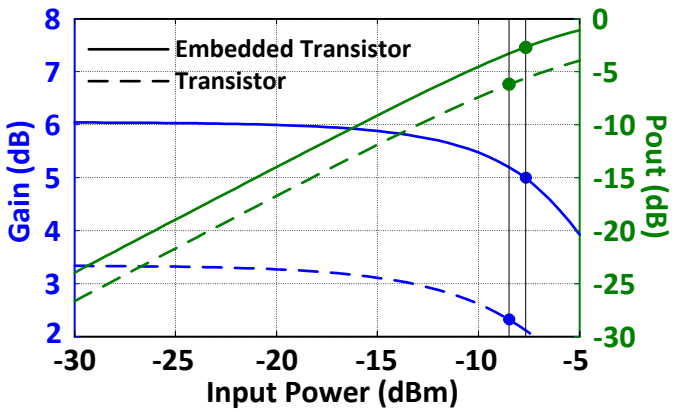


FIGURE 4.2. Maximum available gain and 1-dB compression point of a 10 μm NMOS transistor with/without embedding at 260 GHz.

4.2. Effect of the Matching Loss on the Maximum Power Gain

T-embedding feeds back a part of output power of the A2P to its input. This in turn reduces the real part of the input impedance of the embedded A2P. Accordingly, an embedded A2P with higher G_{ma} has a smaller input resistance. Assuming a constant load and source, reduction in the real part of the input impedance increases the resistance transformation ratio. The loss of a matching network is worse when the resistance transformation ratio is higher. Therefore, there must be an optimum G_{ma} that maximizes the total power gain from the source to the load (G_T).

To investigate this effect and find the optimum value of G_{ma}, the total gain which includes the input and output matching networks losses is calculated. Here, we assume the matchings are done using an L-match structure that consists of a capacitor and an inductor. The quality factor of the inductors is neglected as inductors at millimeter-wave and THz frequencies have much higher quality factors than capacitors. It can be shown that the power efficiency of an L-match network, η, is [**20**]:

$$\eta_{in/out} = 1 - \frac{\sqrt{T_{in/out} - 1}}{Q_C}, \tag{4.2}$$

where Q_C is the quality factor of the capacitor used in the matching networks. T is the resistance transformation ratio and is given as

$$T_{in/out} = \frac{R_{port}}{R_0} \quad if \quad R_{port} > R_0, \quad T_{in/out} = \frac{R_0}{R_{port}} \quad if \quad R_{port} < R_0. \tag{4.3}$$

For the input matching network (T_{in}), R_{port} is the input resistance of the embedded A2P, and R_0 is the source resistance. For the output matching network (T_{out}), R_{port} is the output resistance of the embedded A2P and R_0 is the load resistance. Supposing η_{in} and η_{out} are the power efficiencies of the input and output matching networks respectively, the total power gain, G_T, can be written as:

$$G_T = \eta_{in} \cdot G_{ma} \cdot \eta_{out}, \tag{4.4}$$

η_{in} and η_{out} are functions of the resistance transformation ratios, T_{in} and T_{out} respectively, and these resistance transformation ratios change when G_{ma} changes. Hence, η_{in} and η_{out} both are functions of G_{ma}. Accordingly, for a given source, load, and capacitor quality factor, G_T is only a function of G_{ma}.

G_{ma} of an embedded A2P is swept from U to G_{max} by changing the embedding. The total power gain, G_T, is then plotted versus G_{ma} of the embedded A2P for three different Q_C's in Fig. 4.3. The A2P is selected to be the same 10 μm transistor. It can be seen, for $Q_C = 5$, the optimum G_{ma} is 6.8 dB, which is very different from G_{max}.

4.3. Pre-embedding

In practice, the calculated T-embedding may impose some limitations in terms of loss or DC bias and/or isolation on the embedded A2P. For example, Fig. 3.6 shows that the series embedding of the 10 μm common-source NMOS transistor is a capacitor at 250 GHz, which can be very lossy. Moreover, this mandates the need for a bypass inductor for DC current, which is also very lossy. To overcome this issue, it is desirable to remove the

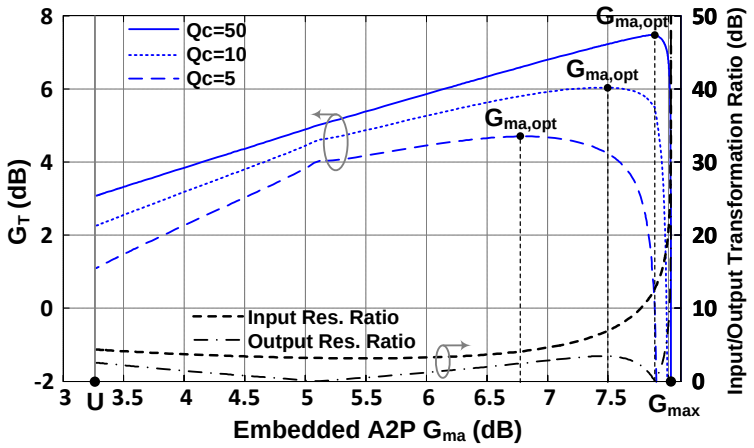


FIGURE 4.3. Input/Output resistance transformation ratio ($10 \times log_{10}(T_{in/out})$), and the total power gain (G_T) versus G_{ma} of the emebedded transistor.

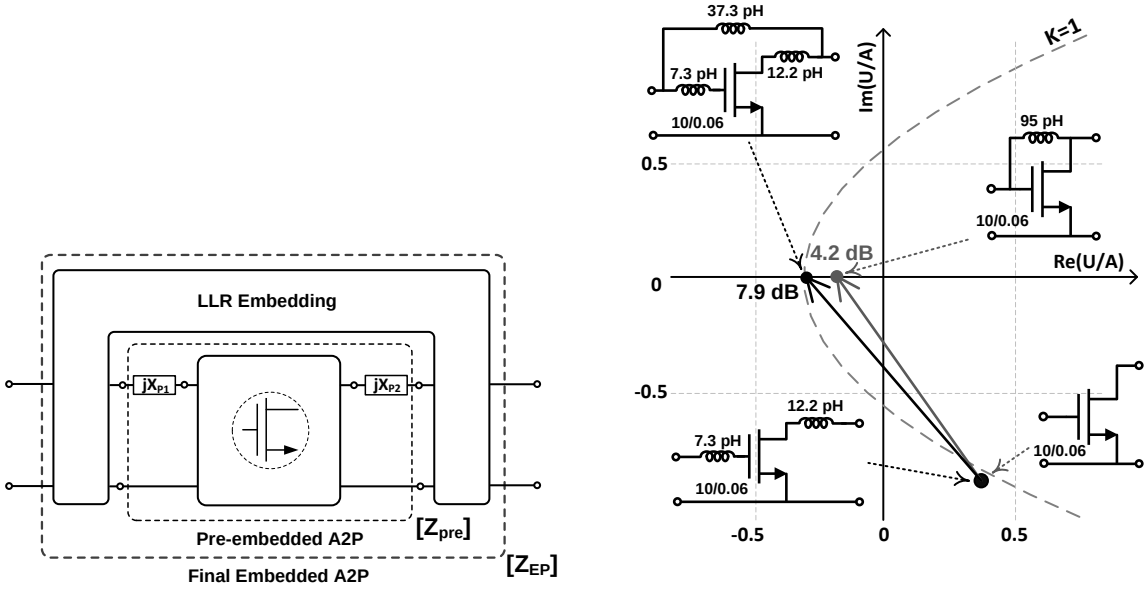
capacitor. To do so, pre-embedding can be used. As shown in Fig. 4.4(a), for the 10 μm transistor, the pre-embedding is selected to consist of two passive elements jX_{P1} and jX_{P2}. The pre-embedding shown in this figure does not alter A and hence does not change the coordinate of the two-port in the gain plane. However, it changes the direction of the movement by the same embedding element. Using (3.7), it can be shown that the direction of the movement changes by $\Delta\varphi = \angle\Delta Z - \angle\Delta Z_{pre}$, where ΔZ and ΔZ_{pre} are the determinants of the impedance matrices of the A2P and the pre-embedded A2P, respectively.

To verify the pre-embedding shown in Fig. 4.4(a), the series capacitor is removed and the transistor is embedded by parallel embedding with and without pre-embedding. The movements with and without pre-embedding are shown in Fig. 4.4(b). The figure illustrates that the final power gain is 3.7 dB lower if the pre-embedding is not used. The transistor with pre-embedding reaches almost G_{max} of 8 dB at 250 GHz.

4.4. Implemented Amplifier and Measurement Results

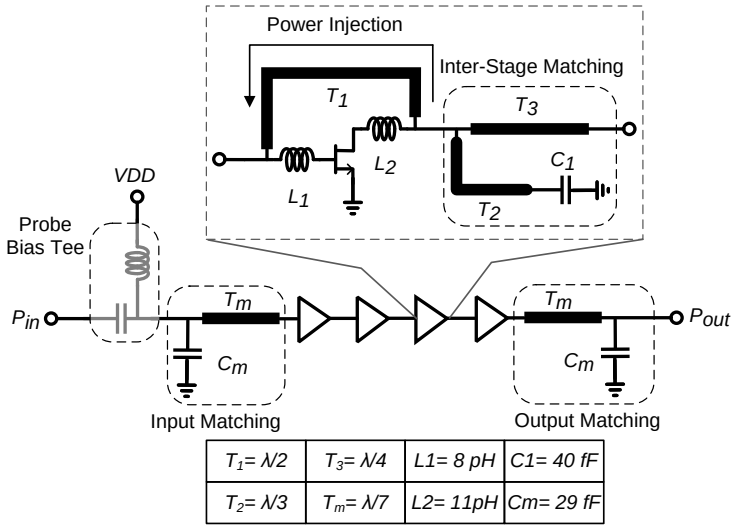
To show the feasibility of the proposed embedding in boosting G_{ma}, a four-stage embedded amplifier is fabricated in 65 nm CMOS technology at 260 GHz. To increase f_{max}, two

5 μm NMOS transistors are used in parallel to achieve an f_{max} of 352 GHz, and they are used as the core of the embedded amplifier stages. Fig. 4.5 shows the circuit schematic of the proposed four-stage embedded amplifier. G_{ma} and G_{max} of this transistor are 3.6 dB and 7.5 dB at 260 GHz, respectively. Simulations show that the series embedding that is needed to reach G_{max} is capacitive, and it is desirable to eliminate it and use pre-embedding as discussed in Chapter 4. To boost G_{ma} to 7.4 dB at 260 GHz, the loss-less pre-embedding elements, X_{P1} and X_{P2}, and the parallel embedding are found to be 7 pH, 12.3 pH, and 37.5 pH, respectively. Shown in Fig. 4.5, the real pre-embedding elements are lossy, and hence slightly different from the calculated loss-less elements. The parallel embedding T_1 is implemented using a microstrip transmission line and behaves as a 50 pH inductor in the circuit. The pre-embedding along with T_1 boosts G_{ma} to 6 dB, which is 2.4 dB higher than G_{ma} of the transistor.



(a) (b)

FIGURE 4.4. (a) A2P pre-embedded by X_{P1} and X_{P2}. (b) gain boosting with/without pre-embedding when the series capacitor is removed.



T_1= λ/2	T_3= λ/4	L1= 8 pH	C1= 40 fF
T_2= λ/3	T_m= λ/7	L2= 11pH	Cm= 29 fF

FIGURE 4.5. Circuit schematic of the proposed four-stage embedded amplifier for maximum gain-boosting.

In this design, input/output matching and inter-stage matchings introduce loss of 1.8 dB and 3.6 dB, respectively. Therefore, the total simulated power gain of the amplifier is 9.6 dB. All of the components that are used for embedding and impedance matching are implemented using microstrip transmission lines and metal-oxide-metal (MOM) capacitors.

As shown in Fig. 6.11a, the amplifier has a maximum measured small-signal gain of 9.2 dB at 257 GHz and input and output reflection coefficients of -5.5 dB and -8.5 dB, respectively. Fig. 4.7 illustrates that the proposed amplifier is unconditionally stable in simulation and measurement. The chip consumes 27.6 mW of power from 1 V supply in Figs. 6.11a and 4.7.

Fig. 4.8 displays the setup that is used for large-signal measurements. As shown in Fig. 4.9, at 255 GHz the maximum PAE is 1.35% with VDD=0.8 V, and the maximum output saturated power (P_{sat}) is -3.9 dBm with VDD=1 V. The amplifier consumes 13.7 mW and 27.6 mW at VDD=0.8 V and VDD=1 V, respectively. Fig. 4.10 shows the simulation and measurement results of saturation power as a function of frequency when VDD=1 V.

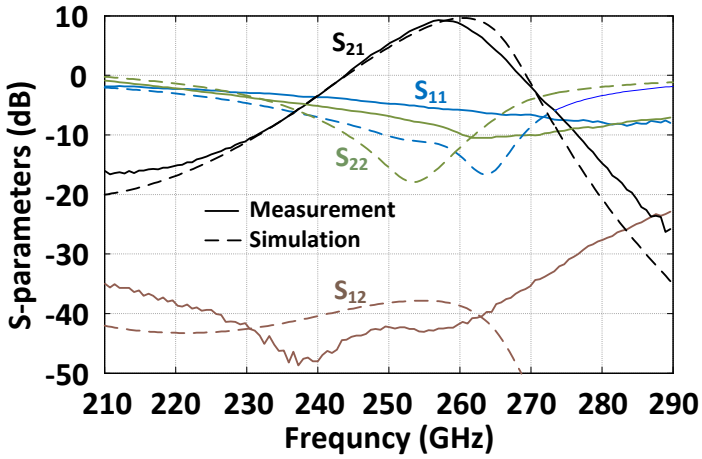
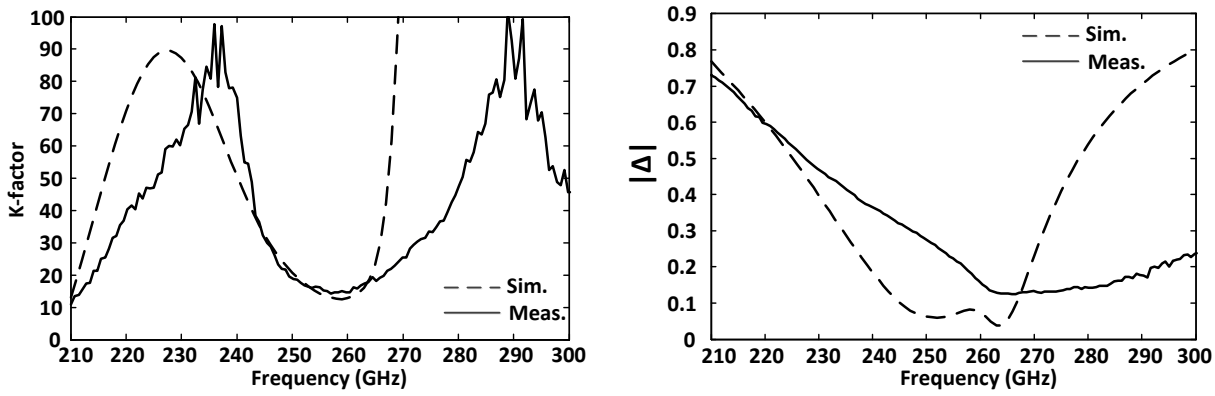


FIGURE 4.6. Simulated and measured S-parameters of the proposed gain-boosted amplifier.



(a) (b)

FIGURE 4.7. Stability measures simulation and measurement results. The amplifier is unconditionally stable.

The die micrograph is shown in Fig. 6.9, and the chip size is 800×180 μm^2. Table I presents a summary of the implemented four-stage amplifier and compares its performance with the state-of-the-art. The amplifier has the highest operation frequency among the reported amplifiers in any silicon technology. The saturated output power (P_{sat}) of the amplifier is higher than any silicon-based amplifier beyond 220 GHz. Other specifications are comparable to amplifiers in compound semiconductors with considerably higher f_{max}.

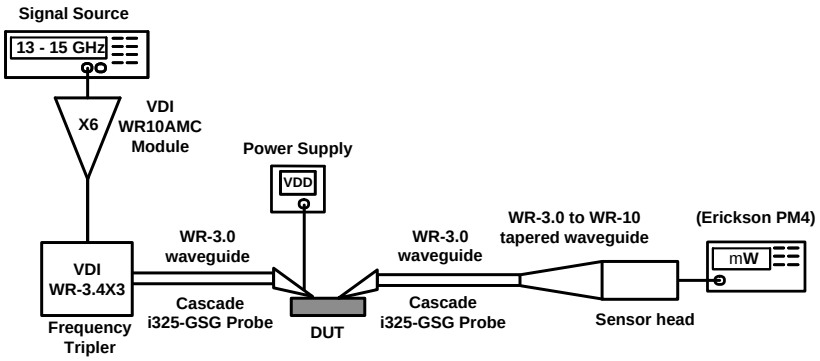
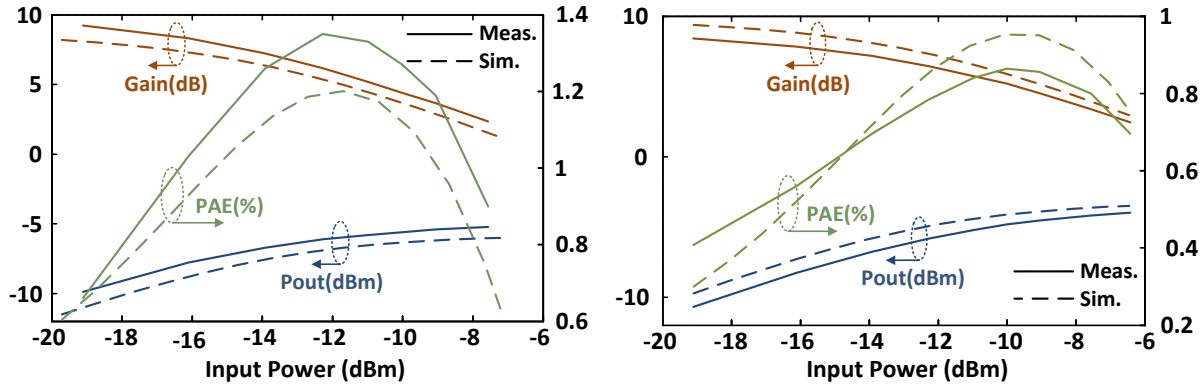


FIGURE 4.8. Test setup for large-signal measurements.The internal Bias Tee of Cascade i325-GSG Probe is used to bias the amplifier.



(a) (b)

FIGURE 4.9. Power added efficiency, output power and large-signal gain of the amplifier for (a) $V_{DD} = 0.8V$ (b) $V_{DD} = 1V$.

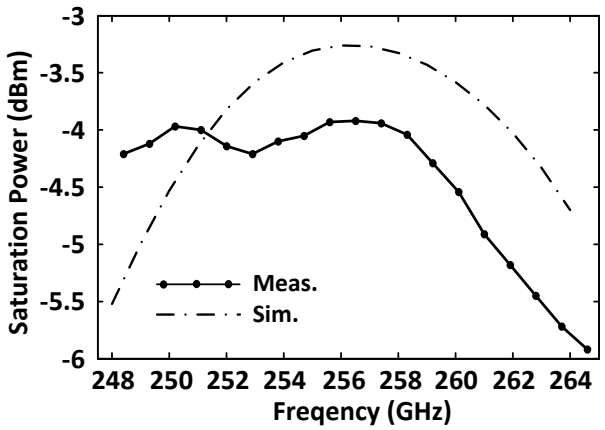


FIGURE 4.10. Simulated and measured saturated output power as a function of frequency.

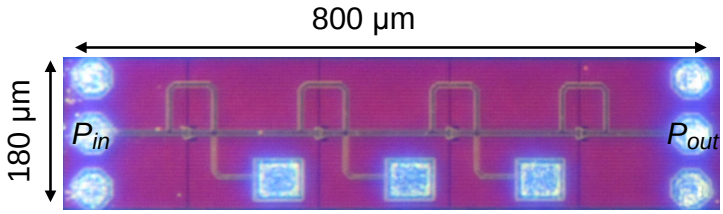


FIGURE 4.11. Chip microphotograph.

TABLE I
COMPARISON OF THE FABRICATED AMPLIFIER WITH THE STATE-OF-THE-ART.

Ref.	Tech.	f_{max} (GHz)	Freq. (GHz)	Gain (dB)	3-dB BW (GHz)	Sup. Vol. (V)	P_{1-dB} (dBm)	P_{sat} (dBm)	Peak PAE (%)	P_{DC} (mW)	Topology	Area (mm^2)
[15]	25 nm InP HEMT	1500	1000	9	100[1]	N/A	N/A	N/A	N/A	N/A	10 CS stages	N/A
[32]	130 nm SiGe HBT	435	220	16	28	3.6	N/A	N/A	N/A	144	3 Diff. Cascode Stages	0.45
[33]	250 nm InP DHBT	550	324	4.8	3 (2-dB)	1.4	N/A	1.1	0.6	16.8	1 CB stage	0.12
[34]	50 nm InP HEMT	1200	340	15	25[1]	2.2	N/A	10	N/A	294.8	4 CE stages	0.49
[35]	40 nm CMOS	275	213.5	10.5	13	0.8	-7.2	-3.2	0.75	42.3	9 CS stages	0.013
[36]	50 nm InP HEMT	N/A	220	10.4	30	2.2	18	N/A	3.7	2165	4 CS stages 8 power comb.	0.96
[37][2]	250 nm InP HBT	700	190-260	28	70	N/A	19[3]	N/A	4.5	1770	3 Cascode stages 4 power comb.	1.536
[38] [2]	130 nm InP DHBT	1100	670	24	150	1.8	N/A	-4	N/A	N/A	9 CB stages	0.3123
[39]	32 nm SOI CMOS	320	210	15	14	1	2.7	4.6	6	40	3 Neutralized diff. stages	0.06
This work	**65 nm CMOS**	**345 GHz**	**257**	**8.5**	**12.2**	**0.8**	**-8**	**-5.5**	**1.3**	**13.7**	**4 CS stages**	**0.14**
This work	**65 nm CMOS**	**352 GHz**	**257**	**9.2**	**12.2**	**1**	**-8**	**-3.9**	**0.8**	**27.6**	**4 CS stages**	**0.14**

[1] Estimation from the reported results.
[2] High-gain version.
[3] Maximum output power.

CHAPTER 5

Embedding and Output Power

5.1. The Impact of Limited Gain on the PA's Output Power at Near-f_{max} Frequencies

As frequency increases, the loss mechanisms in both active and passive devices start to dominate the performance of amplifiers. On one hand, in passives, the loss of metallic conductors increases proportional to the square-root of frequency, due to the skin effect. Moreover, dielectric substrates become more lossy, as dielectric loss tangent increases proportional to frequency. These effects result in low quality factor passives that adversely affects the matching networks' loss and hence the amplifier gain. On the other hand, internal losses of transistors diminish maximum available power gain with frequency, and causes the transistor to become a passive element beyond f_{max}. These factors make the design of amplifiers challenging and in some cases impossible at near-f_{max} frequencies. In addition to the high loss and low gain challenges of small-signal amplifier design at these frequencies, power amplifiers suffer from limited output power and low input/output impedances which increase matching loss even further.

Fig. 5.1(a) shows an NMOS common-source differential amplifier neutralized by C_N capacitors. The output of the amplifier is matched to 50Ω using an L-matching network for three different transistor sizes: 10um, 20um, and 40um in a 65nm CMOS process. The quality factors of the inductor and capacitor of the L-matching network are selected to be 20 and 8, respectively, at all frequencies. Fig. 5.1(b) shows matching loss versus frequency for the three transistor sizes, as well as unilateral power gain (U) of a 10um NMOS transistor. U of 20um and 40um NMOS transistors is assumed to be the same as 10um NMOS transistor,

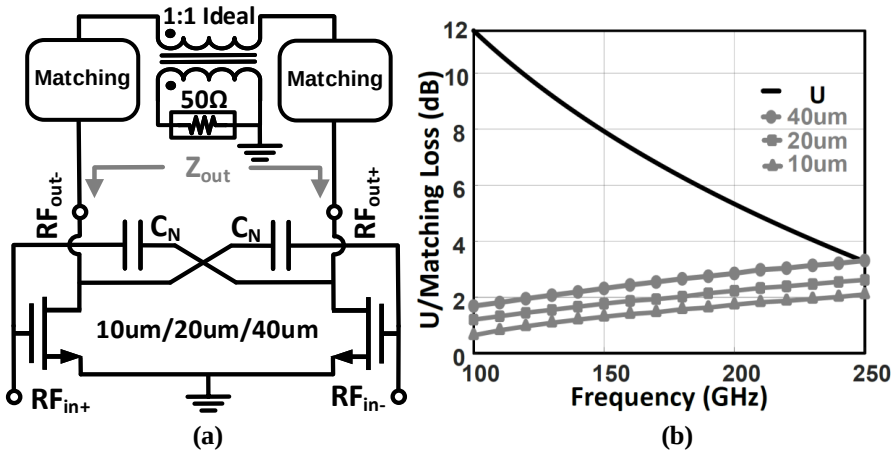


FIGURE 5.1. Transistor/passive devices gain/loss versus frequency. (a) Circuit schematic of a neutralized differential common-source amp-cell with three different transistor sizes. (b) Simulated unilateral power gain (U) of a 10/20/40um NMOS common-source transistor, and the losses of output matching network of the amp-cell shown in (a) to 50Ω.

since the metal connections that are used to make 10um transistors in parallel in order to make 20um and 40um transistors are very short and low loss. As it can be seen, U falls below the matching loss at frequencies higher than 250GHz for 40um transistor size, forcing the designer to reduce the transistor size or operation frequency. In reality, quality factors of matching network elements are not constant, and drop with frequency, making it harder to design high gain amplifiers with larger transistors at high frequencies. The rise in loss at high frequencies not only reduces the overall small-signal gain, but also adversely affects output power of a PA. Since the available gain from amp-cells at high mm-wave frequency band is small, multiple amp-cells must be cascaded to achieve a reasonable gain. In cascaded PA's, the amp-cells close to the input, called the driver amp-cells, are meant to increase the small signal gain. Every amp-cell added after the drivers has to deliver higher power to its load compared to its preceding amp-cell, while increasing the overall power gain of the PA. As shown in Fig. 5.2(a), each amp-cell needs its preceding matching network, and together they are called a stage (amp-cell + preceding matching network). Having the practical aspect of the PA in mind, we evaluate the highest output power of this stage at the point that the

gain of the stage is compressed to the minimum gain of 1 dB. This ensures that the PA has an acceptable power gain when it is delivering its highest power. In other words, a PA stage with less than 1 dB gain is not useful even if it can deliver high output power. As shown in Fig. 5.2(b), since the small-signal power gain of the stage is already 1dB, no compression is acceptable, and therefore, the maximum output power of the stage is 6dBm at the input power of $P_{i,Stage}$=5dBm, right before the compression in gain starts. Even though the amp-cell has 1dB output compression point (OP1dB) of 9dBm , and P_{sat} of 11dBm, it only delivers 6dBm at 1dB stage gain. This shows that low small-signal stage gain limits the maximum power that the amp-cell can deliver with an acceptable gain. The high power capability of the amp-cell, however, can be traded off to boost the small signal power gain, and extend the Amplification region (stage-gain¿1dB) to higher input powers. This results in higher output power at 1dB stage gain.

Shown in Fig. 5.3(a), a small fraction of the output power can be fed back to the input port of the amp-cell using an embedding network to boost the power gain. blueUsing a numerical simulator (e.g., Matlab) a constant fraction of the output power of the amp-cell is extracted and fed back to its input to emulate the operation of a lossless embedding. The feedback power is constructively added to the input power of the amp-cell to boost its power gain. This numerical simulation shows that, although the embedding reduces OP1dB and P_{sat} of the embedded amp-cell to 6.7dBm, and 9.05dBm, respectively, it increases the small-signal power gain of the stage to 4dB as shown in Fig. 5.3(b). The boost in the stage small-signal gain translates to 3dB gain compression at 1dB stage-gain. This extends the Amplification region to 7.1dBm compared to 5dBm of the non-embedded case, and increases the output power of the stage from 6dBm to 8.1dBm at the same 1dB stage gain. Fig. 5.3(b) also shows that although the OP1dB has dropped, the output power at 1dB stage gain is well above it. This analysis shows that embedding not only boosts the small signal power gain of a PA, but also improves the output power of the PA at a specific power gain.

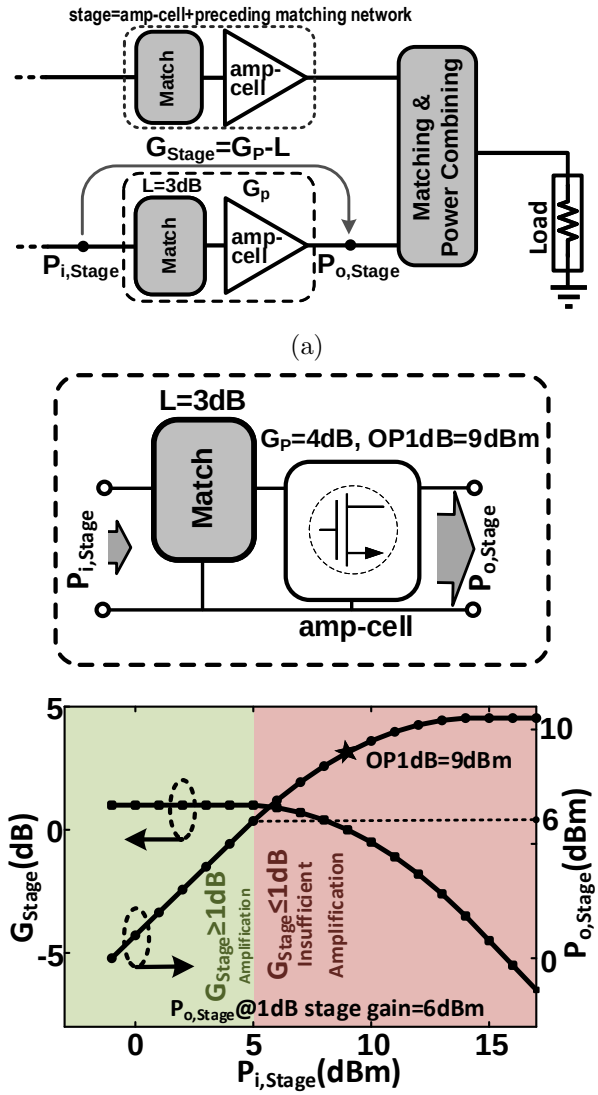


FIGURE 5.2. Maximum output power of a cascaded PA with a minimum stage-gain of 1dB (a) Block diagram of the last stage in a cascaded PA. (b) Simulated power performance of a high-power, low-gain amp-cell.

5.2. Output Power in Embedded Amplifiers

The previous section illustrated the effect of power gain on the output power of a PA by ideally subtracting some signal power from the output and adding it to the input port. In an actual circuit implementation however, a passive network performs this feedback operation.

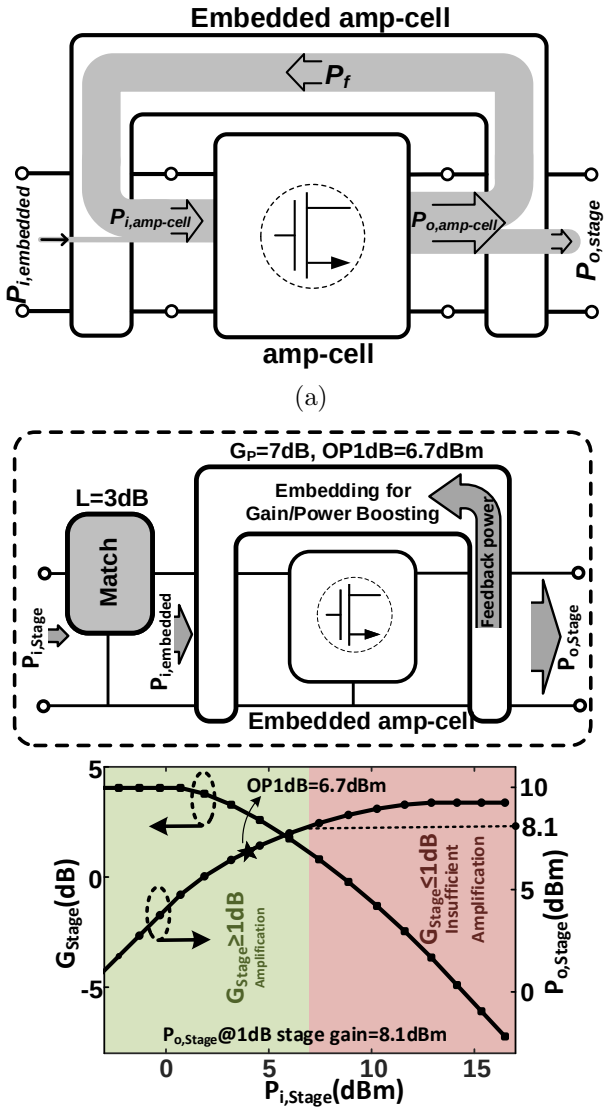


FIGURE 5.3. Effect of gain boosting using embedding on the output power of a PA. (a) The power flow that results in boosting the power gain. (b) The performance of the cascaded PA after embedding the amp-cell of the last stage.

As a result not only the gain is boosted but also the power delivery capability of the stage is affected. This is because the feedback network directly influences the impedances that are seen by the amp-cell.

blueSince gain boosting is always performed using small-signal analysis, to find the relation

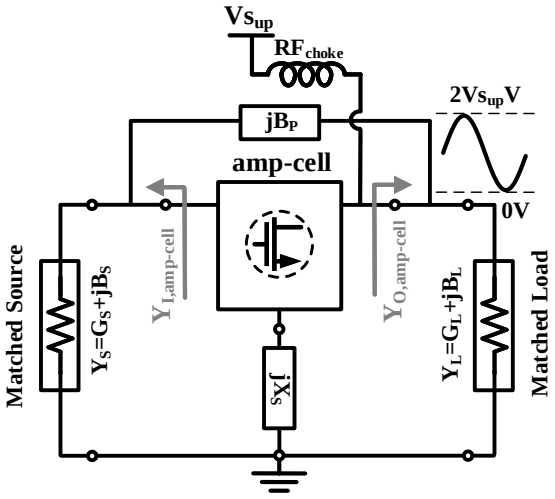


FIGURE 5.4. An amp-cell embedded by T-embedding and supplied through an RF_{choke}.

between the gain and output power of an embedded amp-cell and optimize them simultaneously, we must use its small-signal parameters to estimate the maximum linear output power. To this end, the setup shown in Fig. 5.4 is used where an amp-cell is embedded by T-embedding [**6**].

To conserve the hard-earned power-gain, the embedded amp-cell is assumed to be conjugate matched to the source and load impedances. To simplify the power analysis, we assume that the output voltage of the amp-cell experiences clipping before its input voltage, and this clipping is the only nonlinear effect that causes gain compression. Hence, the maximum linear output power of the amp-cell shown in Fig. 5.4 can be estimated as:

$$P_{o,max} = 0.5V_{Sup}^2 \cdot G_L, \tag{5.1}$$

where V_{Sup} is the supply voltage of the amp-cell and G_L is the conductance of the simultaneously matched load admittance. Embedding in general, functions as a feedback network, and as such it alters the admittances seen from the input and output ports of the embedded amp-cell (G_S and G_L in Fig. 5.4, respectively). Because V_{Sup} does not change with embedding, blueand knowing that load pull would decrease the power gain of the embedded

amp-cell compromising its output power with a minimum acceptable gain, the maximum output power of the amp-cell can be estimated from G_L. By changing the impedances seen by the amp-cell, embedding can increase or decrease the output power of the amp-cell itself. In case it increases the output power of the amp-cell at higher rate than the increase in the feedback power(Fig. 5.3(a)), embedding can boost both the power gain and the output power of the embedded amp-cell simultaneously.

There are several T-embedding networks that can boost power gain of an amp-cell to a certain value, each of which results in a different G_L, and thus different output power. For example, using the gain-plane approach in Fig. 5.5, it is shown that the power gain of an arbitrary amp-cell can be boosted to U by different movements to different coordinates on the U curve (the gray curve in Fig. 5.5) [**4**, **6**, **18**, **51**, **54**, **63**]. All these movements result in the same power gain of U, however, they each need a different set of passive elements (jX_S and jB_P) to perform the gain boosting [**6**]. This naturally results in different G_L and hence the maximum output power of the amp-cell would not be the same for the different movements. In [**6**], the equations of series and shunt embeddings (jX_S and jB_P), are derived to move only to the horizontal axis, Re(U/A), for a desired gain mainly to maximize the stability margins and simplify the derivation. However, moving to a coordinate on Re(U/A) axis for a desired gain does not necessarily result in the maximum output power. To find the optimum embedding for the maximum output power of an embedded amplifier, the equations for jX_S and jB_P are generalized to cover the whole stable region of K¿1. The equations and the descriptions are given in Appendix B. In other words, given the desired gain and the location on the equi-G_{ma} curve, the exact passive components can be calculated using these equations. Moreover, they help us to quickly and efficiently optimize the embedding network for a desired gain value.

Having this theoretical foundation, and given a specific amp-cell, G_L can also be calculated for each movement in the gain plane. Shown in Fig. 5.6, the contours of equi-G_{ma} and

equi-G_L of a 40um common-source NMOS in 65nm technology at 200GHz are plotted using the equations in Appendix B. blueTo plot Fig. 6, first, we selected a rectangle that is large enough to cover the entire stable region in the gain-plane (boundaries of this rectangle can be always changed if later in the next simulation steps it turns out it does cover the entire stable region). Second, this rectangular region is divided to small pixels. Using the equations in Appendix B the embedding networks are calculated and are used to move the amp cell to all these pixels. Knowing the embedding networks, K, G_{ma}, and G_L were calculated for all of the pixels. The region that corresponds to K≥1 is found using numerical methods. Finally, the equi-G_{ma} and equi-G_L contours within the stable region were plotted numerically.

It is evident from the figure that different coordinates on an equi-G_{ma} contour are associated

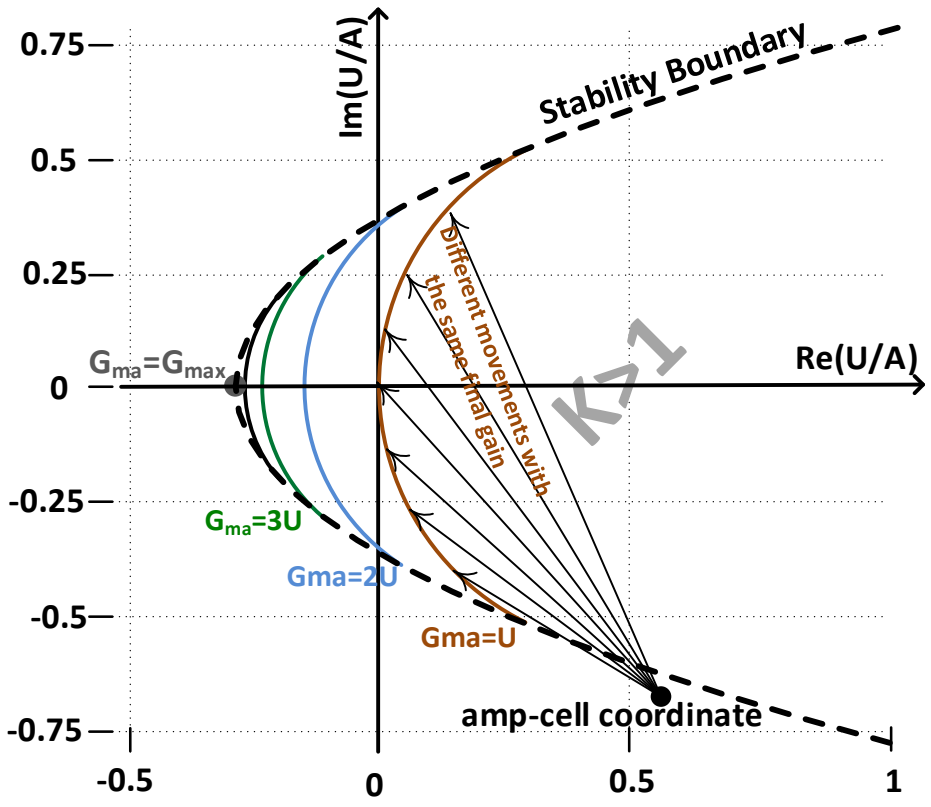


FIGURE 5.5. Different movements (embeddings) can result in the same boosted power gain in a gain plane.

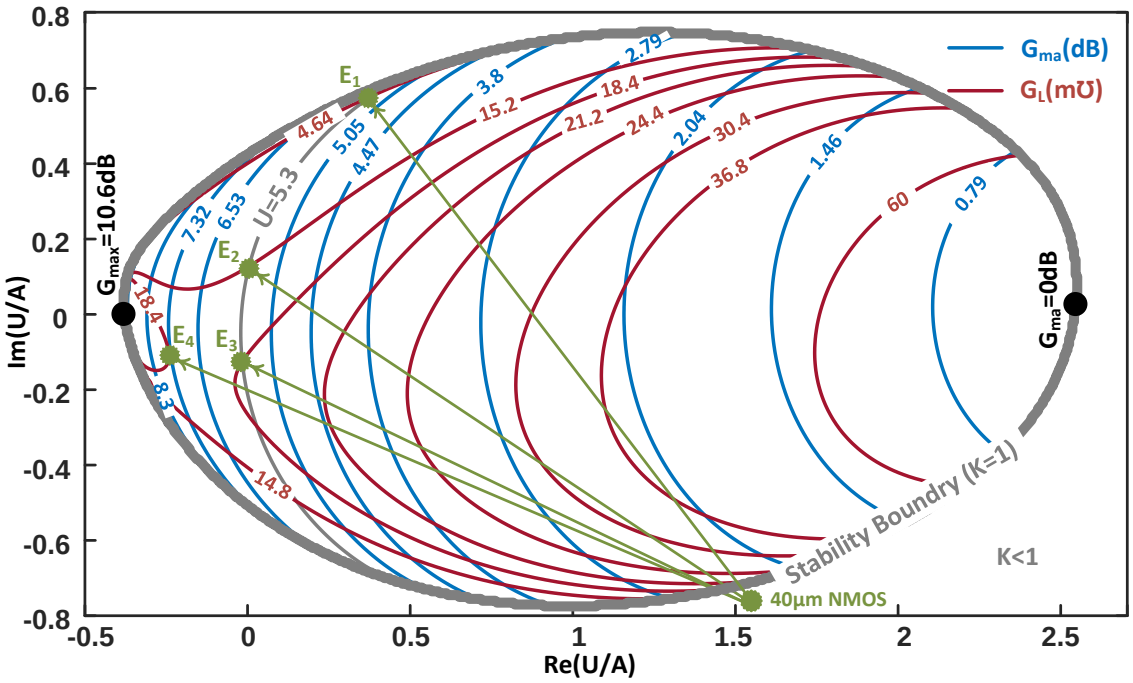


FIGURE 5.6. Contours of equi-G_{ma} and equi-G_L, the conductance of simultaneously matched load admittance, in the gain-plane for a 40μm common-source NMOS transistor in 65nm Bulk CMOS process at 200Hz.

with different G_L values, resulting in different output power. For example if one selects to boost the power gain to U, a movement to E_1, would result in G_L=4.64m℧. For V_{Sup}=1V, this translates to a maximum output power of $P_{O,max}$=3.65dBm. However, for the same power gain of U, the transistor can be embedded to move to E_2 or E_3, where G_L is equal to 15.2m℧ and 18.4m℧ resulting in 8.8dBm and 9.6dBm output power, respectively. These power levels are significantly higher than the one in E_1. Moreover, E_2 and E_3 are much further from the stability boundary compared to E_1 and therefore, are much more reliable operating points. Interestingly, as shown in Fig. 5.6, the embedding that moves the transistor to E_4 not only results in higher gain of 7.3dB, but also a higher output power of 6dBm, compared to the one for E_1. Intuitively speaking, to boost the power gain to higher values, embedding has to send a larger fraction of the output power to the input of the amp-cell. At the same time the embedding is also changing the conductance seen by the amp-cell,

real($Y_{O,amp-cell}$). In other words, in the case of E_4, the embedding is boosting the gain by feeding back more power but at the same time and with a higher rate is increasing the output power of the amp-cell by increasing real($Y_{O,amp-cell}$). The analysis done in Fig. 5.6 is for a simple amp-cell of a 40um CS CMOS transistor and can be performed for any general amp-cell to understand the PA's trade-offs and behavior and to be able to optimize for the best possible outcome.

CHAPTER 6

Implemented 200GHz CMOS Power Amplifier

6.1. High-Power/Gain Matched-Cascode Amp-Cell

As Fig. 5.3(a) suggests, output power of an embedded power amplifier is directly a function of its amp-cell's power capability. To enhance the output power of a single-transistor amp-cell (e.g., common-source (CS) amp-cell), one can increase the size of the transistor. Nonetheless, a large transistor typically has low input/output impedances, and consequently high matching loss and low stage gain. This limits the maximum transistor size for an acceptable gain and output power at high mm-wave frequencies. The output power of the amp-cell can be boosted further using stacked transistors to increase the output voltage swing without exceeding the allowable voltage stresses of the transistors junctions. However, stacking reduces the power gain since the gate capacitors function as negative feedback in each transistor [**2**, **56**]. This reduces the gain of the amp-cell and limits the operation frequency of this topology to low mm-wave frequencies. In this section we introduce a matched-cascode amp-cell that delivers higher P_{out} at a higher power gain compared to a traditional cascode amp-cell at high mm-wave frequencies.

Gain compression is the result of transistors leaving their linear region, or clipping in the output voltage due to exceeding the rail voltages (e.g., 0V and $2V_{Sup}$). The change of operation region or clipping in the output voltage changes the transfer function of the amp-cell for a fraction of input cycle and leads to harmonic generation and gain compression. To avoid gain compression at low output powers, the amp-cell must be designed such that the output voltage reaches its rail-to-rail swing before the amp-cell transistor(s) exit their linear region. This guarantees that gain compression starts at maximum linear output power.

A CMOS transistor exits its linear region, if V_{GS} falls below threshold voltage (V_{th}) corresponding to Off region, or if V_{GD} exceeds V_{th},corresponding to Triode region. A traditional cascode amp-cell is shown in Fig. 6.1(a) on the left. Starting with the size of the transistors, it is assumed that the maximum transistor size that results in an acceptable matching loss is selected for the CS transistor (M_1). The common-gate (CG) transistor (M_2) is selected to have the same size as the CS to ensure equal drain-source voltages without altering the optimum gate biasing voltages for maximum gate-source/gate-drain swing. On the right side of the figure the small-signal equivalent of the amp-cell is shown. The C_{GD} of the transistors are split to two miller capacitors at the gate and drain terminals, C_{Min} and C_{Mout}, respectively. To reach a high output power, I_{D2} must be maximized without pushing V_{GS} and V_{DS} into nonlinear regions. However, since M_1 and M_2 are large and the operation frequency is high, the total parallel parasitic capacitor ($C_{DB1} + C_{Mout1} + C_{GS2}$) has a very small impedance at high mm-wave frequencies, leading to a small V_{GS2} and hence a small I_{D2}, and output power. In this scenario, to achieve a high I_{D2}, a large V_{GS1} is needed to generate a large I_{D1} and V_{GS2}. Therefore, before delivering high I_{D2} to the load, M_1 enters Off region compressing the power gain of the amp-cell and limiting OP1dB. Moreover, the large parasitic capacitor at the drain of M_2 results in a low power gain, as well, as the amp-cell would have a small output power for large input power. Accordingly, a traditional cascode amp-cell neither has high power gain nor high OP1dB at high mm-wave frequencies. The cascode amp-cell shown in Fig. 6.1(a) has a gain of 2.9dB , and along with 3dB matching loss at the input results in a total stage gain of -0.1dB at 200GHz. The amp-cell also has a OP1dB of 4.7dBm, when matched to its conjugate load impedance and supplied from 2.4V. The output power at 1dB stage-gain is not defined as the small-signal stage-gain is already -0.1dB.

To improve the low impedance at D_1, an inductor can be added between the node and the ground to resonate out the parasitic capacitances, as in Fig. 6.1(b). In this figure, Ind_1 that is composed of the transmission line $TL_{M,1}$ and the DC block capacitor C_{blk} increases the

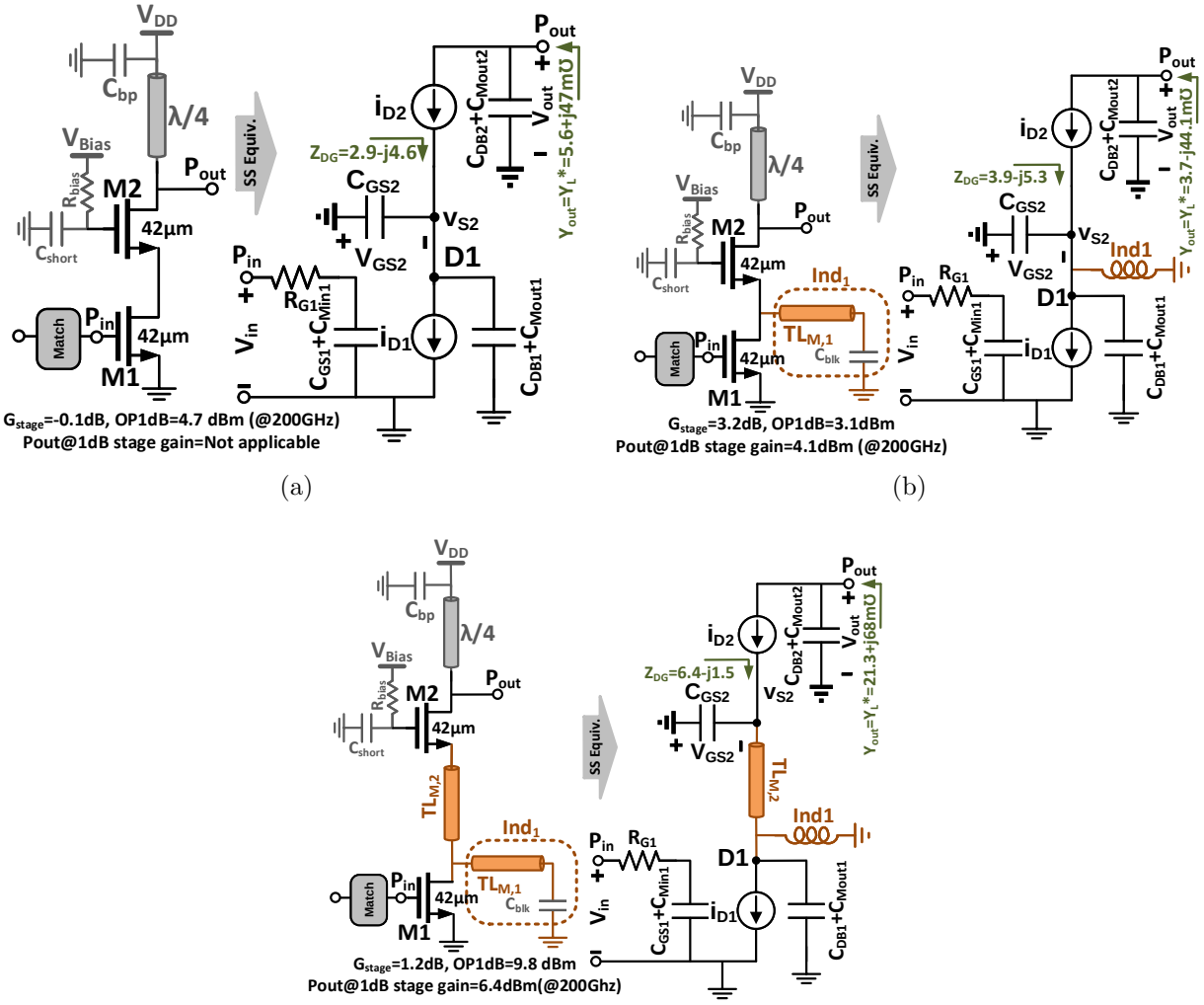


FIGURE 6.1. (a) Traditional cascode has no gain and low OP1dB (b) cascode with the tuning inductor Ind_1 has higher power gain, still degeneration seen by M_2's source terminal reduces OP1dB (c) matched-cascode has a modified degeneration impedance while benefiting from the tuning inductor Ind_1 too. It delivers both high OP1dB and high power gain. In all the three cases the loss of preceding matching network is 3dB, the supply voltage is 2.4V, and the reported numbers are at 200GHz.

total impedance seen by I_{D1}. This increases V_{D1} swing, and accordingly V_{GS2} swing, and boosts power gain and output power at the same time. However, this resonance also degenerates the source of M2 with a higher impedance, Z_{DG}, and results in a smaller conductance

at the output port of the amp-cell. Thus the conductance of the conjugate-matched load drops and $P_{o,max}$ declines. With a small-signal stage gain of 3.2dB, this amp-cell has an OP1dB of 3.1dBm and delivers 4.1dBm to the load at 1dB stage-gain at 200GHz.

To optimize the impedance seen by the source terminal of M_2, TL_{M2} is added between the drain of M_1 and source of M_2 as depicted in Fig. 6.1(c). This transmission line increases the resistance of Z_{DG} from 3.9 to 6.4 and decreases its reactance's absolute value from 5.3 to 1.5 . This increase in the resistance to reactance ratio of the degeneration impedance, increases this ratio at the output of the amp-cell. Therefore, the conductance of Y_{out} increases to 21.3 m℧, and this increases the output power. This amp-cell called matched-cascode as Ind_1, and $T_{L,M2}$ increase the power flow from M_1 to M_2 , and eventually to the load. This amp-cell has an OP1dB of 9.5dBm and its stage-gain is 0.8dB at 210GHz.

The minimum gain of the amp-cell after embedding is selected to be 6dB at 210GHz to make 2dB compression possible before the stage-gain falls below 1dB. Then the embedding around the amp-cell was tuned to find the embedding that maximizes G_L for the same target gain. Finally large-signal simulations were done to fine-tune the embedding for maximum output power. The matched-cascode cell is embedded as shown in Fig. 6.2. All the embedding components are implemented as microstrip transmission lines in m9 metal layer of the process with m2 as the ground plane. $TL_{E,1}$ and $TL_{E,2}$ in Fig. 6.2 are used as pre-embeddings to avoid high loss in series embedding and have an electrical length of 0.1λ and 0.3λ, respectively [**6**]. $TL_{E,3}$ and $TL_{E,4}$, with lengths of 0.25λ and 0.1λ respectively, together with C_f, which is used to DC decouple the input and output of the amp-cell, are used as parallel embedding. The decoupling capacitor C_{blk} is a multi-layer capacitor composed of m2 to m4 metal layers of the process. This decoupling capacitor in conjunction with $TL_{M,1}$ form a 26pH inductor with a quality factor of 11 at 210GHz. All the embeddings are implemented in m9 metal layer of the process. Fig. 6.3 shows the simulation results of the last stage amp-cell before and after embedding. As it can be seen the power gain is boosted by 2.3dB.

This results in 8.5dBm output power at 1-dB stage-gain at 210GHz after embedding.

6.2. wideband, balanced Slot Power Combiner

Utilizing large transistors, and increasing the output swing using the proposed matched-cascode amp-cell, along with gain boosting could be exploited to increase the output power of a PA. To boost the output power further, traditionally power combiners are used at the end of PA chains. Nevertheless, power combiners suffer from known deficiencies namely high loss, and large/imbalanced impedances at the input ports. Large input impedances increase the impedance transformation ratio of the matching network between the last PA cell and the power combiner, and therefore the loss [**6**]. Whereas imbalanced input impedances result in non-optimum loading of the last PA cells as well as phase mismatch of their output signals, both adversely affecting the total output power. This section introduces a two-to-one low-loss, wideband, balanced slot power combiner (SPC) with low input impedance.

The proposed slot power combiner is shown in Fig. 6.4. Two out-of-phase signals from the last PA cells are applied to the input ports of the power combiner (P_1 and P_2). This

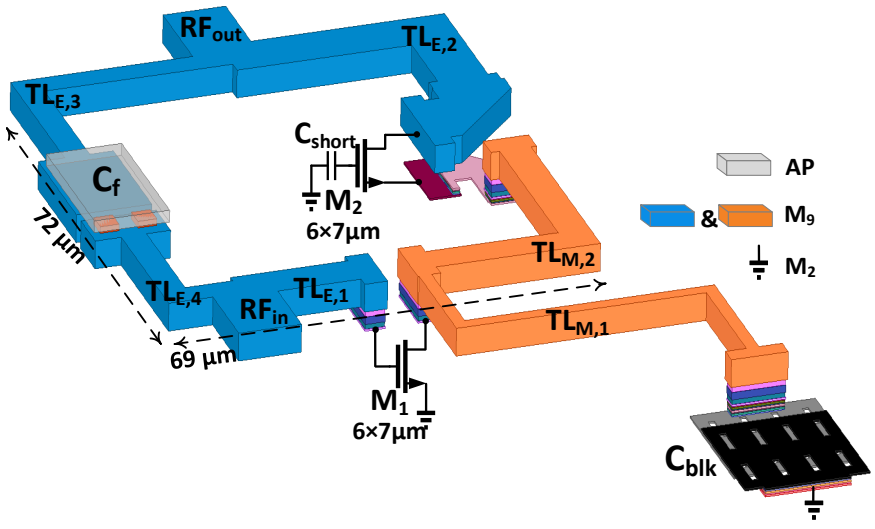


FIGURE 6.2. The embedding used to boost power gain of the matched-cascode amp-cell and maximize its output power.

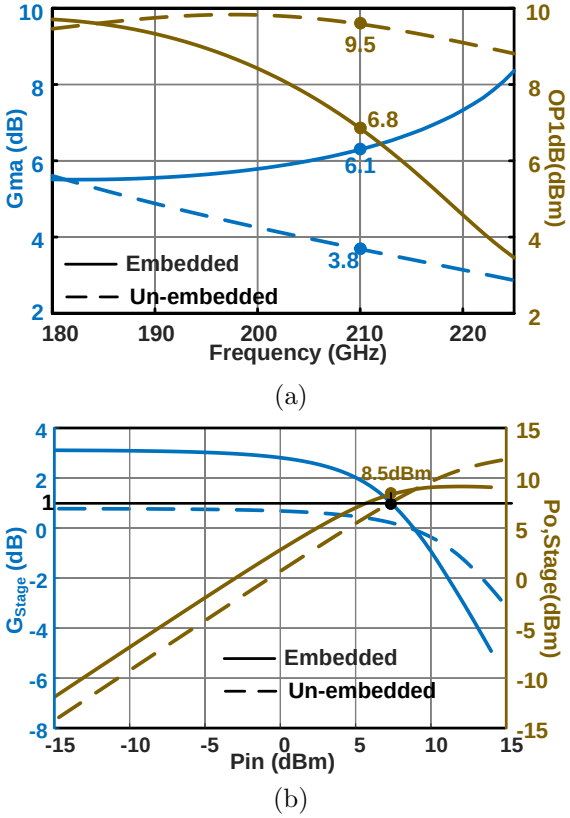


FIGURE 6.3. (a) Maximum available gains (G_{ma})'s and output 1dB compression points of matched-cascode (Un-embedded) and embedded matched cascode (Embedded) versus frequency (b) Stage-gain and stage output power at 1dB stage-gain before and after embedding.

differential signal creates a current in TL_1 , which passes over the slot-line perpendicularly. This current induces an electromagnetic (EM) wave in the slot-line. The reciprocal of this transition takes place between the slot-line and TL_2, which is in parallel with TL_1, and the combined signal would be delivered to the load. Fig. 6.5 shows a microstrip-slotline cross section and signal transition from its input port to the output port. A microstrip on a substrate with height of h and permittivity of ε_r passes perpendicularly over a slotline etched in the ground plane. It is assumed that the input signal, S_i, is fed to the microstrip from the right side. A time-varying electric field ($E_{msl}(t)$) and magnetic field ($H_{msl}(t)$) start traveling towards the open end of the microstrip. At the intersection with the slotline,

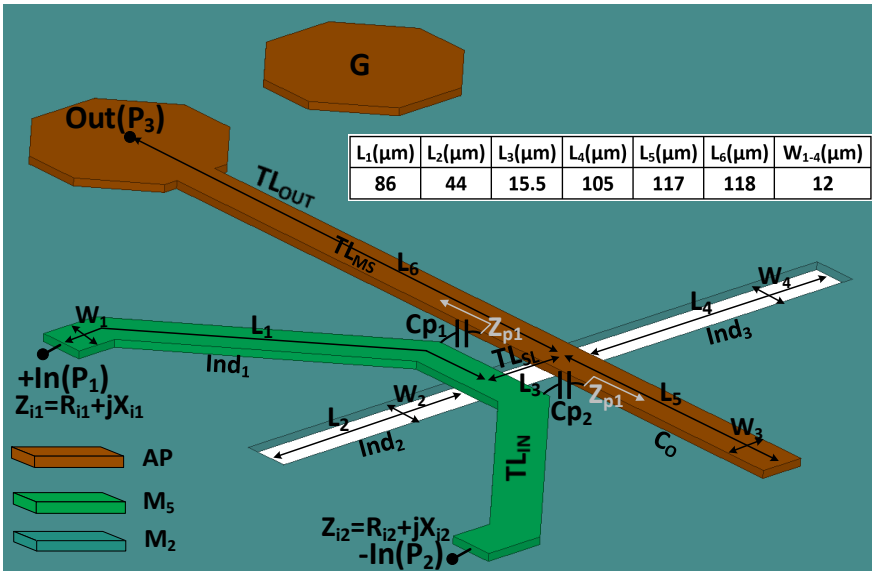


FIGURE 6.4. 2-to-1 differential slot power combiner.

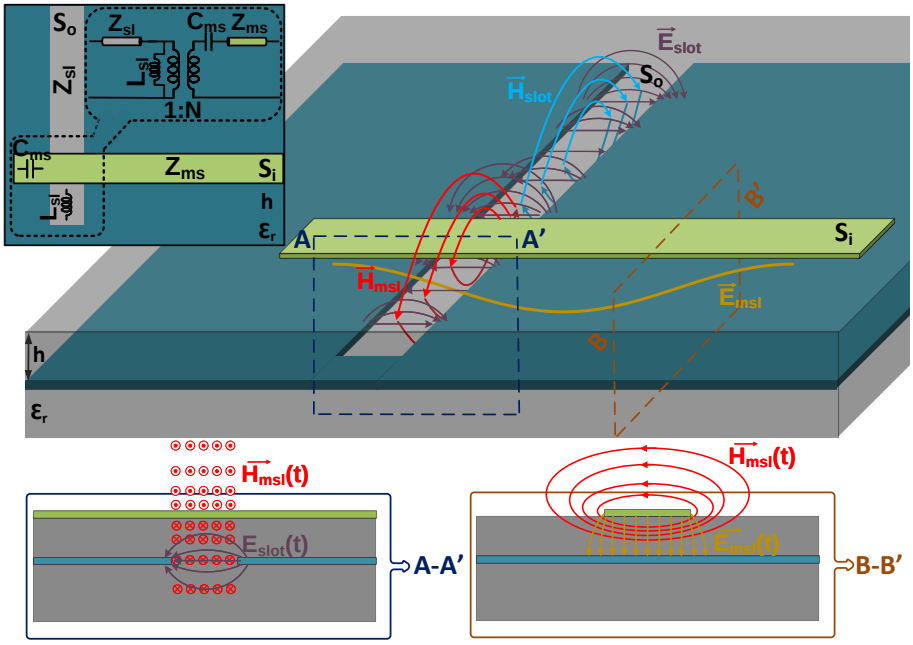


FIGURE 6.5. Microstrip-slotline transition and its equivalent circuit.

the time-varying $H_{msl}(t)$ induces a time-varying electric field ($E_{slot}(t)$) perpendicular to the slotline edges, as shown in Fig. 6.5. This electric field generates a voltage across the edges of the slotline that changes with time and results in a time-varying current in the slotline.

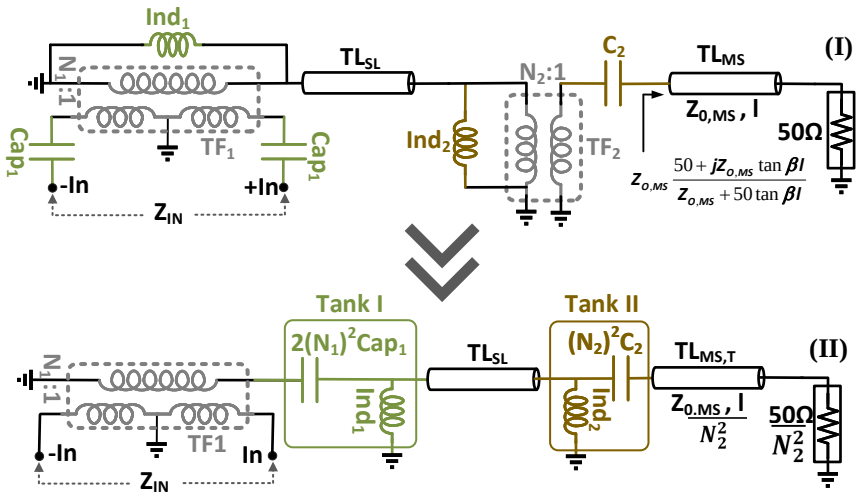


FIGURE 6.6. The equivalent circuit of the slot power combiner shown in Fig. 6.4.

This current generates the slotline time-varying magnetic field $H_{slot}(t)$ and together with $E_{slot}(t)$ propagate to the output port of the slotline. This transition can naturally happen in an opposite fashion from the slotline to the microstrip.

The microstrip-to-slotline transition can be modeled by an equivalent resonant circuit shown on the right side of Fig. 6.5. The circuit consists of a transformer with a transformation ratio of N, where N is a function of transmission lines characteristic impedances Z_{ms} and Z_{sl} [**27**]. L_{sl} is the inductance of shorted slotline and C_{ms} is the capacitance of the open microstrip.

The equivalent circuit of the slot power combiner is shown in Fig. 6.6. Since the signal experiences two transitions between the slot-line and the microstrip, two transformers with inductor and capacitor exist in the equivalent circuit of the slot power combiner (Fig. 6.6(I)). The components in the secondary of TF_2, can be transferred to its primary, and the same can be done to Cap_1. These transfers result in the simplified filter shown Fig 6.6(II). Two tanks exist in the simplified equivalent circuit of the power combiner creating two resonant frequencies. These resonant frequencies can be designed to be far from each other to get a wideband performance [**17**].

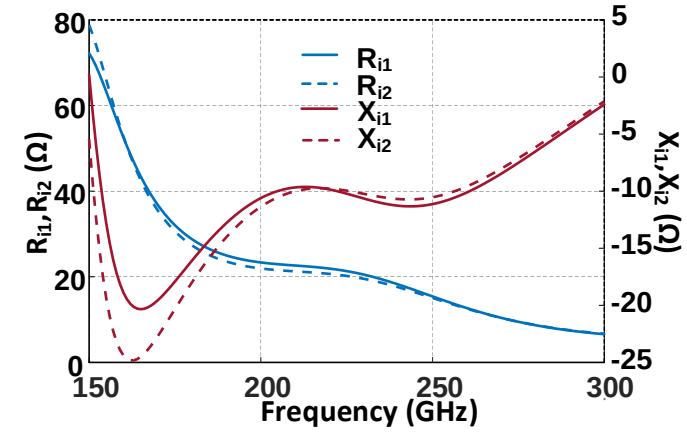
The power combiner's input microstrip line is completely symmetric with respect to the

slotline. At the middle of the structure, as shown in Fig. 6.4, two parasitic capacitors C_{p1} and C_{p2} couple the input and output microstrip lines. These capacitors see different impedances (Z_{P1} and Z_{P2}) and therefore are the only source of imbalance between the inputs in the power combiner. However, the metal layers used for the input and output microstrips are different, and the length of the input microstrip in parallel with TL_{out} is minimized, and therefore, C_{p1} and C_{p2} are very small and the mismatch they cause between input impedances is negligible. As shown in Fig. 6.7(a), the input impedances of the implemented slot power combiner are very close to each other at 170-300GHz. Fig. 6.7(b) illustrates wideband performance of the slot power combiner. The return losses at the input ports stay lower than -10dB from 172GHz to 262GHz, which results in 41.5% fractional bandwidth.

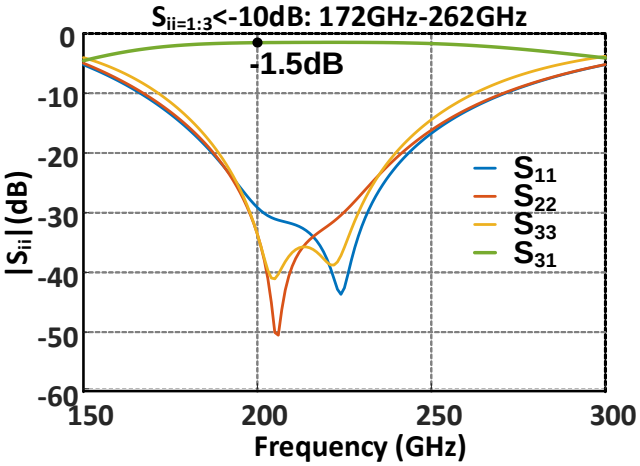
The insertion loss of the combiner is 1.5dB at 200GHz, with a 1-dB bandwidth of 74GHz. To adjust the response of the slot power combiner, one can change the values of the filter components shown in Fig. 6.6 by altering the lengths/widths of the slot-line and microstrip lines in Fig. 6.4. Different inductor sizes, $L_{i,i=1:4}$, in the slot power combiner shown in Fig. 6.4 are increased and the insertion losses and the input impedanceis simulated as shown in Fig. 6.8(b). The black curves in Fig. 6.8, SPC, correspond to the slot power combiner shown in Fig. 6.4. Increasing the lengths of open microstrip line and short slot-lines results in lower center frequencies. The longer these lengths are the larger their equivalent capacitance/inductances would be in Fig. 6.6, and the smaller the resonance frequencies of the tanks are. Increasing L_3 decreases the insertion loss and the same time lowers the center frequency. Fig. 6.8(b) shows that the input ports of the slot power combiner stay matched for over 60GHz bandwidth.

6.3. Implementation and Measurement Results

The chip microphotograph is shown in Fig. 6.9. The dimensions of the chip are 0.95mmx2.6mm, where the active area including input and output pads is 0.7mmx2mm. Using the proposed matched-cascode amp-cell, a 2-by-8 power amplifier is implemented in TSMC 65nm Bulk



(a)

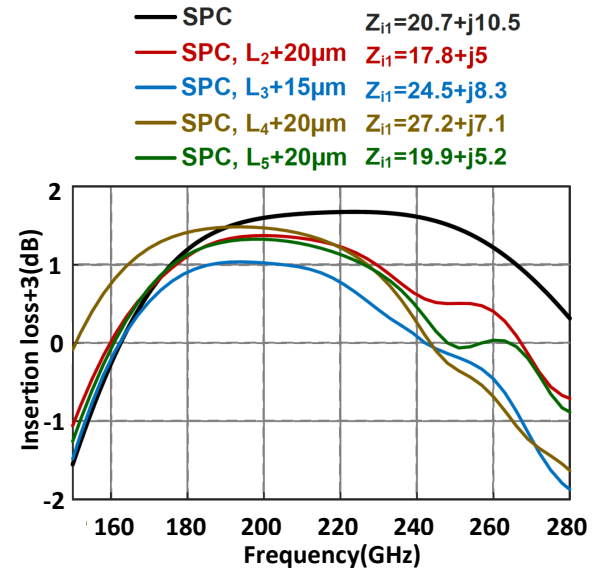


(b)

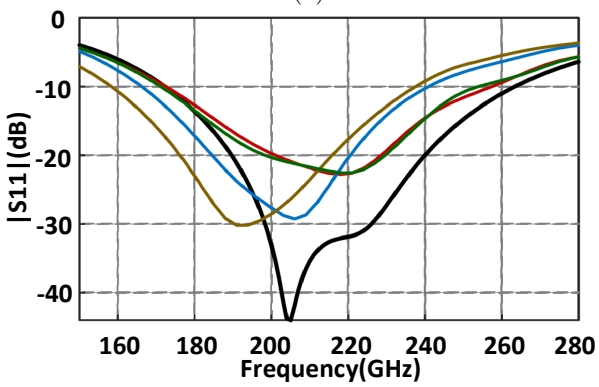
FIGURE 6.7. (a) Simulated input impedances of the slot power combiner shown in Fig. 6.4. (b) Simulated S-parameters of the slot power combiner.

CMOS process at 200 GHz as shown in Fig. 6.10. The matched-cascode amp-cell allows higher voltage swing at the output port, and hence higher output power when compared to a traditional common-source amp-cell. The implementation of neutralizing capacitors for the proposed amp-cell would need very small capacitors with long transmission line routings, because of the amp-cell dimensions. Therefore, neutralizing circuit of the proposed amp-cell would become ineffective.

To maximize the DC efficiency and improve the power gain of the driver stages, the sizes



(a)



(b)

FIGURE 6.8. (a) Changes in the insertion loss and input impedance of the slot power combiner by geometry. SPC is the response of the slot power combiner shown in Fig. 6.4 (b) Changes in the return loss.

of the transistors are reduced towards the input of the PA. The gate biasing voltages of the M1 and M2 (Fig. 6.10) of the driver stages are selected to be slightly lower than the last stages', because it would improve the power gain, and reduce the DC power consumption. In the last stages, higher biasing voltages are chosen to improve the output power of the PA. The first four driver amp-cells have a simulated gain power gain of 6.9dB and an OP1dB of 3.1dBm. The amp-cells of stages 5 and 6 have a simulated power of 5.9dB, and an OP1dB

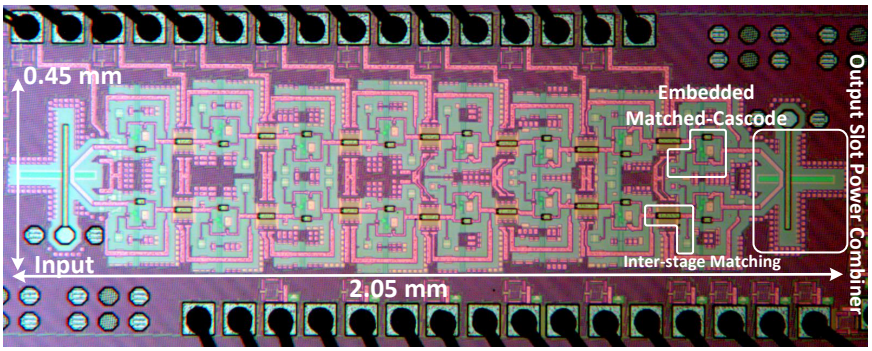


FIGURE 6.9. Die micro-photograph of the PA.

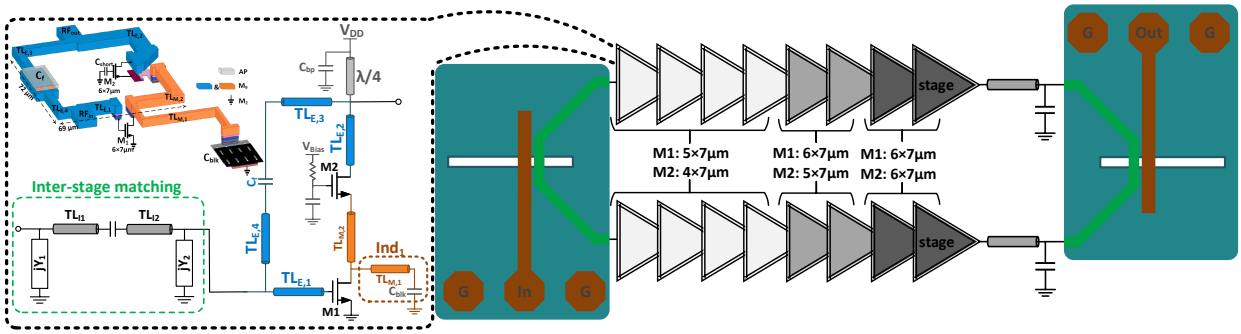
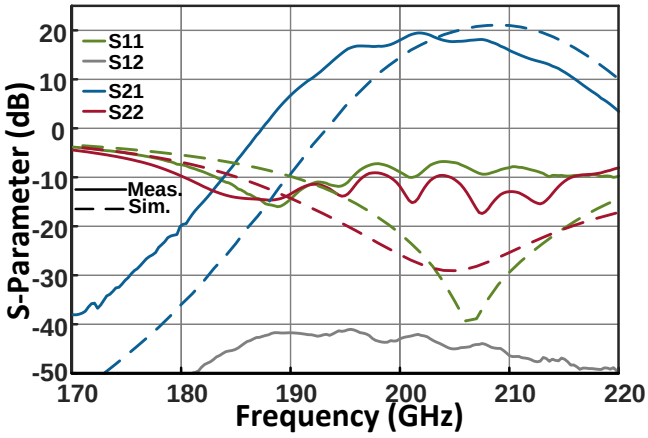


FIGURE 6.10. The proposed 2-by-8 embedded power amplifier (right), the amp-cell and its layout along with the matching network (left). Each 7um transistor has 10 fingers, and each finger has a length of 0.7um.

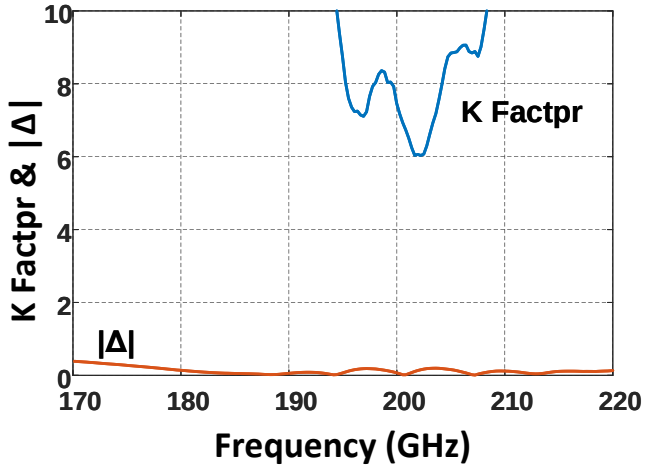
of 6.2dBm.

The slot power combiner shown in Fig. 6.4 is used at the output port of the two power amplification paths to boost the output power. The same slot power combiner is used at the input port as well. To conserve the gain of amp-cells, all of them are matched to their complex conjugate impedances. A capacitor or inductor is used for jY_1 and jY_2 in the inter-stage matching networks when needed. All the PA cells are provided with a V_{Sup} of 2.4V. With a correct gate biasing voltages, simulation shows that the maximum voltage swing on gate-source and gate-drain junctions is 1.1V.

A PNA-X together with two VDI WR-5.1 frequency extender modules are used to measure S-parameters of the PA. The small-signal simulation and measurement results are shown in Fig. 6.11. The simulated S_{21} has a maximum of 20.7dB at 209GHz, and S_{11}/S_{22} are below



(a)



(b)

FIGURE 6.11. Simulated and measured (a) small signal S-parameters and (b) stability factors.

-10dB from from 190GHz to 220GHz. The measurement shows that the PA has a center frequency of 202GHz, at which S_{21} peaks at 19.5dB, with a 3dB bandwidth of 13.4GHz from 195.3GHz to 208.7GHz. There is 7GHz frequency shift between simulated and measured S21. This shift is caused most likely by the inaccuracies in the device interconnects and passive components modeling. The input and output reflection coefficients are less than -6.8 and -9.1 dB from 179.5 GHz to 218.4GHz, respectively. Simulated K and $|\Delta|$ satisfy unconditional stability requirements over all frequencies. The measurement results show that the PA is

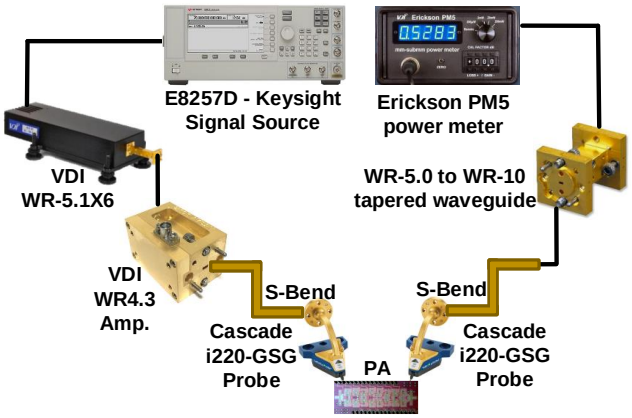
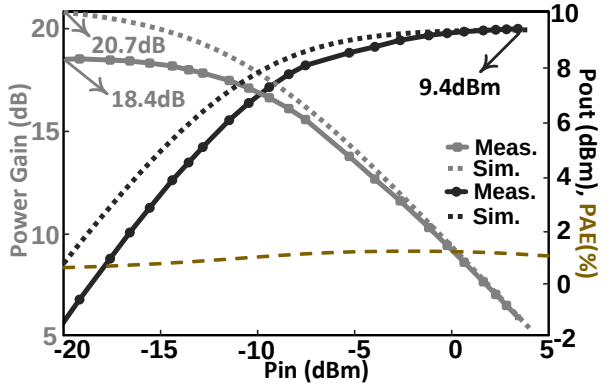


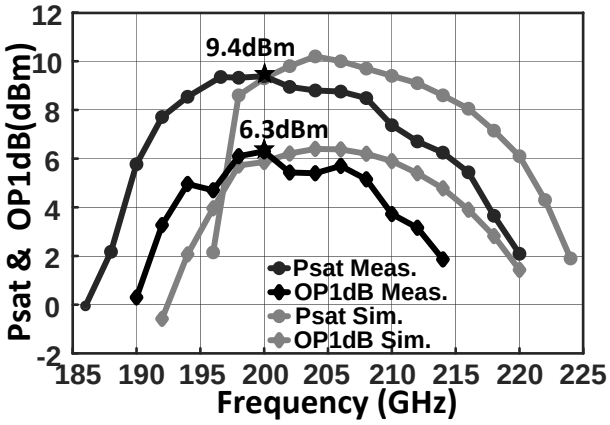
FIGURE 6.12. The large-signal measurement setup.

unconditionally stable and has a stability factor (K) larger than one, and $|\Delta|$ smaller than one from 140GHz to 220GHz.

Fig.6.12 shows the large-signal measurement setup. At low input powers the setup does not include the VDI WR4.3 amplifier, and the frequency extender, VDI WR-5.1x6, is directly connected to the S-bend. The output power of the frequency extender was measured and calibrated using a Erikson PM5 power meter from 180GHz to 220GHz. Then the S-bends and probes were added to the setup, the probes were landed on a through structure of a calibration kit and the output power of the S-bend on the right side of Fig.6.12 was measured across the same frequency band. Using these two sets of information, the loss of S-bends and probes were calibrated. Using all these calibrations and measurements the output power and power gain of the PA were measured versus the input power across the band from 180GHz to 220GHz. However, the output power of the frequency extender was not enough to saturate the PA. Hence, a VDI WR4.3 amplifier was added to the setup as shown in Fig.6.12, and the output power of the VDI WR4.3 amplifier was calibrated similar to other blocks. Fig. 6.13(a) shows that the PA has an output 1-dB compression point of 6.3 dBm, and an output saturated power of 9.4dBm at 200GHz. Shown in Fig. 6.13(b), the PA has a 1-dB P_{sat} bandwidth of 12GHz from 194GHz to 208GHz, and delivers more than 6dBm to its load



(a)



(b)

FIGURE 6.13. (a) Power gain, output power, and PAE. Simulation at 209GHz, measurement at 200GHz (b) Simulated and measured P_{sat}/OP1dB as a function of frequency.

from 191GHz to 214GHz. The output 1-dB compression point stays more than 3dBm from 192GHz to 212GHz. The power added efficiency (PAE) reaches a maximum of 1.03% at output power of 8.77dBm with a power gain of 10.74dB, as shown in Fig. 6.13(a). Table II shows the summary of the proposed embedded power amplifier performance compared to state-of-the-art. The PA features the highest gain, P_{sat}, and OP1dB in CMOS technology at ¿200GHz frequencies.

TABLE II

Reference	**This work**	[33]	[41]	[42]	[43]	[44]	[45]
Technology	**65nm CMOS**	65nm CMOS	130nm BiCMOS	130nm BiCMOS	65nm CMOS	65nm CMOS	32nm SOI CMOS
f_{max} (GHz)	**400**	352	370	500	395	395	320
3dB Bandwidth (GHz)	**195-209**	251-263	200-220	200-255	275-284[1]	227.5-257.5	205-225
Gain (dB)	**19.5 (22.5**)**	9.2	25	12.5 (15.5**)	12	13.9	15**
OP1dB (dBm)	**6.3 (7.8*)**	-8	4	9 (10.5**)	-5.9	-5.1	2.7*
P_{sat} (dBm)	**9.4 (10.9*)**	-3.9	9.6	12 (13.5**)	-4.7	-3.3	4.6*
PAE max (%)	**1.03 (1.4**)**	1.35	0.5	2.14(3**)[2]	1.62	1.6	6**
V_{DD} (V)	**2.4**	1	3.3	3.3	0.85	0.85	1
DC power (mW)	**732**	27.6	1824[1]	740	17.85	23.8	40
Active area (mm^2)	**0.92 (0.52***)**	0.14	0.84[1]	0.83	0.056	0.053	0.06***
FOM[%]	**52.1 (57.9**)**	30	54	51 (55.5)	33	36.4	50.6

PERFORMANCE COMPARISON TO STATE-OF-THE-ART.

*Loss of output balun/power combiner is de-embedded
**Loss of input and output balun/power combiner is de-embedded
*** Areas of input and output blauns as well as DC pads are not included
[1] Calculated from reported numbers and/or graphs
[2] Max. drain efficiency
[%] $FOM=P_{SAT}[dBm]+Gain[dB]+10\log(freq[GHz])+10\log(PAE_{MAX}[\%])$

CHAPTER 7

Conclusion

A general embedding is proposed to boost the power gain of an embedded active two-port to G_{max} in this thesis. The proposed technique utilizes movement in the defined gain-plane to boost the power gain. The required movements are achieved by only two passive components as parallel and series embeddings. These embeddings are analyzed and calculated for any given active two-port using only its Z-parameters. Implementation issues are investigated as well as the circuit characteristics of the embedded network. To show the feasibility of the proposed embedding, a four-stage embedded amplifier is implemented in 65 nm CMOS technology with a power gain of 9.2 dB at 260 GHz. Next, the analysis and effect of power gain, and gain boosting by embedding on the PA output power was presented. Equations for power contours of embedded amp-cells were derived and presented to help designers find the optimum embedding that maximizes the output power for a particular gain. Analyzing the power limitations of a cascode cell, a high-power, high-frequency and embedded amp-cell was introduced. Then, a wideband, balanced, series power combiner was designed and used to further boost the output power Using embedded matched-cascode amp-cells and the slot power combiner, a 200GHz PA with 19.5dB gain and 9.4dBm P_{sat} was implemented in 65nm Bulk CMOS, and its performance was reported.

APPENDIX A

A.1. Embedding Elements Calculation

To calculate the value of the final embeddings , X_{TS} and B_{TP}, we start with calculating A of the embedded A2P, A_{ET}, and we select the values of the embeddings such that the coordinate of the embedded A2P in the gain-plane is $(-\frac{U}{G_{max}}, 0)$. We suppose that the A2P in Fig. 3.5b is embedded first by X_{TS}, then by B_{TP}. Using (3.4) and (3.6), it can be shown that:

$$\begin{aligned} A_{ET} = \frac{Y_{ET,21}}{Y_{ET,12}} &= \frac{\left(-\frac{Z_{21}+jX_{TS}}{\Delta Z_{ES}}\right) + jB_{TP}}{\left(-\frac{Z_{12}+jX_{TS}}{\Delta Z_{ES}}\right) + jB_{TP}} \\ &= \frac{Z_{21} + jX_{TS} - jB_{TP}\cdot\Delta Z_{ES}}{Z_{12} + jX_{TS} - jB_{TP}\cdot\Delta Z_{ES}}, \end{aligned} \tag{A.1}$$

where Z_{ij} are the elements of the A2P impedance matrix ($\mathbf{Z}$), and ΔZ_{ES} is given by:

$$\begin{aligned} \Delta Z_{ES} =& (Z_{11} + jX_{TS})\cdot(Z_{22} + jX_{TS}) - \\ & (Z_{12} + jX_{TS})\cdot(Z_{21} + jX_{TS}). \end{aligned} \tag{A.2}$$

At the coordinate that corresponds to G_{max}, $(-\frac{U}{G_{max}}, 0)$, we have $A_{ET} = -G_{max}$, therefore,

$$-G_{max} = \frac{Z_{21} + jX_{TS} - jB_{TP}\cdot\Delta Z_{ES}}{Z_{12} + jX_{TS} - jB_{TP}\cdot\Delta Z_{ES}}. \tag{A.3}$$

(A.3) in fact consists of two equations: one the real part and the other one the imaginary part of the right-hand side of it. These equations are found to be:

$$B_{TP}\cdot Im(\Delta Z_{ES})\cdot(1 + G_{max}) + R_{12}\cdot G_{max} + R_{21} = 0, \tag{A.4}$$

and

$$j[B_{TP} \cdot Re(\Delta Z_{ES}) \cdot (1 + G_{max}) + X_{TS} \cdot (1 + G_{max}) + G_{max} \cdot X_{12} + X_{21}] = 0. \tag{A.5}$$

Solving (A.4) and (A.5) for X_{TS} and B_{TP} results in (3.9).

A.2. Proof of Equation of $K > 1$ Boundary

For $K = 1$, we have [**52**]:

$$K - \sqrt{K^2 - 1} = 1 \tag{A.6}$$

or

$$G_{ma} = |A| \,. \tag{A.7}$$

Recalling (3.2), on the boundary of $K > 1$ we have:

$$\frac{|A|}{U} = \left| 1 - \frac{|A|}{U} \cdot Re\left(\frac{U}{A}\right) - j\frac{|A|}{U} \cdot Im\left(\frac{U}{A}\right) \right|^2 . \tag{A.8}$$

Hence

$$\frac{|A|}{U} = 1 - 2\left|\frac{A}{U}\right| \cdot Re\left(\frac{U}{A}\right) + 1; \tag{A.9}$$

i.e.,

$$\frac{1}{2} = \left|\frac{U}{A}\right| - Re\left(\frac{U}{A}\right); \tag{A.10}$$

i.e.,

$$\left(\frac{1}{2} + Re\left(\frac{U}{A}\right)\right)^2 = \left|\frac{U}{A}\right|^2; \tag{A.11}$$

which results in:

$$\frac{1}{4} + Re\left(\frac{U}{A}\right) = \left(Im\left(\frac{U}{A}\right)\right)^2. \tag{A.12}$$

APPENDIX B

Embedding for Maximum Output Power

To find the coordinate of an equi-gain arc that results in the maximum output power, the equations of T-embedding in [**6**] must be generalized to move the amp-cell to any arbitrary coordinate in the gain-plane. Once the generalized equations are derived, one can plug in all the coordinates of an equi-gain curve, and by using the analysis in Chapter 5 find the coordinate with the maximum output power i.e. maximum G_L. The generalized equations of T-embedding are driven as follow. In these equations, (H,V) is any desired coordinate in the gain-plane, and $Z_{i,j}$'s are the Z-parameters of the amp-cell.

$$X_{TS} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}, \tag{B.1}$$
$$B_{TP} = (C_5 \times X_{TS} + C_6)/(C_3 \times X_{TS} + C_4)$$

where

$$a = C_1 \times C_3 + C_5 \times C_7,$$
$$b = C_1 \times C_4 + C_2 \times C_3 + C_5 \times C_8 + C_6 \times C_7, \tag{B.2}$$
$$c = C_2 \times C_4 + C_6 \times C_8,$$

where

$$
\begin{aligned}
C_1 &= U - H, \\
C_2 &= U \times Im(Z_{12}) - V \times Re(Z_{21}) - H \times Im(Z_{21}), \\
C_3 &= (H - U) \times A - V \times B, \\
C_4 &= (H - U) \times Im(\Delta Z) + V \times Re(\Delta Z), \\
C_5 &= -V, \\
C_6 &= H - 1, \\
C_7 &= (H - U) \times B + V \times A, \\
C_8 &= (U - H) \times Re(\Delta Z) + V \times Im(\Delta Z),
\end{aligned}
\tag{B.3}
$$

where

$$
\begin{aligned}
A &= Re(Z_{11}) + Re(Z_{22}) - Re(Z_{12}) - Re(Z_{21}), \\
B &= Im(Z_{11}) + Im(Z_{22}) - Im(Z_{12}) - Im(Z_{21}), \\
\Delta Z &= Z_{11}Z_{22} - Z_{12}Z_{21},
\end{aligned}
\tag{B.4}
$$

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