UNIVERSITY OF CALIFORNIA

Santa Barbara

Evaluating MIS- and Schottky- Gate Structures for N-polar GaN HEMTs

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in

Electrical and Computer Engineering

by

Wenjian Liu

Committee in charge:

Professor Umesh K. Mishra, Chair

Professor Steve P. DenBaars

Professor Mark J. Rodwell

Professor Chris Van de Walle

Dr. Brian R. Romanczyk

June 2022

The dissertation of Wenjian Liu is approved:

_____

Prof. Steven P. DenBaars

_____

Prof. Mark J. Rodwell

_____

Prof. Chris Van de Walle

_____

Dr. Brian R. Romanczyk

_____

Prof. Umesh K. Mishra, Committee Chair

March 2022

This page is optional]

Evaluating MIS- and Schottky- Gate Structures for N-polar GaN HEMTs

by

Wenjian Liu

ACKNOWLEDGEMENTS

With all the help and support from so many individuals, it has been a fun and fortunate journey for me during the years at UCSB. Sitting in front of the blue Pacific Ocean and enjoying the soft breeze, I deeply appreciate the whole experience I had and more importantly, the people who created the environment of my experiencing.

First and foremost, I would like to sincerely thank my advisor, Prof. Umesh Mishra for accepting me as a member of his "GaN electronics" family when I was not sure about working on previous research topics. Working in his research group with topics from materials to device to circuit level, I am truly grateful to the amount of freedom and guidance he provided. The training of "being a processer" in his group has been beneficial for me to learn to work with certainty and uncertainty consistently along a long journey. His passion, optimism and hard-working have shown me how to achieve success and inspired me how to deal with probably everything in life. I am very proud of being a part of his group and happily ready to face challenges in the future.

I would also like to thank Prof. Steven DenBaars, Prof. Mark Rodwell and Prof. Chris Van de Walle for serving in my committee. Their wealth of knowledge on the MOCVD, RF circuit and physic helped me connect my research topics better. I am very thankful to their insights and guidance along the way. I would like to express special thanks to Dr. Brian Romanczyk for many hands-on trainings. I still remember the fast response he gave when some unexpected issues happened during the fabrications. His deep understanding on the deep recess N-polar GaN HEMT is priceless. I would like to acknowledge Dr. Paul Maki (ONR) and Dr. Young-Kai Chen (DARPA) for funding this work.

I thank Dr. Islam Sayed very much, who was a “dynamic dual” of mine at UCSB. The N-polar GaN diode epis in this work were grown by him. We worked together on diode studies and had many great discussions. The last things I could forget are these moments when we looked into interesting data and tried to propose models to explain them. It has also been a great fun playing tennis with Islam and Brian. I would like to thank Matt Guidry for helping measure HEMT devices and passing me his knowledge on various measurements. My sincere thanks also go to Stacia Keller for her insightful guidance on N-polar GaN epi growth and constant optimism. I also thank other DREaM HEMT team players, including Xun, Pawana, Weiyi, Emre and Henry, for giving so many good thoughts and advice for the projects. I thank Nirupam Hatui for providing the MOCVD N-polar GaN HEMT epi and Christian Wurm for MBE n+ regrowth.

I have been extremely lucky to work with current and past members in the Mishra Group. It has been great experience to go through all the ups and downs with you. Along the way, I thank Islam, Chirag, Xun, Brian, Matt, Silvia, Onur, Haoran, Niru, Steven, Pawana, Shubhra, Weiyi, Christian, Aditya, Athith, Emmanuel, Henry, Christopher, Emre, Bobby, Boyu, Johnny. I would also like to thank Prof. Elaheh Ahmadi at University of Michigan and her team including Kam, Ashley, and Subhajit, for our fruitful collaboration. I would also like to thank Prof. Jim Buckwalter and Rohit for collaborating on DREaM project.

I would also like to thank the diligent and knowledgeable UCSB Nanofab staff for maintaining a world-class university fabrication cleanroom. Bill Mitchell, Don, Aidan, Brian Lingg, Biljana, Ning, Brian Thibeault, Mike and Lee helped me solve various tool issues and made my processing work much easier. I would like to thank Val and other administrative staff at ECE department for their assistance during the journey.

Last but not least, I would like to acknowledge the unwavering support from my friends and family. It would be impossible for me to achieve this step without all your help. While writing the acknowledgements, I felt extremely lucky to have your companion along the way. Many sweet memories came back to my mind, and I know that is the taste of happiness.

VITA OF WENJIAN LIU

March 2022

EDUCATION

Ph.D., Electrical and Computer Engineering 2022
University of California Santa Barbara, CA, U.S

Master, Materials Science and Engineering 2017
Tsinghua University, Beijing, China

Bachelor, Mechanical Engineering 2015
Tsinghua University, Beijing, China

EXPERIENCE

1. Dynamic Range-enhanced Electronic and Materials (DREaM) using Nitrogen-polar Gallium Nitride material. (Graduate Student Researcher, Advisor: Prof. Umesh Mishra, ONR/DARPA)

- Design, fabricate, and measured N-polar GaN High Electron Mobility Transistor with gate length of sub-50nm targeting 94 GHz applications.
- Achieved high output power of 6.2 W/mm and record-high efficiency (PAE) of 33.8% at 94 GHz.

2. MOS and Schottky structures on N-polar GaN for high-frequency and high-power applications. (Graduate Student Researcher， Advisor: Prof. Umesh Mishra, ONR)

- Proposed a dielectric analysis methodology including bulk and interface traps on wide bandgap semiconductors.
- Studied the reliability of MOCVD grown AlSiO and SiN on N-polar GaN under voltage stress and annealing conditions.
- Developed Ruthenium as the first excellent Schottky gate metal on N-polar Gallium Nitride HEMT.

3. Teaching Assistant/Reader, Department of Electrical and Computer Engineering, University of California, Santa Barbara.

- ECE 221A/221B, graded the homework assignments and exams 1/2020 – 3/2020
- ECE 10A/10AL, held office hours, taught discussion sections, lead lab sessions, graded assignments and exams 9/2019 – 12/2019

JOURNAL PUBLICATIONS

- **Wenjian Liu,** Brian Romanczyk, Matthew Guidry, Nirupam Hatui, Christian Wurm,

Weiyi Li, Pawana Shrestha, Islam Sayed, Stacia Keller, Umesh K. Mishra, Ru/N-polar GaN Schottky-HEMT with 27% PAE and 4.87 W/mm at 94 GHz. (Submitted to *IEEE Electron Device Letters*).

- Aditya Raj, Athith Krishna, Brian Romanczyk, Nirupam Hatui, **Wenjian Liu**, Stacia Keller, and Umesh K. Mishra, GaN/AlGaN superlattice based E-mode hole channel FinFET with Schottky gate. (Submitted to *IEEE Electron Device Letters*).

- **Wenjian Liu,** Brian Romanczyk, Matthew Guidry, Nirupam Hatui, Christian Wurm, Weiyi Li, Pawana Shrestha, Xun Zheng, Stacia Keller, Umesh K Mishra, 6.2 W/mm and Record 33.8% PAE at 94 GHz from N-polar GaN Deep Recess MIS-HEMTs with ALD Ru Gates. *IEEE Microwave Wireless Component Lett.*, vol. 31, no. 6, pp. 748-751, June 2021.

- Zhe Jian, Islam Sayed, Subhajit Mohanty, **Wenjian Liu,** Elaheh Ahmadi, Improved operational reliability of MOCVD-grown AlSiO gate dielectric on β-Ga2O3 (001) by post-metallization annealing, *Semiconductor Science & Technology*, vol. 36, no. 9, July 2021.

- Henry Collins, Islam Sayed, **Wenjian Liu,** Shubhra S Pasayat, Aidan A Taylor, Weiyi Li, Stacia Keller, UK Mishra, Investigation and optimization of N-polar GaN porosification for Regrowth of smooth hillocks-free GaN films. *Applied Physics Letters*, 119, 042105 (2021).

- Zhe Jian, Islam Sayed, **Wenjian Liu,** Subhajit Mohanty, Elaheh Ahmadi, Characterization of MOCVD-grown AlSiO gate dielectric on β-Ga2O3 (001), *Applied Physics Letters*, 118, 172102(2021).

- **Wenjian Liu**, Islam Sayed, Jana Georgieva, Silvia Chan, Stacia Keller, Umesh K Mishra, A systematic and quantitative analysis of the bulk and interfacial properties of the AlSiO dielectric on N-polar GaN using capacitance–voltage methods. *Journal of Applied Physics*, 128, 074101(2020).

- Islam Sayed, **Wenjian Liu**, Jana Georgieva, Athith Krishna, Stacia Keller, Umesh K Mishra, Characterization of AlSiO dielectrics with varying silicon composition for N-polar GaN-based devices. *Semiconductor Science and Technology*, 35, 095027(2020).

- **Wenjian Liu**, Islam Sayed, Brian Romanczyk, Nirupam Hatui, Matthew Guidry, William J Mitchell, Stacia Keller, Umesh K Mishra, Ru/N-Polar GaN Schottky Diode with Less Than 2 μA/cm² Reverse Current, *IEEE Electron Device Letters*, 41, 1468-1472(2020). (**Cover paper**)

- Islam Sayed, **Wenjian Liu**, Brian Romanczyk, Jana Georgieva, Silvia Chan, Stacia Keller, Umesh K Mishra, Improved operation stability of in-situ AlSiO dielectric grown on (000-1) N-polar GaN by MOCVD. *Applied Physics Express*, 13, 6(2020).

- **Wenjian Liu**, Islam Sayed, Brian Romanczyk, Nirupam Hatui, Jana Georgieva, Haoran Li, Stacia Keller, Umesh K Mishra, Near-ideal Ru/N-polar GaN Schottky diode with ultralow reverse leakage, *Device Research Conference (DRC)*, July 2020, doi: 10.1109/DRC50226.2020.9135165.

- Islam Sayed, **Wenjian Liu**, Silvia Chan, Chirag Gupta, Haoran Li, Stacia Keller, Umesh K Mishra, Flat-band voltage stability and time to failure of MOCVD-grown SiO2 and Si3N4 dielectrics on N-polar GaN, *Applied Physics Express*, 12, 121001(2019).

- Islam Sayed, Bastien Bonef, **Wenjian Liu**, Silvia Chan, Jana Georgieva, James S Speck, Stacia Keller, Umesh K Mishra, Electrical properties and interface abruptness of AlSiO gate dielectric grown on 000 1^{-} N-polar and (0001) Ga-polar GaN, *Applied Physics Letters*, 115, 172104(2019).

- **Wenjian Liu**, Islam Sayed, Chirag Gupta, Haoran Li, Stacia Keller, Umesh Mishra, An improved methodology for extracting interface state density at Si3N4/GaN. *Applied Physics Letters*, 116, 022104(2020).

- Islam Sayed, **Wenjian Liu**, Silvia Chan, Chirag Gupta, Matthew Guidry, Haoran Li, Stacia Keller, Umesh Mishra, Net negative fixed charge for Si_3N_4 and SiO_2 grown in-situ on 000-1 N-polar GaN. *Applied Physics Letters*, 011928(2019).

- Yingqi Zhang, Shaofan Zhao, Cheng Song, **Wenjian Liu**, Kefu Yao, Na Chen, Electrical-field control of ferromagnetism in a Co-Fe-Ta-B amorphous alloy, *Materials & Design*, 143(2018).

- Xue Liu, Hao Liu, Dong Wang, En-Peng Wang, **Wenjian Liu**, Kefu Yao, Na Chen, Metallic glass strengthening thermoplastic elastomer composites with enhanced wear resistance. *Physica E: Low-dimensional Systems and Nanostructure*, 90(2017).

- Na Chen, Hongping Li, Akihiko Hirata, Zhaochu Luo, Zhongchang Wang, **Wenjian Liu**, et al. "Transparent magnetic semiconductor with embedded metallic glass nano-granules". *Materials & Design*, 132(2017).

- **Wenjian Liu,** Hongxia Zhang, Jin-an Shi, Zhongchang Wang, Cheng Song, Xiangrong Wang, Siyuan Lu, Xiangjun Zhou, Lin Gu, Dmitri V. Louzguine-Luzgin, Mingwei Chen, Kefu Yao, Na Chen, A room temperature magnetic semiconductor from a ferromagnetic metallic glass, ***Nature Communications*** 7, 13497(2016).

CONFERENCES

- Weiyi Li, Brian Romanczyk, Matthew Guidry, **Wenjian Liu**, Stacia Keller and Umesh K. Mishra, A physics-based model on transport for N-polar GaN deep recess HEMT, *Compound Semiconductor Week*, 2022 (submitted)

- Weiyi Li, Tsung-Yin Tsai, Brian Romanczyk, Matthew Guidry, **Wenjian Liu**, Stacia Keller, Yuh-renn Wu, and Umesh K. Mishra, Effects of strain on electron effective mass in GaN and performance GaN HEMT, *Compound Semiconductor Week*, 2022 (submitted)

- M. Guidry, P. Shrestha, **W. Liu**, B. Romanzyk, N. Hatui, C. Wurm, R. Karnaty, S. Keller, J. F. Buckwalter, and U. K. Mishra, Improving N-polar GaN MISHEMTs for mm-Wave Transmitter and Receiver Applications, *GOMACTech* 2022. (Accepted)

- **Wenjian Liu**, Brian Romanczyk, Matthew Guidry, Nirupam Hatui, Christian Wurm, Weiyi Li, Pawana Shrestha, Islam Sayed, Stacia Keller, Umesh K. Mishra, mm-wave N-polar GaN Schottky-HEMTs with ALD Ru on the AlGaN cap layer, *Lester Eastman Conference (LEC)*, 2021.

- **Wenjian Liu,** Brian Romanczyk, Matthew Guidry, Nirupam Hatui, Christian Wurm, Weiyi Li, Pawana Shrestha, Islam Sayed, Stacia Keller, Umesh K. Mishra, Ru/N-polar GaN Schottky-HEMT with 27% PAE and 4.87 W/mm at 94 GHz. *2021 Device Research Conference* (DRC).

- Islam Sayed, **Wenjian Liu,** Silvia Chan, Stacia Keller, Umesh K. Mishra, MOCVD-based Dielectrics on GaN, *IEEE Semiconductor Interface Specialists Conference (SISC)*, 2021.

- Matthew Guidry, Brian Romanczyk, Pawana Shrestha, Xun Zheng, Nirupam Hatui, Christian Wurm, Rohit Karnaty, **Wenjian Liu,** et al., N-polar GaN Deep Recess MISHEMTs: A Device technology for high power, high linearity and low noise at mm-wave frequencies, *GOMACTech* 2021.

- Aditya Raj, Athith Krishna, Brian Romanczyk, Nirypam Hatui, **Wenjian Liu,** Stacia Keller, and Umesh K. Mishra, GaN/AlGaN supperlattice based E-mode p-channel MES-FinFET, *2021 Device Research Conference* (DRC).

- Zhe Jian, Islam Sayed, **Wenjian Liu,** Subhajit Mohanty, Elaheh Ahmadi, Electrical Properties of MOCVD-Grown AlSiO Gate Dielectric on (001) β-Ga_2O_3, *The 62nd Electronic Materials Conference (EMC)*, 2021.

- **Wenjian Liu,** Brian Romanczyk, Matthew Guidry, Nirupam Hatui, Christian Wurm, Weiyi Li, Pawana Shrestha, Xun Zheng, Stacia Keller, Umesh K Mishra, 6.2 W/mm and Record 33.8% PAE at 94 GHz from N-polar GaN Deep Recess MIS-HEMTs with ALD Ru Gates. *International Microwave Symposium (IMS)* 2021.

- **Wenjian Liu**, Islam Sayed, Brian Romanczyk, Nirupam Hatui, Jana Georgieva, Haoran Li, Stacia Keller, Umesh K Mishra, Near-ideal Ru/N-polar GaN Schottky diode with ultralow reverse leakage, *2020 Device Research Conference (DRC)*.

- **Wenjian Liu,** Islam Sayed, Jana Georgieva, Silvia Chan, Stacia Keller, Umesh K Mishra, Analysis of the Bulk and Interfacial Properties of AlSiO Grown on N-Polar GaN. *The 62nd Electronic Materials Conference (EMC)*, 2020.

- Islam Sayed, **Wenjian Liu**, Silvia Chan, Chirag Gupta, Matthew Guidry, Haoran Li, Stacia Keller, Umesh K. Mishra, Exploring the electrical properties of SiO2 and SiN on (000-1) N-polar GaN, *International Conference on Nitride Semiconductors (ICNS)*, 2019.

- **Wenjian Liu,** et al., Magneto-transport properties of a ferromagnetic metallic glass, IUMRS-ICA2016, Qingdao, China, 2016.

PATENT APPLICATIONS

N-polar III-N semiconductor device structures, filed by Brian Romanczyk, Emmanuel Kayede, **Wenjian Liu**, Islam Sayed, and Umesh K. Mishra. Application number: 17/352,139.

AWARDS

Outstanding TA award, ECE, University of California, Santa Barbara, 2020

ABSTRACT

Evaluating the MIS- and Schottky- Gate Structures for N-polar GaN-HEMTs

Wenjian Liu

GaN-based high electron mobility transistors (HEMTs) and monolithic microwave integrated circuits (MMICs) have emerged as a leading technology for power amplification at high frequency. N-polar GaN-based HEMTs are very promising to achieve high output power and high efficiency for solid-state millimeter wave power amplifiers. The advantages come from both the GaN material, and the polarization engineering enabled by the N-polar orientation. Harnessing these advantages, Romanczyk et al. reported a record-high 8.84 W/mm power density at 94 GHz from a N-polar GaN deep-recessed HEMT with a SiN gate dielectric.

To further boost the high-frequency and high-power performance in N-polar GaN HEMTs, improving the gate structure is critical to enhancing both stability and gain during device operation. This dissertation is devoted to the evaluation of gate structures on N-polar GaN including MIS- and Schottky structures. Part of the evaluation is conducted through the MIS-capacitor and Schottky diode structures to understand the interface properties. Another part of the evaluation wis in the form of N-polar GaN deep recess HEMTs to pursue the high performance at 94 GHz.

A series of MIS- capacitors consisting of SiN and AlSiO with different thicknesses on N-polar GaN were fabricated to investigate their interface states. An improved model combining the effects from interface states and bulk hole traps is proposed to extract the

interface state density accurately. Based on the model, the D_{it} can be obtained by extrapolating the trap density to a zero-thickness dielectric. The average D_{it} value and the bulk trap parameters can be thereby quantified. The results, model and analysis presented provide new insights into studying D_{it} of various dielectrics on GaN and other wide-bandgap semiconductors.

Schottky barrier diode of ruthenium (Ru) deposited by atomic layer deposition on N-polar GaN was investigated. The Schottky diodes showed near-ideal thermionic current behavior under forward bias and reverse bias at various temperatures. The barrier height was extracted to be 0.77 eV at room temperature. The combination of the 0.77 eV barrier and thermionic current characteristic resulted in < 2 μA/cm^2 reverse current at -5 V, which is a record-low value for N-polar GaN Schottky diodes.

ALD Ru gate was adopted into the N-polar GaN deep recess MIS- and Schottky HEMTs. The ALD Ru effectively fills the narrow T-gate stems aiding realization of shorter gate lengths with lower gate resistance than in prior work. For the ALD Ru MIS-HEMTs, the gate length was scaled down to 48 nm resulting in the demonstration of a record-high 8.1 dB linear transducer gain measured at 94 GHz by load-pull techniques. This increased gain has enabled a record 33.8% power-added efficiency (PAE) with an associated output power density (P_O) of 6.2 W/mm. The Ru/N-polar GaN Schottky-HEMT operating at W-band has also shown good large signal performance. The fabricated Schottky HEMT with L_G of 60 nm has a high peak extrinsic transconductance of 798 mS/mm with a gate leakage in pinch-off below 3×10^{-4} A/mm at V_{DS} = 5V. The Schottky-HEMT shows high PAE of 27.1% and P_O of 4.87 W/mm at 94 GHz and $V_{DS,Q}$ = 16V. The peak PAE is 31.8% with associated P_O of 3.31 W/mm at $V_{DS,Q}$ = 12V.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Chapter 1. Introduction and Motivation

In this chapter, the introduction of the development from Gallium Nitride (GaN) materials to the N-polar GaN high electron mobility transistors (HEMTs) are presented. In addition to its revolutionary impact on photonics, GaN-based material system has also emerged as a leading technology in electronics targeting high power and high efficiency applications. At mm-wave frequency (30GHz-300GHz), N-polar GaN deep recess MIS-HEMTs stands out with exceptionally high output power density and high efficiency through continuous improvements in epitaxial structure and device design. With these optimizations, this dissertation moved further on and focuses on evaluating different gate structures on N-polar GaN and their utilizations in deep recess N-polar GaN HEMTs.

1.1 GaN Material System and Applications

GaN is a direct bandgap III-V semiconductor, consisting of group-III element Gallium (Ga) and group-V element Nitrogen (N). In its common wurtzite crystal structure, GaN has a bandgap of 3.4 eV at room temperature, which has enabled many applications in photonics and electronics. In photonics, GaN in combination with InGaN enabled blue light emission and led to the invention of blue light emitting diodes (LED), which revolutionized the lighting and display industry [1-3]. When GaN is alloyed with other group-III elements Al and In, $Ga_xAl_yIn_zN$ (x+y+z=1) is formed and can be grown epitaxially. By adjusting the composition of Ga, Al, In, the bandgap of $Ga_xAl_yIn_zN$ can span from 0.6 eV (InN) to 6.2 eV (AlN) [4-6]. This bandgap range covers the light emission spectrum from infrared to deep UV as shown in **Fig. 1.1**. With the technological advancement made in GaN-based LEDs, the lighting industry has produced efficient and high-brightness LED products for indoor and outdoor lighting,

automotive lighting, disinfecting lighting and displays. Furthermore, driven by strong demand in smart watches, mobile phones, TVs, augmented reality and virtual reality, advanced display using micro-LED (μ-LED) is predicted to soar from 0.6 billion dollars in 2021 to 21.2 billion dollars in 2027 according to the Research and Markets report [7].

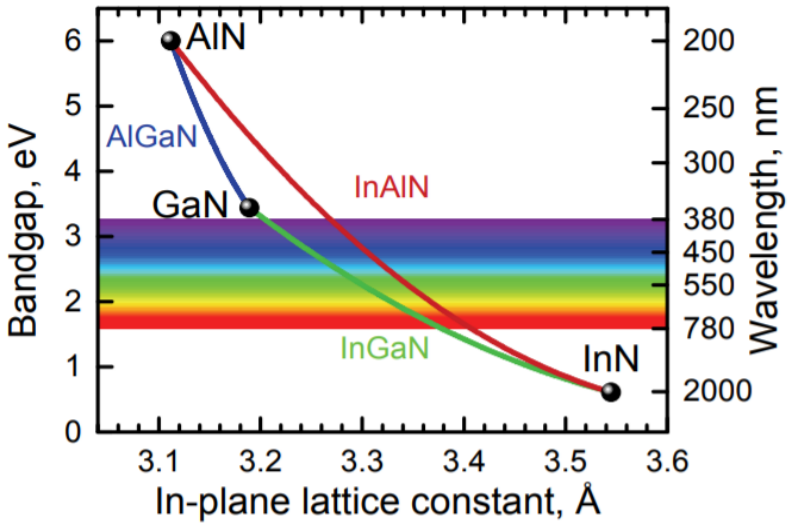


Figure 1.1 Bandgaps of wurtzite GaN, AlN and InN and their alloys versus their lattice constant at 300K [6].

Along with the improved material quality, reduced cost and enormous applications of GaN photonics, the relatively mature Ga-polar GaN-based material system has also been widely deployed in electronic devices, mainly for power conversion and radio frequency (RF) solid state power amplification [8-10]. As listed in **Table 1.1**, GaN has outstanding properties for high power and high-efficient electronic devices. Compared with other semiconductors such as Si, GaAs and SiC, the 3.4 eV bandgap helps GaN electron devices operate at high temperature, survive higher critical electric field and hold higher voltage for the same spacing. In a typical AlGaN/GaN high electron mobility transistor (HEMT) structure, a polarization charge is induced by the AlGaN/GaN interface, and a two-dimensional electron gas (2DEG)

is induced in GaN. The 2DEG has a high sheet charge density, in the order of 10^{13} cm^{-2}, high electron mobility of ~ 2000 cm^2/ (V s) and saturated electron velocity of ~2.5×10^7 cm/s. The high sheet charge density, high electron mobility and saturated electron velocity result in high current density and low on-resistance in GaN-based transistors.

Table 1.1 Material properties of related to power performance for different semiconductors [8,11]

	Eg(eV)	ε_r	μ_n(cm^2/Vs)	V_{sat}(10^7 cm/s)	E_{br}(MV/cm)	Θ(W/cm K)
Si	1.1	11.8	1350	1.0	0.3	1.5
GaAs	1.42	13.1	8500	1.0	0.4	0.43
4H-SiC	3.2	10	700	2.0	3.0	3.3-4.5
GaN	3.4	9.0	1200 (Bulk) 2000 (2DEG)	2.5	3.3	1.3
β-Ga2O3	4.9	10	300	1.1	8.0	0.11

GaN applications in power devices:

During electric power conversion from DC/AC to DC/AC, the switching behavior of power electronics (typically in the frequency range of kHz to MHz) is not 100% electrically efficient and will cause conversion loss. The conversion loss occurs in on-state, off-state and on-off transitions. The loss is manifest in the form of heat and requires cooling systems. The inefficient conversion decreases the battery life, needs more power generation, and could potentially worsen global warming issue.

To achieve high efficiency during the power conversion, two basic requirements for transistors are high breakdown voltage (V_{br}) and low on-state resistance (R_{on}) [12]. For a given power needed to be transmitted, a high voltage implies a low current. With a low current, less

I^2R power is wasted as heat. For devices with a combination of low on-state resistance and low switching capacitances, there will be less power consumed by the transistor itself during the transition and on-state. Therefore, three characteristics -- high breakdown voltage, low capacitance, and low on-state resistance, will make the transistors switch more energetically efficient. GaN material system can be made into various device structures and achieve these requirements due to its high critical electric field, high mobility, and high charge density. Several high-efficient commercial GaN power electronics have entered the market, such as miniaturized mobile device charging adapter, data center power supplies, etc. There is also significant potential for GaN power electronics used in the power management of electrical vehicles as GaN power devices are competitive with Si-based and SiC-based power devices.

GaN applications in RF power amplifiers:

While GaN power devices are typically used at frequency up to ~10 MHz, GaN radiofrequency (RF) devices usually operates at higher frequency up to hundreds of GHz. As the frequency increases, the power generation is becoming more and more challenging especially at mm-wave frequencies. The combination of high current density, high critical electric field and high electron mobility and velocity makes GaN well-suited for power amplification at high frequency. Through a literature survey, the GaN HEMTs have been compared with other compound semiconductors in RF power amplification. As shown in **Fig. 1.2**, GaN in chip-level can generally provide higher output power than GaAs and InP at the same frequency [13].

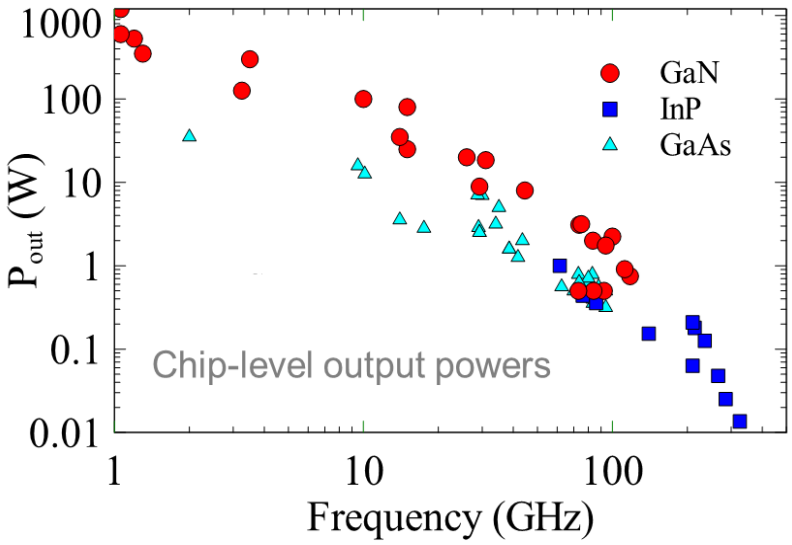


Figure 1.2 Chip-level Output power density versus frequency for GaN, InP and GaAs from literature [Credits to Dr. Brian Romanczyk and Dr. Matt Guidry]

Power amplification at high frequency requires several metrics to evaluate the device performance. There are four typical parameters used widely as criteria: 1) current gain cut-off frequency f_T; 2) power gain cut-off frequency f_{max}; 3) output power density, P_O; 4) power added efficiency, *PAE*. f_T and f_{max} are small-signal figures of merit. Intrinsic f_T can be mathematically expressed as:

$$f_{T,int} = \frac{1}{2\pi\tau} = \frac{v}{2\pi L_G} \tag{1.1}$$

where τ is the electron transit time from source to drain, v is the velocity of electron travelling through the gate and L_G is the gate length. f_T reflects the time needed for electron travelling from source to drain and can limit the speed of device operation. f_T can also be expressed in the language of capacitance and resistance. From the experimental data, f_T will be extracted when the magnitude of measured small signal short-circuit current gain $/h_{21}/^2$ is extrapolated to unity (0 dB) following -20 dB/dec line versus the frequency. Effectively scaling down L_G will reduce the transit time and increase the f_T.

f_{max} is defined as the frequency where the Mason's unilateral power gain (U) becomes unity (0dB). In a field effect transistor device circuit model, the f_{max} can be derived as the formula below:

$$f_{max} = \frac{f_T}{\sqrt{\frac{4(R_S+R_g+R_{ds})}{R_{ds}}+2\pi f_T R_g C_{gd}}} \tag{1.2}$$

From experimental measured small signal results, f_{max} can be obtained through the fitting line of U versus frequency with -20 dB/dec line. High f_t, small R_s, small R_g and high R_{ds} is beneficial to obtain high f_{max}.

Typical power amplifiers operate at large signal with large voltage and current swing. P_O and PAE reflects the large signal performance of devices. Output power P_O can be approximately calculated as:

$$P_O = \frac{1}{4}\,(V_{DS,Q} - V_{knee})I_{knee} \tag{1.3}$$

where $V_{DS,Q}$ is the quiescent voltage, V_{knee} is the knee voltage and I_{knee} is the maximum saturation drain current during the device operation at the frequency. High $V_{DS,Q}$, low V_{knee} and high I_{knee} will be desired to maximize the output power.

PAE is defined as:

$$PAE = \frac{P_O - P_{IN}}{P_{DC}} = (1 - \frac{1}{G})\frac{P_O}{P_{DC}} \tag{1.4}$$

where the P_O is the RF output power, P_{IN} is the RF input power and P_{DC} is the DC power consumption of the transistor at the operation frequency which is determined in large part by the quiescent bias condition ($I_{DS,Q}$ and $V_{DS,Q}$) of the device. G is defined as the gain, which represents the ratio between P_O and P_{IN}. PAE illustrates the efficiency by which a transistor

converts DC and input RF power to a high output RF power. High gain at low quiescent bias can lead to high PAE since the P_{DC} stays in low level.

To fulfill these four metrics above, GaN RF devices have been developed for the past decades in both academic research and commercial products. In 1994, Khan et al. [14] demonstrated AlGaN/GaN HEMT with scaled gate length of 0.25 um and f_T of 11 GHz and f_{max} of 140 GHz. In 1996, Wu et al. [15] reported the first AlGaN/GaN HEMT power performance at 2 GHz and the device had P_o of 1.1 W/mm and PAE of 18.6% with a 1 um gate length. Furthermore, the SiN passivation to reduce the DC-RF dispersion and field-plate to relieve the peak electric stress technology enabled a high-power density of 41 W/mm at 4 GHz in 2006 [16]. However, these two technologies added extra parasitic capacitance and hindered the performance at higher frequencies. Development around the further gate scaling, regrown source/drain contact and recess-trench gating helped researchers achieved Pout of 10.5W/mm and PAE of 33% at 40GHz [17], 13.7 W/mm with associated 40% PAE [18], and a high PAE of 55% [19] in the past. At higher mm-wave frequencies, a GaN based MMIC showed a peak PAE of 27% and P_O of 1.7 W/mm at 83 GHz [20]. At 94 GHz, Brown et al. demonstrated 24.2% PAE and 1.5 W/mm P_O in a pre-matched device [21]. At 96 GHz, Niida et al. reported 3.6 W/mm P_O and 12.7 PAE using quaternary AlInGaN barrier [22].

In the market, companies provide various GaN-based RF products operating at high frequencies. The advantages in high current density and high voltage swing at high frequency enabled the GaN-based MMIC to operate with high efficiency in a smaller die area. As shown in **Fig. 1.3**, For a similar Ka-band power amplifier, Qorvo GaN product has ¼ area of GaAs counterpart, while offering more power and more efficiency [23]. The miniature of circuit and

possible longer transmission distance due to high power are great advantages of GaN RF electronics.

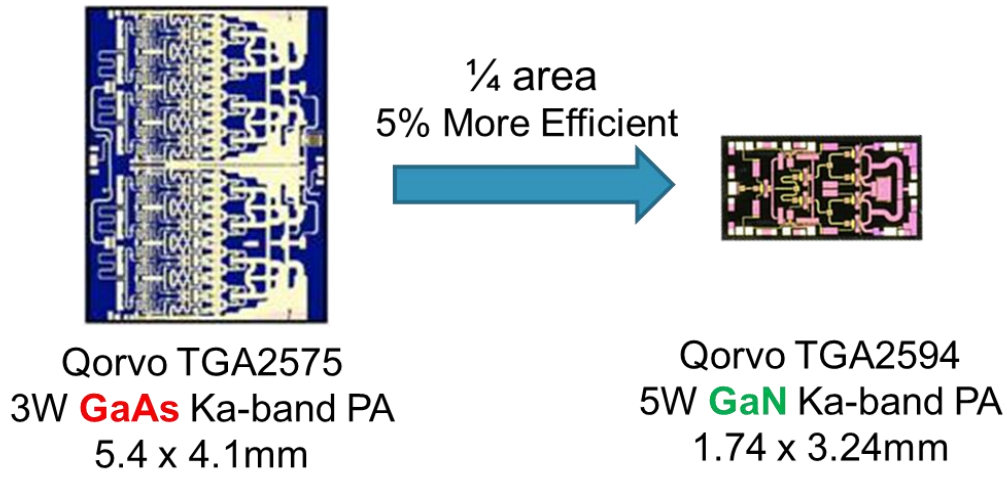


Figure 1.3 The MMIC products from Qorvo for Ka band application using GaAs (left) and GaN (right) technologies [23].

GaN-based RF electronics with high power and high efficiency at high frequency can be deployed in various applications including 5G communications, virtual reality/augmented reality (VR/AR) data transmission, imaging, and long-range radar detection. One of the potential exciting applications for GaN-based amplifiers at high frequency would be the satellite communication. In June 2020, SpaceX applied for the use of the E-band (60 GHz – 90 GHz) in their Gen2 constellation, which is expected to incorporate up to 30,000 satellites and cover the entire globe [24]. In this frequency range, GaN-based MMICs hold great potentials to fulfill the requirements of SpaceX satellite constellations.

1.2 N-polar GaN Epitaxial Structure and mm-wave Transistors

For the GaN RF electronics discussed above, their device structures are based on the Ga-polar GaN epitaxial structure. There are some trade-offs for the Ga-polar related devices

to deliver high output power and high efficiency at high frequencies (eg. mm-wave and higher frequency). To achieve higher frequency operation, f_T needs to be high and L_G should be decreased as in **Eq. 1.1**. Small L_G will decrease the R_{ds} and thus f_{max} in **Eq. 1.2** will be reduced with small L_G while other parameters kept the same. This prevents the simultaneous achievement of high f_T and high f_{max} due to the lack of good aspect ratio (L_G/h). Therefore, both L_G and h need to be reduced at the same time so that f_T can be improved and f_{max} will not be degraded. However, small h in Ga-polar will introduce less 2DEG in the channel, which may lower the current density and diminish the power performance. Therefore, the scaling of h and L_G in Ga-polar structure causes a tradeoff and is hard to decrease simultaneously while maintaining other parameters necessary for efficient power amplification especially for dimensions required for mm-wave power amplification.

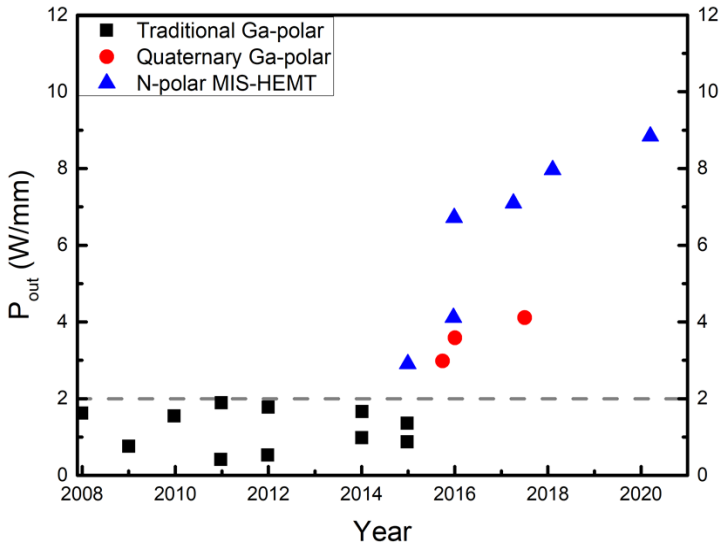


Figure 1.4 The output power density for GaN technology at mm-wave frequencies [13, 25].

As shown in the **Fig. 1.4**, the traditional Ga-polar devices performance have saturated for the past decade at around 2 W/mm of efficient output power density at mm-wave frequencies [25]. The trade-off existing in Ga-polar GaN-HEMTs could be alleviated by the

design of N-polar GaN HEMTs and the output power density can be increased by a great amount as will be described as following.

N-polar GaN has a reverse polarization field as the Ga-polar GaN. The charge inducing layer is the bottom AlGaN layer and doping as shown in **Fig. 1.5**. This solves the fundamental tradeoff between L_G and h in the Ga-polar case. To be specific, h can be reduced in the N-polar case along with the L_G while the charge density of the 2DEG in the channel remains high.

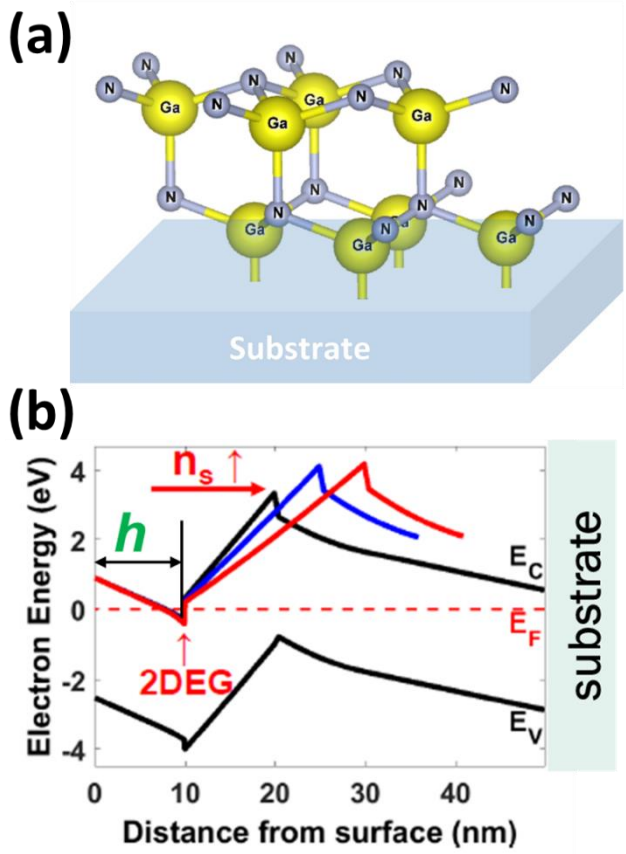


Figure 1.5 (a) N-polar GaN on substrate and (b) band diagram for a typical N-polar GaN epitaxial structure.

Even with the enhanced scaling afforded by N-polar GaN, compared with the Ga-polar GaN HEMTs, the design of N-polar GaN HEMT needs a comprehensive set of optimizations of material growth and device fabrication to be able to fully harness its potential.

A breakthrough of N-polar GaN deep recess HEMT done by B. Romanczyk et al. demonstrated superior Pout of 8.84 W/mm and associated PAE of 27 % at 94 GHz by load-pull measurements [26, 27]. The output power density of 8.84 W/mm is around 400% improvement than other Ga-polar HEMT devices and has remained the record output power density at 94GHz as shown in **Fig. 1.4**. The technical aspects on the deep recess N-polar GaN MIS-HEMT will be discussed here to elaborate the state of arts in detail. The understanding on that device and further possible improvements will be explored and are the focus of this thesis. The device has sophisticated design of epitaxial structure (**Fig. 1.6**) and fabricated device structure (**Fig. 1.7**) as described below.

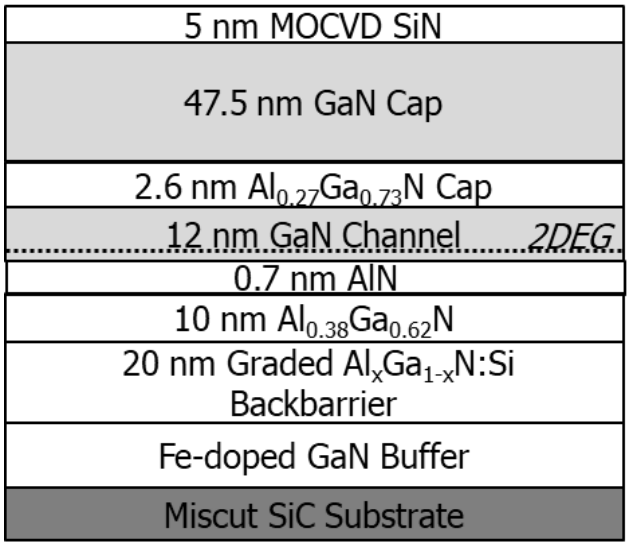


Figure 1.6 The epitaxial structure of N-polar GaN used in ref [26].

The epitaxial structure optimization includes miscut SiC substrate, back barrier, channel thickness as shown in **Fig. 1.6**. The AlGaN/GaN cap layer is discussed in the fabricated device structure.

- Miscut substrate

The miscut substrate (or vicinal substrate) was introduced in N-polar GaN growth to tackle the low surface mobility of the group-III adatoms on N-polar surface and minimize the formation of hexagons in the grown films [28, 29]. In 2007, S. Keller et al. [30] developed the use of vicinal c-plane sapphire substrates with 0.5° - 4° toward a-plane and m-plane to grow N-polar GaN and reported smooth surface morphology. Further analysis revealed 4° misorientation could reduce the number of edge dislocations significantly. The epitaxial structures of N-polar GaN thin film used in this dissertation were grown on the miscut sapphire or SiC substrate with 4° misorientation. SiC substrate is typically better than sapphire for pursuing high-power and high efficiency, due to its better thermal conductivity.

- Back barrier

During the N-polar thin film MOCVD growth, considerations in the back barrier design are important to achieve high mobility in the channel and minimize the dispersion from the back barrier. The iron doped GaN buffer first set the Fermi level in the buffer layer through the Fe dopant pinning. The negative polarized GaN/AlGaN interface may introduce deep donor traps, which could act as a source of dispersion when the Fermi level moves close to the valance band of the back barrier [31, 32]. The Si doping in the GaN and AlGaN graded layer was used to keep the Fermi level away from the valence band at the bottom GaN/AlGaN

interface [33]. Following the Si-doped layers, 10nm UID AlGaN and 0.7nm AlN were used to suppress the ionized dopant and alloy scattering effect on the 2DEG in the channel.

- Channel thickness

The thickness of the channel layer needs to be shrunk down for a better aspect ratio and high frequency operations. As the channel thickness decreases, the mobility of the 2DEG in the GaN channel also decreases due to the centroid of the 2DEG movement towards to the back barrier. The mobility would decrease rapidly when the channel thickness is less than 10 nm [13, 34]. Besides, enhanced surface depletion reduces the 2DEG sheet charge density as channel thickness is narrowed down. Thus, the channel thickness was selected to be around 12nm.

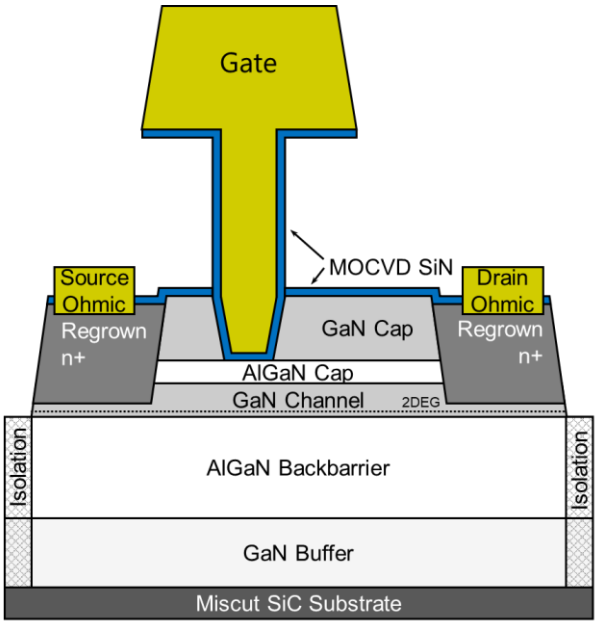


Figure 1.7 The device structure of fabricated N-polar GaN deep recess MIS-HEMT [26].

The device structure optimization includes Ohmic contact, dispersion control using the GaN cap layer and the self-aligned deep recess gate. The large-signal performance is characterized using a W-band load-pull system.

- Regrown n^+ Ohmic contact

The N-polar orientation also benefits the Ohmic contact to the 2DEG [31]. Regrown n^+ GaN contact is typically used in mm-wave GaN HEMTs for both Ga-polar and N-polar to minimize the contact resistance. In Ga-polar case, the regrown n^+ will typically contact the edge of the 2DEG in the channel because the charge induce layer AlGaN was etched away and 2DEG does not exist below the regrown n^+. However, in N-polar case, the 2DEG will still exist in the GaN before the n+ regrown and a planar contact is formed between the 2DEG and the regrown n^+. The planar contact in N-polar case over the edge contact in Ga-polar case usually reduces the parasitic source and drain contact resistances. The N-polar GaN deep recess HEMTs use MBE to regrow n+ GaN contacts.

- Dispersion control using GaN cap layer

Rather than conventional passivation using SiN or other dielectrics, the dispersion control in the deep recess N-polar GaN HEMT is from the 47.4nm thick GaN cap above the AlGaN cap layer. The innovative use of GaN cap on top of AlGaN simultaneously allows enhanced conductivity in the access region and excellent DC-RF dispersion control [26, 35]. For the enhanced conductivity, the GaN cap reduces the electric field in the channel and increases both the sheet charge density and the mobility. For the DC-RF dispersion control, the 47.5 nm

GaN cap layer separates the GaN surface from the 2DEG channel well and needs higher threshold voltage to deplete the charge in the channel compared to SiN passivated devices.

- Self-aligned deep recess gate

There are two ways developed to realize the deep recess gate structure in N-polar GaN HEMTs, self-aligned by B. Romanczyk [26] and re-aligned by S. Wienecke [35]. Due to the challenges of alignment tolerance and process variation during the device fabrications, self-alignment fabrication procedure tends to be more desired and reliable. Even though there are more flexibilities in device design in a re-align process, the large-signal results from re-aligned deep recess N-polar GaN HEMTs seems not as good as the reported self-aligned devices.

- W-band load-pull characterization

Load pull measurement is a valuable method to characterize new and developing RF power electronics with the flexibility to tune the load impedance. Large-signal performance at 94 GHz for N-polar GaN deep recess HEMT was measured by the W-band load-pull system constructed by M. Guidry et al. [36]. The W-band load-pull system is a passive system with source and load tuners. Through the detailed analysis and design of output matching range, drive power and the device under test (DUT) W_G, the system is suitable for characterizing high-power performance of N-polar GaN HEMT at 94 GHz.

1.3 Gate Structures in N-polar GaN Devices

Gate structure is one of the most important factors affecting the performance of a field effect transistor as it controls the current in the channel. With the optimization on epitaxial structure, ohmic contact and dispersion control in N-polar GaN HEMTs, further improvement

on the gate structure is becoming critical. The consideration for designing a gate structure includes the gate length (L_G), gate to channel distance (h), gate stability and robustness (trapping and breakdown voltage), gate leakage (I_G), gate resistance (R_G) etc. On N-polar GaN, researchers have used different gate structures to pursue performance for different applications. For power electronic applications, O. Koksaldi et al. [37] demonstrated a field plated gate using 10 nm SiN as gate dielectric and achieved breakdown voltage over 2000V and low dynamic on-resistance. X. Zheng also reported the high combination of f_{max}*$V_{DS,Q}$ in a N-polar GaN HEMT with L_G of ~100nm [38]. For mm-wave applications, the N-polar GaN deep recess MIS-HEMT by B. Romanczyk *et al.* demonstrated record-high output power density and good efficiency at 94 GHz. The deep recess HEMTs has been using 5nm MOCVD SiN as the gate dielectric with gate length more than 60 nm [26, 27].

In spite of the demonstrated great performance of the prior 94 GHz N-polar GaN devices, there is still room to improve the gate related aspects. The MOCVD SiN or other gate dielectric on N-polar GaN has not been explored systematically before and the knowledge on that is needed to understand the quality of gate dielectric and strengthen the gate structure. The trap related analysis will be needed to characterize the gate stability behavior for MIS-structures. From the perspective of gain, further scaling the gate length in N-polar GaN HEMT is desired. Schottky gating structure on N-polar GaN can reduce the gate to channel distance and enable further scaling without causing severe short channel effects. Developing good Schottky metal on N-polar is therefore another possible way to pursue high performance in HEMT devices. While scaling down the gate length laterally and gate to channel distance vertically can be used to improve the gain, the gate resistance challenges for small L_G will need careful considerations. Scaling down the gate length in a deep recess structure using

previous thermal evaporated Cr gate will be a big challenge due to the incomplete filling of the T-gate stem and resulting high gate resistance. New gate metal deposition would be necessary to reduce the gate resistance for highly-scaled devices.

1.4 Overview of This Dissertation

This dissertation evaluates different gate structures on N-polar GaN including MIS- and Schottky structures. Part of the evaluation is conducted through the MIS-capacitor or Schottky diode structures with attempts to understand the physics and interface properties. Another part of the evaluation is in the form of N-polar GaN deep recess HEMTs to pursue the high performance at 94 GHz.

In Chapter 2 and Chapter 3, MIS structures with MOCVD grown SiN and AlSiO on N-polar GaN are studied in the form of capacitors. A series of metal-insulator-semiconductor capacitors consisting of dielectric with different thicknesses on N-polar GaN have been fabricated to investigate their interface states. An improved model is presented which can extract the bulk hole traps in the dielectric under some simplifying assumptions for the first time. By combining the effects from interface states and bulk hole traps, the interface state density D_{it} can be extracted more accurately by extrapolating the trap density to a zero-thickness dielectric. The average D_{it} value and the bulk trap parameters can be quantified. The results, model and analysis presented here provide new insights into studying D_{it} of various dielectrics on GaN and other wide-bandgap semiconductors.

In chapter 4, the Schottky barrier diode of ruthenium (Ru) deposited by atomic layer deposition on N-polar GaN is investigated. The Schottky diodes showed near-ideal thermionic current behavior under forward bias and reverse bias at various temperatures. The barrier height values extracted from both regions agreed well at each temperature and the barrier was extracted to be 0.77 eV at room temperature. The difference between the predicted barrier height (0.6 eV) and the experimental barrier heights (0.77eV) indicated the Schottky barrier height was enhanced by 0.17 eV. The combination of the 0.77 eV barrier and thermionic current characteristic resulted in < 2 μA/cm^2 reverse current at -5 V, which is a record-low value for N-polar GaN Schottky diodes.

In Chapter 5 and Chapter 6, ALD Ru gate has been adopted into the N-polar GaN deep recess MIS- and Schottky HEMTs. The ALD Ru effectively fills the narrow T-gate stems aiding realization of shorter gate lengths with lower gate resistance than in prior work. For the ALD Ru MIS-HEMTs, the gate length was scaled down to 48 nm resulting in the demonstration of a record-high 8.1 dB linear transducer gain measured at 94 GHz by load-pull. This increased gain has enabled a record 33.8% power-added efficiency (PAE) with an associated output power density (P_O) of 6.2 W/mm. The Ru/N-polar GaN Schottky-HEMT operating at W-band has also been investigated and its good large signal performance is reported. Thank to the direct Schottky contact between Ru and N-polar GaN channel, the fabricated Schottky HEMT with L_G of 60 nm has a high peak extrinsic transconductance of 798 mS/mm with a gate leakage in pinch-off below 3×10^{-4} A/mm at V_{DS} = 5V. The Schottky-HEMT shows high power-added efficiency (PAE) of 27.1% and output power density (P_O) of

4.87 W/mm at 94 GHz and $V_{DS,Q}$ = 16V. The peak PAE is 31.8% with associated P_O of 3.31 W/mm at $V_{DS,Q}$ = 12V.

References

1. F. Ponce, D. Bour, "Nitride-based semiconductors for blue and green light-emitting devices," *Nature* **386,** 351–359, 1997.
2. S. Pimputkar, J. Speck, S. P. DenBaars, and S. Nakamura. "Prospects for LED lighting," *Nature Photon* **3,** 180–182, 2009.
3. J. Heber, "Nobel Prize 2014: Akasaki, Amano & Nakamura," *Nature Phys* **10,** 791, 2014.
4. D. Zhu, D. J. Wallis, C. J. Humphreys, "Prospects of III-nitride optoelectronics grown on Si," *Rep. Prog. Phys.*, **76** 106501, 2013.
5. G. Li, W. Wang, W. Yang, Y. Lin, H. Wang, Z. Lin, and S. Zhou, "GaN-based light-emitting diodes on various substrates: a critical review," *Rep. Prog. Phys.,* 79, 056501, 2016.
6. D. S. Arteev, A. V. Sakharov, E. E. Zavarin, W. V. Lundin, A. N. Smirnov, V. Y. Davydov, M. A. Yagovkina, S. O. Usov, A. F. Tsatsulnikov, "Investigation of Statistical Broadening in InGaN Alloys," *J. Phys.: Conf. Ser.* **1135,** 012050, 2018.
7. Global Micro-LED Market with Covid-19 Impact Analysis by Application (Display (Smartwatch, NTE Device, Smartphone and Tablet, Television, Digital Signage), Lighting (General, Automotive)), Display Panel Size, Vertical and Region - Forecast to 2027. Available online: https://www.researchandmarkets.com/reports/4535720/micro-led-market-byapplication-display#pos-0 (accessed on Jan 28, 2022).
8. U. Mishra, L. Shen, T. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proceedings of the IEEE*, vol. 96, pp. 287-305, 2008.
9. K. J. Chen, O. Haberlen, A. Lidow, C. Tsai, T. Ueda, Y. Uemoto, Y. Wu, "GaN-on-Si Power Technology: Devices and Applications," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 779-795, March 2017.

10. R. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, W. L. Pribble, "A review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, June 2012.
11. H. Xue, Q. He, G. Jian, S. Long, T. Pang, and M. Liu, "An Overview of the Ultrawide Bandgap Ga2O3 Semiconductor-Based Schottky Barrier Diode for Power Electronics Application," *Nanoscale Research Letters*,13:290, 2018.
12. E. A. Jones, F. F. Wang and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707-719, Sept. 2016.
13. B. Romanczyk, Insight into the Design, Fabrication, and mm-Wave Power Performance of N-Polar GaN Deep Recess HEMTs, *Ph.D. dissertation*, University of California, Santa Barbara, 2018.
14. M. A. Khan, J. N. Kuznia, D. T. Olson, W. J. Schaff, J. W. Burm, and M. S. Shur, "Microwave performance of a 0.25 μm gate AlGaN/GaN heterostructure field effect transistor", *Appl. Phys. Lett.*, vol. 65, pp. 1221-1123, 1994.
15. Y. F. Wu, B. P. Keller, S. Keller, D. Kapolnek, S. P. Denbaars, and U. K. Mishra, "Measured microwave power performance of AlGaN/GaN MODFET," *IEEE Electron Device Lett.*, vol. 17, pp. 455-457, 1996.
16. Y. F. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40 W/mm double field plated GaN HEMTs", *IEEE DRC Tech. Dig.*, p. 151, June 2006.
17. T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "High-power AlGaN/GaN HEMTs for Ka-Band applications", *IEEE Elect. Dev. Letts.*, vol. 26, pp. 781-783, 2005.
18. Y. F. Wu, M. Moore, A. Abrahamsen, M. J. Mitos, P. Parish, S. Heikman, A. Burk, "High voltage millimeter wave GaN HEMTs with 13.7 W/mm power density", *IEDM Tech. Dig.*, pp. 405-408, Dec. 2007.

19. J. S. Moon, D. Wong, M. Hu, P. Hashimoto, M. Antcliffe, C. McGuire, M. Micovic, P. Willadson, “55% PAE and high power Ka band GaN HEMTs with linearized transconductance via n+ GaN source contact ledge”, *Electron Device Letters*, vol. 29, pp. 834-837, 2008.
20. A. Margomenos, A. Kurdoghlian, M. Micovic, K. Shinohara, D. F. Brown, A. L. Corrion, H. P. Moyer, S. Burnham, D. C. Regan, R. M. Grabar, C. McGuire, M. D. Wetzel, R. Bowen, P. S. Chen, H. Y. Tai, A. Schmitz, H. Fung, A. Fung, and D. H. Chow, “GaN technology for E, W and G-band applications,” *IEEE Compound Semicond. Integrated Circuit Symp. (CSICS)*, La Jolla, CA, USA, pp. 1-4, 2014.
21. D. F. Brown, A. Williams, K. Shinohara, A. Kurdoghlian, I. Milosavljevic, P. Hashimoto, R. Grabar, S. Burnham, C. Butler, P. Willadsen, and M. Micovic, “W-band power performance of AlGaN/GaN DHFETs with regrown n+ GaN ohmic contacts by MBE,” *IEEE Int. Electron Devices Meet. (IEDM)*, Washington, DC, USA, pp. 19.3.1-19.3.4, 2011.
22. Y. Niida, Y. Kamada, T. Ohki, S. Ozaki, K. Makiyama, Y. Minoura, N. Okamoto, M. Sato, K. Joshin, and K. Watanabe, “3.6 W/mm high power density W-band InAlGaN/GaN HEMT MMIC power amplifier,” *2016 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*, pp. 24- 26, 2016.
23. https://www.qorvo.com/products/p/TGA2575; https://www.qorvo.com/products/p/TGA2594;
24. "Starlink Gen2 FCC Application Narrative Attachment". FCC.report. June 2020. Retrieved 2020-06-18. https://fcc.report/IBFS/SAT-LOA-20200526-00055/2378669.
25. https://dev.ims-ieee.org/ims_files/get?filepath=ims-slides2021/We02F_3.pdf, 2021.
26. B. Romanczyk, S. Wienecke, M. Guidry, H. Li, E. Ahmadi, X. Zheng, S. Keller, U. K. Mishra, “Demonstration of constant 8 W/mm power density at 10, 30, and 94 GHz in state-of-the-art millimeter-wave N-polar GaN MISHEMTs,” *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 45–50, Jan. 2018.

27. B. Romanczyk, X. Zheng, M. Guidry, H. Li, N. Hatui, C. Wurm, A. Krishna, E. Ahmadi, S. Keller, U. K. Mishra, “W-band power performance of SiN-passivated N-polar GaN deep recess HEMTs,” *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 349-352, Mar. 2020.
28. M. Sumiya, K. Yoshimura, T. Ito, K. Ohtsuka, S. Fuke, K. Mizuno, M. Yoshimoto, H. Koinuma, A. Ohtomo, and M. Kawasaki, “Growth mode and surface morphology of a GaN film deposited along the N-face polar direction on c-plane sapphire substrate,” *J. Appl. Phys.* 88, 1158, 2000.
29. S. Keller, H. Li, M. Laurent, Y. Hu, N. Pfaff, J. Lu, D. F. Brown, N. A. Fichtenbaum, J. S. Speck, S. P. DenBaars and U. K. Mishra, “Recent progress in metal-organic chemical vapor deposition of 000-1 N-polar group-III nitrides,” *Semicond. Sci. Technol*. 29, 113001, 2014.
30. S. Keller, N. A. Fichtenbaum, F. Wu, D. Brown, A. Rosales, S. P. DenBaars, J. S. Speck, and U. K. Mishra, “Influence of the substrate misorientation on the properties of N-polar GaN films grown by metal organic chemical vapor deposition,” *J. Appl. Phys*. 102, 083546, 2007.
31. M. H. Wong, S. Keller, Nidhi, S. Dasgupta, D. J. Denninghoff, S. Kolluri, D. F. Brown, J. Lu, N. A. Fichtenbaum, E. Ahmadi, U. Singisetti, A. Chini, S. Rajan, S. P. DenBaars, J. S. Speck, and U. K. Mishra, “N-polar GaN epitaxy and high electron mobility transistors,” *Semicond. Sci. Techol.*, vol. 28, no. 7, p. 074009, 2013.
32. C. A. Schaake, D. F. Brown, B. L. Swenson, S. Keller, J. S. Speck, and U. K. Mishra, “A donor-like trap at the InGaN/GaN interface with net negative polarization and its possible consequence on internal quantum efficiency,” *Semicond. Sci. Techol.*, vol. 28, no. 10, p. 105021, 2013.
33. S. Rajan, A. Chini, M. H. Wong, J. S. Speck, and U. K. Mishra, "N-polar GaN/AlGaN/GaN high electron mobility transistors," *J. Appl. Phys.*, vol. 102, no. 4, 2007.
34. Haoran Li, “New aspect in MOCVD of metal- and N-polar (Al,Ga)N and its device applications,” *Ph.D. dissertation*, University of California, Santa Barbara, 2018.

35. S. Wienecke, B. Romanczyk, M. Guidry, H. Li, E. Ahmadi, K. Hestroffer, X. Zheng, S. Keller, and U. K. Mishra, "N-polar GaN cap MISHEMT with record power density exceeding 6.5 W/mm at 94 GHz," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 359-362, Mar. 2017.
36. M. Guidry et al., "W-band passive load pull system for on-wafer characterization of high power density N-polar GaN devices based on output match and drive power requirements vs. gate width," *Proc. 87th ARFTG Microw. Meas. Conf.*, San Francisco, CA, USA, pp. 1–4, May 2016.
37. O. S. Koksaldi, J. Haller, H. Li, B. Romanczyk, M. Guidry, S. Wienecke, S. Keller, and U. K. Mishra, "N-Polar GaN HEMTs Exhibiting Record Breakdown Voltage Over 2000 V and Low Dynamic On-Resistance," *IEEE Electron Device Letters*, vol. 39, pp. 1014-1017, 2018.
38. X. Zheng, H. Li, M. Guidry, B. Romanczyk, E. Ahmadi, K. Hestroffer, S. Wienecke, S. Keller, and U. K. Mishra, "Analysis of MOCVD SiNX passivated N-polar GaN MIS-HEMTs on sapphire with high $f_{max} \bullet V_{DS,Q}$," *IEEE Electron Device Letters*, vol. 39, p. 409-412, 2018.

Chapter 2. An Improved Methodology for Extracting D_{it} at Si_3N_4/GaN

In this chapter, a series of metal-insulator-semiconductor capacitors consisting of Si_3N_4 dielectric with different thicknesses on N-polar GaN have been fabricated to investigate their interface states. The measurement value extracted from ultraviolet assisted capacitance-voltage (UV-assisted CV) methods can be explained by the existence of spatially uniform hole traps in Si_3N_4. An improved model combining the effects from interface states and hole traps in Si_3N_4 is proposed to extract the interface state density (D_{it}) accurately. Based on the model, the D_{it} can be obtained by extrapolating the trap density to a zero-thickness dielectric. The extracted average D_{it} value of Si_3N_4/GaN interface is ~3.8×10^{11} cm^{-2} eV^{-1} and the hole trap concentration in Si_3N_4 is ~3.1×10^{18} cm^{-3}. The results, model and analysis presented here provide new insights into studying D_{it} of various dielectrics on GaN and other wide-bandgap semiconductors.

2.1 Dielectrics on Semiconductor

Abrupt semiconductor surfaces contain a large amount of unterminated/dangling bonds, which are chemically reactive. Compared to the band structure in the bulk semiconductor, the band structure at the surface is modified and the states can exist in the otherwise forbidden energy bandgap. The states are localized at the surface and called surface states. Surface states include intrinsic states and extrinsic states. “Intrinsic” means these states would occur even when the surface is an ideal crystal structure. These intrinsic states were first presented by Tamm [1] and Shockley [2] and correspond to the wavefunction solutions to the Schrodinger equation at the boundary of a periodic potential, which decays exponentially into the vacuum. The wavefunctions of surface states were drawn from the conduction band and valence band of the bulk crystal. In the energy bandgap, the states drawn from the conduction band tends to

accept electrons hence are acceptor-like while the states drawn from the valence band tends to donate electrons hence are donor-like. “Extrinsic” surface states are referred to the surface states caused by non-idealities at the surface, like reconstruction, native defects, impurities, dislocations or other structural defects [3-5]. These non-idealities depend on the environment and conditions during material growth and device processing. Extrinsic surface states could also introduce donor-like or acceptor-like states. These donor-like or acceptor-like states from intrinsic or extrinsic surface states will be filled or emptied, which cause surface charge transfer and help determine the Fermi level in the material.

When dielectrics are grown/deposited on the surface of semiconductors, there will be multiple types of interface states formed at the dielectric/semiconductor interface. Compared to the surface states of the semiconductor including intrinsic surface states and extrinsic surface states, the interface formation process is further complicated and may generate additional states. Over the past century, researchers have developed several models [6-12] to describe semiconductor interface states, formed with either metals or dielectrics. However, due to the complexity and subtlety, the endeavor to create a unified predictive theory on the interface states has been frustrating [13]. Through the insights from surface states of semiconductor, some conceptual understanding on the interface states can be obtained. Assuming the dielectric is ideal and the same methodology as the surface state of semiconductor is still applied, there could be also some intrinsic interface states existing at the dielectric/semiconductor interface. At the same time, interface related non-idealities would contribute to extrinsic interface states, including un-compensated dangling bonds, impurities, irregular bonding, grain boundary and so on. It is worth noting that stacking two materials together may introduce some two-dimensional defects when the contacting planes vary. Alike

the surface states, the interface states can be heavily dependent on the processing treatment, such as semiconductor surface cleaning/treatment, dielectric deposition conditions, post deposition annealing, etc.

Furthermore, different from the relatively well-grown bulk semiconductors, the growth/deposition of dielectrics is usually less ideal, and more defects can be formed in the bulk dielectric. The growth of dielectric starts on the surface of semiconductor, which may bring defects and stress on the dielectric thin films in the beginning. The structure of the following grown bulk dielectric would be affected and deviate from ideal crystal structure, if not amorphous. The origin of bulk dielectric defects could be native defects, impurities, grain boundary or other structural defects. In high-k $HfO_2/SiO_2/Si$ devices, bulk traps are usually present in the HfO_2. In 2003, Degreaeve et al. reported the bulk HfO_2 trap density was around 10^{16}-10^{17} cm^{-3} using charge pumping technique [14]. Some experimental and calculation studies attributed the bulk traps in HfO_2 to oxygen vacancy and oxygen interstitial [15-19]. Bulk traps could also be generated during device use as a result of positive bias temperature instability or time dependent dielectric breakdown degradation mechanisms [20-21].

There are also some possible fixed/mobile charges formed at the interface and in the bulk dielectrics. These charges remain the same charge and would not donate or accept extra electrons. Their effects on the devices during dynamic operation are limited and would not be included here.

2.2 Traps in Metal/Insulator/Semiconductor Structure

Under the context of the energy band diagram, the traps in Metal/Insulator/Semiconductor (MIS) structure can be categorized based on their spatial distribution and energetic distribution

as shown in **Fig 2.1** assuming an accumulation bias condition. In this chapter, both near-interfacial and interface traps are described as "interface traps/states" for the sake of model simplification and physical understanding. Near-interface and interface traps are hard to distinguish by typical electrical measurements, while in the 1990s Fleetwood et al. developed a revised nomenclature as "border traps" and "interface traps" for defects to separate them in metal/oxide/semiconductor (MOS) devices [22].

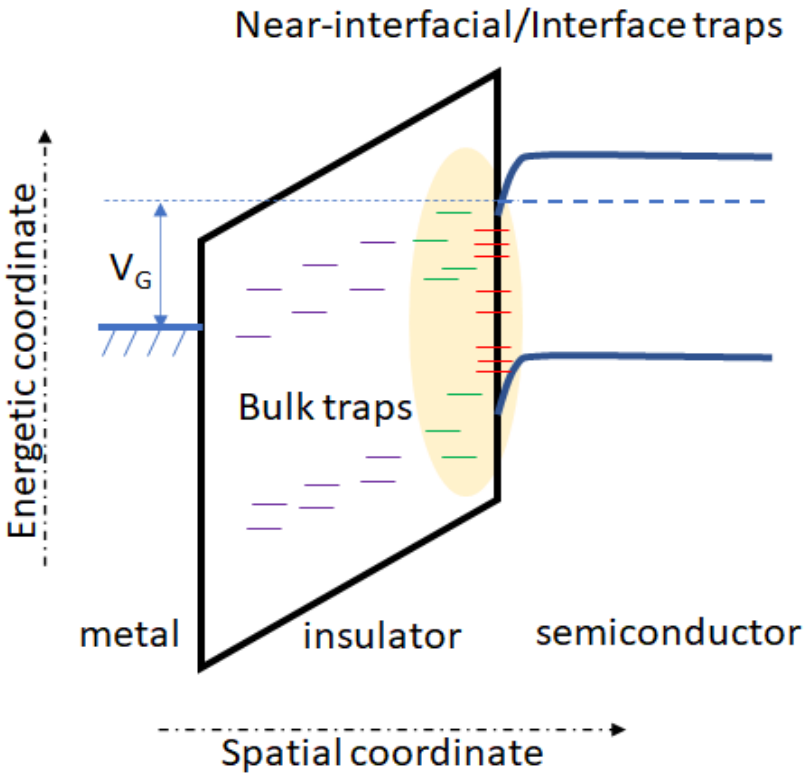


Figure 2.1 Schematic of traps in a Metal/Insulator/Semiconductor structure based on their spatial distribution and energetic distribution assuming accumulation bias conditions.

Depending on their spatial and energetic locations, traps have different time constants and will respond to different frequencies of applied signals. The time constant for state with energy E is exponentially dependent on the energy difference E_C-E or E-E_V. The state in the mid-gap usually has large time constant since it is energetically separated from both the conduction

band and valence band. The bulk trap with some distance to the semiconductor also has a time constant interacting with the charge in the channel, which is exponential dependence on the distance assuming an ideal barrier in the absence of hopping conduction.

The electrically active interface and bulk states will act as local traps, which would capture or emit electrons as the Fermi level sweeps across the traps. The interaction between traps and carriers affects the operation of transistors adversely. 1) One of the effects is lowering the carrier mobility due to the extra electrical Coulomb scattering from the charged traps. 2) In addition, these charged/discharged traps will contribute to a corresponding capacitance, shift the threshold voltage and affect the carrier charge density in the channel. 3) Besides, the trap states can serve as the steppingstones to cause high gate leakages through tunneling or hopping conduction. In some extreme stress situations, these structural and electrical weak points around the defects/traps may lead to early failures during device operations.

2.3 Interface States of Dielectric/WBG Semiconductor

Wide-bandgap (WBG) materials with bandgap in the range of 2~4 eV, such as GaN and SiC, have boosted the power performance of electronics dramatically, providing high operation voltage, low on-resistance, and high output power [23,24]. Developing high-quality gate dielectrics on WBG semiconductors is crucial to achieve low gate leakage, high operation voltage and stable electrical operations in metal-insulator-semiconductor field effect transistors (MIS-FETs) and metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) [25]. In GaN devices, the dielectric passivation layer is typically used in the access region between the gate and source/drain region to mitigate the severe DC-RF dispersion issue.

The interface state density (D_{it}) of dielectrics on WBG semiconductors is one of the key performance metrics to assess the quality of dielectrics. Due to the large bandgap of WBG semiconductors, the time needed to charge/discharge the interface states close to the mid-gap are much longer than other semiconductors with small bandgaps. In WBG semiconductor based MISFETs and MISHEMTs, high D_{it} at the interface between the gate dielectric and the channel is detrimental to device performance and can cause inefficient Fermi level response and poor gate control [26]. Moreover, when poor-quality dielectrics passivate the access regions, interface states with relatively large time constants can lead to current collapse and reduce the maximum current [27-29].

In order to improve and optimize the dielectrics on WBG semiconductors, an accurate method to evaluate D_{it} is required. Conventional Terman method, high-low frequency method, and the conductance method, well-established for the SiO_2/Si system [30], may not be an effective way to measure the whole bandgap distribution for WBG semiconductors due to the low minority carrier generation rate in WBG semiconductor systems [31]. Deep Level Transient Spectroscopy and Deep Level Optical Spectroscopy [32,33] probe a fraction of the gap depending on temperatures or the availability of incident light wavelengths [34].

2.4 UV-assisted C-V Methods and Thickness Series of MOCVD SiN

An effective and efficient approach developed for characterizing D_{it} on WBG semiconductor systems is the photo-assisted high-frequency capacitance-voltage (C-V) method [34-38]. Swenson et al proposed an ultraviolet-assisted capacitance-voltage (UV-assisted C-V) technique for measuring the average D_{it} of MOCVD grown SiN on GaN [39]. The technique utilized the UV illumination to overcome the low minority carrier generation rate in WBG semiconductor systems and utilized the benefit of SiN as a dielectric on GaN

with a negative valence band offset compared with the GaN as a pathway of draining excess holes out of the capacitor. Swenson however assumed that only the interface traps would contribute to the voltage difference between the ideal dark curve and the shifted post-UV curve. Based on the assumption, formulas to obtain D_{it} were derived and the D_{it} distribution across the bandgap of GaN measured.

Specifically, in the method developed by Swenson et al, the effect from traps in bulk dielectrics has not been discussed, which may result in an inaccurate extraction of D_{it} [30,40,41]. In this following part of the chapter, through a series of metal-insulator-semiconductor capacitors (MISCAPs) with various dielectric thicknesses, an improved physical model and analysis is proposed to extract the accurately by accounting for the effects of dielectric bulk hole traps using modified ultraviolet photo-assisted UV-assisted C-V methods. The thickness series was designed to separate the contribution of the bulk traps and interface states. The methodology is similar to the method for extracting the net fixed interface charges between dielectric and semiconductor, which is widely used in studying semiconductors. The MISCAPs consist of in-situ grown Si_3N_4 (SiN) on N-polar GaN. SiN is often used as the effective passivation dielectric for GaN HEMTs [29]. Moreover, devices based on N-polar GaN utilizing SiN gate dielectrics have demonstrated tremendous potential for high power and high frequency electronic applications [42,43]. Therefore, the accurate determination of SiN/N-polar GaN is of great interest. Some figures and materials of the following chapter was reproduced from [**Wenjian Liu**, Islam Sayed, Chirag Gupta, Haoran Li, Stacia Keller, Umesh Mishra, "An improved methodology for extracting interface state density at Si3N4/GaN." *Applied Physics Letters,* 116, 022104(2020).], with the permission of AIP Publishing.

2.5 Epitaxial Structure and Device Fabrication

The epitaxial structure of the SiN on N-polar GaN is shown in **Fig. 2.2(a).** The epitaxial layers are grown by metal organic chemical vapor deposition (MOCVD) on c-plane sapphire substrates misoriented by 4° towards a-plane [44]. The doping concentrations for the 800 nm n^+ GaN and the 600 nm n^- GaN are 2.5×10^{18} cm^{-3} and 2.5×10^{17} cm^{-3}, respectively. SiN with different thicknesses (5 nm, 10 nm, 20 nm, and 30 nm) was grown in situ at 1030 °C. The dielectric thickness was measured by X-ray reflectivity and ellipsometry. The difference between them is within the range of 5%.

The cross-section schematic of the fabricated SiN on N-polar GaN MISCAPs is shown in **Fig. 2.2(b).** In the fabrication process, the SiN was firstly etched by CF4/O2-based ICP dry etch and the n^-/n^+ GaN was etched by BCl_3/Cl_2-based RIE dry etch, which etched into the n^+ GaN layer by ~200 nm. Then the Ohmic contact to the n^+ GaN was formed when Ti/Au (25 nm/200 nm) was deposited as the gate and ohmic electrodes.

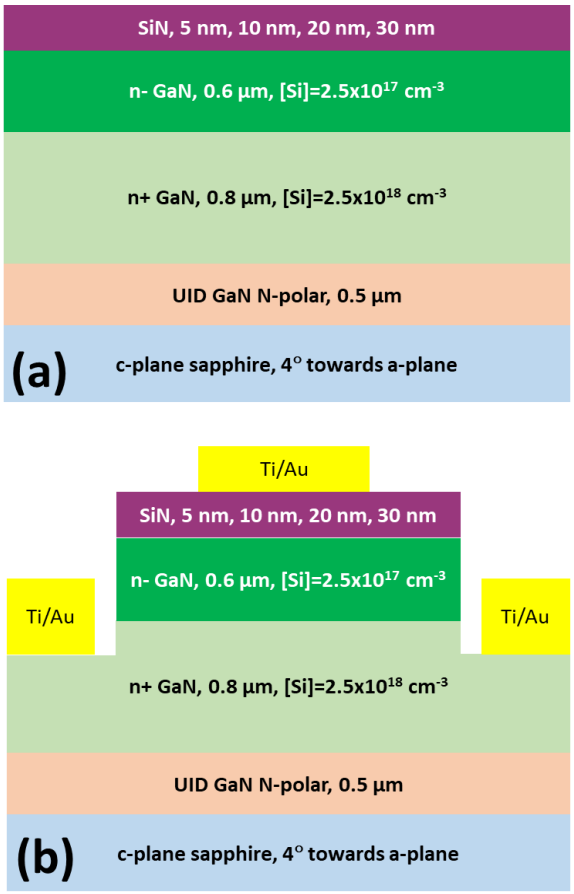


Figure 2.2 (a) The epitaxial structure grown by MOCVD; (b) The cross-section schematic of the fabricated SiN on N-polar GaN MISCAPs.

2.6 Measurements and Energy Band Diagrams

All measurements were performed using an Agilent B1500 semiconductor device analyzer equipped with medium power source/monitor units and multi-frequency capacitance measurement unit. The frequency and amplitude of AC signals used for C-V measurement were 1 MHz and 50 mV, respectively. The DC voltage was swept with a 30-mV voltage step and a 0.6 V/s sweep rate. An EXFO OmniCure1000 spot curing system with a high-pressure Hg lamp filtered between 320 nm and 500 nm was used as the UV illumination source. The spectrum of the illumination source was shown in the **Fig. 2.3** below.

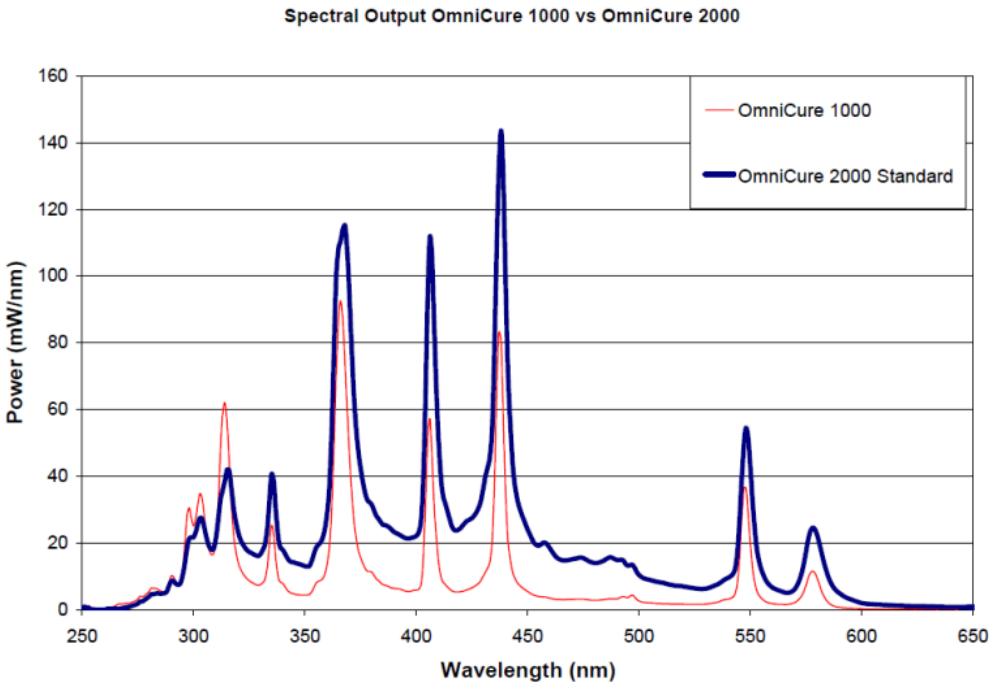


Figure 2.3 Output Spectra of Omnnicure 1000 vs. Omnicure 2000 (Courtesy of EXFO). Omnicure 1000 was used in these measurements.

There are three main sweep steps for UV-assisted C-V methods as shown in **Fig. 2.4** [34,35]. First, the voltage is swept from depletion to accumulation. At accumulation, the device is held for 10 minutes to ensure all the traps are filled with electrons, which is considered as the initial state. Second, another C-V sweep from depletion to accumulation is implemented to register the initial state as the dark curve in **Fig. 2.4 (a).** The aforementioned C-V sweeps are done under dark condition. Third, the device is held at -10 V bias and is UV-illuminated to generate electron-hole pairs for 30 seconds with an incident power intensity around 0.18 W/cm^2. The free holes generated by UV are captured by the interface traps and bulk dielectric traps, as shown in the energy band diagram **Fig. 2.4 (b)**[45]. Note that the dielectric bulk hole traps are taken into consideration in the band diagram, which is generally ignored and can cause inaccurate determination of interface state density value. The existence

of hole traps in the SiN after the UV illumination is mentioned by previous studies [46-49] but not analyzed.

In these band diagrams, assuming the hole trap concentration is low in SiN, for simplicity we take its valance band and conduction band as straight lines. The electron quasi-Fermi level (E_{Fn}) and hole quasi-Fermi level (E_{Fp}) split because of electron and hole generation from UV illumination. After the UV exposure and under depletion electric field with -10 V bias for 10 minutes or more, free holes leave the SiN and the SiN/GaN interface through the gate contact as shown in **Fig. 2.4 (c).** The holes captured by interface states and bulk hole traps can be measured by a following C-V sweep from depletion to accumulation, which is referred as the post-UV curve in **Fig. 2.4 (a).** During this sweep, the interface states will follow electron quasi-Fermi level, keep capturing electrons and become neutralized, resulting in a capacitance ledge. As illustrated in **Fig. 2.4 (d)**, while the interface states are capturing the electrons, the dielectric bulk hole traps also capture the electrons and become partially neutralized, thus contributing to the capacitance ledge as well. In **Fig. 2.4 (d)**, The hole quasi-Fermi level (E_{Fp}) varies a little as the electron Fermi level (E_{Fn}) moves across interface states due to the interface E_{Fp} pinning [35].

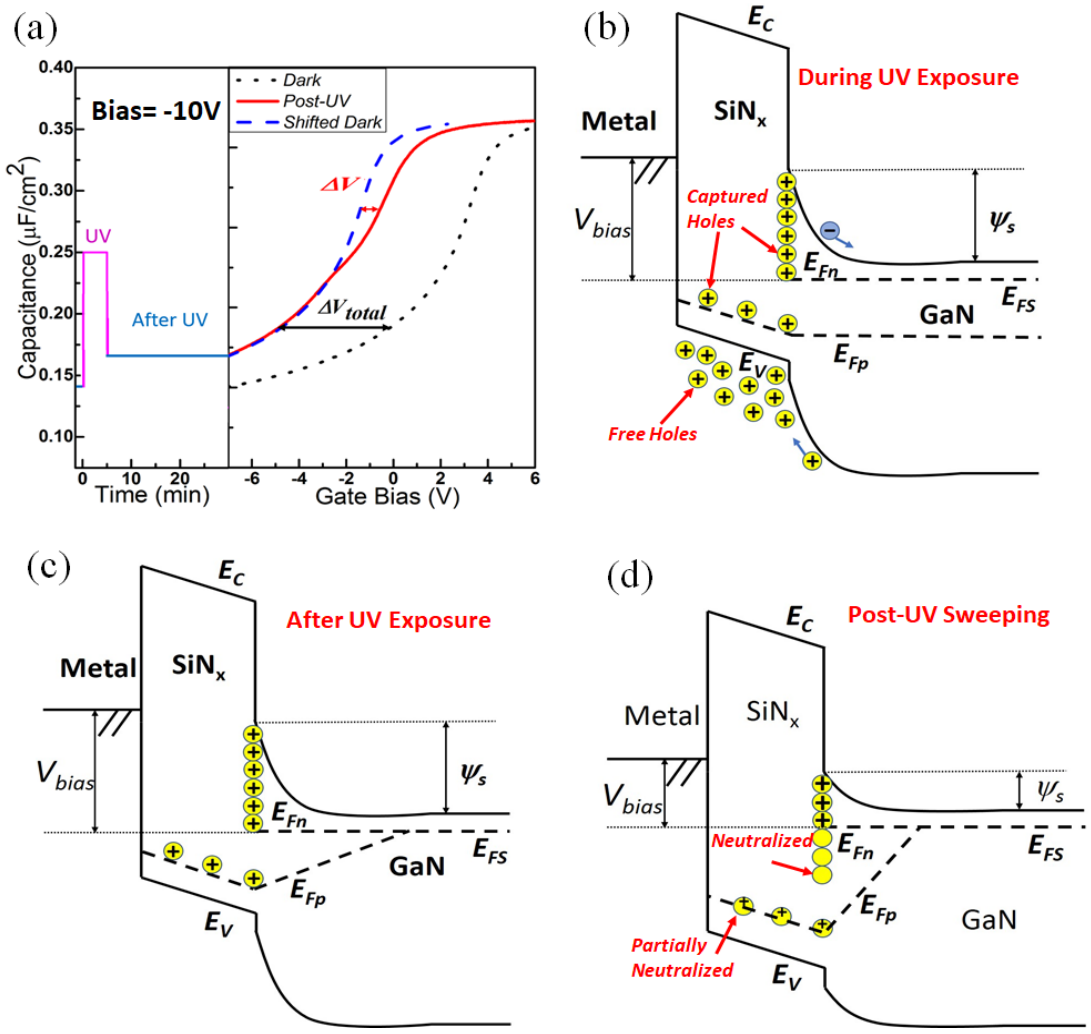


Figure 2.4 (a) UV-assisted C-V methods with three curves from sweeping, ΔV_{total} is the voltage shift as a result of the captured holes at the interface and inside the bulk of dielectric, ΔV represents the electron capture from the interface state and dielectric hole traps during post-UV sweeping; and the energy band diagrams at different stage of the UV-assisted UV methods:(b) during UV exposure, (c) after UV exposure, and (d) during post-UV sweeping.

Factors during the measurement settings

When applying the above methodology to investigate the bulk and interface traps, some factors during the measurement setting could potentially impact the final outcomes.

These factors include the UV illumination duration, *Post-UV* hold time and bias sweep rate, which will be discussed separately as follows.

- **The UV illumination duration**

In the measurements, 30 seconds was used for the UV illumination duration. To investigate the possible impact of the UV illumination duration time, additional experiments with 10-second, and 1-minute duration were done. The shift V_{total} in the C-V curves between the two CV sweep, the first measured in the dark prior to and the second post UV illumination, nearly saturates for an exposure time of 30 seconds or more.

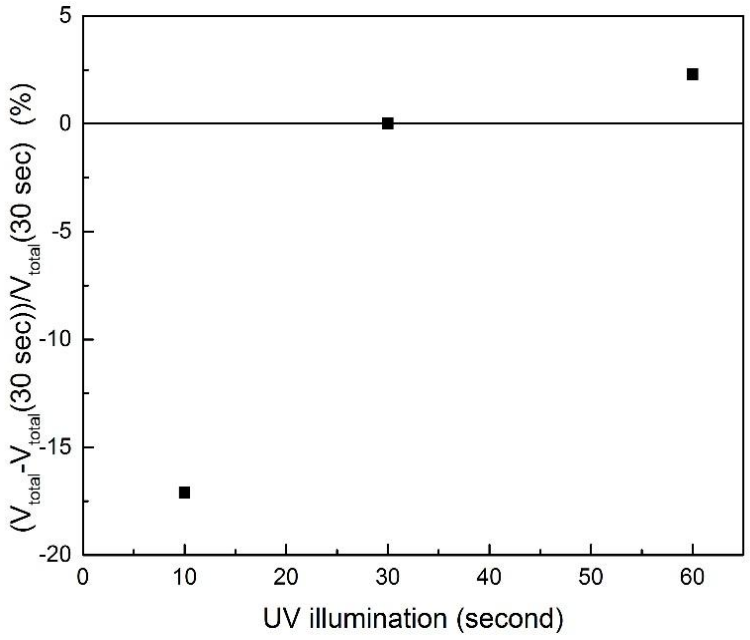


Figure 2.5 V_{total} change (V_{total}-V_{total}(30 second))/ V_{total}(30 second) vs. illumination time (second) plot with 10-second, 30-second and 60-second UV illumination.

For example, as shown in the **Fig. 2.5**, for the 10 nm SiN sample, the V_{total} change with respect to 30-second (V_{total}-V_{total}(30 second))/ V_{total}(30 second), were -17.1% for 10-second, 2.3% for 1 minute. Further increases in the UV illumination did not contribute to the difference

in V_{total} meaningfully. Therefore, the shift V_{total} can be treated to be saturated with 30 seconds UV illumination applied.

- **Post-UV holding time**

After UV exposure, the devices were held at -10V bias for 10 minutes in the manuscript. To address the recovery process, 10 minutes and 20 minutes hold time before *Post-UV* sweeping were conducted. As shown in the **Fig. 2.6.** below, the 10min_*Post-UV* (red dash line) and 20min_*Post-UV* (black dash line) curves are almost identical, which indicates the recovery process will not affect the results in the analysis when no less than 10-minute hold time is used. In order to show the two curves, the line width in below figure was selected to be small. The almost identical *Dark* and *Post-UV* lines has negligible difference in the resulted trap density values.

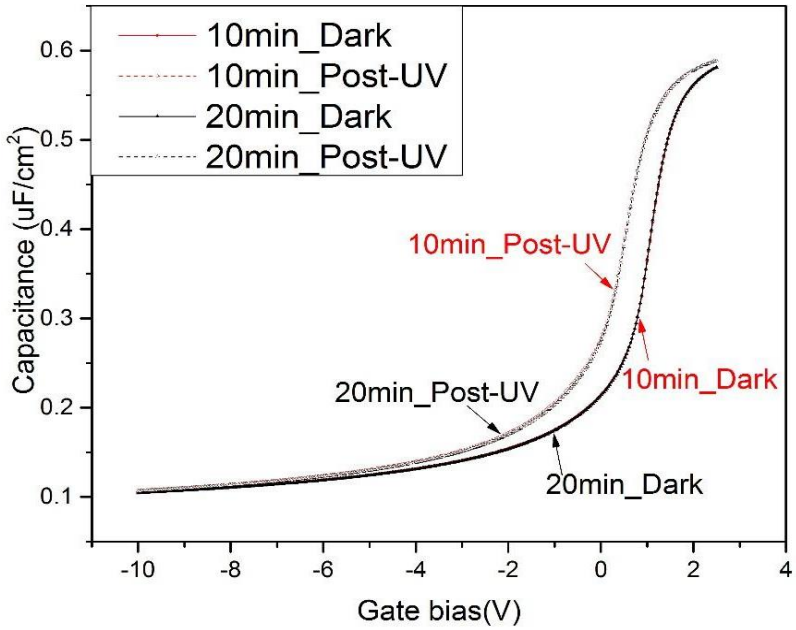


Figure 2.6 Impact of 10 minutes (red solid and dash lines) and 20 minutes (black solid and dash lines) hold time on the CV sweeps measured in the dark, prior to and post UV illumination.

- **Bias sweep rate:**

The ΔV represents the neutralization process by electrons during the C-V sweep. After UV illumination, the trapped holes with positive charges exist at the interface and inside the SiN bulk. The sweep rate has a slight effect on the measured trap density. For the 10 nm sample, the measured average trap density measured slightly depends on the sweep rate: 4.93 $\times 10^{11}$ $cm^{-2}eV^{-1}$ for 0.3 V/s, 4.89 $\times 10^{11}$ $cm^{-2}eV^{-1}$ for 0.6 V/s, 4.61$\times 10^{11}$ $cm^{-2}eV^{-1}$ for 1.2 V/s, as shown in **Fig. 2.7**. The slight difference would not have a significant effect the methodology developed above. The data in this chapter was collected with the sweep rate 0.6 V/s.

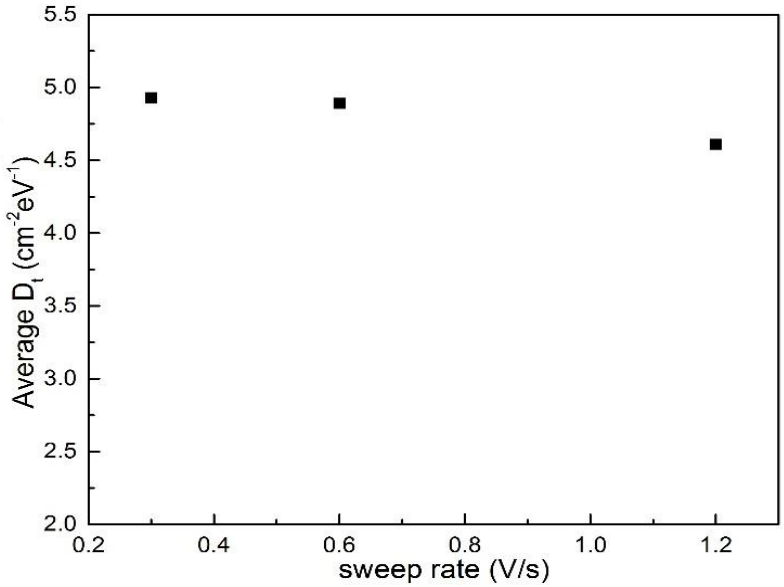


Figure 2.7 Measured average trap density vs. sweep rate. The sweep rates are 0.3 V/s, 0.6 V/s and 1.2 V/s

2.7 Bulk Trap and Interface States

2.7.1 Extracting bulk trap concentration

Based on the two measured curves, *dark curve* and *post-UV curve*, the interface state density and dielectric hole trap concentration after UV illumination can be calculated. The *dark curve* is shifted to match the capacitance value *of post-UV curve* in the deep depletion regime as shown in **Fig. 2.8 (a)**. The voltage shift, ΔV_{total} , is the consequence from the total captured holes. If the hole trap distribution in dielectric bulk is assumed to be homogeneous with concentration n_{t0}, the ΔV_{total} can be written as

$$\Delta V_{total} = q \frac{Q_0}{\varepsilon A} t + q \frac{n_{it}}{2\varepsilon} t^2 , \quad (2.1)$$

where q is the electron charge, Q_0 is the captured hole number at the interface, ε is the dielectric constant of SiN, t is the thickness of SiN, A is the device area and n_{t0} is the hole trap concentration in SiN with unit cm^{-3}. The two terms in **Eq. 2.1** reflect the contributions from the interface and the captured holes in the bulk dielectric after the UV illumination. The measured curves of MISCAPs with 10 nm and 30 nm SiN are shown in **Fig. 2.8 (a)** and **Fig. 2.8 (b)**, whose ΔV_{total} are 0.8 V and 4.8 V, respectively.

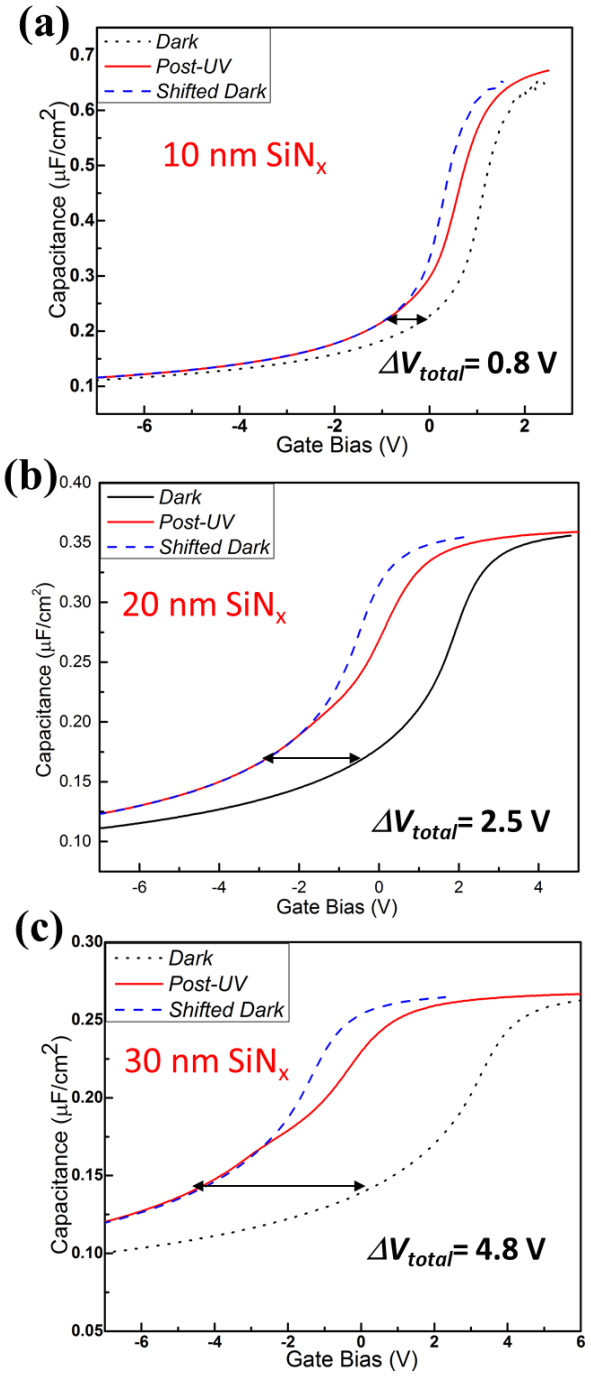


Figure 2.8 Capacitance-voltage curves of (a) 10 nm, (b) 20 nm and (c) 30 nm SiN MISCAPs

The measured ΔV_{total} values versus SiN thickness are plotted in **Fig. 2.9**. The red dot line is the fitting curve assuming there is no hole captured in SiN while the blue solid curve according to Eq. (1) assumes homogeneous distributed hole traps in the SiN. The excellent

fitting of the latter with coefficient of determination $R^2 = 0.9996$ strongly indicates the presence of spatially uniform-distributed hole traps in SiN. Furthermore, the n_{t0} value is extracted to be ~3.1×10^{18} cm^{-3}. In a metal/oxide/nitride/oxide/silicon (MONOS) nonvolatile memory structure, Aozasa et al. [] found the energy level of the hold trap was 0.8-0.9 eV above the valance band and its density was 1-4 ×10^{18} cm^{-3}. Compared with the previously mentioned bulk trap concentration of 10^{16}-10^{17} cm^{-3} in HfO_2 reported in 2005 [14], the hole trap concentration at the order of ~10^{18} cm^{-3} in the MOCVD SiN is relatively high and could be optimized further.

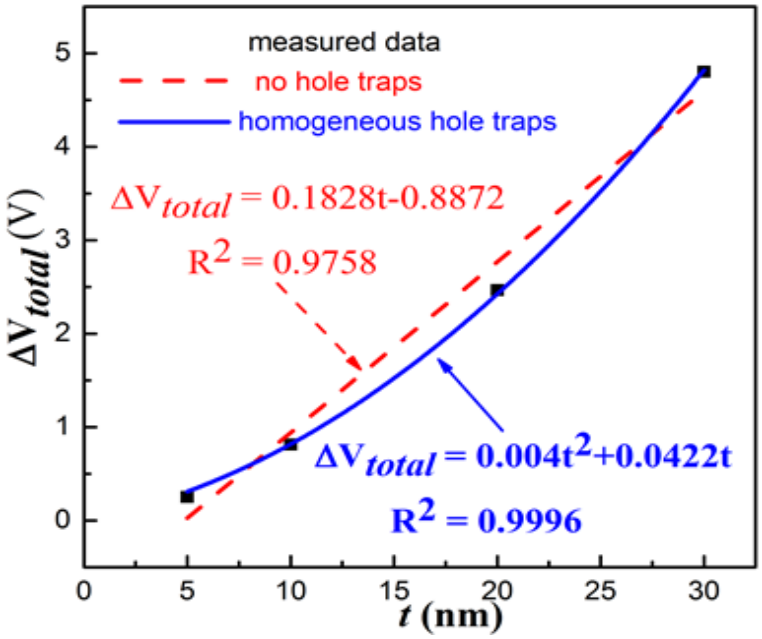


Figure 2.9 measured ΔV_{total} (black dots) versus the SiN thickness along with the linear (red dashed line) and parabolic (blue solid line) fitting.

2.7.2 Extracting interface state density and bulk trap density

In **Fig. 2.4 (a)**, ΔV can be defined as the voltage difference between the post-UV curve and shifted dark curve with the same capacitance value. The negative-charged electron capturing during the post-UV sweep results in a larger bias voltage in order to achieve the same capacitance and thus a positive ΔV. As the gate bias swings to the accumulation regime, the magnitude of semiconductor surface potential ψ_s gradually reduces and the interface states below the electron quasi-Fermi level continue to populate with electrons and become neutralized. Thus, ΔV keeps increasing as the corresponding capacitance increases. Moreover, hole traps in dielectric also capture electrons and contribute to ΔV during the change of ψ_s. Then the total contribution of ΔV coming from the interface states and the hole traps in SiN can be expressed as

$$\Delta V = q\left(\frac{N_{it}}{C_{ox}} + A\int_0^t \frac{n_{ht}}{C(x)}dx\right), \tag{2.2}$$

where N_{it} is the number of captured electrons by interface states, C_{ox} is the insulator capacitance and equal to $\varepsilon A/t$, $C(x)$ is the capacitance at the distance x from the metal and equals to $\varepsilon A/x$, n_{it} is the number of captured electrons by the dielectric hole traps per cm^3. The first term and the second term in **Eq. 2.2** are the contributions from electron capture by (i) the interface states and (ii) the bulk dielectric, respectively. The interface state density D_{it} is defined as the number change of captured electron by interface states per unit area following the change of surface potential

$$D_{it} = \frac{dN_{it}}{A \times d\psi_s}, \tag{2.3}$$

ψ_s can be calculated by the GaN depletion region width from the measured series capacitance composed by the insulator capacitance and the semiconductor capacitance. To connect **Eq.**

2.3 with the ΔV , we take the derivative of ΔV in **Eq. 2.2** with respect to ψ_s and multiply by $C_{ox}/(A \times q)$. The parameter is named as trap density D_t

$$D_t = \frac{C_{ox}}{A \times q} \times \frac{d\Delta V}{d\psi_s} = \frac{dN_{it}}{A \times d\psi_s} + t\frac{dn_{it}}{2d\psi_s} = D_{it} + t\frac{dn_{it}}{2d\psi_s} \quad , \tag{2.4}$$

where D_t combines the effects from the interface states and the dielectric hole traps. The second term in **Eq. 2.4** represents the contributions from $dn_{it}/d\psi_s$ with unit $cm^{-3}eV^{-1}$, which is related to the dielectric hole trap distribution in the energy scale. D_t has a linear relationship with dielectric thickness if $dn_{it}/d\psi_s$ remains constant.

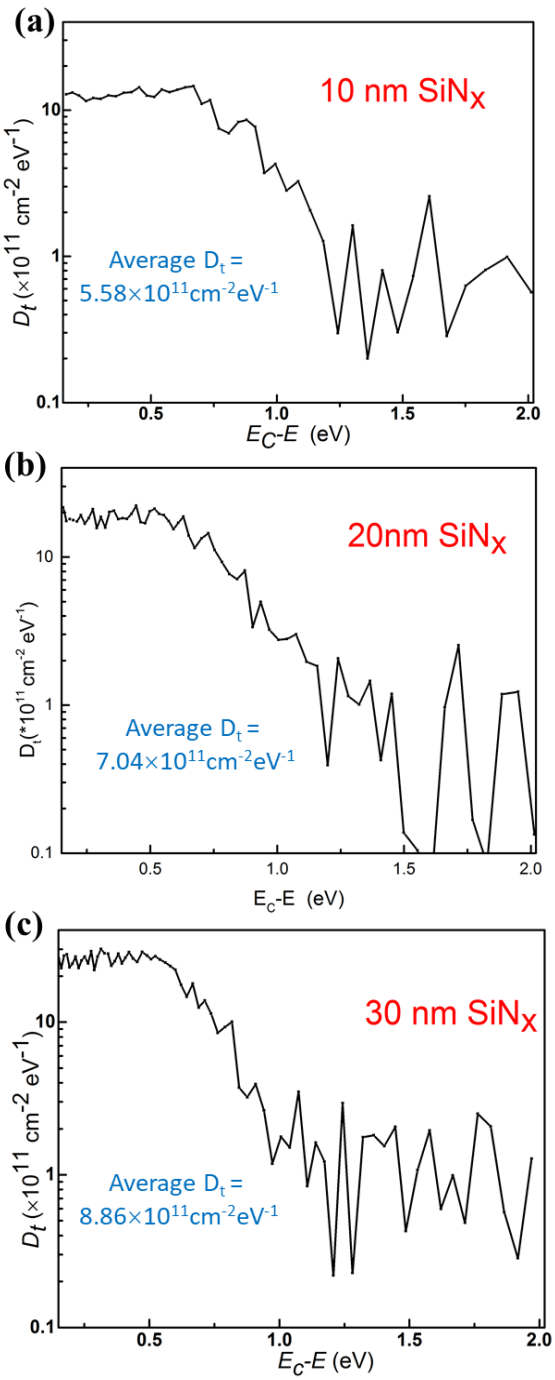


Figure 2.10 The D_t versus E_C-E curves of: (a) 10 nm, (b) 20nm and (c) 30 nm SiN MISCAPs;

The experimental D_t for 10 nm, 20 nm and 30 nm SiN are shown in **Fig. 2.10 (a)**, **Fig. 2.10 (b)** and **Fig. 2.10 (c)** along with their average D_t in the range from E_C to E_C-2 eV, where E_C is the energy of the conduction band bottom. The average D_t is typically used to

characterize the overall interface state density [36,38, 50]. The average D_t for 5 nm, 10 nm, 20 nm and 30 nm are 4.59 $\times 10^{11}$ cm^{-2} eV^{-1}, 5.58×10^{11} cm^{-2} eV^{-1}, 7.04×10^{11} cm^{-2} eV^{-1} and 8.86×10^{11} cm^{-2} eV^{-1}, respectively. The Dt values are plotted against their corresponding SiN thicknesses in **Fig. 2.11**.

As indicated in **Fig. 2.11**, the average D_t values for different thicknesses are summarized and D_{it} can be extracted according to **Eq. 2.4**. The good linear fitting indicates that the $dn_{it}/d\psi_s$ has a constant value of 3.35×10^{17} cm^{-3} eV^{-1}. A possible reason for the constant $dn_{it}/d\psi_s$ can be explained as follows. For amorphous SiN, previous studies demonstrated a "band tail" existing above the valance band, which can act as the hole traps in a continuous form [51]. During the changing of ψ_s , the hole quasi-Fermi level only varies a little bit because of the nearly pinning of E_{Fp} as in **Fig. 2.4(d)**. Therefore, as a first-order approximation, the change of hole occupancy with ψ_s can be treated as a constant.

In the past, the wide utilization of SiN as charge trapping layer in the flash nonvolatile memory inspired researchers to investigate the electron/hole traps in bulk SiN. There are multiple experimental and calculation papers [53-57] which proposed various traps models and their structural origins in amorphous SiN, while the accurate determination may depend on conditions used in experiments and calculations. One of the models [54] explored the silicon dangling bond as the charge trapping center using electron paramagnetic resonance (EPR) and suggested that the electron/hole trapping is caused by charge state change in preexisting positively/negatively charged Si sites. Kamigaki et al. [55] found signals from Si dangling bond with unpaired electron by EPR and estimated the hole trap density to be one order larger than the electron trap density. Further analysis proposed nitrogen vacancies in amorphous bulk SiN is responsible for the hole traps. Within the framework of Quantum-

Espresso simulation, Gritsenko et al. [56] calculated the model of nitrogen vacancy with hydrogen passivation and obtained hole trap energy level 0.9 eV above valance band.

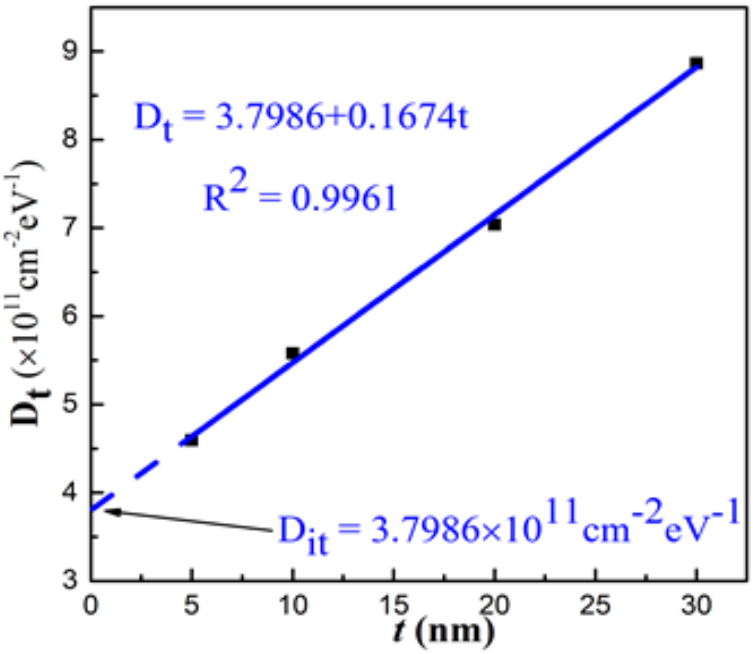


Figure 2.11 The linear fitting of D_t versus thickness. The y-axis intercept shows the D_{it} is ~3.8×10^{11} cm^{-2} eV^{-1}.

The extracted value of the actual average D_{it} is around 3.8×10^{11} cm^{-2} eV^{-1}, which is lower than the measured D_t without considering hole traps in SiN. Mizue et al. [37] did not consider the effect from bulk Al_2O_3 hole traps in Al_2O_3/AlGaN system and reported minimum interface state density value of 1×10^{12} cm^{-2} eV^{-1} near the bottom of conduction band using photo-assisted CV methods, which is overestimated when compared with (1-3) $\times$ 10^{11} cm^{-2} eV^{-1} [52]. Using UV-assisted C-V methods, Swenson et al. [35] also obtained the overestimated interface state density value for SiN/GaN. The analysis demonstrated in this study suggests the overestimated values can result by describing D_t as the actual D_{it}.

2.8 Summary

The methods developed in this chapter are very useful to study the dielectrics on GaN or in general, WBG semiconductors, in terms of two aspects. First, the actual interface states density can be extracted when the D_t fitting line is extrapolated to zero-thickness, which is the exact interface ideally. Second, the parameters n_{it0} and $dn_{it}/d\psi_s$ can set up a comparable value to evaluate the quality of the bulk dielectrics. To some extent, n_{it0} is an overall indicator for the bulk dielectric structural imperfections. Also, the $dn_{it}/d\psi_s$ can provide information of dielectric trap distribution across energy scale. In all, the two aspects quantified in the study can be critical for evaluating and improving the quality of dielectrics, which may determine the gate leakage, breakdown voltage, DC-RF dispersion and reliability during device operations.

In summary, we have analyzed the interface states of SiN on N-polar GaN systematically through a series of dielectrics with different thicknesses. Our results indicated the existence of uniform hole traps in bulk SiN after UV exposure. An improved model including the effect of SiN hole traps is derived and applied to extract the accurate D_{it} value. The average D_{it} is ~3.8×10^{11} cm^{-2} eV^{-1} after extrapolated measured trap density to zero-thickness dielectric. Also, new hole traps parameters in SiN from the analysis are proposed as potential evaluation for the quality of dielectrics grown on semiconductors. The model and analysis can potentially pave the way for accurate determination of D_{it} in dielectrics on GaN and can be extended to other WBG semiconductor systems as well. Based on the accurate D_{it} data obtained from the model, researchers are able to optimize the dielectrics on WBG semiconductors.

References

1. I. Tamm, “On the possible bond states of electrons on a crystal surface,” *Phys. Z. Sowjetunion.* 1, 733, 1932.

2. W. Shockley, “On the surface states associated with a periodic potential,” *Phys. Rev.* 56, 317, 1939.

3. W. E. Spicer, P. W. Chye, P. R. Skeath, C. Y. Su, and I. Lindau, “New and unified model for Schottky barrier and III-V insulator interface states formation,” *J. Vac. Sci. Technol.* 16, 1422, 1979.

4. W. E. Spicer, I. Lindau, P. Skeath, and C. Y. Su, “Unified defect model and beyond,” *J. Vac. Sci. Technol.* 17, 1019, 1980.

5. L. Kipp, R. Adelung, N. Trares-Wrobel, and M. Skibowski, “Extrinsic surface states traced by surface photovoltage in photoemission,” *App. Phys. Lett.*, vol. 74, 1836, 1999.

6. W. Schottky, “Discrepancies in Ohm’s laws in semiconductors,” *Phys. Z* 41, 570, 1940.

7. N. F. Mott, “Note on the contact between a metal and an insulator or semi-conductor,” *Math. Proc. Cambridge* 34, 568, 1938.

8. J. Bardeen, “Surface states and rectification at a metal semi-conductor contact,” *Phys. Rev.* 71, 717, 1947.

9. V. Heine, “Theory of surface states,” *Phys. Rev.* 138, A1689, 1965.

10. F. Flores and C. Tejedor, “A simple approach to covalent surfaces,” *J. Phys. France* 38, 949, 1977.

11. J. Tersoff, “Theory of semiconductor heterojunctions: the role of quantum dipoles,” *Phys. Rev. B* 30, 4874, 1984.

12. W. Monch, “Chemical trends of barrier heights in metal-semiconductor contacts: on the theory of the slope parameter,” *Appl. Surf. Sci.* 92, 367, 1996.

13. B. S. Eller, J. Yang, and R. J. Nemanich, “Electronic surface and dielectric interface states on GaN and AlGaN,” *J. Vac. Sci. Technol. A* 31, 050807, 2013.

14. R. Degraeve et al. “Effect of bulk trap density on HfO2 reliability and yield,” *IEDM Tech. Dig.,* p. 935, 2003.

15. A Y Kang, P M Lenahan, J F Conley, “Electron spin resonance observation of trapped electron centers in atomic-layer-deposited hafnium oxide on Si,” *App. Phys. Lett.* 83, 3407, 2003.

16. P M Lenahan, J F Conley, “Magnetic resonance studies of trapping centers in high-k dielectric films on silicon,” *IEEE Trans EDM Reliab*. 5, 90, 2005.

17. A S Foster, V B Sulimov, F L Gejo, A L Shluger, R N Nieminen, “Structure and electrical levels of point defects in monoclinic zirconia,” *Phys Rev B* 64, 224108, 2001.

18. A S Foster, F L Gejo, A L Shluger, R N Nieminen, “Vacancy and interstitial defects in hafnia,” *Phys Rev B* 65, 174117, 2002.

19. M. Houssa, J.L. Autran, A. Stesmans, and M.M. Heyns, “Model for interface defect and positive charge generation in ultrathin SiO2/ZrO2 gate dielectric stacks,” *Appl. Phys. Lett.* 81, 709, 2002.

20. G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, “Review on high-k dielectric reliability issues,” *IEEE Trans on Device and materials Reliability,* vol 5., 5, 2005.

21. J. Chen, Y. Nakasaki, and Y. Mitani, “Deep insight into process-induced pre-existing traps and PBTI stress-induced trap generations in high-k gate dielectric through systematic RTN characterizations and ab initio calculations,” *2016 Symposium on VLSI* technology digest of technical papers.

22. D. M. Fleetwood, “Border traps in MOS devices,” *IEEE Trans on Nuclear Science,* vol. 39, 269, 1992.

23. U. Mishra, L. Shen, T. Kazior, and Y.-F. Wu, “GaN-based RF power devices and amplifiers,” *Proceedings of the IEEE,* vol. 96, pp. 287-305, 2008.

24. F. lacopi, M. Van Hove, M. Charles, and K. Endo, “Power electronics with wide bandgap materials: Toward greener, more efficient technologies,” *MRS Bulletin,* vol. 40, pp. 390-395, 2015.

25. M. Asif Khan, G. Simin, J. Yang, J. Zhang, A. Koudymov, M.S. Shur, R. Gaska, X. Hu, and A. Tarakji, “Insulating gate III-N heterostructure field-effect transistors for high power microwave and switching applications,” *IEEE Transactions on Microwave Theory and Technique*, vol. 51, pp. 624-633, 2003.

26. R. Engel-Herbert, Y. Hwang, and S. Stemmer, “Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces,” *Journal of Applied Physics*, vol. 108, p. 124101, 2010.

27. X. Zheng, H. Li, M. Guidry, B. Romanczyk, E. Ahmadi, K. Hestroffer, S. Wienecke, S. Keller, and U. K. Mishra, “Analysis of MOCVD SiNX passivated N-polar GaN MIS-HEMTs on sapphire with high fmax□VDS,Q,” *IEEE Electron Device Letters*, vol. 39, p. 409-412, 2018.

28. Y. Yue, Y. Hao, J. Zhang, J. Ni, W. Mao, Q. F, and L. Liu, “AlGaN/GaN MOS-HEMT with HfO2 dielectric and Al2O3 interfacial passivation layer grown by atomic layer deposition,” *IEEE Electron Device Letter*, vol. 29, pp. 838-840, 2008.

29. X. Hu, A. Koudymov, G. Simin, J. Yang, M. Asif Khan, A. Tarakji, M.S. Shur, and R. Gaska, “Si3N4/AlGaN/GaN-metal-insulator-semiconductor heterostructure field effect transistors,” *Applied Physics Letter*, vol. 79, pp. 2832-2834, 2001.

30. H. Deuling, E. Klausmann, and A. Goetzberger, “Interface states in Si-SiO2 interface,” *Solid-State Electronics*, vol. 15, pp. 559-571, 1972.

31. A. Hiraiwa, S. Okubo, K. Horikawa, and H. Kawarada, “Advanced photo-assisted capacitance-voltage characterization of insulator/wide bandgap semiconductor interface using super-bandgap illumination,” *Journal of Applied Physics*, vol. 125, p. 175704, 2019.

32. A.R. Arehart, A. Corrion, C. Poblenz, J.S. Speck, U.K. Mishra, and S.A. Ringel, “Deep level optical and thermal spectroscopy of traps in n-GaN grown by ammonia molecular beam epitaxy,” *Applied Physics Letters*, vol. 93, p. 112101, 2008.

33. A.F. Basile, J. Rozen, J.R. Williams, L.C. Feldman, and P.M. Mooney, “Capacitance-voltage and deep level transient spectroscopy characterization of defects near SiO2/SiC interfaces,” *Journal of Applied Physics*, vol. 109, p. 064514, 2011.

34. R. Yeluri, X. Liu, B. L. Swenson, J. Lu, S. Keller, and U. K. Mishra, “Capacitance-voltage characterization of interfaces between positive valence band offset dielectrics and wide bandgap semiconductors,” *Journal of Applied Physics*, vol. 114, p. 083718, 2013.

35. B.L. Swenson, and U.K. Mishra, “Photoassisted high-frequency capacitance-voltage characterization of the Si3N4/GaN interface,” *Journal of Applied Physics*, vol. 106, p. 064902, 2009.

36. Y.Q. Wu, T. Shen, P.D. Ye, and G.D. Wilk, “Photo-assisted capacitance-voltage characterization of high-quality atomic-layer-deposited Al2O3/GaN metal-oxide-semiconductor structures,” *Applied Physics Letters*, vol. 90, p. 143504, 2007.

37. C. Mizue, Y. Hori, M. Miczek, and T. Hashizume, “Capacitance-Voltage characterization of Al2O3/AlGaN/GaN structures and state density distribution at Al2O3/AlGaN interface,” *Japanese Journal of Applied Physics*, vol. 50, p. 021001, 2011.

38. I. Sayed, B. Bonef, W. Liu, S. Chan, J. Georgieva, J. S. Speck, S. Keller, and U. K. Mishra, “Electrical properties and interface abruptness of AlSiO gate dielectric grown on (000-1) N-polar and (0001) Ga-polar GaN,” *Applied Physics Letters*, vol. 115, p. 172104, 2019.

39. B. Swenson, “Contributions to the understanding of (Al,Ga)N-silicon nitride interfaces,” *PhD dissertation,* University of California, Santa Barbara, 2011.

40. M. Tapajna, M. Jurkovic, L. Valik, S. Hascik, D. Gregusova, F. Brunner, E. M. Cho, and J. Kuzmik, “Bulk and interface trapping in the gate dielectric of GaN based metal-oxide-semiconductor high-electron-mobility transistors,” *Applied Physics Letter,* vol. 102, p. 243509, 2013.

41. X. Sun, O.I. Saadat, K.S. Chang-Liao, T. Palacios, S. Cui, and T.P. Ma, “Study of gate oxide traps in HfO2/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by use of ac transconductance method,” *Applied Physics Letter,* vol. 102, p. 103504, 2013.

42. B. Romanczyk, S. Wienecke, M. Guidry, H. Li, E. Ahmadi, X. Zheng, S. Keller, and U. K. Mishra, “Demonstration of constant 8 W/mm power density at 10, 30, and 94 GHz in state-of-the-art millimeter-wave N-polar GaN MISHEMTs,” *IEEE Transactions on Electron Devices*, vol. 65, pp. 45-50, 2018.

43. O. S. Koksaldi, J. Haller, H. Li, B. Romanczyk, M. Guidry, S. Wienecke, S. Keller, and U. K. Mishra, “N-Polar GaN HEMTs Exhibiting Record Breakdown Voltage Over 2000 V and Low Dynamic On-Resistance,” *IEEE Electron Device Letters*, vol. 39, pp. 1014-1017, 2018.

44. I. Sayed, W. Liu, S. Chan, C. Gupta, M. Guidry, H. Li, S. Keller, and U. K. Mishra, “Net negative fixed interface charge for Si3N4 and SiO2 grown in-situ on 000-1 N-polar GaN,” *Applied Physics Letters*, vol. 115, p. 011928, 2019.

45. T. Cook, C. Fulton, W. Mechouch, R. Davis, G. Lucovsky, and R. Nemanich, “Band offset measurement of the Si3N4 /GaN(0001) interface,” *Journal of Applied Physics,* vol. 94, pp. 3949-3954, 2003.

46. S.E. Curry. P.M. Lenahan, D.T. Krick, J. Kanicki, and C. Kirk. “Evidence for a negative electron-electron correlation energy in the dominant deep trapping center in silicon nitride films,” *Applied Physics Letters*, vol. 56, pp. 1359-1361, 1990.

47. Y. Kamigaki, S. Minami, and H. Kato, “A new portrayal of electron and hole traps in amorphous silicon nitride,” *Journal of Applied Physics,* vol. 68, pp. 2211-2215, 1990.

48. D. Jouse, J. Kanicki, and J.H. Stathis, “Observation of multiple silicon dangling bond configuration in silicon nitride,” *Applied Physics Letters,* vol. 54, pp. 1043-1045, 1989.

49. E. Vianello, F. Driussi, P. Blaise, P. Palestri, D. Esseni, L. Perniola, G. Molas, B.D. Salvo, and L. Selmi. “Explanation of the charge trapping properties of silicon nitride storage layers for NVMs—Part II: Atomic and electrical modeling,” *IEEE Transaction on Electron Devices,* vol 58. pp. 2490-2499. 2011.

50. X. Liu, R. Yeluri, J. Kim, S. Lal, A. Raman, C. Lund, S. Wienecke, J. Lu, M. Laurent, and S. Keller, “In-situ metalorganic chemical vapor deposition and capacitance-voltage characterizations of Al2O3 on Ga-face GaN metal-oxide-semiconductor capacitors,” *Applied Physics Letters,* vol. 103, p. 053509, 2013.

51. A. Iqbai, W.B. Jackson, C.C. Tsai, J.W. Allen, and C.W. Bates Jr., “Electronic structure of silicon nitride and amorphous silicon/silicon nitride band offsets by electron spectroscopy,” *Journal of Applied Physics,* vol. 61, pp. 2947-2954, 1987.

52. Y. Hori, C. Mizue, and T. Hashizume, “Process conditions for improvement of electrical properties of Al2O3/n-GaN structure prepared by atomic layer deposition,” *Japanese Journal of Applied Physics,* vol. 49, p. 080201, 2010.

53. H. Aozasa, I. Fujiwara, A. Nakamura, Y. Komatsu, “Analysis of carrier traps in Si3N4 in oxide/nitride/oxide for metal/oxide/nitride/oxide/silicon nonvolatile memory,” *Jpn. J. Appl. Phys. 38,* 1441–1447, 1999.

54. W.L. Warren, J. Robertson, et al., “Electron paramagnetic resonance investigation of charge trapping centers in amorphous silicon nitride films,” *J. Appl. Phys.* 74 (6), 4034–4046, 1993.

55. Y. Kamigaki et al., “A new portrayal of electron and hole traps in amorphous silicon nitride,” *J. Appl. Phys.* 68 (5), 2211–2215, 1990.

56. V.A. Gritsenko, S.S. Nekkrashevich, V.V. Vasilev, A.V. Shaposhnikov, “Electronic structure of memory traps in silicon nitride,”, *Microelectronic Engineering* 86, 1866-1869, 2009.

57. Eli Lusky, Yosi Shacham-Diamond, Assaf Shappir, et al., “Traps spectroscopy of the Si3N4 layer using localized charge-trapping nonvolatile memory device,” *Appl. Phys. Lett*. 85 (4), 2004.

Chapter 3. A systematic dielectric analysis of AlSiO on N-polar GaN

The bulk and interfacial properties of aluminum silicon oxide (AlSiO) on N-polar GaN were investigated systematically employing capacitance-voltage (C-V) methods on metal-oxide-semiconductor capacitors (MOSCAPs) using a thickness series of the AlSiO dielectric. The fixed charge density, electron slow trap density and electron fast trap density located near the interface were extracted to be -1.5×10^{12} cm^{-2}, 3.7×10^{11} cm^{-2} and 1.9×10^{11} cm^{-2}, respectively. Using ultraviolet (UV) assisted C-V methods, an average interface state density of $\sim 4.4 \times 10^{11}$ cm^{-2} eV^{-1} and a hole trap concentration in bulk AlSiO of $\sim 8.4 \times 10^{18}$ cm^{-3} were measured. The negative fixed interface charge makes it favorable to achieve a normally-off GaN transistor. The analysis presented in this chapter provides a systematic and quantitative model to study the properties of oxide dielectrics on wide bandgap (WBG) semiconductors, which can promote the development of MOS-based WBG semiconductor devices.

3.1 AlSiO on GaN

3.1.1 AlSiO on Ga-polar GaN

Aluminum silicon oxide (AlSiO) dielectric using high-temperature MOCVD *in-situ* growth on Ga-polar GaN was first developed by S. Chan et al. at UCSB in 2016 [1]. The selection of AlSiO involved considerations on the high band offset to reduce the possible leakage current over the barrier and the high dielectric constant (relative to SiO_2) to reduce the electric field stress in the dielectric [2]. As shown in **Fig. 3.1**, the calculated energy band lineup with respect to GaN [3] suggests Al_2O_3 and SiO_2 as attractive candidates with both large positive conduction band and valence band offset. As a comparison, the experimental

SiN band alignment has a negative valence band offset of -0.6 eV [4], as discussed in Chapter 1. While Al_2O_3 has relatively lower band offsets than SiO_2, the higher dielectric constant of Al_2O_3 is an advantage. Alloying Si with tunable concentration into Al_2O_3 can form amorphous AlSiO and allows the ability to tune these properties to meet specific applications.

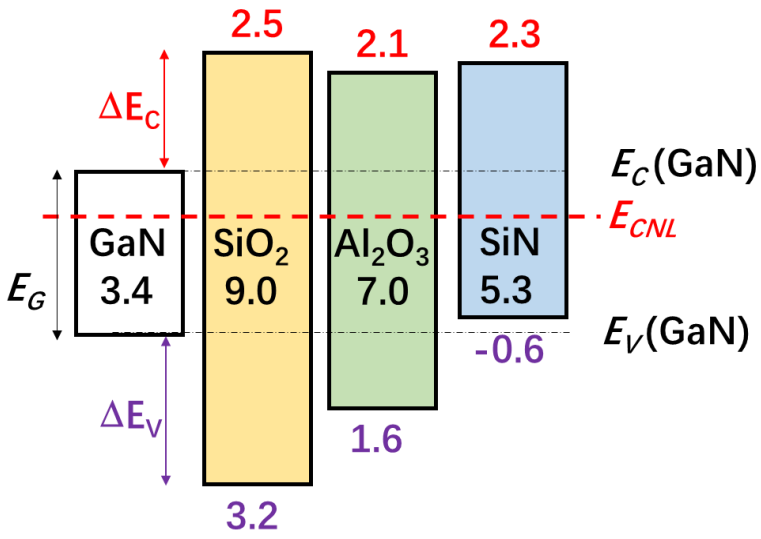


Figure 3.1 The calculated energy band lineup of SiO2 and Al2O3 with respect to GaN from [3]; the experimental SiN band alignment data is from [4].

In that study [1], the AlSiO on Ga-polar GaN MOS-capacitors exhibited reduced interfacial trap density, low gate leakage and ultra-low hysteresis, compared with the Al_2O_3 dielectric. Later, Ito et al. [5] and Kikuta et al. [6] from Toyota Central R&D Labs conducted low-temperature (250 °C) ALD method to deposit *ex-situ* AlSiO (or "Al_2O_3/SiO_2 nanolaminates") by stacking Al_2O_3 and SiO_2 layer by layer.

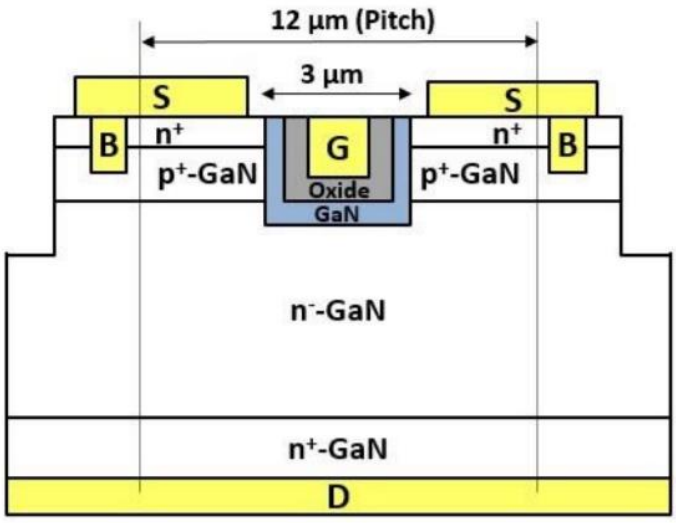


Figure 3.2 The structure of OG-FET using MOCVD AlSiO as the gate oxide in the trench gate structure [7].

In 2017, Gupta et al. reported the first demonstration of a GaN vertical trench MOSFET using the AlSiO as gate dielectric, which is called the OG-FET [7]. The structure of OG-FET is shown in **Fig. 3.2**. After the gate region recess etch, the AlSiO and GaN were grown *ex-situ* on the trenched $n^+/p^+/n^-$ GaN surface to improve the vertical channel mobility and hold high voltage. Due to the high quality of the AlSiO/GaN grown by MOCVD, the resulted normally-off vertical GaN FET showed excellent breakdown voltage of 1.2 kV and an on-resistance of 2 mΩ cm^{-2}. These outstanding results with high breakdown voltage and low on-resistance gained great attention among GaN power electronics researchers.

3.1.2 AlSiO on N-polar GaN

The successful growth of AlSiO on etched Ga-polar GaN surface in a trench structure inspired the possible application of AlSiO in the N-polar GaN deep recess HEMT structure, which also has an etched trench gate structure. To investigate the interfaces between the

MOCVD grown AlSiO on Ga-polar GaN and N-polar GaN, Sayed et al. [8] conducted a comparative study by the means of atom probe tomography (APT) measurements. Through a laser-pulse mode to evaporate materials layer by layer, APT was used to collect the 3D elemental information and evaluate the alloy distribution in the AlSiO layer and AlSiO/GaN interface. The one-dimensional concentration profile of Al, O and Ga was reconstructed from the center of the measured 3D APT results and is shown in **Fig. 3.3**.

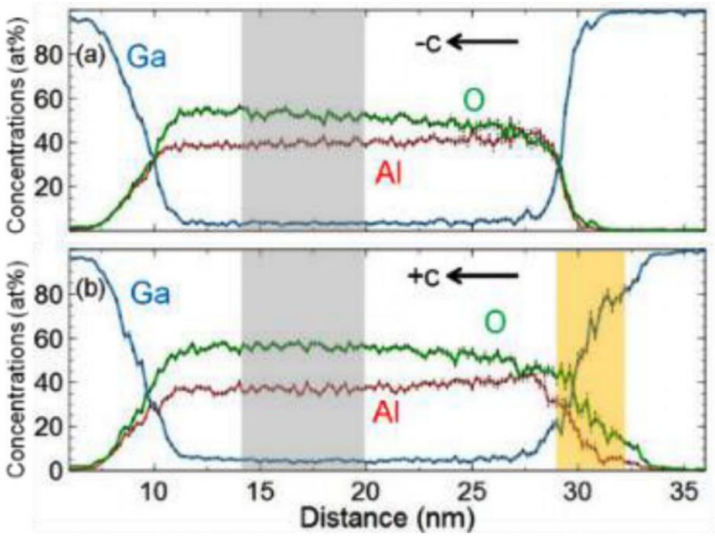


Figure 3.3 The one-dimensional concentration profiles of Al, O and Ga along the growth direction from the APT 3D reconstruction of (a) the N-polar sample and (b) the Ga-polar sample [8].

In **Fig. 3.3**, the AlSiO/N-polar GaN with a positive surface polarization charge shows a more abrupt interface, as compared to that grown on Ga-polar GaN with a negative surface polarization charge. The abrupt interface for the N-polar AlSiO MOSCAP has resulted in a lower interface trap density and negligible frequency dispersion in C-V characteristics with respect to the Ga-polar MOSCAP. Hence AlSiO on N-polar GaN can potentially be applied in high-performance N-polar GaN-based transistors. The detailed understanding on the AlSiO grown on N-polar GaN will be helpful.

In the previous chapter and reported in other publications, we conducted comprehensive studies of MOCVD grown SiN on N-polar GaN using capacitance-voltage (C-V) methods [9, 10]. The basic framework to analyze the dielectric properties, such as the fixed interface charge, interface states and bulk dielectric hole traps, was developed. In this chapter, we summarize and extend these methods to study the dielectric AlSiO on N-polar GaN. Through a thickness series of AlSiO on N-polar GaN MOSCAPs and capacitance-voltage (C-V) methods, our comprehensive analysis includes fixed interface charges, near-interface electron traps, dielectric built-in electric field, interface state density and bulk hole traps. The approach pursued in this study can be widely applied to other dielectrics and boost the progress of WBG semiconductor MOSCAPs and MOSFETs. Some figures and materials of the following chapter was reproduced from [**Wenjian Liu**, Islam Sayed, Jana Georgieva, Silvia Chan, Stacia Keller, Umesh K Mishra, A systematic and quantitative analysis of the bulk and interfacial properties of the AlSiO dielectric on N-polar GaN using capacitance–voltage methods. *Journal of Applied Physics,* 128, 074101(2020).], with the permission of AIP Publishing.

3.2 Epitaxial Structure and Device Fabrications

The schematic structure of the MOSCAPs composed of AlSiO with a silicon composition of 37% grown on N-polar GaN is shown in **Fig. 3.4**. The N-polar epitaxial layers were grown on c-plane sapphire substrates misoriented by 4° towards a-plane by metal organic chemical vapor deposition (MOCVD). Prior to loading the substrate into the MOCVD chamber, three cycles of UV-ozone and HF treatment were conducted, which was found to reduce the Si concentration effectively [11,12]. The precursors used in this work were trimethylgallium

(TMGa), ammonia (NH_3), oxygen (O_2), trimethyl-aluminum (TMAl) and disilane (Si_2H_6). From bottom to top, the epitaxial layers included 1.5 µm unintentionally doped GaN, 800 nm n^+ GaN:Si with a doping concentrations of 2.5×10^{18} cm^{-3}, 600 nm n^- GaN with unintentional doping of 2.5×10^{17} cm^{-3} and the AlSiO layer. The AlSiO layers with different thicknesses (9 nm, 17 nm, and 25 nm) were grown *in situ* at 700 °C in our reactor which is capable of growing both nitrides and oxides in the same run. The TMAl, Si_2H_6, and O_2 flows used for the AlSiO growth were 3.2 µmol/min, 3.2 µmol/min, and 4.4 mmol/min., respectively.

The fabrication process is similar to that of the SiN/N-polar GaN MIS-capacitor in previous chapter. The MOCVD grown AlSiO was etched by the diluted buffered HF. Ti/Au (25 nm/200 nm) was deposited by e-beam evaporation as the gate and ohmic electrodes after the reactive ion etching (RIE) etching into n+ GaN.

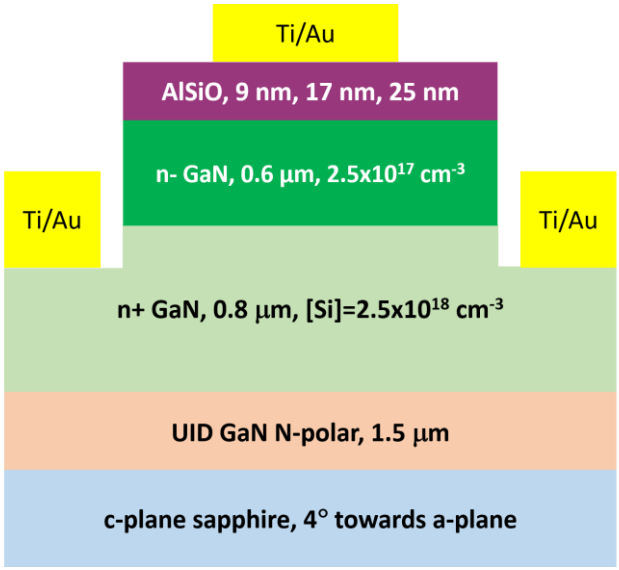


Figure 3.4 The cross-section schematic of the AlSiO on N-polar GaN MOSCAPs**.**

C-V stress measurements were conducted to extract the near-interface electron fast and slow trap densities. For the interface states and bulk hole trap study, ultraviolet (UV) assisted C-V methods were used to overcome the issue of the low generation rate of holes in n-type GaN as described in chapter 29, 13,14]. The frequency and amplitude of AC signals used for C-V measurements were 1 MHz and 50 mV, respectively. The DC voltage was swept with a 35-mV voltage step and a 0.6 V/s sweep rate. All measurements were performed using an Agilent B1500 semiconductor device analyzer equipped with medium power source/monitor units and a multi-frequency capacitance measurement unit. An EXFO OmniCure1000 spot curing system with a high-pressure Hg lamp filtered between 320 nm and 500 nm was used as the UV illumination source.

3.3 Electron Traps and Fixed Charge at/near the Interface

3.3.1 Electron fast and slow traps near the AlSiO/N-polar GaN interface

The slow and fast near-interface states are distinguished according to their different electron emission characteristics. Interface states with fast emission characteristics are referred to as fast traps and interface states with slow emission time characteristics are referred to as slow traps. The densities of fast and slow traps were quantified by measuring the hysteresis of C-V measurements.

The C-V curves of the AlSiO MOSCAPs without and with voltage stress were measured and shown in **Fig. 3.5** (a) and (b). The MOSCAPs with different AlSiO thicknesses were measured up to different maximum positive voltages to maintain the same maximum electric fields in AlSiO. The maximum negative bias is -10 V for all three samples. The C-V measurements included two stages. The first stage included sweeping the voltage from depletion to accumulation, holding the voltage for 10 minutes stress under accumulation, and

then sweeping the voltage backward from accumulation to depletion. The second C-V sweep includes sweeping the voltage from depletion to accumulation and backward without any voltage stress.

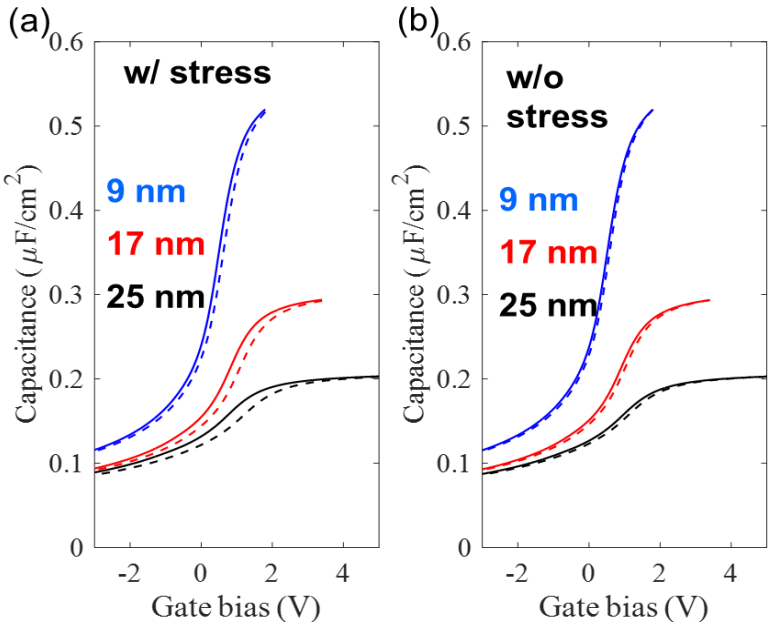


Figure 3.5 C-V curves of AlSiO MOSCAPs (a) without and (b) with stress for different AlSiO thicknesses. The CV curves in (a) and (b) are plotted only from -3 to 5V for visual clarity. The solid lines represent CV sweeps from depletion bias to accumulation bias (the forward sweep) and the dotted lines represent CV sweeps from accumulation bias to depletion bias (the reverse sweep).

Since the first C-V sweep included additional 10 minutes voltage stress, the electrons filled both the slow and fast near-interface states. Since the second C-V sweep did not include voltage stress duration in accumulation, the electrons filled only fast near-interface traps. Hence, the hysteresis (ΔV_{FB}), measured from the second C-V curve, was used to estimate density of fast near interface states. The hysteresis, measured from the first C-V curve, was used to estimate the summation of density of fast and slow near interface states. The difference

in the hysteresis from the first and second C-V sweeps gave the density of slow trap states.

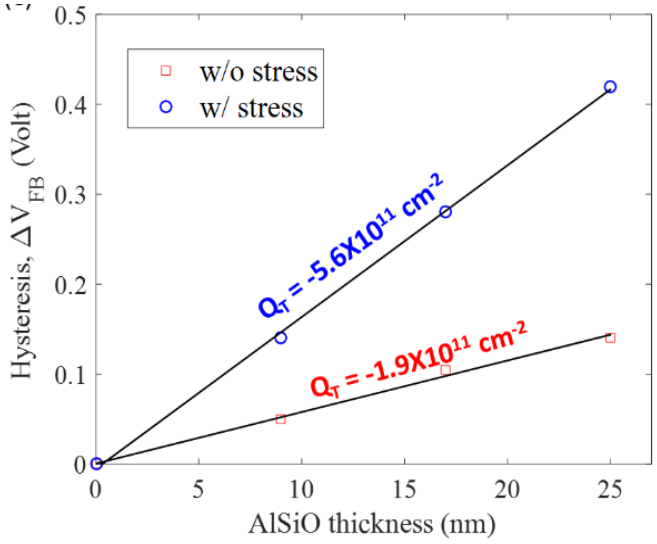


Figure 3.6 ΔV_{FB} vs. AlSiO thickness as extracted from Fig. 2.5 without stress (red square) and with stress (blue circle) and their fitting lines to obtain the net fixed interface charge.

The electron trap density Q_T can be expressed through [15-18],

$$Q_T = C_{ox}\Delta V_{FB}, \tag{3.1}$$

where the C_{ox} is the oxide capacitance biased to accumulation. The enhancement of ΔV_{FB} after stressing the MOSCAPs is evident when **Fig. 3.5** (a) and (b) are compared. The ΔV_{FB} values are plotted in Fig. 2.6. The linear relationship and the good fit through the origin for both cases of with and without stress indicate the validity of the **Eq. 3.1**, implying the near-interface location of electron traps. The fast trap density was extracted to be 1.9×10^{11} cm^{-2} and the slow trap density excluding the contribution from fast traps is 3.7×10^{11} cm^{-2}. Compared with SiN on N-polar GaN with 2.6×10^{11} cm^{-2} fast electron trap density and 2.63×10^{12} cm^{-2} slow electron trap density [9], AlSiO on N-polar has less slow and fast electron trap densities. The almost one order of magnitude smaller slow electron trap density indicates that AlSiO can

offer better flat-band and threshold voltage stability.

3.3.2 Net negative interface fixed charge and built-in electric field in the AlSiO

The flat band voltages (V_{FB}) extracted from the forward sweep curves in Fig. 2.5 are depicted in Fig. 2.7 and follow a linear dependence on the AlSiO thickness. Assuming negligible charges in the dielectric, the V_{FB} is given by [19],

$$V_{FB} = \phi_{ms} - \frac{qQ_{F,net}}{\varepsilon_0 \varepsilon_{r1}} t \quad , \tag{3.2}$$

where ϕ_{ms} is the work function difference between metal and semiconductor, $Q_{F,net}$ is the net charge at the AlSiO and GaN interface, t is the dielectric thickness, q is the electron charge, ε_0, ε_{r1} are the vacuum permittivity and relative dielectric constant of AlSiO (estimated to be 7.65 based on the 37% Si concentration in AlSiO), respectively.

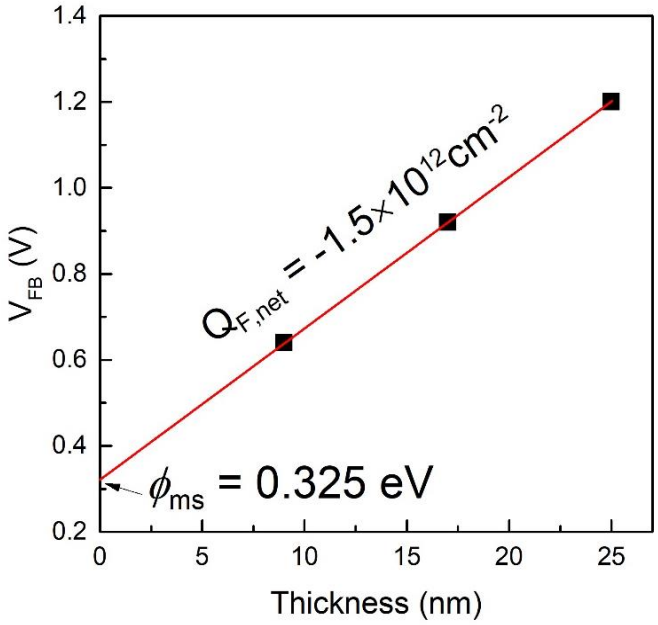


Figure 3.7 The extracted V_{FB} vs. AlSiO thickness to obtain $Q_{F,net}$.

Through fitting with the **Eq. 3.2**, we obtain a net negative interface fixed charge of -1.5 × 10^{12} cm^{-2} at the AlSiO/N-polar GaN interface, and the metal-semiconductor work function difference is 0.325 V. The obtained work function difference is close to the ideal value with Ti work function (4.33 eV) and n^- GaN work function (~4.0 eV [20]). Compared with the positive interface fixed charge in the Ga-polar case [16], the negative interface fixed charge in the N-polar case is beneficial to design and achieve normally-off transistors.

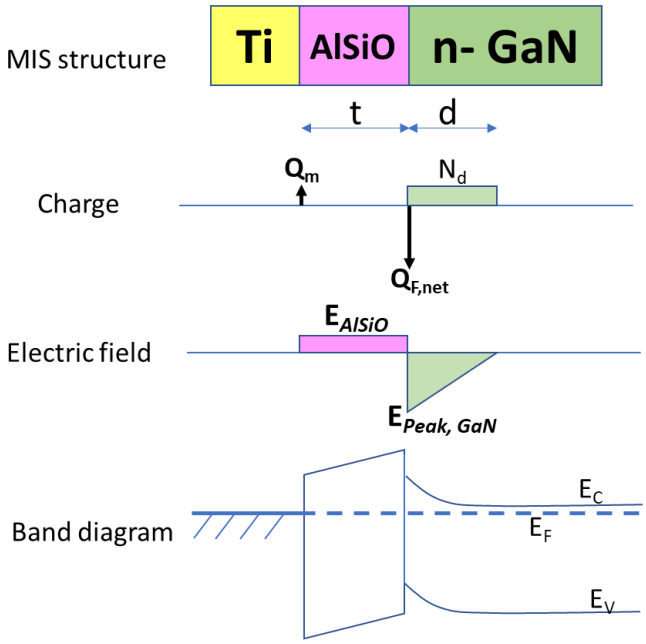


Figure 3.8 At zero bias, the charge profile, electric field and the energy band diagram of the MOSCAPs.

Furthermore, the built-in electric field in the AlSiO at zero bias (E_{AlSiO}) can be calculated. Based on the extracted $Q_{F,net}$ and ϕ_{ms}, the charge profile, electric field and energy band diagram are sketched in **Fig. 3.8**. From the diagrams, the charge neutrality and ϕ_{ms} equations are:

$$Q_m + N_d \bullet d = -Q_{F,net}, \tag{3.3}$$

$$\phi_{ms} = -\frac{qQ_m}{\varepsilon_0 \varepsilon_{r1}} t + \frac{q(-Q_{F,net} - Q_m)}{2\varepsilon_0 \varepsilon_{r2}} d \quad , \tag{3.4}$$

where Q_m is the sheet charge in the metal, N_d is the doping concentration in n-GaN, d is the depletion region width in n-GaN, and ε_{r2} are the relative dielectric constant of GaN. After solving the above **Eq. 3.3** and **Eq. 3.4** with respect to different dielectric thicknesses t, the E_{AlSiO} were calculated and summarized in **Table. 3.1**. The magnitude of the E_{AlSiO} in all samples are < ~0.1 MV/cm, while the peak electric fields in GaN (E_{AlSiO}) are > ~0.22 MV/cm suggesting a near balancing between the net interface charge and the ionized charge in n^- GaN. The possible reason behind this observation is the formation of compensating interface fixed charges during the growth of AlSiO on N-polar GaN with the positive surface polarization charge [9, 16]. It is noteworthy that the introduced negative fixed interface charges may alleviate the electric field stress on AlSiO when the GaN operates under some extreme electric field.

Table 3.1 The calculated AlSiO built-in electric field values (| E_{AlSiO} |), peak electric field values in GaN (| $E_{Peak, GaN}$ |) for different MOSCAPs.

***t* (nm)**	**9**	**17**	**25**
d (nm)	54.9	56.5	58.5
Q_m ($\times 10^{12}$ cm^{-2})	0.42	0.37	0.33
| E_{AlSiO} | (MV/cm)	0.099	0.087	0.078
| $E_{Peak, GaN}$ | (MV/cm)	0.22	0.23	0.24

3.3.3 Sign of net interface fixed charge

There is accumulated knowledge on the net fixed interface charges at the interface of different dielectrics on Ga-polar and N-polar GaN over the past years from Mishra group.

Table 3.2 summarizes these values for the same kind of dielectrics, which were all *in-situ* grown on GaN by MOCVD. While it is noted that the dielectric growth process on GaN may not be same on the surfaces with two different polarities, the trend might still be indicative.

Table 3.2 Net interface fixed charge of SiN and AlSiO on Ga-polar and N-polar GaN

	Ga-polar GaN	N-polar GaN
SiN	+ 1×10^{12} cm^{-2} [21]	- 2.9×10^{12} cm^{-2} [9]
AlSiO	+ 4×10^{12} cm^{-2} [2]	- 1.5×10^{12} cm^{-2} [8]

From the **Table. 3.2**, the Ga-polar GaN tends to have positive net fixed interface charge for both SiN and AlSiO while the N-polar one has the negative net interface charge. The distinctive characteristic may be explained by the polarity of GaN and the associated surface polarization charge. Ga-polar GaN has negative surface charge due to polarization while N-polar GaN has positive one. During the growth of dielectric on the charged surface, some "compensation" effect [22,23] may happen to minimize the total energy at the interface between dielectric and GaN. This can result in the opposite sign of net fixed charge corresponding to the surface charge. To be more specific, Ga-polar surface will induce net positive fixed interface charge and N-polar one will induce negative fixed interface charge. The possible correlation between the net fixed interface charge and the polarity of GaN is interesting and deeper understanding beyond the hypothesis presented will be beneficial.

3.4 Interface States Density and Bulk Hole Traps in the AlSiO

Using the ultraviolet (UV)-assisted Capacitance-Voltage (C-V) methods, we have developed a methodology accounting for the hole traps in bulk dielectrics and accurately

extract the interface state density. The methodology was applied to the SiN/GaN system which has a negative valence band offset. Here, we expand the same methodology to the AlSiO/GaN system which has a positive valence band offset [2, 24] and illustrate the possible general validity of the methodology.

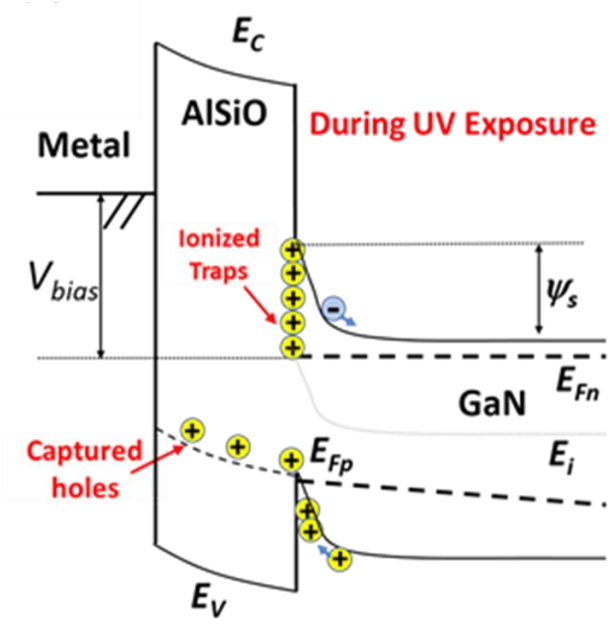


Figure 3.9 The band diagram to show the process of trap ionization and hole capturing during the UV exposure (forming of the hole inversion layer and populating the bulk hole traps).

Based on the UV-assisted C-V methods, the band diagrams are shown in **Fig. 3.9**, **Fig. 3.10** and **Fig. 3.11**, to demonstrate the trap states at different stages and derive the corresponding C-V related equations [10]. Different from the case of SiN on N-polar GaN, the positive valence band offset of AlSiO/N-polar GaN will introduce different behavior of the C-V characteristics because of holes accumulated at the interface as shown in these band diagrams. There were three C-V sweeps in the UV-assisted C-V methods. First, the voltage was swept from depletion to accumulation, the device was held for 10 minutes under accumulation to ensure all the traps are filled with electrons, and then the voltage was swept

backward to depletion. Second, the voltage was swept from depletion to accumulation again and this CV sweep is the *dark curve* in **Fig. 3.12**, as the C-V sweeps were measured under dark condition. Third, the device was held at -10 V bias and was UV-illuminated to generate electron-hole pairs for 30 seconds with power intensity around 0.18 W/cm^2. During the UV exposure, as shown in **Fig. 3.9**, the holes generated by UV illumination accumulate at the AlSiO/N-polar GaN interface forming the hole inversion layer. The accumulated holes at the interface ionize the interface traps and are captured by the bulk hole traps in AlSiO. The detailed capture mechanism of holes currently is not fully understood but hole capture and subsequent hopping as a potential mechanism is surmised. The electron quasi-Fermi level (E_{Fn}) and hole quasi-Fermi level (E_{Fp}) split during to the UV-illumination.

In the **Fig. 3.10**, after the UV exposure, the device is held in depletion bias under the dark environment, the total band bending in GaN increases when the forming of hole inversion layer and populating of bulk hole traps complete. The hole quasi-Fermi level locates at the top of the valance band of GaN at the interface.

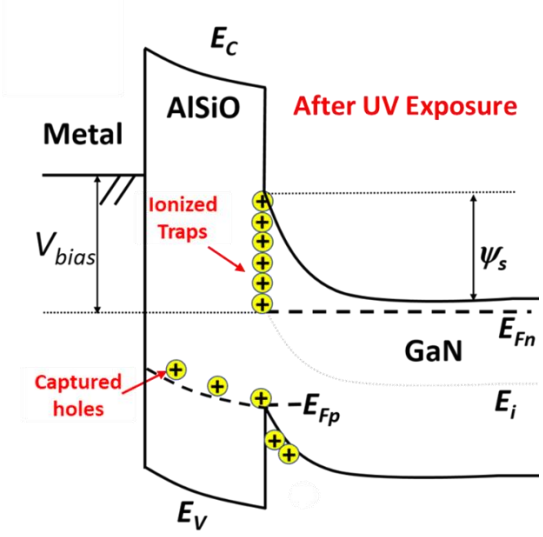


Figure 3.10 The band diagram to show the stabilized ionized traps and captured holes after the UV exposure (completion of forming the hole inversion layer and populating the bulk traps).

In **Fig. 3.11**, during the gate bias sweeping after the UV (*Post-UV* sweeping), the electron and hole fermi level moving cause the neutralization of the interface states and the captured holes in the bulk. The process involves the electron capturing at the interface and in the AlSiO bulk. At the interface, not only the ionized traps will capture electrons to become neutral, but also the accumulated free holes will capture electrons as well. The total capturing of electron can be reflected in the C-V sweeping curves. The third sweep from depletion to accumulation is shown as the *Post-UV curve* in **Fig. 3.12**.

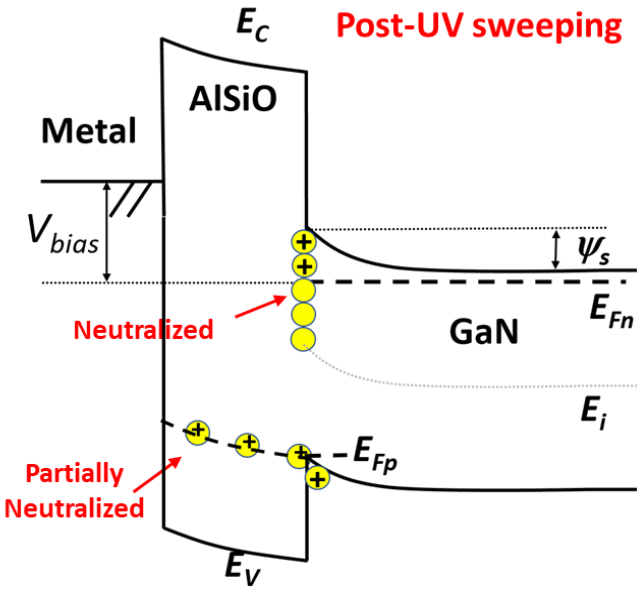


Figure 3.11 The energy band diagrams during post-UV sweeping (neutralization of interface and bulk traps).

Two C-V curves were measured prior to (*Dark Curve*) and post shining UV (*Post-UV curve*) and have been shifted ΔV_{total} to capture the information of holes captured/accumulated at the interface and the bulk dielectric. The measured UV-assisted C-V curves for the MOSCAPs with 9 nm, 17 nm and 25 nm AlSiO are shown in **Fig. 3.12** (a), (b) and (c),

respectively. The voltage shift ΔV_{total} for them are 1.49 V, 3.66 V and 7.68 V, respectively. It is noted that the shifting of *Post-UV* curve to fit the Dark curve at the deep depletion region can introduce some small amount of inaccuracy because the exact same capacitance values in the two curves are not possible to achieve from the measurement results. However, the small amount of inaccuracy would not impact the extraction of D_t or D_{it} since only the derivative of ΔV to surface potential matters and a constant value shift has no effect on D_t or D_{it}.

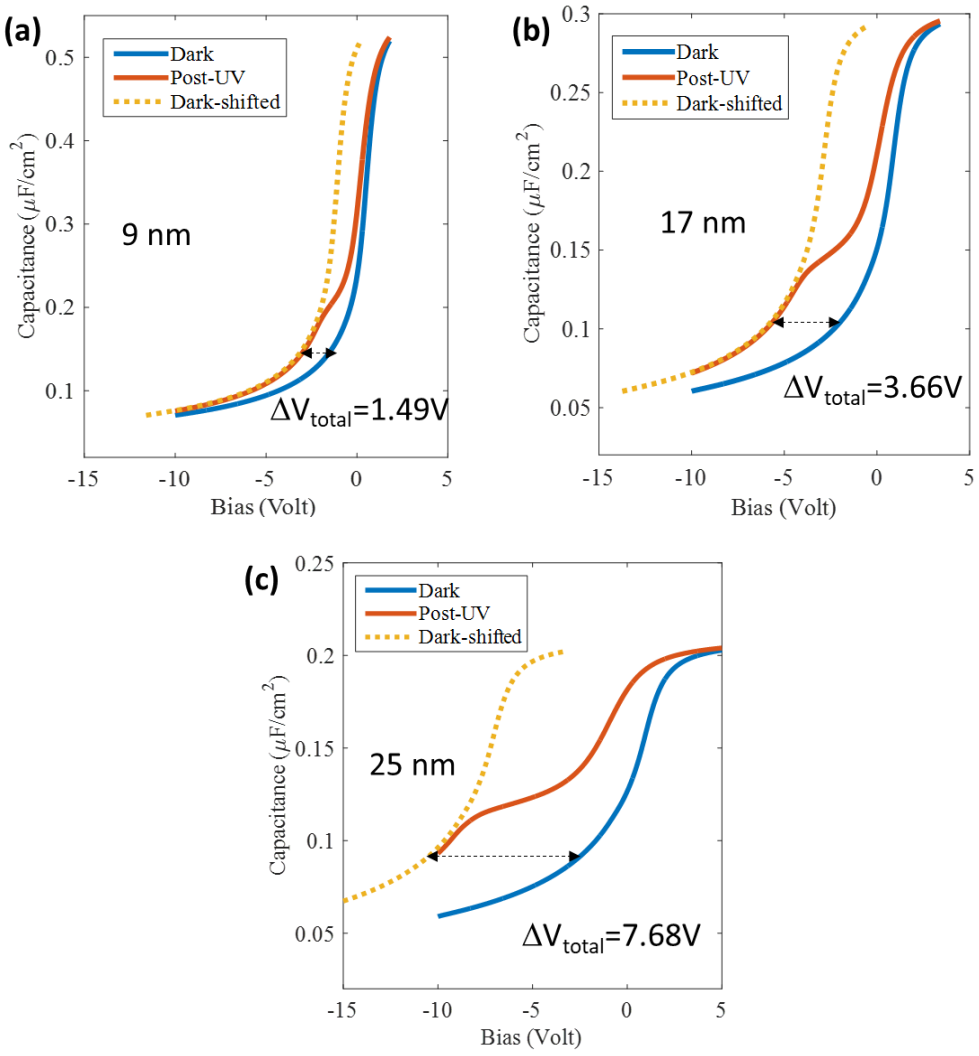


Figure 3.12 The measured C-V curves and shifted voltages ΔV_{total} for (a) 9 nm, (b) 17 nm and (c) 25 nm AlSiO.

The shifted voltage ΔV_{total} versus thickness of the AlSiO is depicted in **Fig. 3.13** and was used to fit the quadratic equation:

$$\Delta V_{total} = q\frac{Q_0}{\varepsilon_0 \varepsilon_{r1} A}t + q\frac{n_{ht0}}{2\varepsilon_0 \varepsilon_{r1}}t^2 \quad , \tag{3.5}$$

where Q_0 is the number of captured and accumulated holes at the interface, A is the device area and n_{ht0} is the uniform hole trap concentration in AlSiO with unit cm^{-3}. The n_{ht0} is extracted to be 8.4×10^{18} cm^{-3} in the AlSiO. The structural origin of the hole traps can be investigated further by the means of defects related first-principle calculations. For instance, Choi et al [25] suggested several types of native defects and impurities as the origin of bulk hole traps in the Al_2O_3.

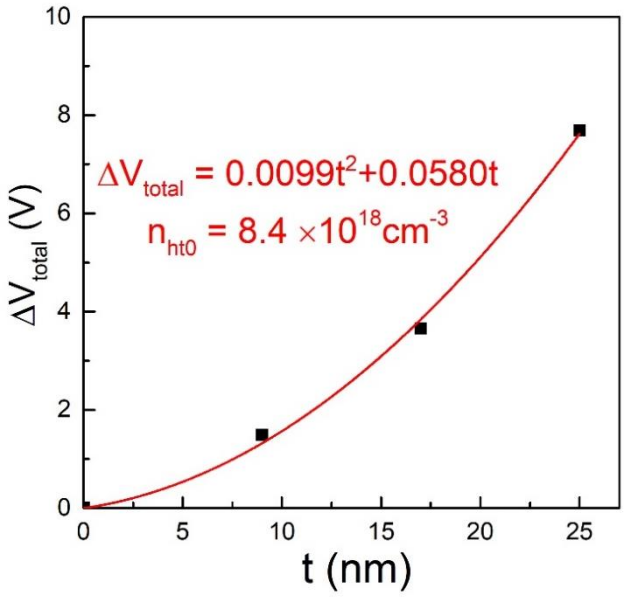


Figure 3.13 The fitting plot of ΔV_{total} vs thickness used to extract hole trap concentration in AlSiO.

Using the same methodology and code developed since Swenson et al and Yeluri et al, the total calculated density of traps (D_t) v.s. the energy is obtained and plotted in **Fig. 3.14**. As

shown in **Fig. 3.14** (a), (b) and (c), the total calculated density of traps (D_t) from photo-C-V curves (black triangles) exhibits a typical "bump" behavior (hole ledge) near E_C, which is an effect from the accumulated holes due to positive valence band offset and not related to positive charges due to ionized traps [24]. This effect was excluded to obtain the D_t (red dot), which accounts for the contributions from interface state density and the hole trap in the bulk [8, 24].

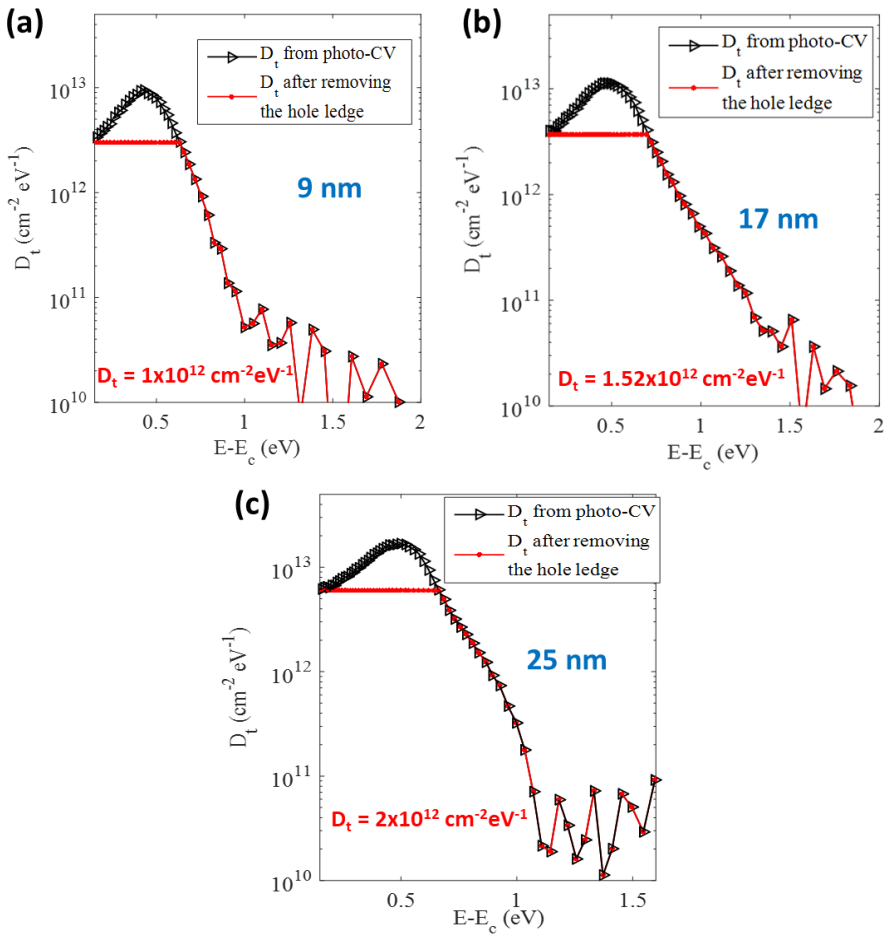


Figure 3.14 The D_t from photo-C-V (black triangle) and the D_t after removing the hole ledge (red dot) of (a) (a) 9 nm, (b) 17 nm and (c) 25 nm AlSiO MOSCAPs

The relationship between total density of traps and interface states is expressed as:

$$D_t = D_{it} + t\frac{dn_{ht}}{2d\psi_s} \tag{3.6}$$

where the $dn_{ht}/d\psi_s$, with unit $cm^{-3}eV^{-1}$, is related to the dielectric hole trap distribution in energy scale. The extracted D_{it} at AlSiO/GaN from **Fig. 3.15** is ~4.44×10^{11} cm^{-2} eV^{-1}. The quantified interface state density here can play a role to study the DC-RF dispersion behavior and the bulk hole traps concentration is useful to understand the performance of p-type devices. Overall, the results and methodology above can provide more insights into understanding and improving dielectric in terms of interface states and bulk hole traps.

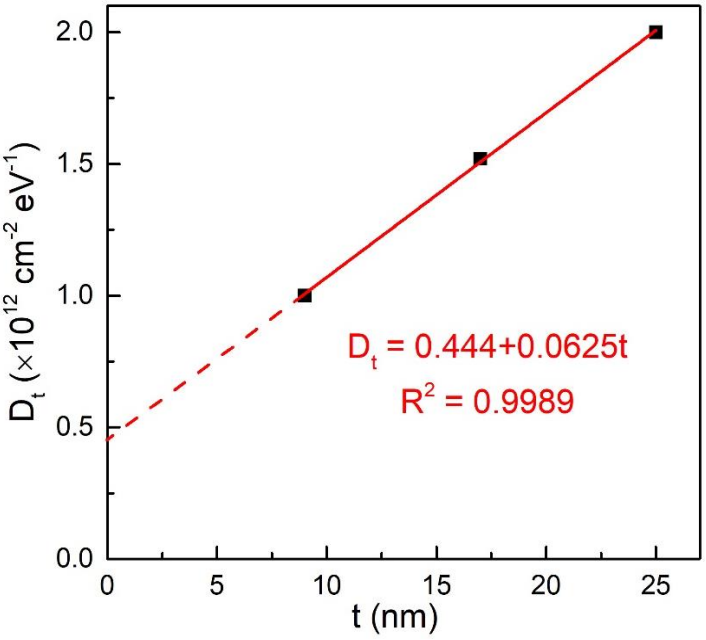


Figure 3.15 The D_{it} extraction from D_t vs thickness based on Eq. 3.6.

3.5 UV-assisted C-V Methodology for β-Ga_2O_3 System

The UV-assisted C-V methodology in this chapter can be further expanded into other wide bandgap semiconductor systems with positive valance band offset. Our collaboration

with Zhe (Ashley) Jian and Prof. Elaheh Ahmadi from University of Michigan, explored the application into Al_2O_3 and AlSiO on β-Ga_2O_3 with a bandgap of 4.9 eV [26, 27] to investigate their bulk and interface properties. The major difference in the experimental settings would be the UV illumination source with shorter wavelength to generate electron-hole pairs in β-Ga_2O_3, which was called *deep* UV-assisted C-V methods.

For Al_2O_3 on β-Ga_2O_3 study, the Al_2O_3 was grown by atomic layer deposition (ALD) and the effects of ALD temperature and post-deposition annealing were studied. ALD at high temperatures and PDA in O_2 at 500 °C can improve the breakdown voltage and reduce hysteresis. Through the analysis on the bulk traps and interface state density developed above, the interface state density and bulk trap density were extracted to be 1.34×10^{12} cm^{-2} eV^{-1} and 2.98×10^{18} cm^{-3} eV^{-1}, respectively.

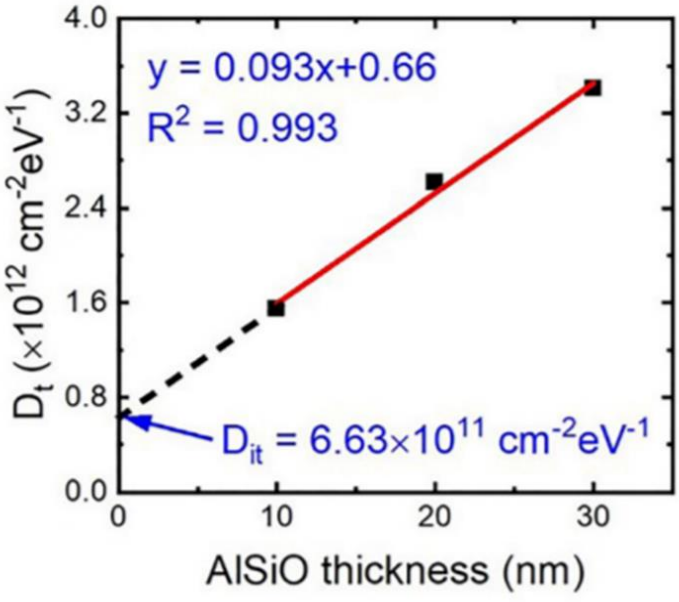


Figure 3.16 The linear fit of the average trap density as a function of AlSiO thickness in AlSiO/β-Ga_2O_3 MOSCAPs [27].

Furthermore, the *ex-situ* MOCVD grown AlSiO on β-Ga_2O_3 was also studied using

the similar methodology. The UV-ozone and wet chemical treatment was used as a surface pre-treatment before the MOCVD growth on β-Ga_2O_3 and was found to help reduce the near-interface traps. As shown in **Fig. 3.16**, the average interface state density and bulk trap density were 6.63×10^{11} cm^{-2} eV^{-1} and 4.65×10^{17} cm^{-3} eV^{-1}. Compared with the ALD Al_2O_3, the AlSiO on β-Ga_2O_3 had better performance with half of the interface trap density in Al_2O_3/β-Ga_2O_3. The bulk trap density of the AlSiO grown on β-Ga_2O_3 is around one sixth of that in Al_2O_3/β-Ga_2O_3. These excellent results indicate the high quality of the MOCVD ex-situ grown AlSiO on β-Ga_2O_3 and its promising applications in future β-Ga_2O_3 related research. Moreover, the successful application into β-Ga_2O_3 of the developed UV-assisted C-V methodology further reveals the possible universality of the methodology, which can be expanded into other WBG system, such as AlGaN and diamond materials systems.

3.6 Summary

In summary, we have developed a systematic and quantitative analysis to understand the interfacial and bulk properties of AlSiO on N-polar GaN. Through a thickness series of AlSiO metal-oxide-semiconductor capacitors (MOSCAPs) and capacitance-voltage (C-V) methods, the fixed charges, electron slow and electron fast trap densities located near the interface were extracted to be -1.5×10^{12} cm^{-2}, 3.7×10^{11} cm^{-2} and 1.9×10^{11} cm^{-2}, respectively. The built-in electric field in AlSiO was less than 0.1 MV/cm when the AlSiO layer was more than 9 nm thick. Using UV assisted C-V methods, an average interface state density of ~4.44×10^{11} cm^{-2} eV^{-1} and a hole trap concentration in bulk AlSiO of ~8.4×10^{18} cm^{-3} is determined. The analysis can serve as a methodology to study the properties of dielectrics on WBG

semiconductors and to optimize MOS-based WBG semiconductor device performance.

References

1. S. H. Chan, M. Tahhan, X. Liu, D. Bisi, C. Gupta, O. Koksaldi, H. Li, T. Mates, S. P. DenBaars, and S. Keller, "Metalorganic chemical vapor deposition and characterization of (Al,Si)O dielectrics for GaN-based devices," *Japanese Journal of Applied Physics*, vol. 55, p. 021501, 2016.
2. S. Chan, "First developments of AlSiO gate dielectrics by MOCVD: A pathway to efficient GaN electronics," *Ph.D. dissertation*, University of California, Santa Barbara), 2018.
3. Z. Yatabe, J. T. Asubar, and T. Hashizume, "Insulated gate and surface passivation structures for GaN-based power transistors," *J. Phys. Appl. Phys.,* vol. 49, no. 39, p. 393001, 2016.
4. T. Cook, C. Fulton, W. Mecouch, R. Davis, G. Lucovsky, and R. Nemanich, "Band offset measurements of the Si_3N_4/GaN (0001) interface," *J. Appl. Phys.,* 94, 3949, 2003.
5. K. Ito, D. Kikuta, T. Narita, K. Kataoka, N. Isomura, K. Kitazumi, and T. Mori, "Band offset of Al1−xSixOy mixed oxide on GaN evaluated by hard X-ray photoelectron spectroscopy," *Jpn. J. Appl. Phys.,* vol. 56, no. 4S, p. 04CG07, Mar. 2017.
6. D. Kikuta, K. Itoh, T. Narita, and T. Mori, "Al2O3/SiO2 nanolaminate for a gate oxide in a GaN-based MOS device," *J. Vac. Sci. Technol. Vac. Surf. Films*, vol. 35, no. 1, p. 01B122, Dec. 2016.
7. C. Gupta, S. H. Chan, A. Agarwal, N. Hatui, S. Keller and U. K. Mishra, "First Demonstration of AlSiO as Gate Dielectric in GaN FETs; Applied to a High Performance OG-FET," in *IEEE Electron Device Letters*, vol. 38, no. 11, pp. 1575-

1578, Nov. 2017.

8. I. Sayed, B. Bonef, W. Liu, S. Chan, J. Georgieva, J. S. Speck, S. Keller, and U. K. Mishra, “Electrical properties and interface abruptness of AlSiO gate dielectric grown on (000-1) N-polar and (0001) Ga-polar GaN,” *Applied Physics Letters*, vol. 115, p. 172104, 2019.
9. I. Sayed, W. Liu, S. Chan, C. Gupta, M. Guidry, H. Li, S. Keller, and U. K. Mishra, “Net negative fixed interface charge for Si_3N_4 and SiO_2 grown in-situ on 000-1 N-polar GaN,” *Applied Physics Letters*, vol. 115, p. 011928, 2019.
10. W. Liu, I. Sayed, C. Gupta, H. Li, S. Keller, and U. Mishra, “An improved methodology for extracting interface state density at Si_3N_4/GaN,” *Applied Physics Letters*, vol. 116, p. 022104, 2020.
11. S. Chowdhury, “Aluminum Gallium nitride / Gallium nitride CAVETs for high power switching application,” *Ph.D. dissertation*, University of California, Santa Barbara, 2010.
12. D. Ji, C. Gupta, A. Agarwal, S. H. Chan, C. Lund, W. Li, S. Keller, U.K. Mishra and S. Chowdhury, “Large-Area In-Situ Oxide, GaN Interlayer-Based Vertical Trench MOSFET (OG-FET),” *IEEE Electron Device Lett.,* vol. 39, no. 5, pp. 711–714, 2018.
13. A. Hiraiwa, S. Okubo, K. Horikawa, and H. Kawarada, “Advanced photo-assisted capacitance-voltage characterization of insulator/wide bandgap semiconductor interface using super-bandgap illumination,” *Journal of Applied Physics*, vol. 125, p. 175704, 2019.
14. E. Ber, B. Osman, and D. Ritter, “Measurement of the variable surface charge concentration in gallium nitride and implications on device modeling and physics,”

IEEE Transactions on Electron Devices, vol. 66, pp. 2100-2105, 2019.

15. F. Heiman and G. Warfield, "The effect of oxide traps on the MOS capacitance," *IEEE Transactions on Electron Devices*, vol. 12, pp. 167-178, 1965
16. X. Liu, J. Kim, R. Yeluri, S. Lal, H. Li, J. Lu, S. Keller, B. Mazumder, J. Speck, and U. Mishra, "Fixed charge and trap states of in situ Al2O3 on Ga-face GaN metal-oxide-semiconductor capacitors grown by metalorganic chemical vapor deposition," *Journal of Applied Physics*, vol. 114, p. 164507, 2013.
17. D. K. Schroder, Semiconductor Materials and Device Characterization (*John Wiley & Sons*), 2006.
18. C. Bae, C. Krug, G. Lucovsky, A. Chakraborty, and U. Mishra, "Work-function difference between Al and n-GaN from Al-gated n-GaN/nitride-thin-Ga2O3/SiO2 metal oxide semiconductor structures," *Appl. Phys. Lett.,* 84, 5413, 2004.
19. SM Sze, "Semiconductor devices: physics and technology," *New York: John Wiley & Sons*, 2008.
20. T. Cook, C. Fulton, W. Mechouch, R. Davis, G. Lucovsky, and R. Nemanich, "Band offset measurement of the Si3N4 /GaN(0001) interface," *Journal of Applied Physics*, vol. 94, pp. 3949-3954, 2003.
21. B.L. Swenson, and U.K. Mishra, "Photoassisted high-frequency capacitance-voltage characterization of the Si3N4/GaN interface," *Journal of Applied Physics,* vol. 106, p. 064902, 2009.
22. L. A. Lyon, and J. T. Hupp, "Energetics of semiconductor electrode/solution interfaces: EQCM evidence for charge compensating cation adsoptoin and intercalation during accumulation layer formation in the Titanium Dioxide/Acetronitrile system," *J. Phys.*

Chem., 99, 15718-15720, 1995.

23. J. A. Mundy, Y. Hikita, T. Hidaka, T. Yajima, T. Higuchi, H. Y. Hwang, D. A. Muller, and L. F. Kourkoutis, "Visualizing the interfacial evolution from charge compensation to metallic screening across the manganite metal-insulator transition," *Nature Communications*, 5, 3464, 2014.
24. M. Choi, A. Janotti, and C. G. Van de Walle, "Native point defects and dangling bonds in α-Al2O3," *Journal of Applied Physics*, vol. 113, p. 044501, 2013.
25. Z. Jian, S. Mohanty, E. Ahmadi, "Deep UV-assisted capacitance-voltage characterization of post-deposition annealed Al2O3/β-Ga_2O_3 (001) MOSCAPs," *Appl. Phys. Lett.* 116, 242105, 2020.
26. Z. Jian, I. Sayed, W. Liu, S. Mohanty, E. Ahmadi, "Characterization of MOCVD-grown AlSiO gate dielectric on β-Ga_2O_3 (001)," *Appl. Phys. Lett.* 118, 172102, 2021.

Chapter 4. Ru/N-polar GaN Schottky Diode

In this chapter, the Schottky barrier diode using ruthenium (Ru) deposited by atomic layer deposition on N-polar GaN is investigated. The Schottky diodes showed near-ideal thermionic current behavior under forward bias and reverse bias at various temperatures. The barrier height values extracted from both regions agreed well at each temperature and the barrier was extracted to be 0.77 eV at room temperature. The difference between the predicted barrier height (0.6 eV) and the experimental barrier heights (0.77eV) indicated the Schottky barrier height was enhanced by 0.17 eV. The combination of the 0.77 eV barrier and thermionic current characteristic resulted in < 2 $\mu A/cm^2$ reverse current at -5 V, which is a record-low value for N-polar GaN Schottky diodes. As a comparison, the Ru on Ga-polar GaN Schottky barrier diode, which has a barrier height of 1.0 eV, exhibited a ~ two-orders of magnitude higher leakage than Ru on N-polar GaN at -5 V due to other parasitic leakage mechanisms specific to the Ga-polar orientation and process.

4.1 Schottky Structure on N-polar GaN

N-polar GaN based high electron mobility transistors (HEMTs) are very promising for solid-state millimeter wave power amplifiers. The advantages come from the GaN material, and the polarization engineering enabled by the N-polar orientation [1-3]. GaN has superior material properties such as a large bandgap, high charge density, high electron mobility and high electron saturation velocity, which are of great importance. In addition, the N-polar orientation can provide extra benefits in a HEMT structure, such as low ohmic contact resistance [4], strong back barrier [5] and improved scalability [6]. Harnessing these

advantages, Romanczyk et al. [7] reported a record-high 8.84 W/mm power density at 94 GHz from a N-polar GaN deep-recessed HEMT with a SiN gate dielectric.

To further boost the high-frequency and high-power performance in N-polar GaN HEMTs, scaling down the gate length while preserving a good aspect ratio is desirable to achieve both high f_T and f_{max}. In the record high P_{out} MIS-HEMT device, the total distance from gate to channel (the centroid of 2DEG) includes 5nm thick SiN, a 2 nm AlGaN and a 9 nm GaN channel. Assuming a good aspect ratio of 5, the minimum expected scaled gate length would be around 80 nm. The typically used gate dielectric added more distance from gate to the channel and hindered the further scaling down of the gate length. It should be noted that the thickness of GaN channel is hard to reduce further because the mobility of the 2DEG could drop significantly. One way to further scaling down is to remove the gate dielectric and utilize the Schottky-HEMT gate structure. By removing the gate dielectrics, Schottky-HEMTs in N-polar GaN with gate directly above AlGaN can achieve a deeply scaled gate while preserving a good aspect ratio. Without the gate dielectric, the gate length can be scaled down to 55 nm given the same AlGaN/GaN thickness and aspect ratio. One would expect more gain and more efficiency when the L_G scaling down is improved in a similar HEMT device.

Another advantage without using the gate dielectric would be that the possible unreliability in the bulk of gate dielectric could be eliminated. In Chapter 2 and Chapter 3, the analysis provided insights that the dielectric on N-polar GaN (or in general including other semiconductors as well) has bulk traps and interface states. While the interface state also exists at the metal/semiconductor interface in Schottky-HEMT structure, the close contact to the gate electrode makes the charging/discharging process fast, which would follow the gate signal and have only limited effects on the reliability of devices.

However, it has been difficult to obtain a good Schottky barrier on N-polar GaN to reduce the gate leakage in HEMTs. Rajan et al. [5] demonstrated a Ni gated N-polar AlGaN/GaN Schottky HEMT but with a ~4 mA/mm high gate leakage. Hardy et al. [8] also reported a ~3mA/mm gate leakage in a Pt/Au gated N-polar HEMT due to the poor Schottky barrier on N-polar GaN. Other Schottky diodes with various metals on N-polar GaN [9-12] have also shown low barrier height values associated with other parasitic conducting paths (not fully understood), which led to unacceptably high reverse currents to be used in practical HEMTs.

The **Fig. 4.1** below summarized the reported barrier height values on N-polar GaN and some associated reverse currents. Majority of the reported values are less than 0.7 eV except one reported a barrier height of around 0.9 eV using Pt as the Schottky metal. It should be also noted that the barrier heights for nominally same metal could be varying from different groups depending on material quality and surface preparation before metal deposition. In a simple theory, the ideal barrier height of a Schottky barrier can be determined by the metal work function and the electron affinity of the semiconductor. In the case of GaN as the semiconductor, the relationship can be expressed as:

$$\phi_B = \phi_m - \chi(\mathrm{GaN}) \tag{4.1}$$

where ϕ_B is the barrier height, ϕ_m is the metal work function and χ(GaN) is the electron affinity of GaN, which is typical chosen to be 4.1 eV for n^- GaN at 300 K [30]. All the experimental data points are below the line of ideal barrier height.

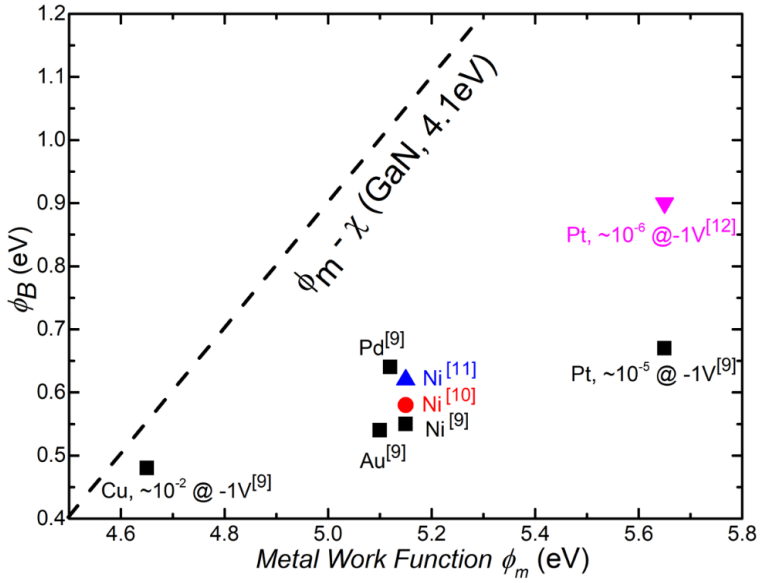


Figure 4.1 The Schottky barrier heights and some reverse currents (with unit A/cm^2) for metals with various work functions on N-polar GaN from the literature.

The deviation from the ideal line can be explained by the interface charge transferring and the formed interface dipoles. As discussed in the dielectric/semiconductor system of Chapter 2, the intrinsic and extrinsic interface states also occur in metal on semiconductor system and could complicate the barrier height behavior. The barrier height would be sensitive to many factors including the material surfaces, processing treatment and metal deposition etc. The barrier height variation for the nominally same metal could be explained by those factors. More discussion on the deviation from ideal line will be presented in part "*Enhanced barrier height*" of this chapter.

4.2 ALD Ru on N-polar GaN

This chapter presents the investigation of ruthenium (Ru) deposited by atomic layer deposition (ALD) on N-polar GaN for use as a Schottky diode with this section detailing the

process of Schottky barrier formation and the structure used. ALD Ru can provide excellent filling in nanoscale T-gate stem trenches with high-aspect ratio while simultaneously offering easy process integration as Ru can be etched by oxygen plasma. The successful use of Ru and demonstrated reliability in dynamic random-access memory (DRAM) makes it a readily available metallurgy in foundries [13]. As will be shown in the following part of the chapter, the ALD Ru on N-polar GaN diode device has a 0.77 eV barrier height at room temperature and thermionic current behavior. The barrier height values at various temperatures extracted from the forward bias region and the reverse bias region agreed well. With the combination of 0.77 eV barrier height and a thermionic current characteristic, the reverse leakage was < 2 μA/cm^2 at -5V, which is a record-low value for N-polar GaN Schottky barrier diodes. Besides, the Ru deposited by ALD can fill the extremely scaled gate in N-polar GaN HEMTs and enable further advances in high-power and high frequency performance. Part of the figures and materials in this chapter are reproduced © 2020 IEEE., with permission, from [**Wenjian Liu**, Islam Sayed, Brian Romanczyk, Nirupam Hatui, Matthew Guidry, William J Mitchell, Stacia Keller, Umesh K Mishra, Ru/N-Polar GaN Schottky Diode with Less Than 2 μA/cm² Reverse Current, *IEEE Electron Device Letters*, 41, 1468-1472(2020).] and [**Wenjian Liu**, Islam Sayed, Brian Romanczyk, Nirupam Hatui, Jana Georgieva, Haoran Li, Stacia Keller, Umesh K Mishra, Near-ideal Ru/N-polar GaN Schottky diode with ultralow reverse leakage, *Device Research Conference (DRC)*, July 2020, doi: 10.1109/DRC50226.2020.9135165.].

Epitaxial structure and device fabrication

The fabrication procedure of the circular Ru/N-polar GaN Schottky diode was shown in **Fig. 4.2**. First, the N-polar GaN epitaxial layers were grown by metal organic chemical vapor deposition (MOCVD) on a c-plane sapphire with a miscut 4 ° towards the a-plane

[14,15]. As shown in **Fig. 4.2 (a)**, the epitaxial structure consisted of an unintentionally doped (UID) GaN buffer layer, an 800 nm n^+ GaN layer, a 600 nm n^- GaN layer and a 5 nm protective SiN cap layer. For comparison, a Ga-polar sample was also grown. The Ga-polar sample had equivalent epi structure as the N-polar one, except a sapphire substrate without a miscut was used (a conventional process). The doping values extracted from capacitance-voltage (C-V) measurements for N-polar and Ga-polar n^- GaN were 2×10^{17} cm^{-3} and 3.7×10^{17} cm^{-3}, respectively. X-ray diffraction (XRD) rocking curves were measured to evaluate the quality of the epitaxial structures since the full-width-half-maximum (FWHM) of symmetrical and asymmetrical scans is proportional to screw and edge dislocations, respectively. The FWHM of (0002) and (20-21) diffraction peaks were 320.4 arcsec and 644.4 arcsec on the N-polar sample and were 300 and 464 arcsec on the Ga-polar sample. These corresponded to extracted dislocation densities of approximately 1-2 $\times$ 10^9 cm^{-2} for both samples, confirming their equivalent and good quality.

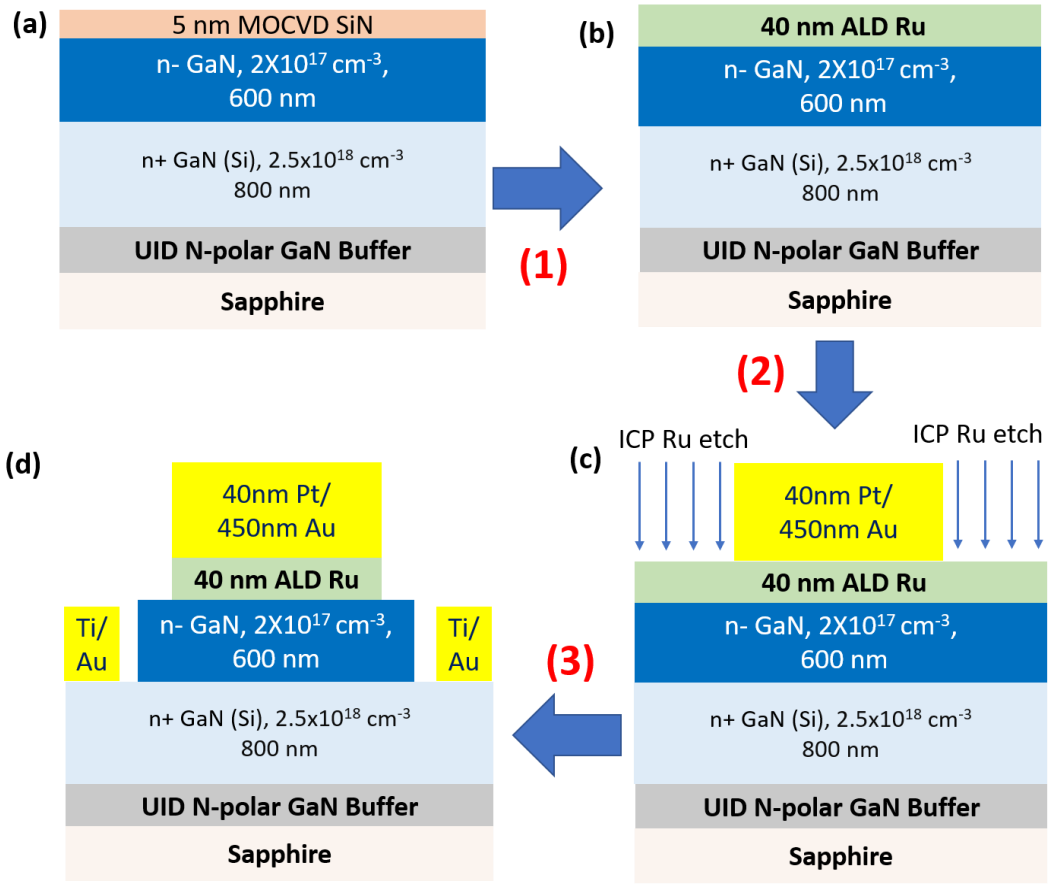


Figure 4.2 The fabrication procedure of Ru/N-polar GaN Schottky diodes: (a) MOCVD-grown N-polar GaN epitaxial structure; (b) 40nm ALD Ru as the Schottky contact metal; (c) the formation of Ru/Pt/Au Schottky gate electrode; (d) final device structure of the circular Schottky diode. Ru/Ga-polar GaN Schottky diodes were processed in the same way.

The N-polar and Ga-polar samples were fabricated together as described in the following. In step (1) of **Fig. 4.2**, the GaN surface was exposed by the removal of the MOCVD SiN using HF: HNO_3 solution. Then a 40 nm thick Ru Schottky contact metal was deposited on the entire sample surface by ALD at 300 °C using Ex03Ru (Hansol Chemical, Korea) and O_2 precursors as shown in **Fig. 4.2** (b). In step (2), anode probe metal Pt (40 nm)/Au (450 nm) with a 100 μm diameter was deposited using electron beam evaporation and a lift-off

technique. In **Fig. 4.2** (c), the excess Ru was etched using a O_2/Cl_2-based inductively coupled plasma (ICP) etch using the Pt/Au electrode as a mask to define the anode contact. Finally, step (3) included mesa etching by reactive-ion etching (RIE) and the deposition of non-annealed Ti/Au (25 nm/200 nm) ohmic contacts to the n+ GaN by e-beam evaporation to complete the circular Ru/N-polar GaN Schottky diode structure in **Fig. 4.2** (d). There was a 30 μm lateral spacing between the edge of the etched mesa and the anode metal.

4.3 Barrier Height

4.3.1 Forward bias region

Temperature-dependent DC current-voltage (I-V) curves are measured from 298 K (room temperature) to 448 K with 25 K per step. Both the forward-bias region (**Fig. 4.3**) and the reverse-bias region (**Fig. 4.4**) were used to extract the barrier heights at each temperature. The I-V relation of a Schottky barrier diode can be expressed as [9]:

$$I = I_S(e^{\frac{qV}{nkT}} - 1) \tag{4.1}$$

$$ln\ (\ I_S/T^2)\ = ln(A^*)\ - q\phi_B/kT \tag{4.2}$$

where I_S is the saturation current density, n is the ideality factor, q is the electron charge, k is the Boltzmann constant, T is the temperature, ϕ_B is the Schottky barrier height, and A^* is the Richardson's constant. A^* varies from 5 to 26.4 A cm^{-2} K^{-2} for GaN [9-11,16]. A typical value of 24 A cm^{-2} K^{-2} was used in this analysis. Under a forward bias region with $V > 3kT/q$, the I-V can be simplified as:

$$ln\ (I) = ln(I_S) + qV/nkT \tag{4.3}$$

Eq. 4.3 was used in the region from 0.15 V (to maintain $V > 3kT/q$) to 0.3 V (to avoid the influence from the contact resistance). From the linear fit of ln(I) versus V shown in **Fig. 4.3**, the saturation current density from the forward bias region ($I_{S,F}$) and the associated ideality factor (n) were obtained at various temperatures. Then the barrier height values ($\phi_{B,F}$) were calculated using **Eq. 4.2** and plotted in **Fig. 4.5** along with the ideality factor n.

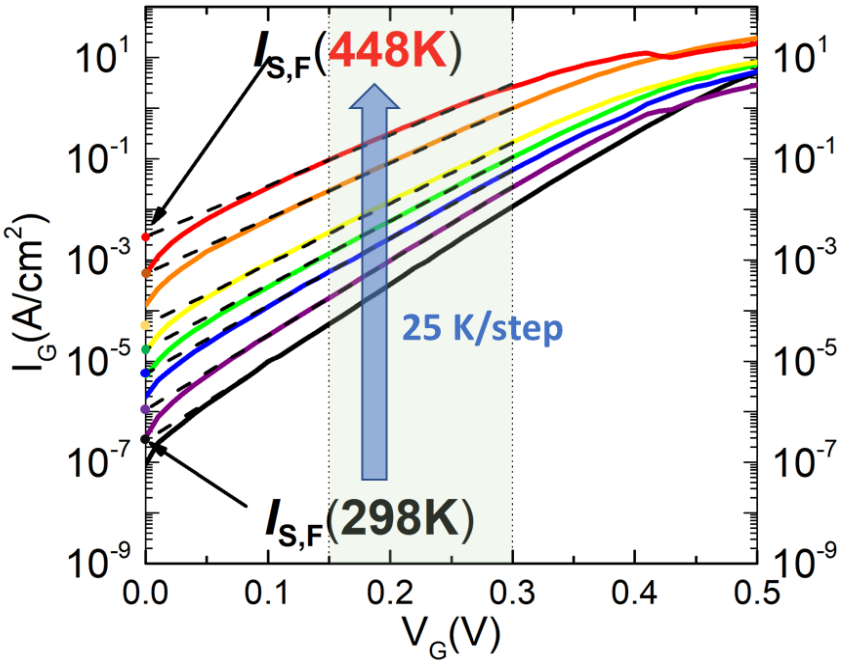


Figure 4.3 Temperature dependent DC *I-V* curves (solid lines) of the N-polar Schottky diode for temperatures from 298 K to 448 K with 25 K per step under forward bias. At each temperature, the saturation current density values were obtained by linearly extrapolating to zero bias in the log-scale (dashed lines). The voltage (V_G) was applied on the Ru/Pt/Au electrode and the shaded regions represent the voltage region where the fitting was conducted.

4.3.2 Reverse bias region

In the reverse bias region from -1 V to -5 V (< -3 kT/q range), shown as the shaded region in **Fig. 4.4**, the slow increase of the current plotted on a log-scale with the applied reverse bias was consistent with the image charge induced barrier lowering effect [17, 18]:

$$ln\,(I) = ln(I_S) + q\Delta\phi_B(\mathrm{V})/kT \tag{4.4}$$

where $\Delta\phi_B(V)$ is the imaging charge induce barrier lowering effect and treated as linear-dependent on V here. Without any other parameters, ln(I) from -1 V to -5 V was extrapolated to zero bias to obtain the saturation current in the reverse bias region ($I_{S,R}$) as **Fig 4.4** shows.

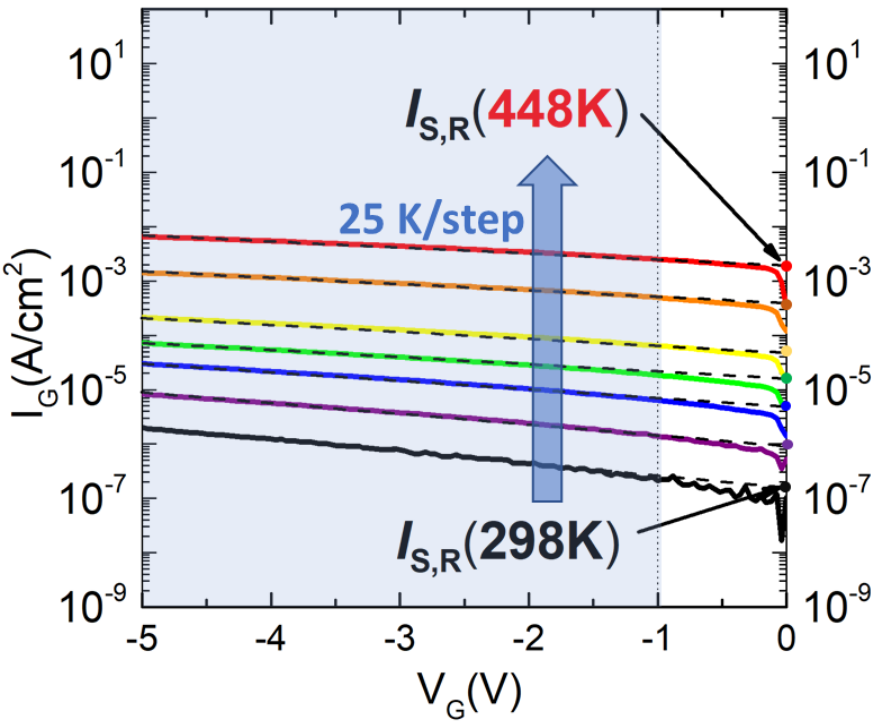


Figure 4.4 Temperature dependent DC *I-V* curves (solid lines) of the N-polar Schottky diode for temperatures from 298 K to 448 K with 25 K per step under reverse bias. The extraction process is the same as the forward bias region and the shaded regions represent the voltage region where the fitting was conducted.

From $I_{S,R}$ and **Eq. 4.2**, the barrier height value ($\phi_{B,R}$) was calculated as shown in **Fig. 4.5**. The consistent barrier heights from both forward bias region and reverse bias region experimental data in N-polar GaN-based Schottky diodes indicate a near-ideal Schottky diode behavior. The values of ideality factor *n* at different temperatures ranged from 1.06 to 1.10 and indicated a thermionic current behavior in the forward bias region. The barrier height $\phi_{B,R}$ from the reverse saturation current value agreed well with $\phi_{B,F}$ at each temperature, further revealing that the current behavior in the Ru/N-polar GaN Schottky diode was thermionic in nature.

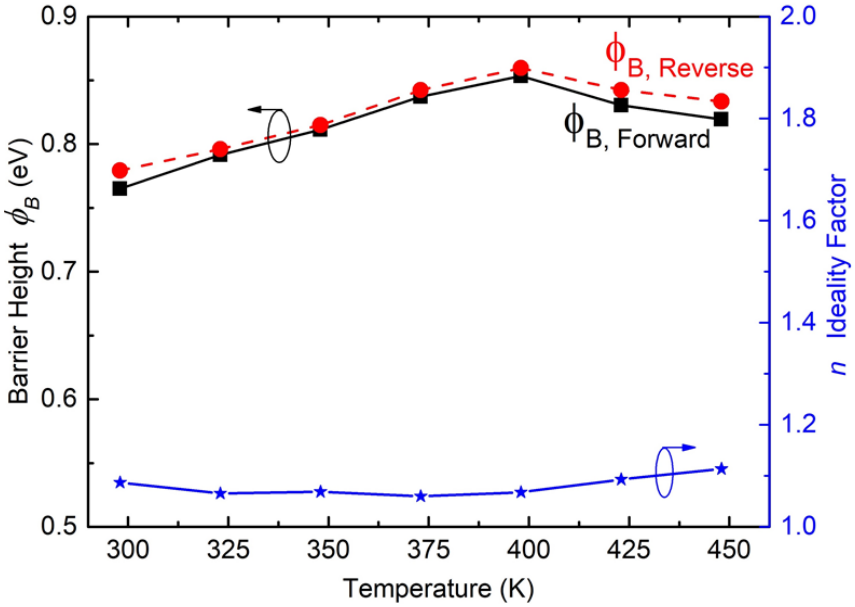


Figure 4.5 Barrier height values extracted from the forward bias region $\phi_{B,F}$ and the reverse bias region $\phi_{B,R}$ (left y-axis); ideality factor n (right y-axis) extracted at various temperatures from 298K to 448K for the Ru on N-polar GaN Schottky diodes.

As shown in **Fig. 4.5**, the barrier height of ~0.77 eV at 298 K, increased to ~0.85 eV at 398 K and then dropped to ~0.82 eV a 448K. The positive temperature coefficient of the barrier height from 298 K to 398 K can be explained by the interface barrier inhomogeneity

in GaN related Schottky diodes as studied and reported by several researchers [19-21]. Using the methodology described in ref [22, 23], our data can be explained by a standard deviation value of 128 mV from an assumed barrier height Gaussian distribution. The negative temperature coefficient is not common in GaN Schottky related publications. Yildirim et al. [22] observed a negative dependence on temperature in C-V data and attributed it to the bandgap shrinkage at high temperature. Lu et al. [24] obtained a bandgap temperature coefficient of -1.08 meV/K for GaN. If the Schottky barrier height decrease was attributed to bandgap shrinkage, our negative temperature coefficient was estimated to be ~ -0.6 meV/K for conduction band edge downward and stays within a reasonable range.

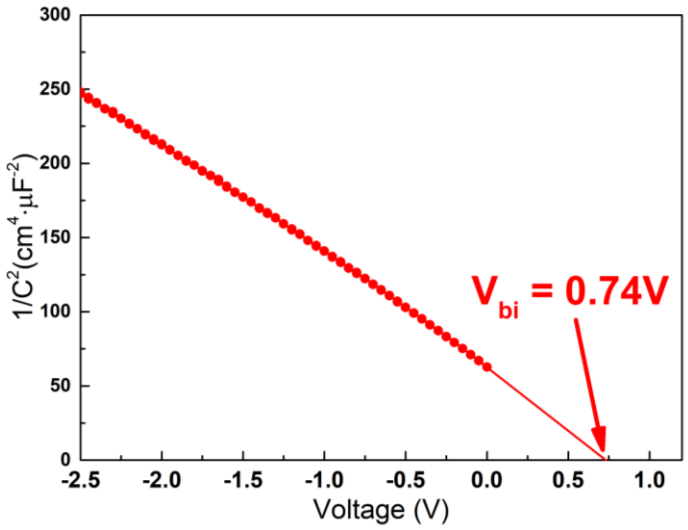


Figure 4.6 The room temperature $1/C^2$ versus V with extracted doping of 2×10^{17} cm^{-3} and V_{bi} of 0.74 eV, from which the calculated barrier height value is in close agreement with value from I-V extraction.

C-V measurements were also performed to extract the barrier height at room temperature and the $1/C^2$ versus V is shown in **Fig. 4.6**. From the $1/C^2$-voltage relationship, built-in voltage V_{bi} of 0.74 eV was extracted and the barrier height of 0.81 eV was calculated

[9]. The extracted barrier height from C-V (0.81 eV) was in close agreement with that extracted from I-V measurement (0.77 eV).

4.3.3 Enhanced barrier height

In an ideal thermionic current conducting behavior, the current has an exponential dependence on the barrier height as shown in **Eq. 4.1** and **Eq. 4.2**. To obtain a low reverse current, high barrier height plays a critical role to reduce the reverse current in an exponential way. In prior N-polar GaN Schottky barrier studies, many of the efforts were put on these metals with relatively high work function metal, including Au (work function 5.1eV), Pd (work function 5.13eV), Ni (work function 5.15eV) and Pt (work function 5.65eV). The reason can be simply described in **Eq. 4.1**. The equation assumes that the barrier formed is purely caused by the energy levels of bulk properties of metals and the semiconductor.

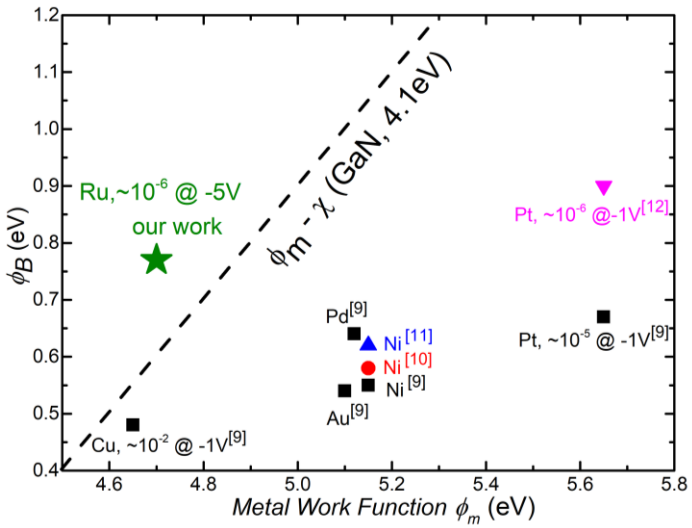


Figure 4.7 Adding the ALD Ru/N-polar GaN Schottky data point into Fig. 4.1

However, in fact there are multiple sources of interfacial interactions between the metal and semiconductor which can cause the transfer of charges, form interfacial dipoles,

form interfacial layers which can reduce/enhance the barrier height [17, 28]. **Fig. 4.7** summarizes the data points of Schottky barrier height on N-polar GaN in the literature from **Fig. 4.1** and includes the Ru on N-polar GaN Schottky barrier data point. The dotted line represents the ideal barrier height behavior without considering the interfacial charges. Unfortunately, the points from other studies have lower barriers than the equation predicted as these data points are below the ideal dotted line. The reduced barrier heights do not favor the low reverse currents desired in Schottky-devices. The variations in the same metal can be caused by non-idealities during the device fabrication, semiconductor growth or other surface-related processes as discussed in the interface states part of chapter 2.

The Ru on N-polar GaN in our study is above the dotted line and has an enhanced barrier behavior. The difference between the predicted and the experimental barrier heights are 0.17 eV based on the Ru work function of 4.7eV. In an exponentially dependent behavior, the extra 0.17 eV can reduce the saturation current by a factor of 746 ($e^{0.17eV/0.0257eV}$) at room temperature with kT of 0.0257eV, which is roughly a 3-orders of magnitude reduction. With attempts to understand the physics of the enhanced barrier height between Ru and N-polar GaN, a simple model considering the interface charge (or interface dipole) will be helpful and the schematic diagrams depicting the hypothesis are shown in **Fig. 4.8** below.

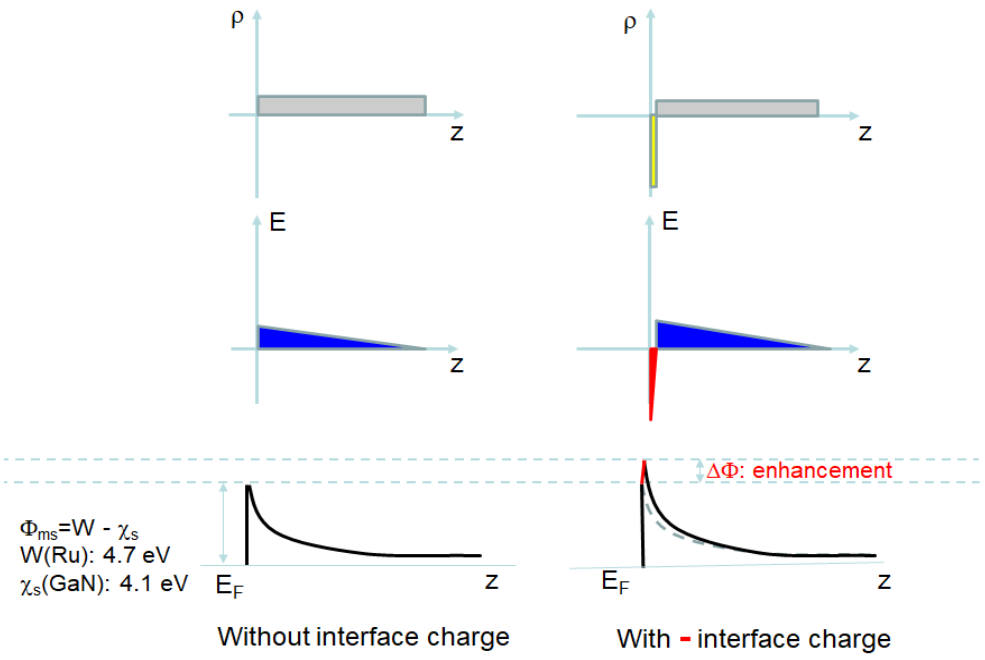


Figure 4.8 The schematics of charge, electric field and band diagram to show the effect of interface charge on the barrier height.

Starting from the charge profile ρ, the electric field and energy band diagram can be drawn to represent the effect of the interface charge. The charge neutrality is maintained with the charge in the metal which is not shown in the diagram. Without the interface charge, the barrier height would be the same as **Eq. 4.1** predicted. Assuming there is some uniformly distributed negative interface charge existing at the semiconductor surface with a charge density of ρ_0 and depth of δ, the effective barrier height will be increased by the amount of $\Delta\Phi$. Assuming the doping concentration in the n- GaN layer is N_D and $|\rho_0| >> qN_D$, the $\Delta\Phi$ can be approximately given as follows [29]:

$$\Delta\Phi = -\rho_0\delta^2/(2\varepsilon_r) \tag{4.5}$$

where the ε_r is the permittivity of GaN. When the 0.17 V enhanced barrier height is taken into the **Eq. 4.5**, the charge density ρ_0 and depth of δ can be estimated. For instance, a δ of 1 nm would indicate the ρ_0 of -1.67 × 10^{20} cm^{-3} and 0.5 nm would give -6.69 × 10^{20} cm^{-3}. The total amount of charge $/\rho_0 * \delta /$ in the region is around 1.67 × 10^{13} cm^{-2}, which is around the same order of the polarization charge at the GaN surface. As a part of the interface between semiconductor and metal, the physical origin of the negative interface charge is hard to examine in a rigorous way and its exploration by the means of XPS will be presented in the "***XPS analysis***" of this Chapter.

4.4 ALD Ru on Ga-polar GaN and N-polar GaN

4.4.1 Reverse leakage conduction

As a companion sample, the ALD Ru on Ga-polar GaN Schottky diodes were processed along with the N-polar GaN sample. The comparison of the Schottky *I-V* characteristics of Ru on Ga-polar and N-polar GaN at room temperature is shown in **Fig. 4.9**.

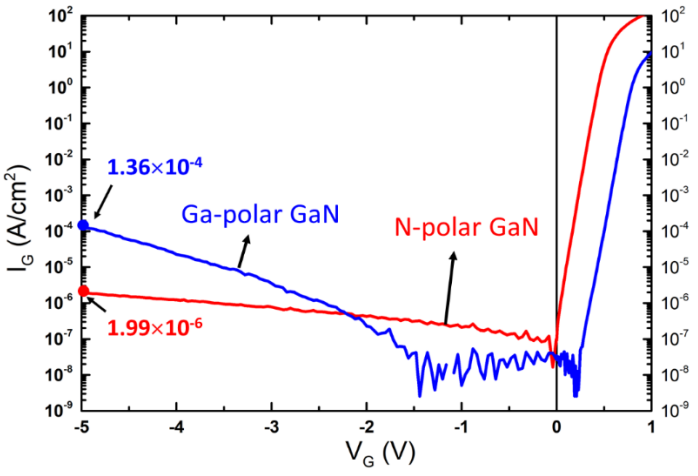


Figure 4.9 *I-V* curves of Ru/N-polar GaN (red) and Ru/Ga-polar GaN (blue) Schottky diodes at room temperature.

For the Ga-polar device, the barrier height and ideality factor extracted from the 0.35~0.5 V forward bias region were 1.0 eV and 1.26, respectively. It is noted that the barrier height of Ru on Ga-polar GaN is around 0.23 eV larger than that on N-polar GaN. Suemitsu et al. [10] also observed similar barrier height difference of 0.21 eV in Ni on Ga-polar and N-polar GaN. An effective Schottky barrier height model based on the different polarization-induced surface charges with finite thickness was proposed to explain the relatively larger barrier height in Ga-polar case by Suemitsu et al [10]. The current density from -1.5 V to 0.26 V was below the detectable limits of the instrument due to the 1.0 eV barrier height value. However, unlike the ideal thermionic current characteristic observed for the N-polar GaN diodes across the whole applied bias range, the reverse leakage of Ga-polar diode started off lower due to the higher barrier height but was then overwhelmed by other leakage mechanisms beyond -2.3 V. At -5 V, the Ga-polar diodes had a reverse current of 1.36×10^{-4} A/cm^2, while the N-polar case with a 1.99×10^{-6} A/cm^2.

The almost two-orders of magnitude higher leakage in the Ga-polar case suggests that its dominant conducting mechanism under reverse bias was not thermionic current. Other parasitic leakage mechanisms, such as trap-assisted tunneling, field-emission tunneling, and hopping conduction through dislocations may contribute to the high reverse leakage [25-27]. The band diagrams presented in **Fig. 4.10** schematically depicted the reverse current conduction mechanisms and illustrated our hypothesis that other parasitic conduction in N-polar GaN may be suppressed.

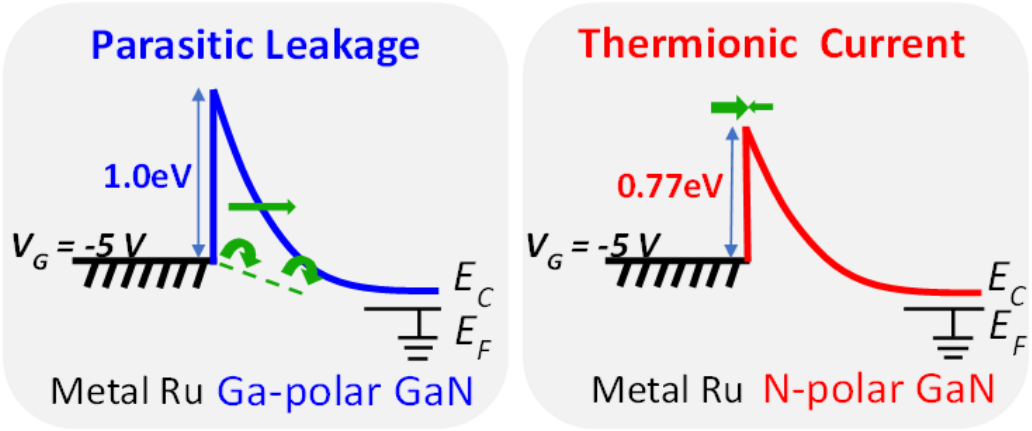


Figure 4.10 The band diagrams reflect the reverse current behavior, where the green arrows represent the dominant conducting mechanisms. (Left one for Ga-polar, right one for N-polar)

The comparison between Ru on N-polar and Ga-polar GaN Schottky diodes indicates that both the barrier height value and the reverse current conduction mechanism are important to achieve low reverse leakage. Prior to this study, the lowest reverse current reported in N-polar GaN Schottky diodes was 10^{-6} A/cm^2 at -1V with a 0.9 eV barrier height for a non-ideal Pt/N-polar GaN Schottky diode [12]. In our study, because of the ideal thermionic current characteristic, the Ru/N-polar GaN Schottky diode with a lower 0.77 eV barrier achieved 2×10^{-7} A/cm^2 at -1V, which is a record-low reverse current among N-polar GaN Schottky diodes.

4.4.2 High reverse bias voltage

The high break-down voltage and stability at high electric fields can enable high voltage swing at the drain bias and provide more output power density and higher efficiency when applied into transistors. To study the break-down voltages in our experiments, we applied up to -60V reverse bias on Ru/N-polar GaN. As shown in **Fig. 4.11**, the reverse I-V

curve remains well behaved and there were no sudden instabilities before the current hit the compliance, which represents the robustness of the Ru on N-polar GaN Schottky diode. To estimate the tolerance of high electric field in the Ru/N-polar GaN Schottky diode, a conservative -50 V is taken as the break-down voltage to calculate the maximum electric field in the Schottky junction. The maximum electric field at the interface is around 2 MV/cm.

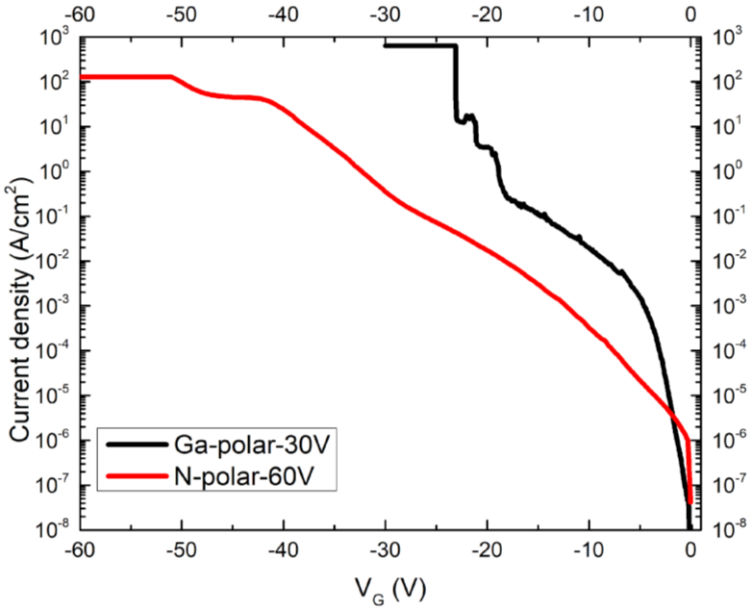


Figure 4.11 The break-down measurement of Ru on N-polar (red) and Ga-polar (black) GaN

As a comparison, for the Ru on Ga-polar GaN, the break-down happened around -25V. Even though the electrical behavior at extreme electric fields is hard to analyze due to the activation of alternate current paths and ionization of traps (loosely referred to as leakage paths), the difference between Ga-polar and N-polar is clear at the low and high electric field. At the voltage below 3 V, the dominant reverse current in Ga-polar GaN case and N-polar GaN is the thermionic current. After the transition around 3V, the parasitic leakage behavior in Ga-polar started to become the major part and surpass the thermionic current in N-polar. The transition in reverse current indicates earlier activation of leakage paths in Ga-polar case,

To some extent, the break-down voltage test conducted in the study can only illustrate the advantage of Ru/N-polar GaN over its counterpart Ru/Ga-polar GaN, while other metals on Ga-polar GaN may demonstrate stable Schottky diodes.

4.5 XPS Analysis

The enhanced barrier height at the Ru/N-polar GaN interface is helpful to reduce the reverse current exponentially. The negative interface charge can be invoked to explain the enhanced barrier height from the perspective of charge transferring. However, the structural and physical reasons may also be a reason and hence the chemical bonding or elements analysis, is interesting to investigate. Even though some analysis methods can be used to study the interface, fully understanding the physics of a complicated interaction at the interface is not easy by any means. Here, the depth profile of the XPS study is used to track the O, Ru, Ga elements and their bonding energy levels.

As determined by ellipsometry, around 43 nm Ru film was deposited at the N-polar GaN surface by the ALD method. The Ru/N-polar GaN piece sample for XPS analysis was co-deposited with the Schottky device sample. For XPS analysis, the sample was loaded into the high vacuum XPS analysis chamber and etched by Ar ion cycle by cycle to obtain the depth profile. The etch time per cycle was 10 sec and the etch rate of Ru was roughly 2.87 nm/ 10sec. A total 230 sec etching time was completed until the sample was well etched into the GaN body. It is worth noting that the detection of the X-ray excited electrons can be generated from the materials down to the 10 nm below the surface. The obtained XPS spectrum is not the exact surface but over a range of around 10 nm from the surface.

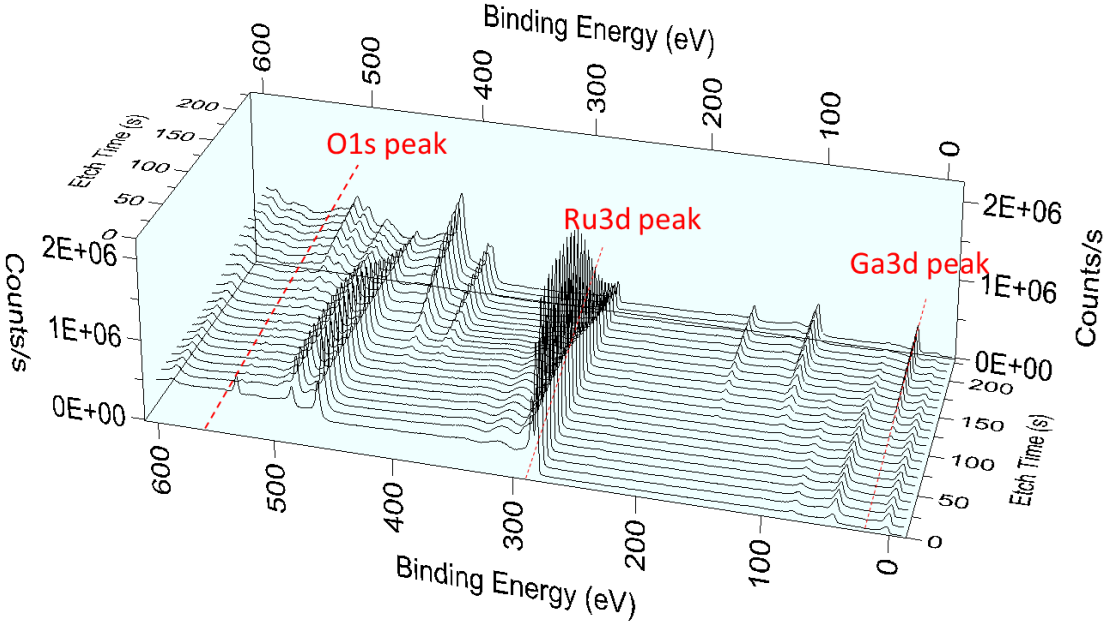


Figure 4.12 The XPS spectrums of each cycle during the Ar etching with notations on O1s, Ru3d and Ga3d peaks.

The etch profile with binding energy spanning from 0 eV to 600 eV was shown in **Fig. 4.12**. The O1s peak (530 eV), Ru3d peak (284.8 eV) and Ga3d peak (20 eV) annotated in **Fig. 4.12** was used to extract their atomic ratios. Other peaks are from different atomic energy levels or Auger peaks. The depth profile of atomic ratio of O, Ru and Ga is shown in **Fig. 4.13**. The first XPS spectrum before Ar etching indicated around 50% oxygen atomic weight, which means the oxidation of Ru at the surface and some formation of RuO_2. After the first 10 sec Ar+ etch, the oxygen ratio dropped significantly and stayed in the low level around 5 % constantly. At the interface defined by the intersection of the atomic ratio of Ru and Ga, the oxygen level is low, and the Ru peak is stable without an obvious peak shift.

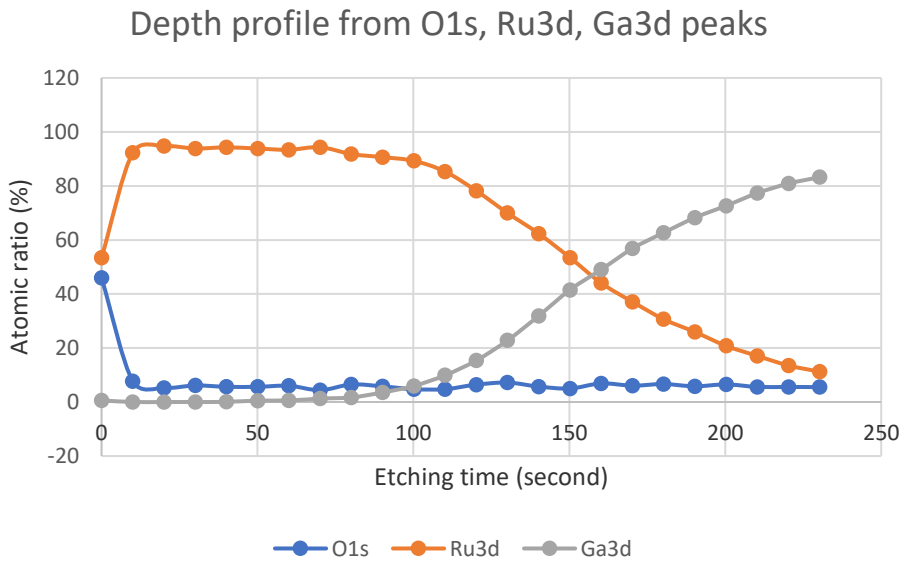


Figure 4.13 The depth profile of O, Ru and Ga atomic ratio from the analysis on Fig. 4.12

The consistency of low oxygen concentration and stable Ru peak seems to suggest the chemical bonding at the interface is normal within the accuracy of the XPS tool used in the study. There is no obvious oxygen involvement or other bonding with Ru at the Ru/N-polar GaN interface. The negative interface charge at the Ru/N-polar GaN interface seems not caused by the oxygen or other bonding with Ru at the levels detectable by XPS. The reasons for enhanced barrier height would require other analysis methods or first-principle tools to provide more insights.

4.6 ALD Pt on N-polar GaN

In an ultra-scaled deep recess structure, the ALD deposition methods will be beneficial to fill the deep trench and provide low gate resistance. Among the available ALD conductive materials in the nanofab facilities at UCSB, the Ru and Pt are the two possible options to study. In the case of ALD Pt, on one hand, there are two possible disadvantages. One is the higher

resistivity compared with Ru (Ru: 71 nΩ m, at 0 °C; Pt： 96 nΩ m, at 0 °C; ref [31]) and the other is the difficulty to remove the excess ALD Pt. Due to the chemical inertness, etching of Pt usually involves more ion bombardment, which may introduce undesired processing related issues. On the other hand, Pt has a larger work function than Ru, which seems to be an advantage. Based on the idealized calculation of barrier height, Pt was expected to provide higher barrier height compared to Ru.

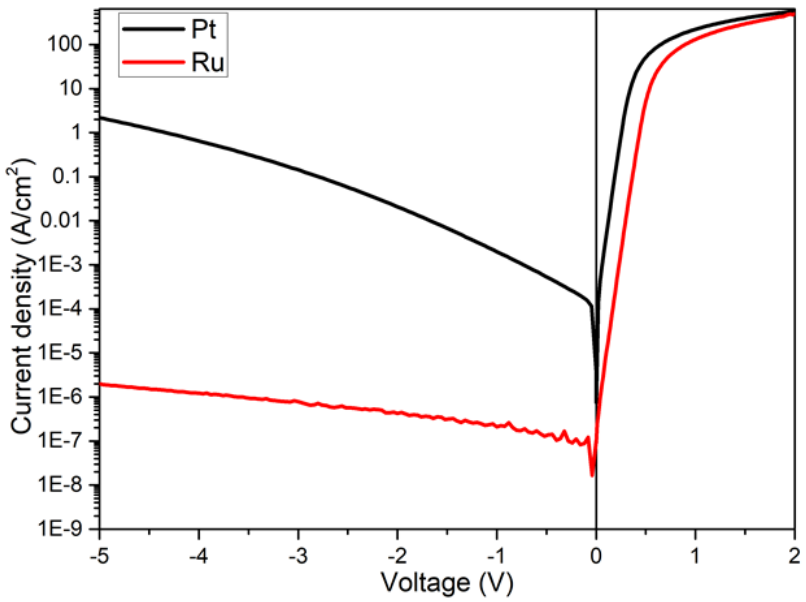


Figure 4.14 The comparison between ALD Pt/N-polar GaN and ALD Ru/N-polar GaN

The ALD Pt on N-polar GaN was also studied and co-processed as the ALD Ru on N-polar GaN. One difference is the deposition and etching of Pt. The deposition of ALD Pt is using *TMCpPt* and O_3 precursors. Ion milling was used to etch away the excess Pt after the gate hard mask. Other processing was the same as the ALD Ru on N-polar GaN study. From the IV curve in **Fig. 4.14**, the Pt on N-polar GaN diode generally has higher current for both forward bias and reverse bias regions. The barrier height extracted from the forward bias

region was around 0.6 eV, which is close to the previous reported value [9]. The 0.6 eV is around 1 eV lower than 1.6 eV calculated from ideal work function-electron affinity formula. Similar as the discussion on Ru/N-polar GaN enhanced barrier, the reduced barrier height of Pt/N-polar GaN can be also attributed to the interface charge/dipoles.

4.7 Summary

In this Chapter, Schottky diodes composed of Ru deposited by ALD on N-polar GaN were investigated. The Schottky diodes exhibited a ~0.77 eV barrier height value at room temperature and showed ideal thermionic current behavior in both forward and reverse bias regions. The reverse current was less than 2 $\mu A/cm^2$ at -5V, which is the best among various metals on N-polar GaN Schottky diodes reported. The Ru/N-polar GaN Schottky barrier diode developed here is an initial step to achieve Schottky-HEMTs with a highly scaled gate length. Along with more development, it can potentially enable further advances in N-polar GaN-based solid state millimeter wave power amplifiers and circuits.

References

1. M. Wong, S. Keller, Nidhi, S. Dasgupta, D. J. Denninghoff, S. Kolluri, D. F. Brown, J. Lu, N. A. Fichtenbaum, E. Ahmadi, U. Singisetti, A. Chini, S. Rajan, S. P. Denbaars, J. S. Speck, and U. K. Mishra, "N-polar GaN epitaxy and high electron mobility transistors," *Semicond. Sci. Technol.,* vol. 28, p. 074009, Jun. 2013.

2. S. Wienecke, B. Romanczyk, M. Guidry, H. Li, E. Ahmadi, K. Hestroffer, X. Zheng, S. Keller, and U. K. Mishra, "N-polar GaN cap MISHEMT with record power density exceeding 6.5 W/mm at 94 GHz," *IEEE Electron Device Lett.,* vol. 38, no. 3, pp. 359-362, Mar. 2017.

3. U. K. Mishra, L. Shen, T. E. Kazior and Y. Wu, "GaN-based RF power devices and amplifiers," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287-305, Feb. 2008.

4. M. H. Wong, Y. Pei, T. Palacios, L. Shen, A. Chakraborty, L. S. McCarthy, S. Keller, S. P. Denbaars, J. S. Speck, and U. K. Mishra, "Low nonalloyed ohmic contact resistance to nitride high electron mobility transistors using N-face growth," *Appl. Phys. Lett.*, vol. 91, p. 232103, Dec. 2007.

5. S. Rajan, A. Chini, M. H. Wong, J. S. Speck, and U. K. Mishra, "N-polar GaN/AlGaN/GaN high electron mobility transistors," *J. Appl. Phys.*, vol. 102, p. 044501, Aug. 2007.

6. P. S. Park, D. N. Nath, and S. Rajan, "Quantum capacitance in N-polar GaN/AlGaN/GaN heterostructures," *IEEE Electron Device Lett.,* vol. 33, no. 7, pp. 991-993 Jul. 2012.

7. B. Romanczyk, X. Zheng, M. Guidry, H. Li, N. Hatui, C. Wurm, A. Krishna, E.

Ahmadi, S. Keller, and U. K. Mishra, “W-band power performance of SiN-passivated N-polar GaN deep recess HEMTs,” *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 349-352, Mar. 2020.

8. M. T. Hardy, D. F. Storm, B. P. Downey, D. S. Katzer, D. J. Meyer, T. O. McConkie and D. J. Smith, “Charge control in N-polar InAlN high-electron-mobility transistors grown by plasma-assisted molecular beam epitaxy,” *J. Vac. Sci. Technol. B*, vol. 33, p. 061207, Nov. 2015.

9. B. P. Downey, D. J. Meyer, D. S. Katzer, D. F. Storm, and S. C. Binari, “Electrical characterization of Schottky contacts to N-polar GaN,” *Solid-State Electron.,* vol. 86, pp. 17-21, Aug. 2013.

10. T. Suemitsu, and I. Makabe, “Effective Schottky barrier height model for N-polar and Ga-polar GaN by polarization-induced surface charges with finite thickness,” *Phys. Status. Solidi B*, vol. 257, no. 4, p. 1900528, Dec. 2019.

11. Y. Liu, S. Dogan, H. Morkoc, S. S. Park, and K. Y. Lee, “Effects of hydrostatic and uniaxial stress on the Schottky barrier heights of Ga-polarity and N-polarity n-GaN,” *Appl. Phys. Lett.*, vol 84, no. 12, pp. 2112-2114, Mar. 2004.

12. U. Karrer, O. Ambacher, and M. Stutzmann, “Influence of crystal polarity on the properties of Pt/GaN Schottky diodes,” *Appl. Phys. Lett.,* vol. 77, no. 13, pp. 2012-2014, Sep. 2000.

13. M.A. Pawlak, M. Popovici, J. Swerts, K. Tomida, Min-Soo Kim, B. Kaczer, K. Opsomer, M. Schaekers, P. Favia, H. Bender, C. Vrancken, B. Govoreanu, C. Demeurisse, Wan-Chih Wang, V. V. Afanas'ev, I. Debusschere, L. Altimime, J.A. Kittl ,

"Enabling 3X nm DRAM: Record low leakage 0.4 nm EOT MIM capacitors with novel stack engineering," *Proc. IEEE IEDM*, pp. 277-279, Dec. 2010.

14. I. Sayed, W. Liu, S. Chan, C. Gupta, M. Guidry, H. Li, S. Keller, and U. Mishra, "Net negative fixed interface charge for Si_3N_4 and SiO_2 grown in situ on 000-1 N-polar GaN," *Appl. Phys. Lett.,* vol. 115, p. 032103, Jul. 2019.

15. S. Keller, H. Li, M. Laurent, Y. Hu, N. Pfaff, J. Lu, D. F. Brown, N. A. Fichtenbaum, J. S. Speck, S. P. DenBaars, and U. K. Mishra, "Recent progress in metal-organic chemical vapor deposition of (000-1) N-polar group-III nitrides," *Semicond. Sci. Technol*. vol. 29, p. 113001, Aug. 2014.

16. M. A. Laurent, G. Gupta, D. J. Suntrup, S. P. DenBaars, and U. K. Mishra, "Barrier height inhomogeneity and its impact on (Al, In, Ga)N Schottky diodes*," J. Appl. Phys.*, vol. 119, p. 064501, Feb. 2020.

17. W. Monch, "Barrier heights of real Schottky contacts explained by metal-induced gap states and lateral inhomogeneities," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.,* vol. 17, no. 4, p.1867, 1999.

18. C. Hou, R. M. Gazoni, R. J. Reeves, and M. W. Allen, "High-temperature β-Ga_2O_3 Schottky diodes and UVC photodetectors using RuOx contacts," *IEEE Electron Device Lett.*, vol. 40, no. 10, pp.1587-1590, Oct. 2019.

19. X. Li, T. Pu, L. Li, and J. Ao, "Enhanced sensitivity of GaN-based temperature sensor by using the series Schottky barrier diode structure," *IEEE Electron Device Lett.,* vol. 41, no. 4, pp.601-604, Apr. 2020.

20. J. Osvald, J. Kuzmik, G. Konstantinidis, P. Lobotka, A. Georgakilas, “Temperature dependence of GaN Schottky diodes I-V characteristics,” *Microelectronic Engineering*, vol. 81, pp. 181-187, Aug. 2005.

21. T. Maeda, M. Okada, M. Ueno, Y. Yamamoto, T. Kimoto, M. Horita, and J. Suda, “Temperature dependence of barrier height in Ni/n-GaN Schottky barrier diode,” *Appl. Phys. Express.,* vol. 10, p. 051002, Apr. 2017.

22. N. Yildirim, K. Ejderha, and A. Turut, “On temperature-dependent experimental I-V and C-V data of Ni/n-GaN Schottky contacts,” *J. Appl. Phys.,* vol. 108, p. 114506, Dec. 2010.

23. J. H. Werner and H. H. Guttler, “Barrier inhomogeneities at Schottky contacts,” *J. Appl. Phys.*, vol. 69, no. 1, 1522-1533, Feb. 1991.

24. C. Lu, and S. N. Mohammad, “Validity/invalidity of Schottky-Mott rules for Schottky contacts to III-V nitride semiconductor heterostructures,” *Appl. Phys. Lett.,* vol. 89, p. 162111, Oct. 2006.

25. J.W.P. Hsu, M. J. Manfra, D.V. Lang, S. Richter, S. N. G. Chu, A. M. Sergent, R. N. Kleiman, L. N. Pfeiffer, and R. J. Molnar, “Inhomogeneous spatial distrubition of reverse bias leakage in GaN Schottky diodes,” *Appl. Phys. Lett.*, vol., 78, no. 12, pp. 1685-1687, Mar. 2001.

26. E. J. Miller, E. T. Yu, P. Waltereit, and J. S. Speck, “Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy,” *Appl. Phys. Lett.*, vol. 84, no. 4, pp. 535-537, Jan. 2004.

27. W. Lu, L. Wang, W. Gu, D. P. R. Aplin, D. M. Estrada, P. K. L. Yu, and P. M. Asbeck, "Analysis of reverse leakage current and breakdown voltage in GaN and InGaN/GaN Schottky barriers," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 1986-1994, Jul. 2011.

28. W. Monch, "Chemical trends of barrier heights in metal-semiconductor contacts: on the theory of the slope parameter," Appl. Surf. Sci. 92, 367, 1996.

29. S. M. Sze, K. K. Ng, Physics of Semiconductor Devices, 3rd ed., *Wiley,New York*, USA2007.

30. V. Bougrov, M. E. Levinshtein, S. L. Rumyantsev, A. Zubrilov, "Properties of Advanced SemiconductorMaterials GaN, AlN, InN, BN, SiC, SiGe," John Wiley & Sons, Inc., New York, 2001.

31. https://en.wikipedia.org/wiki/Electrical_resistivities_of_the_elements_(data_page)#CRC

Chapter 5. N-polar GaN Deep Recess MIS-HEMTs with ALD Ru Gates

This chapter discusses the W-band power performance of N-polar GaN deep recess MIS-HEMTs using a new atomic layer deposition (ALD) ruthenium (Ru) gate metallization process. The deep recess structure is utilized to control the DC-RF dispersion and increase the conductivity in the access regions. The ALD Ru effectively fills the narrow T-gate stems aiding realization of shorter gate lengths with lower gate resistance than in prior work. In this work, the gate length was scaled down to 48 nm resulting in the demonstration of a record-high 8.1 dB linear transducer gain measured at 94 GHz by load-pull. This increased gain has enabled a record 33.8% power-added efficiency (PAE) with an associated output power density (P_O) of 6.2 W/mm at 94 GHz.

5.1 Gate Resistance Challenges While Scaling Down

In prior deep recess N-polar GaN MIS-HEMTs by Romanczyk et al. [1,2] and Wienecke et al. [3] the gate metallization processes were done by E-beam evaporated Chromium (Cr). While excellent device performance of 8.8 W/mm with an associated PAE of 27.0% at 94 GHz was achieved, the foot gate length was limited to ~70 nm. One major reason for these devices limiting further scaling is the rising gate resistance using E-beam evaporation process. The gate resistance (R_G) vs. gate length (L_G) data was collected by Dr. B. Romanczyk and is shown in **Fig. 5.1**. For devices with gate width (W_G) of 2 × 37.5 μm in our typical π-feed T-gate structure, the gate resistance usually saturates around 2.5 Ω when the gate length is larger than ~70 nm. The gate resistance increases rapidly as the gate length gets below ~60nm and is almost doubled to 5 Ω when the L_G is reduced to ~40 nm. Further TEM inspection shows that the filling of the stem of the high-scaled T-gate from the E-beam

deposition process is not complete and a void exists in the stem. The incomplete filling of the T-gate stem can cause the high gate resistance and reduce the gain significantly as the gate length goes below 50 nm.

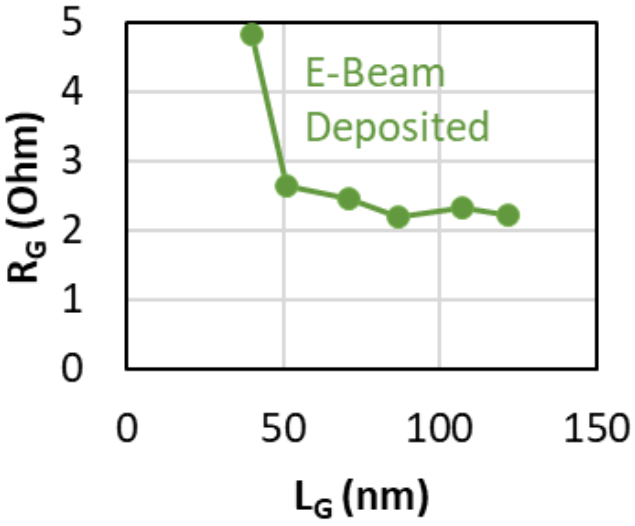


Figure 5.1 Gate resistance R_G vs. foot gate length L_G of E-beam evaporated Cr deposition. (Credits to Dr. B. Romanczyk)

To achieve higher PAE in W-band, which was still primarily limited by gain, it is necessary to scale down the gate length (L_G) while maintaining the deep recess structure. This requires a transition away from the existing gate metallization process, which would fail for gate lengths below ~60 nm due to incomplete filling of the stem of the T-gate using e-beam evaporated Cr. In this chapter, we present a N-polar GaN deep recess MIS-HEMT using a new ALD Ru metallization process to realize T-gates with 48 nm L_G and good control of gate resistance. Part of the figures and materials in this chapter are reproduced © 2021 IEEE., with permission, from [**Wenjian Liu**, Brian Romanczyk, Matthew Guidry, Nirupam Hatui, Christian Wurm, Weiyi Li, Pawana Shrestha, Xun Zheng, Stacia Keller, Umesh K Mishra, 6.2 W/mm and Record 33.8% PAE at 94 GHz from N-polar GaN Deep Recess MIS-HEMTs with

ALD Ru Gates. IEEE Microwave Wireless Component Lett., vol. 31, no. 6, pp. 748-751, June 2021].

5.2 Epitaxial Structure and Device Fabrication

5.2.1 Epitaxial structure

The sample was grown by metal organic chemical vapor deposition (MOCVD) on a miscut C-face SiC substrate. The epitaxial structure is shown in **Fig. 5.2** and, from bottom to top, consisted of a Fe-doped GaN buffer, a Si-doped graded AlGaN back barrier, a 12 nm unintentionally doped (UID) GaN channel, a 3.6 nm AlGaN cap layer, a 47.5 nm UID GaN cap layer and a 5 nm MOCVD SiN layer. TLM measurements indicated a sheet resistance of 288 Ω/□ in the GaN-capped access region. Compared to prior work using 2.6 nm as the AlGaN cap thickness, the 3.6 nm was selected with attempt to allow more over-etch during the selective etch of GaN cap over AlGaN cap layer thereby increasing the process tolerance.

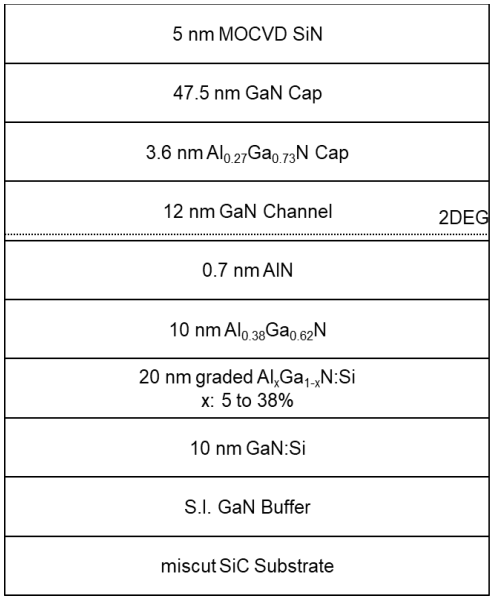


Figure 5.2 The N-polar GaN epitaxial structure grown by MOCVD

5.2.2 Device structure

Fig. 5.3 presents a cross-section of the fabricated device structure. The fabrication process followed the previous self-aligned deep recess approach [1, 2] and was modified to replace the e-beam evaporated Cr with ALD Ru as the gate stem metal. The excess Ru outside the gate region was etched away using an O_2/Cl_2 plasma [4]. Other relevant aspects of the device fabrication include n+ contacts regrown by MBE, a 5 nm MOCVD SiN gate dielectric, and a final 24 nm PECVD SiN passivation layer. The detailed fabrication steps and some optimizations are presented as follows.

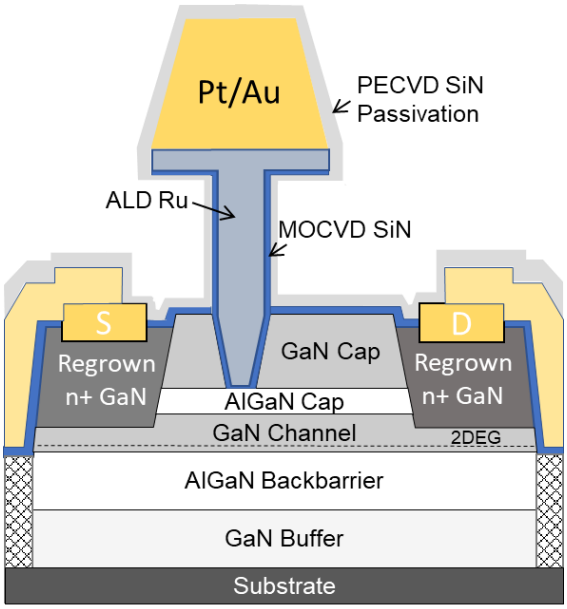


Figure 5.3 The N-polar GaN deep recess MIS-HEMT device structure with ALD Ru as the gate metal.

5.2.3 Processing steps

The device fabrication flow of N-polar GaN deep recess MIS-HEMT device structure with ALD Ru gate metal can be divided into three parts including 1) source/drain n+ regrowth and isolation; 2) gate recess and gate metallization; 3) Ohmic contact and passivation.

For the source/drain n+ regrowth and isolation part, **Fig. 5.4** illustrates the detailed process from step 1 to step 6. Starting from the epitaxial sample with 5 nm in-situ MOCVD grown SiN protective layer (step 1), the sample the first undergoes hard mask deposition consisting of ~10 nm ALD Al_2O_3, ~330 nm PECVD SiO_2 and ~10 nm Cr metal deposited by E-beam evaporator (step 2). The e-beam lithography (EBL) using UV-N photoresist (PR) defined the nominal source to drain distance (L_{SD}). The pattern from EBL was transferred to Cr mask using a Cl_2/O_2-based inductively coupled plasma (ICP) dry etch. Then the UV-N PR was removed, and patterned Cr mask was left above SiO_2 layer. A following high-power $CHF_3/CF_4/O_2$-based ICP dry etch transferred the pattern to SiO_2 and stopped within the Al_2O_3 layer due to the over etch of SiO_2 needed. The etch selectivity (> 10) of SiO_2 over Al_2O_3 allows~50 nm SiO_2 over etch. Patterned Cr was removed by Cl_2/O_2-based ICP dry etch after the pattern was transferred to SiO_2. The Al_2O_3 below SiO_2 was wet etched by AZ300 developer and the MOCVD SiN layer was etched by CF_4/O_2-based ICP dry etch, which would not etch the GaN cap surface meaningfully. Next BCl_3/SF_6-based ICP etch was used to etch the GaN cap and selectively stopp in the AlGaN cap layer. The AlGaN cap layer was then etched by low power BCl_3/Cl_2-based RIE and around 2 nm of the GaN channel was etched to ensure the n+ GaN regrowth on GaN channel (step 3).

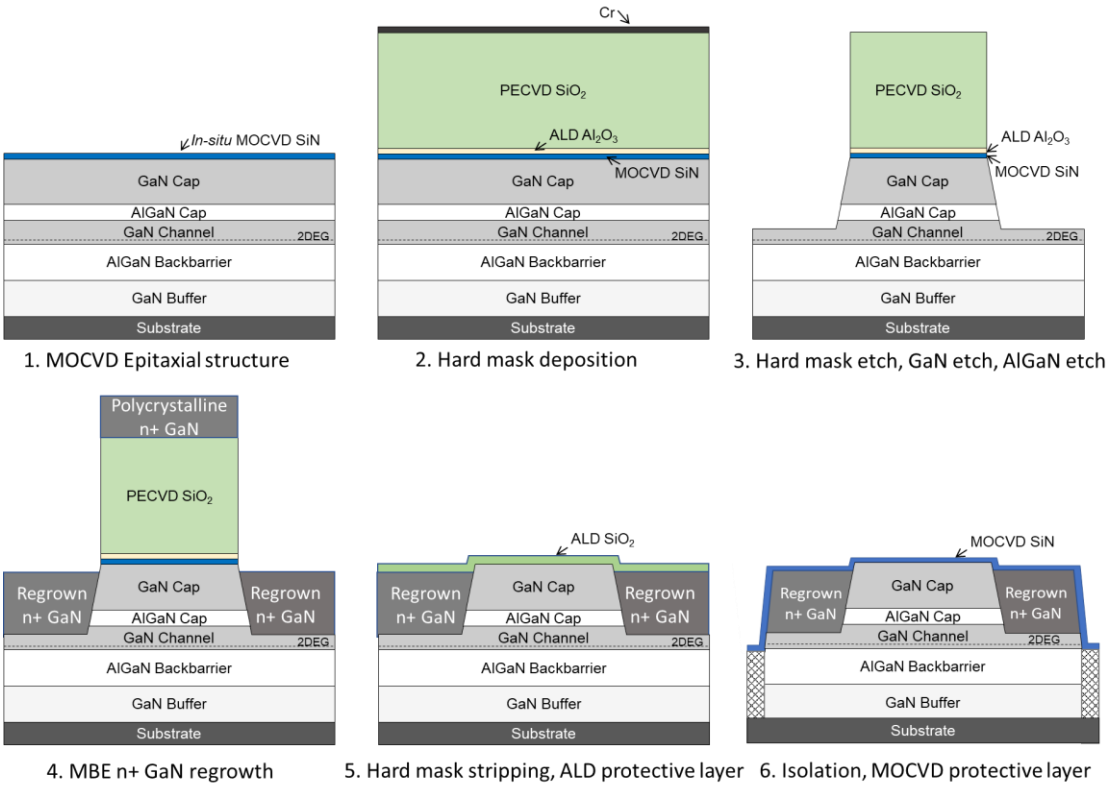


Figure 5.4 The processing steps in part 1) source/drain n+ regrowth and isolation

Step 4 shows the schematic after the MBE n+ GaN regrowth, which included 20nm UID GaN and 30 nm high Si-doped n+ GaN. SEM images showed some polycrystalline GaN on top of the PECVD SiO_2 hard mask. The $SiN/Al_2O_3/SiO_2$/polycrystalline n+ GaN stacked layers were stripped away in HF: HNO_3 (1:1) solution. Then 40 nm ALD SiO_2 was deposited to protect the GaN surface (step 5). The isolation of device included ALD SiO_2 etch, regrown n+ layer etch and ion implantation with the optical lithography PR patterns. After the removal of PR and SiO_2, 7 nm MOCVD SiN was deposited as protective layer (step 6).

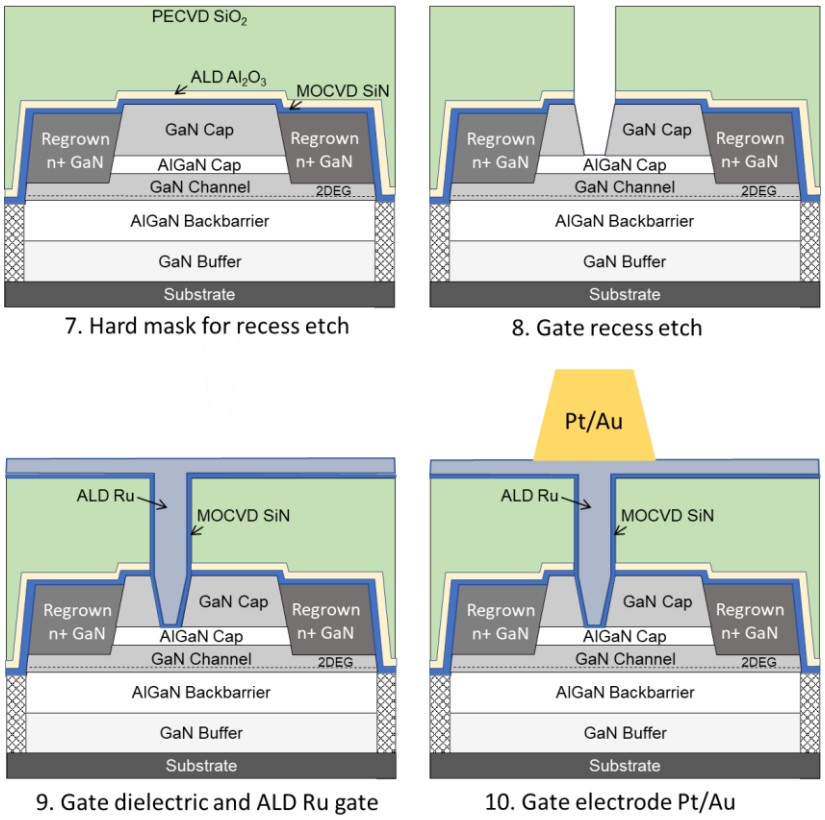


Figure 5.5 The processing steps in part 2) gate recess and gate metallization

In **Fig. 5.5**, the gate recess and gate metallization part (from step 7 to step 10) start with the hard mask deposition. ~10 nm Al_2O_3 and ~220 nm PECVD SiO_2 were deposited on top of the MOCVD SiN (step 7). The recess dimensions are defined by the EBL using CSAR as the resist for SiO_2 etch. Similar to step 3, the SiO_2, Al_2O_3, SiN and GaN cap are etched away in order till the etch stopped on the AlGaN cap layer (step 8). The dimensions of exposed AlGaN cap layer are defined as the foot gate length. In step 9, ~5 nm SiN gate dielectric was deposited by MOCVD and ~45nm Ru metal was deposited by ALD as the gate metal on MOCVD SiN. The ALD Ru gate metal is supposed to provide better filling in the stem trench and reduce the gate resistance. The top-gate is patterned by EBL using UV-6 as resist. Pt/Au

gate electrode is deposited by e-beam evaporation and lifted-off. The ALD Ru and Pt/Au conclude the gate metallization (step 10).

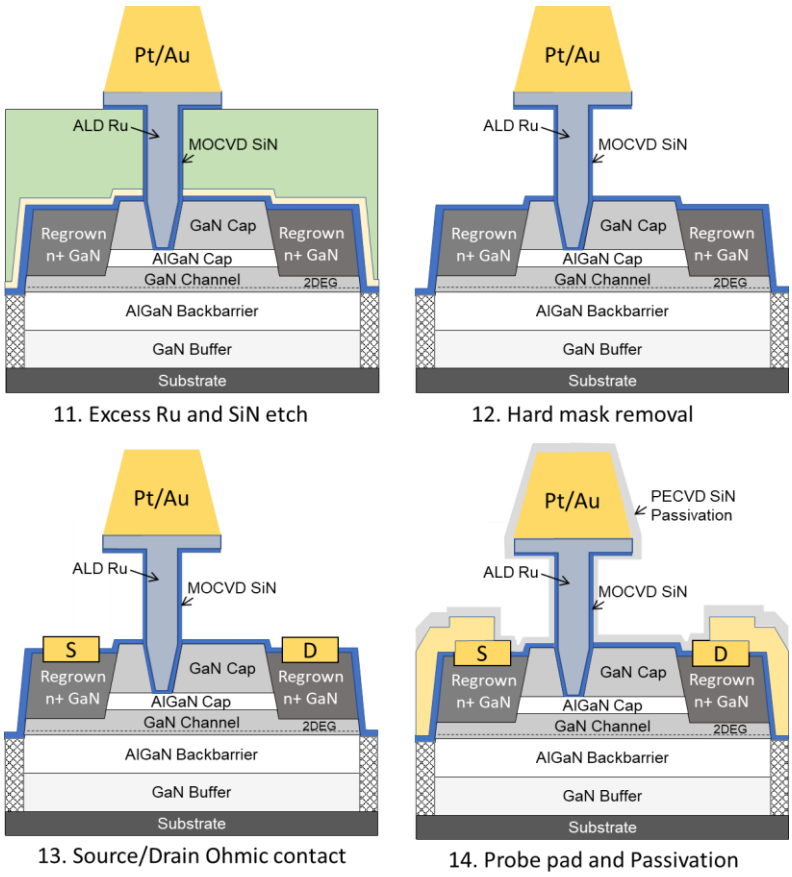


Figure 5.6 The processing steps in part 3) Ohmic contact and passivation

The last part is the Ohmic contact and passivation (from step 11 to step 14 in **Fig. 5.6**). Using the top gate Pt/Au as a mask, the excess Ru is etched by Cl_2/O_2-based high power ICP dry etch. Excess SiN is also etched away using CF_4/O_2-based ICP dry etch (step 11). The hard mask Al_2O_3/SiO_2 is removed in a buffered HF: H_2O (1:4) solution while the MOCVD SiN is barely etched. A "T"-shape gate is formed (step 12). After the optical lithography for Ohmic contact layer, SiN is etched by CF_4/O_2-based ICP etch and ~7 nm n+ GaN is etched by BCl_3/Cl_2-based RIE etch. In step 13, prior to the Ohmic metal Ti/Au (20 nm/100 nm)

deposition by e-beam evaporation, 60 seconds HCl: H_2O (1:1) surface treatment is used. Finally, PECVD SiN layer is deposited to passivate the device and achieve better dispersion control (step 14).

5.3 DC Performance

5.3.1 TLM measurements

The total pad metal to the 2DEG contact resistance consists of the metal to n+ GaN contact resistance, the n+ GaN resistance and the n+ GaN to the 2DEG contact resistance. These values can be extracted from the TLM measurements with a series of separations. The general equation can be expressed as:

$$R_{total} = R_{sheet} + 2R_{contact}$$

Where R_{total} is the measured resistance for various separations, R_{sheet} is the sheet resistance of the material and $R_{contact}$ is the contact resistance from one side. The TLM extraction data are shown in the figures below. **Fig. 5.10** is used to extract the metal to n+ GaN contact resistance. The y-interception of the n+ GaN TLM fitting line implies the contact resistance of 3.5 Ω. Given the metal pad width of 20 μm, the metal to n+ GaN contact resistance is 0.07 Ω mm and the associated sheet resistance is 116 Ω/□.

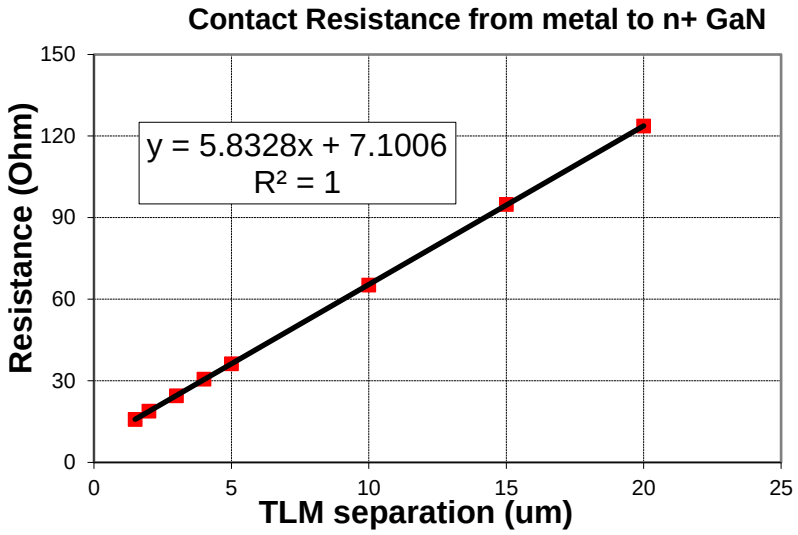


Figure 5.7 The TLM measurements to extract the metal to n+ GaN contact resistance

The total contact resistance can be obtained through the fitting of GaN cap TLM structures in **Fig. 5.11**. Similar to the extraction of metal to n+ contact resistance, the total contact resistance from metal to 2 DEG is extracted to be 0.16 Ω mm with metal pad width of 20 μm and the associated epi sheet resistance is 288 Ω/□ with the epi pad width of 21 μm. Compared with prior N-polar deep recess HEMT epi (around 220 Ω/□ in ref [1, 2]), the epi sheet resistance here is more than 25% higher. Even though the increased epi sheet resistance is undesired, the results from this epi using ALD Ru gate metal showed great improvement in PAE as shown in the following parts.

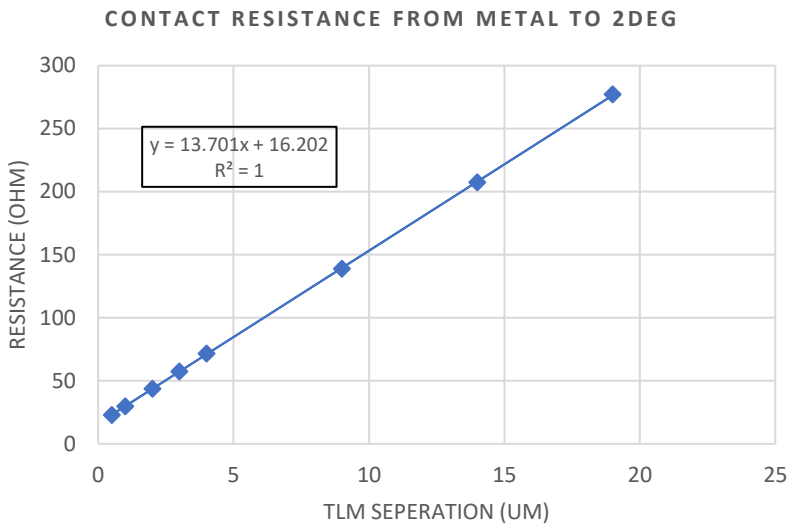


Figure 5.8 The TLM measurements to extract the total contact resistance from metal to 2DEG.

5.3.2 Input and output DC characteristics

Unless otherwise stated, the reported devices have a L_G of 48 nm, gate to drain spacing (L_{GD}) of 220 nm, and source to drain (L_{SD}) of 340 nm. The gate has a width (W_G) of 2 × 37.5 μm with a π-feed layout. The PECVD SiN passivation layer thickness is 24 nm, which is founded to improve the output power density and PAE. The impact of different SiN passivation will be discussed later in the Chapter.

The input characteristics are shown in **Fig. 5.12 (a)**, demonstrating a peak extrinsic transconductance (g_m) of 440 mS/mm at V_{DS} of 5 V and a current density of 1.34 A/mm at V_{GS} of 0 V.

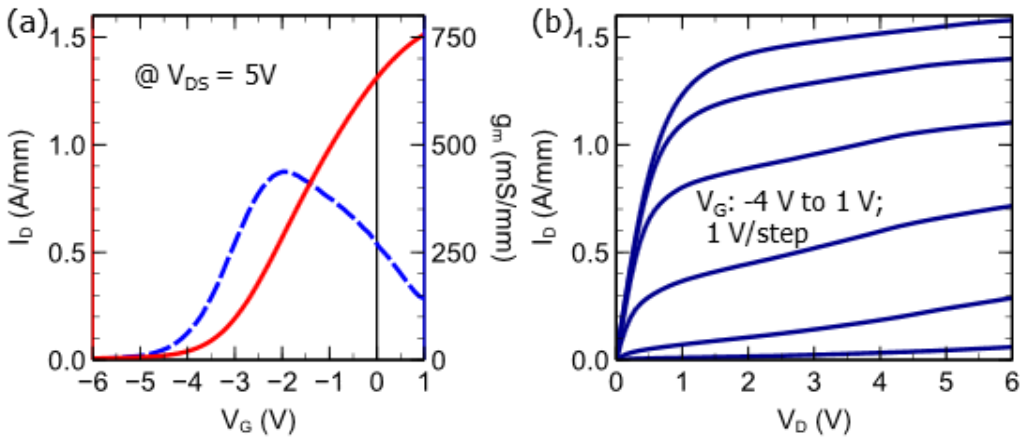


Figure 5.9 DC performance: (a) I_{DS}-V_{GS} input curves with peak extrinsic g_m of 440 mS/mm at V_{DS} of 5 V and 1.34 A/mm at V_G = 0 V; (b) I_{DS}-V_{DS} output characteristics with V_G from -4 V to 1 V.

In **Fig. 5.12(b)**, an on-resistance of 0.49 Ω·mm was extracted at V_{GS} = 1 V. From capacitance-voltage measurements, the sheet charge density in the channel is around 7×10^{12} cm^{-2}, which is lower than in [10] and is attributed to lower doping levels in the as-grown epi structure. The lower sheet charge density and its impact on device performance will be discussed further in section "***CV- measurement and high current density from TLM***" of the Chapter.

5.3.3 Breakdown voltage

To evaluate the breakdown voltage (V_{BR}), a series of transistors with various gate to drain distance (L_{GD}) were characterized using the drain current injection method [5]. With a constant 1 mA/mm drain current injected, the V_{BR} corresponds to the maximum V_{DS} as the gate voltage decreases to pinch off the channel.

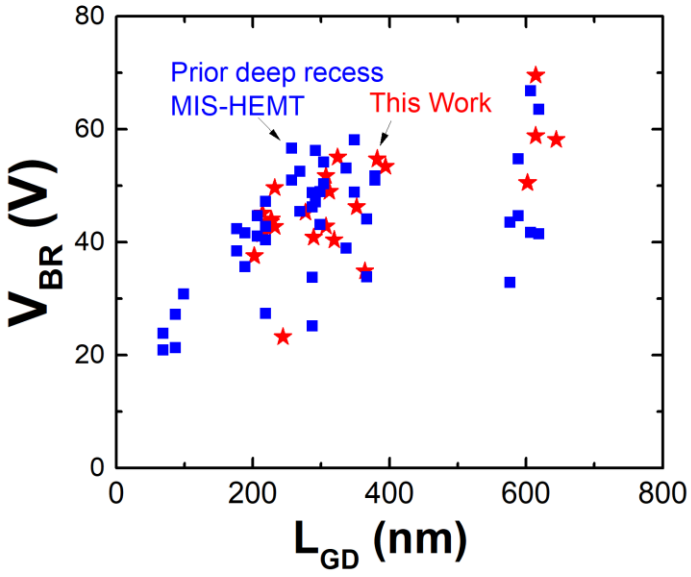


Figure 5.10 V_{BR} measured in a series of transistors with 1 × 25 um W_G and various L_{GD} using the drain current injection method at 1 mA/mm. This Ru MIS-HEMT work (red start) is compared with data from ref [1] (blue square).

The V_{BR} vs. L_{GD} response is presented in **Fig. 5.13**. Similar to our prior e-beam Cr gated N-polar GaN deep recess MIS-HEMTs, the breakdown voltage with around 250 nm L_{GD} stayed in the range of around 40 V to 50 V. This work utilizing ALD Ru as the gate metal does not cause the degradation of breakdown performance. Such a high breakdown voltage with small L_{GD} enables the large voltage swing while maintaining low resistance, which produces high output power.

5.4 Pulsed I-V and Small Signal Performance

5.4.1 Pulsed measurements

As with previous N-polar GaN deep recess devices, the GaN cap layer and SiN passivation layer on the access regions reduced the DC-RF dispersion significantly. Dual-pulsed pulsed I-V measurements with a 650 ns pulse width and 0.02% duty cycle were conducted on a device with L_{SD} of 500 nm L_G of 78 nm, and W_G of 2 × 37.5 μm. The device was biased in pinch-off ($V_{GS,Q}$ = -5V) and a $V_{DS,Q}$ up to 15 V. In **Fig. 5.14**, the DC-RF dispersion was low as expected from previous reported results. It should be noted that the device showed the increase in current density under $V_{GS,Q}$ = -5 V and $V_{DS,Q}$ = 15 V conditions compared to the DC bias conditions. The increase in the pulsed current was observed before and can be introduced as anti-dispersion [6], which could be attributed to some positive charge generated in the gate dielectric, depletion region or back barrier during the pulsed conditions. The anti-dispersion could help achieve a high current density and thereby the power density.

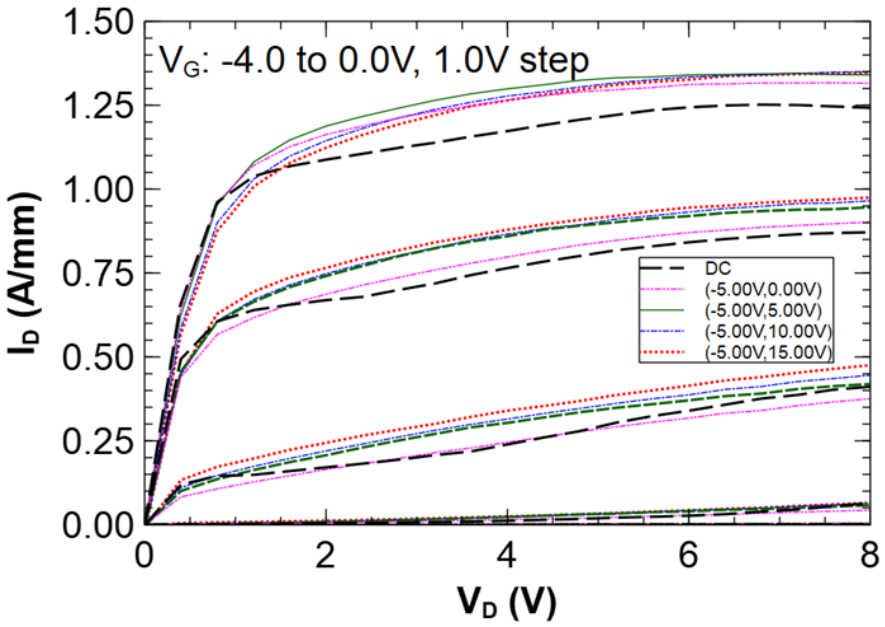
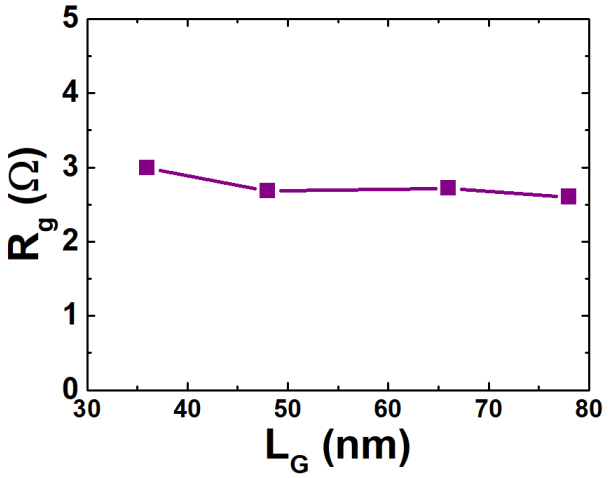


Figure 5.11 Pulsed I-V measurements with 650 ns pulse and 0.02% duty cycle under ($V_{GS,Q}$, $V_{DS,Q}$) = (-5 V, 0), (-5 V, 5 V), (-5 V, 10 V), (-5 V, 15 V) conditions, along with DC curves.

5.4.2 Small-Signal performance and gate resistance

The S-parameters were measured up to 67 GHz and used to extract the device's equivalent circuit parameters. After the probe pad was de-embedded via on-wafer open and short structures, the gate resistance (R_G) values were extracted, based on the methodology in [7] for a range of L_G from 78 nm to 36 nm with top gate length of 400 nm as shown in **Fig. 5.15(a)**. As L_G scales down, R_G does not significantly change, which indicates that R_G is predominantly determined by Pt/Au top metal (**Fig. 5.3**) and the better filling of ALD Ru metal into the high aspect ratio T-gate stem trenches provides more transistor gain. For **Fig. 5.15(b)**, the f_{max} achieves a maximum value at L_G of 48 nm, which could be understood through the trend of R_G and f_T v.s. L_G. When the L_G scaling further down to 36 nm, the f_T still increases while the increase in R_G hindered the further increase of fmax.



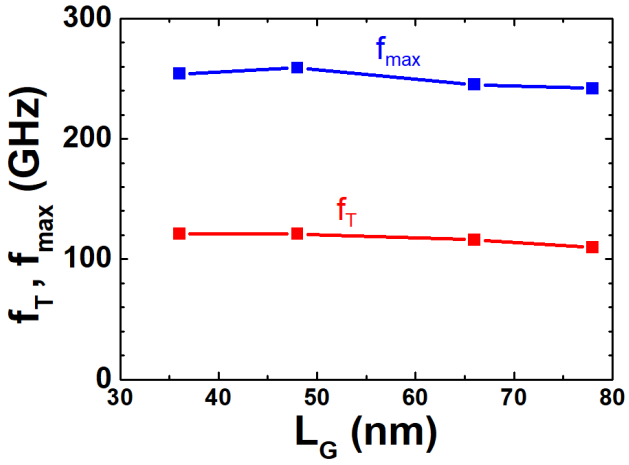


Figure 5.12 (a) Gate resistance and (b) peak f_{max} and f_T extracted from small signal measurements for different L_G

To understand the gain at a typical bias current density used for W-band operation, the bias was set to be 12 V V_D and -2.5 V V_G, under which the peak f_{max} was measured. In **Fig. 5.16**, based on the measured $|h_{21}|^2$ (red circle) and the unilateral gain U (blue square) results, f_T and f_{max} were extrapolated to be 112 GHz and 260 GHz, respectively. The maximum stable gain (green triangle) is 10.7 dB at 67 GHz.

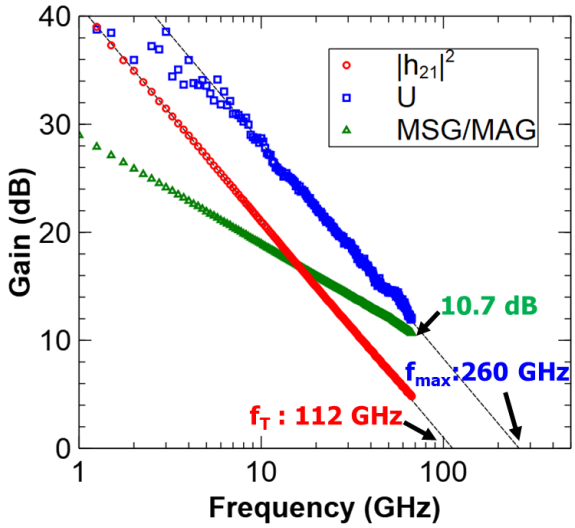


Figure 5.13 Maximum available gain (MSG/MAG) measured at V_D = 12V and V_G = -2.5V

5.5 Large-Signal Performance at 94 GHz

The 94 GHz uncooled continuous-wave (CW) large-signal data presented here was obtained using a Maury Microwave passive tuner-based load pull system. The configuration of this load pull system was detailed in [8]. The device was operated in class AB at quiescent drain current ($I_{DS,Q}$) of 500 mA/mm, balancing the trade-off between gain and drain efficiency to maximize PAE [9].

The load pull power sweeps at 94 GHz for $V_{DS,Q}$ 16 V and 18 V are presented in **Fig. 5.17(a)** and **(b)**. In **Fig. 5.17(a)**, at $V_{DS,Q}$ = 16 V, a maximum total output power of 26.2 dBm (417 mW) was measured with an associated power-added efficiency (PAE) of 34.8%. To the best of our knowledge, the 34.8% PAE represents the highest reported efficiency for a GaN device in W-band. At the same time, the associated output power density is very high at 5.6 W/mm. When the $V_{DS,Q}$ is increased to 18 V in **Fig. 5.17(b)**, the output power density rises to 6.2 W/mm with an associated 33.8% PAE. Possible augmentation in power density by further increasing $V_{DS,Q}$ is limited by the matching range of the load tuner in our measurement setup. The record high PAE resulted from the high linear transducer gain (G_T) of 8.1 dB at 94 GHz, a record for N-polar GaN, resulting from the scaled gate length that the ALD gate process enabled. The key 94 GHz large signal results are also summarized in **Table 5.1**.

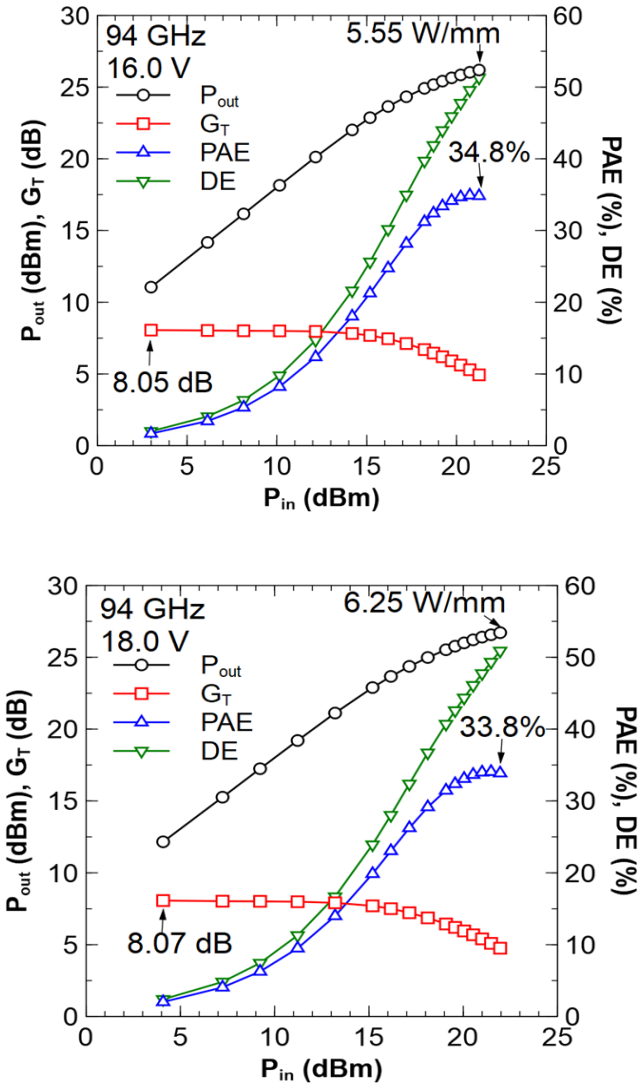


Figure 5.14 Load pull power sweeps at 94 GHz with 500 mA/mm $I_{DS,Q}$ and $V_{DS,Q}$ of (a) 16 V and (b) 18 V.

Table 5.1 Summary of the 94 GHz large-signal results at $V_{DS,Q}$ = 16V and 18V.

$V_{DS,Q}$ (V)	Γ_{source}	Γ_{load}	$G_{T,max}$ (dB)	Peak P_O (W/mm)	Assoc. PAE (%)
16	-0.64-0.18j	-0.34+0.50j	8.1	5.6	34.8
18	-0.64-0.18j	-0.34+0.50j	8.1	6.2	33.8

Fig. 5.18 benchmarks our work with prior N-polar GaN devices and other Ga-polar devices and MMICs in the literature. In **Fig. 5.18(a)**, prior N-polar GaN devices [2, 10, 11] using the deep recess structure and e-beam deposited Cr gate metal have reached very high power densities up to 8.8 W/mm. The high PAE of 34.2 % was also achieved at 87 GHz [12]. With the new use of ALD Ru as gate metal, the N-polar GaN device in this work pushes the efficiency to new heights while also demonstrating very high power density. The power densities were slightly lower on this wafer compared to prior N-polar GaN due to lower than usual 2DEG charge in this sample.

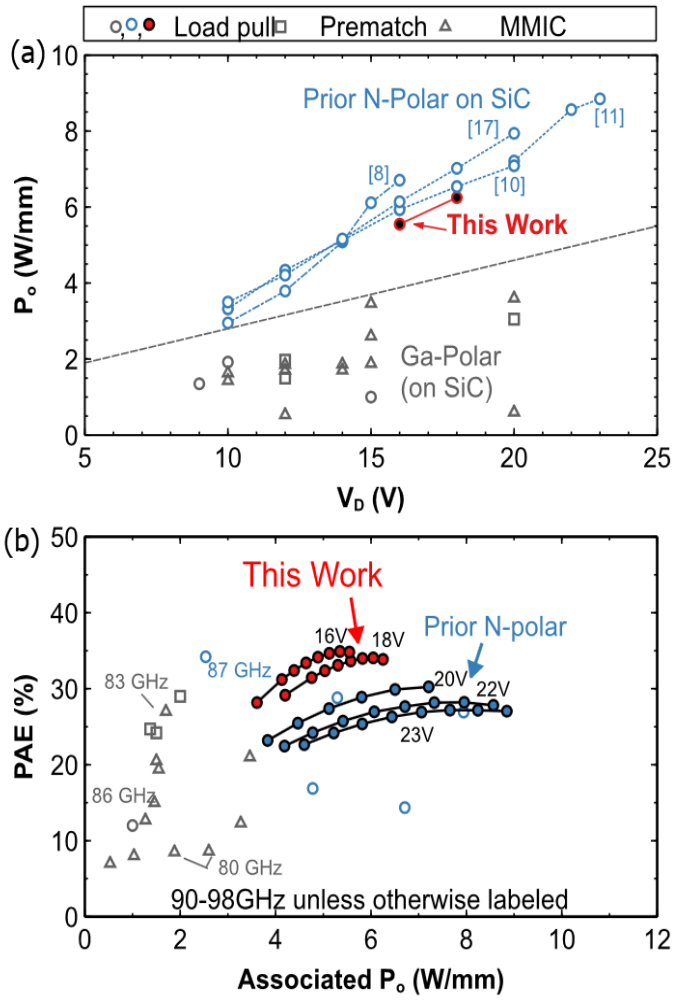


Figure 5.15 Benchmarking (a) the Po-V_D and (b) the PAE-associated P_O from this work with prior N-polar devices and other Ga-polar GaN devices and MMICs in the literature. Ga-polar points are referred in [1].

Despite of the lower power density in this work compared with some prior N-polar devices, the performance is still exceptional and more optimized epitaxy with the new gate process is expected to maximize both output power and efficiency.

5.6 Effects of PECVD SiN Passivation

Previous study shows that further passivation using PECVD deposited SiN can reduce the dispersion more, achieve higher output power density and improve the PAE [2]. However, the PECVD SiN passivation layer will add extra parasitic capacitance and could reduce the gain especially when the passivation layer is too thick. The effect of PECVD SiN thickness on the gain was studied to understand the trade-off between dispersion and parasitic capacitance caused by the passivation. The thicknesses of the PECVD SiN passivation layer were 0, 40 and 24nm. The measurements were done on the devices in three steps: 1) without passivation layer; 2) then 40 nm SiN passivation layer was deposited by PECVD; 3) lastly the 40 nm PECVD SiN passivation layer was thinned to be 24 nm by diluted buffered HF etch.

The pulse-IV measurement was used to characterize the dispersion behaviour with and without passivation. While the device with 0 nm SiN passivation shows evident knee voltage walk out, the 40 nm and 24 nm passivation both show better dispersion control as shown in **Fig. 5.19**. The bias conditions include DC condition and ($V_{GS,Q}$, $V_{DS,Q}$) = (0, 0), (-5 V, 10 V) pulsed conditions.

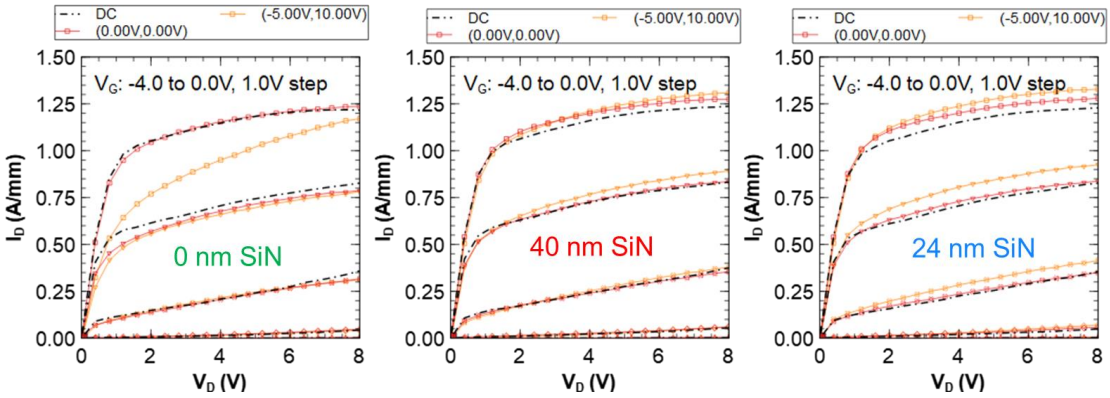


Figure 5.16 The Pulse-IV for the device with L_{SD} of 740 nm, L_G of 78 nm and W_G of 75 um. The device was measured with 0 nm SiN, 40 nm SiN and 24 nm SiN.

Through small signal measurements, the passivation layer was found to decrease the gain as expected. For the measured device with L_{SD} of 420 nm, L_G of 48nm and W_G of 75 µm in **Fig. 5.20**, the maximum stable gain or maximum available gain (*MSG/MAG*) dropped from 10.6 dB to 10.1 dB at 67 GHz when the device is passivated with 40 nm PECVD SiN. The thinning process from 40 nm to 24 nm helped recover most of the gain to 10.5 dB.

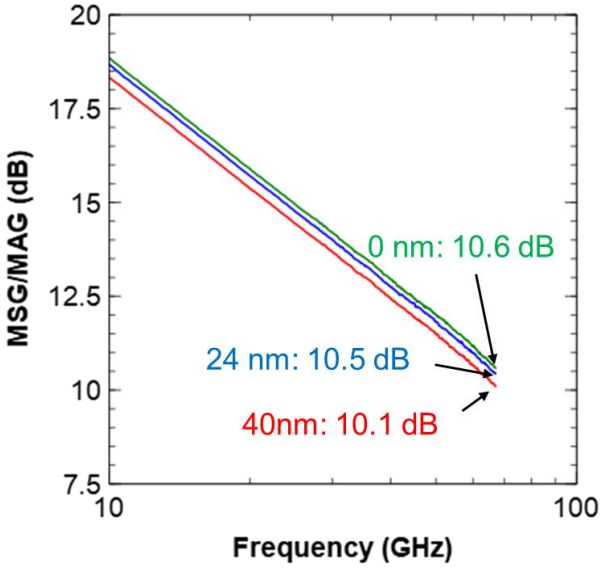


Figure 5.17 The *MSG/MAG* of the device with L_{SD} of 420 nm, L_G of 48 nm and W_G of 75 µm. The data was acquired at the peak fmax bias conditions.

The pulse-IV and small signal results clearly indicated that the thickness of PECVD SiN passivation layer needed to balance the trade-off between dispersion and gain. The impact on the 94 GHz power performance was studied through 94 GHz load-pull measurements. The relatively low $V_{DS,Q}$ of 12V was selected to ensure that the device can be measured several times without degradation. In **Fig. 5.21**, the transducer gain G_T vs. input power P_{in} was plotted for the series of SiN passivation layer. For all the P_{in} level, 40 nm passivation provided the lowest G_T and illustrated the penalty from excessive passivation. In the low P_{in} region,

parasitic capacitance impacted the G_T most and 0 nm passivation gave the highest G_T. As the P_{in} increased above 15 dBm, 24 nm passivation started to perform best, which is the result of good dispersion control in a highly stressed environment.

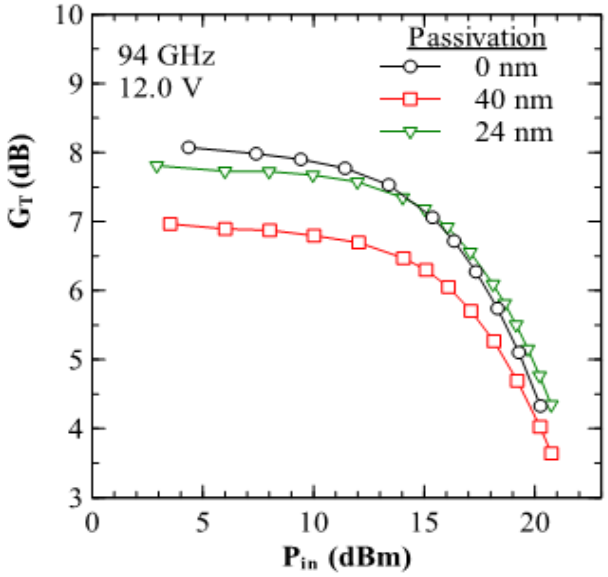


Figure 5.18 The transducer gain G_T vs. available input power measured by 94 GHz load-pull measurements for different SiN passivation.

To show the benefits of a proper passivation, the power performance P_{out}, DE and PAE of 0 and 24 nm passivation layer were added in **Fig. 5.22**. At $V_{DS,Q}$ of 12V, the peak P_{out} and PAE are both increased after the 24 nm passivation along with the gain improvement. The big boost in peak PAE from ~30% to ~35% demonstrated the necessity to properly passivate the device.

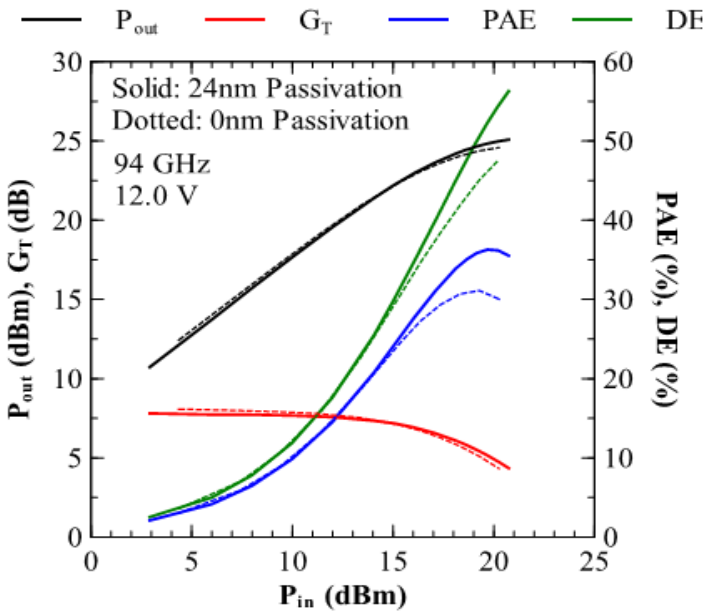


Figure 5.19 The P_{out}, G_T, PAE and DE against the available input power from load-pull measurements.

5.7 CV and High Current Measurements

The relatively low power density compared to the best result at 94 GHz is possibly caused by the lower DC current density given the same $V_{DS,Q}$ and excellent dispersion control. The C-V capacitor is measured at 100 kHz to obtain the sheet charge density under the gate. As shown in **Fig. 5.23**, the sheet charge density at 0V is less than 7×10^{12} /cm^2 with ALD Ru as the gate metal. After taking the threshold voltage shift into consideration, the charge density at V_{GT} (defined as V_G -V_T) of 3V in this sample is 9.6×10^{12} /cm^2 while the sample with best Pout has 1.32×10^{13} /cm^2. The charge density is around 30% lower in this ALD Ru gated device and could explain the lower power density.

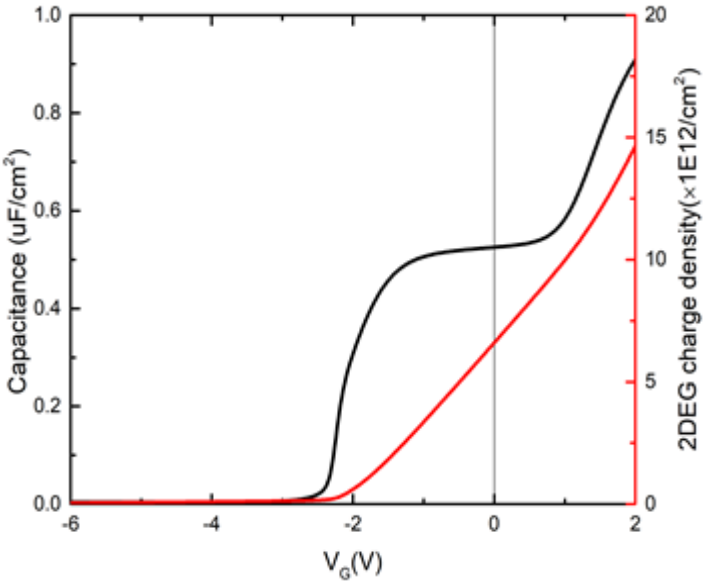


Figure 5.20 The CV measurement of Ru/SiN/GaN capacitor structure**.**

Even though the 3.6 nm thick AlGaN cap as opposed to 2.6 nm AlGaN cap in the best Pout sample may reduce the charge in the channel, our BandEng simulation indicates that the reduced charge could mostly come from the back barrier Si-doping drift to lower concentration.

A direct way to look into the low current density at high $V_{DS,Q}$ is to measure the TLM structures with GaN cap and SiN layer. This structure does not have gate metal on top and can exclude the effect from different gate metals (Cr vs. ALD Ru). The TLM with 500 nm L_{SD} is biased to high voltages and close to current saturation.

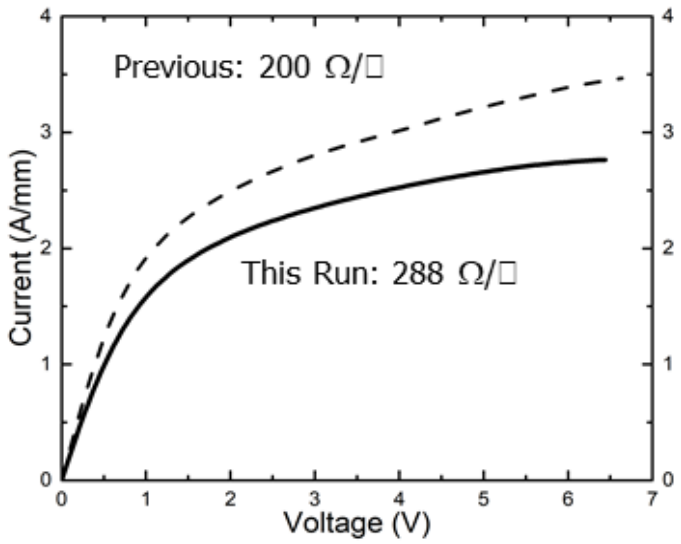


Figure 5.21 The current with voltage sweep on the access region TLM with 500nm L_{SD}. Previous data from ref.?? is plotted in dash line and this work is plotted in solid line.

As the **Fig. 5.24** shows, the current density in this sample is generally low for all the bias. In the low bias region, the slope indicates the higher sheet resistance in this sample given the similar contact resistance. The current density at 6V is around 25% lower than the previous best Pout sample. Future experiments should be done on epi with high sheet charge density and high current density, in order to pursue better output power density and efficiency.

5.8 Summary

A N-polar GaN high mobility electron transistor with deep recess structure and ALD Ru gate metal demonstrated record high PAE of 33.8% and high power density of 6.2 W/mm at 94 GHz. The deep recess structure in conjunction with a thin SiN passivation has excellent control over the DC-RF dispersion and the ALD Ru metal fills a narrow 48 nm trench gate, providing high gain. This device combination in N-polar GaN HEMTs pushes the high output

power and high efficiency performance at mm-wave frequency into new possibilities. N-polar GaN today is very promising for mm-wave power amplifiers and further development will continue to improve performance.

References

1. B. Romanczyk, et al., “Demonstration of constant 8 W/mm power density at 10, 30, and 94 GHz in state-of-the-art millimeter-wave N-polar GaN MISHEMTs,” IEEE Trans. Electron Devices, vol. 65, no. 1, pp. 45–50, Jan. 2018, doi: 10.1109/ted.2017.2770087.

2. B. Romanczyk, et al., “W-band power performance of SiN-passivated N-polar GaN deep recess HEMTs,” IEEE Electron Device Lett., vol. 41, no. 3, pp. 349-352, Mar. 2020, doi: 10.1109/LED.2020.2967034.

3. S. Wienecke et al., “N-polar GaN cap MISHEMT with record power density exceeding 6.5 W/mm at 94 GHz,” IEEE Electron Device Lett., vol. 38, no. 3, pp. 359–362, Mar. 2017, doi: 10.1109/led.2017.2653192.

4. W. Liu, et al., “Ru/N-polar GaN Schottky diode with less than 2 □A/cm2 reverse current,” IEEE Electron Device Lett., vol. 41, no. 10, pp 1468-1471, Oct. 2020, doi: 10.1109/LED.2020.3014524.

5. S. R. Bahl and J. A. del Alamo, “A new drain-current injection technique for the measurement of off-state breakdown voltage in FETs,” IEEE Trans. Electron Devices, vol. 40, no. 8, pp. 1558–1560, Aug. 1993, doi: 10.1109/16.223723.

6. B. Romanczyk, Insight into the Design, Fabrication, and mm-Wave Power Performance of N-Polar GaN Deep Recess HEMTs, Ph.D. dissertation, University of California, Santa Barbara, 2018.

7. M. Guidry et al., “Small-signal model extraction of mm-wave N-polar GaN MISHEMT exhibiting record performance: Analysis of gain and validation by 94 GHz

loadpull," in IEEE MTT-S Int. Microw. Symp. Dig., San Francisco, CA, USA, May 2016, pp. 1–4, doi: 10.1109/MWSYM.2016.7540047.

8. M. Guidry et al., "W-band passive load pull system for on-wafer characterization of high power density N-polar GaN devices based on output match and drive power requirements vs. gate width," in Proc. 87th ARFTG Microw. Meas. Conf., San Francisco, CA, USA, May 2016, pp. 1–4, doi: 10.1109/ARFTG.2016.7501955.

9. B. Romanczyk et al., "W-band N-polar GaN MISHEMTs with high power and record 27.8% efficiency at 94 GHz," in IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2016, pp. 3.5.1–3.5.4, doi: 10.1109/IEDM.2016.7838339.

10. B. Romanczyk et al., "W-band N-polar GaN MISHEMTs with high power and record 27.8% efficiency at 94 GHz," in IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2016, pp. 3.5.1–3.5.4, doi: 10.1109/IEDM.2016.7838339.

11. B. Romanczyk et al., "mm-wave N-polar GaN deep recess MISHEMT delivering over 7 W/mm and 25% power-added efficiency at 94 GHz," in International Symposium on Compound Semiconductor (ISCS), Berlin, Germany, May. 2017.

12. B. Romanczyk et al., "Record 34.2% efficient mm-wave N-polar AlGaN/GaN MISHEMT at 87 GHz," Electron. Lett., vol. 52, no. 21, pp. 1813–1814, Oct. 2016, doi: 10.1049/el.2016.2664.

Chapter 6. Ru/N-polar GaN Schottky-HEMT

In this Chapter, a Ru/N-polar GaN Schottky-HEMT operating at W-band has been investigated and its good large signal performance is reported. Thanks to the direct Schottky contact between Ru and N-polar GaN channel, the fabricated Schottky HEMT with L_G of 60 nm has a high peak extrinsic transconductance of 798 mS/mm with a gate leakage in pinch-off below 3×10^{-4} A/mm at V_{DS} = 5V. The Schottky-HEMT shows high power-added efficiency (PAE) of 27.1% and output power density (P_O) of 4.87 W/mm at 94 GHz and $V_{DS,Q}$ = 16V. The peak PAE is 31.8% with associated P_O of 3.31 W/mm at $V_{DS,Q}$ = 12V.

6.1 Prior W-band GaN HEMTs

N-polar GaN MIS-HEMTs have demonstrated excellent output power performance with high efficiency at W-band (75-110 GHz). Compared with Ga-polar GaN HEMTs, either in MIS-structure or Schottky-structure, N-polar GaN HEMTs have exploited additional advantages from the reversed polarization. The advantages of the N-polar orientation are: a strong back barrier, improved scalability and low ohmic contact resistance [1-5]. Furthermore, the GaN cap layer in the deep recess N-polar GaN HEMT structure [6-8] can result in high RF current density and low knee voltage by mitigating the DC-RF dispersion and increasing access region conductivity. At 94 GHz, Romanczyk et al. [9] obtained record-high output power density (P_O) of 8.84 W/mm and an associated power-added efficiency (PAE) of 27% in a deep recess N-polar GaN MIS-HEMT where SiN grown by metal organic chemical vapor deposition (MOCVD) was used as the gate dielectric. In a similar MIS-HEMT device with an atomic layer deposited (ALD) ruthenium (Ru) gate, Liu et al. [10] realized record-high PAE of 34% and associated P_O of 6.2 W/mm at 94 GHz.

While N-polar GaN deep recess MIS-HEMTs have achieved several records of power performance at W-band, there is no demonstrated N-polar GaN Schottky-HEMTs with W-band performance up to now. At W-band, scaling down the gate length while maintaining a good aspect ratio is critical. Removing the gate dielectric used in GaN HEMTs would allow for Schottky-HEMTs with greatly reduced gate-to-2DEG distance thus better aspect ratio and further scaling. In Ga-polar GaN HEMTs, all the W-band performance data points in the literature are from their Schottky-barrier gated structure [11-20]. **Fig. 6.1** shows the W-band large signal performance of Ga-polar Schottky-HMET from literature and N-polar MIS-HEMT from Mishra group. The Schottky-HEMT in N-polar GaN operating at W-band is still missing and of great interest.

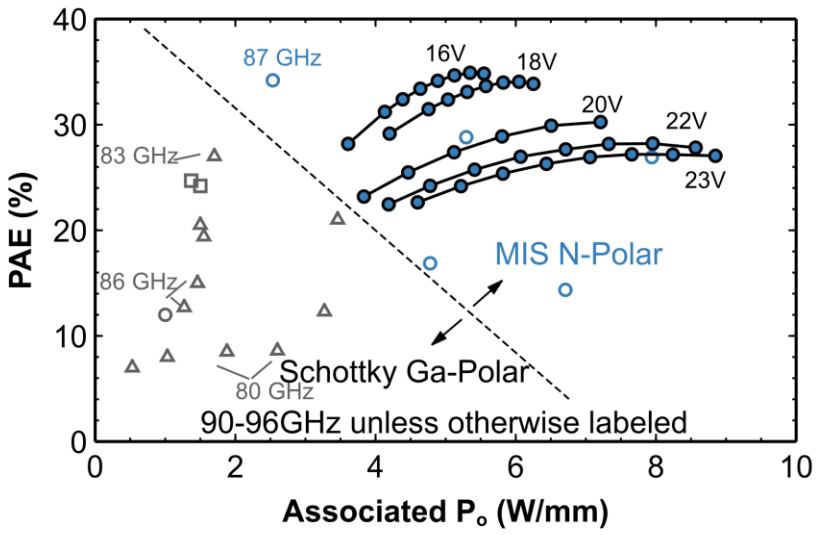


Figure 6.1 The W-band large signal performance of Ga-polar Schottky-HMET from literature and N-polar MIS-HEMT from Mishra group

However, the lack of a good Schottky metal on N-polar GaN with low reverse leakages has hindered the advance of N-polar GaN Schottky-HEMTs in the past. Various metals including Pt, Ni, Pd, Cu etc., on N-polar GaN [21-24] formed low Schottky-barrier height

associated with parasitic leakage mechanisms, which caused the high gate leakage. In Chapter 4, ALD Ru as a promising Schottky metal on N-polar GaN was demonstrated [25]. The formed barrier between the Ru and pristine N-polar GaN surface is 0.17eV higher than the value predicted by metal work function and GaN electron affinity [26]. Due to the enhanced barrier height and the near-ideal thermionic current behavior, the Schottky diode had a record low reverse current of less than 2 $\mu A/cm^2$ at V_G of -5V [25]. Additionally, the ALD method is well suited to fill the high-aspect-ratio foot gate stem for the deep recess HEMT structure and provide low gate resistance for short gate length needed at W-band [10].

Here, the use of ALD Ru as the Schottky gate in a scaled N-polar GaN deep recess HEMT helps achieve good W-band load-pull power performance. Due to the good Schottky contact between Ru and N-polar GaN, the fabricated Schottky HEMT with L_G of 60 nm has a high peak extrinsic transconductance of 798 mS/mm and the off-state gate leakage is around 3×10^{-4} A/mm at V_{GS} = -4V and V_{DS} = 5V. From the 94 GHz load-pull measurements, the N-polar GaN HEMTs showed high PAE of 27.1% and associated P_O of 4.87 W/mm at $V_{DS,Q}$ = 16V. The peak PAE is 31.8% with associated P_O of 3.31 W/mm at $V_{DS,Q}$ = 12V.

6.2 Epitaxial and Device Structure

The sample was grown by MOCVD on a miscut SiC substrate. **Fig. 6.2** presents the epitaxial structure, composed of a semi-insulating GaN buffer using Fe for compensation, a AlGaN back barrier which incorporated a graded section with Si doping, a 12 nm GaN channel, a 3.6 nm $Al_{0.27}Ga_{0.73}N$ cap, a 47.5 nm GaN cap layer and a 5 nm MOCVD SiN protective layer. The epi structure is the same as prior one used in ALD Ru N-polar GaN MIS-HEMT in chapter 5, while they were grown at different days.

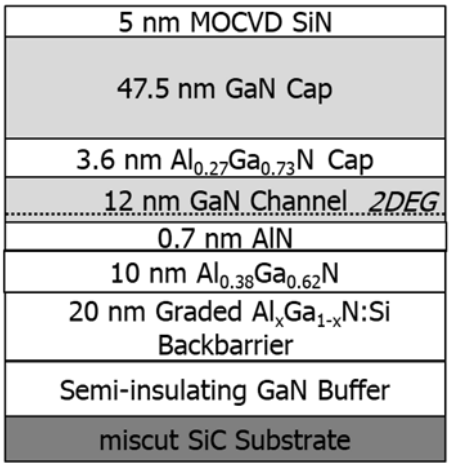
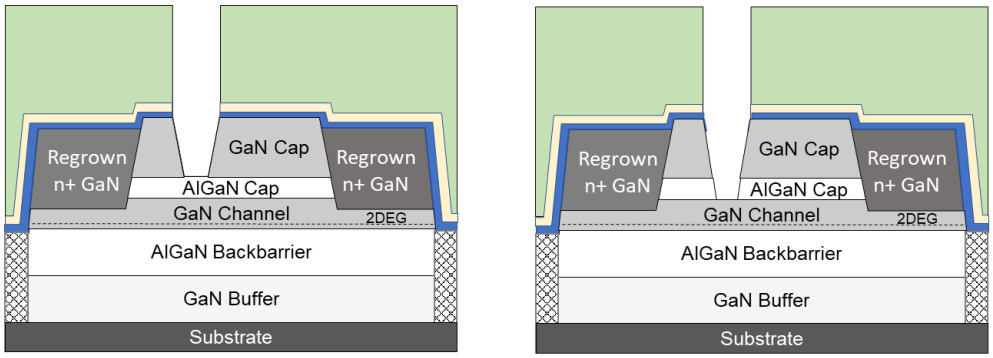


Figure 6.2 The MOCVD grown N-polar GaN epitaxial structure used in N-polar GaN Schottky-HEMT

The fabrication adopted the self-aligned deep recess process detailed in Chapter 5 as **Fig. 6.3** (a), which was changed to utilize ALD Ru as the Schottky gate metal. As shown in **Fig. 6.3** (b), prior to the deposition of the ALD Ru, the AlGaN cap above the GaN channel was etched, resulting in the Schottky barrier formed on the GaN channel. The etching process was done by low power BCl_3/Cl_2-based RIE and around 1 nm of the GaN channel was etched. It should be noted that the BCl_3/Cl_2-based RIE etch could introduce different interface properties between the Ru and N-polar GaN, compared with the interface in Ru/N-polar GaN diode study in Chapter 4.



(a) Gate recess etch in MIS-HEMT (b) Gate recess etch in Schottky-HEMT here

Figure 6.3 The gate recess etching step comparison between (a) MIS-HEMT and (b) Schottky-HEMT

A cross-section of the fabricated Ru/N-polar GaN Schottky-HEMT device structure is shown in **Fig. 6.4**. The sheet resistance of the GaN-capped access region obtained by characterizing TLM structures was measured to be 278 Ω/□. The sheet charge in the 2DEG channel is around 1.1×10^{13} cm^{-2}, which is lower than previous samples [8], caused by the lower doping in the epi. The pad metal to the 2DEG contact resistance was 0.16 Ω·mm and the regrown n+ GaN to the 2DEG contact resistance is 0.03 Ω·mm. The sheet resistance of epi and contact resistance from metal to 2DEG are in align with the results from Chapter 5.

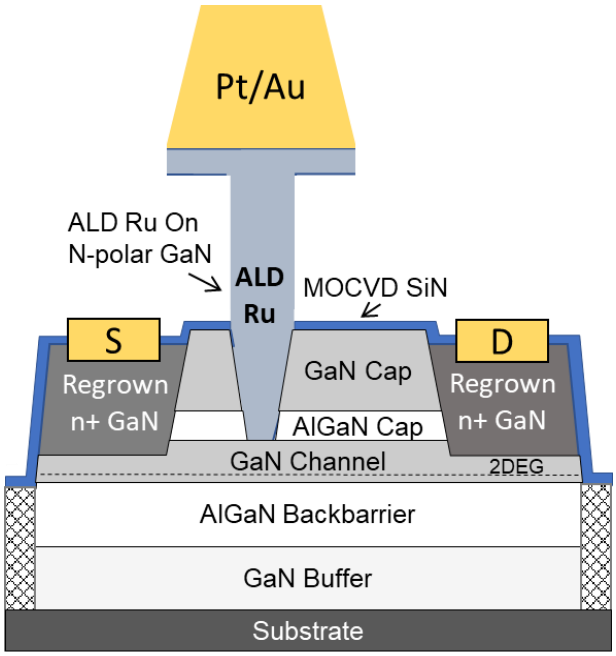


Figure 6.4 The deep recess Schottky-HEMT device structure with ALD Ru gate metal on N-polar GaN.

6.3 DC Performance and Gate Leakage

The reported devices have a 2 × 37.5 μm gate width (W_G), a gate length (L_G) of 60 nm, a source to drain spacing (L_{SD}) of 420 nm with a gate to drain distance (L_{GD}) of 290 nm. In **Fig. 6.5** (a), The transfer characteristics demonstrated an excellent peak extrinsic transconductance (g_m) of 798 mS/mm at V_{DS} of 5 V, which is more than 60% higher than that of comparable N-polar GaN MIS-HEMTs [8, 27].

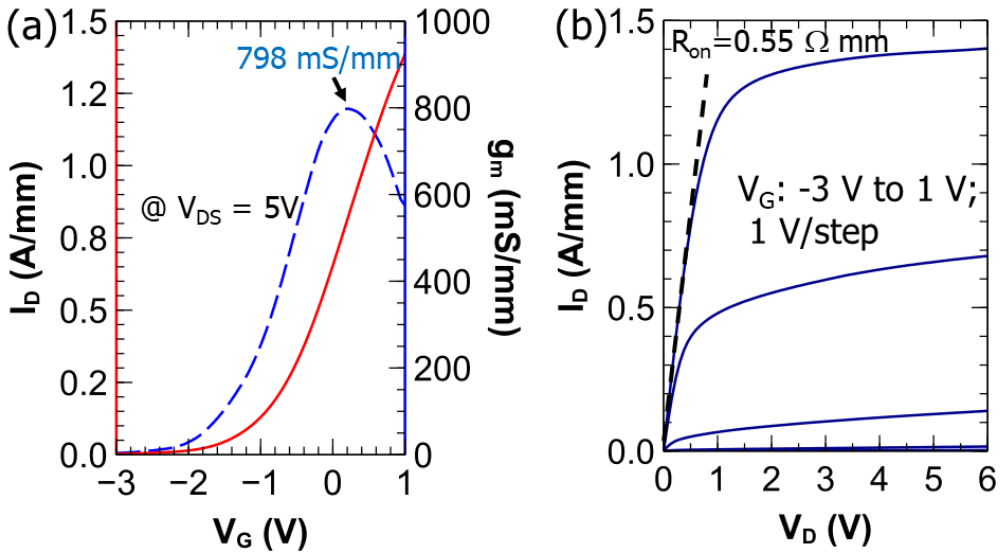


Figure 6.5 DC performance of the device with L_{SD}-420 nm, L_G-60 nm, W_G-2×37.5 µm: (a) I_{DS}-V_{GS} at V_{DS} of 5 V with peak extrinsic g_m of 798 mS/mm; (b) I_{DS}-V_{DS} with V_G varying from -3 V to 1 V in 1V steps.

The increase of the peak g_m value can be explained by the reduced gate to 2DEG distance without the existence of the gate dielectric. The threshold voltage was extracted to be around -0.9V. In **Fig. 6.5** (b), at V_G = 1V, an on-resistance (R_{on}) from low V_{DS} was extracted to be 0.55 Ω mm. The three terminal hard breakdown voltage was up to 40 V for transistor with L_{GD} of around 290 nm.

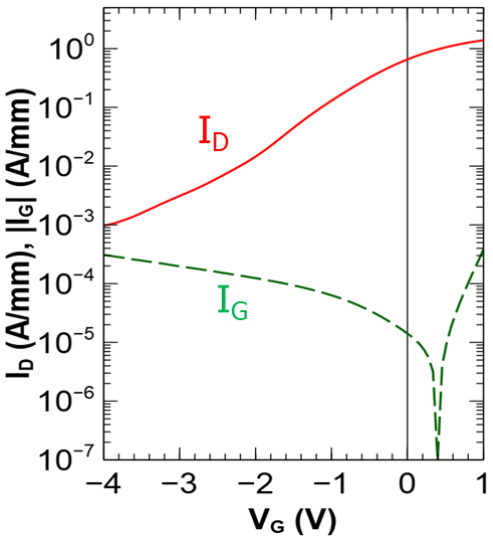
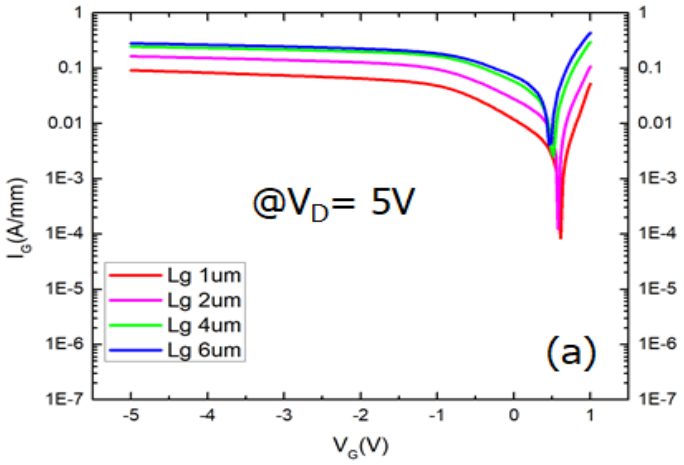


Figure 6.6 I_D (red solid), and I_G (green dashed)-V_G in semi-log scale at V_{DS} = 5 V

In **Fig. 6.6**, The gate current (I_G) is around 3×10^{-4} A/mm at V_{GS} = -4V and V_{DS} = 5V, which is around one-order of magnitude less than previous Ni-gated N-polar GaN planar Schottky-HEMT, with 0.7 μm L_G [5]. Compared with the reverse current density in the Ru on pristine N-polar planar GaN Schottky diode, the gate leakage in the deep recess Schottky-HEMTs is relatively high. In Ga-polar deep recess Schottky-HEMTs, relatively high gate leakage was observed due to several possible reasons. Chu et al. [28, 29] proposed that the surface charges on the thick GaN cap may lead to electric field crowding and high gate leakage. It is also possible that the etched GaN surface may lower the barrier height and cause high gate leakage [30-34]. Zhang et al. [35] used a new atomic layer etching technique to recess-etch the gate and showed a more than 3-order reduction in gate current than conventional etch. Besides, the possible leakage through the contact on the GaN cap sidewall may cause high gate current. For our N-polar deep recess HEMTs, the relatively high gate current is currently under investigation and lower gate leakage is needed in the future, which can offer better on/off ratio.

Gate leakage and barrier

To investigate the gate current through the foot gate region GaN channel or the sidewall GaN cap. The off-state gate current I_G vs. V_G in transistors with different gate lengths from 6 µm to 1 µm was measured at V_{DS} = 5V as shown in **Fig. 6.7** (a) above. Then based on **Fig. 6.7** (a), I_G vs. gate length L_G at V_G of -3 V was plotted in the **Fig. 6.7** (b). As the gate length reduces, the gate current also reduces. Although the I_G vs. L_G is not a strict linear behavior, the dependence on the L_G suggests the gate current is dominated by the leakage through the foot gate for these relatively large L_G dimensions. However, this analysis is unreliable for a L_G of 60nm. For small gate length less than 100 nm, it is hard to separate the contributions of the gate leakage at the edge from the gate leakage through the bottom foot gate. The electric field around the edge is usually highest and could have exponentially increased the gate leakage, which may dominate the simplest expectation of a linear dependence of L_G length.



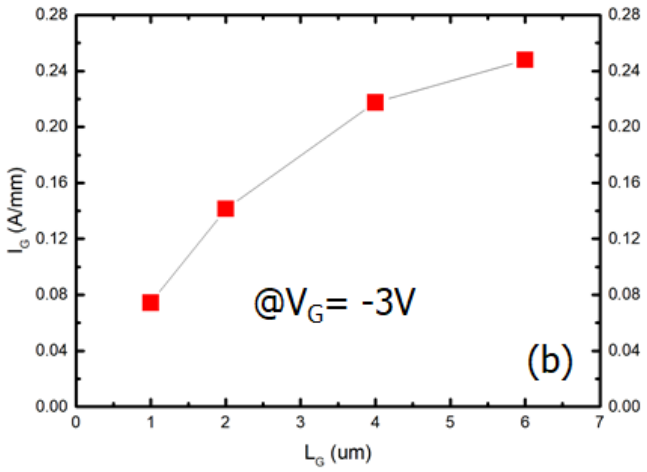


Figure 6.7 (a) I_G vs. V_G in transistors with different gate lengths from 6 um to 1 um was measured at V_{DS} = 5V; (b) I_G vs. gate length L_G at V_G of -3 V from (a)

The barrier height between Ru and the virgin N-polar GaN surface on sapphire substrate (Ru/GaN (N-polar) /Sapphire) was studied in ref. [25] and ref. [26]. In those papers, the diode device structure was designed to specifically investigate the barrier height and the conducting mechanism. The epi structure consisted of the n- GaN (to form Schottky barrier with Ru, the anode) and the n^+ GaN as the cathode (to form uniform current flow into the barrier). Accurate barrier height extraction from I-V and C-V data relied on the structure with uniform current flowing and the n^- GaN depletion.

However, the HEMT epi structure on SiC substrate used in this Chapter adopted lateral 2DEG as the current flow medium and the barrier height extraction based on the ideal equations may not be rigorous. Therefore, the C-V structure from the HEMT epi structure can be measured as an initial estimation on the barrier height values. Based on the forward bias region in the CV structure, the saturation current (I_s) was obtained through the extrapolation to zero bias and the barrier height of the HEMT structure is extracted to be 0.41eV using the

methods in ref. 25. The extracted lower barrier height indicates that the etching damages on the surface of N-polar GaN could reduce the barrier height and increase the gate leakage.

6.4 Small Signal Performance and Pulsed I-V

The S-parameters under different bias conditions were measured up to 67 GHz using a Keysight N5227A PNA calibrated by the LRRM method at the probe tips [36]. On-wafer open and short structures were used to de-embed the probe pad. The f_{max} contour at various V_{GS} and V_{DS} bias conditions was shown in **Fig. 6.8** (a). The peak f_{max} occurred at V_{GS} of 0V, V_{DS} of 12V and I_{DS} of 770 mA/mm.

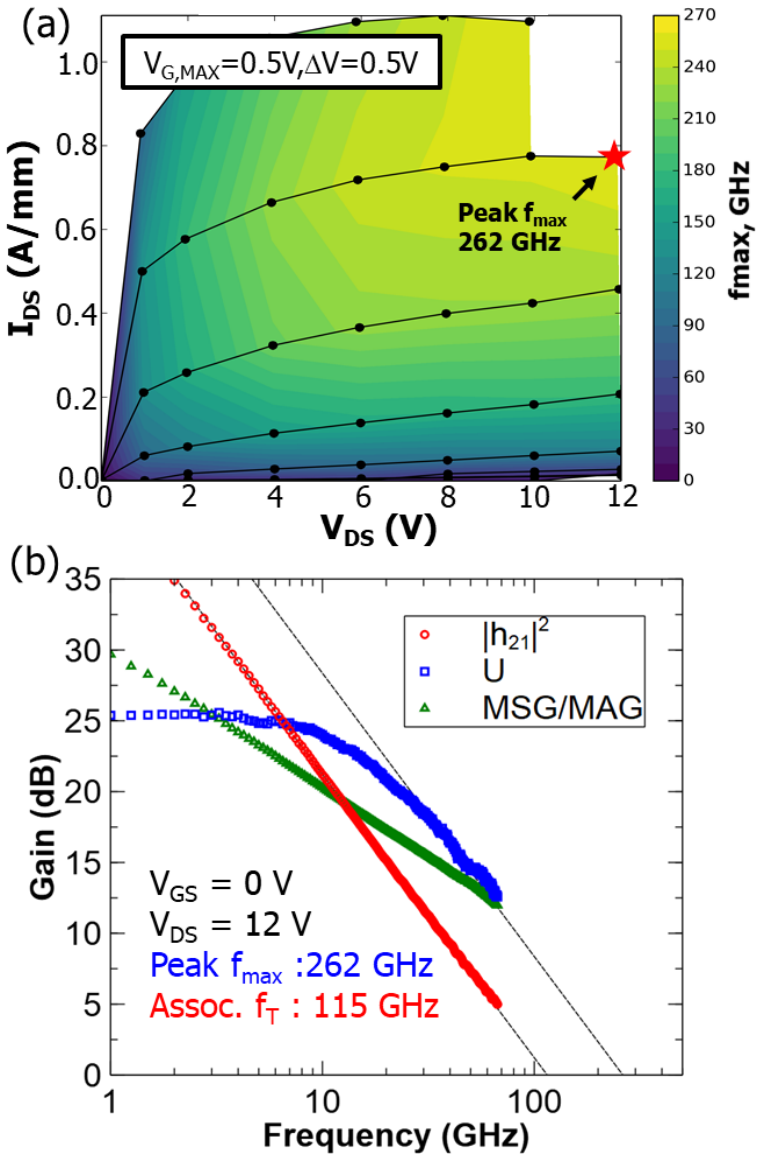


Figure 6.8 Small signal results for the device with L_{SD}-420 nm, L_G-60 nm, W_G-2×37.5 μm: (a) f_{max} contour plot with peak fmax biased at V_G= 0 V and V_D=12 V; (b) Gain-frequency plot at bias point with peak f_{max} 262 GHz.

In **Fig. 6.8** (b), the peak f_{max} from the gain-frequency plot was extrapolated to be 262 GHz via a 20 dB/decade slope from the unilateral gain (U). The associated f_T was extracted to be 115GHz from $|h_{21}|^2$. At the peak *fmax* bias conditions, the maximum stable gain in **Fig. 6.8** (b) is 12.6 dB at 67 GHz. This small signal gain is around 2dB higher than that in the Ru MIS-

HEMTs with 48 nm L_G [10]. The peak f_T was 131 GHz at V_{GS} = 0V and V_{DS} = 4V from the f_T contour.

Dual-pulsed pulsed I-V measurements with a 650 ns pulse width and 0.02% duty cycle were conducted on a device with L_{SD} of 740 nm L_G of 60 nm, and W_G of 2 × 37.5 μm. The device was biased in pinch-off ($V_{GS,Q}$ = -2V) and a $V_{DS,Q}$ up to 10 V. In **Fig. 6.9**, the DC-RF dispersion was low as expected from previous reported results and showed similar enhanced current density at the high $V_{DS,Q}$ of 10 V. Similar anti-dispersion behaviour is also observed as the MIS-HEMTs shown in Chapter 5.

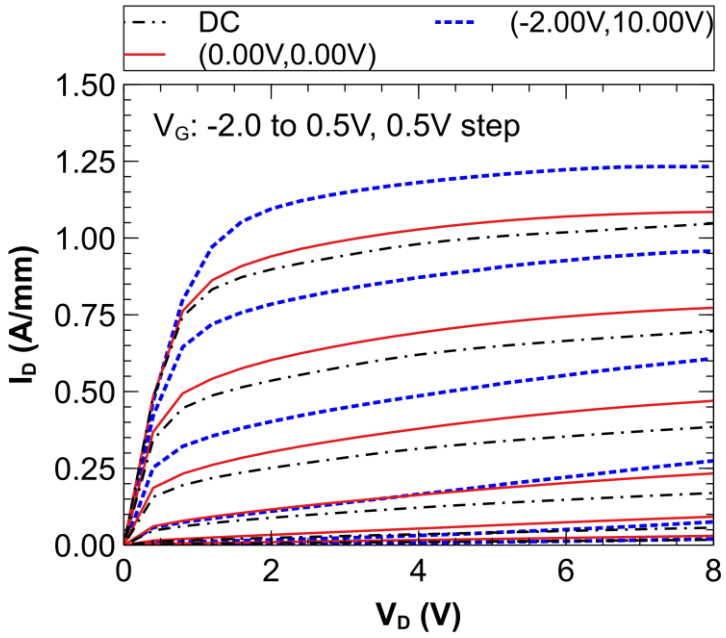


Figure 6.9 Pulsed I-V measurements with 650 ns pulse and 0.02% duty cycle under $V_{GS,Q}$ = -2 V and $V_{DS,Q}$ = 10 V condition, along with DC and ($V_{GS,Q}$, $V_{DS,Q}$) of (0,0) curves.

6.5 Large Signal Performance at 94 GHz

The quiescent current $I_{DS,Q}$ bias condition is investigated to optimize the PAE with the tradeoff between gain and DE. In prior MIS-HEMTs, Romanczyk et al., [37] investigated the impact of the bias conditions on the large signal performance including PAE, DE, Po and G_T. It was found that a $I_{DS,Q}$ of around 500 mA/mm could maximize the PAE. Here, the Schottky-HEMT is also biased at different $I_{DS,Q}$ levels from 215 mA/mm to 579 mA/mm while the quiescent voltage $V_{DS,Q}$ is kept to be 12 V as shown in **Fig. 6.10**. 94 GHz load pull measurements were conducted using the system described in [38]. For the high $I_{DS,Q}$ of 579 mA/mm, a G_T at low input power could achieve around 7.5 dB when the device operates close to class-A conditions. When the $I_{DS,Q}$ level is less than 482 mA/mm, the amplifier operation moves towards deep Class-AB and the G_T starts to fall off evidently. At these high current $I_{DS,Q}$ levels above 300 mA/mm, the G_T is compressed as the input power increases.

For low bias current at 215 mA/mm and 270 mA/mm, the initial gain expansion behavior is observed in the N-polar GaN Schottky-HEMT, which we have not typically seen before in N-polar GaN MIS-HEMT. Additionally, In **Fig. 6.10** (b), the DE at low $I_{DS,Q}$ is high since the DC power consumption decreased during the deep Class-AB operation. The combination of gain expansion and high DE at low $I_{DS,Q}$ could result in a higher PAE compared to the case of high $I_{DS,Q}$. From **Fig. 6.10** (d), the 215 mA/mm bias current gives higher peak PAE and higher PAE across all output power.

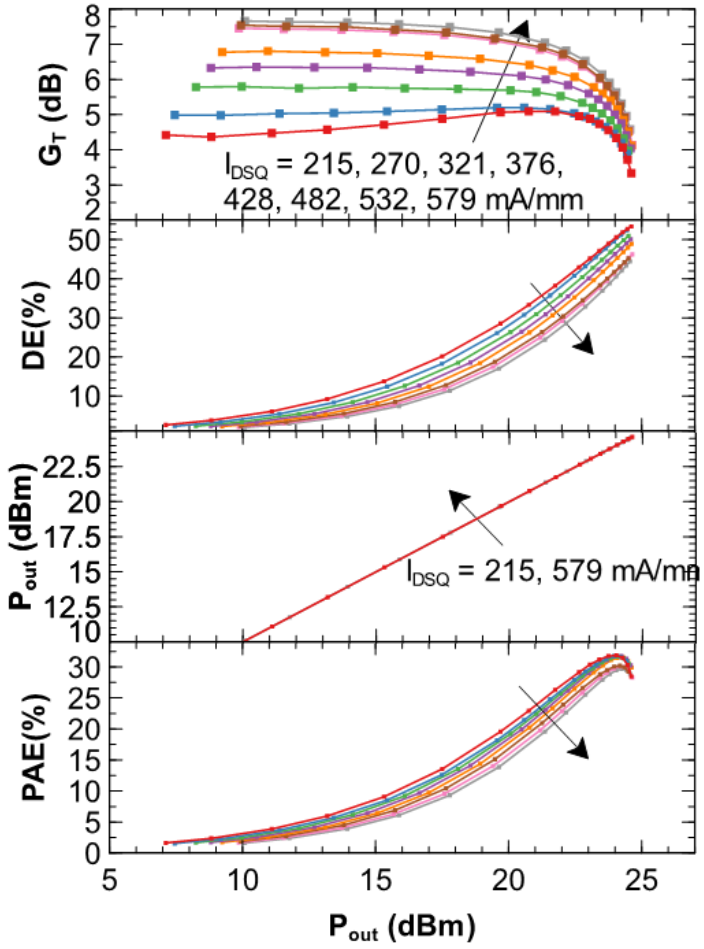


Figure 6.10 The 94 GHz load-pull power sweep measurements at different $I_{DS,Q}$ conditions (215, 270, 321, 376, 428, 482, 532, 579 mA/mm, with arrows showing the change from 215 mA/mm to 579 mA/mm) and fixed $V_{DS,Q}$ of 12 V. The results (a) G_T, (b) DE (%), (c) Pout and (d) PAE (%) are plotted against the output power P_{out}.

From **Fig. 6.10**, the G_T, Po, PAE and DE at different $I_{DS,Q}$ are taken at the output power level corresponding to the peak PAE and these data points are plotted in **Fig. 6.11**. The peak PAE generally increases as the $I_{DS,Q}$ decreases while the associated output power varies a bit. The maximum PAE of 31.9% happens at the low current density level of 215 mA/mm.

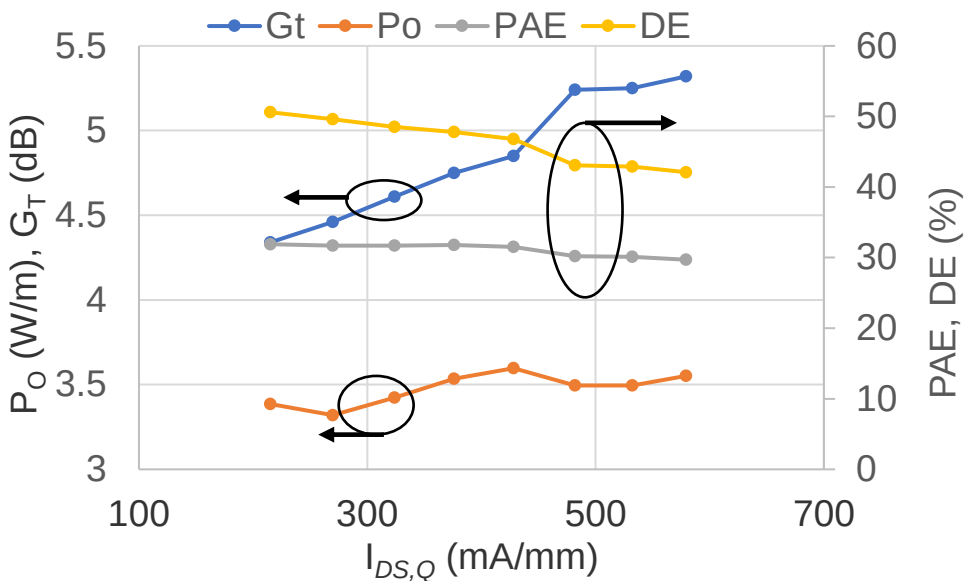


Figure 6.11 Impact of the $I_{DS,Q}$ on large signal performance for the device at 12 $V_{DS,Q}$. G_T, PO, PAE and DE are all taken at the P_{out} corresponding to the peak PAE in the power sweep.

Power sweep results, including the output power (P_{out}), transducer gain (G_T), PAE and drain efficiency (DE), for $V_{DS,Q}$ of 12V, and 16V are shown in **Fig. 6.12** (a) and (b). The device was biased at a quiescent current ($I_{DS,Q}$) of 267mA/mm in class AB operation. The $I_{DS,Q}$ of 267 mA/mm is selected to optimize the PAE through the tradeoff between the gain and the drain efficiency based as discussed before. The reason for not selecting 215 mA/mm or lower $I_{DS,Q}$ is due to the considerations on achieving peak output power density. In **Fig. 6.12** (a), at $V_{DS,Q}$ =12 V, a peak P_O of 3.92 W/mm was measured with an associated PAE of 28.0% and the peak PAE was up to 31.8% with an associated P_O of 3.31 W/mm. When the $V_{DS,Q}$ was increased to 16 V in **Fig. 6.12** (b), the output power density rose to 4.87 W/mm with an associated 27.1% PAE. The peak Po and peak PAE happened at different input power (P_{in}) levels. The key 94 GHz large signal power and PAE results with $V_{DS,Q}$ of 12V, 14V, and 16V are also summarized in **Table 6.1**, along with their maximum transducer gain ($G_{T,max}$).

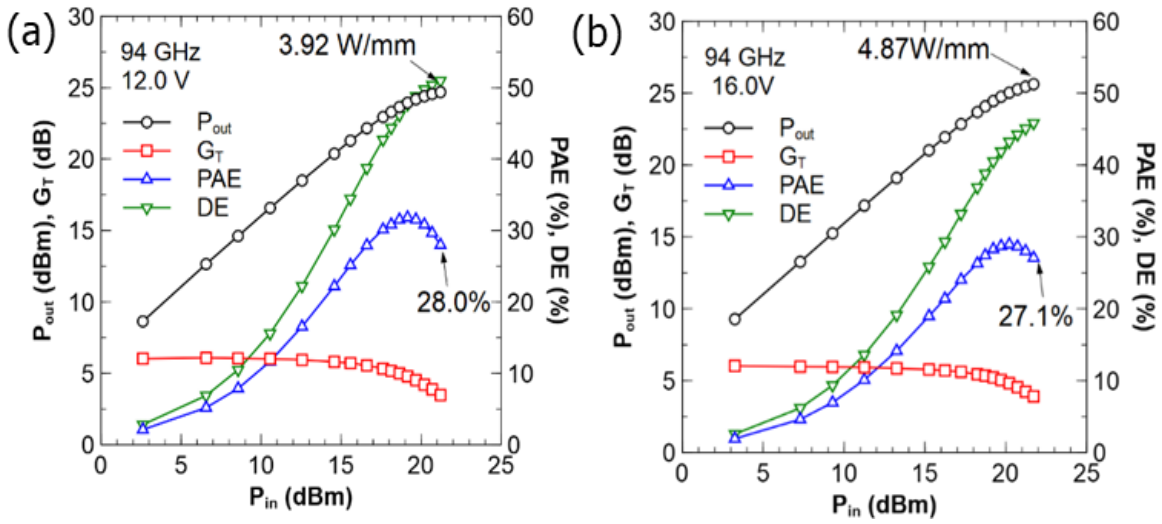


Figure 6.12 94 GHz load pull power sweep results with 267 mA/mm $I_{DS,Q}$ and $V_{DS,Q}$ of (a) 12 V and (b) 16 V.

Table 6.1 Summary of large signal results at 12 V, 14 V and 16 V.

$V_{DS,Q}$ (V)	$G_{T,max}$ (dB)	Peak P_O (W/mm)	Assoc. PAE (%)	Peak PAE (%)	Assoc. P_O (W/mm)
12	6.0	3.92	28.0	31.8	3.31
14	5.9	4.35	28.7	30.3	3.74
16	6.0	4.87	27.1	29.0	4.25

This N-polar GaN Schottky-HEMT targeting W-band performance was benchmarked in **Fig. 6.13** and demonstrating good performance. At W-band, this N-polar GaN Schottky-HEMT generally has better power performance than all the Ga-polar GaN HEMTs. Compared with the best N-polar GaN MIS-HEMTs, our Schottky device demonstrated slightly lower P_O and PAE at higher biases.

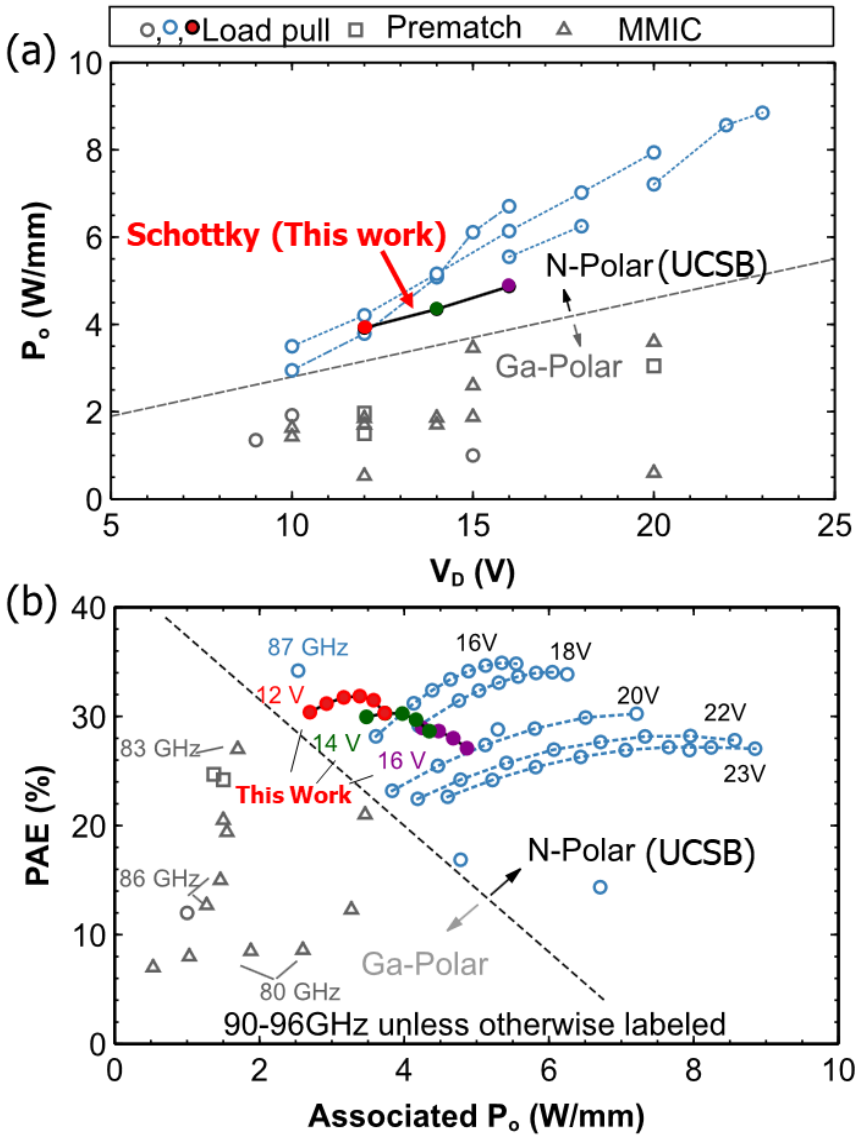


Figure 6.13 Benchmarking (a) the Po-V_D and (b) the PAE-associated P_O of this N-polar GaN Schottky-HEMTs work at $V_{DS,Q}$ = 12V (red solid), 14V (green solid), and 16V (purple solid) with the literature from [8,10] including N-polar MIS-HEMTs and Ga-polar HEMTs.

In **Fig. 6.13** (a), at the V_D of 12 V, the Schottky demonstrated similar power density as the N-polar GaN MIS-HEMTs, while the overall power and efficiency of the Schottky work are less at higher $V_{DS,Q}$. The lower output power density and PAE can be caused by the lower current density in the device and limited by the matching range in the load-pull measurement

system. With the demonstrated good vertical scaling in the Ru/N-polar GaN Schottky-HEMTs, further optimizing the epitaxy and scaling-down the gate length is anticipated to provide more output power density and better efficiency.

Load-pull result comparison between MIS-HEMT and Schottky-HEMT

While the N-polar GaN Schottky-HEMT demonstrated excellent improvement in g_m, there are many factors which can contribute to the reported large signal performance including the access region resistance, channel resistance, bias conditions, impedance matching, etc. Compared with the best output power density of 8.8 W/mm in prior MIS-HEMT in ref. [9], the power density of the Schottky HEMT is limited by the relatively high sheet resistance in the epi (278 Ω/ □ in Schottky-HEMT, 185 Ω/ □ in the MIS-HEMT) and the lower current density in the device. At the peak PAE condition and at $V_{DS,Q}$ of 16V, the comparison with the best PAE of 34% of another MIS-HEMT in ref. [10] is shown in **Table 6.2**. The average output current (I_{out}, unit: mA/mm) in the Schottky-HEMT work is lower and the transducer gain is lower. The lower output current can be caused by the high gate current (I_{in}, unit: mA/mm), which prevents the gate from forwarding bias further and providing more charge in the channel. The output characteristic in DC behavior (**Fig. 6.5** (**b**)) also shows higher on-resistance of 0.55 Ω/mm in the Schottky-HEMT while MIS-HEMT has 0.49 Ω/mm on-resistance at the same V_G of 1 V (**Fig. 5.12** (**b**)). Another factor is the matching of device in the 94 GHz load-pull system. For both MIS-HEMT and Schottky-HEMT, the load and source impedance are not perfectly matched due to the tuning range limit of our load-pull system [38]. The matching conditions for Schottky-HEMT is different from MIS-HEMT and the mismatch will be more significant because the current density is lower, and the ideal matched

impedance of load-line will be further out of the tuning range. The details of the comparison are shown in the **Table 6.2** below.

Table 6.2 Load-pull results comparison at the peak PAE between this Schottky-HEMT work and previous MIS-HEMT in Chapter 5 (Ch. 5) at $V_{DS,Q}$ of 16 V.

Device	**Γ_{source}**	**Γ_{load}**	***Gt*** ***dB***	V_{out} V	***I_{out}*** ***mA/mm***	V_{in} V	***I_{in}*** ***mA/mm***	*DE* *%*	Pout W/mm	PAE %
MIS Ch. 5	(-0.64, -0.18)	(-0.34, 0.50)	***5.29***	16.0	***674.1***	-3.20	***-0.0037***	*49.56*	5.35	34.9
Schottky (This work)	(-0.57, -0.39)	(-0.26, 0.56)	***4.82***	16.0	***613.9***	-0.90	***-7.1791***	*43.20*	4.25	29.0

6.6 Ru/AlGaN HEMT Results

In previous N-polar GaN Schottky HEMT structure with ALD Ru directly on the GaN channel, the gate leakage was around 3×10^{-4} A/mm at V_G = - 4V, which was relatively high compared to the leakage in diode structure and needed to be reduced. Here, a Schottky-HEMT structure using the AlGaN cap layer on the GaN channel to form a Schottky barrier with the ALD Ru is also investigated. The epi structure is the same as the one used in Ru/N-polar GaN Schottky HEMT in **Fig 6.2**. and device structure are shown in **Fig. 6.14**. The gate leakage was reduced to 2×10^{-5} A/mm at V_G = - 4V, which is more than one-order less than that in the Ru on GaN channel Schottky-HEMT. The N-polar GaN HEMT with Ru on AlGaN cap Schottky

gates with gate length (L_G) of 60 nm, showed PAE of 22.8% and P_O of 3.5 W/mm at 94 GHz and $V_{DS,Q}$ bias of 14V.

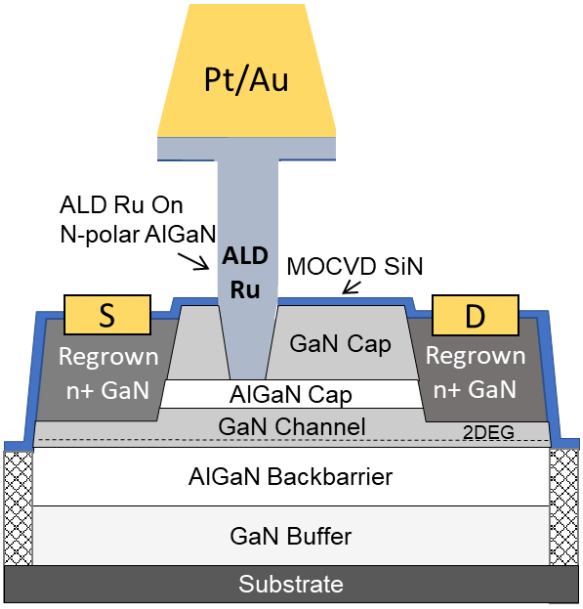


Figure 6.14 The N-polar GaN deep recess Schottky-HEMT device structure with ALD Ru on the AlGaN cap.

The reported devices have a source to drain spacing (L_{SD}) of 420 nm, a L_G of 60 nm and a gate to drain distance (L_{GD}) of 290 nm. The linear-scaled transfer characteristics are shown in **Fig. 6.15** (a), demonstrating a good peak extrinsic transconductance (g_m) of 602 mS/mm at V_{DS} of 3 V. In **Fig. 6.15** (b), the drain current (I_D) and gate current (I_G) are plotted in log-scale to compare the Ru on AlGaN cap Schottky-HEMT (Ru/AlGaN) here and the previous Ru on GaN (Ru/GaN) Schottky-HEMT with the same L_G, L_{SD} and L_{GD} dimensions. The gate current (I_G) of Ru/AlGaN is around 2×10^{-5} A/mm at V_G = - 4V, which is around one-order of magnitude less than previous Ru/GaN. The reduced gate leakage can be explained by the increased Schottky barrier height formed between AlGaN cap and ALD Ru.

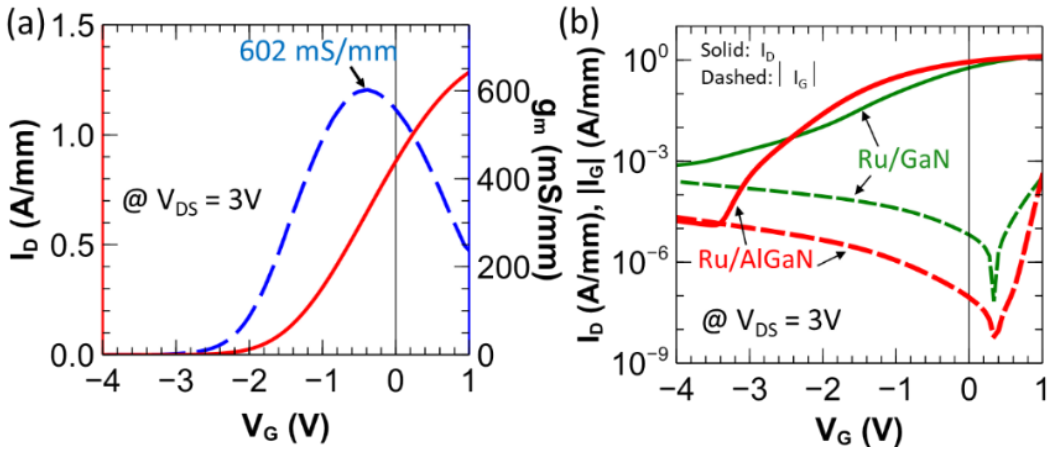


Figure 6.15 DC performance: (a) I_{DS}-V_{GS} with peak extrinsic g_m of 602 mS/mm at V_{DS} of 3 V; (b) I_D(solid lines), $|I_G|$(dashed lines)-V_G in semi-log scale at V_{DS} = 3 V, Ru/AlGaN in red lines compared with Ru/GaN in green lines.

The S-parameters were measured up to 67 GHz under different bias conditions. As shown in **Fig. 6.16** (a) and (b), the peak f_t occurred at V_{GS} = -0.5V and V_{DS} = 4V and was extrapolated to be 124 GHz via a 20 dB/decade slope from the unilateral gain U. The peak f_{max} was 245 GHz at V_{GS} = -0.5V and V_{DS} = 12V. The *ft/fmax* of 124GHz/245GHz is slightly less than that of 131GHz/262GHz in Ru/GaN, which is related to the addition of gate to channel distance from the AlGaN cap layer.

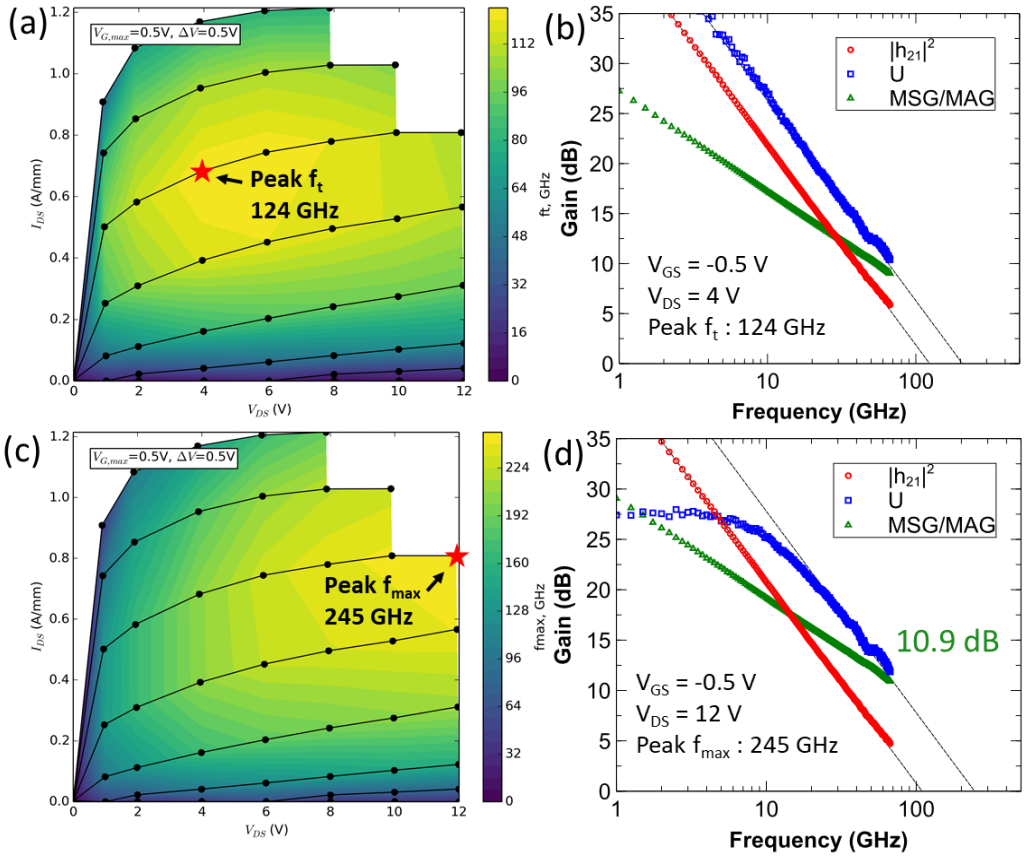


Figure 6.16 Small signal results for the device with L_{SD}-420 nm, L_G-60 nm, W_G-75 µm: (a) f_t contour with peak f_{max} at V_G= -0.5 V and V_D=4 V; (b) Gain-frequency at bias of peak f_t 124 GHz; (c) f_{max} contour with peak f_t at V_G= -0.5 V and V_D=12 V; (b) Gain-frequency at bias of peak f_{max} 245 GHz;

Early 94 GHz load pull measurements were conducted and the power sweep for $V_{DS,Q}$ 12V was presented in **Fig. 6.17**. The device was operated in class AB at quiescent drain current ($I_{DS,Q}$) of 500 mA/mm, which is the same as the bias conditions in N-polar MIS-HEMTs. Other bias conditions also gave similar large signal performance. A peak P_o of 3.2 W/mm was measured with an associated PAE of 22.8% while the peak PAE was 25.5%. Similar as the discussion in ALD Ru/N-polar GaN Schottky-HEMT case, optimizing the measurement

conditions and further scaling with the Ru on N-polar AlGaN Schottky-HEMTs are anticipated to provide more output power and better efficiency.

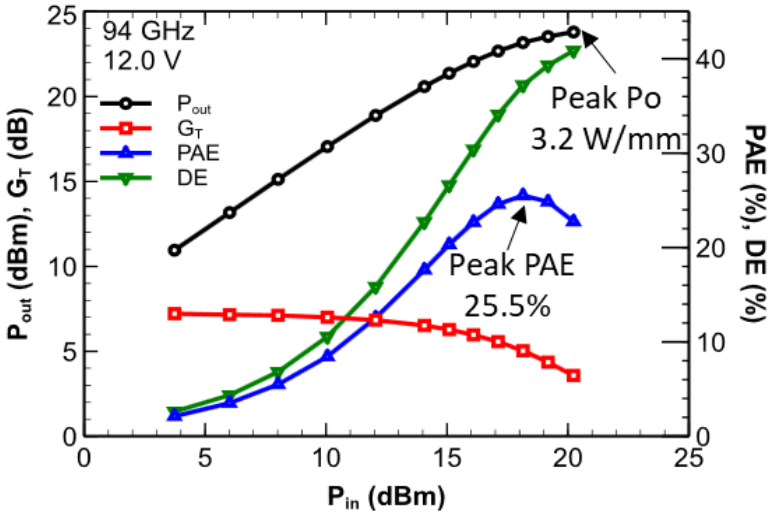


Figure 6.17 Load pull power sweep at 94 GHz with 500 mA/mm $I_{DS,Q}$ and $V_{DS,Q}$ of 12 V.

6.7 Summary

In this article, Ru/N-polar GaN Schottky-HEMT operating at W-band has been investigated and its good load pull power performance is reported. Even though the Schottky contact between Ru and the etched N-polar GaN, the fabricated Schottky HEMT with L_G of 60 nm has a peak extrinsic transconductance of 798 mS/mm and the gate leakage is around 3×10^{-4} A/mm. The Schottky-HEMT shows high PAE of 27.1% and P_O of 4.87 W/mm at 94 GHz $V_{DS,Q}$ = 16V. The measured peak PAE is 31.8% with associated P_O of 3.31 W/mm at $V_{DS,Q}$ = 12V. The Ru/N-polar GaN Schottky-HEMT demonstrated here can be optimized further and may provide an alternative path for N-polar GaN to be implemented in solid-state millimeter wave power amplifiers and circuits.

References

1. M. Wong, S. Keller, Nidhi, S. Dasgupta, D. J. Denninghoff, S. Kolluri, D. F. Brown, J. Lu, N. A. Fichtenbaum, E. Ahmadi, U. Singisetti, A. Chini, S. Rajan, S. P. Denbaars, J. S. Speck, and U. K. Mishra, "N-polar GaN epitaxy and high electron mobility transistors," *Semicond. Sci. Technol.,* vol. 28, p. 074009, Jun. 2013.

2. S. Keller, H. Li, M. Laurent, Y. Hu, N. Pfaff, J. Lu, D. F. Brown, N. A. Fichtenbaum, J. S. Speck, S. P. DenBaars, U. K. Mishra, "Recent progress in metal-organic chemical vapor deposition of $000\bar{1}$ N-polar group-III nitrides," *Semicond. Sci. Techol.,* vol. 29, no. 11, p. 113001, 2014.

3. M. H. Wong, Y. Pei, T. Palacios, L. Shen, A. Chakraborty, L. S. McCarthy, S. Keller, S. P. Denbaars, J. S. Speck, and U. K. Mishra, "Low nonalloyed ohmic contact resistance to nitride high electron mobility transistors using N-face growth," *Appl. Phys. Lett.,* vol. 91, p. 232103, Dec. 2007.

4. P. S. Park, D. N. Nath, and S. Rajan, "Quantum capacitance in N-polar GaN/AlGaN/GaN heterostructures," *IEEE Electron Device Lett.,* vol. 33, no. 7, pp. 991-993 Jul. 2012.

5. S. Rajan, A. Chini, M. H. Wong, J. S. Speck, and U. K. Mishra, "N-polar GaN/AlGaN/GaN high electron mobility transistors," *J. Appl. Phys.*, vol. 102, p. 044501, Aug. 2007.

6. S. Wienecke, B. Romanczyk, M. Guidry, H. Li, E. Ahmadi, K. Hestroffer, X. Zheng, S. Keller, and U. K. Mishra, "N-polar GaN cap MISHEMT with record power density exceeding 6.5 W/mm at 94 GHz," *IEEE Electron Device Lett.,* vol. 38, no. 3, pp. 359-362, Mar. 2017.

7. B. Romanczyk, M. Guidry, S. Wienecke, H. Li, E. Ahmadi, X. Zheng, S. Keller, U. K. Mishra, “Record 34.2% efficient mm-wave N-polar AlGaN/GaN MISHEMT at 87 GHz,” *Electron. Lett.,* vol. 52, no. 21, pp. 1813–1814, Oct. 2016.

8. B. Romanczyk, S. Wienecke, M. Guidry, H. Li, E. Ahmadi, X. Zheng, S. Keller, U. K. Mishra, “Demonstration of constant 8 W/mm power density at 10, 30, and 94 GHz in state-of-the-art millimeter-wave N-polar GaN MISHEMTs,” *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 45–50, Jan. 2018.

9. B. Romanczyk, X. Zheng, M. Guidry, H. Li, N. Hatui, C. Wurm, A. Krishna, E. Ahmadi, S. Keller, U. K. Mishra, “W-band power performance of SiN-passivated N-polar GaN deep recess HEMTs,” *IEEE Electron Device Lett.,* vol. 41, no. 3, pp. 349-352, Mar. 2020.

10. W. Liu, B. Romanczyk, M. Guidry, N. Hatui, C. Wurm, W. Li, P. Shrestha, X. Zheng, S. Keller, U. K. Mishra, “6.2 W/mm and Record 33.8% PAE at 94 GHz from N-Polar GaN Deep Recess MIS-HEMTs With ALD Ru Gates,” *IEEE Microwave Wireless Component Lett.,* vol. 31, no. 6, pp. 748-751, June 2021.

11. A. Margomenos, A. Kurdoghlian, M. Micovic, K. Shinohara, D. F. Brown, A. L. Corrion, H. P. Moyer, S. Burnham, D. C. Regan, R. M. Grabar, C. McGuire, M. D. Wetzel, R. Bowen, P. S. Chen, H. Y. Tai, A. Schmitz, H. Fung, A. Fung, and D. H. Chow, “GaN technology for E, W and G-band applications,” *Proc. IEEE CSICS*, La Jolla, CA, USA, Oct. 2014.

12. D. F. Brown, A. Williams, K. Shinohara, A. Kurdoghlian, I. Milosavljevic, P. Hashimoto, R. Grabar, S. Burnham, C. Butler, P. Willadsen, and M. Micovic, “W-band power performance of AlGaN/GaN DHFETs with regrown n+ GaN ohmic contacts by MBE,”

IEDM Tech. Dig., Washington, DC, USA, Dec. 2011.

13. Y. Niida, Y. Kamada, T. Ohki, S. Ozaki, K. Makiyama, Y. Minoura, N. Okamoto, M. Sato, K. Joshin, and K. Watanabe, "3.6 W/mm high power density W-band InAlGaN/GaN HEMT MMIC power amplifier," *Proc. IEEE PAWR*, Austin, TX, USA, pp. 24–26, Jan. 2016.

14. D. Marti, S. Tirelli, V. Teppati, L. Lugani, J.-F. Carlin, M. Malinverni, N. Grandjean, and C. R. Bolognesi, "94-GHz large-signal operation of AlInN/GaN highelectron-mobility transistors on silicon with regrown ohmic contacts," *IEEE Electron Device Lett.,* vol. 36, no. 1, pp. 17–19, Jan. 2015.

15. D. Xu, K. K. Chu, J. A. Diaz, M. Ashman, J. J. Komiak, L. M. Pleasant, C. Creamer, K. Nichols, K. H. G. Duh, P. M. Smith, P. C. Chao, L. Dong, and P. D. Ye, "0.1-μm atomic layer deposition Al2O3 passivated InAlN/GaN high electron-mobility transistors for E-band power amplifiers," *IEEE Electron Device Lett.*, vol. 36, no. 5, pp. 442–444, May 2015.

16. D. Schwantuschke, B.-J. Godejohann, S. Breuer, P. Bruckner, M. Mikulla, R. Quay, and O. Ambacher, "Broadband E-band power amplifier MMIC based on an AlGaN/GaN HEMT technology with 30 dBm output power," *Proc. IEEE CSICS*, pp. 1–4, Oct. 2016.

17. M. Micovic, A. Kurdoghlian, A. Margomenos, D. F. Brown, K. Shinohara, S. Burnham, I. Milosavljevic, R. Bowen, A. J. Williams, P. Hashimoto, R. Grabar, C. Butler, A. Schmitz, P. J. Willadsen, and D. H. Chow, "92–96 GHz GaN power amplifiers," *IEEE MTT-S Int. Microw. Symp. Dig.,* pp. 1–3, Jun. 2012.

18. E. Ture, P. Bruckner, M. Alsharef, R. Granzner, F. Schwierz, R. Quay, and O. Ambacher,

"First Demonstration of W-Band Tri-gate GaN-HEMT Power Amplifier MMIC with 30 dBm Output Power," *IEEE MTT-S International Microwave Symposium (IMS)*, pp. 35-37, June 2017.

19. D. Marti, L. Lugani, J. Carlin, M. Malinverni, N. Grandjean, and C. R. Bolognesi, "W-Band MMIC Amplifiers Based on AlInN/GaN HEMTs Grown on Silicon," *IEEE Electron Device Lett.,* vol. 37, no. 8, pp. 1025–1028, Aug. 2016.

20. K. Makiyama, S. Ozaki, N. Okamoto, T. Ohki, Y. Niida, Y. Kamada, K. Joshin, and K. Watanabe, "S5-H7: GaN-HEMT technology for high power millimeter-wave amplifier," *Proc. IEEE LEC*, Ithaca, NY, USA, pp. 1–4 Aug. 2014.

21. B. P. Downey, D. J. Meyer, D. S. Katzer, D. F. Storm, and S. C. Binari, "Electrical characterization of Schottky contacts to N-polar GaN," *Solid-State Electron.,* vol. 86, pp. 17-21, Aug. 2013.

22. T. Suemitsu, and I. Makabe, "Effective Schottky barrier height model for N-polar and Ga-polar GaN by polarization-induced surface charges with finite thickness," *Phys. Status. Solidi B*, vol. 257, no. 4, p. 1900528, Dec. 2019.

23. Y. Liu, S. Dogan, H. Morkoc, S. S. Park, and K. Y. Lee, "Effects of hydrostatic and uniaxial stress on the Schottky barrier heights of Ga-polarity and N-polarity n-GaN," *Appl. Phys. Lett.*, vol 84, no. 12, pp. 2112-2114, Mar. 2004.

24. U. Karrer, O. Ambacher, and M. Stutzmann, "Influence of crystal polarity on the properties of Pt/GaN Schottky diodes," *Appl. Phys. Lett.,* vol. 77, no. 13, pp. 2012-2014, Sep. 2000.

25. W. Liu, I. Sayed, B. Romanczyk, N. Hatui, M. Guidry, W. J. Mitchell, S. Keller, and U. K.

Mishra, “Ru/N-polar GaN Schottky diode with less than 2 □A/cm2 reverse current,” *IEEE Electron Device Lett.,* vol. 41, no. 10, pp 1468-1471, Oct. 2020.

26. W. Liu, I. Sayed, B. Romanczyk, N. Hatui, J. Georgieva, H. Li, S. Keller, and U. K. Mishra, “Near-ideal Ru/N-polar GaN Schottky diode with ultralow reverse leakage,” *Device Research Conference (DRC)*, June 2020.

27. B. Romanczyk, W. Li, M. Guidry, N. Hatui, A. Krishna, C. Wurm, S. Keller, U. K. Mishra, “N-Polar GaN-on-Sapphire Deep Recess HEMTs With High W-Band Power Density,” *IEEE Electron Device Lett.,* vol. 41, no. 11, pp 1633-1636, Nov. 2020.

28. L. Shen, R. Coffie, D. Buttari, S. Heikman, A. Chakraborty, A. Chini, S. Keller, S. P. DenBaars, and U. K. Mishra, “Unpassivated GaN/AlGaN/GaN power HEMTs with dispersion controlled by epitaxial layer design,” *Journal of Electronic Materials*, vol.33, no.5, pp.422-425, May 2004.

29. R. Chu, L. Shen, N. Fichtenbaum, Z. Chen, S. Keller, S. P. DenBaars, and U. K. Mishra, “Correalation between DC-RF dispersion and gate leakage in deeply recessed GaN/AlGaN/GaN HEMTs,” *IEEE Electron Device Lett.,* vol. 29, no. 4, pp 303-305, Mar. 2008.

30. D. Buttari, S. Heikman, S. Keller, and U. K. Mishra, “Digital etching for highly reproducible low damage gate recessing on AlGaN/GaN HEMTs.” *Proceedings IEEE Lester Eastman Conf. on High performance devices,* Newark, DE, USA, Aug. 2002.

31. T. Egawa, G. Zhao, H. Ishikawa, M. Umeno, and T. Jimbo, “Characterizations of recessed gate AlGaN/GaN HEMTs on sapphire,” *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 603–608, Mar. 2001.

32. S. Arulkumaran, T. Egawa, L. Selvaraj, and H. Ishikawa, “On the effects of gate-recess etching in current collapse of different cap layers grown AlGaN/GaN high-electron-mobility transistors,” *Japanese Journal of Applied Physics*, vol. 45, no. 8, pp. L220-L223, Feb 2006.

33. T. J. Anderson, M. J. Tadjer, M. A. Mastro, J. K. Hite, K. D. Hobart, C. R. Eddy, and F. J. Kub, “Characterization of Recessed-Gate AlGaN/GaN HEMTs as a Function of Etch Depth,” *Journal of Electronic Materials,* Vol. 39, No. 5, 2010.

34. H. Kim, M. Kang, J. J. Kim, K. Seo, and H. Cha, “Effects of recess-gate structure on AlGaN/GaN-on-SiC MIS-HEMTs with thin AlOxNy MIS gates,” *Materials*, 13, 1538, 2020.

35. Y. Zhang, S. Huang, et al., “Millimeter-wave AlGaN/GaN HEMTs with 43.6% power-added-efficiency at 40GHz fabricated by atomic layer etching gate recess.” *IEEE Electron Device Lett.,* vol. 41, no. 5, pp. 701-704, May. 2020.

36. M.C. A. Koolen, J. A. M. Geelen, and M. P.J. G. Versleijen, “An improved deembedding technique for on wafer high-frequency characterization,” *Proc. Bipolar Circuits Tech. Meeting*, Minneapolis, MN, USA, pp. 188-191, Sep. 1991.

37. B. Romanczyk et al., “W-band N-polar GaN MISHEMTs with high power and record 27.8% efficiency at 94 GHz,” *IEDM Tech. Dig.,* San Francisco, CA, USA, pp. 3.5.1–3.5.4, Dec. 2016.

38. M. Guidry et al., “W-band passive load pull system for on-wafer characterization of high power density N-polar GaN devices based on output match and drive power requirements vs. gate width,” *Proc. 87th ARFTG Microw. Meas. Conf.*, San Francisco, CA, USA, pp.

1–4, May 2016.

Chapter 7. Conclusions

To further boost the high-frequency and high-power performance in N-polar GaN HEMTs, the improvement on gate structure is critical. This dissertation is devoted to the evaluation of gate structures on N-polar GaN including MIS- and Schottky structures. Part of the evaluation is conducted through the MIS-capacitor and Schottky diode structures to understand the interface properties. Another part of the evaluation is in the form of N-polar GaN deep recess HEMTs to pursue high performance at 94 GHz.

A series of metal-insulator-semiconductor capacitors consisting of Si_3N_4 dielectric with different thicknesses on N-polar GaN have been fabricated to investigate their interface states. The measurement value extracted from ultraviolet assisted capacitance-voltage (UV-assisted CV) methods can be explained by the existence of spatially uniform hole traps in Si_3N_4. An improved model combining the effects from interface states and hole traps in Si_3N_4 is proposed to extract the interface state density (D_{it}) accurately. Based on the model, the D_{it} can be obtained by extrapolating the trap density to a zero-thickness dielectric. The extracted average D_{it} value of Si_3N_4/GaN interface is ~3.8×10^{11} cm^{-2} eV^{-1} and the hole trap concentration in Si_3N_4 is ~3.1×10^{18} cm^{-3}. The results, model and analysis presented here provide new insights into studying D_{it} of various dielectrics on GaN and other wide-bandgap semiconductors.

The bulk and interfacial properties of aluminum silicon oxide (AlSiO) on N-polar GaN were investigated systematically employing capacitance-voltage (C-V) methods on metal-oxide-semiconductor capacitors (MOSCAPs) using a thickness series of the AlSiO dielectric. The fixed charge density, electron slow trap density and electron fast trap density located near the interface were extracted to be -1.5×10^{12} cm^{-2}, 3.7×10^{11} cm^{-2} and 1.9×10^{11} cm^{-2},

respectively. Using ultraviolet (UV) assisted C-V methods, an average interface state density of ~4.4×10^{11} cm^{-2} eV^{-1} and a hole trap concentration in bulk AlSiO of ~8.4×10^{18} cm^{-3} were measured. The negative fixed interface charge makes it favorable to achieve a normally-off GaN transistor. The analysis presented in this chapter provides a systematic and quantitative model to study the properties of oxide dielectrics on wide bandgap (WBG) semiconductors, which can promote the development of MOS-based WBG semiconductor devices.

Schottky barrier diode of ruthenium (Ru) deposited by atomic layer deposition (ALD) on N-polar GaN is investigated. The Schottky diodes showed near-ideal thermionic current behavior under forward bias and reverse bias at various temperatures. The barrier height values extracted from both regions agreed well at each temperature and the barrier was extracted to be 0.77 eV at room temperature. The difference between the predicted barrier height (0.6 eV) and the experimental barrier heights (0.77eV) indicated the Schottky barrier height was enhanced by 0.17 eV. The combination of the 0.77 eV barrier and thermionic current characteristic resulted in < 2 $\mu A/cm^2$ reverse current at -5 V, which is a record-low value for N-polar GaN Schottky diodes.

ALD Ru gate has been adopted into the N-polar GaN deep recess MIS- and Schottky HEMTs. The ALD Ru effectively fills the narrow T-gate stems aiding realization of shorter gate lengths with lower gate resistance than in prior work. For the ALD Ru MIS-HEMTs, the gate length is scaled down to 48 nm resulting in the demonstration of a record-high 8.1 dB linear transducer gain measured at 94 GHz by load-pull. This increased gain has enabled a record 33.8% power-added efficiency (PAE) with an associated output power density (P_O) of 6.2 W/mm. The Ru/N-polar GaN Schottky-HEMT operating at W-band has also shown good large signal performance. The fabricated Schottky HEMT with L_G of 60 nm has a high peak

extrinsic transconductance of 798 mS/mm with a gate leakage in pinch-off below 3×10^{-4} A/mm at V_{DS} = 5V. The Schottky-HEMT shows high PAE of 27.1% and P_O of 4.87 W/mm at 94 GHz and $V_{DS,Q}$ = 16V. The peak PAE is 31.8% with associated P_O of 3.31 W/mm at $V_{DS,Q}$ = 12V.