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Publication Date
1989-09-01

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Presented at the International Conference on the Science and Technology of Defect Control in Semiconductors, Yokohama, Japan, September 17–22, 1989, and to be published in the Proceedings

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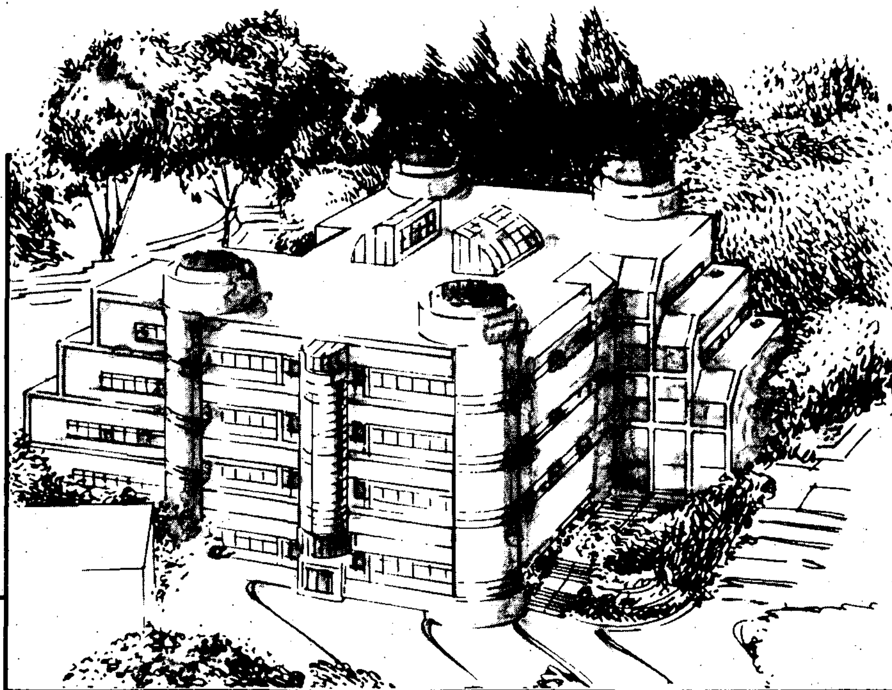

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Prepared for the U.S. Department of Energy under Contract DE-AC03-76SF00098

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Heteroepitaxy of GaAs on Si: Methods to Decrease the Defect Density in the Epilayer

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HETEROEPITAXY OF GaAs ON Si: METHODS TO DECREASE THE DEFECT DENSITY IN THE EPILAYER

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In this paper, the fundamental mechanisms of defects formation and procedures used to improve the structural quality of GaAs grown on Si are discussed. Patterned growth, strained-layer superlattices, and proper thermal cycling are promising approaches to help achieve high quality GaAs layers grown on Si substrates.

1.INTRODUCTION

Near-lattice matched heteroepitaxy is the fundamental growth process for all optoelectronic semiconductor devices and for the most advanced digital devices on III/V semiconductors, such as high-electron mobility transistors (HEMTs or MODFETs). However, the few binary substrates available as bulk crystals (mainly GaAs and InP), and the limited quality and small diameters of these materials, severely hamper the development of device technology. Therefore the possibility of growing high-quality lattice mismatched heteroepitaxy has attracted increasing interest in the last few years.[1] The most important systems of this kind are GaAs/Si, Ge/Si, InP/Si, and a wide variety of lattice mismatched ternary and quaternary heterostructures, including strained-layer superlattices.

Among these systems, GaAs/Si is the most promising and the most demanding. On the plus side, the opportunity to replace GaAs substrates with large-diameter, lightweight, fracture-resistant Si, and to integrate GaAs optoelectronic devices with Si digital logic is extremely promising. On the minus side, this system has to overcome all possible difficulties encountered in lattice mismatched heteroepitaxy: large mismatches in lattice constant, thermal-expansion coefficient, and elastic constants; high dislocation mobility in the epilayer; and the specific problems of polar-on-nonpolar growth and autodoping of the epilayer from the substrate. In the last few years, impressive progress in this field has been reported.[2,3] Dislocation densities around 10^7 cm^{-2} close to the range generally accepted in II/VI semiconductor devices, can be attained routinely. However, in order to achieve general utilization of GaAs/Si technology, it is not sufficient to demonstrate the feasibility of certain devices, though these breakthroughs are important milestones. A general application of GaAs requires a thorough understanding of the materials problems encountered. This understanding should help to decrease the defect density further by one to two orders of magnitude, and to decrease the residual strain by a factor of two, making GaAs/Si fully usable for optoelectronic and digital devices.

Therefore, this paper will concentrate on the GaAs/Si system. Many of the conclusions reached for this system can be applied for the cases of other lattice mismatched heteroepitaxy.

In the first part of this paper, the mechanisms responsible for defect formation will be discussed. In the second part the nature of the defects formed will be investigated, and the third part deals with attempts to further decrease the defect density.

2.ORIGIN OF DEFECTS IN LATTICE MISMATCHED HETEROEPITAXY

The failure to achieve device-quality GaAs/Si layers is generally attributed to the mismatch in lattice constant between epilayer and substrate. However, lattice mismatch itself does not need to be a severe problem, if it is possible to introduce a network of misfit dislocations at the interface that can balance the misfit strain. The high density of defects in the epilayer is due rather to the difficulty of introducing misfit dislocations without forming a high density of threading parts, which is connected to the problem of growing a highly strained layer in a two-dimensional mode. In addition, differences in the thermal-expansion coefficients of the epilayer and substrate, and the problem of growing a polar crystal on a nonpolar substrate, create additional difficulties. As a result of these problems, threading defects in the epilayer are formed during the growth process or during postgrowth cooling by propagation into the epilayer. This is clearly shown by the

width of the x-ray rocking curve, which is typically more than one order of magnitude broader than in GaAs/GaAs homoepitaxy [4] or GaAs/AlGaAs/GaAs near-lattice-matched heteroepitaxy. The dominant threading defects found propagating through the epilayer are dislocations, stacking faults, twins and antiphase boundaries.

2.1 Substrate Contamination

Our own observations [5] and those of others [6] lead to the conclusion that some impurities, such as oxides or carbides, are frequently left over on the Si surface despite application of elaborate cleaning procedures to the Si surface before GaAs deposition. Most of the commonly used substrate preparation treatments employ a high-temperature silicon reduction step [7]. Such a high-temperature process is frequently undesirable or impossible in a given growth system. Even after such a cleaning procedure, islands of impurities can still be observed. [5,6,8] Cross-sectional transmission electron microscopy (TEM) typically shows a white band at the interface between the GaAs and Si, which has frequently been attributed to artifacts of the TEM sample preparation. Our own investigation of metal/GaAs heterostructures deposited insitu in ultrahigh vacuum did not reveal a white band. Only air-exposed surfaces showed a white band at the interface [9,10]. In GaAs/Si heteroepitaxy, formation of this white band does not occur after application of a Ga reduction process as suggested by Kroemer [11,12], confirming that in most cases this white band indicates contamination at the heterointerface.

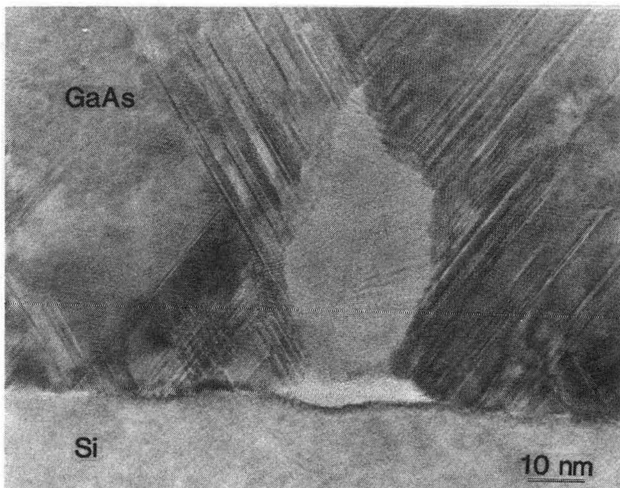

Fig. 1: High-resolution image of the GaAs on Si interface taken in <110> projection. Note that interface contamination is the source of polycrystallinity and other defects.

Additional defects such as stacking faults (Fig. 1) or antiphase boundaries can originate at irregularities caused by contamination at the substrate. In addition, impurities at the interface can be responsible for three-dimensional growth of GaAs on Si, as discussed in the next chapter.

2.2 Initial Growth

In idealized layer-by-layer growth (2d), the critical thickness for misfit dislocation formation is exceeded after only a few monolayers of growth.[13] Thus it could be possible to incorporate the corresponding density of 90° sessile misfit dislocations with a low density of threading arms. Such two-dimensional networks of misfit dislocations have indeed been observed, e.g., in the case of GaAsP on GaP.

TEM investigations of the initial growth of GaAs on an Si substrate show that three-dimensional growth (separate islands) is taking place instead of two dimensional growth. Islands elongated along <110> with {111} side faces is the dominant initial growth mode. It has been found that the critical thickness for misfit dislocation formation increases with decreasing lateral dimension of the islands, i.e. it should be possible to grow "towers" of mismatched material without any misfit dislocations.[14]

The reason for three-dimensional growth is not well understood yet. One of the reasons may be strain energy due to the 4% lattice mismatch between Si and GaAs [15]. However, investigation of early stages of growth of GaP on Si where the lattice mismatch is only 0.4% shows the same feature of separate island formation.[16] Theoretical calculations by Northrup[17] predict that under As-rich conditions, the equilibrium structure should consist of GaAs islands surrounded by a Si (100) 2x1: As terminated surface, and under Ga-rich conditions, GaAs islands should be surrounded by surface terminated by Ga-As dimers.

A new model based on total energy calculations[18] provides a description of growth on terraces and surface steps. The authors show the role of double-layer steps on the Si surface in initiating layered epitaxial growth of cubic GaAs. They conclude that growth of cubic zinc blende GaAs on flat regions of Si (100) is suppressed and that only a high-energy wurtzite structure can be grown on terraces under large inhomogenous strain. Step topology prevents mixing in the immediate neighborhood of the steps and promotes three-dimensional growth.

The 3d growth mode requires formation of misfit dislocations when the islands are already quite thick (10nm).

In this case, only 60° dislocations can glide to the heterointerfaces in the form of half-loops, leaving a high density of threading arms. A certain amount of 90° dislocations might be formed at the island's edge or upon island coalescence.

In this stage of growth, TEM examinations show a high density of stacking faults extended parallel to the {111} side faces of the islands. It is not yet clear if these stacking faults are formed during the growth as a result of misplaced atoms, as recently proposed[16], or if they represent dissociated 60° dislocations formed by glide of only one partial dislocation to the heterointerface upon exceeding the critical thickness, or whether they are formed during cooling, as a consequence of the different thermal expansion coefficient.[19]

2.3 Polar on Nonpolar Growth

The {100} surface of Si is generally reconstructed in (2x1) and (1x2), with a monoatomic step between these domains.[20] Growth of GaAs starts with a preferred interfacial bonding, mostly Si-As. Therefore such a two-domain substrate generally results in a two-domain epilayer, with an antiphase relation between the domains. Etching of the surface,[21] TEM cross-sectional analysis using convergent beam electron diffraction (CBED),[22] or dark-field imaging with (200) and (-200) reflections. can reveal the presence of antiphase domains (APDs).[23] Only the CBED analysis can determine directly the polarity of each domain on a microscale.[22] The density of APDs generally decreases with increasing layer thickness due to the annihilation of antiphase boundaries (APBs) during growth.

2.4 Different Thermal-Expansion Coefficients

Photoluminescence studies have shown that tensile strain is present in GaAs grown on Si, rather than compressive strain, as expected from the lattice mismatch between GaAs (5.653 Å) and Si (5.431 Å). We found that the density of misfit dislocations is related to the stress relief at the growth temperature and that this density is too large for the smaller lattice mismatch at room temperature[19]. The difference in thermal expansion coefficient ($\alpha_{GaAs} = 6.8 \times 10^{-6}/°C$, $\alpha_{Si} = 2.6 \times 10^{-6}/°C$) produces new strain during cooling from the growth temperature in opposition to the lattice-mismatch strain.[24] The tensile strain observed experimentally is considerably lower than the expected value 2.4×10^{-3}, indicating strain relief by plastic flow. Cooling from 600°C to only 400°C is sufficient to generate a biaxial tensile stress far above the experimentally determined critical resolved shear stress of 15 MPa at 400°C [25], resulting in the glide of additional threading dislocations of various types from the interface into the epilayer.

3. DEFECTS FORMED IN HETEROEPITAXIAL LAYERS

3.1 Misfit Dislocations

Dislocations in the diamond lattice have Burgers vectors **b** of a/2<110> and prefer line directions **u** along valleys of the Peierls potential in the <011> direction. Thus, two types of perfect misfit dislocations can be formed: edge dislocations with both **u** (e.g., [011]) and **b** (e.g., a/2[01-1]) in the (100) interface, or 60° dislocations with only **u** in the interface (e.g., [011]), but **b** of one of the four <110> directions inclined to the interface (e.g., a/2[101]). The first type of misfit dislocation in the interfacial plane is sessile, Lomer-type, as there exists no joint {111} glide plane containing both **u** and **b**. As **b** lies in the interface plane, maximum stress relief is obtained from this type of misfit dislocation. On the other hand, the second type of misfit dislocation can glide to (and from) the interface, as **u** and **b** lie on one of the inclined {111} planes ((11-1) in our example). Only the component of **b** in the interface orthogonal to **u**, i.e. in our example the component in the [01-1] direction, relieves the misfit strain (for **b** = a/2 [101]: a/4[01-1]), the length of which is 50% of the misfit Burgers vector of the first type of dislocation. In addition, the second type of misfit dislocation can dissociate in 90° and 30° partial dislocations according to:

a/2[101] --> a/6 [2-11] + a/6 [112],

forming a stacking fault on the (11-1) plane. It is interesting to note that one of the partials, which stays at the heterointerface, still removes 33% or 17%, respectively, of the misfit strain relief of the total 90° dislocation.[26]

In summary, three different types of misfit dislocations can be formed to remove lattice mismatch: 90° dislocation, 60° dislocation, and partial dislocations, the effectiveness of misfit strain relief decreasing in this order.

3.2 Threading dislocations

Threading dislocations can be formed as a result of the process of generating misfit dislocations at the heterointerface. In the simplest case, a half-loop glides from the surface to the interface, forming a 60° misfit dislocation. However, the threading arms cannot glide undisturbed

across a large distance; they will react with other threading arms and become immobile. In addition, island formation can also be the source of the increased number of threading dislocations. Although the island edge will first be beneficial in eliminating the threading arms, e.g. of dislocation half-loops, island coalescence might be the most important reason for the presence of a high threading dislocation density. Whenever misfit dislocations from two coalescing islands do not match up precisely, threading arms must be formed. It was shown experimentally that 60° dislocations are formed at the edges of such islands.[27]

In addition, 60° misfit dislocations are glissile on {111} planes inclined to the interface. Therefore they can easily propagate into the epilayer if a sufficient stress is present, e.g., upon cooling down.

3.3 Stacking Faults and Twins

Stacking faults and twins are major defects observed in heterolayers grown on Si. However, it is not clear if the stacking faults are formed during growth or cooling down. Pirouz[16] suggested that deposition errors in the early stages of film growth are responsible for generation of these defects. He argued that island growth and coarsening is taking place due to the energy difference between atomic sites at the surface of small and large nuclei. Coarsening leads to faceting on low energy planes. Deposition errors can be formed on {111} facets of islands. He assumed that the energy associated with misdeposited atomic layers is 50 % of the stacking-fault energy making the misdeposition energy per atom smaller than the average thermal energy.

In order to investigate the correlation between faceting and stacking fault formation, GaAs samples grown by MBE on the {110} GaAs substrate were studied by plan-view and cross-section TEM. Previous work [28] found high quality GaAs can be grown only on tilted GaAs (110) substrate, whereas growth on vicinal (110) results in a high faceted growth mode. The GaAs layer grown on vicinal {110} substrate shows faceting on the {111} planes (Fig.2a). However cross-section TEM performed on these samples does not reveal any stacking faults (Fig.2b). This experiment rules out Pirouz's prediction that facet growth leads to formation of growth errors such as stacking faults. Facet formation itself is not necessarily connected with stacking fault formation if there is no difference in lattice constant or thermal-expansion coefficient between the substrate and the layer.

Stacking faults might be formed during cooling down process from the growth temperature to the room temperature.

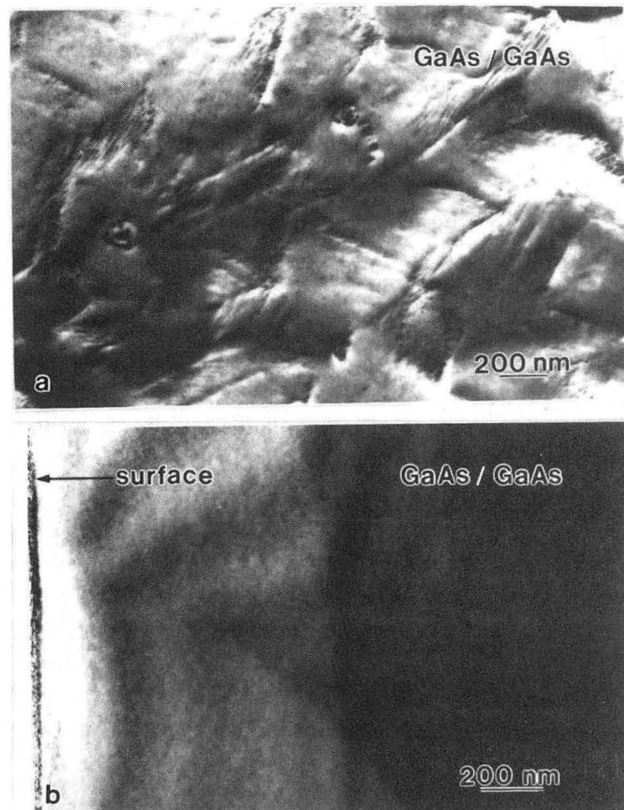

Fig. 2: a) Plan-view TEM micrograph showing facets formed in GaAs grown on vicinal (110) GaAs substrate, b) Cross-section TEM micrograph from the same sample. Note lack of stacking faults.

Misfit dislocations at the interface can be forced to dissociate on a {111} plane inclined to the interface, leaving one partial dislocation at the interface and forming an extended stacking fault. The formation of extended stacking faults by glide processes was first found in plastically deformed semiconductors cooled under high stress.[29,30] This model of a partial dislocation gliding from the interface during the cooling process and back down to the interface during annealing above the growth temperature can easily explain why stacking faults are so effectively eliminated during annealing process that it will be discussed in section 4.2. An alternative explanation to the formation of such planar defects can be their nucleation at the initial stage of growth for strain relief.[31]

Frequently stacking faults are found in a V shaped configuration. Such a configuration suggests stacking fault formation upon island coalescence. A misplacement mechanism, however, cannot explain V-shaped stacking faults observed experimentally in heterolayers. Grown-in

stacking faults within one island can only have a roof-shape (upside-down V) The stacking faults should be statistically distributed on both {111} planes visible in the [110] projection. The V shaped arrangement of stacking faults (shown in Figs.3 and 5) can be explained only by island coalescence or by semiconductor surface irregularities due to contamination.

3.4 Antiphase Boundaries

Polar on nonpolar growth is connected with the appearance of antiphase domains (APDs). Their appearance is most probably due to the presence of single steps at the Si surface and the preferred bonding of As with Si. The presence of single steps was observed by using many surface sensitive techniques[32] and it was confirmed by cross-sectional TEM.[33]

Such APDs are three-dimensional islands, and the boundaries (APBs) between these islands can be formed on low index as well as on high-index planes. Our own observations show that very often such boundaries macroscopically appear to be formed on various planes, for example, on {111} planes, although microscopically they consist of terraces of {110} APBs.[22] Formation of APBs on {110} planes would confirm Petroff's prediction that {110} and {112} APBs with alternating As-As and Ga-Ga bonds have the lowest energy of formation[34]

It has been reported that misorientation from the nominal (100) orientation by 2°-4° towards [011] direction leads to the disappearance of antiphase boundaries[35]. Our own observations show that, even for such misoriented substrates, antiphase domains can be found if the growth conditions are not optimized, preferentially in the areas close to the interface[36]. Many of these domains terminate inside the epilayer, so that only a small number of APBs extend to the surface. Drastic changes of the APD density are observed upon changing the growth parameters. After post-growth annealing, APD-free layers were found even on nominal (100) substrates.[21] The growth of APD-free GaAs is a major achievement, reached of last two years in GaAs heteroepitaxy.

4. METHODS TO DECREASE THE DEFECT DENSITY IN HETEROEPITAXIAL LAYERS

A very successful method for the growth of GaAs on Si is two-step growth in which an initial buffer layer ~100-300 Å thick is first grown at a low temperature (~400°C), and then growth is continued at ~650°C. The dislocation density decreases with layer thickness due to the interaction and annihilation of dislocations. Pearton et al[37] showed directly by x-ray rocking-curve analysis, the increase in crystalline quality with GaAs layer thickness. However, with increasing layer thickness, new problems occur with cracking, wafer bowing, and decreased energy dissipation through a thick GaAs layer during device operation. These problems limit the useful thickness of GaAs/Si to 2-3 μm.

4.1 Initial Growth: Buffer Layers

4.1.1 Low-Temperature Growth

It was found that the number of misfit dislocations is related to the stress relief at the growth temperature, and that this number is too high for the samples cooled to room temperature. This TEM observation is a confirmation of photoluminescence observations of tensile stress of GaAs on Si samples at room temperature, instead of the compressive stress that would have been expected based on the difference in lattice parameters of both materials.

In order to have fewer dislocations at the interface and stress-free layers at room temperature, one should lower the growth temperature. However, the results of growth at temperatures as low as 300°C showed (Fig.3) that, instead of decreasing the number of perfect dislocations the number of partial dislocations with stacking faults increases.[38] This would suggest that atom mobility at 300 °C is too low, and indeed, growth errors as suggested by Pirouz[16] can easily be formed.

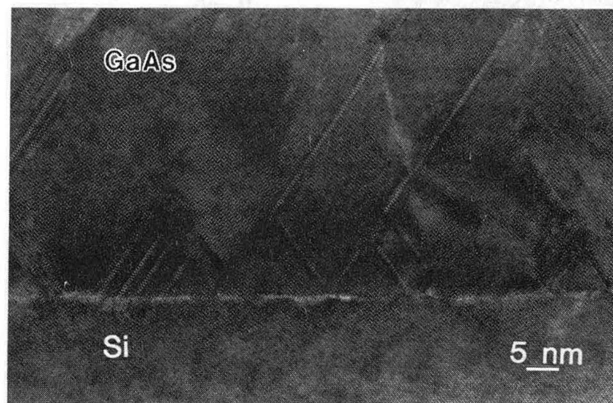

Fig. 3: High-resolution image of GaAs grown by MBE at 300°C on Si substrate. Note high density of partial dislocations with stacking faults formed in V-shape and lack of pure edge type misfit dislocations.

4.1.2 Two Dimensional Initial Growth

In order to decrease the density of threading defects, all efforts should be made to force the GaAs to grow two-dimensional. The application of migration-enhanced epitaxy (MEE)[39] to the growth of lattice-mismatched semiconductor systems has resulted in substantial improvements in the crystalline quality of heteroepitaxial films compared with conventional growth methods. The most important feature in MEE is its precise and independent control of the group III and V beam fluxes during growth. In MEE growth, the group III and group V beam fluxes were alternatively modulated by opening and closing the shutter of each effusion cell. In the case of GaAs growth, the absence of As molecules on the host substrate increases the surface mobility of the impinging Ga molecules, thereby increasing the surface-diffusion length of the Ga molecules.This enables a more two-dimensional growth mode. It also allows the deposited Ga and As molecules to achieve proper stoichiometry at much a lower substrate temperature than is possible with conventional MBE. Precise layer-by-layer growth has been demonstrated[39]

A modification of this method is modulated enhanced epitaxy[40] where only the As_4 beam flux is modulated (open and closed) and the Ga beam stays open all the time. Our TEM study of plan view samples shows Moire' fringes distributed uniformly over large areas of the sample (Fig.4).

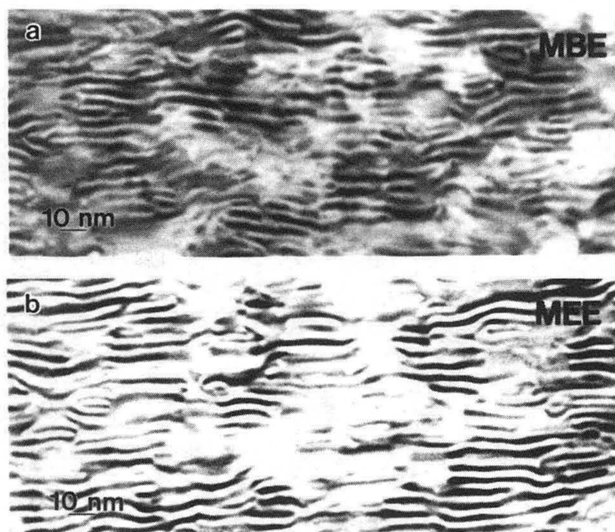

Fig. 4: Plan view micrograph showing Moire' fringes : a) in MBE grown GaAs on Si, b) in MEE grown GaAs on Si

Photoluminescence studies of these samples show very narrow lines. It was observed in these samples that the nucleation density increased and the spacings between the nucleated islands decreased This led to the formation of many V-shaped double stacking faults with partial dislocations, which can interact, leaving perfect dislocation at the interface (Fig.5).

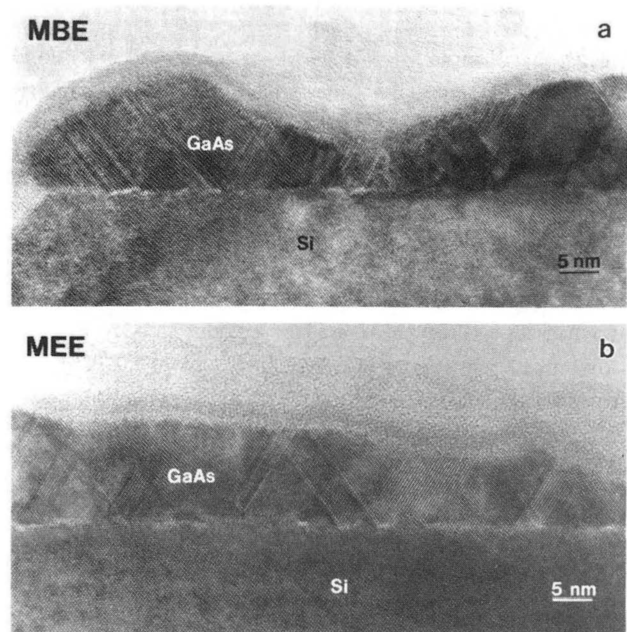

Fig. 5: High-resolution TEM of cross-section samples shown in Fig. 4.

It was also reported that low As_4 overpressure (7As : 1Ga) during initial growth leads to flat islands[41]. It was estimated that a continuous film was formed at around 100 Å in the low As_4 pressure case and at around 500 Å in the high As_4 pressure case.

Another promising method for increasing two dimensional growth is to start with a lattice-mismatched system such as AlGaP, which provides very good wetting. Umeno's group first reported the role of Al during the growth of GaP on Si.[42,43] The addition of small amounts of Al causes perfect two-dimensional growth (Fig.6). This might be due to the high affinity of Al for oxide formation, allowing Al compounds to grow on both clean and contaminated surfaces.[42]

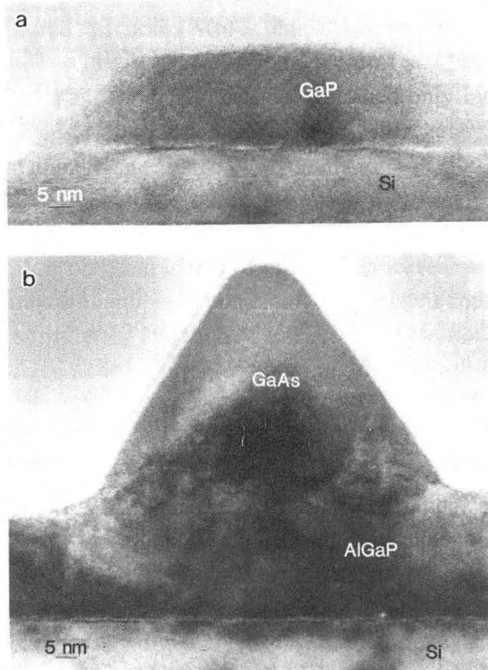

Fig. 6: a) Island growth of GaP on Si. b) Two-dimensional growth occurs after adding Al to GaP. Note island growth of GaAs on Al GaP.

4.2 Thermal Treatments

4.2.1 Conventional Post-growth Annealing

If the heteroepitaxial layer is grown strain-free with the correct density of misfit dislocations at the interface, any change in temperature will induce strain, the sign and magnitude of which depends on the difference between growth temperature and annealing temperature. Thus it is possible to move dislocations by thermal cycling during or after the growth. It was reported that annealing at 850°C under arsenic overpressure results in dislocation rearrangement at the interface forming a majority of Lomer type dislocations and decreasing the number of stacking faults.[44,45] Our own observations do not confirm these results fully. Furnace annealing at 800°C for 10 min changed the defect rearrangement only slightly. The dislocation density remains in the same range as that for as-grown samples, but the dislocations are more tangled. A slight decrease in stacking fault density was observed. This discrepancy can indicate a strong dependence on the detailed annealing conditions, requiring careful optimization.

4.2.2 Rapid Thermal Annealing

Noticeable improvements in the quality of GaAs/Si epilayers grown by MBE were observed after rapid thermal annealing (RTA) at 800°C for 10 sec by the capless close-proximity method in a commercial heatpulse furnace. The density of stacking faults after this treatment was very low (Fig.7), possibly because of the different cooling rate compared to furnace annealing. Partial dislocations mobilized during annealing could glide back to the interface to recombine with the second partial. During rapid cooling they were "frozen" in this state and did not dissociate again into partials. This mechanism is beneficial for the removal of stacking faults but prohibits stress relief during cooling, as evidenced by cracking of the GaAs epilayers that experienced RTA. Cracking was even more severe than in as-grown samples. The heterointerface was observed to be more undulated after RTA, compared to as-deposited samples. Independent electrical measurements of devices after RTA[46] showed a noticeable improvement for forward and reverse bias characteristics. Leakage currents were reduced by more than two orders of magnitude after this treatment.

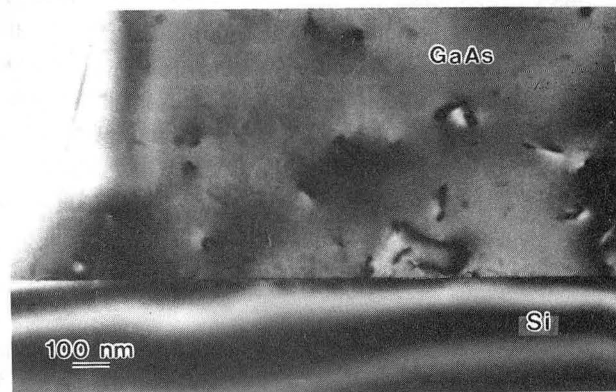

Fig. 7: TEM cross-section of GaAs on Si after rapid thermal annealing. Note lack of stacking faults after such annealing.

4.2.3. Thermal Cycling During Growth

It was reported that *insitu* annealing at 800°C for 5 min during growth is more efficient in defect reduction than *exsitu* annealing[47]. *Insitu* annealing causes visible dislocation bending, providing a better chance for threading dislocations to interact and, ideally, to move to the periphery of the wafer. After this treatment the dislocations density was reduced to 2 x 10^7/cm.[2]

Yamaguchi et al.[48,49] carried out a very successful systematic study of thermal treatments during MOCVD growth. It involved thermal cycling during growth in which annihilation and coalescence of dislocations were caused by dislocation movement under the alternating thermal stress. The growth GaAs was interrupted several times, and the substrate temperature was lowered to room temperature, followed by a temperature increase up to 900°C and subsequent annealing for up to 15 min at this temperature in an arsine atmosphere. After this treatment, the substrate temperature was again lowered to 700°C, and a new layer of GaAs was grown in the same fashion. This process was repeated several times. The reported dislocation density for GaAs grown on Si with this thermal cycling was estimated from the etch-pit density to be as low as $1\text{-}2 \times 10^6/cm^2$. Such thermal cycling during growth appears to be a very promising approach for decreasing the defect density in the heterolayer.

4.3 Patterned Growth

The goal of growing a lattice-mismatch heteroepilayer with a network of misfit dislocations confined to the interface and no threading dislocations in the epilayer is difficult to achieve for a homogeneous 3" wafer. It would require the threading "arms" of misfit dislocations to glide across the whole wafer without being blocked by other threading dislocations. However, it appears to be much easier to achieve this goal if the growth area is confined to a small part of the substrate, e.g., by patterning lines or mesas on the substrate.[14]

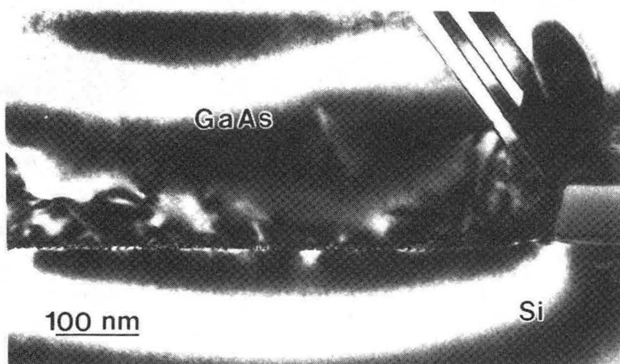

Fig. 8: Cross-section TEM micrograph near the patterned boundary. Note stacking faults present at the boundary with polycrystalline material grown over SiN and very low density of defects within the stripe of 100nm width GaAs.

One example of patterned growth is the growth of GaAs on Si through openings in an oxide or nitride[50-52]. Our own results[53] show that GaAs grown above the SiN mask was polycrystalline, but in the open areas where the nitride was removed, monocrystalline GaAs was detected with a much lower dislocation density than is found in the typical two-step growth (Fig. 8). The stacking fault density was much lower in the entire pattern, increasing only at the border with nitride. This decrease in defect density is probably connected with the stress release at the periphery of the patterns in polycrystalline areas. Post-growth annealing at 850°C in arsenic overpressure results in significant grain growth in the remaining polycrystalline GaAs overgrown on the amorphous areas such as oxides or nitrides, and the elimination of defects at the transition region from polycrystalline to single-crystal growth. An increase of Hall mobility of 30% was observed in these annealed samples. Fitzgerald et al.[14] proposed patterned growth by growing a lattice-mismatch $In_{0.05}Ga_{0.95}As$ layers on free-standing mesa structures of GaAs (2μm high, with diameters 60nm and larger). Only misfit dislocations were observed in these structures. The epilayer was dislocation-free, and no threading dislocations were detected by cathodoluminescence in these structures. This method may also be useful in the growth of GaAs on Si substrates; however, particular design patterns should be tested in order to determine if the result is compatible with device applications.

4.4 Strained-Layer Superlattices

As mentioned before, in order to obtain device quality epitaxial GaAs material, a reliable method for suppressing defect propagation in the epilayer is necessary. One promising method is the use of strained-layer superlattices (SLSLs), which cause dislocations to bend into the strained interface, thus promoting dislocation interactions. It was reported[12] that by application of SLSLs of InGaAs/GaAs with 10-nm-thick periods grown on Si (211), blocking of dislocation propagation did not occur at all interfaces inside the SLSLs but occurred almost entirely at the uppermost interface between the strained layers and the final GaAs layer (Fig.9). It was concluded that reduction of dislocation density was only weakly dependent on the period number of the strained-layer superlattices. InGaAs/GaAs strained-layer superlattices proved to be more efficient in dislocation bending than InGaAs/InGaP SLSLs. Because it was recognized that the period number did not influence the

reduction of dislocation propagation and that the upper interface of SLSLs is most efficient in dislocation bending, packages consisting of five periods of SLSLs (InGaAs/GaAs) were applied. Indeed, each set of SLSLs caused additional dislocation bending, but in some areas additional dislocations were formed at the lower interface between the buffer layer and the SLSL[12] Therefore, in some areas the dislocation density was slightly higher. However, on the average, the dislocation density in this sample was in the ~$2 \times 10^7/cm^2$ range, which is very low, taking into account the fact that all misfit dislocations in GaAs grown on Si(211) are 60° dislocations with Burgers vector inclined to the interface.

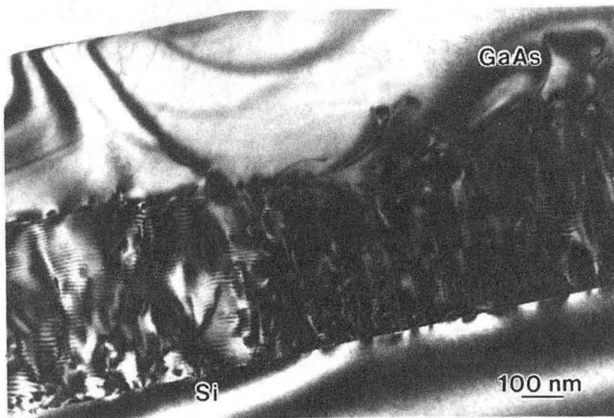

Fig. 9: TEM cross-section micrograph of the GaAs/Si interface with 50 periods of $In_{0.25}Ga_{0.75}As$/GaAs SLSL grown directly at the interface with Si. Note the large number of stacking faults formed at the interface, propagating through the SLSL and stoping at the last interface with epilayer of GaAs. Bending of dislocations was most effective at this interface as well.

Similar behavior was found with MOCVD-grown GaAs/GaAsP SLSLs[54]. In this case, it could be shown that the same effect of dislocation bending into the strained interface could be achieved by growing 1000 Å-thick strained layers of GaAsP instead of growing SLSL packages. Lattice-matched AlGaAs/GaAs layers were found[12] to have no distinct effect on dislocation propagation. These observations allow one to draw some conclusions about the interaction mechanism of strained-layer superlattices with dislocations. A package of SLSLs with periods on the order of 20 nm interacts with dislocations in a manner similar to a single strained layer whose thickness equals the total thickness of the SLSL package. For such short periods of SLSLs, only the strain due to the deviation of the average lattice constant inside the SLSL from the surrounding material is relevant to the dislocation interaction. Thus "symmetrical" SLSLs of the InGaAs/GaAsP type in GaAs are relatively ineffective. This important conclusion can be easily understood by the long-range nature of the dislocation strain field.The optimum lattice constant and strain level should be determined by the following considerations. On one hand, the strain needs to be large enough to efficiently induce dislocation bending; i.e., each strained layer should exceed the critical thickness for strain relaxation by the formation of interfacial misfit dislocations. On the other hand, the amount of strain should not be too large, or the threading dislocation density may not be high enough to form the required density of misfit dislocations at the strained interface. If the strain is larger than the value obtained from these considerations, new dislocations will be formed for strain relief when the layer exceeds a second critical thickness, as pointed out by Yamaguchi.[55]

5.CONCLUSIONS

This report on the mechanisms used to reduce the density of structural defects in the heteroepitaxial growth of GaAs on Si leads to the promising conclusion that such growth is possible and that higher qualities of epilayers can be obtained. The first step, the controlled growth of antiphase domain-free GaAs/Si, has been achieved. The cleaning of the Si substrate has been improved, but is not yet satisfactory. Of special interest should be approaches avoiding the high temperature substrate annealing steps currently used. Such high annealing temperatures result in roughening of the Si surface and are generally incompatible with patterned epitaxy. A promising approach is the use of Ga reduction and/or the growth of ternary, Al-containing buffer layers, as pioneered by Umeno's group.[42,43]

Further defect-reduction strategies, such as thermal cycling during growth, post-growth annealing, and the use of strained-layer superlattices, have to be optimized. The combined use of some of these methods, together with the possibilities of patterned epitaxy appear to make high-quality growth of lattice-mismatched heterostructures such as GaAs/Si achievable. Only such optimized low-defect material will allow one to make practical use of the numerous devices possible with this technology, including minority carrier devices, the feasibility of which already has been demonstrated in GaAs/Si heteroepitaxy.

ACKNOWLEDGMENT

The authors would like to acknowledge their ongoing collaborations in this field with T. George and H. Lee from UC Berkeley, R. Mariella from Lawrence Livermore Laboratory, S. Nozaki from INTEL and M. Umeno from Nagoya University. This work was supported by the Director, Office of Energy Research, Office of Basic Energy Sciences, Materials Science Division of the U. S. Department of Energy under Contract No. DEACO3-76SF00098. Use of the electron microscopes at the National Center for Electron Microscopy of Lawrence Berkeley Laboratory is acknowledged.

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