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Simultaneous synthesis and integration of two-dimensional electronic components

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Two-dimensional (2D) materials such as transition metal chalcogenides can be used to create different components of electronic devices, including semiconducting channels and metallic electrodes and interconnects. However, devices are typically fabricated using a step-by-step process that can introduce defects and impurities, leading to a reduction in device performance. Here we show that 2D electronic components can be chemically synthesized and integrated simultaneously in a single step, creating 2D devices in which each component in the active layer is connected via covalent bonds instead of physical interfaces. The approach involves the phase-patterned growth of atomic layers, and, using 2D molybdenum ditelluride ($MoTe_2$) as the active material, we show that it can be used to construct high-performance field-effect transistors (FETs) and arrays of logic devices. We also use the technique to construct FETs with ultrashort gate lengths, bilayered FETs with vertical interconnections and flexible devices.

Over the past few decades the complexity of integrated circuits based on silicon metal–oxide–semiconductor field-effect transistors (MOSFETs) has increased dramatically as the number of components in a circuit has increased according to Moore's law[1]. However, as the dimensions of MOSFETs approach their thermal and quantum limits, further scaling of the devices is becoming increasingly difficult and costly[2,3]. As a result, considerable effort has been exerted in exploring the potential of low-dimensional electronic materials (for example, nanowires[4], carbon nanotubes (CNTs)[5] and two-dimensional (2D) materials[6]) as building blocks for constructing smaller devices[7–12]. Monolayer and few-layer MoS_2 has, for example, been theoretically predicted to be superior to silicon at the sub-5 nm scaling limit, and ultrashort MoS_2 FETs with a 1 nm physical gate length have been shown experimentally to exhibit excellent switching characteristics[8]. However, as there are only a few atoms in the vertical dimension of these ultrathin materials, it is very easy to introduce defects and impurities into them when using conventional device fabrication processes, which leads to degradation in device performance. Therefore, developing new device manufacturing strategies that are specifically designed for 2D semiconductors is essential, and a key challenge is integrating individual 2D devices into circuits.

In this Article, we propose a non-destructive strategy for building integrated circuits based on 2D materials and demonstrate the potential of this approach using ultrathin $MoTe_2$ as the active material. In contrast to the step-by-step fabrication of components used in conventional techniques (Fig. 1a), we construct and integrate ultrathin channels, contacts and interconnects simultaneously via a one-step chemical synthesis, creating circuits where all these components are connected through covalent bonds instead of physical interfaces (Fig. 1b). This one-step and one-piece construction strategy can significantly reduce contact barriers and interfacial impurities compared with traditional approaches to the fabrication

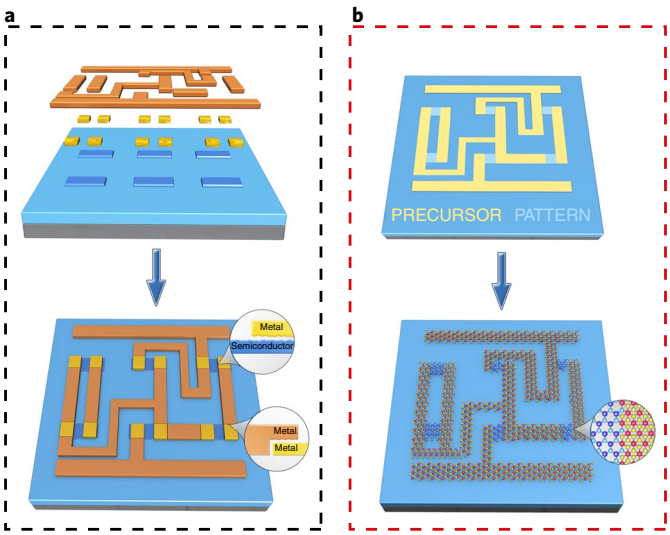

Fig. 1 | Comparison of our proposed circuit construction approach with a traditional approach. a, Traditional circuit fabrication via step-by-step construction of the channels, contacts and interconnects. Components are contacted physically with a lot of interfaces. **b**, Our approach for constructing ultrathin circuits by simultaneously synthesizing and integrating electronic components. Precursors are first patterned into desired structures according to the device design, followed by a single-step phase-controlled chemical synthesis. The predesigned precursor pattern is converted into an integrated circuit where the semiconducting phase is used as channels and the metallic phase serves as source–drain electrodes and interconnects. All these components are connected through covalent bonds.

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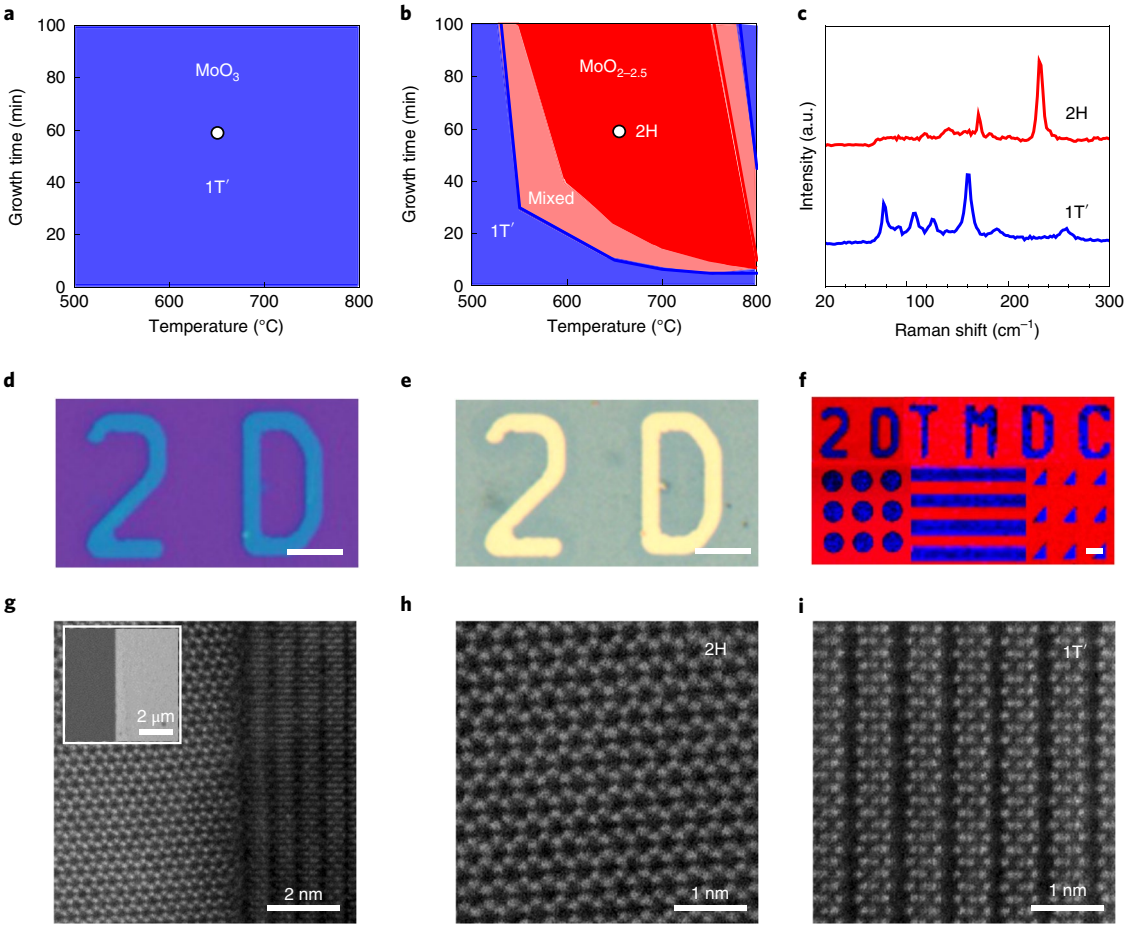

Fig. 2 | Characterizations of 2H/1T′ $MoTe_2$ heterophase junctions. a,**b**, Phase diagram of the phase evolution of CVD-grown $MoTe_2$ thin film as a function of tellurization temperature and duration utilizing MoO_3 (**a**) and $MoO_{2-2.5}$ (**b**) as precursor. Note that the phase states of products are determined via Raman spectroscopy. The white dots indicate the condition used for the synthesis of 1T′ and 2H heterophase patterns in this work. **c**, Typical Raman spectra of 2H and 1T′ $MoTe_2$. **d**, Optical image of the MoO_x pattern, in which the '2D' pattern is MoO_3 and the background is $MoO_{2.0-2.5}$. **e**, Optical image of the $MoTe_2$ heterophase pattern after tellurizing the oxide pattern shown in **d**. '2D' is converted to the 1T′ phase and the background is tellurized to the 2H phase. **f**, Raman mapping images of the heterophase pattern with 231 cm^{-1} (E_{2g} mode of 2H $MoTe_2$, red) and 160 cm^{-1} (A_g mode of 1T′ $MoTe_2$, blue) peak intensities. In **d**–**f**, scale bars, 5 μm. **g**, Typical STEM image of an atomically straight boundary of 2H/1T′ $MoTe_2$. Inset: large-scale SEM image of the heterophase structures. The other kind of boundary is shown in Supplementary Fig. 10. **h**,**i**, STEM images of 2H (**h**) and 1T′ (**i**) $MoTe_2$ near the boundary.

of 2D devices. It therefore provides a new approach for building high-performance devices based on 2D materials. To illustrate the potential of the method, we use it to construct FETs with ultrashort gate lengths, bilayered transistors with vertical interconnections and flexible devices.

Patterned synthesis of $MoTe_2$ heterophase junction

Due to their diverse compositions and properties, a large variety of 2D transition metal chalcogenides (TMDCs) can potentially serve as semiconducting channels (including n-type 2H MoS_2, $MoSe_2$ and p-type 2H $MoTe_2$, WSe_2) and metallic electrodes and interconnects (including 1T/1T′ $MoTe_2$, WTe_2 and VSe_2) to create functional devices[13–15]. Individual FETs built through the random connection of metallic TMDCs and semiconducting TMDCs by sequential growth have demonstrated improved contacts compared with metal-contacted FETs[12]. However, the construction of integrated circuits based on these 2D TMDCs remains a challenge because the semiconducting and metallic elements need to be assembled into complicated architectures in order to form functional circuits. To address this, we simultaneously produce channels, contacts and interconnects and sew these components into well-organized architectures for functional devices through the patterned growth of heterophase 2D $MoTe_2$.

We chose 2D $MoTe_2$ as the active material as it can provide both semiconducting and metallic components by tuning its structure to the hexagonal or monoclinic phase, respectively (Supplementary Fig. 1). In light of theoretical predictions that the concentration of Te monovacancies can invert the thermodynamic stability of these two phases[11], we tellurized $MoO_{2.0-2.5}$ and MoO_3 thin films at 650 °C to produce $MoTe_2$ with varied defect densities (Supplementary Methods) and obtained 2H and 1T′ $MoTe_2$, respectively, according to the phase evolution of $MoTe_2$ thin film as a function of tellurization temperature and duration (Fig. 2a,b). More details on the mechanism of phase-selective growth and characterizations are provided in Supplementary Figs. 2–7.

As the thin-film precursors for the phase-selective growth of $MoTe_2$ can be patterned into desired architectures via standard lithographic processes, we achieved the simultaneous growth of 2H and 1T′ $MoTe_2$ into predesigned patterns (Fig. 2d,e). The obtained $MoTe_2$ patterns with the heterophase structure are clearly displayed in Raman mapping images (Fig. 2f) as 2H $MoTe_2$ exhibits two Raman modes at ~171 cm^{-1} (A_g mode) and ~231 cm^{-1} (E_{2g} mode), whereas

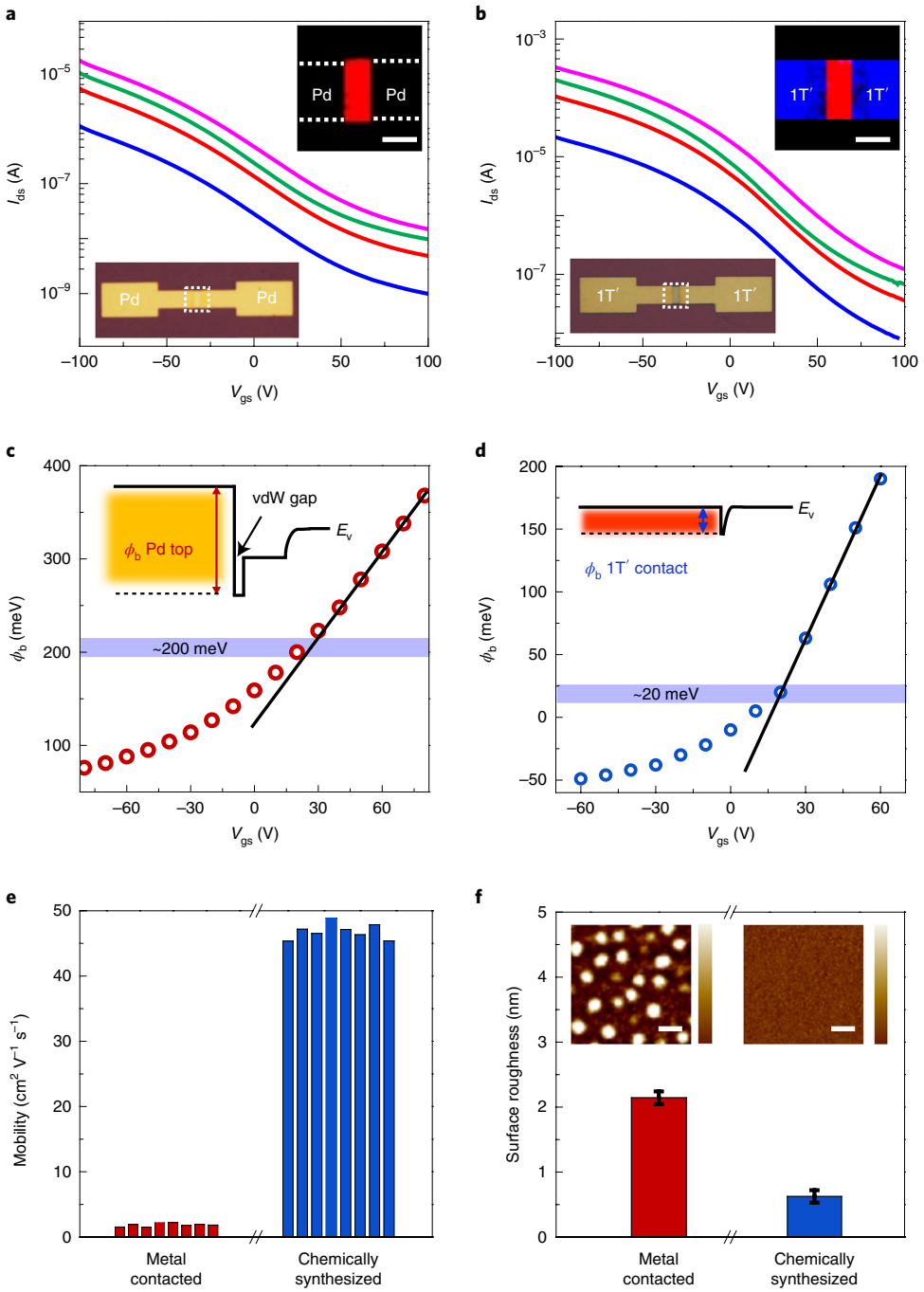

Fig. 3 | Comparisons of the electrical performances of chemically synthesized FETs and traditional fabricated FETs. a,**b**, Typical I_{ds}–V_{gs} curves for $MoTe_2$ FETs with a Pd contact (**a**) and a 1T′ contact (**b**) measured at various bias voltages. The bias voltages for the curves are 1.5, 1, 0.5 and 0.1 V from top to bottom. Insets: optical images (lower) and Raman mapping images (upper) for the two FETs. Scale bars, 5 μm. Note that the overlapped regions were tellurized into 1T′ $MoTe_2$ rather than 1T′/2H vertical stacks (Supplementary Fig. 11g,h). **c**,**d**, Barrier heights (Φ_b) measured at different gate voltages for FETs with a Pd contact (**c**) and a 1T′ contact (**d**). The lavender bands represent the estimated Schottky barrier height. Insets: energy band diagrams for Pd (**c**) and 1T′ (**d**) contacts to 2H $MoTe_2$ layers. vdW, van der Waals. **e**, Statistics of mobility measured at V_{ds} = 1 V in Pd-contacted FETs (red columns) and chemically synthesized FETs (blue columns). **f**, Surface roughness of the $MoTe_2$ channels in Pd-contacted (red column) and chemically synthesized (blue column) devices. Error bars represent standard deviation. Insets: AFM images of the two kinds of channels. Scale bars, 200 nm.

1T′ $MoTe_2$ shows a series of peaks of the A_g mode at ~77, ~109, ~125, ~160 and ~258 cm^{-1} (Fig. 2c)[16,17]. Scanning electron microscopy (SEM) images (Supplementary Fig. 8) of the heterophase structures show that our method is capable of patterning complicated features with varied size. Scanning transmission electron microscopy (STEM) imaging on the heterophase $MoTe_2$ samples demonstrate the distinctive hexagonal and monoclinic structures of the 2H and 1T′ phases at atomic scale, respectively, and confirm the high crystallinity of both phases (Fig. 2h,i and Supplementary Fig. 9). The interface of the two phases was connected seamlessly (Fig. 2g and Supplementary Fig. 10), suggesting that the two phases are connected via covalent bonds.

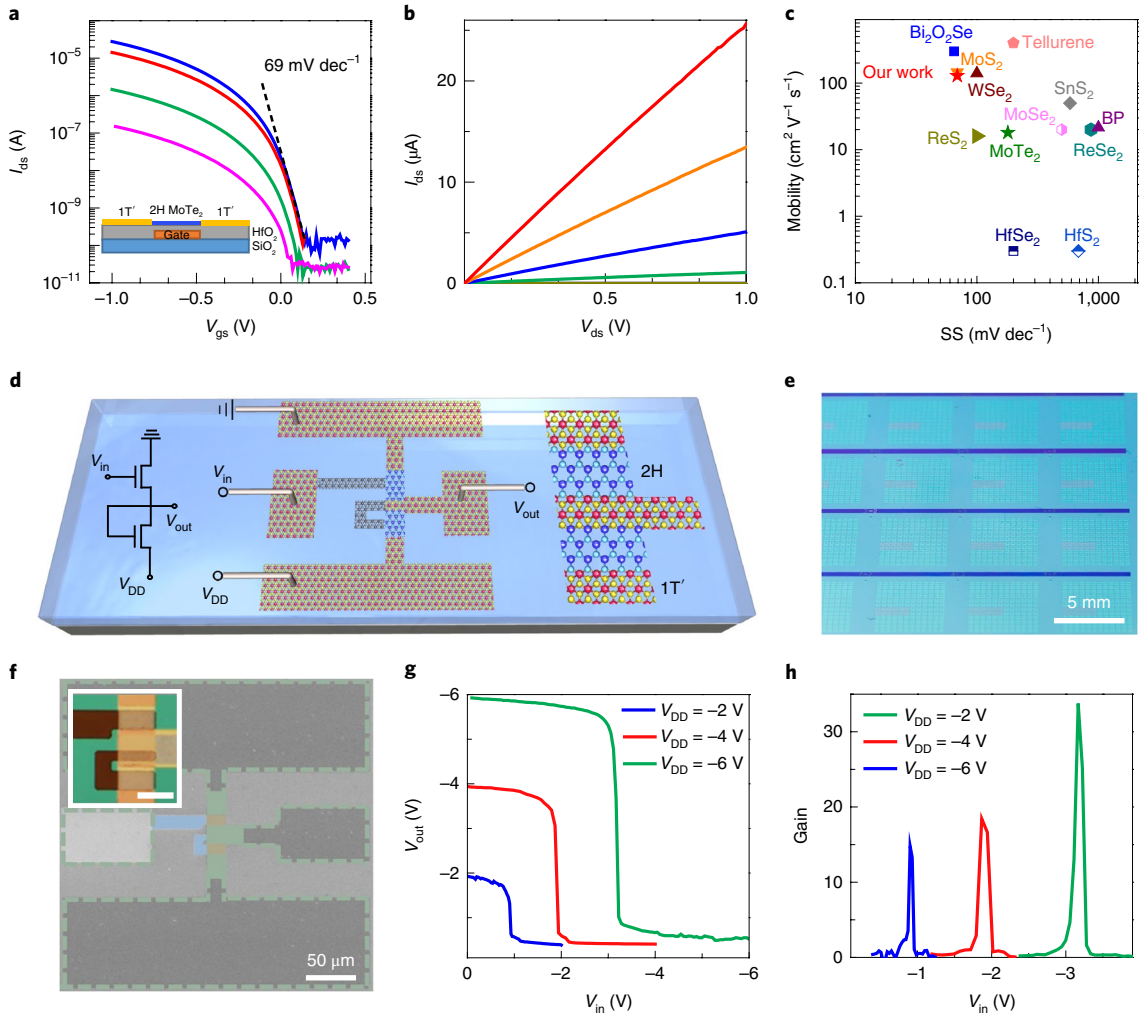

Fig. 4 | Chemically synthesized device array. a, I_{ds}–V_{gs} curves for the chemically synthesized $MoTe_2$ FETs with 12-nm-thick HfO_2 gates. Inset: schematic illustration of the cross-section of the FET. **b**, I_{ds}–V_{ds} curves at different gate voltages from −1 to 0.5 V in steps of 0.25 V from top to bottom. **c**, Comparison of our $MoTe_2$ FETs with FETs fabricated using other 2D semiconductors. Note that the mobility and subthreshold swing (SS) values were taken from the best reported values for each material with high-κ dielectrics[18–29]. **d**, Illustration of a chemically synthesized inverter. According to the circuit diagram for the inverter (left inset), the locations for semiconducting and metallic elements were deposited with precursor patterns. After the synthesis process, the patterns were converted into covalently bonded inverters in which the 2H $MoTe_2$ served as the channels and 1T′ $MoTe_2$ as the contacts and interconnects. **e**, Batch-synthesized devices (~1,500) on a centimetre scale. **f**, SEM image of a $MoTe_2$ inverter. To identify the chemical components of each part in the device, 2H $MoTe_2$, 1T′ $MoTe_2$ and WTe_2 (under HfO_2) are rendered in light yellow, green and blue, respectively, in the SEM image. Inset: optical image of the inverter (scale bar, 20 μm). **g**, Typical transfer characteristics of an inverter operating at $V_{DD} = -2$, −4 and −6 V. **h**, Signal gains of the inverter for the same vales of V_{DD}.

Construction of FETs and integrated devices

Based on the seamless connection of the semiconducting and metallic components in the phase-patterned 2D $MoTe_2$, we designed and synthesized FETs using the 2H phase as the semiconducting channel and the 1T′ phase as the source and drain. Compared with traditional FETs fabricated by sequential steps, our one-step and one-piece construction of FETs effectively avoids interfacial contaminations and material degradation as the obtained FETs can be probed immediately after synthesis without any post-synthesis lithographic process. In addition, the replacement of physical channel–electrode contacts with covalent connections can dramatically improve charge injection and thus enhance electrical performance. The transfer characteristic of the chemically synthesized $MoTe_2$ FETs measured at room temperature in vacuum behaves as a p-type semiconductor with an on/off current ratio of ~10^3 and an estimated mobility of ~50 $cm^2 V^{-1} s^{-1}$, which is much higher than that of a Pd-contacted FET (~2 $cm^2 V^{-1} s^{-1}$) with the same device configuration (Fig. 3a,b,e) and comparable to the best reported values[11,12,16]. The covalently bonded contacts dramatically lowered the Schottky barrier height to ~20 meV, one order of magnitude lower than that of the Pd contacts (~200 meV) (Fig. 3c,d and Supplementary Fig. 11). Meanwhile, the channel surface of chemically synthesized FETs (roughness (R_a) ≈ 0.6 nm) is cleaner and smoother than the lithographically fabricated devices (R_a ≈ 2.1 nm) (Fig. 3f). On balance, our chemically synthesized $MoTe_2$ FETs possess higher mobility, lower contact barrier and neater surface compared with traditionally fabricated devices (Supplementary Table 1).

In addition to the back-gated FETs, we introduced buried local gates and 12-nm-thick high-κ hafnium oxide (HfO_2) dielectrics to achieve optimal gate control separately on individual FETs. The as-synthesized FETs exhibited an on/off current ratio of ~10^5, mobility of up to ~130 $cm^2 V^{-1} s^{-1}$ and subthreshold swing down to ~69 mV dec^{-1}, which is approaching the theoretical limit of 60 mV dec^{-1} (Fig. 4a,b).

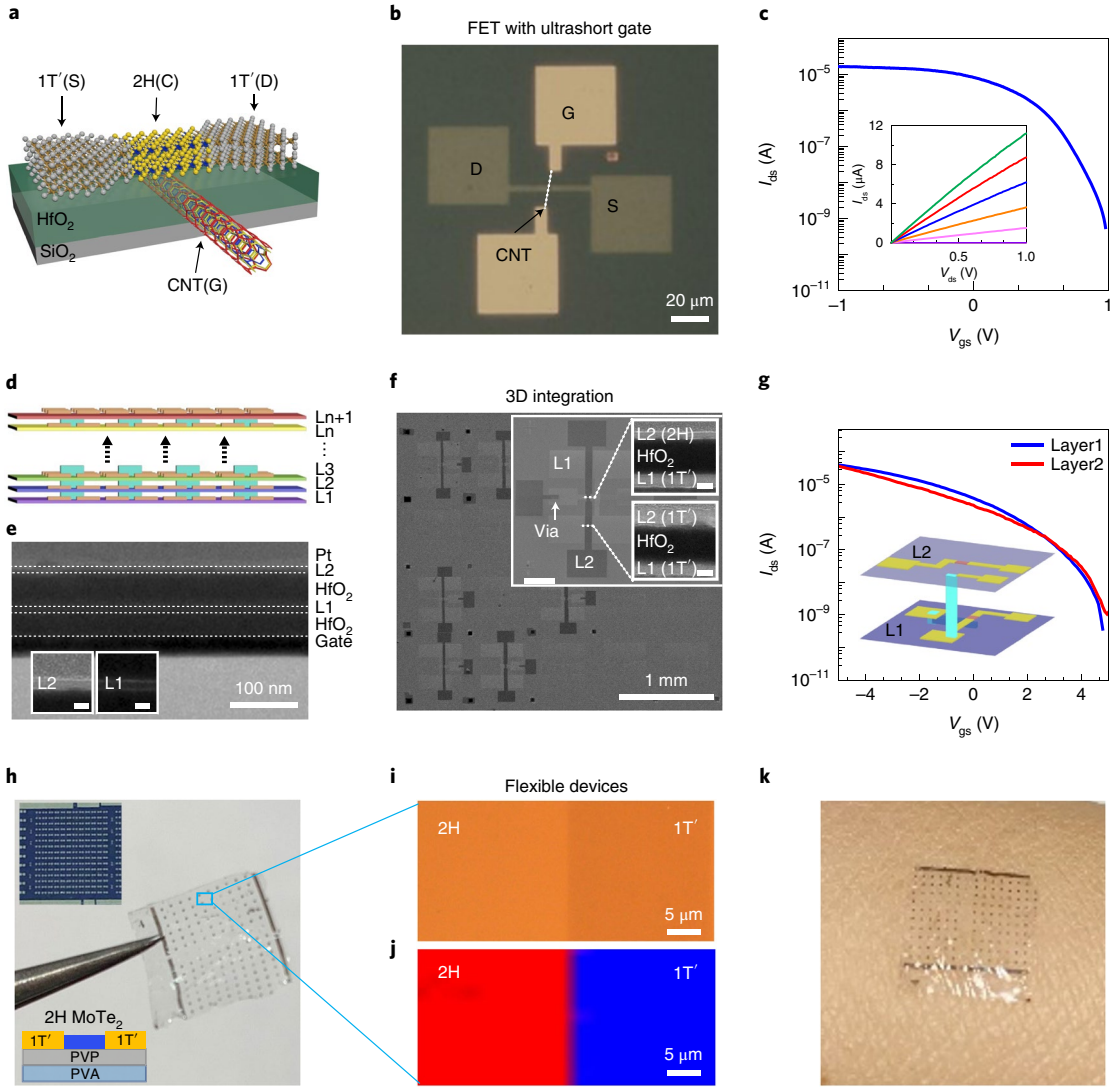

Fig. 5 | Potential applications. a, Schematic of a chemically synthesized 1T′/2H $MoTe_2$ FET with a CNT gate. **b**, Optical image of a representative CNT-gated $MoTe_2$ FET. **c**, I_{ds}–V_{gs} curve for the CNT-gated 1T′/2H $MoTe_2$ FETs. Inset: I_{ds}–V_{ds} curves at different gate voltages from −1 to 1 V in steps of 0.25 V from top to bottom. **d**, Illustration of 3D integrated circuit constructed by the repeated growth of phase-patterned $MoTe_2$. **e**, Cross-sectional TEM image of the multilayered structure in a bilayer circuit. Inset: enlarged images of the first (L1) and second (L2) $MoTe_2$ layers. Scale bars (inset), 10 nm. **f**, SEM image of $MoTe_2$ device arrays on the first (lighter) and second (darker) layers. Inset: an enlarged image of a pair of vertically connected devices in different layers (scale bar, 100 μm). The two cross-sectional TEM images present the varied vertical structures of the circuits along the respective white dashed lines (scale bars, 15 nm). **g**, Typical transfer curves measured on two connected neighbouring devices, both showing p-type conductance switching. Inset: schematic 3D illustration of the device layout. Note that the 1T′ $MoTe_2$ in layer 1 is used as the gate of devices in layer 2. **h**, Self-supporting film with an array of 144 stretchable transistors. Insets: image of the device array on a SiO_2/Si substrate before peeling-off (top) and cross-sectional schematics for the film with devices (bottom). **i**,**j**, Optical (**i**) and Raman mapping (**j**) image of a 1T′/2H $MoTe_2$ junction on PVP/PVA film, respectively. **k**, Intrinsically stretchable chemically synthesized $MoTe_2$ devices on PVP/PVA film attached to a human wrist.

The performance of the $MoTe_2$ FETs we synthesized is among the top values based on 2D materials (Fig. 4c)[18–29], demonstrating the potential of our approach in fabricating high-performance devices. Further analysis of the device performance parameters is provided in Supplementary Figs. 12 and 13 and Table 2.

Next, we explored the chemical synthesis of integrated devices such as arrays of logic inverters and radiofrequency (RF) transistors. According to the device design for the inverters and RF transistors, the locations for the semiconducting and metallic elements were first deposited with $MoO_{2.0–2.5}$ and MoO_3 patterns, respectively, in the desired size and geometry on chips with buried gates (Supplementary Fig. 14). The chips were then tellurized at 650 °C and the channel materials, contacts and interconnects were formed simultaneously (Fig. 4d,f) during the tellurization to produce a large array of logic inverters and RF transistors (Fig. 4e) on a centimetre scale, revealing extraordinary large-area manufacturing ability of this method. The obtained inverters composed of 2H $MoTe_2$ as channels and 1T′ $MoTe_2$ as contacts and interconnects were ready to work after the synthesis process (Supplementary Fig. 15). The transition voltage of all the 2D digital inverters approached the ideal voltage (V_{DD}/2) and the output swing (defined as the largest difference in V_{out}) was close to the supply voltage (V_{DD}), showing excellent logic-level conservation (Fig. 4g). Furthermore, in our chemically synthesized $MoTe_2$

inverter, the voltage gain was up to ~35 under a supply voltage of −6 V (Fig. 4h), which meets the requirements for integrated circuits consisting of multiple cascaded inverters[30]. The synthesized RF transistors were designed with a two-gate structure to enlarge the aspect ratio (Supplementary Fig. 16)[31]. The cutoff frequency f_T of as-synthesized $MoTe_2$ RF transistors with a 5 μm gate length reached up to 320 MHz, as determined by on-chip microwave measurements followed by de-embedding procedures. The successful construction of both logic and RF devices with high performance demonstrates the capability of building complicated circuits with our strategy. Moreover, the performances of our inverters and RF transistors did not show obvious degradation after three months, exhibiting excellent air stability (Supplementary Fig. 17).

Potential applications

Compared with silicon, the ultrathin nature of 2D materials allows for optimal electrostatic control in ultrashort transistors as well as maximizing the integration density in the vertical direction. In addition, 2D materials are more flexible and therefore promising in constructing flexible electronics. Based on these advantages we demonstrated the applications of our approach for the following: FETs with ultrashort gates, 3D integration and flexible electronics. To demonstrate the scaling potential of the approach, we constructed $MoTe_2$ FETs with ultrashort gate lengths by introducing CNTs as the gate electrodes (Fig. 5a). We first buried arrays of CNTs under the HfO_2 dielectrics and then synthesized 1T′/2H $MoTe_2$ FETs on the HfO_2 dielectrics (Fig. 5b and Supplementary Fig. 18). The obtained FETs with ~4 nm CNT gates exhibit excellent switching characteristics with a subthreshold swing of ~73 mV dec^{-1} and on/off current ratio of ~10^5 (Fig. 5c).

To show the feasibility of our approach for 3D integration we synthesized heterophase $MoTe_2$-based electronic devices at different vertical levels with interconnections as schematically shown in Fig. 5d. The first layer of $MoTe_2$ with channel and contact patterns was synthesized on a SiO_2/Si substrate with buried gates and then covered with a thin film of HfO_2. An additional layer of patterned 2H/1T′ $MoTe_2$ was synthesized on the HfO_2 using the same procedures as used for the bottom layer. Accompanied by synthesis of the $MoTe_2$ in the top layer, the neighbouring layers were also interconnected through an etched via (Supplementary Fig. 19a). Arrays of $MoTe_2$ FETs were successfully fabricated in different levels (Fig. 5e,f) and the obtained FETs in the two levels both showed p-type conductance switching with similar on/off ratios (~10^5) and mobility (~30 cm^2 V^{-1} s^{-1}), confirming that synthesis of the additional layers does not degrade the performance of the bottom layers (Fig. 5g). Resistance measurements confirmed a reliable interconnection between the two layers (Supplementary Fig. 19b,c). These results demonstrate the potential of our approach in pursuing 3D integrated circuits based on ultrathin materials for dramatically increased integration density in order to outperform traditional planar integrated circuits.

The atomically thin 2D TMDCs also have good flexibility and thus are ideal candidates for building flexible electronic devices. We peeled off the chemically synthesized device array from the original substrate by using polyvinylpyrrolidone (PVP) and polyvinylalcohol (PVA) thin films as the mediator[32] and obtained a free-standing thin film with device arrays (Fig. 5h). The device patterns were faithfully transferred to the PVP/PVA thin film, as confirmed by both optical images and Raman mapping images (Fig. 5i,j). The obtained thin film can be conformably attached to skin and can sustain a tensile strain of 14% without breaking (Fig. 5k and Supplementary Fig. 20), providing new possibilities for future flexible, stretchable and wearable electronics based on 2D materials.

Conclusions

We have reported an approach for constructing scalable electronic devices with 2D TMDCs in which each component in the active layer is connected via covalent bonds. As a proof of the concept, we demonstrated the one-step synthesis of integrated circuits through the phase-patterned growth of ultrathin $MoTe_2$. Our strategy significantly reduces contact issues and structural damage for ultrathin semiconductors compared with conventional methods, and can facilitate the design and optimization of circuits. The process is not limited to $MoTe_2$; other 2D TMDCs that can be grown into patterned junctions composed of both semiconducting and metallic parts by composition or phase modulations are also suitable candidates as active materials. $MoSe_2$(n-type)–WSe_2(p-type)–multilayer $PtSe_2$(metallic) can, for example, be synthesized via an in situ selenization process[13,33].

The approach is based on ultrathin materials, and thus ultrashort channels can be created through the introduction of nanoscale gates. The density of integration can also be significantly increased through 3D integration via repeated growths at different levels, providing new possibilities for extending Moore's law. The demonstrated combination of chemically synthesized 2D devices and soft polymers also provides new insight into the construction of flexible and wearable electronic devices. Therefore, our approach provides an alternative design architecture for future integrated circuits and opens a direction for building high-performance electronic devices based on ultrathin materials.

Methods

Preparation of MoO_x precursors for the phase-selective synthesis of $MoTe_2$. A $MoO_{2.0–2.5}$ thin film (5 nm) was deposited on a SiO_2/Si substrate by magnetron sputtering of Mo followed by ambient oxidation at room temperature for the synthesis of 2H-phase $MoTe_2$. A MoO_3 thin film (10 nm) was deposited on the SiO_2/Si substrate by thermal evaporation of MoO_3 powder (Alfa Aesar, 99.999%). The MoO_x precursor patterns were fabricated by sequential preparations of $MoO_{2.0–2.5}$ and MoO_3 patterns by electron-beam lithography (EBL) or photolithography, followed by deposition and liftoff. Ar plasma treatment (30 W, 100 s) was carried out before the synthesis to remove surface contamination and excessive oxidation.

Synthesis of 2H, 1T′ and 2H/1T′ heterophase $MoTe_2$ structures. The synthesis of $MoTe_2$ was carried out in a home-built furnace with a 1-inch quartz tube under atmospheric pressure. Tellurium powder (Alfa Aesar, 99.999%, 0.3 g) was loaded into an Al_2O_3 boat located at the centre of the furnace and the substrate with MoO_x precursor facing down was placed over the tellurium powder. After purging the system with Ar gas for 15 min, the furnace was heated to 650 °C at a rate of 50 °C min^{-1}. When the temperature reached ~500 °C, tellurium was vaporized and then reacted with MoO_x precursor under a gas flow of 20 s.c.c.m. H_2/Ar (5% H_2 by volume). After being kept at 650 °C for another 60 min, the furnace was cooled naturally to room temperature.

Transfer of 2H, 1T′ and 2H/1T′ heterophase $MoTe_2$ structures. We utilized a poly(methyl methacrylate) (PMMA)-mediated transfer method to transfer the as-grown $MoTe_2$ to holey carbon TEM grids for TEM imaging. First, the source SiO_2/Si substrate with $MoTe_2$ was coated with PMMA film (Allresist, AR-P 679.04). The substrate was then etched by KOH solution (10 wt%) to detach the PMMA film from the substrate. The PMMA/sample film was rinsed thoroughly using deionized water and attached to TEM grids. Finally, the PMMA film was removed with acetone vapour[34].

We used a PVP/PVA-mediated transfer approach to peel off the as-grown $MoTe_2$ devices to construct flexible devices. First, the source SiO_2/Si substrate with $MoTe_2$ devices was coated with PVP thin film. The PVP solution was prepared by dissolving 1.5 g of PVP (Alfa Aesar, average M_w 58,000), 3 ml of N-vinylpyrrolidone (NVP) (J&K, 99.5%) and 1 ml of H_2O in 6 ml ethanol. Then, PVA polymer film as the second layer (Alfa Aesar, 98–99% hydrolysed) was used to enhance the strength of the mediator. Finally, the polymer mediator-carrying device array was peeled off directly and slowly from the edges of the substrate[32].

Characterizations of 2H, 1T′ and 2H/1T′ heterophase $MoTe_2$ structures. The optical images were captured with an Olympus BX 51M microscope. AFM images were taken with Bruker Dimension Icon in tapping mode. Raman spectra were collected with a Horiba–Jobin–Yvon Raman system under 532 nm laser excitation with a power of 2 mW. Raman mapping images were performed with a step of 2 μm. The Si peak at 520.7 cm^{-1} was used for calibration in the data analysis. X-ray photoelectron spectroscopy measurements were performed with an ESCALAB 250Xi system using Al Kα as the excitation source. All binding energies were referenced to the C 1*s* peak at 284.8 eV. GIXRD patterns were taken with Bruker D8 Advance XRD-7000 with grazing incidence angle of 2°. TEM images and selected

area electron diffraction patterns were acquired with an FEI Tecnai G20 at 200 kV. STEM images were obtained with a JEOL ARM 200F system at 200 kV. SEM images were acquired with a Hitachi SU8010 scanning electron microscope at 10 kV.

Device fabrication and measurement. To compare the electrical performance with our chemically synthesized $MoTe_2$ FETs, the metal-contacted 2H $MoTe_2$ FETs were fabricated using EBL followed by thermal deposition of Pd (~30 nm) as the source and drain electrodes.

$MoTe_2$ FETs with local gates, RF transistor and inverter were synthesized on SiO_2/Si substrates with buried gates. To fabricate the buried gates, the geometry of the gate electrodes was first defined by photolithography on SiO_2/Si followed by deposition of 30 nm W by magnetron sputtering. Then, 50 nm HfO_2 was deposited on top of the W gate electrodes using atom layer deposition and served as the gate dielectrics. A second photolithography stage, inductively coupled plasma etching and MoO_3 deposition were conducted to wire out the buried gate as a test pad. The channel was defined by photolithography and deposition of Mo. The source and drain electrodes were then defined by photolithography and MoO_3 deposition. Finally, the chips were tellurized at 650 °C and the $MoO_{2.0-2.5}$ (deposited Mo after natural oxidation) and MoO_3 were converted to semiconducting 2H $MoTe_2$ and metallic 1T′ $MoTe_2$, respectively. At the same time, the construction of the devices was completed. After the synthesis, the obtained RF transistors and inverters were measured without any post-synthesis treatment. For the 3D integration, HfO_2 (~50 nm thick) was deposited on the first layer as the insulator, then the chemical synthesis of functional layers was repeated.

Construction of CNT-gated $MoTe_2$ FETs began with fabrication of gate pads on CNTs via photolithography followed by deposition of 20 nm W by magnetron sputtering. Then, 12 nm HfO_2 was deposited on top of the W gate electrodes using atomic layer deposition to serve as the gate dielectrics. The channel and source–drain electrodes were deposited as $MoO_{2.0-2.5}$ and MoO_3 patterns, respectively. Finally, the samples were tellurized at 550 °C to convert the oxides to semiconducting 2H $MoTe_2$ and metallic 1T′ $MoTe_2$, respectively.

The performances of the FETs and inverters were measured with a probe station under high vacuum (~10^{-6} mbar) at room temperature using an Agilent B1500A analyser. The RF transistors were measured with a probe station under atmospheric pressure at room temperature using a Keysight N5247A network analyser.

Data availability

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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Author contributions

L.Y.J. and T.-L.R. co-supervised the study. L.Y.J. and Q.Z. conceived the ideas. Q.Z., X.-F.W., S.-H.S. and Q.L. performed the experiments. L.G., X.Y.Z., C.-P.Y. and X.Z.L. performed STEM measurements and analysis. H.Y.L. performed SEM and GIXRD measurements and analysis. J.Y.Z. performed EBL fabrications. L.Y.J., Q.Z., T.-L.R. and X.-F.W. co-wrote the manuscript. All authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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