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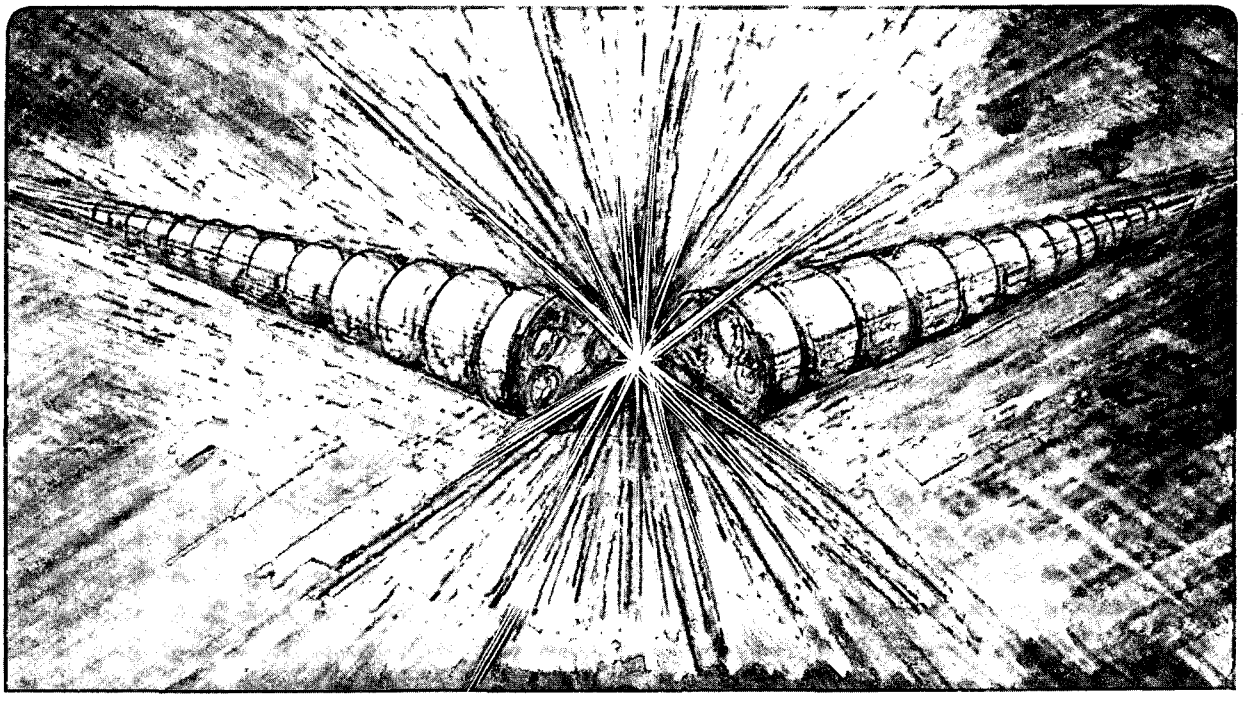

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Abstract

A smart pixel detector is being developed for Time Resolved Crystallography for biological and material science applications. Using the Pixel Detector presented here, the Laue method will enable the study of the evolution of structural changes that occur within the protein as a function of time. The x-ray pixellated detector is assembled to the integrated circuit through a bump bonding process. Within a pixel size of $150x150\mu m^2$, a low noise preamplifier-shaper, a discriminator, a 3 bit counter and the readout logic are integrated. The read out, based on the Column Architecture principle, will accept hit rates above $5x10^8/cm^2/s$ with a maximum hit rate per pixel of 1MHz. This detector will allow time resolved Laue crystallography to be performed in a frameless operation mode, without dead time. Target specifications, architecture and preliminary results on the 8x8 front-end prototype and the column readout are presented.

I. INTRODUCTION

X-ray detection for protein crystallography experiments has been relying on energy integrating media (films) or frame based imaging devices (imaging plates, phosphor screens coupled to Charge Coupled Devices -CCDs). These detectors offer excellent spatial resolution but the time needed to read them out is prohibitively long for time resolved crystallography. Phosphor screens with CCDs readout currently being introduced as the next generation of energy integrating devices still have read out time on the order of one second.

Smart Pixel Arrays Detectors offer substantial improvements when compared with existing devices. In particular frameless readouts will enable two or three orders of magnitude in time resolution improvement for time resolved crystallography. Originally these detectors were pursued at Lawrence Berkeley National Laboratory by the High Energy Physics community in relation to its experimental needs in charged particle tracking at low radii, high luminosity particle colliders.

Smart Pixel Array Detectors consist of monolithic arrays of reverse biased semiconductor diodes hybridized with an Application Specific Integrated Circuit (ASIC) instrumenting each diode in the array. Incident X-rays, through direct energy conversion, are absorbed in the pixels where they create electron/hole pairs. When the photon is totally converted in a pixel, the number of pairs is proportional to its energy. The electronic signal generated can be processed on an event basis or integrated over a period of time on many events. Smartness resides entirely in the capability of the signal processor and readout structure. Event driven smart pixel array detectors based on the Column Architecture can provide multiparameter information (energy and time), with sparse and frameless readout, without dead time [1]. Low end, energy integrating smart pixels offer substantial speed advantage when compared to CCDs and an unique advantages for time resolved or static Laue protein crystallography and are likely to open new insights into the molecular processes.

II. PIXEL ARCHITECTURE

The silicon diode array is bump-bonded to the integrated circuit configuring a module (fig.1). The column based architecture allows the IC's output pads to be on one side of the module which will make easier the assembly of the whole detection area.

The readout electronics architecture is shown in Figure 2. The individual pixel processor consists of a low-noise amplifier shaper followed by a comparator which provides the counting of individual photons with an energy above a programmable energy threshold. To accommodate the very high rates, above $5.10^8/cm^2/s$, each pixel processor has a 3 bit pre-scaler which divides the event rate by 8. Overflow from the divider which defines a pseudo fourth bit will generate a readout sequence where the pixel's address is readout. The pixel address is converted off-chip and used to increment a location in an histogramming memory to generate the computerized image of the Laue diagram.

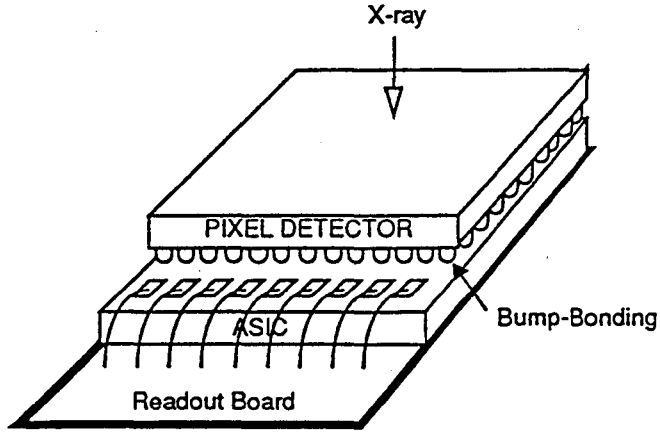

Fig. 1: Smart pixel module

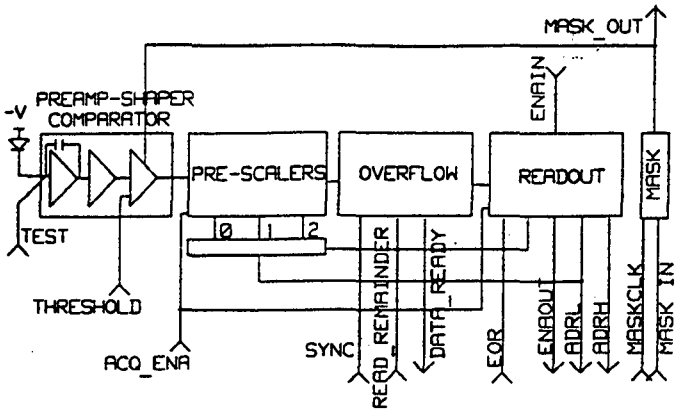

Fig.2: Electronics architecture

III. An 8x8 ANALOG PIXEL PROTOTYPE

An 8x8 analog pixel prototype has been integrated in the *HP* 0.8µm 3 metal process available through *MOSIS*. This first prototype contains only the analog front-end (integrator-shaper) that will allow us to check the connectivity of the bump bonding process as well as to characterize different detector material to be used (Silicon, CdZnTe). CdZnTe pixels with identical geometry are being developed by U.C. San Diego in association with *DIGIRAD* (San Diego, CA).

The third metal layer has been only used in the layout as a ground plane to shield the electronics from the detector and to prevent any coupling from the digital circuitry to the inputs.

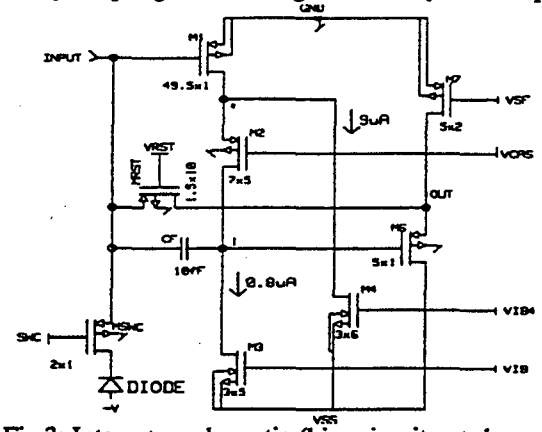

Fig.3: Integrator schematic (bias circuit not shown)

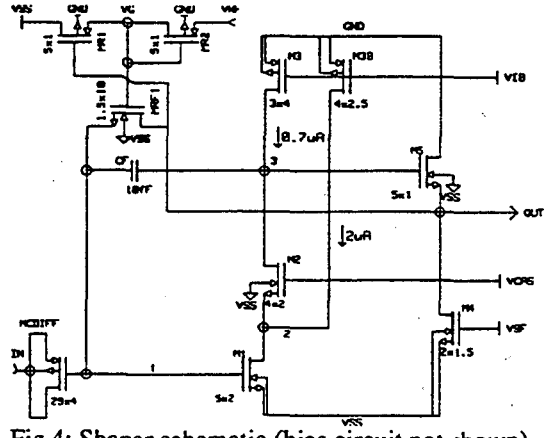

Fig.4: Shaper schematic (bias circuit not shown)

Figure 3 shows the schematic of the cascoded low-noise integrator optimized for 0.3pF detector capacitor. The DC reset is provided by the transistor M_{RST} with the external control voltage V_{RST}. An on-chip photodiode has been integrated (gated by transistor M_{SWC}) to allow optical test on the array. The preamplifier is coupled to the shaper (fig. 4) using the gate oxide capacitor of a MOS transistor (C_{diff}=0.2pF) for the differentiation stage.

A MOS transistor (M_{RF1}), biased in its linear region by M_{R1} and M_{R2}, is used to implement the feedback resistor of the shaper amplifier. The shaping time constant can be adjusted with V_{RF} and the shaper bias current, from 50ns to 150ns. The small dynamic range ensure a relatively good linearity of the shaping [2].

The integrator and shaper output pulses are shown in figure 5. The total gain is 860mV/fC (or 140mV/1000e-). The noise measured without any detectors connected at the input is 52e^-_{RMS} which should rise up to 110e^-_{RMS} with the silicon diode connected at the input (C_{det}+$C_{parasitic}$~0.3pF). The overall power consumption is less than 50uW/channel (V_{SS}=-3V).

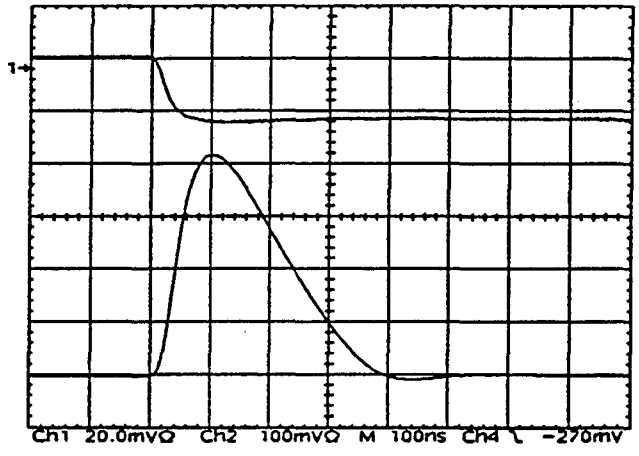

Fig.5: Integrator and shaper output

The peak hit-rate specification on one pixel is 1MHz. The preamplifier has to be reset at a higher rate if we want to keep its dynamic infinite without any pile-up (fig.6). The trade-off is between the counting rate capability and the noise generated by the fast reset of the preamp (parallel noise generated by the MOS feedback resistor). The shaping time being set around 100ns (i.e. peaking time), table 1 gives the Equivalent Noise Charge (ENC):

Preamp's RESET	10µs	800ns
Equivalent Noise Charge (RMS)	52e-	64e-

Table 1: ENC for different preamp's reset (no detector)

The fast reset of the integrator has only a small effect on the noise performance and allows an infinite dynamic range. The shaper's baseline is kept constant which would have not been the case for longer reset time constants due to the differentiation.

In a later prototype, the comparator will be DC coupled to the preamp-shaper to achieve the energy discrimination (threshold will be set around 3.6keV or 1000e-). In order to get a good threshold adjustment, the DC output voltage should be reproduced from pixel to pixel. The measurements of the 8x8 arrays over 17 chips have shown that the standard deviation of the shaper's output voltage is around σ=8mV which correspond to 57e- (the expected value, as interpolated from M.Pelgrom et al. [3], was around 5mV).

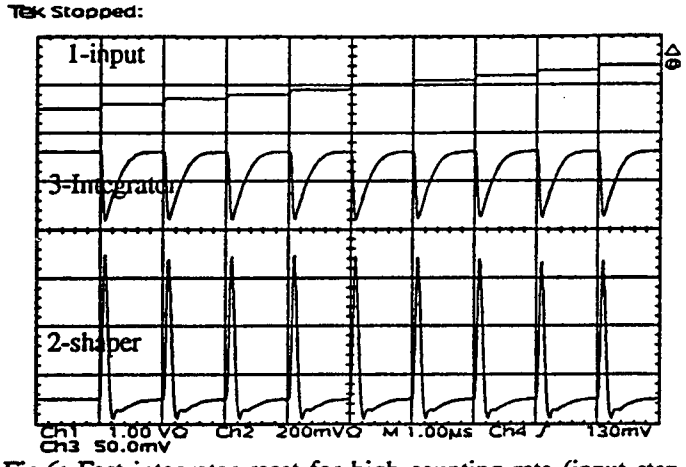

Fig.6: Fast integrator reset for high counting rate (input step voltage going through 10fF equivalent to 2000e- injected)

IV. COLUMN READOUT PROTOTYPE

A prototype of the pre-scaler and the readout logic has been integrated and tested. The pre-scaler is a 3 bit counter dividing the event rate by 8. When a pixel has accumulated 8 counts, the overflow bit (the pseudo fourth bit) is sent to the end of the column via the DATA_READY line (fig.7). The end of the column generates then a synchronization signal SYNC to prevent any overwriting of the overflows while the pre-scalers are counting and the readout sequence starts. The *ripple logic*, common to 2 columns, sends the overflowing pixel's address, ADRL and ADRH, to the end of the column where they are formatted and forwarded to the data acquisition logic. These addresses are analog currents generated at the pixel level. The conversion of the addresses will be done externally.

When a pixel address readout is completed, the *end-of-column logic* sends an *end-of-read* signal (EOR) and processes another overflowing pixel, if any. Each pixel readout cycle takes approximately 80ns. The readout sequence ends when the *end-of-column* receives the ENAOUT of the *ripple logic*.

When the acquisition has stopped a *read remainder* cycle (fig.8) allows to get the contents of the pre-scalers. A masking logic has also been implemented to turn off any undesirable pixel.

Every signal going through the column is a current signal which means that the associated voltage on the line is less than 0.8Volts for a better speed and lower power consumption. The information generated by the detectors assemblies consists of the pixel address within the detector system. Dual columns of 100 pixels operate independently and in parallel to accommodate the very high incident rate. The storage of information will be implemented through the usage of histogramming memory modules. These modules will be built around standard fast off the shelf commercial memory chips [4]. The chips controllers will be optimized for speed.

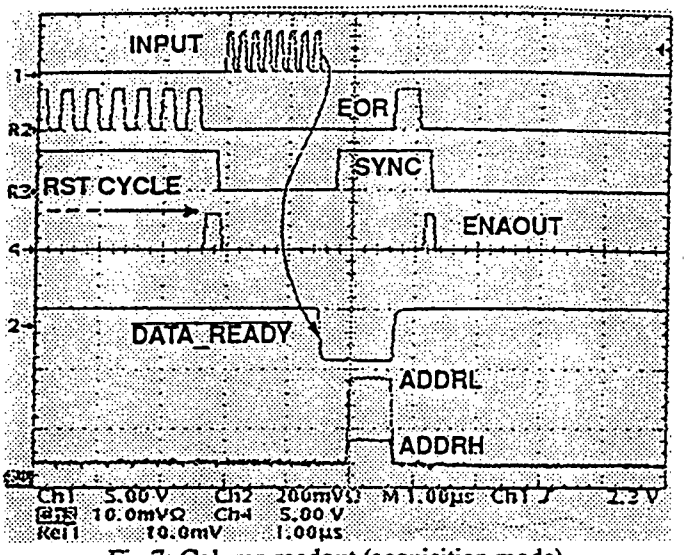

Fig.7: Column readout (acquisition mode)

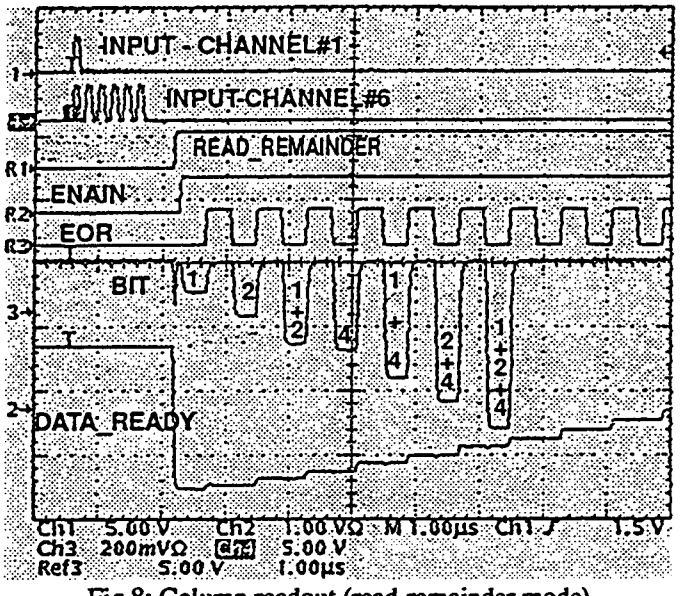

Fig.8: Column readout (read-remainder mode)

V. COLUMN ADDRESS ENCODER

A column address encoder is being build to convert the analog address into a digital address used to increment the histogramming memory. The histogramming memory readout consists of three main functions: a priority encoder, a histogram memory DSP and a random trigger synchronization, fig.9.

The priority encoder is designed for sparse scan readout of 100 pixel addresses in one dual-column. The encoder generates a 7 bits pixel address and the column address.

The histogramming memory DSP (HSP48410 histogrammer/accumulating buffer) is configured to operate in the asynchronous mode where each address points to a 24 bit register (counter) yielding to a 10 bit x 24 bit memory unit. The 10 bit pixel address from the column encoder is sampled and the associated pixel's 24 bit register is incremented.

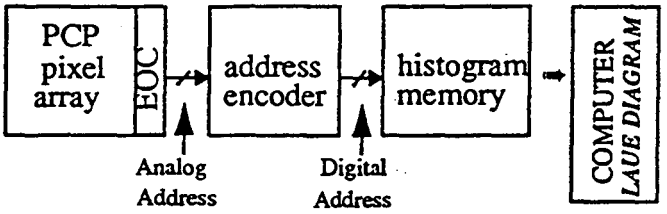

Fig.9: Column encoder addressing scheme

VI. HYBRIDIZATION TECHNOLOGY

Chip hybridization technology as well as wafer level technologies have been investigated for prototypes and production. At the chip level gold bumps and conductive thermoplastic are affordable and proven for bumps no less than 50μm in diameter. They are also effective at the wafer/module level hence offer an effective to transition the development from a prototype to a module. Assemblies are being made at *ETEC* (Peabody, MA) using conductive thermoplastic. This process has the advantage of being low temperature, low pressure and thus less likely to damage the ASIC or the detector particularly in the case of CdZnTe where surface damage can lead to a substantial increase of surface current.

Wafer level processes (solder bumps, indium bumps) cannot be easily or cheaply adapted to the chip level bumping but are very effective for mass production quantities. However solder cannot be used with CdZnTe due to the high temperature required.

VII. LAYOUT

The 2 main blocs of the electronics have already been integrated. Figure 10 shows the actual layout of the complete pixel readout (analog front-end and the digital readout) within 150x150μm^2. Analog and digital circuits will have independent supplies.

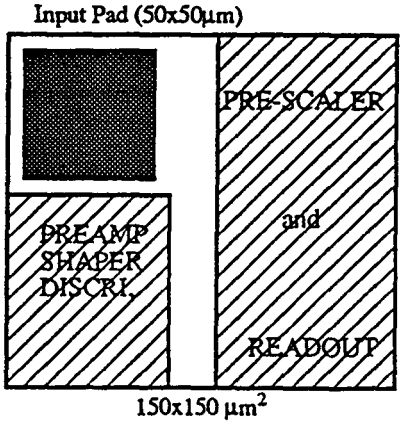

Fig.10: Floor plan of the complete pixel

VIII. CONCLUSIONS

The analog signal processor tested has shown very good performance summarized in table 2. The 8x8 analog pixel array connected to a 10 bit ADC and histogramming memory will be used to characterize Silicon and CdZnTe pixel detectors. The column architecture readout will allow to meet the particular needs of protein crystallography.

Transfer Gain	860 mV/fC
Shaping time constant	100 ns
ENC for C_d= 0 pF (measured)	64 e- rms
ENC for C_d= 0.3pF (expected)	120 e- rms
Power Consumption (V_{supply}= 3 V)	50 μW
Sustainable average event rate	5x10^8 cm^2/s (100KHz/pixel)
Sustainable peak rate per pixel	1 MHz

Table:2 Performance of the pixel readout

Time resolved Laue crystallography will be performed in a frameless operation mode without dead time. The dual-columns operate independently regrouping in the final prototype 100 pixels. Acquisition and readout are done concurrently allowing a sustainable event rate of 5x10^8/cm^2/s (100kHZ average/pixel). The fast reset capability of the integrator accommodates a sustainable peak rate/pixel of 1 Mhz with an infinite dynamic range. The pixel masking capability will allow to turn off defective pixels in any desired pattern. The column architecture gives the possibility to abut modules on 3 sides for large arrays, and these into larger elements.

A full 50x50 array will be constructed. This will be the basic ASIC for a complete system. These building blocks will be combined into 2x2 arrays modules.

IX. ACKNOWLEDGMENTS

We would like to thank C.Rossington and J.Walton from LBNL for fabricating the silicon pixel detectors.

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