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Los Angeles

Heterogeneous Integration of Wafer Bonded Wide Bandgap Semiconductors

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy in

Materials Science and Engineering

by

Michael Evan Liao

2022

ABSTRACT OF THE DISSERTATION

Heterogeneous Integration of Wafer Bonded Wide Bandgap Semiconductors

by

Michael Evan Liao

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2022

Professor Mark S. Goorsky, Chair

With bandgaps > 2 eV, the appealing electronic and optical properties of wide bandgap semiconductor materials such as β-Ga_2O_3, GaN, 4H-SiC, AlN, and diamond are promising candidates for next generation high power electronic devices. While these materials have been demonstrated to surpass silicon's fundamental efficiency limits at high power and/or frequencies, their fullest potential has yet to be realized. This is primarily due to a lack of fundamental understanding of material processing and thermal management of heat generated during device performance. The focus of this dissertation will be addressing fundamental processing of heterogenous integration with focus on β-Ga_2O_3 as well as the origin of surface roughening for homoepitaxial GaN growth for ~kV device layers.

Chemical mechanical polishing of β-Ga_2O_3 is a key issue for this emerging material. Smooth surfaces (< 0.5 nm rms) and subsurface damage-free (010) β-Ga_2O_3 were achieved with low-pressure (1 kPa) chemical mechanical polishing. Material removal rates ranged from ~200

μm/hr to 0.4 μm/hr depending on the lapping/polishing slurry used. With 3 orders of magnitude of control over the material removal rate, β-Ga_2O_3 can be efficiently lapped and polished to achieve damage-free substrates suitable for epitaxy, wafer bonding and layer transfer.

Next, an important step in the successful transfer of β-Ga_2O_3 layers along a non-cleavage plane (010) is demonstrated through exfoliation via helium ion implantation for the first time. Helium implanted substrates were annealed at 200 °C followed by 500 °C to initiate helium bubble nucleation and promote bubble growth at the implanted projected range, respectively. Micron-sized surface blistering covering the entire implanted area was observed, confirming exfoliation. These observations match early reports of silicon blistering which, when combined with established direct wafer bonding practices, leads to large-scale transfer of controlled thickness β-Ga_2O_3 layers along non-cleavage-plane orientations.

Thermal strain at elevated temperatures due to differences in coefficients of thermal expansion between materials is an important consideration for heterogeneous integration processes. The coefficients of thermal expansion of β-Ga_2O_3 were measured from single crystalline substrates because: (1) the high anisotropy of β-Ga_2O_3 and (2) technological relevance to heterogenous integration. All CTE values reported here are linear under the temperature regime relevant for epitaxial growth – between room temperature to 1000 °C.

A technique to fabricate novel heterojunction interfaces referred to as surface activated bonding involves bombarding wafer surfaces with noble gas ions in ultrahigh vacuum prior to bonding. The resulting bonded interface typically consists of a few ~nm thick amorphous or damaged region. However, there is a lack of fundamental understanding of these interfaces. Si bonded to Si structures were fabricated as a model system to fundamentally understand bonded interfaces fabricated using this ion bombardment method. These thin amorphous interfaces are

highly electrically resistive and impede electron transport across the bonded interfaces. However, post-bond annealing is demonstrated to recrystallize the bonded interface and form conductive interfaces at temperatures of 450 °C compared to ~1000 °C when utilizing other wafer bonding methods.

Another model system used in this work were InP|InP bonded structures to study the impact of relative crystallographic orientation between the two wafers (twist misalignment) on the electronic transport across bonded interfaces. Twist misalignment between bonded wafers is found to impede electronic transport across the interface. The findings presented here suggest that misorientation plays an important role in the transport properties of interfaces. This is especially important for heterogenous integration of materials that may not have the same crystal structure where minimizing mismatch between orientations corresponds to minimizing tilt and twist misorientation.

With the development of polishing and exfoliation for β-Ga_2O_3, a thin film of ($\underline{2}$01) β-Ga_2O_3 was exfoliated and transferred to (0001) 4H-SiC. The ($\underline{2}$01) orientation of β-Ga_2O_3 best matches the basal plane of 4H-SiC to minimize tilt misorientation; and the in-plane directions were aligned such that [010] β-Ga_2O_3 ‖ [11$\underline{2}$0] 4H-SiC to minimize twist misorientation. The surface activated bonding technique was utilized for bonding, which induced a thin ~nm amorphous interfacial region at the bonded interface. Annealing the bonded structure at 800 °C for 1 hour: (1) removed residual strain in the exfoliated β-Ga_2O_3 layer due to the ion implant, (2) reduced lattice mosaicity in the β-Ga_2O_3 film, and (3) recrystallized the amorphous bonded interface. The thermal transport across the bonded interface increased with the change in structural characteristics. The thermal conductivity of the transferred β-Ga_2O_3 layer doubled and the thermal boundary conductance improved by ~20% after the anneal.

GaN is more technologically matured than β-Ga$_2$O$_3$, but one of the major challenges with GaN is maintaining smooth surfaces during epitaxial growth (~tens of microns) to fabricate high power device layers and to facilitate bonding and layer transfer. It is found that localized lattice distortions in GaN substrates serve as nucleation sites for macro-steps and macro-terraces. After nucleating, these macro-features grow laterally along the surface and coalesce, leading to significant roughening of the wafer surface. While previous studies focused on substrate miscut as a means to control macro-feature formation, localized lattice tilt from defects is another important contributor to macro-feature formation. Hence, near zero-defect GaN substrates will be necessary for achieving thick GaN device layers on the order of tens to hundreds of microns for ~kV to ~20 kV applications.

The dissertation of Michael Evan Liao is approved.

Suneel Kodambaka

Dwight Christopher Streit

Timothy S. Fisher

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Table of Contents

List of Tables

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Chapter 1: Introduction

1.1 Motivation

     Recently, power devices with up to 3.3 kV blocking have successfully been commercialized for vehicle electrification and power converters in medium voltage applications using wide bandgap semiconductors. This class of semiconductors have bandgaps > 2 eV and have appealing electronic and optical properties suitable for next generation high power applications. It is anticipated that by the year 2030, ~80% of all electricity could pass through some form of power electronics.[1] Wide bandgap materials include β-Ga_2O_3, GaN, 4H-SiC, AlN, and diamond, and some of their materials properties is shown in Table 1.1.

	Si	4H-SiC	GaN	β-Ga_2O_3	AlN	Diamond
Bandgap (eV)	1.12	3.26	3.39	4.5-4.9	6.1	5.5
Thermal Conductivity (W/cm/K)	1.3	4.2	1.3-2.0	0.11-0.27	2.85	10-20
Mobility (cm^2/V/s)	1300	1000	1200	300	300	2000
Breakdown Electric Field (MV/cm)	0.3	2.5	3.3	8.0	12-17	7.5-10
Dielectric Constant	11.8	9.7	9.0	10	8.5	5.5
Baliga's FOM	1	340	1450	3444	10067	24661

Table 1.1: Materials Parameters of Various Wide Bandgap Materials vs Silicon

     However, wide bandgap devices with higher voltage ratings are shown to suffer from reduced yield and reliability due to high density of material defects,[2] undeveloped understanding of material processing, and insufficient thermal management. Despite empirical demonstrations of surpassing silicon in the high power and/or frequency technology space, none of the wide bandgap materials have yet realized their fullest potential. This is primarily due to a lack of fundamental understanding of not only defects, but also material processing and thermal management of heat generated during device performance. In order to achieve de-carbonization

in the manufacturing sector, electric grids, and electric generation technologies, it is critical to develop high efficiency devices with voltage ratings between 6.5-20 kV. De-carbonization has become very significant to combat the existential threat of climate change to humanity, and the Department of Energy has made it a top priority.[3] Development of materials processing is crucial to fully utilizing wide bandgap materials. For example, chemical mechanical polishing is essential for achieving both smooth < 1 nm rms roughness surfaces and subsurface-damage-free material. Without a fundamental understanding of polishing, subsequent processes would not be possible such as epitaxy, wafer bonding and transfer, and device fabrication. Furthermore, improper polishing (e.g., too high pressures, aggressive abrasives or solvents, etc...) introduces polish-induced defects that would compromise subsequent processing such as growth or exfoliation and ultimately device performance. Fundamental knowledge is required to accelerate the realization of next generation wide bandgap high power devices to their fullest potential. Wide bandgap semiconductor applications include next generation wireless communications and power electronics for microgrids, high efficiency motor drives, and high voltage power converters/inverters. The impacts of wide bandgap materials would benefit the reliability and security of the U.S. electrical grid, reduce emissions contributing to climate change, and reduce costs of electricity consumption.

1.2 References

[1] https://arpa-e.energy.gov/technologies/programs/pndiodes

[2] R. E. Stahlbush, et. al., 2022 IEEE IRPS Conference 65–61.

[3] https://www.energy.gov/articles/doe-announces-423-million-and-new-industry-partnerships-decarbonize-american-manufacturing

Chapter 2: Background and Theory

2.1 Chemical Mechanical Polishing

Chemical mechanical polishing (CMP) is one of the most essential processes that enables the possibility of epitaxy, wafer bonding, and devices. The CMP process consists of a chemical and a mechanical component, which in conjunction can produce a synergetic effect in removing material. The chemical component comes from the polishing slurry solvent, which is typically either an acidic or basic (e.g., NaOH, KOH, or NaClO) solvent. A suitable solvent would be one that chemically alters the surface of a material (either bulk substrate or a thin film) such that the surface layer is mechanically weaker than the underlying material.[1,2] This weaker surface layer could be an oxide layer[2] or a passivating hydroxide salt layer in the case of β-Ga_2O_3 reacting to NaOH or KOH.[3,4] This weakened surface layer is then removed by the mechanical component of the CMP process. The mechanical component usually is associated with abrasive particles such as colloidal silica, ceria, or alumina, but can be from the polishing pad for abrasive-free CMP. Regarding the use of abrasive particles, the abrasive particle concentration has been shown to be directly proportional to material removal rate.[5,6,7]
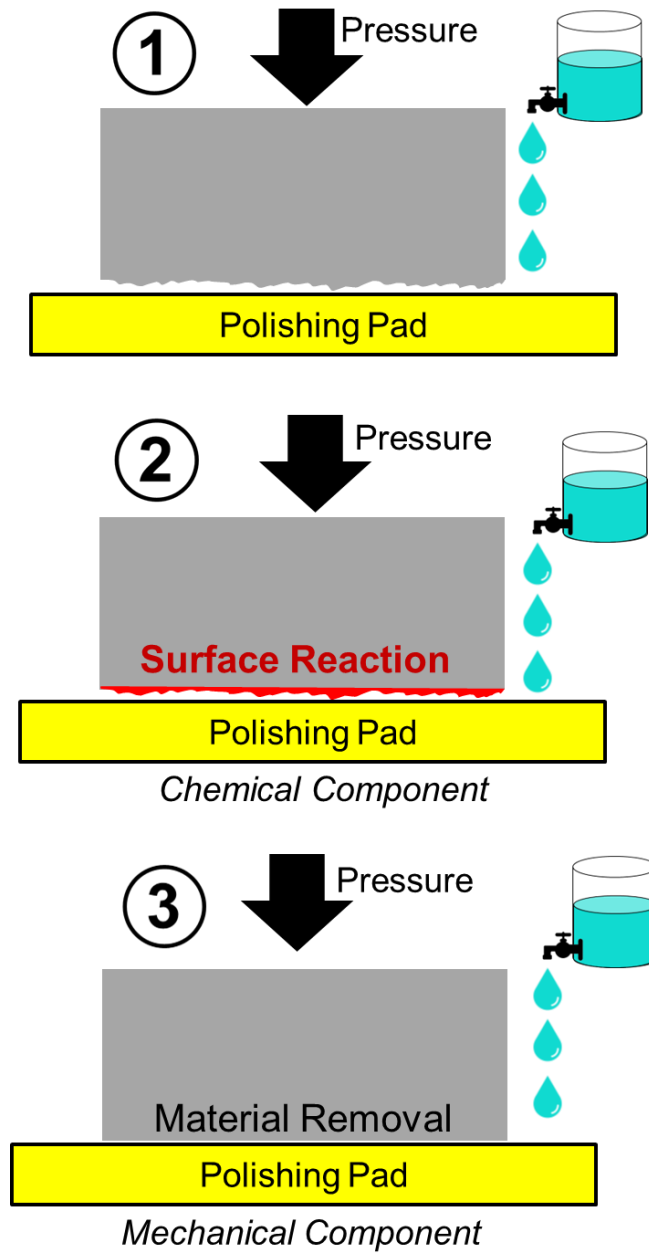
Figure 2.1. Schematic of the CMP process: (1) initial rough surface, (2) chemical surface reaction with the polishing slurry solvent, and (3) mechanical removal of weakened surface layer.

Applied pressure is another important parameter, where too high pressures induce subsurface damage while too low pressures result in no polishing action.[2,8] Samples are held by a

vacuum jig and placed on a rotating polishing pad while polishing slurry is dispensed on the pad directly at a constant rate. A set of polishing parameters (applied pressure, pad rotation speed, pad material, slurry solvent, and abrasive particle material, size, and concentration) and is optimized when both smooth scratch-free surfaces (< 1 nm rms roughness) and subsurface-damage-free material are achieved simultaneously. A Logitech PM5 polisher was used in this dissertation and peristaltic pumps were utilized to controllably dispense slurry.

2.2 X-ray Diffraction and Topography

X-rays can be used to nondestructively characterize materials by x-ray diffraction (XRD). XRD can be utilized to nondestructively characterize the lattice distortion, strain, and thickness of thin films. The underlying principle is the phase relationship between the incident X-rays and the exiting X-rays after interacting with a sample. If waves are in-phase, then they reinforce each other and the path difference among the waves is an integer multiple of the wavelength. If waves are out-of-phase, then their amplitudes annihilate each other and the path difference among the waves is a factor of half-integer wavelengths.

The key features of the triple-axis XRD setup used in this dissertation are shown in Figure 2.2. To deconvolute peak broadening contributions due to strain and thickness (ω:2θ scanning axis) versus lattice mosaicity, tilt, and lateral coherence length (ω scanning axis), triple-axis XRD is utilized. An exaggerated schematic showing the difference in acceptance angle between double-axis and triple-axis acceptance angles are shown in Figure 2.3. Triple-axis employs a (220) Si analyzer crystal before the detector, while double-axis is the same setup without the analyzer crystal. The acceptance angle of the double-axis diffraction optics is on the order of tenths of a degree, while the triple-axis diffraction optics setup achieves an acceptance

angle of ~10" (thousandths of a degree). Triple-axis is a useful optics setup to unequivocally

separate strain-related vs lattice-tilt-related peak broadening. X-ray ω:2θ measurements are used

to assess strain, while X-ray rocking curves (ω measurements) are used for assessing lattice

mosaicity (tilt) and misorientation – which can correspond to lattice damage, low-angle grain

boundaries, etc.
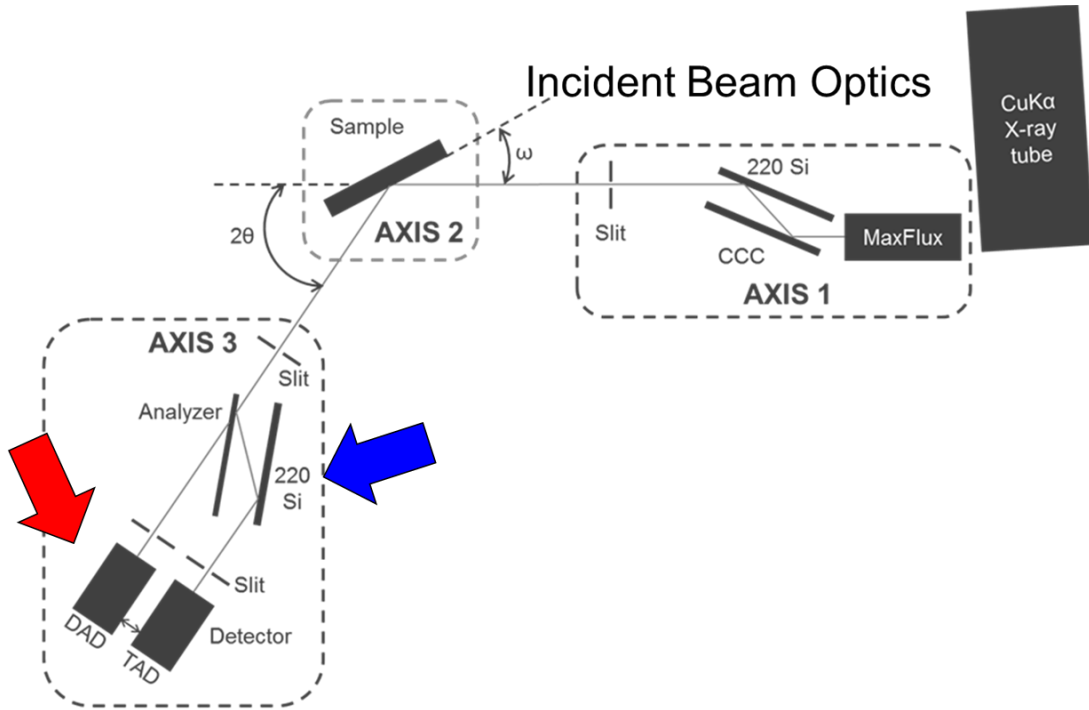
Figure 2.2. Schematic diagram of the high-resolution triple-axis X-ray diffraction setup. DAD

corresponds to Double-Axis Diffraction, while TAD corresponds to Triple-Axis Diffraction.
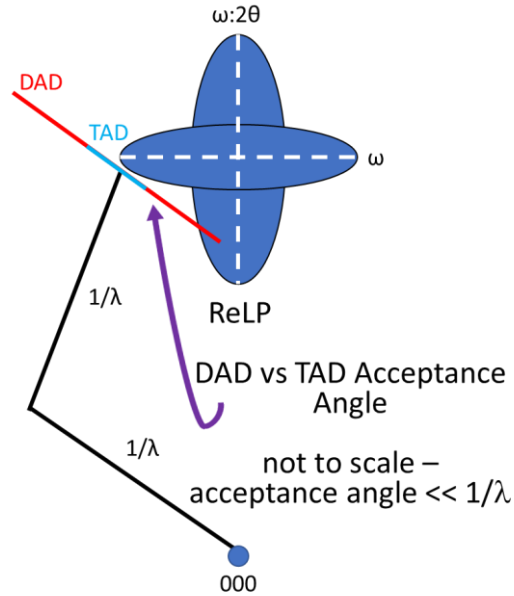
Figure 2.3. Schematic of double-axis vs triple-axis acceptance angle for measuring a symmetric reflection.

Another useful nondestructive technique is double-crystal X-ray reflection topography.[9] Here, a sample is rocked along the ω scanning axis and film is exposed to the diffracted beam at a given rocking curve angle. In this dissertation, synchrotron double crystal X-ray topography images were generated at the 1-BM beamline of the Advanced Photon Source at Argonne National Laboratory. An X-ray energy of 8.05 keV (~Cu Kα_1) was used for all measurements. A (333) Si beam conditioner with a ~46° miscut was used as the first crystal to expand the incident X-ray beam and to increase the angular resolution of the topography measurement. All X-ray topography images were recorded on Agfa Structurix D3 X-ray films. Two types of X-ray topography images were generated: single exposure and superimposed images. Single exposure images expose separate pieces of film for each point along the rocking curve. Superimposed images are obtained by exposing a single piece of film to multiple points along the X-ray rocking

9

curve. As demonstrated in our previous work for a diverse roster of materials, more information is preserved by recording single exposure images, e.g., tilt and strain can be deconvoluted and magnitude of tilt and/or strain can be extracted.[10,11,12,13,14] Furthermore, our recent work for bare GaN substrates developed a methodology for generating tilt maps from film by superimposing single exposure images to visualize how lattice distortion is distributed spatially across a wafer.[15,16] A schematic of the reflection topography technique is shown in Figure 2.4.
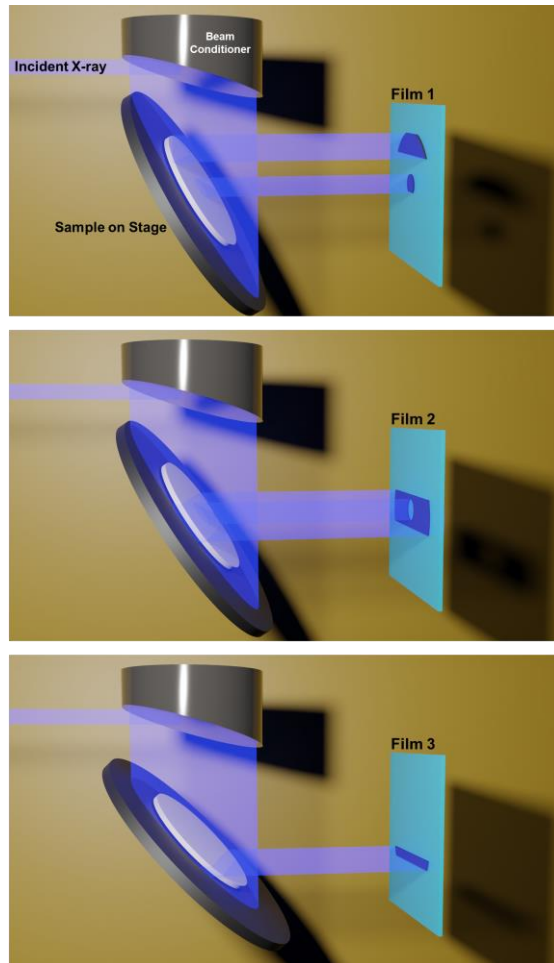
Figure 2.4. Schematic of the double-crystal reflection X-ray topography technique. The sample is rocked at different angles along the rocking curve and individual sheets of film is exposed to the corresponding diffracted beam at each angle. If the sample is defect-free and flat, the entire wafer would be imaged at one single angle. However, defects such as dislocations and low-angle

grain boundary as well as curvature diffract different parts of the material at different angles along the ω scanning axis. The individual films can be recombined to generate a rocked image as well as a lattice distortion map (i.e., tilt and strain maps) for a given sample.

2.3 Atomic Force Microscopy

Atomic force microscopy (AFM) is an excellent tool for assessing surface roughness of materials. It is especially useful for direct-wafer-bonding applications since AFM can measure height at the nanometer resolution. The basic principle of AFM is Hooke's law for springs: the force exerted on a spring is directly proportional to the spring's displacement from its equilibrium state. The "spring" in AFM is a cantilever with a fine tip, whose tip size is typically less than 20 nm in diameter. The force is due to the interaction between the cantilever tip and a sample surface. The spring constant of typical cantilevers ranges from 0.01 to 50 N/m. The cantilever is connected to a piezoelectric device, which is sensitive to mechanical forces exerted on the cantilever. A laser and photodiode are setup in order to monitor the cantilever, as shown in Figure 2.5.
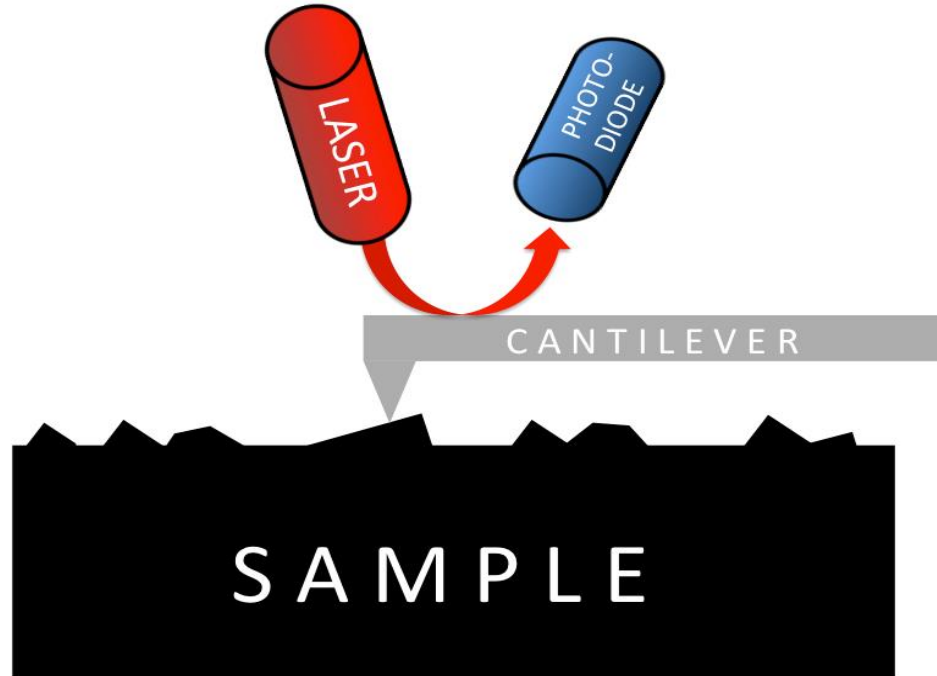
Figure 2.5. Schematic diagram of the AFM setup.

During each scan, the cantilever initially oscillates at its resonant frequency. As the cantilever tip moves along the sample surface, the tip is close enough to the surface such that van der Waals interactions is appreciable, i.e. attractive forces at relatively far distances and repulsive forces are close distances. As the tip encounters various surface topological features, the cantilever's frequency dampens. This dampening is detected by the laser-photodiode setup since the laser is reflecting off of the cantilever near the vicinity of the tip. When a decrease in frequency is detected, the height of the cantilever is adjusted in order to revert its frequency back to its original value; this adjustment is recorded as the height of a spot. An image of a sample surface can then be generated from the change in cantilever height with respect to in-plane surface location.

After probing the sample surface, the root mean square (RMS) of the sample surface topology is calculated and the resulting value interpreted as surface roughness. RMS roughness

is chosen to quantify surface roughness instead of arithmetic mean roughness because valleys and peaks, i.e. local extrema, influence RMS values more than they influence arithmetic mean values. Thus, for applications such as direct wafer bonding of semiconductors, where sub-nanometer roughness is required for high-quality bonding, RMS values better characterize surface roughness.

2.4 Wafer Bonding

Wafer-bonding is the process of bonding materials, either to form homojunctions or heterojunctions, that can form interfaces ill-suited for epitaxy and potentially create interfaces with desirable emergent properties.[17] While epitaxy has provided pathways of fabricating a myriad of groundbreaking devices, epitaxial layer thicknesses are limited by a thermodynamically-driven critical thickness due to lattice mismatch in heteroepitaxial systems.[18] Larger lattice mismatch between two materials corresponds to thinner epitaxial layer critical thicknesses and larger induced strain in the epitaxial layer. Exceeding this critical thickness could lead to the formation of dislocations emanating at the substrate-epitaxial layer interface if the epilayer relaxes, which consequently degrades device properties including carrier mobility reduction and leakage current enhancement.[19,20] Without the restrictions of lattice parameter mismatch, direct wafer-bonding greatly opens up the potential for various materials combinations for many electronic devices that are not realizable through epitaxial means. In fact, direct wafer-bonding of III-V semiconductors has led to the fabrication of high-efficiency multijunction solar cells.[21,22] Additionally, direct wafer-bonding has not only provided a method of device fabrication, but also a way of characterizing and understanding the properties of interfaces across bonded materials.

While direct wafer-bonding is not bound to lattice mismatch restrictions, there are many surface considerations that determine the quality of the resulting bonded interface between materials and, by extension, the device performance. These include an understanding of surfaces both chemically (type of bonding across the interface) and topologically (smoothness and curvature). The type of bonding across the interface is determined chemically based on the surface treatments used to obtain clean and passivated surfaces. High smoothness and low curvature will also help obtain a high-quality bonded interface.[17] The properties of excellent wafer-bonding consist of a large uniform bonded area, high mechanical resilience across the bonded interface, and (in the interest of this project) minimal electrical resistance across the interface. During its infancy, direct wafer-bonding was poorly understood and taken as some abstruse process with no commercial potential. However, successful work of silicon-to-silicon bonding by Shimbo et al.,[23] (Toshiba) and silicon bonding with thermally grown oxide to make silicon-on-insulator structures by Lasky et al.,[24] (IBM) not only increased widespread interest but also helped make direct wafer-bonding commercially realizable.

The foundation for understanding bonding mechanisms for various material pairs stems from a study by Stengl et al.,[25] on the silicon homojunction system (Si|Si). Bonding falls under two categories: hydrophobic and hydrophilic bonding. Hydrophobic surfaces repels water by, for example, having a single monolayer of hydrogen atoms adhering to the material's surface. On the other hand, hydrophilic surfaces attract water molecules by usually having a layer of oxide or hydroxide ions that can adhere to water molecules well. Water that sticks to the hydrophilic surface forms chemisorbed layers (~few monolayers) of water at the bonded interface, which can help improve the interfacial bond strength between two materials.

One of the main features of bonding hydrophilic surfaces, i.e., surfaces terminated with hydroxyl groups, is that the surface has a few monolayers of water molecules. The water molecules can be thought of as a bridge that helps join two hydrophilic surfaces together. Therefore, hydrophilic bonding is more tolerant of rougher surfaces compared to hydrophobic bonding. The hydrophilic surface bonding process can be summarized in three main stages. (1) The oxide layer at the material's surface of a wafer reacts with water molecules to form X-OH bonds at the surface (X represents the atoms/species of the material to be bonded). (2) The wafer surfaces with adsorbed water are physically brought together in order to form hydrogen bonds between the water molecules. The distance between the wafer surfaces is on the order of ~1 nm. (3) The wafers are then annealed to evaporate the water at the interface in order to bring the wafers closer together by creating direct chemical bonds of surface groups via capillary forces. Schematically stage (2) looks like, starting from the bulk material moving towards the interface:

$$(\text{bulk-X-OH})–(\text{H}_2\text{O})_n–(\text{HO-X-bulk})$$
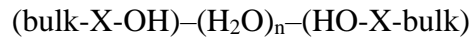
where $(\text{H}_2\text{O})_n$ represents the monolayers of water molecules. Annealing treatments help strengthen the interfacial bonds and remove water via diffusion out of the system along the bonded interface. Further annealing of these interfacial bonds results in a condensation reaction that forms stronger interfacial bonds between the two wafers, i.e.:

$$(\text{bulk-X})\text{-O-}(\text{X-bulk})$$
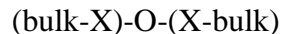
The interfacial bonding energy has been shown to improve and reach near bulk strength of the starting materials.[25,26]

The transport characteristics of bonded interfaces are the focus of this dissertation. Surfaces with any layers of insulating oxides or any insulating hydroxide-based layers will increase the interfacial electrical resistance between two bonded semiconductor wafers. In order

to minimize this detrimental effect, the bonding between semiconductors would typically employ the hydrophobic bonding mechanism. (The hydrophilic bonding mechanisms should not be completely discounted for bonding semiconductors for electrical applications since this mechanism may be relevant for newer wide-bandgap materials like Ga_2O_3). Hydrophobic bonding is dominated by van der Waals dispersion forces between two extremely smooth wafers. From purely a theoretical standpoint, any solid materials that are flat, clean, and smooth enough can be bonded together with other solid materials (to form homojunctions or heterojunctions) at room temperature and be held together purely by van der Waals forces. Intuitively, the smoother the surfaces of a solid material, the less friction it will experience with another smooth surface. However, there is a critical point where if a surface becomes sufficiently smooth enough, friction starts to increase and van der Waals forces come into play since an extremely (uniform) smooth surface has a greater areal contact with another smooth surface's atoms compared to two rough surfaces.

Hydrophobic bonding between two semiconductor wafers have been studied and employed since the 1980's for the Si|Si system and for III-V semiconductor materials since the 2000's.[27] Hydrophobic bonding can be obtained by etching a semiconductor surface with a strong acid or base in order to create a nonpolar surface that repels water. After etching, the time the semiconductor spends in ambient air should be minimized in order to lessen the formation of polar oxides that form from reacting with oxygen in ambient atmosphere. One solution to prevent oxide formation prior to bonding is to process the materials surfaces and bond under vacuum, as demonstrated for silicon by Flötgen, et al.[28] Chemical approaches demonstrated by Jackson et al.,[29] and Seal et al.,[30] show successful bonding of both GaAs and InP homojunction and heterojunction combinations at room temperature and at ambient atmospheric pressure. After

stripping off the oxide layers of the III-V materials, the wafers are submerged in an aqueous $(NH_4)_2S$ solution in order to form a chemisorbed passivating sulfur layer. While some oxide was still present at the interface, the harmful effect of oxides on the electrical performance was mitigated after annealing the bonded structures.

For either bonding mechanism, both hydrophobic and hydrophilic wafer bonding requires smooth surfaces prior to bonding. In other words, optimal bonding occurs for large areal contact between two wafers. What this physically translates to is surfaces having low curvatures, low net thickness variation, and low roughness. Since van der Waals bonding is significant only for atoms in close proximity, wafers need to be brought less than 1 nm from each other. Thus, the RMS roughness of the surfaces would ideally be around 1 nm or less.

A relatively newer technique to fabricate novel heterojunction interfaces is surface activated bonding. Here, wafers are bombarded with noble gas ions in ultrahigh vacuum prior to bonding. The resulting bonded interface typically consists of a few ~nm thick amorphous or damaged region. While a many different homojunction and novel heterojunction structures have been reported in the literature, there is a lack of fundamental understanding of these interfaces. Understanding the electrical and thermal transport characteristics of these interfaces is essential for being able to engineer bonded interfaces. Wafer-bonding could enable us to integrate different materials in order to exploit benefits and mitigate shortcomings.

2.5 References

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Chapter 3: Chemical Mechanical Polishing of β-Ga₂O₃

3.1 Introduction

Chemical mechanical polishing (CMP) is a critical process for every semiconductor material. Achieving smooth < 1 nm rms roughness surfaces is critical for devices, epitaxy, and wafer bonding. However, the current literature is deficient in detailed chemical mechanical polishing (CMP) studies for β-Ga₂O₃. Huang et al.,[1] utilized colloidal silica in NaOH to CMP (100) β-Ga₂O₃ while using an applied pressure of 15 kPa. In a follow-up study, Huang et al.,[2] varied the slurry solvent chemistry while using colloidal silica particles and 13 kPa of applied pressure. While smooth epi-ready surfaces were achieved, subsurface damage had not been assessed in either study. High pressures are often employed to reduce processing time because pressure is directly proportional to material removal rate.[3,4,5,6] However, as demonstrated in our previous work with polishing various III-V materials, high applied pad pressure will induce subsurface damage despite achieving smooth surfaces.[7] On the other hand, if the applied pressure is insufficient, then little to no polishing occurs.[8] Hence, the applied pressure must be optimized such that polishing action occurs while simultaneously not inducing subsurface damage.[7,9,10,11,12] In the most recent study by Huang et al.,[13] the applied pressure had been lowered to 1.5 kPa and 800-nm alumina particles were used in the CMP slurry. For abrasive CMP, using particles that are too hard for a given polished material will induce scratches and subsurface damage.[7,8] Subsurface damage had not been assessed in that case and therefore it was not clear if alumina is suitable for achieving subsurface damage-free β-Ga₂O₃.

Polishing of a different orientation, (010) β-Ga₂O₃, had recently been reported in a very comprehensive study by Blevins et al.,[14] but the applied pressure was not reported. In that study, subsurface damage was assessed using double-axis X-ray rocking curves by monitoring the

changes in the rocking curve FWHM. The subsurface damage associated with X-ray diffraction peak broadening may consist of cracks, dislocations, and similar extended defects. Our previous work[7,9,10,11,12] has demonstrated that the peak widths below the half maximum are more sensitive to lattice distortions induced by subsurface damage (i.e., FWXM, where X < 0.5). However, the damage associated with peak broadening below the FWHM may not be visible by other means, such as with transmission microscopy images, e.g., at an intermediate step where a polished substrate is approaching, but has not yet achieved a damage-free state. Additionally, our previous work employed triple-axis X-ray rocking curves to assess subsurface lattice damage.[7,9,10,11,12] Performing XRD measurements using triple-axis optics is advantageous over the more widely used double-axis measurements because peak broadening is deconvoluted into its lattice tilt/mosaicity (ω scanning axis) and strain (ω:2θ scanning axis) components. On the other hand, peak widths of rocking curves measured in double-axis combines the contributions of both lattice tilt and strain. While double axis measurements provide useful information, a more fundamental understanding of the nature of subsurface damage (e.g., tilt vs strain) is essential for studies that range from the elimination of subsurface damage to the impact on epitaxial growth and device performance. Furthermore, the X-ray beam used by Blevins et al.,[14] projected ~20 mm across wafer surface, spanning nearly the entire diameter of the substrate. By using a wide incident X-ray beam, the rocking curve widths are susceptible to broadening from lattice curvature across a wafer,[15] which obscures the effect of polishing especially towards the final CMP steps. The X-ray rocking curves were also reported to be measured while mounted on the polishing plate, which is a practical measurement that allows for more rapid assessment of changes. However, as shown in our recent work,[16] such sample mounting for X-ray rocking curve measurements can

bend substrates by several arcsec of curvature and induce rocking curve broadening that can obscure the contribution of polishing damage to the width.

In this study, polishing parameters for (010) β-Ga$_2$O$_3$ are optimized to achieve both smooth (sub-nm rms) surfaces and subsurface damage-free material simultaneously. These procedures, especially the final polishing steps, are also necessary to achieve high crystalline quality layers produced by light-gas induced exfoliation processes.[17] The (010) orientation has the highest thermal conductivity[18] compared to the other orientations of β-Ga$_2$O$_3$. Additionally, compared to the other orientations, (010) β-Ga$_2$O$_3$ has been reported to be less susceptible to stacking faults and twinning defects during epitaxial growth.[19,20] However, this study is certainly expected to serve as a guide for CMP processes of other orientations.

3.2 Experimental Details

Lapping and chemical mechanical polishing was performed on a Logitech PM5 CMP tool. The flow rate was 10 mL/min and the pad rotation speed was 30 RPM for both the lapping and polishing. A mechanically harder polyurethane impregnated polyester felt polishing pad[21] was used exclusively for the lapping steps, while both the felt pad and a softer polyurethane poromeric polishing pad[21] were used for the polishing steps. The applied pressure on the substrates was varied from 1 kPa to 10 kPa using DI water on the poromeric pad to optimize the pressure. Because β-Ga$_2$O$_3$ is inert to water,[22] there is no chemical component and only mechanical abrasion is supplied by the polishing pad. Based on results from that study (described below), 1 kPa was then used for all the lapping and polishing steps. The particles used for lapping were either 0.3 μm or 5 μm alumina particles in deionized water. CMP employed colloidal alumina in sodium hypochlorite (Chemlox) or colloidal silica in NaOH (both 70 nm

particles). A final 10-minute cleaning step on a separate poromeric pad was performed after CMP to remove residual slurry particles: a dilute 1:10 NaOCl solution and a dilute 1:2 citric acid solution were mixed on the polishing pad.[8,11,12] 1.5×1.0 cm^2 (010) β-Ga$_2$O$_3$ substrates grown using the edge-defined film-fed growth method were polished.

Subsurface damage was assessed by measuring symmetric (020) β-Ga$_2$O$_3$ rocking curves with triple-axis X-ray diffraction. The incident X-ray beam width was reduced to ~0.14 mm with mechanical slits in order to reduce the impact of lattice curvature and avoid obscuring the rocking curve data from non-polishing effects. The projected X-ray footprint across the substrates was ~0.28 mm for the symmetric (020) β-Ga$_2$O$_3$ reflection. An FEI TITAN S/TEM operating at a 300 keV accelerating voltage was employed to generate scanning transmission electron microscopy (STEM) images aligned to the [$\bar{1}$02] zone axis. Both cross-sectional brightfield (BF) and high angle annular dark field (HAADF) STEM images were generated. The FIB system was also used to mill fiducial markers on the substrates to measure material removal rates for each polishing step using AFM.

3.3 Results and Discussion

First, the softer poromeric polishing pad was used with DI water to study the effect of applied pressure on β-Ga$_2$O$_3$ CMP. Here, there is no chemical action and only mechanical abrasion is provided by the pad. The subsurface damage was assessed by measuring the diffuse scatter intensity from triple-axis symmetric (020) β-Ga$_2$O$_3$ XRD rocking curves (e.g., peak widths taken at the FW(0.001)M). The FWHM and FW(0.001)M for commercially available pristine β-Ga$_2$O$_3$ substrates are ~13" ± 2" and ~120" ± 10", respectively as shown in Figure 3.1. Using pristine substrates is important for studying the effects of various polishing parameters,

otherwise poor crystalline quality material would obscure the analysis. With high quality

crystals, any broadening in the rocking curves could unequivocally be attributed to the effect of

polishing. After 1 hour of polishing at 10 kPa, the rocking curve FWHM and FW(0.001)M

increased to 33" ± 4" and 890" ± 20", respectively. Even polishing another identical pristine

substrate using 3 kPa for 1 hour broadened the rocking curve FWHM to 27" ± 3" and

FW(0.001)M to 650" ± 20". The diffuse scatter intensity is indicative of subsurface damage and

shows that even 3 kPa of applied pressure is unsuitable for β-Ga_2O_3 CMP. This results suggests

that subsurface damage was likely introduced in prior studies that used pressures of 13 kPa to 15

$kPa^{1,2}$. Using an applied pressure of 1 kPa for 1 hour was found to not induce damage; as shown

in Figure 3.1, the peak widths are unchanged from its as-received pristine state. The rms surface

roughness did not change (< 0.5 nm) when using any pressures from 1 kPa to 10 kPa. This

indicates that smooth surfaces do not necessarily correspond to pristine, damage-free material.
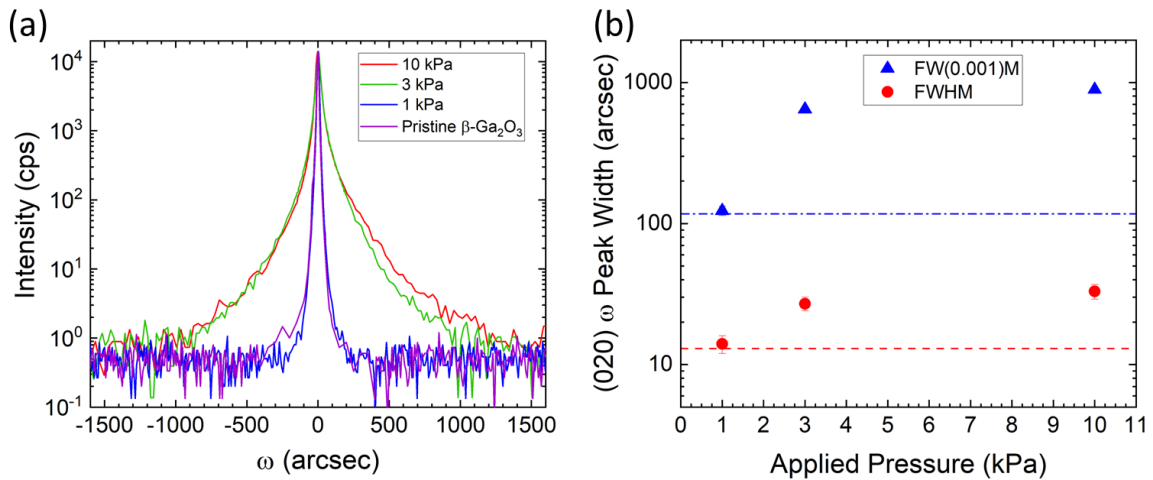
Figure 3.1. (a) Triple-axis X-ray diffraction rocking curves of the (020) β-Ga_2O_3 symmetric

reflection. The applied pressure was decreased from 10 kPa to 1 kPa using DI water and a soft

poromeric polishing pad. (b) Corresponding FWHM and FW(0.001)M peak widths for each

pressure, where the dashed lines correspond the peak widths of commercially available pristine (010) β-Ga$_2$O$_3$ (the FWHM is ~13" ± 2" and FW(0.001)M is ~120" ± 10").

To determine a compatible polishing pad material, a relatively harder felt pad was compared with a softer poromeric pad. Colloidal silica slurry (70 nm particles) and 1 kPa applied pressure were utilized for both pads. After one hour on the felt pad, the rocking curves in Figure 3.2 show that the harder pad induces subsurface damage. The corresponding FWHM and FW(0.001)M peak widths broadened to 24" ± 3" and 410" ± 20", respectively. The polishing damage is due to the mechanical abrasion from the harder felt pad. As shown in Figure 3.2, upon using the same silica slurry on the softer poromeric pad for ~135 minutes, the damage was completely removed. Figure 3.2 corresponds to the same substrate where subsurface damage was induced and subsequently eliminated. A total of ~0.9 μm of material was removed to revert the substrate back to its pristine state. We demonstrate that soft poromeric polishing pads, 1 kPa of applied pressure, and colloidal silica slurry are appropriate polishing parameters for achieving smooth surfaces and subsurface-damage-free material simultaneously.
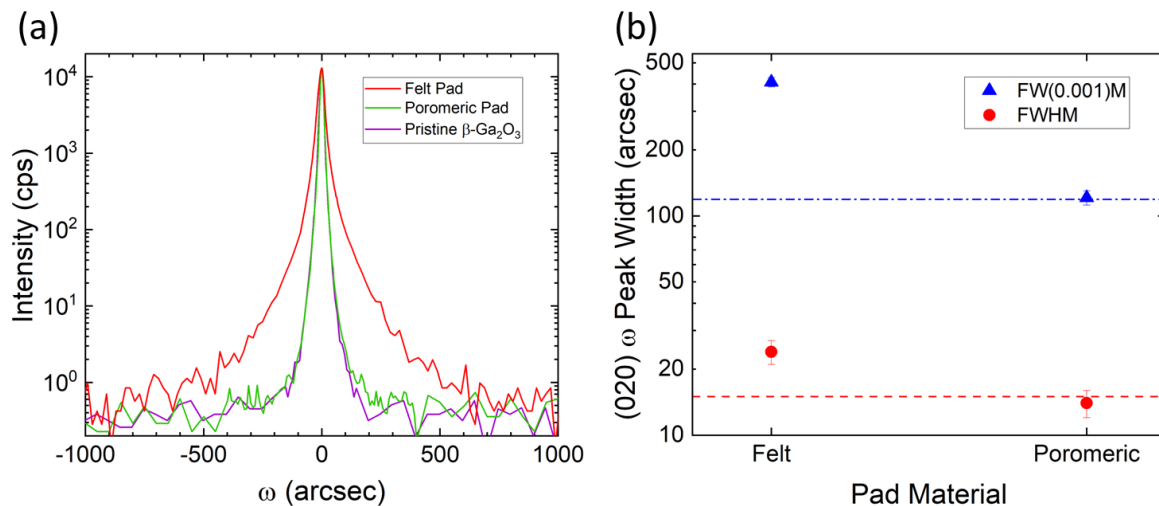
Figure 3.2. (a) Triple-axis X-ray diffraction rocking curves of the (020) β-Ga$_2$O$_3$ symmetric reflection for polishing on a harder felt pad versus a softer poromeric pad. The applied pressure was 1 kPa and colloidal silica slurry was used for both pads. All three rocking curves correspond to the same substrate. The as-received pristine substrate was polished on the felt pad first for 60 minutes, followed by the poromeric pad for 135 minutes. (b) Corresponding FWHM and FW(0.001)M peak widths for each pad material, where the dashed lines correspond the initial peak widths of this substrate (FWHM is ~15" ± 2" and FW(0.001)M is ~120" ± 10").

Lapping and polishing are key steps for semiconductor wafers whose surfaces are roughened from wafer slicing and grinding. To demonstrate, the rough sides of as-received single-side polished (010) β-Ga$_2$O$_3$ substrates were lapped and polished. As shown in Figure 3.3(a), the (020) rocking curve not only shows a broad main peak at ω = 0" with a FWHM of 180" ± 20" and a FW(0.001)M of 8900" ± 100", but also an even broader peak at ~5600" along ω. This second broader peak corresponds to highly misaligned material, which shows that the grinding process induced so much subsurface damage that the lattice near the surface is tilted ~1.6° away from the rest of the underlying substrate. The sample was oriented such that the (100) flat was perpendicular to the incident X-ray beam, i.e., this severe lattice tilt distortion is along the direction normal to the (100) cleaveage plane (the mechanically weakest plane of β-Ga$_2$O$_3$). The AFM shown in Figure 3.4(a) also shows surface cracks and voids aligned and elongated preferentially along the (100) plane. The rms roughness of the rough surface was initially 60 nm. Triple-axis (020) symmetric ω:2θ scans were also measured to assess the presence of strain induced by the wafer slicing and grinding process as shown in Figure 3.3(c). One ω:2θ scan was measured at the main peak along the rocking curve at ω = 0", and a second

26

ω:2θ scan was measured at the peak associated with the highly misaligned material at ω = 5600".

The ω:2θ FWHM of the misaligned material is 290" ± 40" (dotted curve) while the ω:2θ FWHM

of the peak measured at ω = 0" is 70" ± 10" (dashed curve). The broader ω:2θ peak width is

associated with strain, which indicates that the distortion of the highly misaligned material is not

only tilted, but is also strained relative to the underlying material deeper in the substrate. There is

also some strain (less than in the misaligned material) that extends below the misaligned material

because the ω:2θ FWHM of the peak measured at ω = 0" is broader than commercially available

(010) β-Ga$_2$O$_3$ substrates that have triple-axis ω:2θ FWHM of ~20".

These rough surfaces were first lapped with 5 μm Al$_2$O$_3$ particles using the harder felt

polishing pad and applying 1 kPa of pressure. After 2 hours of lapping, the intensity of the peak

due to the highly misaligned material dropped by an order of magnitude as shown in Figure

3.3(a). While the FWHM decreased to 110" ± 10", the FW(0.001)M broadened to 9580" ± 60".

This indicates that lapping with 5 μm Al$_2$O$_3$ particles reduced the thickness of the initial damage

associated with the misoriented layer, but also introduced new subsurface damage (as confirmed

with electron microscopy measurements as shown below). Because the peak broadening is now

symmetric around the main peak, the new subsurface damage induced by the lapping is isotropic.

The rms roughness was reduced to 17 nm, and ~μm wide and tens of nm deep scratches were

observed along arbitrary directions along the surface. Reducing the particle size to 0.3 μm Al$_2$O$_3$

and lapping for 2 hours led to a reduced amount of subsurface damage. Note that with each of

these steps, a significant amount of material is removed, such that the damage measured

corresponds to what was introduced with that step. The rocking curve FWHM remained at 110"

± 10", while the FW(0.001)M decreased to 3690" (from 9580") ± 50". The resulting rms

roughness was ~1 nm and the surface scratches were narrower and shallower: tens of nm wide

and ~1 nm deep. Despite the surface roughness approaching < 1 nm smoothness, the diffuse

scatter intensity shown in the corresponding rocking curve indicated that subsurface damage

remained. After changing the slurry to 70 nm Al_2O_3 and polishing for 6 hours, the rocking curve

FWHM and FW(0.001)M reduced to 48" ± 6" and 1310" ± 50", respectively. The rms roughness

remained unchanged (~1 nm) due to shallow surface scratches. Even when using colloidal

particles, this result indicates that Al_2O_3 is too hard for β-Ga_2O_3. As shown in Figure 3.3, the

rocking curve exhibits diffuse scatter intensity due to subsurface damage indicating that Al_2O_3 is

unsuitable as a final polishing step.

CMP using colloidal SiO_2 (~2.5× softer than Al_2O_3) for 10 hours was demonstrated to be

effective in completely removing the remaining subsurface damage. Figures 3.3(a) and 3.3(b)

show both the rocking curve FWHM and FW(0.001)M were reduced to 13" ± 2" and 120" ± 10",

respectively. This matches the same pristine crystalline quality that is commercially available as

shown in Figure 3.3(b). The final rms roughness values over 40×40 μm^2 areas were ≤ 0.5 nm

(0.4 nm as shown in Figure 3.4(e)). Furthermore, the (020) ω:2θ FWHM was reduced to 18" ±

2", which also matches the widths of commercially available pristine substrates and indicates the

strain from subsurface damage was also removed. Figure 3.3(d) compares the (020) triple-axis ω

and ω:2θ scans on the same plot. The widths of the ω:2θ scan are broader than the ω scan (18" vs

13" for the FWHM, respectively, and 230" vs 120" for the FW(0.001)M, respectively). The

broader widths along the ω:2θ scanning axis is not related to the effect of polishing but rather

due to crystal truncation rod scattering. This broadening contribution would be convoluted in

double-axis rocking curve measurements and obscure sub-surface damage broadening.

A 10-minute step with diluted 1:10 bleach and 1:2 citric acid on a clean poromeric pad[11]

was demonstrated to be an effective cleaning method for removing residual colloidal SiO_2

particles on the β-Ga$_2$O$_3$ surface. No particles were observed in $40 \times 40 \ \mu m^2$ AFM scans. The bleach and citric acid were kept separated and mixed on the polishing pad. The applied pressure was kept at 1 kPa. We find that unlike our previous work for III-V CMP[7,9] where bleach and citric acid chemically reacts by oxidizing the III-V surface, β-Ga$_2$O$_3$ is much less reactive to both bleach and citric acid. No reaction was observed even after 12 hours of performing CMP with diluted bleach and citric acid on pristine substrates. The material removal rate was negligible, and no surface roughening was observed while the surface was cleaned.
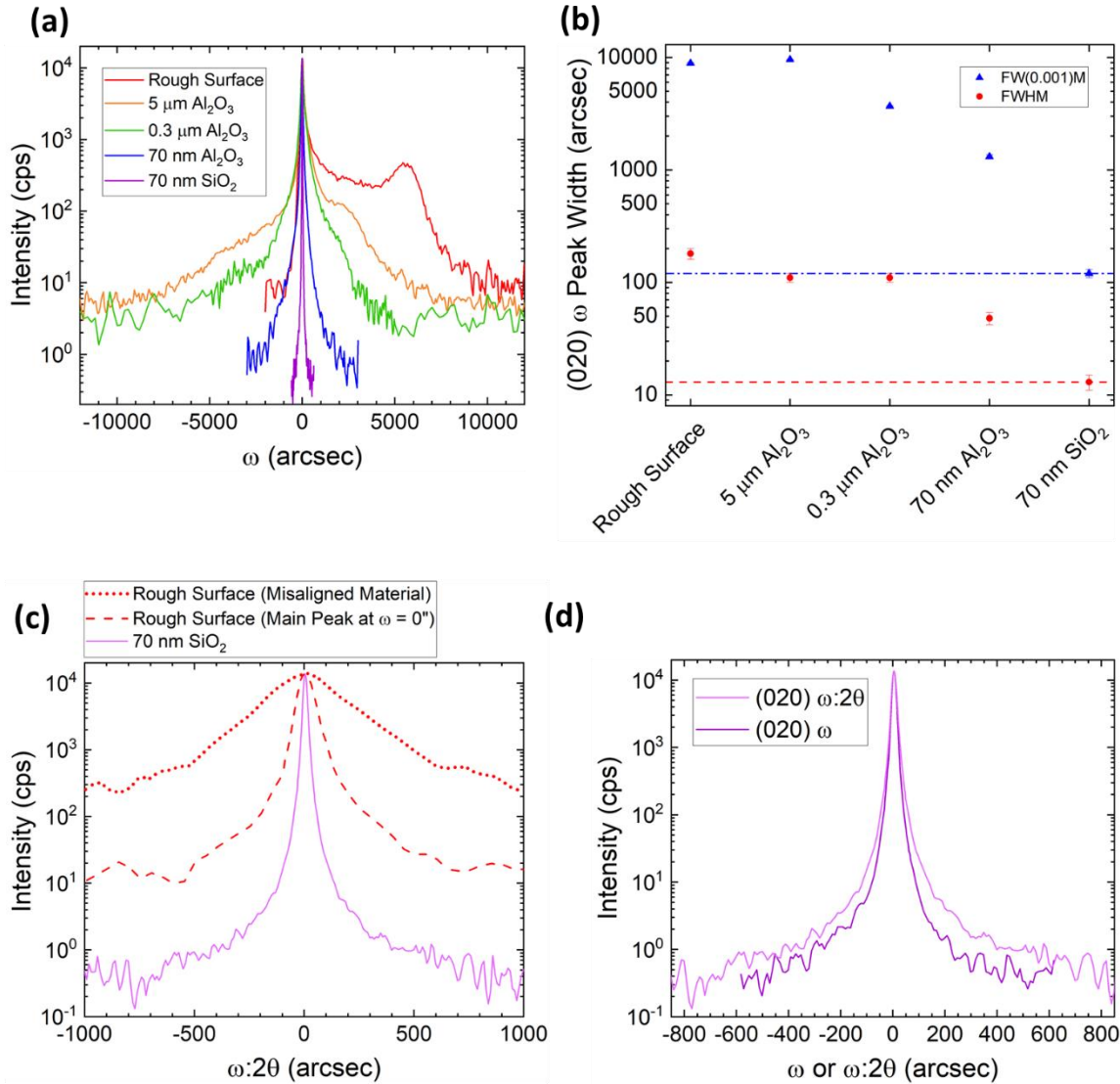
Figure 3.3. (a) Triple-axis X-ray diffraction rocking curves of the (020) β-Ga$_2$O$_3$ symmetric reflection for the (1) as-received rough surface (after wafer slicing and grinding), (2) 2 hours of 5 μm Al$_2$O$_3$ lapping, (3) 2 hours of 0.3 μm Al$_2$O$_3$ μm lapping, (4) 6 hours of 70 nm colloidal Al$_2$O$_3$ CMP, and (5) 10 hours of 70 nm colloidal SiO$_2$ CMP. (b) Corresponding FWHM and FW(0.001)M peak widths for each lapping and CMP step, where the dashed lines correspond the peak widths of commercially available pristine (010) β-Ga$_2$O$_3$ (FWHM is ~13" ± 2" and FW(0.001)M is ~120" ± 10"). (c) Triple-axis ω:2θ (020) β-Ga$_2$O$_3$ symmetric measurements of (1) as-received rough surface measured along the main peak in ω (i.e., at ω = 0"), (2) as-received

30

rough surface measured along the broader peak associated with misaligned material (i.e., at ω = 5600"), and (3) 10 hours of 70 nm colloidal SiO_2 CMP. The ω:2θ peak width is the broadest for the misaligned material, with a FWHM of 290" $\pm$ 40" compared to the ω:2θ peak measured at ω = 0", which has a FWHM of 70" $\pm$ 10". The FWHM after the CMP with SiO_2 is 18" $\pm$ 2". (d) Triple axis ω:2θ vs ω scans of the (020) β-Ga_2O_3 symmetric reflection after 10 hours of 70 nm colloidal SiO_2 CMP.
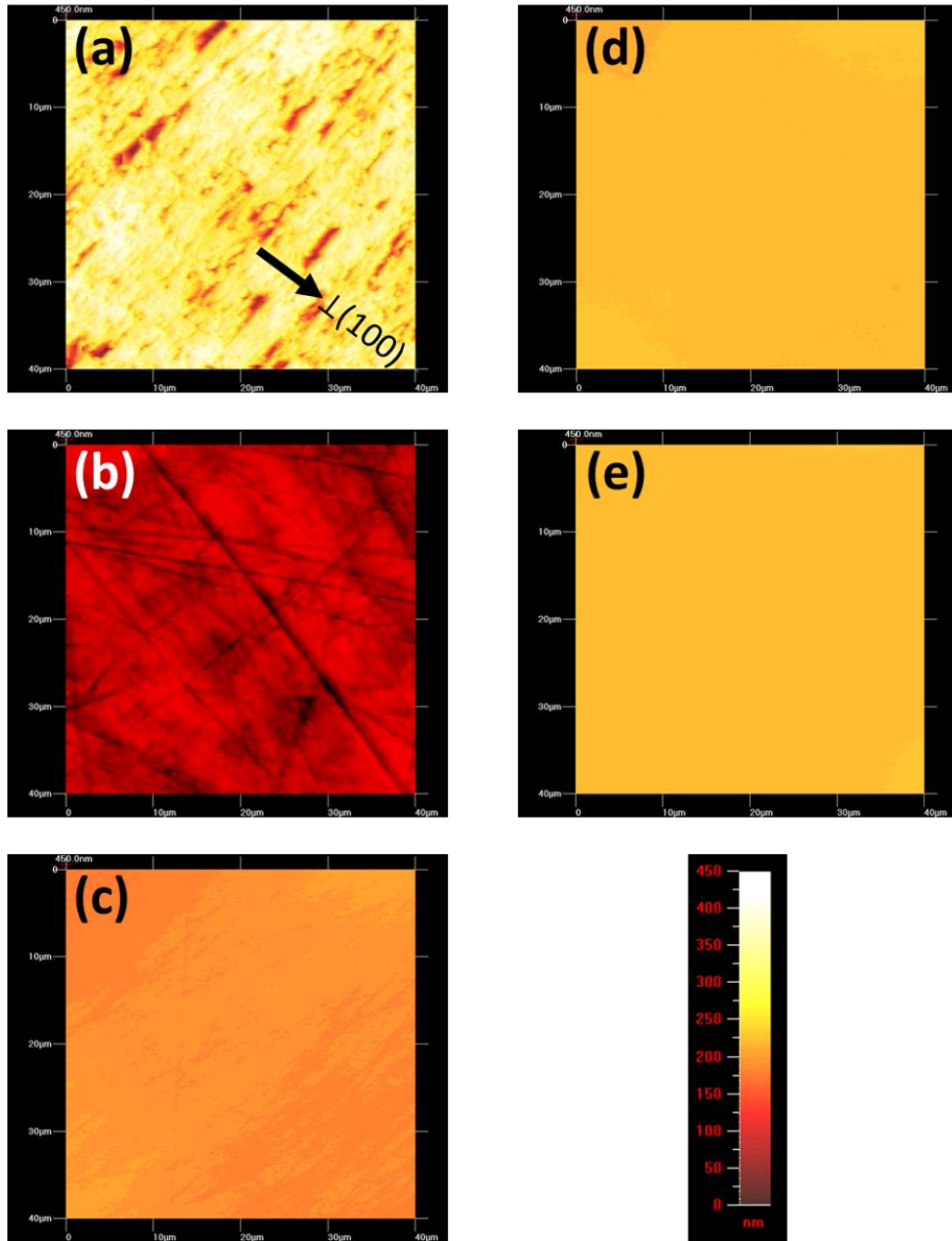
Figure 3.4. 40 × 40 μm^2 AFM scans of (a) as-received rough surface, (b) 2 hours of 5 μm Al$_2$O$_3$ lapping, (c) 2 hours of 0.3 μm Al$_2$O$_3$ μm lapping, (d) 6 hours of 70 nm colloidal Al$_2$O$_3$ CMP, and (e) 10 hours of 70 nm colloidal SiO$_2$ CMP. The rms surface roughness values are: (a) 60 nm, (b) 17 nm, (c) 1 nm, (d) 1 nm, and (e) 0.4 nm. All AFM scans share the same height scale and orientation.

Cross-sectional STEM images were used to image defects associated with the subsurface damage that contributed to the diffuse scatter intensity measured in the XRD rocking curves. A cross-sectional HAADF STEM image of the as-received rough face is shown in Figure 3.5(a). Note that AFM of the surface in Figure 3.4(a) shows surface voids and cracks, which corresponds to the surface morphology observed on the top surface of the HAADF STEM image in Figure 3.5(a). The HAADF STEM image shows that these cracks and voids propagate downwards toward the bulk of the substrate. The long vertical cracks and voids are speculated to be responsible for the second broad peak observed in the rocking curve shown in Figure 3.3(a). These cracks and voids induce severe lattice tilt, and the resulting tilt distortion is observed to be preferentially along the (100) cleavage plane. The depth of these vertical cracks and voids extends beyond the thickness of the TEM sample (~8 μm). After lapping with 5 μm Al_2O_3 for 2 hours, the vertical cracks and voids are no longer observed as shown in Figure 3.5(b), and the surface is flattened. Because ~40 μm of material was removed, the aforementioned vertical cracks and voids do not extend farther than 40 μm below the original damaged rough surface. Magnified BF images are shown in Figure 3.6 to enhance the contrast from dislocations. These high density of dislocations also make up the subsurface damage induced by wafer slicing and grinding (Figure 3.6(a,b,c)) and lapping (Figure 3.6(d,e,f). Each image is taken at a different depth from the surface. These dislocations contribute to the diffuse scatter intensity measured in the XRD rocking curves in Figure 3.3(a). In both cases for grinding or lapping, there is a relatively dark contrast region within the first 200 nm to 300 nm from the surface where the extent of damage is so large that dislocations are not resolvable. The near surface damage region is then followed by a region consisting of mosaic light contrast surrounded by dislocations. Qualitatively, the density of dislocations appears to decrease with depth, i.e., comparing the

contrast going from Figure 3.6(a) to Figure 3.6(c) and from Figure 3.6(d) to Figure 3.6(f). After the last CMP step using the softer colloidal SiO_2 slurry, the subsurface damage was removed, and uniform contrast is observed in the cross-sectional BF STEM image as shown in Figure 3.7. No dark contrast from dislocations is observed, which indicates that the cracks, voids, and dislocations were induced by the wafer slicing, grinding, lapping, and aggressive polishing steps and not due to the inherent crystalline quality of the β-Ga_2O_3.
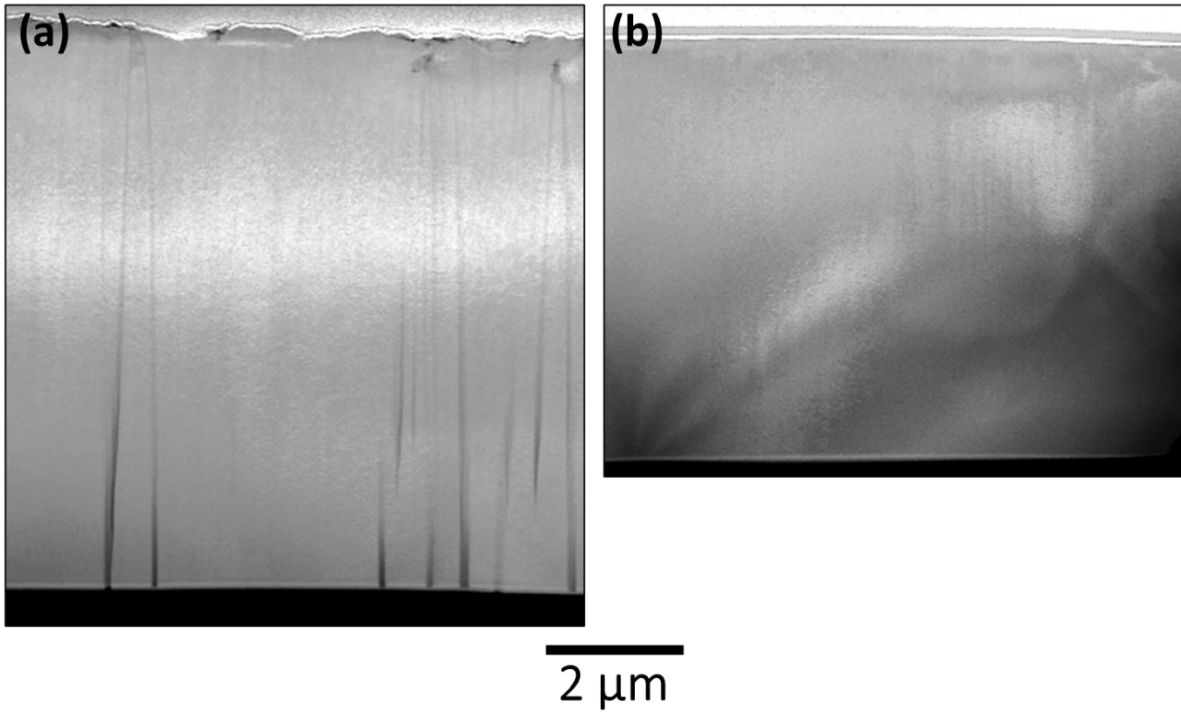
Figure 3.5. Cross-sectional HAADF STEM images of the (a) as-received rough face and (b) after lapping with 5 μm Al_2O_3 for 2 hours. The vertical features with dark contrast in that propagate from the surface to the bulk of the substrate are cracks and voids induced by the wafer slicing and grinding step. After removing ~40 μm of material, lapping flattens the surface and removes the subsurface voids and cracks. The STEM images were aligned to the [$\underline{1}$02] zone axis.
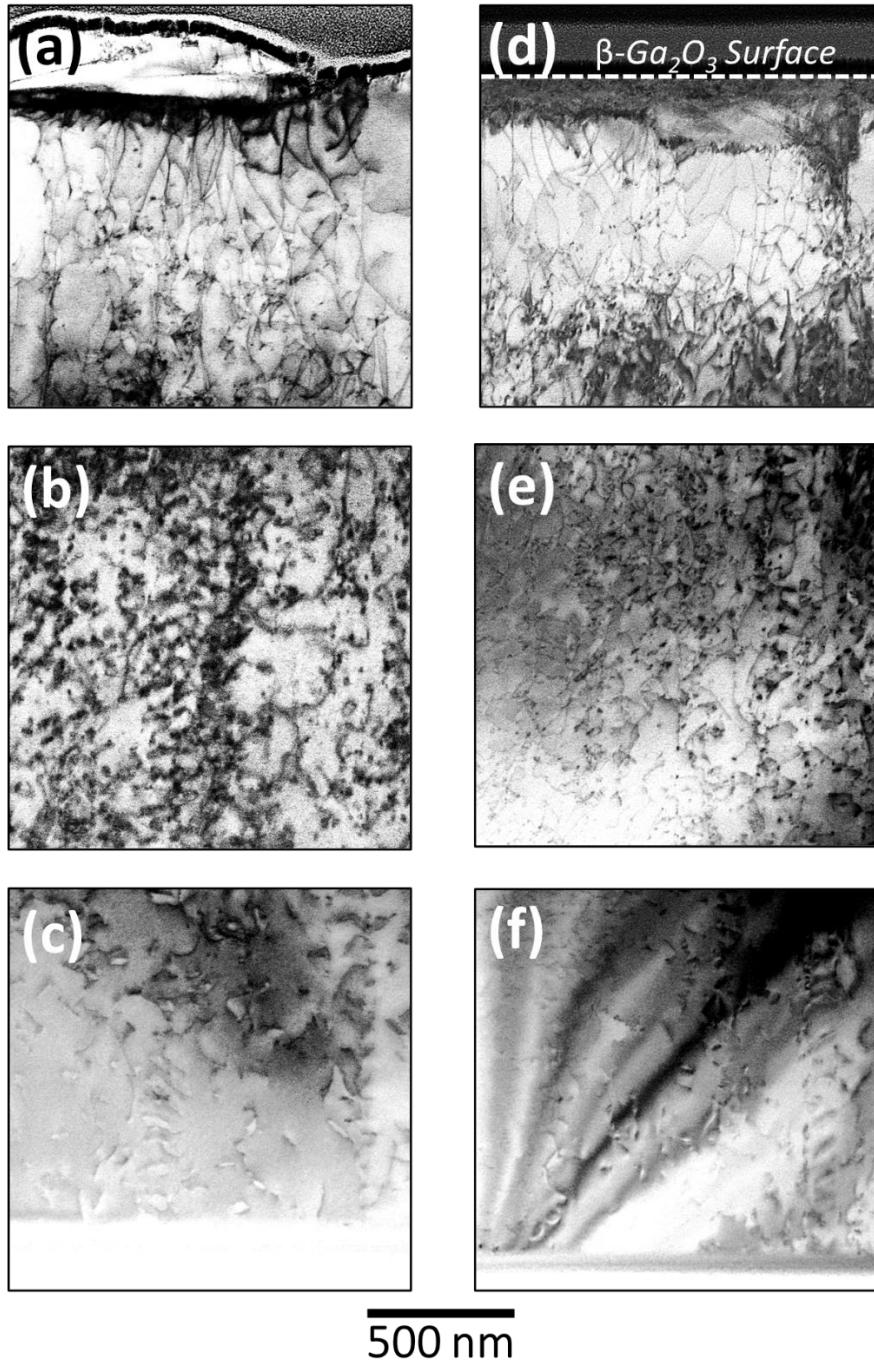
Figure 3.6. Cross-sectional BF STEM images (a,b,c) for the as-received rough side and (d,e,f) after lapping with 5 μm Al_2O_2 for 2 hours. For the as-received rough side images: (a) surface, (b) ~3 μm beneath the surface, and (c) ~8 μm beneath the surface. For the post-lapping images: (d) surface, (e) ~3 μm beneath the surface, and (f) ~6 μm beneath the surface. The dark contrast

features are dislocations that correspond to subsurface damage induced by wafer slicing and grinding for (a,b,c) and lapping (d,e,f). The diagonal dark bands observed in (c) and (f) are artifacts from bending contours of the TEM sample.
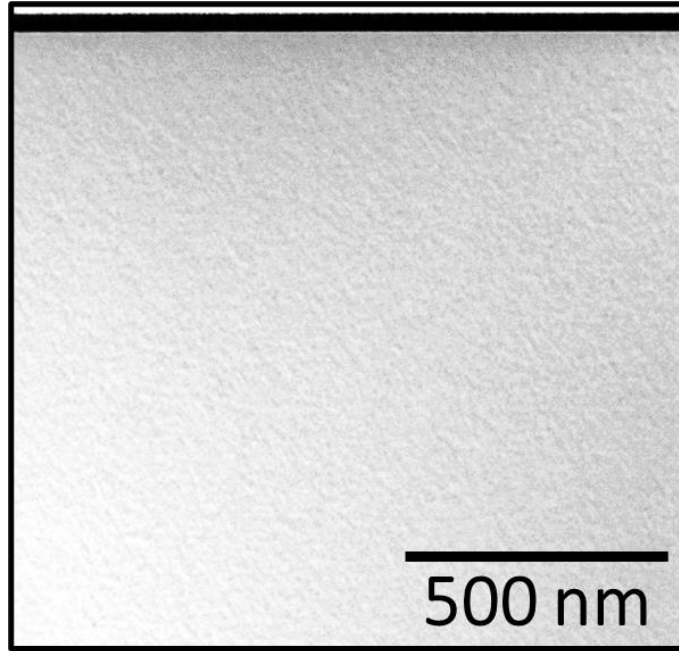
Figure 3.7. Cross-sectional BF STEM image after removing all the subsurface damage taken after the colloidal SiO_2 CMP. Uniform contrast is observed throughout the entire area imaged free of dislocations, cracks, and voids associated with subsurface damage. This STEM image was aligned to the [$\underline{1}$02] zone axis.

The SiO_2 slurry used to obtain subsurface-damage free and smooth β-Ga_2O_3 surfaces was suspended in a NaOH-based solvent and the material removal rate was ~0.4 μm/hr. Work by Huang et al.,[1,2] proposed that NaOH reacts with β-Ga_2O_3 to form a passivating gallium hydroxide salt layer. NaOH has been shown to exhibit extremely slow free etch rates at room temperature, on the order of a few nm/hr.[23] Hence, we propose that the SiO_2 particles provide the mechanical

abrasion to remove the passivated hydroxide surface layer, causing the material removal rate to increase by 2 orders of magnitude compared to the free etch rate of NaOH alone. This is analogous to the polishing mechanism in our previous CMP studies for various III-V materials where bleach and citric acid were used to oxidize the substrate surfaces and the oxide was removed mechanically (the polishing pad was sufficient for the mechanical abrasion in those cases).[7,9,10]

The measured material removal rates for the various abrasives used for lapping and CMP are shown in Figure 3.8. The analysis presented in this current work can be used to optimize lapping and CMP parameters to achieve both smooth surfaces (< 0.5 nm rms roughness) and subsurface-damage-free material simultaneously. Work by Blevins et al.,[14] estimated that wafer slicing induced 75 μm of subsurface damage. They then optimized their polishing parameters to remove 100 μm and reduced the total processing time from ~250 hours to ~28 hours. Using the results presented in this current work, the processing time to achieve smooth, damage-free surfaces would be further reduced to ~17 hours: (1) 4 hours of 5 μm Al_2O_3 to remove ~80 μm of material, (2) 1.5 hours of 0.3 μm Al_2O_3 to remove ~14 μm of material, (3) 1.5 hours of colloidal Al_2O_3 to remove ~2 μm of material, and finally (4) 10 hours of colloidal SiO_2 to remove ~4 μm of material. The removal rate using colloidal SiO_2 was ~0.4 μm/hr, which is suitable for the CMP of thin layers exfoliated using ion implantation. For example, our previous work[17] used He ion implantation to exfoliate ~0.7 μm thick (010) β-Ga_2O_3 layers, which had surface roughnesses of ~4 nm post-exfoliation. Polishing for at least 1 minute with colloidal SiO_2 would smoothen the exfoliated surfaces and remove ~7 nm of material. Even finer control over the removal rate could be achieved by reducing the colloidal SiO_2 concentration. Demonstrated with other materials systems over a weight percent range of 0% to 15%, reducing the abrasive particle concentration

reduces the material removal rate.[24,25,26] The weight percent of colloidal SiO_2 used in this current work was ~40 wt%, so reducing the colloidal SiO_2 concentration to achieve even finer removal rates is expected to be feasible.
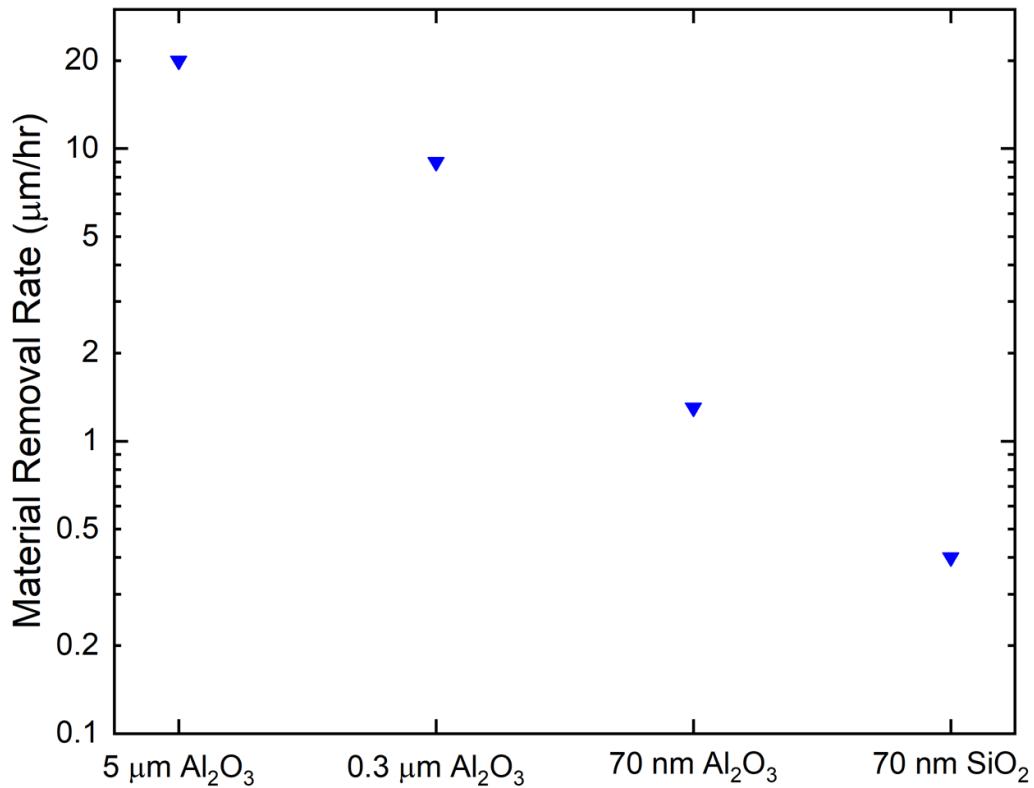
Figure 3.8. Material removal rates measured in AFM from changes in fiducial marker depths made by FIB for the different lapping and CMP slurries used in this study. Lapping was performed with 5 μm Al_2O_3 and 0.3 μm Al_2O_3 particles suspended in DI water. CMP was performed with 70 nm colloidal Al_2O_3 in a NaClO-based solvent and 70 nm colloidal SiO_2 in a NaOH-based solvent.

3.4 Conclusion

CMP parameters of (010) β-Ga_2O_3 were optimized to achieve both smooth (< 0.5 nm

rms) surfaces and subsurface-damage-free material simultaneously. 1 kPa of applied pressure

with colloidal silica slurry on poromeric polyurethane polishing pads rotating at 30 RPM were

found to be the optimal parameters for (010) β-Ga_2O_3. The corresponding (020) β-Ga_2O_3 rocking

curve FWHM and FW(0.001)M peak widths were ~13" and ~120", respectively, which matches

the widths of commercially available pristine β-Ga_2O_3. Pressures $\geq$ 3 kPa were found to induce

subsurface damage despite maintaining smooth surfaces. X-ray rocking curves were invaluable

in characterizing the effects of various lapping and polishing steps and the diffuse scatter

intensity measured by the peak widths below the half max were most sensitive to subsurface

damage. Cross-sectional STEM images showed that wafer slicing and grinding can induce long

vertical cracks and voids that extend ~40 μm from the surface. These cracks and voids appear to

cause severe distortion that tilted the lattice ~1.7° preferentially towards the (100) cleavage

plane. STEM images show that after the final CMP step, all of the subsurface damage was

removed and the wafer was free of voids, cracks, and dislocations. Material removal rates were

measured for various lapping and polishing steps. 5 μm Al_2O_3 and 0.3 μm Al_2O_3 lapping resulted

in removal rates of ~20 μm/hr and ~9 μm/hr, respectively. Colloidal Al_2O_3 and colloidal SiO_2

CMP resulted in removal rates of ~1.3 μm/hr and ~0.4 μm/hr, respectively. We provide a

systematic approach for CMP optimization to determine appropriate parameters that can be

applied to other materials.

3.5 References

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Chapter 4: Exfoliation of (010) β-Ga$_2$O$_3$ Using Ion Implantation

4.1 Introduction

While β-Ga$_2$O$_3$ has one of the lowest thermal conductivity values compared to other wide bandgap semiconductors,[1,2] integration with higher thermal conductivity materials can play a key role in implementing β-Ga$_2$O$_3$ in next-generation high-power applications. In the current literature, heterostructures incorporating thin films of β-Ga$_2$O$_3$ grown on various materials such as GaN[3,4] and sapphire[5,6] have already been reported. However, due to the lattice mismatch between dissimilar materials, epitaxy can achieve only a limited number of orientations of β-Ga$_2$O$_3$ depending on the growth substrate.[7,8] Orientation is a crucial parameter to control since many of the properties of β-Ga$_2$O$_3$ are anisotropic due to its low-symmetry monoclinic crystal structure. For example, the [010] direction exhibits the greatest thermal conductivity while along the [100] direction the thermal conductivity is lower by ~ 60%.[9] This is especially important for heterojunction structures since the thermal conductivity of a heterojunction interface is dominated by the material with the lowest thermal conductivity.[10] A theoretical study of the electronic properties of β-Ga$_2$O$_3$ showed that the hole effective mass may range from $0.40m_h$ to $40m_h$ depending on the crystallographic direction, where m_h is the hole rest mass.[11] Coefficients of thermal expansion (CTE) are pertinent to optimizing processing parameters and, as will be shown later, the CTE along the unit cell axes are not the same, with the a-axis having the lowest value and b-axis the largest.[12] Thus, materials integration via direct wafer bonding will enable a myriad of both orientation and material combinations not realizable through epitaxy.[8] Clearly it is essential to have access to any arbitrary orientation in order to fully utilize the benefits of β-Ga$_2$O$_3$.

Recent work by Kwon et al.,[13] and Tadjer et al.,[14] have demonstrated a mechanical exfoliation method using tape for obtaining ~300 nm to 530 nm thick (100)-oriented, small area β-Ga$_2$O$_3$ layers and transferring the layers to various substrates such as sapphire and diamond. That approach takes advantage of the fact that the (100) plane is one of the two primary cleavage planes[15,16] (the other is (001)) for β-Ga$_2$O$_3$. Some of the challenges associated with that approach are its incompatibility with large-scale processing and limited crystallographic orientation, i.e. only the (100) and (001) cleavage planes are suitable for this method. Areas of up to only ~0.4 mm^2 were successfully transferred to substrates using this mechanical approach.[14] Additionally, Kwon et al.,[13] points out that the thickness of the exfoliated layer from using the tape approach is difficult to control and recycling substrates for subsequent exfoliation becomes more difficult with each extraction. On the other hand, ion implantation has been shown to exfoliate large wafer-scale areas for many semiconductors.[17,18] When used in conjunction with direct wafer bonding, large areas of thin layers can be transferred to a handle substrate.[18] In addition, thickness is a very well-controlled parameter for exfoliation using ion implantation, and can range from nanometers to microns,[19] depending on the implant energy. Post-exfoliated substrates are also easily recyclable for subsequent exfoliation.[18,20,21]

First introduced to exfoliate layers of silicon, ion implantation of hydrogen[17] or helium[22] and subsequent annealing was used to produce silicon-on-insulator structures. Under the appropriate annealing conditions, an implanted substrate surface will blister from the nucleation and growth of hydrogen or helium gas bubbles present near the implanted species projected range beneath the substrate surface. Surface blistering is an indication of successful exfoliation. If an implanted substrate is bonded to a handle substrate prior to any blister-inducing anneal, uniform wafer splitting can be achieved, resulting in a large-area thin layer transferred to a

handle substrate.[17,18] The current literature and previous efforts have further extended the efficacy, analysis, and understanding of hydrogen or helium implantation to silicon,[23–25] germanium,[26] III-V materials,[18,27–29] and II-VI materials[30] where controllable wafer-scale areas of thin layers for various semiconductor materials were successfully exfoliated and transferred. Using ion implantation for thin-film integration naturally fits in the large-scale setting, as outlined by Hayashi et al.:[18] (1) hydrogen or helium ions are implanted in a substrate, (2) the implanted substrate and a handle substrate are direct wafer bonded, and (3) the bonded structure is annealed to promote exfoliation. Regarding β-Ga_2O_3, there have been recent reports of direct wafer bonding of 655-μm and 680-μm thick β-Ga_2O_3 substrates with SiC by Lin et al.,[10] and Xu et al.,[31] respectively, but there are currently no reports on exfoliating β-Ga_2O_3 using ion implantation. The ability to exfoliate β-Ga_2O_3 from non-cleavage plane surfaces, such as (010), makes new device structures possible.

4.2 Experimental Details

Epi-ready, unintentionally Si-doped (concentration of ~1×10^{17} cm^{-3}) Novel Crystal Technology, Inc.[32] (010) β-Ga_2O_3 substrates were implanted at room temperature with He$^+$ at an energy of 160 keV and a dose of 5×10^{16} cm^{-2}. The implanted substrates were then annealed at 200 °C for 12 hours followed by 500 °C for up to 6 hours in air on a hot plate. The samples were in direct contact with the hot plate and Al foil was used to cover the samples. This anneal sequence was based on previous work on exfoliation via ion implantation with other semiconductor materials.[18,20,21,25–30] The low temperature step is associated with He blister nucleation which could be correlated to changes in X-ray diffraction (XRD) ω curves and the higher temperature step is correlated with growth of the blisters. After annealing at 200 °C for 12

hours, the XRD ω peak broadened but did not exhibit blistering at times shorter than 1 hour at 500 °C. A high-resolution Bruker-JV D1 diffractometer using triple-axis diffraction[12,33,34] was used to measure ω:2θ and ω scans of the (020) symmetric reflection. Both atomic force microscopy (AFM) and Nomarski microscopy images were taken to monitor the surface morphological evolution with annealing. An FEI TITAN S/TEM performed at an accelerating voltage of 300 keV was used to obtain scanning transmission electron microscopy (STEM) images of the implanted region with the samples aligned to the [$\underline{1}$02] zone axis. The implantation parameters were used with SRIM[35] to calculate the projected range of the He ions and the displaced atom profile, which were then compared to the STEM measurements.

4.3 Results and Discussion

The symmetric (020) ω:2θ line scans and ω rocking curves of the pre-annealed (post-implanted) and post-annealed (after the 200 °C and 500 °C anneal steps) implanted substrate are shown in Figure 4.4.1. In this case, the substrate was first annealed at 200 °C for 12 hours then subsequently annealed at 500 °C for 6 hours. At the pre-anneal stage, oscillations are observed to the left of the main substrate peak in the ω:2θ scan as shown in Figure 4.4.1(a). These oscillations are associated with tensile strain induced by the implantation caused by the He ions displacing both the Ga and O atoms from lattice sites. This is a common occurrence observed in previous work with implanting other semiconductor materials.[18–21, 25–30] The furthest left fringe in the ω:2θ scan typically corresponds to the maximum strain in the implanted region,[19] which is about 1.01%. The strain oscillation intensity decreased and shifted slightly after annealing at 200 °C for 12 hours as shown in the ω:2θ scan in plots (i) through (iii) of Figure 4.1(a). This indicates a small amount of diffusion and reconfiguration of the implant-related defects. The ω

scans for the as-implanted and annealed 200 °C samples show full width at half maximum (FWHM) values of 17" in both cases (which is also the same as the non-implanted material). However, the ω scan after the 200 °C anneal shows peak broadening at the tails of the peak, e.g. the full width at thousandth maximum (FW(0.001)M), from the pre-anneal state (310") to this annealed state (515") as shown in Figure 4.1(b). While FWHM values are more commonly reported, previous work[21,25] demonstrated that the tails of ω peaks are more sensitive to changes in crystallinity, i.e. mosaicity or tilt in the exfoliated layer. This tail broadening in the ω scan combined with the slight change in the strain profile from the ω:2θ scan is attributed to He gas bubble nucleation at approximately the implant projected range beneath the substrate surface in accordance with earlier work on silicon.[25] After further annealing at 500 °C up to 6 hours, the implant-induced strain was fully relieved, as confirmed by the absence of the strain fringes in the ω:2θ scan as shown in Figure 4.1(a). In the corresponding ω scan, the FW(0.001)M further broadened to 915" and the FWHM also broadens to 44". The further broadening of the ω peak and loss of the strain is attributed to larger scale defects associated with the implanted He. These results are consistent with exfoliation in other materials in which a lower temperature step (200 °C in this study) was used to initiate He bubble nucleation while the higher temperature step (500 °C) was used to induce He bubble growth through diffusion.[27]
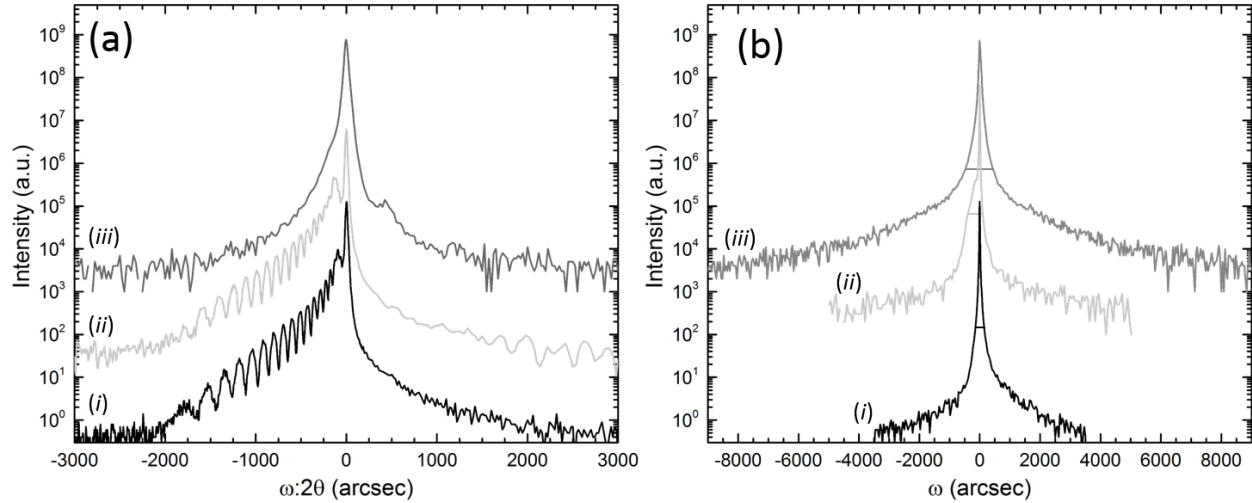
Figure 4.1. ω:2θ (a) and ω (b) triple-axis XRD scans of the (020) symmetric reflection for (i) pre-anneal (post-implant), (ii) anneal at 200 °C for 12 hours, and (iii) anneal at 200 °C for 12 hours followed by 500 °C for 6 hours. The horizontal solid bars in (b) mark the FW(0.001)M of each ω peak.

The surface also showed significant differences before and after the 500 °C step and confirms the exfoliation. The surface was then examined with AFM and Nomarski optical measurements as shown in Figure 4.2 and Figure 4.3, respectively. 40 μm × 40 μm AFM scans of the post-implanted β-Ga$_2$O$_3$ surface prior to any annealing showed the same surface morphology and roughness as the pre-implanted surface, which had a surface root mean square (RMS) roughness of ~ 0.5 nm, demonstrating that the as-implanted samples are suitable for subsequent wafer bonding. Figure 4.2(a) shows the AFM image of the 200 °C annealed sample. The roughness remained low (~ 0.8 nm) after the low temperature annealing step and exhibited the same morphology as the pre-annealed surface. Figure 4.2(b) shows significant blistering occurs with the 500 °C annealing step (6 hours annealing shown here). On a larger scale (600 μm × 450 μm shown here), the Nomarski image in Figure 4.3(a) also shows no features on the surface after the 200 °C anneal. However, as shown in Figure 4.3(b), a uniform distribution of

47

surface blisters with an 18 μm average diameter is observed over the entire implanted surface

with over one third of the surface covered with blisters after the 500 °C anneal. Not shown here,

it was observed in both Nomarski and AFM images that significant blistering occurred even after

one hour at 500 °C. The average blister size after annealing at 500 °C for one hour was 1.4 μm,

which was measured from a 600 μm × 450 μm Nomarski image. The observed surface blistering

and flaking is an indication that exfoliation along the (010) plane for β-Ga$_2$O$_3$ can be readily

achieved, which was an important step previously demonstrated with other materials.[17,18] For the

case of exfoliation or wafer splitting, the implanted material would need to be bonded to another

substrate prior to the high temperature anneal step. In a bonded structure, the bulk of the

substrate below the projected range provides the necessary mechanical support to force the

energy released during He bubble formation to cause wafer splitting instead of surface

blistering.[17]
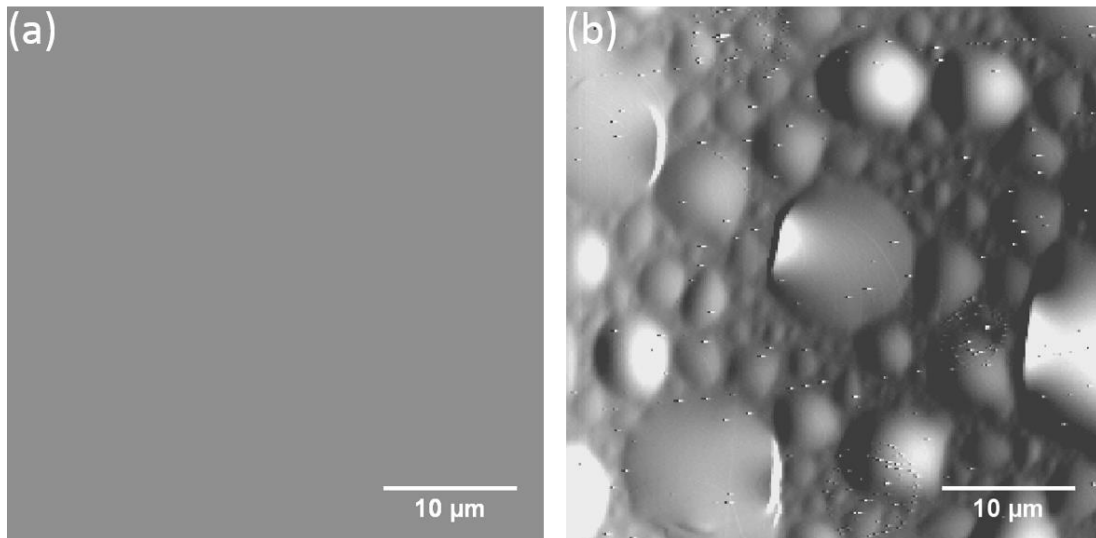
Figure 4.2. AFM scans of the surface after: (a) annealing at 200 °C for 12 hours and (b) annealing at 200 °C for 12 hours followed by 500 °C for 6 hours. Both scans have the same height scale (150 nm).
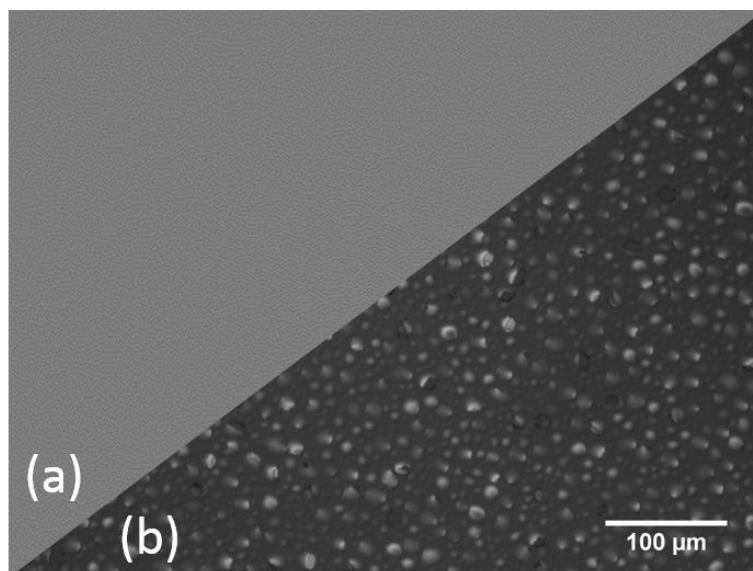
Figure 4.3. Nomarski images of surfaces (a) annealed at 200 °C for 12 hours and (b) annealed at 200 °C for 12 hours followed by 500 °C for 6 hours.

It can be seen from Figure 4.3(b) that some of the blisters completely exfoliated. AFM scans of these exfoliated regions were then measured to examine the exfoliated region morphology as shown in Figure 4.4. The depth of the two exfoliated blisters shown in Figure 4.4(a) were both ~ 0.6 μm. The results from SRIM[35] simulation calculations are in good agreement with these AFM measurements, which predict the ion projected range to be 0.64 μm with a straggle of 0.15 μm and a displacement per atom peak at a depth of 0.57 μm with a straggle of 0.21 μm. In both of these regions shown in Figure 4.4(b) and (c), distorted rhombus features are observed. However, while there may be planar relationships for this observed morphology, we have other AFM scans of these exfoliated regions and found that the shapes are somewhat distorted by the AFM measurement itself. Therefore, we do not wish to make a strong claim about the orientational relationships here and plan to assess this issue later. The average minor axis and major axis length for the features shown in Figure 4.4(b) are 91 nm and 123 nm, respectively, while for Figure 4.4(c) they are 85 nm and 125 nm, respectively. The formation of

49

these features at the projected range during the anneal process correspond to the observed widening of the ω rocking curves shown in Figure 4.1(b). The exfoliated regions exhibited a ~ 4 nm RMS roughness, which can be smoothened and the features removed with chemical mechanical polishing.
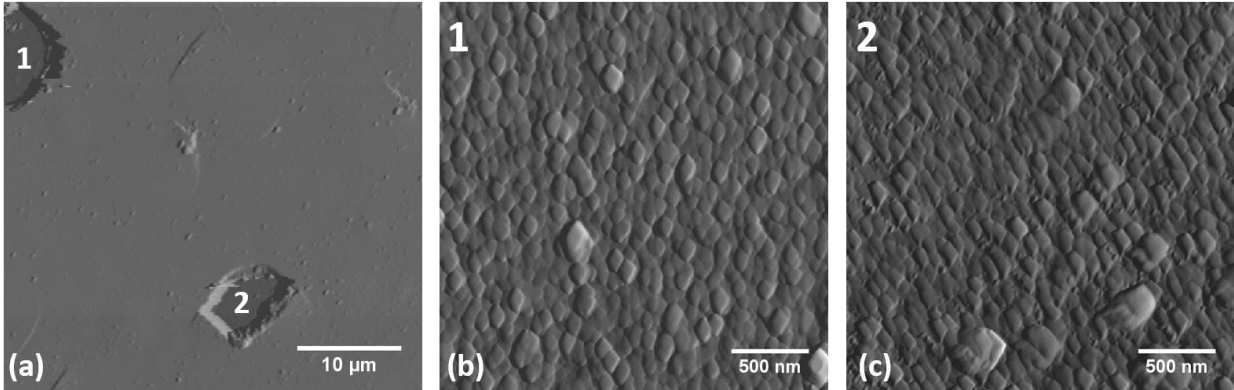
Figure 4.4. A 40 μm × 40 μm AFM scan after the 500 °C for 6 hours step (a) capturing two fully exfoliated blisters (the height scale is 1 μm). Figures (b) and (c) are 2.5 μm × 2.5 μm AFM scans of the exfoliated areas in (a), both having the same height scale of 50 nm. Note that Figure 4.2(b) is similar to Figure 4.4(a) but the height scale is much larger for Figure 4.4(a) to better show the depth of the craters but the individual blisters are not as readily observed.

The TEM samples of both the pre-anneal and post-annealed (500 °C for 1 hour) implanted substrate were aligned along the [$\underline{1}$02] zone axis. The high-angle annular dark-field (HAADF) STEM images are shown in Figure 4.5. The STEM image of the as-implanted sample shown in Figure 4.5(a) shows a dark band parallel to the surface at a depth starting approximately at 0.6 μm. The dark contrast band is ~ 0.01 μm wide and is likely due to a relatively high He content at the projected range, which was ~ 11%. Here, the SRIM[35] simulations are also consistent with the STEM results. After the combined 200 °C and 500 °C

anneal, a relatively uniform crack feature is observed. The height of the crack corresponds to the height of the blister directly above on the surface, which is ~25 nm for this particular blister shown in Figure 4.5(b). The average depth of the crack from the surface is 0.66 μm. To obtain other thicknesses using He ion implantation, the He ion implantation energy would be adjusted.
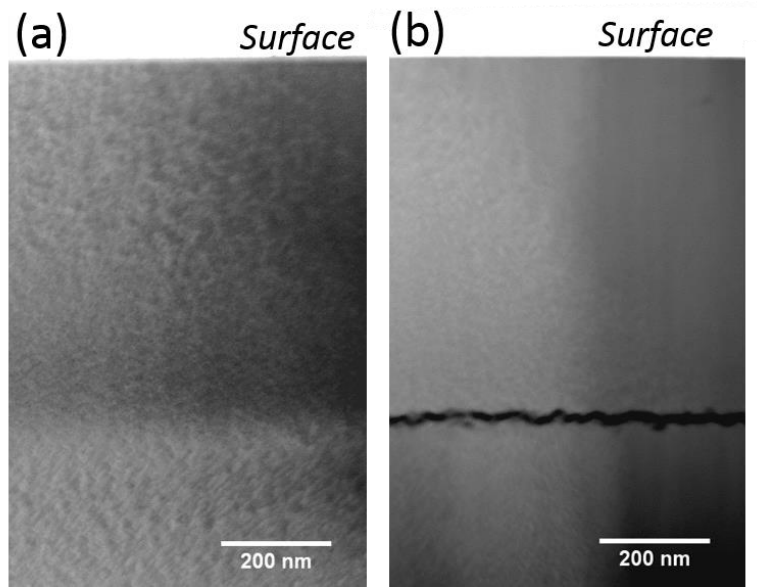
Figure 4.5. HAADF STEM images of the implanted region for (a) post-implant, pre-anneal and (b) post-anneal at 500 °C for 1 hour. The sample was aligned to the [$\underline{1}$02] zone axis. The measured projected range is approximately 0.66 μm.

These results can be coupled with the recent studies that have demonstrated that β-Ga$_2$O$_3$ full wafers can be bonded to other substrates. In one study, β-Ga$_2$O$_3$ was bonded to SiC at room temperature and subsequently annealed at 200 °C to remove some of the damaged interface.[31] However, there was little further analysis concerning the thermal or electrical properties of the bond. In the other report, good thermal and electrical transport across a bonded β-Ga$_2$O$_3$ full wafer / SiC full wafer interface was achieved after annealing at 1000 °C.[10] In both of these cases, the wafers were placed in a vacuum chamber and exposed to an energetic argon beam to facilitate subsequent bonding. Upon bonding, the near surface regions include a damaged layer

on each side of the bond that is typically a few nm thick. The wafer pairs that received the argon

beam treatment must be annealed at elevated temperatures to remove this damage and to improve

the interfacial properties.[36] Our results fit well with the bonding requirements. For example, β-

Ga_2O_3 could be bonded to another wafer using the exposure to an argon beam or simply using a

passivation treatment and subsequent annealing.[18,37] The annealing sequence described here

would then lead to the transfer of the thin layer (e.g. ~ 0.66 μm here but that could easily range

from 60 nm for 10 keV to 1.2 μm for 400 keV using commercial implanters or even thicker

layers using MeV implantation). We note that (at least part of) the 200 °C annealing step can be

employed prior to the bonding since the surface roughness does not change during this step.

After bonding, there can be continued annealing at a low temperature to further improve the

bonded interface and potentially remove any interface damage (e.g. from the argon beam

treatment[31,36]) and then raised to a high temperature to achieve exfoliation.

4.4 Conclusion

In this study, evidence for β-Ga_2O_3 exfoliation along the non-cleavage (010) plane using

He ion implantation is provided. Surface blistering and flaking were observed after annealing at

200 °C for 12 hours followed by 500 °C for 1 to 6 hours. The anneal temperatures employed in

this study are compatible with current direct wafer bonding procedures of β-Ga_2O_3 and SiC

reported in literature, which use temperatures of 200 °C[10] or 1000 °C[31] to strengthen the

heterojunction bond. The mechanism of exfoliating with ion implantation is applicable to a wide

variety of semiconductor materials and works for arbitrary surface orientations.[18–21,25–30] The

general mechanism is the nucleation and growth of helium bubbles (or hydrogen as in the

literature for other materials) at the projected range beneath the substrate surface to achieve

surface blistering or wafer splitting. While this experiment was performed on a (010)-oriented β-Ga$_2$O$_3$ substrate, this process would naturally extend out to other orientations of interest and is expected to lead to materials integration opportunities to take advantage of the desirable properties of β-Ga$_2$O$_3$ (e.g., high field strength) while mitigating some of the less desirable properties (low thermal conductivity).

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Chapter 5: Coefficients of Thermal Expansion of β-Ga₂O₃

5.1 Introduction

Integrating β-Ga₂O₃ with other materials to optimize device performance and realize

novel structures is a promising way to exploit the beneficial properties of β-Ga₂O₃ while

mitigating its shortcomings.[1,2] In particular, direct wafer bonding is a materials integration

approach that offers a pathway to achieve heterostructures for which epitaxial or other deposition

methods are ill-suited.[3,4] However, detailed understanding of many wide bandgap materials and

other semiconductor direct bonded structures remains limited. Thus, experiments and

applications involving both β-Ga₂O₃ homojunctions and heterojunctions will require reliable

knowledge of various materials properties, such as coefficients of thermal expansion (CTE). β-

Ga₂O₃ has a monoclinic crystal structure with lattice parameters a = 1.2214 nm, b = 0.30371 nm,

c = 0.57981 nm, and β = 103.83°, where β is the angle between the 'a' and 'c' axes.[5]

Understanding thermal expansion of single crystalline β-Ga₂O₃ is important in determining

heteroepitaxial and heterojunction strains caused by thermal mismatch in order to, for example,

select proper materials for either epitaxial growth or bonding and assess the structural and

electrical properties in the epitaxial/bonded structures, as demonstrated for other materials

previously.[6–10] In fact, some interesting combinations of β-Ga₂O₃ have already been realized,

including combinations with Al₂O₃,[11,12] GaN,[13–15] ZnO,[16] MgO,[17] and others.[18–22] For general

processing at elevated temperatures of β-Ga₂O₃, whether through epitaxy or direct wafer

bonding, an understanding of the coefficient of thermal expansion (CTE) is especially crucial for

materials combinations with large differences in CTE values.

In the current literature, CTE studies on β-Ga₂O₃ have been reported by Villora et al.,[23]

and Orlandi et al.[24] Powder (polycrystalline) β-Ga₂O₃ was used by Villora et al.,[23] to determine

CTE values from room temperature to 1000 °C. However, few experimental details are provided

and the reported CTE values are not consistent with others reported in literature.[24,25] Orlandi et

al.,[24] reported to have measured CTE values of single crystal β-Ga$_2$O$_3$ over a temperature range

of room temperature to 427 °C; however, this study milled bulk single crystalline β-Ga$_2$O$_3$ into a

fine polycrystalline powder prior to determining the CTE values. Milling can produce strained

surface regions which may make up an appreciable fraction of each grain. The impact of surface

reactions would increase as a result of increased surface area due to milling and may introduce

distortions in the apparent changes in the lattice parameters at various temperatures. In fact, it

can be seen experimentally that the CTE values of other large bandgap semiconductor materials

do vary between single crystalline and polycrystalline forms of a material. For example, the

differences in CTE between polycrystalline and single crystalline GaN along the 'a' and 'c' axes

are ~11% and ~19%, respectively,[26] where CTE of the polycrystalline material is higher than the

CTE of the single crystalline form. For AlN, the differences along the 'a' and 'c' axes are ~55%

and ~29%, respectively.[26] Additionally, the use of powder samples to determine lattice

parameters introduce systematic errors including eccentricity, absorption, and zero errors.[27–29]

5.2 Experimental Details

The CTE measurements reported in this work were performed on single crystalline β-

Ga$_2$O$_3$ substrates. This approach overcomes complications associated with using powder samples

as reported previously,[23,24] especially if the powders were produced by milling of single

crystals.[24] Additionally, the temperature range at which the CTE values were measured spanned

from room temperature to 1000 °C, which is greater than what was previous used by Orlandi et

al.,[24] who went up to 427 °C. Understanding how β-Ga$_2$O$_3$ behaves at elevated temperatures is

expected to provide insight into the usefulness of this material as a substrate for epitaxial deposition and thus, the temperature range used in this study is more technologically relevant for modern growth conditions and useful for current interests.[14,15,30]

A Bede D1 high-resolution X-ray diffractometer and Anton-Paar high temperature stage were utilized in this study. The X-ray source is Cu Kα_1 using a Göbel mirror[31] and a (220) silicon channel cut crystal collimator. The Anton-Paar stage has a platinum-based heating element that holds the sample and is encased in a graphite dome with atmosphere-control. The samples in the high temperature stage were maintained in a N_2 ambient atmosphere for this study. The coefficients of thermal expansion were determined over a temperature range of room temperature to 1000 °C. Measurements were repeated at 50 - 200 °C intervals and cycled from room temperature to the maximum temperature (1000 °C) and back to room temperature to confirm that there were not any non-elastic changes to the lattice parameter as a function of the annealing process itself. Additionally, under these experimental conditions β-Ga_2O_3 does not undergo any phase changes.[3,32–34] Samples from a commercial 2-inch ($\underline{2}$01) oriented single crystalline β-Ga_2O_3 wafer were used, which had thicknesses of approximately 670 µm. The ($\underline{4}$ 0 2), ($\underline{6}$ 0 3), and ($\underline{8}$ 0 4) symmetric reflections were employed as well as ($\underline{12}$ 0 3), ($\underline{12}$ 0 4), ($\underline{6}$ 2 3), and ($\underline{8}$ 2 4) asymmetric reflections as shown in Figure 5.1. The interplanar spacing (d-spacing) values from each of these reflections were used for regression diagnostics combined with nonlinear least-squares to refine unit cell parameters,[35] where the relationship between d-spacing and miller indices (hkl) for the monoclinic crystal system is:

$$\frac{1}{d^2} = \frac{1}{\sin^2\beta}\left(\frac{h^2}{a^2} + \frac{k^2\sin^2\beta}{b^2} + \frac{l^2}{c^2} + \frac{2hl\cos\beta}{ac}\right). \qquad (5.1)$$
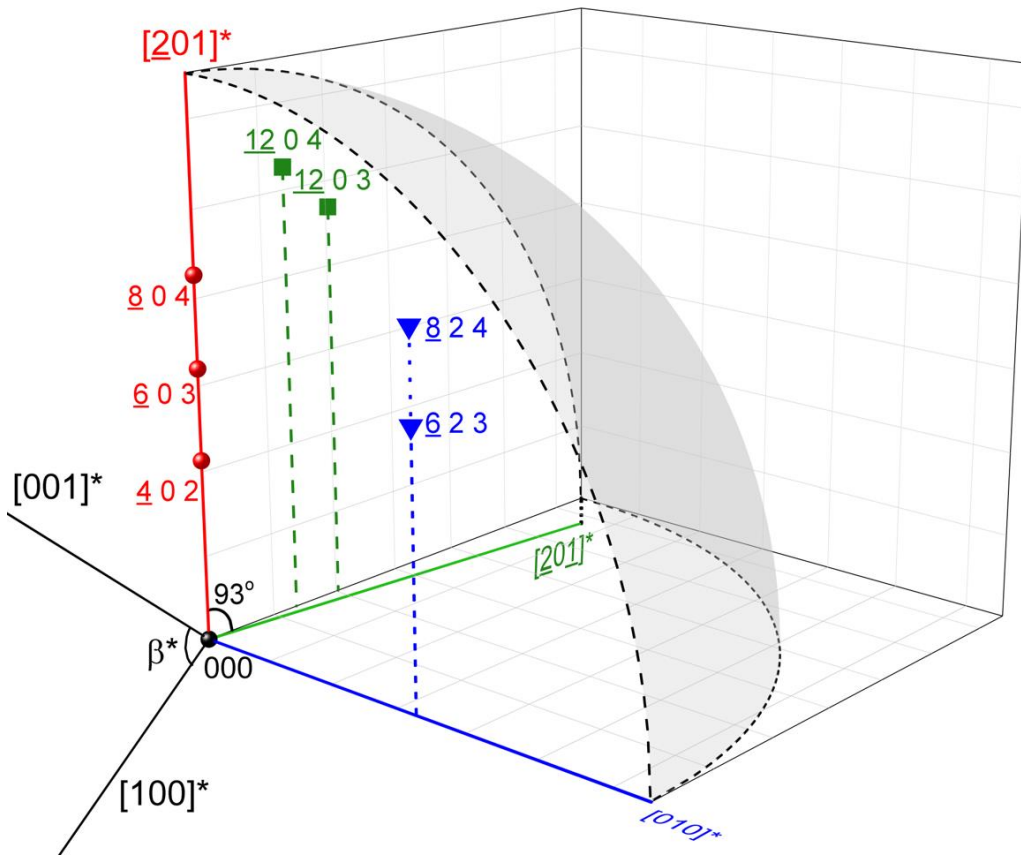
Figure 5.1. Reciprocal lattice points investigated in this study. The symmetric reflections used are the ($\underline{4}$ 0 2), ($\underline{6}$ 0 3), and ($\underline{8}$ 0 4) reflections. The two sets of asymmetric reflections used are the ($\underline{12}$ 0 3) and ($\underline{12}$ 0 4) reflections and the ($\underline{6}$ 2 3) and ($\underline{8}$ 2 4) reflections. Note that these two sets of asymmetric reflections fall within two orthogonal slices of reciprocal space. The [100]* and [001]* reciprocal lattice orientations, and the reciprocal lattice angle β* (76°), are also shown to give perspective of the reciprocal unit cell lattice of β-Ga$_2$O$_3$. The shaded region represents the limiting sphere for Cu Kα$_1$ radiation.

5.3 Results and Discussion

The results of the unit cell lattice parameter lengths 'a,' 'b,' 'c,' and angle β (the angle between the 'a' and 'c' axes) from room temperature to 1000 °C are shown in Figure 5.5.2. The

data was fitted to obtain the CTE values along each axis. The CTE values for each lattice parameter are a_{CTE} = 3.77 x 10^{-6} $°C^{-1}$, b_{CTE} = 7.80 x 10^{-6} °C, and c_{CTE} = 6.34 x 10^{-6} $°C^{-1}$, respectively, and the CTE of the angle β is 1.31 x 10^{-4} °/K. All CTE values reported here were found to be anisotropic and linear under the temperature regime between room temperature to 1000 °C. It can be seen from Equation 1 that the temperature dependence of d-spacing will vary among different crystallographic planes due to the low-symmetry of the monoclinic system since the 'a,' 'b,' and 'c' axes all have different temperature dependences. The uncertainty values of the 'a,' 'b,' and 'c' axes and angle β are: ±0.0003 nm, ±0.00003 nm, ±0.0003 nm, and ±0.05° respectively. Note that the smaller 'b' and 'c' axes expanded at about twice the rate of the larger 'a' axis with increasing temperature. The angle β increased slightly (~ 0.1°) with increasing temperature to 1000 °C. The trends observed here are consistent with studies[23,24] performed previously using powder samples but the values are higher (percent difference ranging from 7% to 59%). This trend where single crystalline CTE values are higher than the polycrystalline CTE values is also observed in sapphire.[26] On the other hand, this trend contrasts to what is observed when comparing the CTE of single crystalline and polycrystalline GaN and AlN; the polycrystalline forms of GaN and AlN exhibited higher CTE values than its single crystalline form.[26] 40 x 40 $μm^2$ atomic force microscopy (AFM) scans and Nomarski optical images taken after the CTE measurements showed no surface degradation (0.5 nm root mean square roughness and no surface pits).
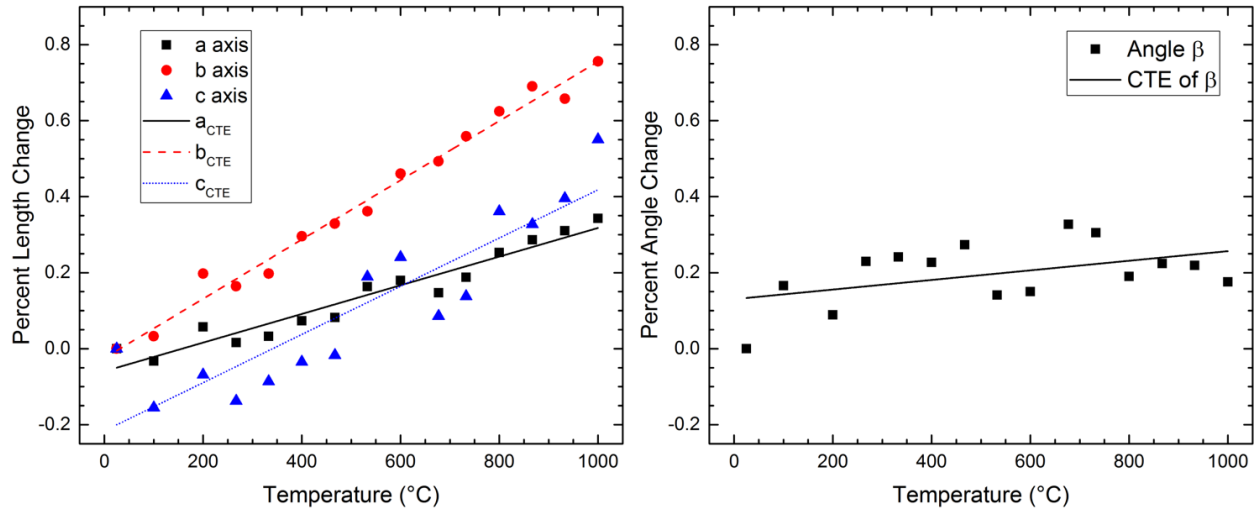
Figure 5.2. The measured lattice parameters a, b, c, and β as a function of temperature. A linear best-fit line is shown for each parameter.

CTE values are useful for predicting thermal strains in heteroepitaxial structures. Several example calculations are reported here in order to demonstrate the expected impact of the differences in CTE along different crystallographic directions when β-Ga_2O_3 is integrated with technologically relevant higher symmetry crystals. Through either wafer bonding or epitaxial means, integration of single crystalline β-Ga_2O_3 to other IV and III-V semiconductor substrates with higher thermal conductivity[36–41] to form heterojunction structures is important for the applications of β-Ga_2O_3 in high-power devices and for GaN-based LEDs. Thermal strains along six evenly distributed in-plane directions were determined in structures that are wafer bonded for ($\underline{2}$01), (010), and (001) oriented single crystalline β-Ga_2O_3 to Si, InP, 3C-SiC, and 6H-SiC substrates at 600 °C and cooled to room temperature, as shown schematically in Figure 5.3 and calculated results summarized in Tables 5.1 through 5.3. The thermal strain, ε, was calculated using the following formula,

$$\varepsilon = \frac{(\alpha_X - \alpha_{Ga_2O_3})\Delta T}{1 + \alpha_X \Delta T}. \qquad\qquad (5.2)$$

where $\alpha_{Ga_2O_3}$ and α_X are the thermal expansion coefficients along a specific crystallographic

direction and ΔT is the temperature difference between processing temperature and room

temperature.
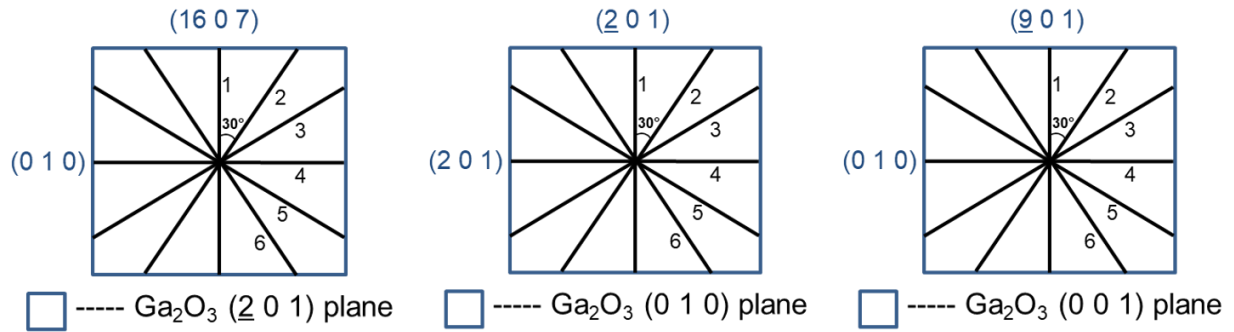
Figure 5.3. The six in-plane directions used in determining in-plane strains for (from left to right)

($\underline{2}$01), (010) and (001) oriented single crystalline β-Ga$_2$O$_3$ to Si, InP, 3C-SiC, and 6H-SiC

substrates. The directions labeled 1 through 6 correspond to directions orthogonal to planes

specified in Tables 5.1 through 5.3.

Plane	($\underline{2}$01) β-Ga$_2$O$_3$		Thermal strain (600 °C – 25 °C)			
		CTE (α) (/°C) along normal direction	(001) Si	(001) InP	(001) 3C-SiC	(0001) 6H-SiC
1	(0 1 0)	7.80×10^{-6}	2.99×10^{-3}	1.84×10^{-3}	1.73×10^{-3}	2.01×10^{-3}
2	(16 10 7)	7.02×10^{-6}	2.54×10^{-3}	1.39×10^{-3}	1.28×10^{-3}	1.56×10^{-3}
3	(16 4 7)	5.80×10^{-6}	1.84×10^{-3}	6.90×10^{-4}	5.75×10^{-4}	8.63×10^{-4}
4	(16 0 7)	4.97×10^{-6}	1.36×10^{-3}	2.13×10^{-4}	9.78×10^{-5}	3.85×10^{-4}
5	(16 $\underline{4}$ 7)	5.80×10^{-6}	1.84×10^{-3}	6.90×10^{-4}	5.75×10^{-4}	8.63×10^{-4}
6	(16 $\underline{10}$ 7)	7.02×10^{-6}	2.54×10^{-3}	1.39×10^{-3}	1.28×10^{-3}	1.56×10^{-3}

Table 5.1. Calculated in-plane strain between ($\underline{2}$01) β-Ga$_2$O$_3$ and various (001) oriented materials processed at 600 °C and cooled to room temperature. The CTE values for Si, InP, 3C-SiC, and 6H-SiC were taken from literature.[27,42–44]

Plane	(010) β-Ga$_2$O$_3$		Thermal strain (600 °C – 25 °C)			
		CTE (α) (/°C) along normal direction	(001) Si	(001) InP	(001) 3C-SiC	(0001) 6H-SiC
1	(2 0 1)	5.11×10^{-6}	1.44×10^{-3}	2.93×10^{-4}	1.78×10^{-4}	4.66×10^{-4}
2	(3 0 10)	6.21×10^{-6}	2.08×10^{-3}	9.26×10^{-4}	8.11×10^{-4}	1.10×10^{-3}
3	($\underline{4}$ 0 5)	6.20×10^{-6}	2.07×10^{-3}	9.20×10^{-4}	8.05×10^{-4}	1.09×10^{-3}
4	($\underline{2}$ 0 1)	5.14×10^{-6}	1.46×10^{-3}	3.11×10^{-4}	1.96×10^{-4}	4.83×10^{-4}
5	(4 0 $\underline{5}$)	6.20×10^{-6}	2.07×10^{-3}	9.20×10^{-4}	8.05×10^{-4}	1.09×10^{-3}
6	($\underline{3}$ 0 $\underline{10}$)	6.21×10^{-6}	2.08×10^{-3}	9.26×10^{-4}	8.11×10^{-4}	1.10×10^{-3}

Table 5.2. Calculated in-plane strain between (010) β-Ga$_2$O$_3$ and various (001) oriented materials processed at 600 °C and cooled to room temperature. The CTE values for Si, InP, 3C-SiC, and 6H-SiC were taken from literature.[27,42–44]

Plane	(001) β-Ga$_2$O$_3$		Thermal strain (600 °C – 25 °C)			
		CTE (α) (/°C) along normal direction	(001) Si	(001) InP	(001) 3C-SiC	(0001) 6H-SiC
1	(0 1 0)	7.80×10^{-6}	2.99×10^{-3}	1.84×10^{-3}	1.73×10^{-3}	2.01×10^{-3}
2	($\underline{9}$ 4 1)	6.84×10^{-6}	2.44×10^{-3}	1.29×10^{-3}	1.17×10^{-3}	1.46×10^{-3}
3	($\underline{45}$ 6 5)	4.67×10^{-6}	1.19×10^{-3}	4.03×10^{-5}	-7.47×10^{-5}	2.13×10^{-4}
4	($\underline{9}$ 0 1)	3.77×10^{-6}	6.73×10^{-4}	-4.77×10^{-4}	-5.92×10^{-4}	-3.04×10^{-4}
5	($\underline{45}$ $\underline{6}$ 5)	4.67×10^{-6}	1.19×10^{-3}	4.03×10^{-5}	-7.47×10^{-5}	2.13×10^{-4}
6	($\underline{9}$ $\underline{4}$ 1)	6.84×10^{-6}	2.44×10^{-3}	1.29×10^{-3}	1.17×10^{-3}	1.46×10^{-3}

Table 5.3. Calculated in-plane strain between (001) β-Ga$_2$O$_3$ and various (001) oriented materials processed at 600 °C and cooled to room temperature. The CTE values for Si, InP, 3C-SiC, and 6H-SiC were taken from literature.[27,42–44]

In Tables 5.1 through 5.3, note that a positive value corresponds to tensile strain while a negative value corresponds to a compressive strain. Using the measured lattice parameters of β-Ga$_2$O$_3$ single crystal wafer, it is predicted that with a bonding temperature of 600 °C each of the ($\underline{2}$01), (010), and (001) oriented single crystal β-Ga$_2$O$_3$ bonded to InP, 3C-SiC, and 6H-SiC have similar tensile thermal strains (except for that along ~ 1/6-1/2 in-plane directions for the (001) β-Ga$_2$O$_3$ bonded structures) within a range from ~ 4.0×10^{-5} to ~ 2.0×10^{-3}, and are ~ 1.5-15 times smaller than that of β-Ga$_2$O$_3$ bonded to Si. Additionally, it is interesting to note that (001) InP, (001) 3C-SiC, and (0001) 6H-SiC bonded to (001) β-Ga$_2$O$_3$ is predicted to result in both tensile and compressive in-plane strain, as shown in Table III. Lastly, (010) oriented β-Ga$_2$O$_3$ bonded to other substrates has more uniform thermal strains along different in-plane directions (less than 5

times difference between the maximum and minimum values) than ($\underline{2}$01) and (001) oriented β-Ga$_2$O$_3$.

GaN and sapphire are also materials of wide-spread current interest. Here, epitaxial structures of (0001) GaN on ($\underline{2}$01) β-Ga$_2$O$_3$ with an in-plane orientation relation of (11$\underline{2}$0) GaN//(010) β-Ga$_2$O$_3$ and MOCVD ($\underline{2}$01) β-Ga$_2$O$_3$ on (0001) sapphire with an in-plane orientation relation of (0 1 0) β-Ga$_2$O$_3$//(1 $\underline{1}$ 0 0) sapphire were studied as well. The schematic in-plane relations are illustrated in Figure 5.4.
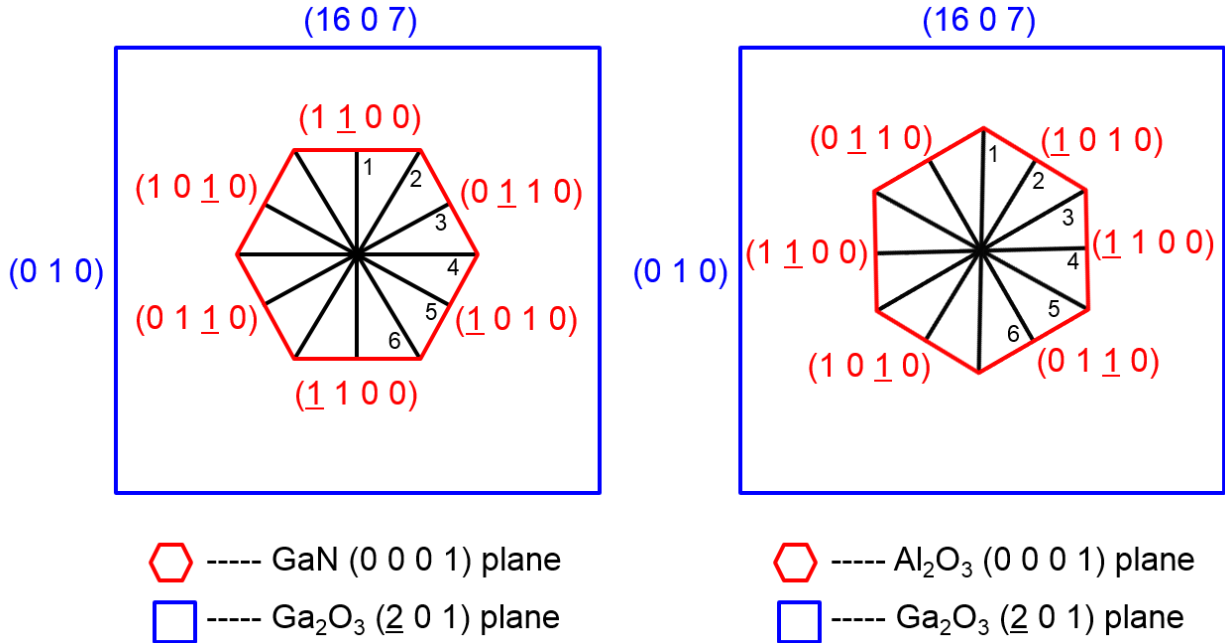
Figure 5.4. The six in-plane directions used in determining in-plane strains between ($\underline{2}$01) oriented single crystalline β-Ga$_2$O$_3$ and GaN (left) and sapphire (right).

For the previously described (0001) GaN//($\underline{2}$01) β-Ga$_2$O$_3$ substrate grown at 1000 °C, tensile thermal strains were determined along 5/6 in-plane directions while compressive strains along the other in-plane directions, which ranged from -5.56 × 10^{-4} to 2.20 × 10^{-3}. It is smaller

than that in GaN grown on sapphire (~ 2.5×10^{-3}) while partially (along ~ 1/3 in-plane directions) smaller than GaN on SiC (~ 7.2×10^{-4}). On the other hand, larger compressive in-plane thermal strain was calculated for the ($\underline{2}$01) β-Ga$_2$O$_3$ deposited on (0001) sapphire substrate at 650 °C with an in-plane orientation relation of (010) β-Ga$_2$O$_3$//(1100) sapphire, ranging from -1.94×10^{-4} to -1.96×10^{-3}. These calculations are summarized in Table 5.4.

| Plane | ($\underline{2}$01) β-Ga$_2$O$_3$ | | (0001) GaN (1000 °C – 25 °C) | | (0001) Sapphire (650 °C – 25 °C) | |
	Miller Indices	CTE (α) (/°C) along normal direction	Miller Indices	In-Plane Strain	Miller Indices	In-Plane Strain
1	(0 1 0)	7.80×10^{-6}	(1 1 $\underline{2}$ 0)	2.20×10^{-3}	(1 $\underline{1}$ 0 0)	-1.94×10^{-4}
2	(16 10 7)	7.02×10^{-6}	(1 0 $\underline{1}$ 0)	1.44×10^{-3}	(1 $\underline{2}$ 1 0)	-6.81×10^{-4}
3	(16 4 7)	5.80×10^{-6}	(2 $\underline{1}$ $\underline{1}$ 0)	2.54×10^{-4}	(0 1 $\underline{1}$ 0)	-1.44×10^{-3}
4	(16 0 7)	4.97×10^{-6}	(1 $\underline{1}$ 0 0)	-5.56×10^{-4}	(1 1 $\underline{2}$ 0)	-1.96×10^{-3}
5	(16 $\underline{4}$ 7)	5.80×10^{-6}	(1 $\underline{2}$ 1 0)	2.54×10^{-4}	(1 0 $\underline{1}$ 0)	-1.44×10^{-3}
6	(16 $\underline{10}$ 7)	7.02×10^{-6}	(0 1 $\underline{1}$ 0)	1.44×10^{-3}	(2 $\underline{1}$ $\underline{1}$ 0)	-6.81×10^{-4}

Table 5.4. Calculated in-plane strain between GaN grown on ($\underline{2}$01) β-Ga$_2$O$_3$ at 1000 °C and ($\underline{2}$01) β-Ga$_2$O$_3$ grown on (0001) sapphire at 650 °C. The CTE values for GaN and sapphire were taken from literature.[42,45–47]

5.4 Conclusion

The lattice parameter coefficients of thermal expansion were determined for β-Ga$_2$O$_3$ using single crystalline β-Ga$_2$O$_3$ wafers. All measurements were done in a controlled N$_2$ environment and subsequent AFM and optical images showed no surface degradation of the β-

Ga$_2$O$_3$ samples after ramping up and down temperatures during the CTE measurements. CTE values for the lattice parameters a, b, c, and β were found to be linear with respect to temperature, which were 3.77 x 10^{-6} °C^{-1}, 7.80 x 10^{-6} °C^{-1}, 6.34 x 10^{-6} °C^{-1}, and 1.31 x 10^{-4} °/K, respectively over a range of room temperature to 1000 °C. Relative magnitudes were the same as those reported in earlier studies on powder samples,[23,24] but the single crystal values turned out to be larger, which is similar to findings for other materials.[26] Prediction calculations of in-plane thermal-induced strains between (010), (001), and ($\underline{2}$01) oriented β-Ga$_2$O$_3$ substrates and various combinations of different materials (Si, InP, 3C-SiC, 6H-SiC, GaN, and sapphire) relevant for both epitaxial and wafer bonding applications involving heterojunction structures were also presented. For the (001) β-Ga$_2$O$_3$ bonded to (001) InP, (001) 3C-SiC, and (0001) 6H-SiC systems and ($\underline{2}$01) β-Ga$_2$O$_3$ bonded to (0001) GaN system, it is predicted that both tensile and compressive in-plane strain will be present if processed at temperatures of 600 °C and 1000 °C and cooled to room temperature, respectively. Interestingly, when comparing (010), (001), and ($\underline{2}$01) β-Ga$_2$O$_3$ orientations, it was found that integrating (010) β-Ga$_2$O$_3$ substrates to these other materials would result in the most uniform thermal strain distribution along different in-plane directions (less than 5 times difference between the maximum and minimum values) compared to bonding with ($\underline{2}$01) and (001) orientated β-Ga$_2$O$_3$.

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Chapter 6: Model System – Silicon Homojunctions Prepared with an Ion-Bombarded Surfaces

6.1 Introduction

While direct wafer-bonding can be used for device fabrication, it can also be used as an approach to characterize and understand the properties of bonded interfaces. Understanding the physics of bonded interfaces would lead to a better control of interfaces to obtain desired properties and ultimately pave the way for integrating unprecedented materials combinations and improve existing device technology. Processing treatments could be efficiently optimized to obtain, for example, improved electronic transport properties under limited thermal budgets. Previous work has demonstrated bonding of III-V materials, to form both homojunctions and heterojunctions, by employing aqueous-sulfur[1,2,3] or elemental sulfur[1,4] passivation methods. However, a high-temperature anneal step is required to form a sufficiently strong bonded interface between the two materials. A minimal temperature bonding procedure is desirable for systems that are restricted by a limited thermal budget and for heterojunction systems where the differences in coefficient of thermal expansion of each material may be too large.

In this work, an ion-bombardment process with varying ion energies in an EVG® ComBond® high vacuum wafer-bonding system[5] is used to remove native oxides on (001) p-type silicon wafers and the treated wafers are subsequently bonded at room temperature. The resulting bonded interface is a few ~nm thick distorted or amorphous region. This technique has been demonstrated to successfully bond materials together,[6,7,8] but there is a lack of fundamental understanding of the nature of interfaces prepared using this method – either the structural or transport characteristics.

73

6.2 Experimental Details

200-mm p-type (001) Si wafers were loaded to an EVG® ComBond® high-vacuum wafer-bonding system[4] and subjected to an argon ion bombardment process with varying ion energies (as multiples of a pre-defined baseline energy E_0) to remove their native oxides. After removing the oxide layer, the wafers were separated into two batches for each energy treatment. One batch was unloaded from the wafer bonding system and the resulting surface layer was analyzed using spectroscopic ellipsometry (SE) and X-ray reflectivity (XRR) to determine the layer thickness and density. 40×40 μm^2 atomic force microscopy (AFM) scans were also employed to assess the changes to the surface roughness. The other batch was transferred in high vacuum to a bonding module where two such surface-treated wafers were directly bonded at room temperature. Aluminum metal contacts were deposited on the resulting bonded structure and current-voltage (I-V) measurements were performed to determine the electrical resistance of the bonded interface. Bonded samples were then subsequently annealed at 450 °C and I-V measurements were repeated. TEM measurements are performed on the bonded samples at the interface using focused ion beam (FIB) on a FEI Titan.

6.3 Results and Discussion

The AFM measurements showed that the root-mean-square roughness value was less than 1 nm across the whole wafer, which is a roughness suitable for direct wafer bonding.[9] The thicknesses and densities of the damaged surfaces of the treated single wafers were determined using SE and XRR. Both methods revealed a previously unreported transition layer at the interface between the bulk (crystalline) silicon and the damaged silicon region. XRR results show that upon increasing the ion energy from $0.5 \cdot E_0$ to E_0, the damaged layer thickness remains

74

constant within experimental error (from 2.2 ± 0.3 nm to 1.8 ± 0.3 nm) while the transition layer

thickness maintains ~1.0 nm in both samples. However, increasing the ion energy from E_0 to

$5 \cdot E_0$ results in an increase in the damage layer thicknesses from 1.8 ± 0.3 nm to 3.5 ± 0.3 nm as

well as a thickness increase of transition layers from ~1.0 ± 0.2 nm to 3.0 ± 0.2 nm. Interestingly,

the damaged silicon layer density is approximately the same across all ion energies used. This

may suggest that under this energy regime, the resulting density of the damaged layer may be ion

mass dependent (i.e. ion species) but ion energy independent. The resulting damaged silicon

region from the Ar ions has a density of 1.85 g/cm^3, which is 20% less than that of crystalline Si

(2.33 g/cm^3) and deposited amorphous silicon (~2.2 g/cm^3), as shown in Figure 6.1.
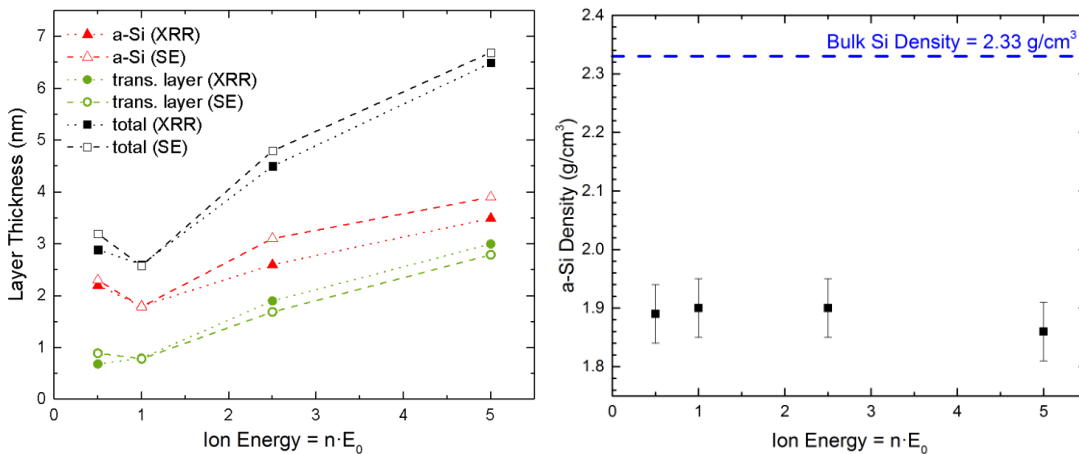
Figure 6.1. Damage layer thickness and layer density versus Ar ion bombardment energy as

determined by XRR and SE measurements. The density of crystalline silicon (c-Si) is 2.33

g/cm^3.

Cross-sectional transmission electron microscopy images of E_0 and $5 \cdot E_0$ bonded samples

show that the damage region between the bonded wafers spans 3.7 nm and 7.5 nm, respectively,

in agreement with the XRR and SE results for single wafer thicknesses. The transition region is

not observed under these TEM imaging conditions. The thicknesses of the damaged region determined by XRR and SE correspond to the triangle data points in Figure 6.6.1. Note that XRR and SE measurements were performed on treated single wafers; thus, the thickness of the damaged layer is half of the total damage thickness observed in TEM. Bonded pairs with thicker damaged regions exhibit lower electrical conductivity across the interface.

I-V measurements show that the bonded samples with amorphous layer thicknesses of 3.7 nm (1.8 ± 0.3 nm from each E_0 wafer) and 7.5 nm (3.5 ± 0.3 nm from each $5 \cdot E_0$ wafer) exhibited interfacial resistances of about 330 $\Omega \cdot cm^2$ and 2220 $\Omega \cdot cm^2$, respectively. TEM images show that annealing at 450 °C for 12 hours removes nearly all of the damage region. The recrystallization bonded interface after annealing is consistent with subsequent I-V measurements that show much smaller, negligible interfacial resistance. In other words, the electrical conductivity across the bonded interface is comparable to the conductivity within the individual bulk crystalline wafers, which indicates the energy barrier across the interface due to the damaged region is mitigated after annealing. The interfacial resistance as a function of interfacial region thickness (and annealing) is shown in Figure 6.2.
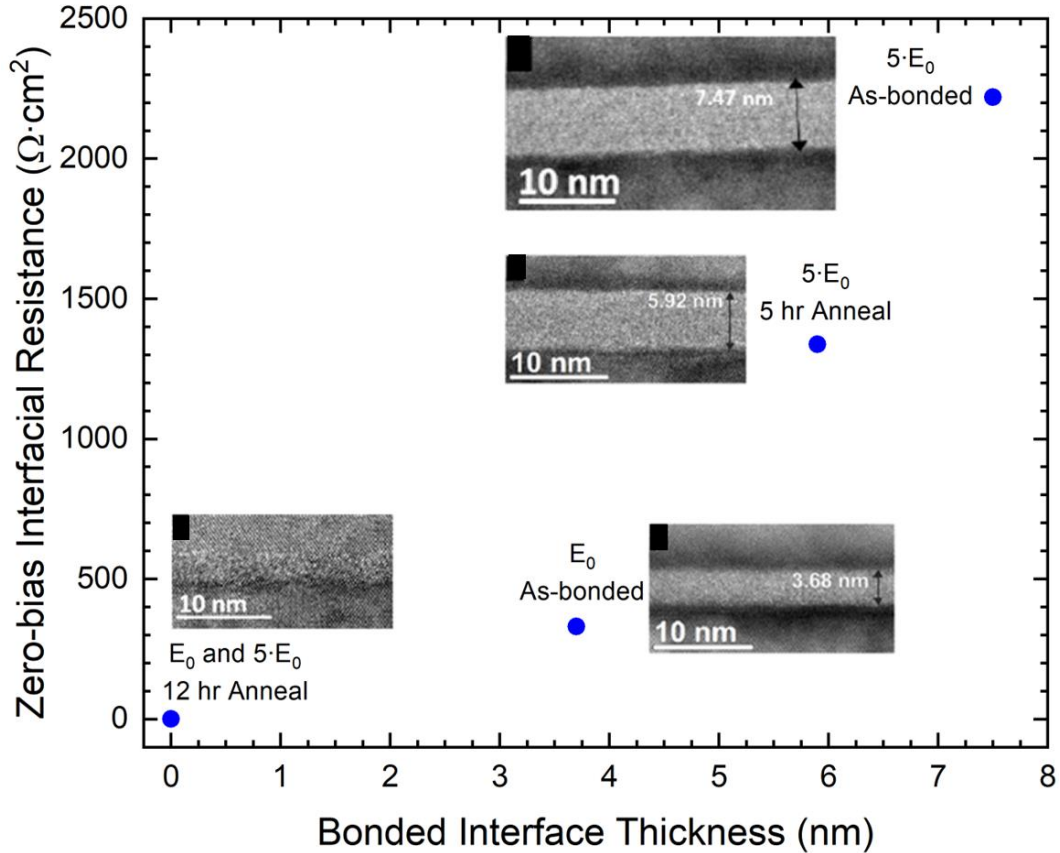
Figure 6.2. The zero-bias interfacial electrical resistance vs bonded interface thickness. Annealing at 450 °C reduces the interfacial region thickness and reduces the resistance as shown for the $5 \cdot E_0$ sample.

6.4 Conclusion

SE and XRR results of the treated single wafers were found to be consistent with each other and concluded that the resulting damaged layer had an energy dependent thickness and an ion-energy independent density. The density was about 80% of the density of single crystalline silicon. The thickness values determined by SE and XRR are also consistent with TEM images. In both the E_0 and $5 \cdot E_0$ samples, the damaged layer was effectively removed after 12 hours of annealing at 450 °C, as shown by TEM images I-V measurements. The electrical resistance of

the bonded interface for the thicker bonded interface (higher ion energy) was 2220 $\Omega \cdot cm^2$, which was reduced to a negligible resistance after annealing. The high electrical resistances across this amorphous region, compared to the bulk Si, is attributed to the fact that electrical transport across these bonded structures pass through three interfaces at the thin ~nm interfacial amorphous bonded region. The results presented here are part of a larger effort towards fundamentally understanding bonded interfaces prepared using this ion bombardment process.

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Chapter 7: Model System – Role of Twist Misorientation on the Electrical Transport Across InP Homojunctions

7.1 Introduction

A fundamental understanding of the impact of different factors on the electrical quality of the bonded interface would give rise to an understanding of how to engineer interfaces to produce desirable emergent properties. Previous work demonstrated the importance of surface passivation treatments prior to bonding, which required a good understanding of the surface chemistry of III-V materials.[1-3] In this work, the effect of rotational misorientation (twist) on the electronic properties across the bonded interface was studied by fabricating InP homojunctions – a fundamental model system using a well-understood material. This work in addition to previous work on the effect of tilt misorientation[6] provides insight as to which crystallographic factors most strongly impact bonding and electronic transport across the interface. Furthermore, since the bonded interface is essentially a grain boundary, information obtained in wafer bonding experiments can also apply to polycrystalline systems where grain boundaries play a significant role in overall device performance. In fact, wafer bonding enables us to have full control over the type of interface, and ultimately create a specific grain boundary that forms between two wafers. Wafer bonding leads to engineering of grain boundaries to fully understand the physics of grain boundaries and how to obtain desired interfacial properties. While the focus is on electronic transport across interfaces, the insight gained here is speculated to be useful for other important characteristics, such as phonon transport.

7.2 Experimental Details

To study the effect of rotation, on-axis (001) $\pm 0.1°$ n-type InP wafers with twist angles ranging from 0° to 90° in 15° increments were bonded. Prior to bonding, the wafers were first cleaved into quarters and submerged in an NH_4OH solution to remove the native surface oxide and then submerged in a 20% aqueous $(NH_4)_2S$ solution for 5 minutes.[1-3,6,8] After drying the wafers with N_2, the wafers were brought face-to-face and very low pressure (kPa) was applied manually at room temperature and in ambient air pressure. The relative rotational misalignment was induced by rotating the top wafer prior to applying pressure. The bonded wafers were then annealed at 400 °C for 2 hours to strengthen the bonded interface followed by a 600 °C anneal for 2 minutes. Metal Ohmic contacts were fabricated on each semiconductor surface and samples were diced into ~2 x 2 mm^2 squares. Current-voltage profiles were measured to extract interfacial resistance of the bonded interface.

7.3 Results and Discussion

Rotational misalignment impacts the electronic properties of the bonded interface follows a cyclic pattern. For the (001) InP wafers, as shown in Figure 7.1, the maximum interfacial resistance corresponded to a 45° twist of $(7.8 \pm 0.2) \times 10^{-3}$ $\Omega \cdot cm^2$ while the minimal resistance values corresponded to 0° and 90° with values of $(6.0 \pm 0.2) \times 10^{-3}$ $\Omega \cdot cm^2$ and $(6.2 \pm 0.4) \times 10^{-3}$ $\Omega \cdot cm^2$, respectively.
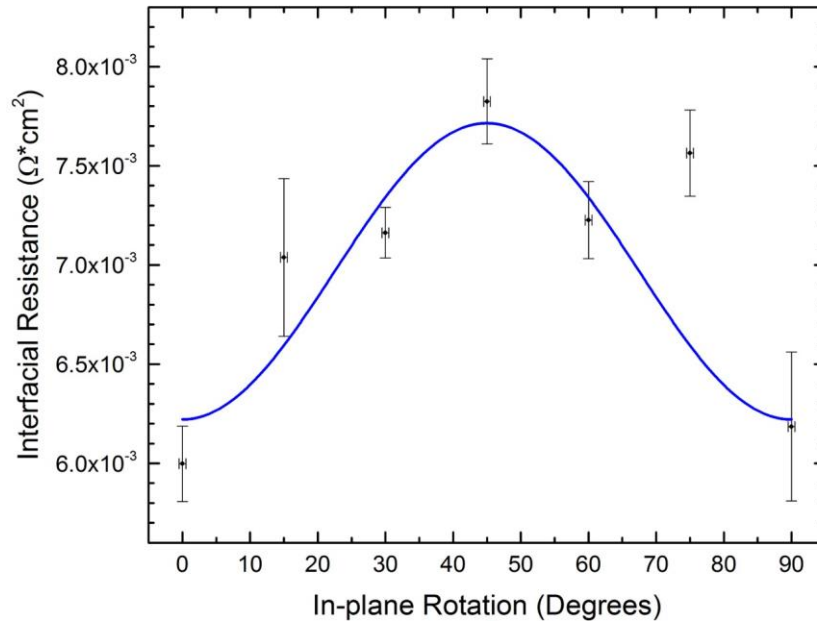
Figure 7.1. Interfacial resistance as a function of in-plane rotational misalignment (twist). The error bars correspond to the standard deviation of 10 samples for each bonded pair.

The vertical error bars for the interfacial resistance correspond to the standard deviation of resistance values for 10 samples for each rotation-angle group. The horizontal error bars for the in-plane rotation angle correspond to the error in the induced rotational misalignment, which was within ± 1°. The 75° rotation group appears to be an anomaly in the general trend. However, this is attributed to a poorer quality bonded interface and/or metal-semiconductor interface compared to the other angle groups.

There is a discrepancy in literature on the effect of rotational misalignment. Kish et al.,[9] claimed rotationally misaligning (001) III-V wafers by 20° and 90° result in the same decrease in electrical conductivity across the bonded interface compared to their 0° bonded wafers. Contrary to this study, Okuno et al.,[10,11] found that 0° and 90° bonded samples result in identical electrical performance. The results presented here are consistent with Okuno et al.,[10,11] in that the values

82

are approximately the same at the end points and with Kish et al.,[9] for low angles up to 20° in that there is an increase in the interfacial resistance for small angular twist misorientations. It is concluded that the effect of rotational misalignment on the electrical conduction across bonded interfaces follows a cyclical pattern and its periodic effect on interfacial conductivity depends on the lattice symmetry of the wafer's surface orientation, which has implications for bonding wafers with different surface symmetries. For GaAs and InP (001) wafers, 0° and 90° bonded samples are expected to exhibit similar, if not equal, resistances since the (001) plane has a four-fold symmetry. This can be visualized by looking at ball-and-stick models of the monolayers closest to the bonded interface from each wafer, as shown in Figure 7.2.

0°   45°   90°
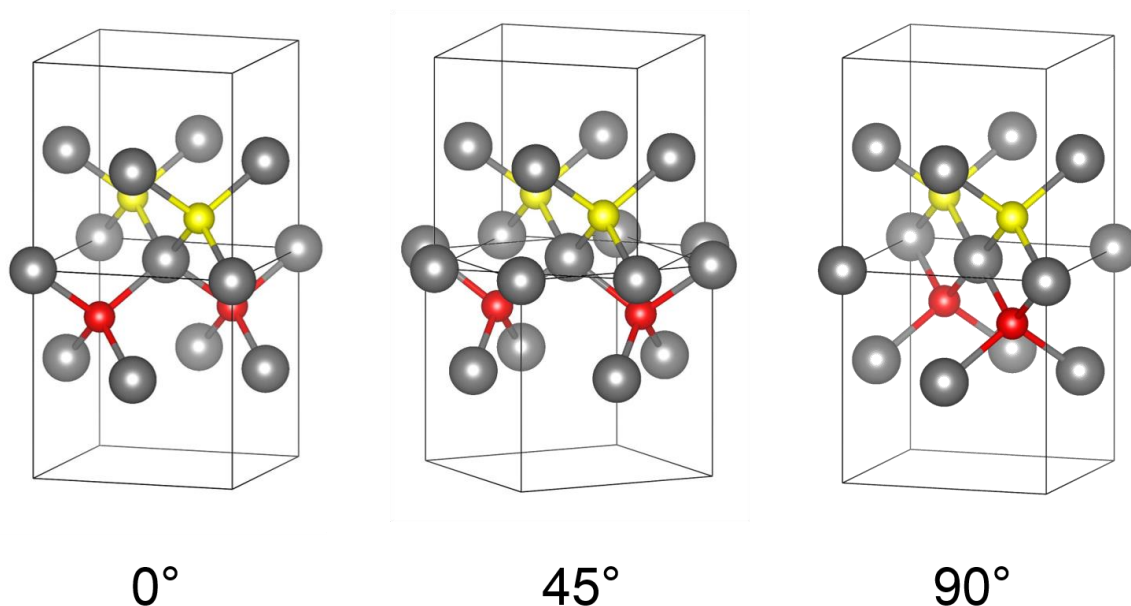
Figure 7.2. Ball-and-stick models of rotational misaligned bonded InP wafers generated using a 3D visualization program.[12] The monolayers adjacent to the bonded interface from each wafer are shown with the cubic unit cell wireframe to guide the eye. The larger atoms represent In atoms while the smaller atoms represent the P atoms.

0° rotational misorientation corresponds to the least amount of misorientation in the sense that across the interface, the repeating pattern of the InP unit cell is uninterrupted between the two bonded wafers. Crystallographically the two bonded wafers look like one continuous single crystal wafer. 90° is similar to 0°, but the unit cells across the bonded interface is not exactly a continuation of each other, but rather mirror images similar to a twin boundary. In the 90° case, one set of atoms are properly lined up across the interface while the other set of atoms are mirror images of each other across the interface. For example, as shown in Figure 7.2, this 90° case shows that the indium atoms do not disrupt the unit cell pattern across the interface while the phosphorous atoms do. The phosphorous atoms in the bottom unit cell are in positions that are mirror images of the top unit cell. It is proposed that this misorientation resulting in a mirror image provides only a small perturbation to the electronic transport across the interface. Lastly, the 45° configuration corresponds to the maximal amount of rotation misorientation since none of the In and P atoms can align from the bottom unit cell to the top unit cell without disrupting the unit cell pattern across the interface. This is the orientation that reduces the symmetry across the interface by the greatest amount compared to other angles. The greater the amount of misorientation across the interface (not necessarily the largest rotational angle), the larger the barrier to electronic transport is. This symmetry effect is hypothesized to apply for other crystallographic orientations and bonding materials with different crystallographic systems. Previous work showed that higher relative tilt across the interface leads to larger barrier heights.[6] For the GaAs|GaAs system, the barrier height increased from 0.56 eV to 1.00 eV when increasing the tilt from 0° to 8°, respectively. For the InP|InP system, the barrier height ranged from 0.26 eV to 0.31 eV. Interestingly, the GaAs|InP heterojunction system exhibited barrier

heights more similar to the InP/InP system than the GaAs|GaAs system, which ranged from 0.31 eV to 0.39 eV when increasing the tilt from 0° to 8°, as shown in Figure 7.3.
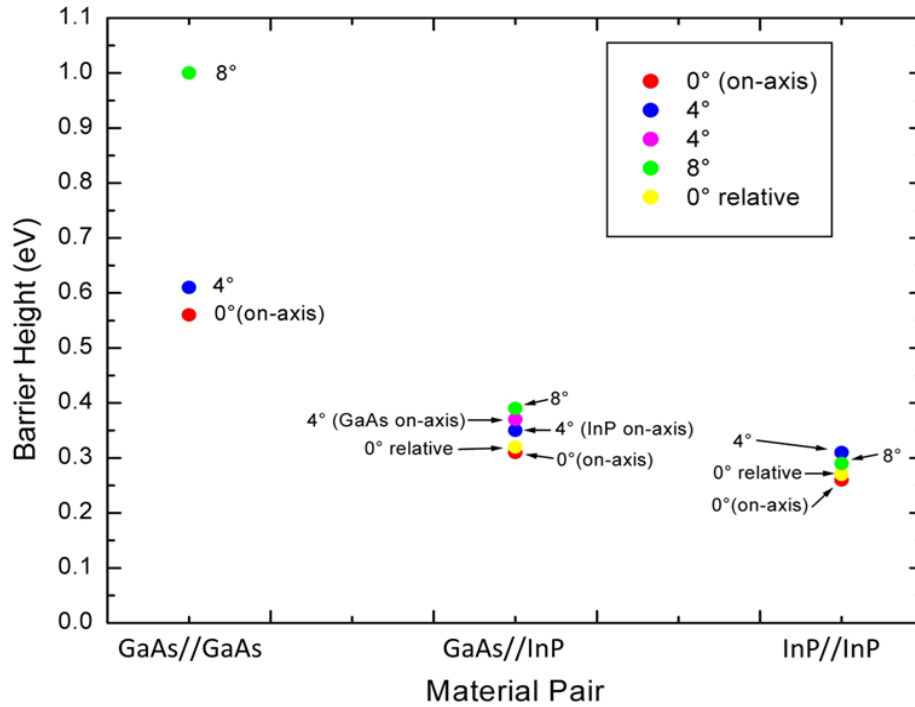
Figure 7.3. Experimentally determined barrier heights from a previous study[6] on the effect of tilt misorientation on GaAs and InP homojunction and heterojunction structures.

These results suggest that materials choice plays a key role in controlling the bonded interface's properties while lattice parameter mismatch appears to play an insignificant role since for the GaAs|InP system the mismatch is ~3.5%. The improved electrical performance of the GaAs|InP system over the GaAs|GaAs is attributed to indium atomic diffusion along the bonded interface as reported by Lo et al.,[13] and Liau et al.[14,15] Thus, based on our findings, indium diffusion is a likely contributing factor for improving electronic transport across the bonded interface. In addition, lattice mismatch does not have a strong impact on the electrical interface

resistance. For example, (001) GaAs bonded to (001) InP without any in-plane misalignment shows a lower interface resistance than GaAs|GaAs bonding. This improved performance in the GaAs|InP structure is consistent with results presented in a previous simulation study on various III-V materials systems[16] and is also consistent with the results of the high-efficiency multijunction III-V solar cells presented by F. Dimroth et al.,[4] and P. T. Chiu et al.[5]

7.4 Conclusion

The effect of tilt and twist misorientation on the electrical properties of bonded III-V wafers was studied by wafer bonding GaAs and InP. Increasing tilt leads to higher electronic transport barrier heights, which can be mitigated by the appropriate materials choice combinations (i.e. changing from a GaAs|GaAs homojunction to a GaAs|InP heterojunction). Twist can also increase the barrier to electrical conduction up to a certain point since it was observed to exhibit a cyclical pattern. This suggests that the symmetry of the wafer's crystallographic orientation plays a role in determining the electronic transport properties across the interface. Electrical characterization of the interface enables us to understand the key factors that influence the properties of a bonded interface. In addition to previous work on surface passivation of III-V's, it is concluded that surface passivation, materials choice, and relative misorientation of the bonded materials are the quintessential determining factors that control the electrical performance of the bonded structure. The findings presented here suggest that misorientation plays an important role in the transport properties of interfaces. This is especially important for heterogenous integration of materials that may not have the same crystal structure where minimizing mismatch between orientations corresponds to minimizing tilt and twist misorientation.

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Chapter 8: Exfoliated and Transferred β-Ga₂O₃ on 4H-SiC

8.1 Introduction

Low thermal conductivity poses an issue for β-Ga₂O₃ power devices due to inefficient heat dissipation. It has been documented that poor heat management in either lateral or vertical β-Ga₂O₃ devices degrades device performance[1] and can even cause permanent device failure.[2,3] It is evident that β-Ga₂O₃ alone cannot manage heat generated during device performance. While heat-related issues are recognized in the current literature, the understanding of thermal management for β-Ga₂O₃ is still in its infancy and much less studied than the electrical characteristics of devices.

Theoretical studies for thermal management of β-Ga₂O₃ devices have investigated various cooling methods: bottom-side cooling (substrate side), top-side cooling (device side), and double-side cooling.[4,5,6] It was found that especially for vertical devices (where reducing the β-Ga₂O₃ thickness is not an option), either top-side or double-side cooling are expected to be most effective for thermal management. While there are some experimental reports studying possible thermal management solutions,[7,8,9,10,11,12] a fundamental understanding of thermal transport across interfaces is still lacking. One important interface in various lateral and vertical device structures is the semiconductor | dielectric interface. These technologically relevant interfaces are utilized for example in metal oxide semiconductor field effect transistors (MOSFETs) and metal oxide semiconductor capacitors (MOSCAPs). One top-side cooling approach could be employed through these semiconductor | dielectric interfaces. The focus of this work is the thermal transport across wafer bonded ($\underline{2}$01) β-Ga₂O₃ | dielectric | (0001) 4H-SiC interfaces, which could be applied to either bottom-side or top-side cooling approaches. For bottom-side cooling, a thin β-Ga₂O₃ layer would be bonded to a high thermal conductivity substrate such as 4H-SiC using an

intermediate dielectric layer. Top-side cooling would instead require transferring a thin layer of high thermal conductive material on the exposed dielectric material between metal contacts.

The dielectric layer in this current study used to assist the bonding between β-Ga_2O_3 and 4H-SiC is a ~30 nm Al_2O_3 layer, which is comparable to thicknesses of Al_2O_3 used in various β-Ga_2O_3 MOSFETs,[13,14,15,16] MOS diodes,[17,18] and MOSCAPs[19,20,21,22] that range from ~10 nm to ~60 nm. A continuation of our previous work,[23] this current study provides further structural analysis of the heterointerfaces for this β-Ga_2O_3 | Al_2O_3 | 4H-SiC system. Here, a 130-nm thick exfoliated ($\underline{2}01$) β-Ga_2O_3 layer was wafer bonded to a (0001) 4H-SiC substrate using a thin ~30 nm Al_2O_3 interlayer at the bonded interface. The β-Ga_2O_3 and 4H-SiC are aligned in-plane such that [010] β-Ga_2O_3 ‖ [11$\underline{2}0$] 4H-SiC. With this alignment of the zone axes, the β-Ga_2O_3 and 4H-SiC have the least amount of twist misalignment (i.e., the least amount of lattice mismatch). Theoretical modeling suggests twist misalignment across interfaces increases the thermal boundary resistance.[24] Previous work on wafer bonded InP | InP demonstrated twist misalignment hinders electronic transport and increases the interfacial electrical resistance.[25] The same trend was demonstrated for electronic transport across wafer bonded GaAs and InP with intentionally induced tilt misalignment.[25,26,27] In general, misalignment across interfaces impedes the transport of phonons and electrons. While the structure fabricated in this study closely mimics a lateral device structure for bottom-side cooling, the characteristics of the interfaces themselves are expected to be applicable in the vertical device setting for top-side cooling. In this scenario, a thin layer of 4H-SiC would be exfoliated and transferred[28,29,30,31,32] on a β-Ga_2O_3 substrate with a dielectric surface layer.

8.2 Experimental Details

2-inch ($\overline{2}$01) β-Ga$_2$O$_3$ substrates grown using the edge-defined film-fed growth method were first implanted with H$^+$ ions at 35 keV with a dose of 1×10^{17} cm^{-2} at room temperature. Then, 30 nm of Al$_2$O$_3$ was then deposited on the implanted β-Ga$_2$O$_3$ substrate surfaces via plasma-enhanced atomic layer deposition at 200 °C. While our previous work demonstrated reducing the Al$_2$O$_3$ layer from 30 nm to 10 nm increases the thermal boundary conductance,[23] 30 nm is used in this current work as a middle-ground system between the thinnest and thickest dielectric layer currently used in devices. The processed β-Ga$_2$O$_3$ substrates were subjected to an ion sputtering treatment consisting of Ar and Si ions to create dangling bonds under vacuum (5 × 10^{-6} Pa); 4-inch (0001) 4H-SiC substrates were also subjected to the same ion sputtering surface treatment in the same bonding chamber. The two surface treated materials were then brought face-to-face and bonded at room temperature.[23] The resulting bonded interface was a 2.9 nm thick amorphous region between the Al$_2$O$_3$ and 4H-SiC. The thin amorphous bonded interface is a common occurrence when bonding covalent materials using this ion bombardment surface treatment.[33,34,35,36,37,38] The bonded structure was then annealed at 450 °C for 6 hours to induce H$_2$ bubble growth at the projected within the β-Ga$_2$O$_3$ substrate and exfoliated a ~400 nm thick layer. The bonded β-Ga$_2$O$_3$ layer was then polished to remove the surface roughness from the exfoliation resulting in a final thickness of ~130 nm bonded to 4H-SiC with an Al$_2$O$_3$ interlayer at the bonded interface.[23] A post-bond annealing was done at 800 °C for 1 hour in ambient atmosphere, using a 5 °C/min ramp up rate on an Instec high temperature stage in an X-ray diffractometer. The peak shift of the (0008) 4H-SiC reflection was used to verify the bonded sample reached 800 °C by using the known coefficient of thermal expansion for 4H-SiC.[39]

The thermal conductivity of the exfoliated β-Ga$_2$O$_3$ and thermal boundary conductance (TBC) before and after the post-bond anneal were measured using time-domain

thermoreflectance (TDTR).[40,41] The pump radius used was 10.1 μm in areal diameter, while the probe radius was 5.8 μm in areal diameter. A low modulation frequency of 2.2 MHz was employed to extract the TBC of the bonded interface buried beneath the exfoliated β-Ga$_2$O$_3$ layer.[23] Structural characterization was performed with a high-resolution Bruker-JV D1 X-ray diffractometer using triple-axis diffraction (acceptance angle of ~10"). The incident X-ray beam is conditioned by a Göbel mirror[42] and a (220) channel-cut silicon crystal, which produces a highly collimated monochromatic beam of Cu Kα$_1$ radiation. The scattered beam optics is a 4-bounce (220) channel-cut silicon analyzer crystal. Triple-axis symmetric ω:2θ and ω scans were measured to measure strain and lattice tilt, respectively. An FEI Nova 600 DualBeam focused ion beam system was used to prepare transmission electron microscopy samples. An FEI TITAN S/TEM operating at a 300 keV accelerating voltage was then employed to generate scanning transmission electron microscopy (STEM) images aligned to the [010] β-Ga$_2$O$_3$ and [11$\underline{2}$0] 4H-SiC zone axes.

8.3 Results and Discussion

The cross-sectional bright-field scanning transmission electron microscopy (STEM) image of the bonded β-Ga$_2$O$_3$ | Al$_2$O$_3$ | 4H-SiC structure is shown in Figure 8.8.1. The Al$_2$O$_3$ intermediate layer is ~30 nm thick and the exfoliated β-Ga$_2$O$_3$ thin film is ~130 nm thick. Note that the bonded interface is between the Al$_2$O$_3$ interlayer and 4H-SiC substrate. Magnified high resolution TEM images of the bonded interface for the as-bonded state and after annealing 800 °C for 1 hour are shown in Figure 8.2(a) and Figure 8.2(b), respectively. The fast Fourier transforms (FFT) in Figure 8.2(c) of the as-bonded state shows the ~2.9 nm layer at the bonded interface is amorphous SiC. After annealing, the FFT in Figure 8.2(d) shows reciprocal lattice

91

points that indicates the amorphous SiC recrystallized during the anneal. For a semi-quantitative comparison, the FFT for bulk 4H-SiC is shown in Figure 8.2(e), and the integrated line extractions taken along the horizontal (Q_X axis) for all the FFTs are plotted in Figure 8.2(f). The FFT for bulk 4H-SiC is measured within the substrate away from the bonded interface where the 4H-SiC lattice is undistorted. For the as-bonded state, the SiC is amorphous and correspondingly shows the greatest amount of diffuse scatter intensity between $\pm$ 6 nm^{-1} along Q_X. After annealing, the diffuse scatter intensity reduces towards the same intensity of bulk 4H-SiC, and the reciprocal lattice points corresponding to the (10$\underline{1}$0) 4H-SiC planes emerged.

During the anneal, the alumina interlayer also recrystallized simultaneously with the 4H-SiC at the bonded interface. Initially, the alumina layer is amorphous, as shown in the cross-sectional TEM image and the lack of reciprocal lattice points in its respective FFT shown in Figure 8.3(a). After annealing at 800 °C for 1 hour, approximately half of the alumina recrystallized starting at the β-Ga$_2$O$_3$ interface, while the other half of the interlayer adjacent to the 4H-SiC interface remained amorphous as shown in Figure 8.3(b). The crystallized Al$_2$O$_3$ layer is (0001) textured, with some regions having an in-plane relationship [010] β-Ga$_2$O$_3$ ∥ [11$\underline{2}$0] Al$_2$O$_3$ shown in Figure 8.3(b), while other regions having an in-plane relationship [010] β-Ga$_2$O$_3$ ∥ [10$\underline{1}$0] Al$_2$O$_3$ (not shown).

The recrystallization of the 4H-SiC layers at the bonded interface and Al$_2$O$_3$ layer both increase the thermal boundary conductance (TBC) by ~20% compared to the as-bonded state. The contribution to the conductance from the crystallized Al$_2$O$_3$ is consistent with work that showed the thermal conductivity of crystalline Al$_2$O$_3$ is higher than its amorphous counterpart.[43] The as-bonded state exhibited a TBC of 66 MW/m^2·K while after annealing at 800 °C for 1 hour the TBC increased to 77 MW/m^2·K. The TBC reported here combines the contributions from: (1)

β-Ga$_2$O$_3$ | Al$_2$O$_3$ interface, (2) Al$_2$O$_3$ interlayer, and (3) Al$_2$O$_3$| 4H-SiC interface. Work by Xu et al.,[44] demonstrated annealing at even higher temperatures of 900 °C further increases the TBC of this β-Ga$_2$O$_3$ | Al$_2$O$_3$ | 4H-SiC structure to ~130 MW/ m^2·K. However, annealing at lower temperatures may be an important consideration for systems with limited thermal budgets. Song et al.,[45] points out that a thermal boundary conductance > 17 MW/ m^2·K would be sufficient to reasonably manage the heat generated from a β-Ga$_2$O$_3$ transistor operating at a 10 W/mm power density that would exceed 1500 °C without heat dissipation strategies. Hence, even the TBC of the as-bonded state would satisfy this requirement. Annealing may be employed to further improve the TBC to comply with heat dissipation requirements for devices operating at even higher power densities. Furthermore, the TBC values achieved here are superior to bonded structures with relatively weak van der Waals forces, e.g., β-Ga$_2$O$_3$ on diamond interfaces fabricated using the mechanical tape exfoliation and transfer technique (TBC ranges from ~8 to ~17 MW/m^2·K).[10,46] Polycrystalline β-Ga$_2$O$_3$ on diamond has already been demonstrated to exhibit high TBC values ranging from ~140 to ~180 MW/m^2·K.[11] Direct wafer bonding β-Ga$_2$O$_3$ on diamond is speculated to exhibit at least comparable TBC values as the polycrystalline β-Ga$_2$O$_3$ films on diamond.
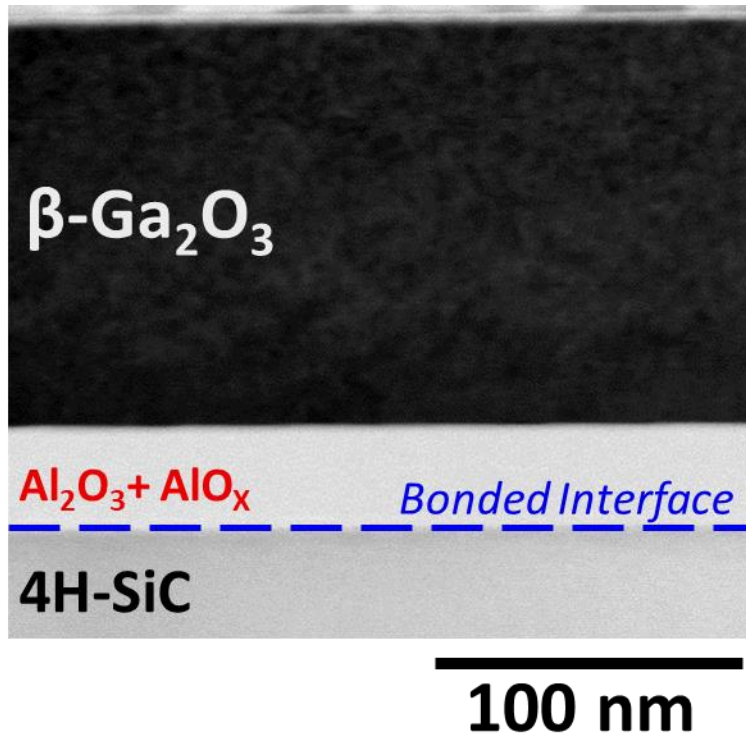
Figure 8.1. Cross-sectional bright-field STEM image of the wafer bonded β-Ga$_2$O$_3$| Al$_2$O$_3$ | 4H-SiC. The bonded interface is between the Al$_2$O$_3$ layer and 4H-SiC substrate.
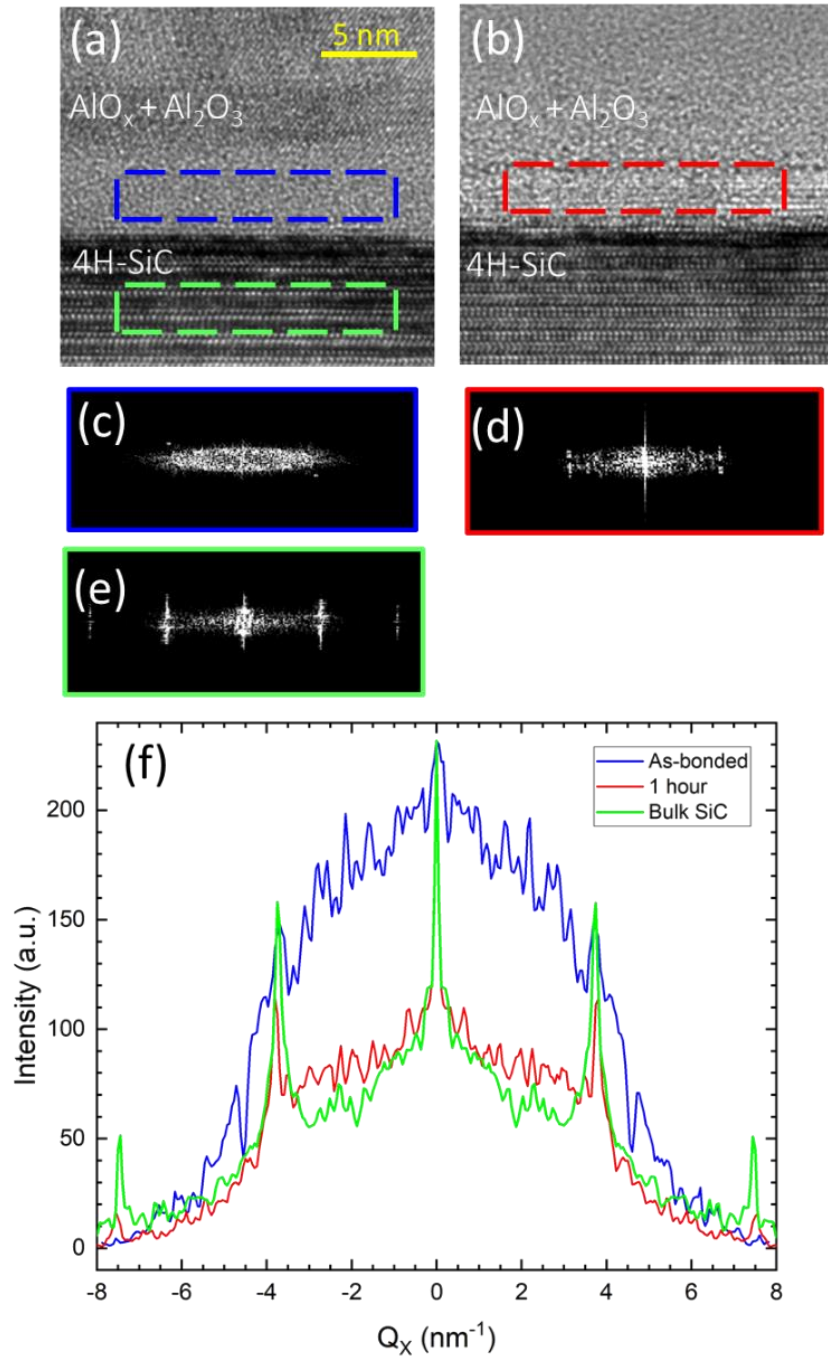
Figure 8.2. Cross-sectional high-resolution transmission electron microscopy images of the wafer

bonded ($\underline{2}$01) β-Ga_2O_3|(0001) 4H-SiC (a) as-bonded and (b) 1 hour anneal at 800 °C. The FFTs

for each of the boxed areas are shown for: (c) amorphous SiC, (d) recrystallized 4H-SiC, and (e)

bulk 4H-SiC beneath the bonded interface. The extracted integrated line scans of the fast Fourier

transform images are shown in (f). The satellite peaks in (f) correspond to the (10$\underline{1}$0) 4H-SiC

interplanar spacing.
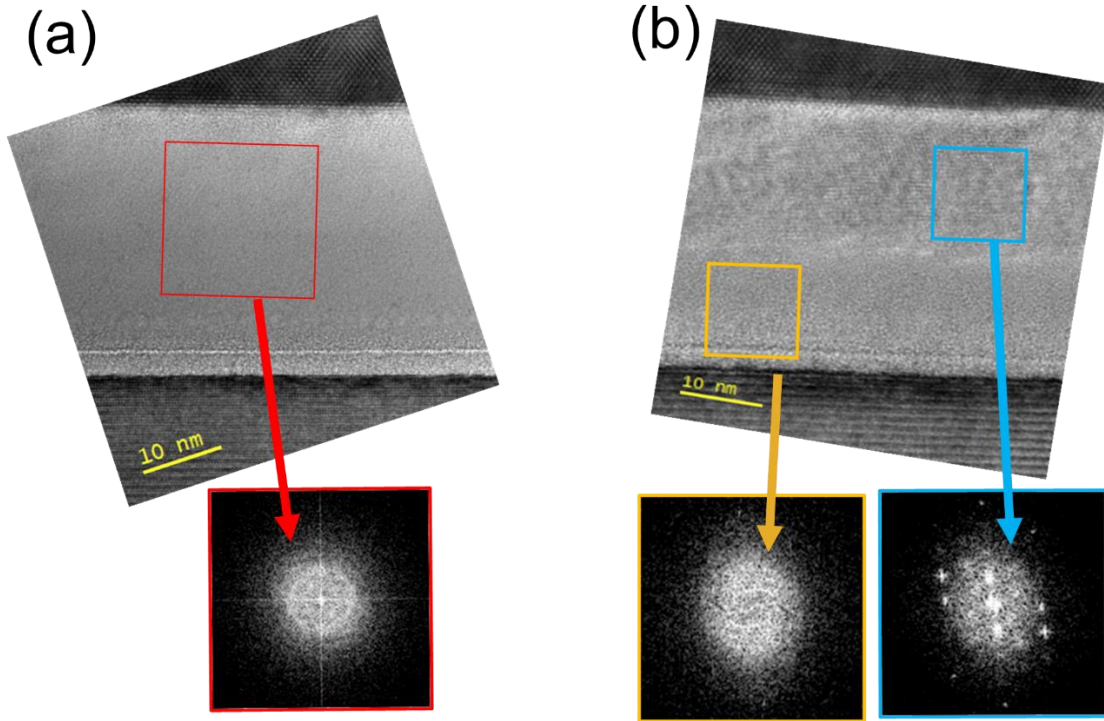
Figure 8.3. Cross-sectional high-resolution transmission electron microscopy images of the alumina interlayer (a) as-bonded and (b) 1 hour anneal at 800 °C. Recrystallization of the Al_2O_3 appears to initiate at the ($\underline{2}$01) β-Ga_2O_3 interface and the crystallization front propagates towards the 4H-SiC.

Triple-axis X-ray diffraction symmetric ($\underline{2}$01) β-Ga_2O_3 ω:2θ scans are shown in Figure 8.4(a). The (0004) 4H-SiC reflection corresponds to 0" along the ω:2θ scanning axis for both as-bonded and post-anneal scans. After annealing, the ($\underline{2}$01) β-Ga_2O_3 peak shifts by ~100" towards higher angles. For the as-bonded state (i.e., post-exfoliation), the peak being at a lower ω:2θ angle prior to annealing indicates that the film is in a tensile strain state. Even after the exfoliation, there is likely residual hydrogen dissolved and/or intercalated in the β-Ga_2O_3 film.

This strain from residual hydrogen is removed after annealing at 800 °C for 1 hour. The thermal conductivity of the β-Ga$_2$O$_3$ film increased after the anneal, from 2.9 W/m·K to 6.0 W/m·K. The reduction in thermal conductivity due to strain is due to strain-field induced phonon-defect scattering discussed in our previous work.[23] The triple-axis symmetric ($\underline{2}$01) β-Ga$_2$O$_3$ rocking curves are shown in Figure 8.4(b), which shows the FWHM decreases from 120" as-bonded to 70" after the anneal. The reduction in lattice mosacity (i.e., reduction in peak width) and corresponding improvement in thermal conductivity is speculated to be due to the dissolution of implant-related extended defects after annealing.[47]
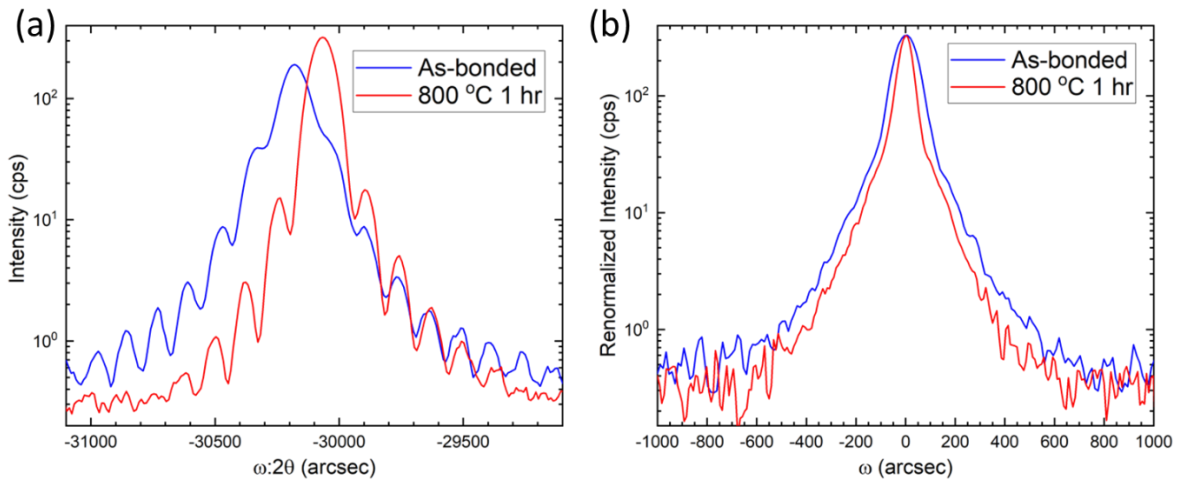
Figure 8.4. Triple-axis X-ray diffraction (a) ω:2θ and (b) ω of the symmetric ($\underline{2}$01) β-Ga$_2$O$_3$ layer. After annealing for 1 hr, residual strain from the ion implantation was reduced and the rocking curve FWHM decreased from 120" to 70".

8.4 Conclusion

Successful exfoliation and bonding of ($\underline{2}$01) β-Ga$_2$O$_3$ on (0001) 4H-SiC using a 30 nm alumina interlayer was demonstrated. The thermal transport and structural characteristics of the

amorphous 4H-SiC | Al_2O_3 bonded interface, Al_2O_3 interlayer, and β-Ga_2O_3 film were assessed.

The amorphous bonded interface was shown to recrystallize along with the Al_2O_3 interlayer,

which improved the TBC by ~20% to 77 MW/m^2·K. Residual strain in β-Ga_2O_3 film from the ion

implantation process was simultaneously removed and improved the thermal conductivity of the

film from 2.9 W/m·K to 6.0 W/m·K. While the surface activated bonding technique is useful for

bonding dissimilar materials, the amorphous or lattice-damaged interfaces created by this process

can be engineered (e.g., annealing) to alter interfacial transport properties.

8.5 References

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Chapter 9: Origins of Macro-Surface Features on Thick GaN Homoepitaxy for kV Device Layers

9.1 Introduction

To fully utilize GaN in the high-power device technology space, thick drift layers on the order of tens of microns are needed to fabricate devices operating in the ~kV regime.[1,2,3,4,5,6,7] Maintaining smooth surfaces during the growth of thick GaN layers will be crucial for optimizing vertical GaN devices because it has been demonstrated that surfaces free of surface morphology (e.g. hillocks and macro-steps/macro-terraces) are required to achieve consistent and well-performing devices.[8] Various surface features have been observed during GaN homoepitaxial growth, including hillocks and macro-steps and macro-terraces.[9,10,11,12] The formation of macro-steps and macro-terraces is the focus of this current study.

Work by Fujikura et al.,[11] varied growth parameters and substrate miscut angle to study the surface features that gave rise to optically hazy GaN surfaces. The hazy morphology corresponded to wavy surface features of meandering bunched steps consisting of macro-steps (m-plane facets; lengths ranged from 10 to 30 μm) and macro-terraces (a-plane facets; and lengths ranged from 30 to 100 μm). These features covered the entire surface viewed within 940 ×700 μm^2 areas. It was concluded that the growth instabilities associated with step meandering that led to macro-step and macro-terraces can be suppressed by growing on vicinal GaN substrates miscut ≥ 0.4° at relatively high growth temperatures or low V/III ratios. However, these macro-steps and macro-terraces that give rise to optically hazy surfaces were only studied after the entire surface of the wafers were covered with these features. The initial growth stages of these macro-steps and macro-terraces have yet to be documented and studied.

In this current study dot-core GaN substrates were employed as a defect-engineering sample to study the origins and evolution of macro-step and macro-terrace formation. Dot-core GaN substrates are prepared by growing GaN on a patterned substrate using hydride vapor phase epitaxy (HVPE). The pattern consists of an array of cores spaced ~0.8 mm apart to concentrate defects at the cores (~10^8 cm^{-2} dislocation density) in order to produce low defect density GaN between the array of cores ($< 10^4$ cm^{-2}).[13,14] The results from studying thick GaN homoepitaxial growth on dot-core substrates are used to leverage our understanding of the macro-features that form during homoepitaxial growth on other types of GaN substrates.

9.2 Experimental Details

Homoepitaxial growth via metal organic chemical vapor deposition (MOCVD) was done on two-inch diameter, free-standing vicinal (0001) GaN substrates miscut 0.4° in the m-direction. Si-doped, n-type GaN substrates grown by hydride vapor phase epitaxy were sourced from a commercial vendor who used different processes to generate substrates with an arrayed dot core pattern of threading dislocations and GaN substrates with a nominally uniform distribution of threading dislocations (i.e., without dot cores). Both substrate types had dislocation densities on the order 10^6 cm^{-2} or lower except at locations of the dot-core structure. GaN epilayers were grown in a Veeco D-125 MOCVD growth system at 200 torr and a pyrometer temperature of 1050-1060 °C using trimethylgallium, ammonia, hydrogen and nitrogen. Silane diluted in nitrogen was used for the n-type dopant. The epi structure on the dot-core substrate was grown using a TMGa molar flux of 38.6 μmoles/min and a V/III ratio of 11,550 while the epi structure grown on the uniform substrate was grown using a TMGa molar

flux of 77.3 µmoles/min and a V/III ratio of 5780. Both conditions have been used to grow pn

diodes that have demonstrated multi-kilovolt reverse breakdown voltages.[1,6]

Synchrotron double crystal X-ray topography images were generated at the 1-BM

beamline of the Advanced Photon Source at Argonne National Laboratory. The (11$\underline{2}$4) GaN

asymmetric reflection was measured in the glancing incidence geometry using an X-ray energy

of 8.05 keV. The (333) Si reflection of a ~46° miscut (111) Si beam conditioner was used as the

first crystal to expand the incident X-ray beam to illuminate the entire 2-inch GaN substrate. All

X-ray topography images were recorded on Agfa Structurix D3 X-ray films. Two types of X-ray

topography images were generated: single exposure and superimposed images. Single exposure

images expose separate pieces of film for each point along the rocking curve. Superimposed

images are obtained by exposing a single piece of film to multiple points along the X-ray rocking

curve. As demonstrated in our previous work for a diverse roster of materials, more information

is preserved by recording single exposure images, e.g., tilt and strain can be deconvoluted and

magnitude of tilt and/or strain can be extracted.[15,16,17,18,19] Furthermore, our recent work for bare

GaN substrates developed a methodology for generating tilt maps from film by superimposing

single exposure images to visualize how lattice distortion is distributed spatially across a

wafer.[20,21]

Optical microscopy images of the wafer surface were measured on a VHX-1000 Keyence

digital microscope. The surfaces were also characterized using a Veeco Dektak 6 profilometer

and a Quesant QScope 250 to generate atomic force microscopy (AFM) images.

9.3 Results and Discussion

Growth was first performed on HVPE dot-core GaN substrates. No surface features were observed optically over the entire bare substrate surface prior to growth. After ~11 μm of homoepitaxial GaN growth on these dot-core substrates, both specular regions and hazy regions were observed corresponding to Figure 9.1(a) and 1(b), respectively.
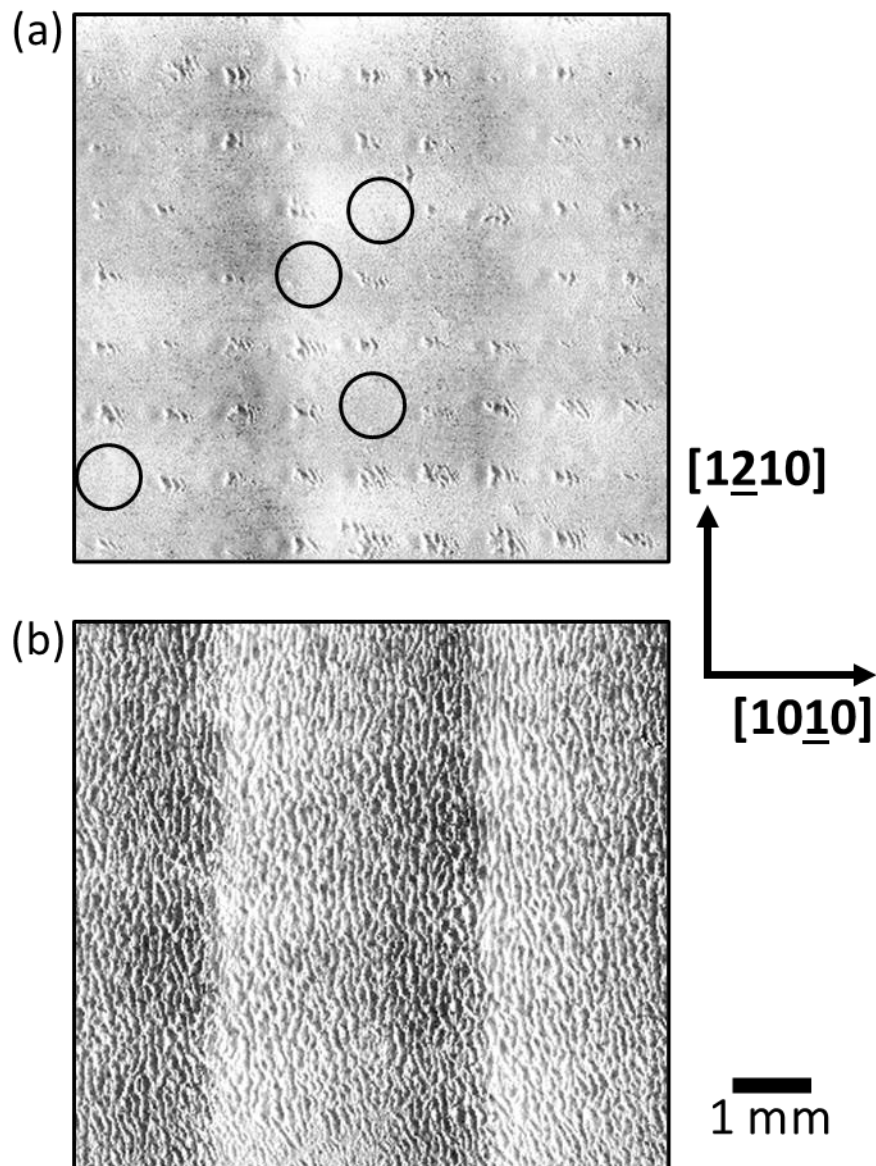

Figure 9.1. After 11 μm growth on a vicinal HVPE GaN substrate with periodic cores. Optical microscope images of (a) an optically specular region and (b) optically hazy region from the

same wafer. The macro-steps and macro-terraces are aligned along the [10$\underline{1}$0], which is also along the substrate miscut direction. Black circled regions in (a) correspond to places where there is an underlying core, but no macro-step or macro-terrace feature is observed. These circles also correspond to the same circles on the lattice tilt map in Figure 9.3(a). Both images share the same scale bar. Note that the vertical soft contrast lines are image stitching artifacts.

While the specular regions appear optically smooth to the naked eye, magnified optical images as shown in Figure 9.1(a) reveal that these specular regions consist of confined groups of macro-step and macro-terrace features aligned along the [10$\underline{1}$0] and spaced ~0.8 mm apart in a periodic array. This periodicity matches the spacing of the cores in the underlying substrate, indicative the high-defect-density cores play a role in the initial growth of these macro-steps and macro-terraces. Our previous work structurally characterized dot-core GaN substrates and found the distortion at the cores is predominately lattice tilt.[20,21] A large field-of-view superimposed X-ray topography image after the 11 μm growth is shown in Figure 9.2. The dark contrast corresponds to diffracted intensity and the periodic butterfly-shaped contour lines correspond to localized lattice tilt distortion from the cores. The relatively uniform contrast between the highly distorted cores correspond to flatter and less defective GaN. We observe that the localized lattice tilt concentrated at the cores serve as nucleation sites for the macro-steps and macro-terraces to form. Work by Fujikura et al.,[11] demonstrated a correlation between miscut of the substrate and the formation or suppression of these macro-steps and macro-terraces at a given growth temperature or V/III ratio. By extension, we find that the radial lattice tilt distortion at the cores[21] can be thought of as localized miscut regions on the substrate. Figure 9.1(a) shows that the macro-step and macro-terrace features initially nucleate at the core centers before growing

laterally and ultimately coalescing with each other as shown in Figure 9.1(b). In contrast, we typically do not observe nucleation of these features on regions between the cores where the GaN is relatively flatter and lower defect density. The threading dislocation density at the cores is reported to be $\sim10^8$ cm^{-2}, while between the cores within the flatter regions the threading dislocation density is $\leq 10^4$ cm^{-2}.[13,14] For comparison, the radius of lattice curvature across the cores ranges from ~0.1 m to ~0.4 m, while the overall curvature of the entire substrate (i.e. the material between the cores) is a much flatter ~90 m. This insight is not apparent when only studying the optically hazy regions of the wafer – the periodicity of the underlying cores is obscured by the complete surface coverage of these features. Surfaces similar to that shown in Figure 9.1(b) are reported in the current literature, but the initial nucleation of these features as shown in Figure 9.1(a) has not yet been reported to the best of our knowledge. Furthermore, the periodicity of the grouped macro-steps and macro-terraces replicating the underlying core spacing has not been documented when growing on dot-core GaN substrates.
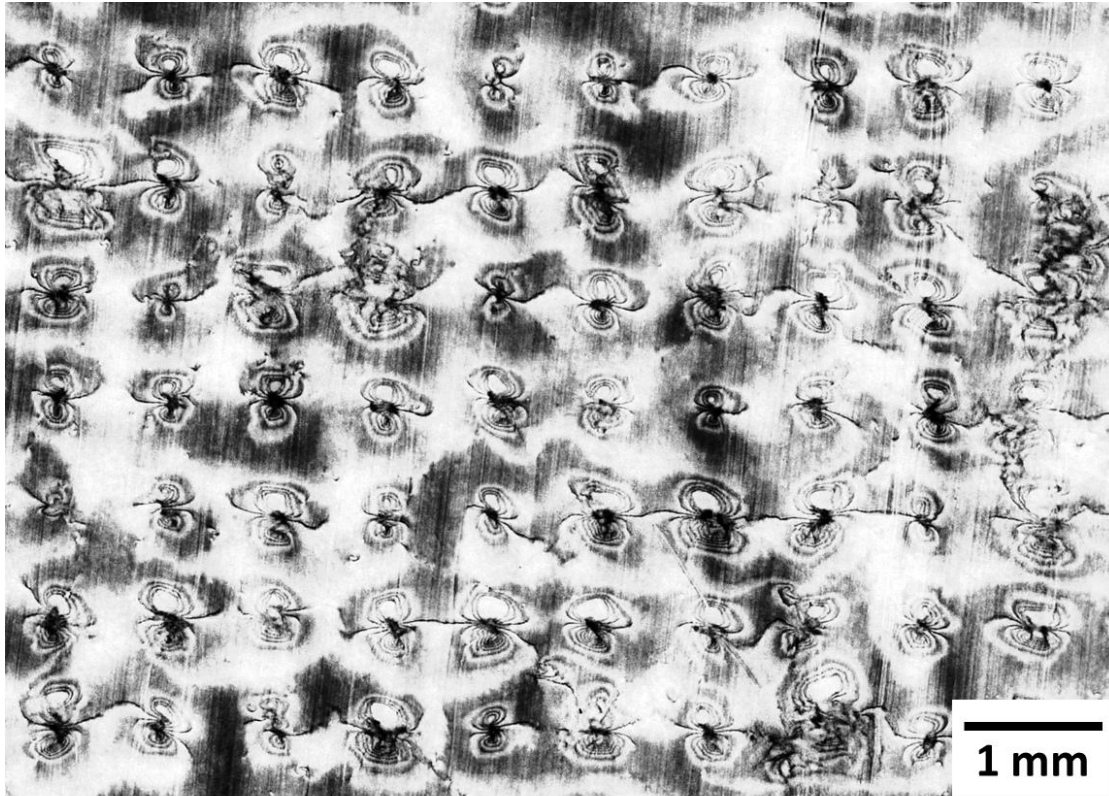
Figure 9.2. Superimposed (11$\underline{2}$4) X-ray topography image of the 11 μm epilayer on HVPE GaN substrate with periodic cores using a ~40" step size over a range of ~670" along the rocking curve axis. Dark contrast corresponds to diffracted intensity. The diffraction contours around each core center corresponds to high localized lattice distortion (radius of curvature ranges from ~0.1 m to ~0.4 m). Regions between the cores correspond to low lattice distortion (i.e. low defect density and low lattice misorientation), which corresponds to uniform contrast. The cores have a periodicity of ~0.8 mm.

X-ray topography lattice tilt maps shown in Figure 9.3 were generated for the same regions shown in Figure 9.1, where Figure 9.3(a) corresponds to the optically specular region and Figure 9.3(b) corresponds to the optically hazy region. The maps were generated over a ~58" angular range tilted along the rocking curve axis. Single exposure images were overlayed and

colored according to their relative position along the rocking curve axis. In both Figure 9.3(a) and 3(b), the highly distorted cores correspond to the butterfly-shaped high color contrast features spaced ~0.8 mm apart. These lattice tilt maps show that areas with the same color correspond to where the lattice is aligned and diffracting simultaneously at a given angle along the rocking curve axis. Areas with different colors correspond to regions that are tilted away from each other and consequently diffract at a different angle. Having a high color contrast over a relatively short spatial distance, e.g. on the cores where the colors range from purple to red over a ~0.5 mm distance, corresponds to high lattice distortion – curvature in this case because the distortion is due to lattice tilt. While all cores exhibit localized lattice tilt distortion, it can be seen in Figure 9.3 that not all the core distortions are not identical. The distortion field typically spans radially over a ~0.5 mm distance and > 120". Interestingly, the distortions over the cores (~15" to ~60") circled in Figure 9.3(a) are smaller (~0.25 mm), and on the surface there are no macro-steps nor macro-terraces over these same cores as shown in Figure 9.1(a). Having the lattice tilt distortions confined to a smaller area, thus resulting in a larger fraction of less defective and flatter material around the core, clearly suppresses the formation of these macro-step and macro-terrace features. Note that even though the lattice tilt map in Figure 9.3(b) clearly shows the distortions of the underlying cores within the hazy regions of the wafer, the lateral growth and coalescence of the macro-features shown in Figure 9.1(b) hinders any determination as to where these macro-steps and macro-terraces nucleate.
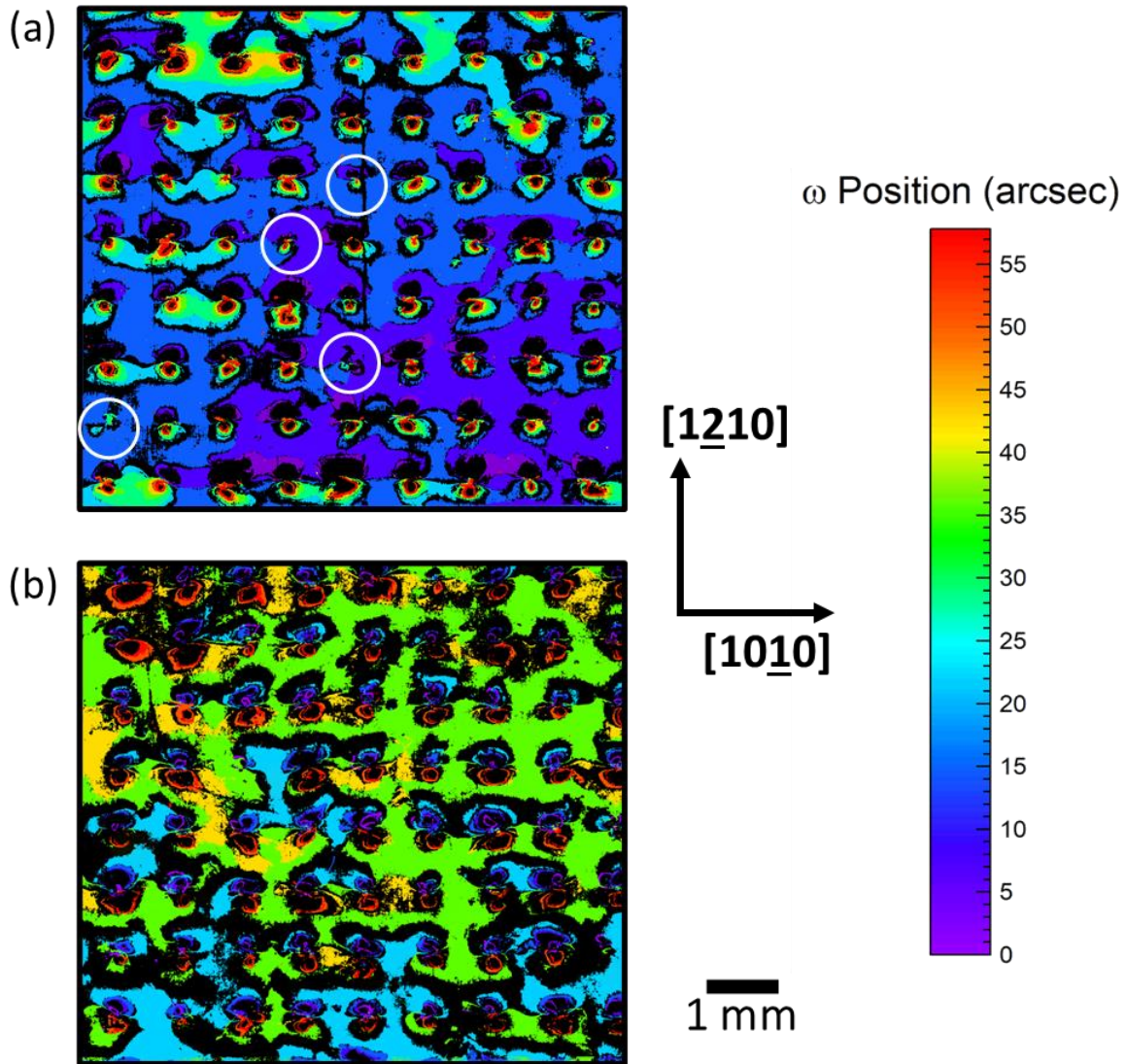
Figure 9.3. Lattice tilt maps generated from single exposure X-ray topography images for (a) a specular region and (b) a hazy region. These correspond to the same regions shown in the optical microscopy images of Figure 9.1(a) and 1(b), respectively. The total range for these maps is ~58" along the rocking curve axis, and the step size is ~7" between each subsequent exposure. Black corresponds to regions of the material that diffract outside the total ~58" scanning range. Regions with high color contrast correspond to high lattice tilt distortions, e.g. the periodic cores spaced ~0.8 mm that correspond to the butterfly-shaped contour lines. Regions with low color contrast correspond to flatter lattice curvature, e.g. large contiguous regions of purple, blue, and

green between the cores. White circles in (a) correspond to regions where no macro-steps or macro-terraces are observed optically on the surface as shown in Figure 9.1(a). Both maps share the same scalebar and color scale.

The presence of dislocations and nanopipes can be optically observed after wet etching.[22,23] A planview optical image of the etched surface is shown in Figure 9.4 after etching with 85% H_3PO_4 at 190 °C for 3 hours, where the intersections of the dotted lines correspond to the core centers. It can be seen the etch pits that correspond to dislocations are concentrated at the core centers, which give rise to the high localized lattice distortion measured with X-ray topography, as shown in Figure 9.2 and Figure 9.3. The larger pits correspond to threading screw dislocations (or nanopipes) while the intermediate-sized and small pits are mixed dislocations and edge dislocations, respectively. Between the cores, little to no dislocations were observed, consistent with the uniform contrast between the cores measured in X-ray topography. Interestingly, the screw dislocation or nanopipe pits were only observed at the highly distorted cores. As discussed later, we propose nanopipes are the primary contributor to macro-feature formation on GaN substrates with uniform threading defect density without dot cores.
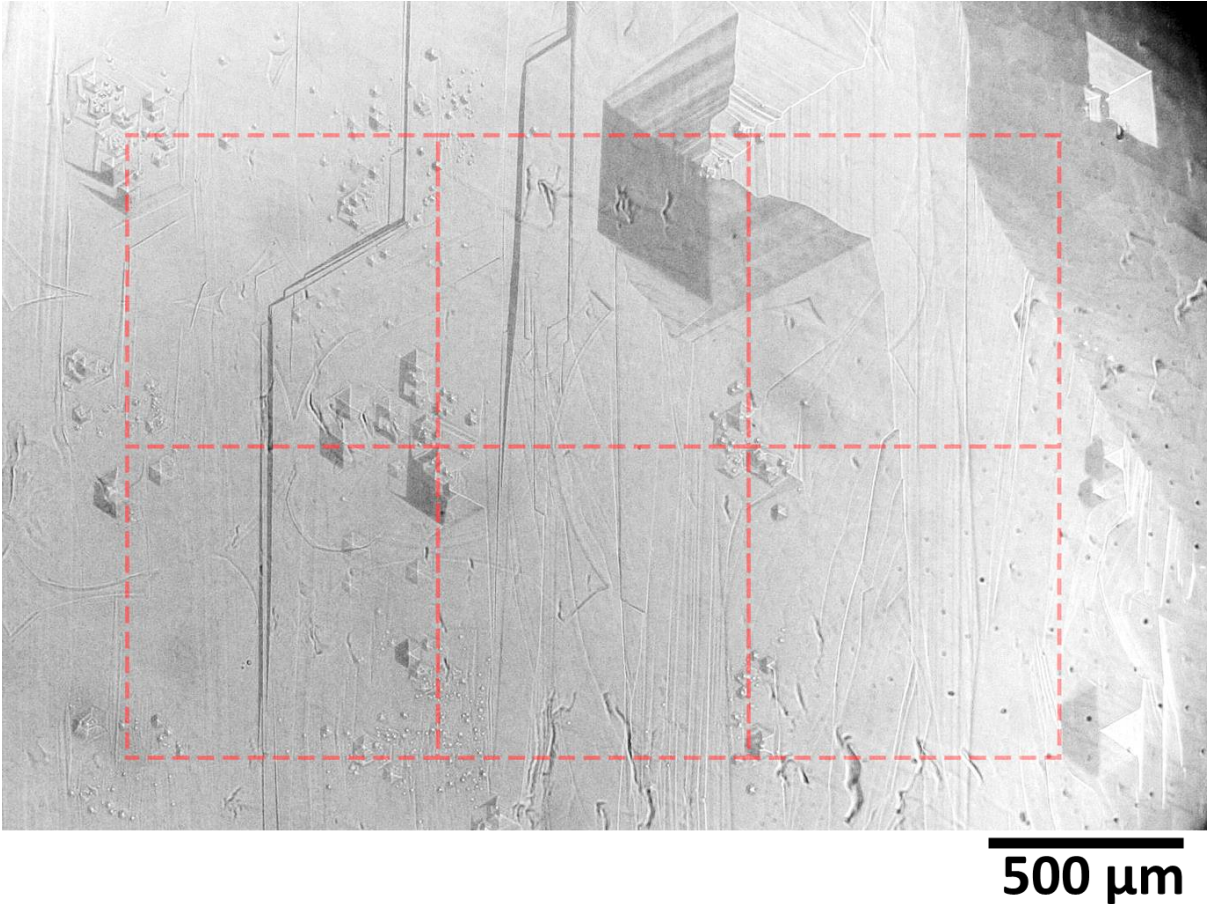
500 μm

Figure 9.4. Planview optical image of the surface of a wet etched dot core GaN substrate. The intersection of the dotted lines corresponds to the core centers. The linear features are on the backside of the substrate which were also etched simultaneously (these are not the same features associated with the macro-terrace and macro-step features). The backside of the substrate were rough and not polished; the linear etched features are associated with damage from the wafer slicing and grinding process.

Linear profilometer measurements were measured along a row of cores both within the specular and hazy regions, as shown in Figure 9.5(a) to 5(b). The macro-terrace lengths ranged from ~30 μm to ~150 μm and the heights ranged from ~200 nm to ~400 nm. Consistent with the optical microscopy images, groups of macro-steps and macro-terraces are spaced ~0.8 mm apart

112

in the profilometer scan within the specular region as shown in Figure 9.5(a). The macro-step

lengths were most easily resolved using AFM, as shown in Figure 9.6(a) and 6(b), where the

length is ~10 μm. The macro-step and macro-terrace lengths measured in this study are

comparable to what was observed by Fujikura et al.[11] The order of magnitude higher in macro-

feature height compared to Fujikura et al.,[11] may be attributed to the differences in growth

conditions (temperature and V/III ratio). Similar to observations reported by Fujikura et al.,[11] the

AFM shown in Figure 9.6(a) and 6(b) reveals a high density of step bunching with step lengths

of ~0.5 to ~1 μm and step heights of ~2 nm to ~5 nm within the macro-step. The AFM image

shown in Figure 9.6(c), from a region between the cores, shows relatively flatter morphology

free of both macro-features and step bunching. Both the surface and the underlying GaN lattice is

flatter in these regions between the highly distorted cores. Coupled with results from our

previous studies that demonstrated annealing GaN substrates at elevated temperatures reduces

the lattice curvature (tilt),[20,21] a pre-growth annealing of substrates may be a way to suppress the

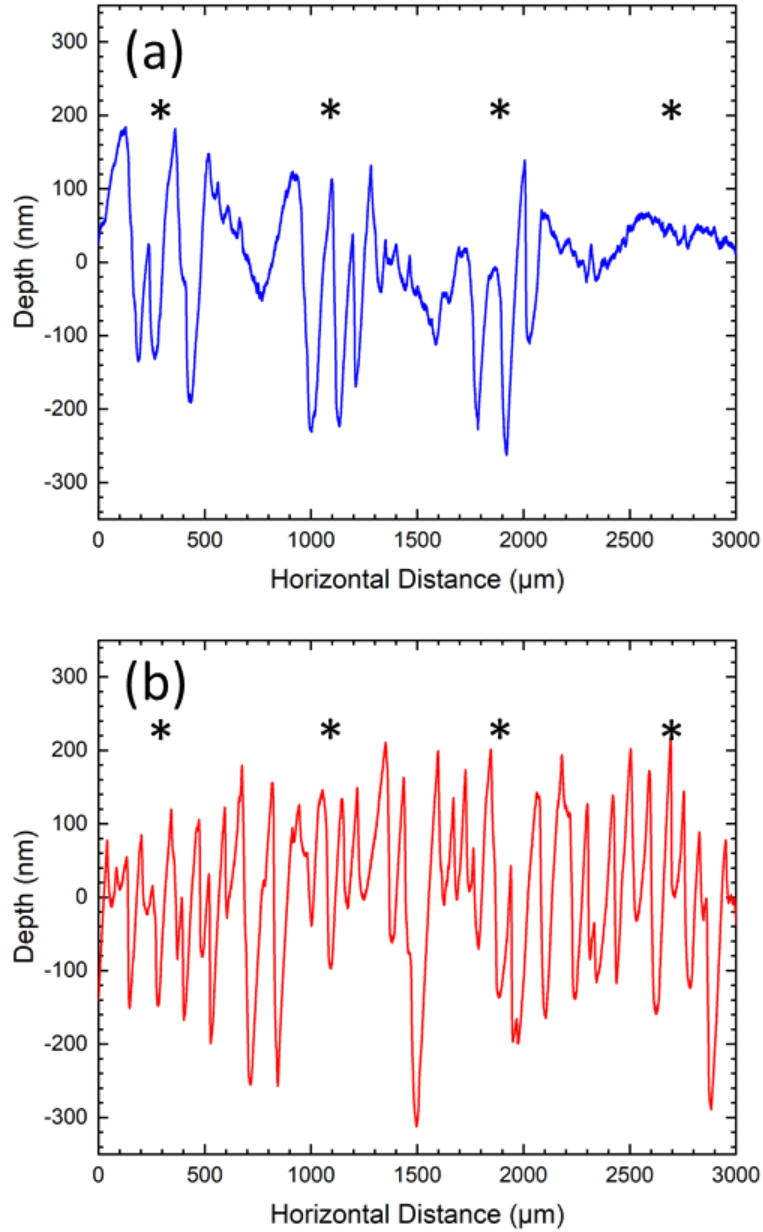nucleation of these macro-steps and macro-terraces.

Figure 9.5. Profilometer scans of the surfaces taken over the centers of cores in (a) a specular region and (b) a hazy region. The asterisks spaced ~0.8 mm mark the centers of underlying cores – showing that the stepped features start to nucleate on the highly distorted cores. The average macro-terrace length is ~80 μm (ranging from 30 μm to 150 μm).
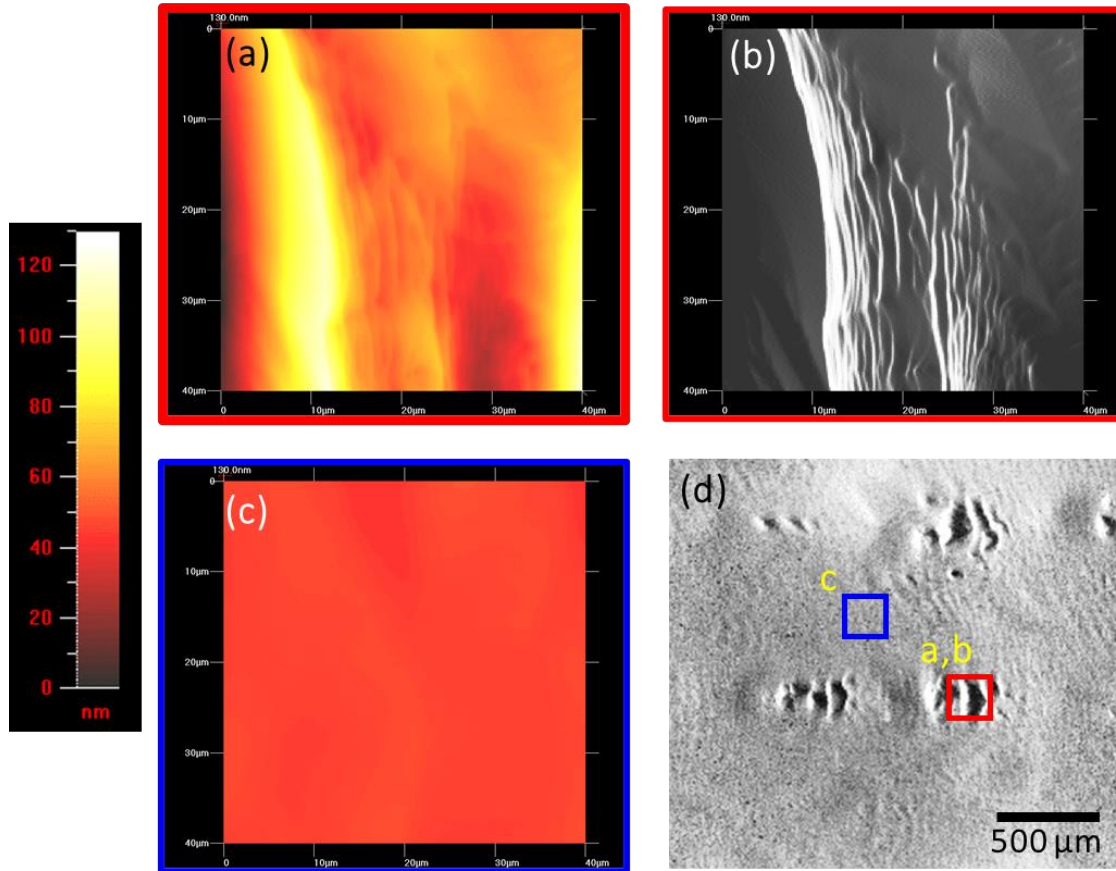
Figure 9.6. 40×40 μm^2 atomic force microscopy images of (a,b) taken on a macro-feature centered over a core and (c) taken on a smooth, featureless region between the periodic array of cores as indicated on the optical image in (d). (a) is a height image while (b) is the amplitude error signal image of the same area to enhance the contrast of the step bunching especially within the macro-step. The steps within the macro-step shown in (a,b) are ~1 μm in length. The r.m.s. roughness is 11 nm. Within the featureless smooth region shown in (c), the r.m.s roughness is 1.1 nm.

The surfaces of homoepitaxial GaN (28 μm thick) growth on HVPE GaN substrate without periodic cores were also examined. An optically hazy region due to macro-steps and

macro-terraces is shown in Figure 9.7, which covered ~70% of the total 2-inch wafer surface. The macro-terraces are ~40 μm in length while the macro-step heights are ~300 nm, which are aligned along the [10$\underline{1}$0] direction. The substrate is miscut along the same [10$\underline{1}$0] direction. Note that unlike the dot-core GaN substate, there are no periodic defect-concentrating cores present and thus the defect distribution is expected to be relatively uniform across the wafer and not exhibit any spatial periodicity or pattern. We speculate that threading screw dislocations (or GaN nanopipes), in particular the spiral growth over this type of dislocation, are the primary source of localized lattice tilt for the nucleation of the macro-steps and macro-terraces on this non-dot-core GaN substrate. Faint outlines of hillocks were observed on the macro-terraces as shown in Figure 9.8(a). AFM for one of these hillocks is shown in Figure 9.8(b) and 8(c). This hillock is ~15 nm tall at the apex, consists of six hillock edges that are ~10 nm in height, and six hillock facets. The hillock edges follow along the <10$\underline{1}$0> directions while the hillock facets follow along the <11$\underline{2}$0> directions. The magnified AFM image of the hillock apex shown in Figure 9.8(d) shows spiral growth over a threading screw dislocation,[24] which is well documented for GaN in the literature.[9,25,26,27,28] From the optical images shown in Figure 9.8(a) and especially in Figure 9.9(a), it is apparent that these macro-terrace features consist of these hillocks due to spiral growth over threading screw dislocations. We propose that these macro-terraces on this substrate initially nucleate as hillocks and the coalescence of these hillocks results in the formation of the macro-terraces and macro-steps as shown in Figure 9.7, 8(a), and 9(a). Within the haze regions of the wafer, the nanopipe density is estimated to be ~3×10^3 cm^2 calculated from Figure 9.9(a), while within specular regions free of macro-features the density is much lower ~2×10^1 cm^{-2} calculated from Figure 9.10. Single exposure X-ray topography images of the same region as Figure 9.9(a) are shown in Figure 9.9(b) and 9(c). Despite the high threading dislocation density

($> 10^6$ cm^{-2}) making it difficult to clearly identify the threading screw dislocation under the hillock apexes, it is still evident the lattice at the hillocks exhibit lattice tilt distortion. For example, the circle and arrow features in Figure 9.9(b) and Figure 9.9(c) diffract at different angles (20" apart in this case) than the surrounding material along the rocking curve axis. Note that dark contrast corresponds to diffracted intensity while light contrast corresponds to no diffraction.
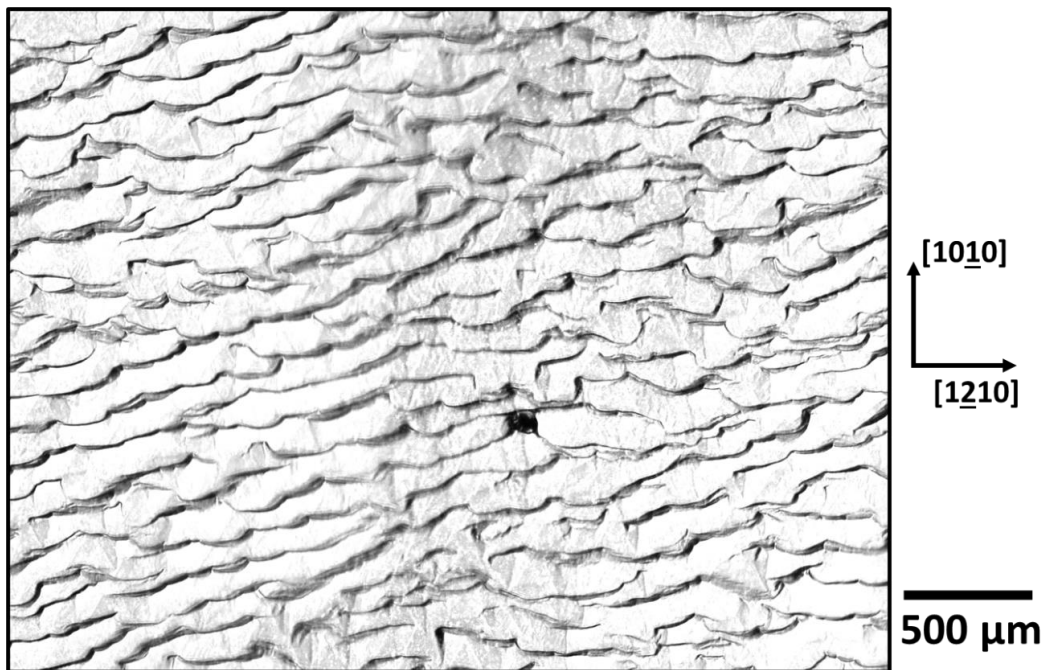

Figure 9.7. Optical image of the surface of the HVPE GaN substrate without periodic cores after 28 μm of homoepitaxial growth. The average macro-step height and macro-terrace length are ~300 nm and ~40 μm, respectively. The macro-features follow along the [10$\underline{1}$0] direction, which is also the miscut direction for this substrate. The substrate miscut is ~1°.
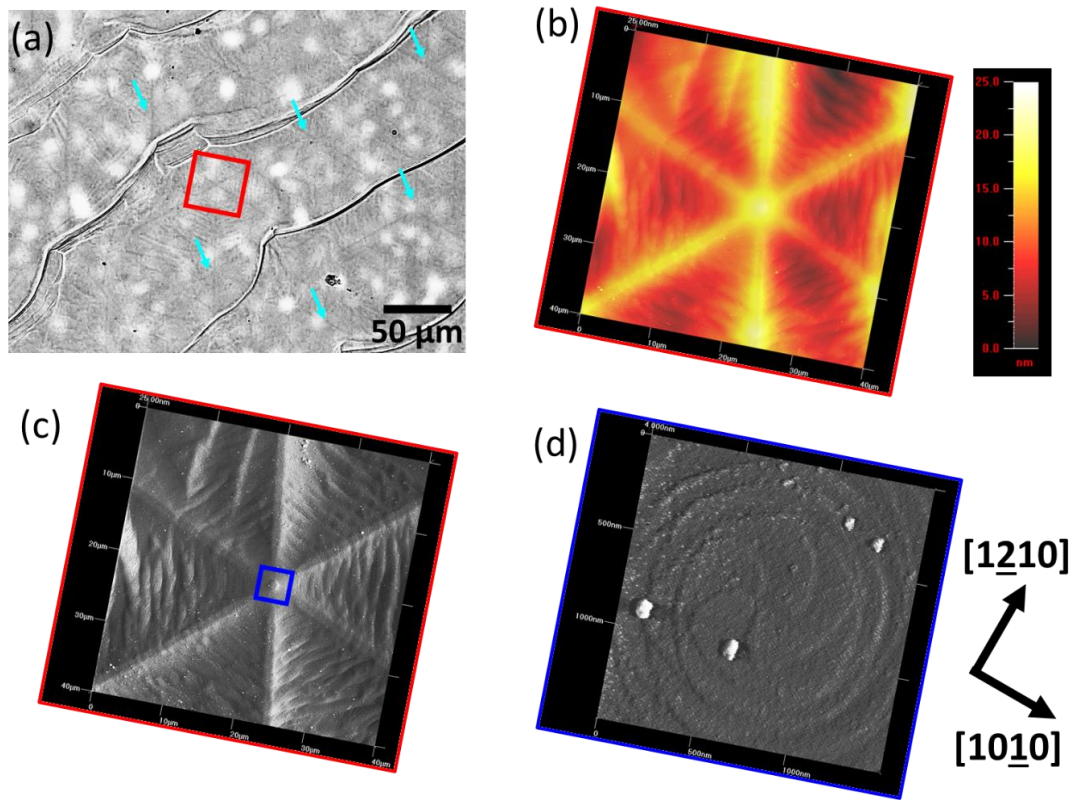
Figure 9.8. (a) Optical image of the surface of the HVPE GaN substrate without periodic cores after 28 μm of homoepitaxial growth with examples of hillocks highlighted on the macro-terraces. The outline of a hillock appears as a faint dark contrast in the optical image. The box corresponds to where the AFM in (b) was taken. (c) is the amplitude error signal image of the same area in (b) to enhance the contrast and highlight the hillock apex, edges, facets, and step bunching. (d) is an amplitude error signal image of the hillock apex that shows spiral growth over a threading screw dislocation.

Figure 9.9. (a) Optical image of the surface of the HVPE GaN substrate without periodic cores after 28 μm of homoepitaxial growth over an optically hazy region. The corresponding single exposure X-ray topography images using the (112$\underline{4}$) GaN reflection are shown in (b) and (c). (b) and (c) are separated by ~20" tilted along the rocking curve axis. Dark contrast corresponds to

119

diffracted intensity. The threading dislocation density is $> 10^6$ cm^{-2}. Circles and arrows correspond to the same features to help guide the eye. All images share the same scale bar.
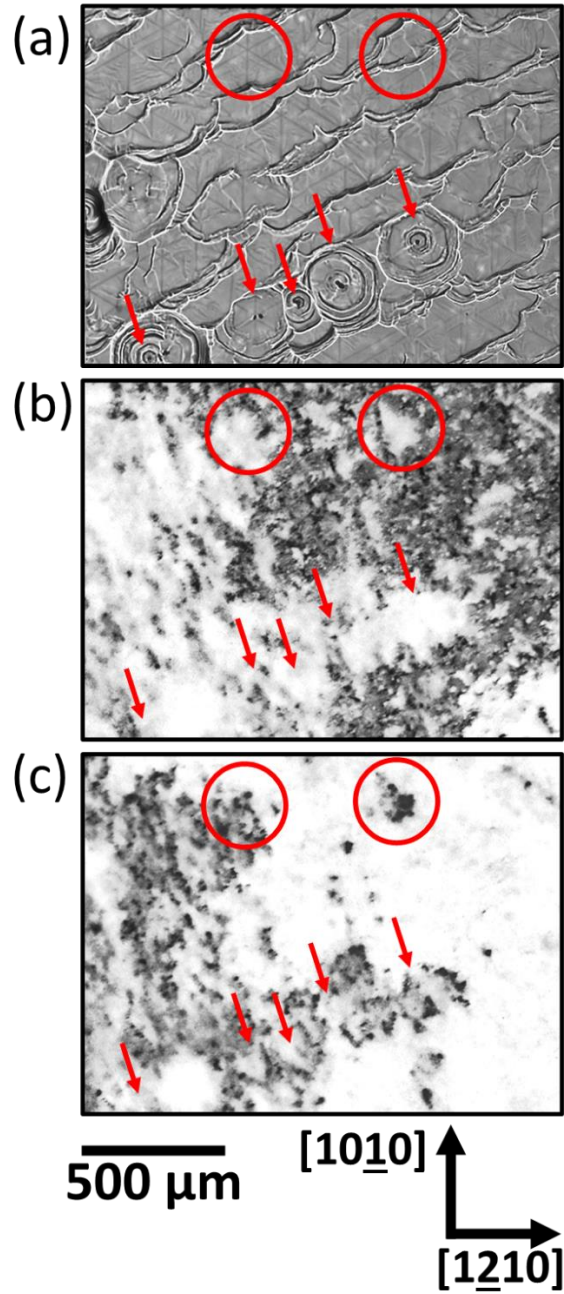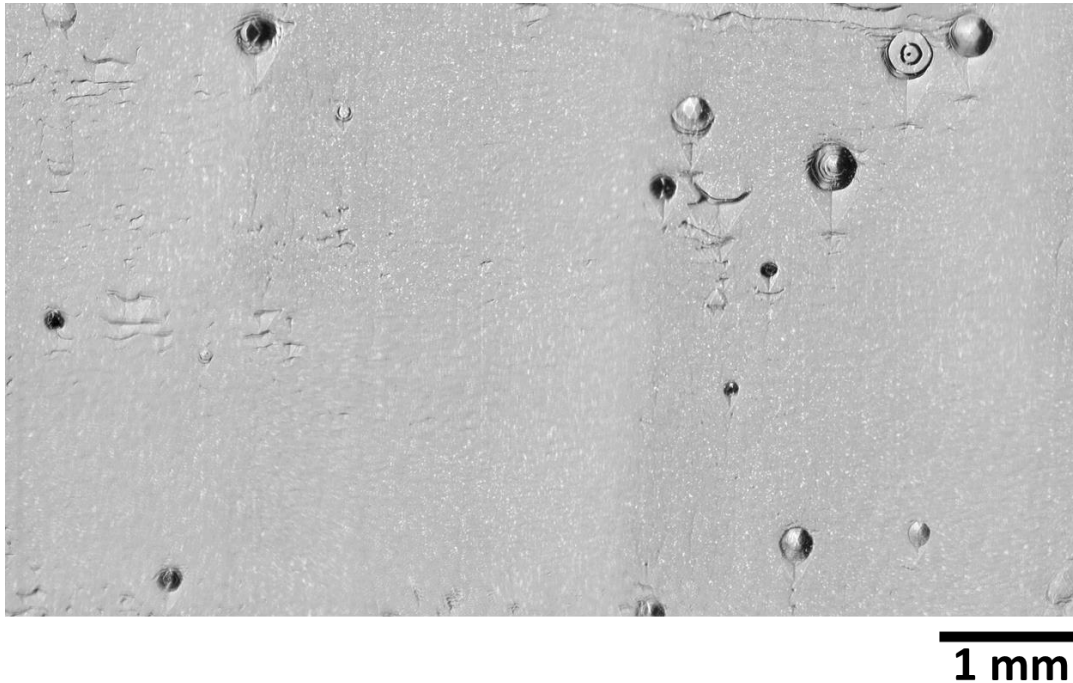

1 mm

Figure 9.10. Optical image of the surface of the HVPE GaN substrate without periodic cores after 28 μm of homoepitaxial growth over an optically specular region. The nanopipe density is $\sim 2 \times 10^1$ cm^{-2}, which is much lower than the density within hazy regions ($\sim 3 \times 10^3$ cm^2 shown in Figure 9.8).

Lastly, another source of localized lattice distortion are surface scratches on the substrate that may be introduced during polishing prior to growth. Across the wafer there were instances of aligned hillocks that were not following any specific crystallographic direction. Examples of hillocks aligned along seemingly arbitrary directions are shown in Figure 9.11(a). We observe that growth over scratches results in a series of hillocks that follow along the path of the scratch.

The single exposure X-ray topography images of the corresponding area are shown in Figure 9.11(b), 11(c), and 11(d), which are separated by ~7" along the rocking curve axis. Scratches appear as ~mm long features, with widths on the order of tens of μm. Even though these substrate surface scratches present prior to growth have widths on the order of tenths of μm, the resulting distortion field around the scratches are much larger – on the order of tens of μm as shown in the X-ray topography images. These aligned hillock features can be avoided by growing on scratch-free substrates, which can be obtained by employing gentle, abrasive-free chemical mechanical polishing.[29]
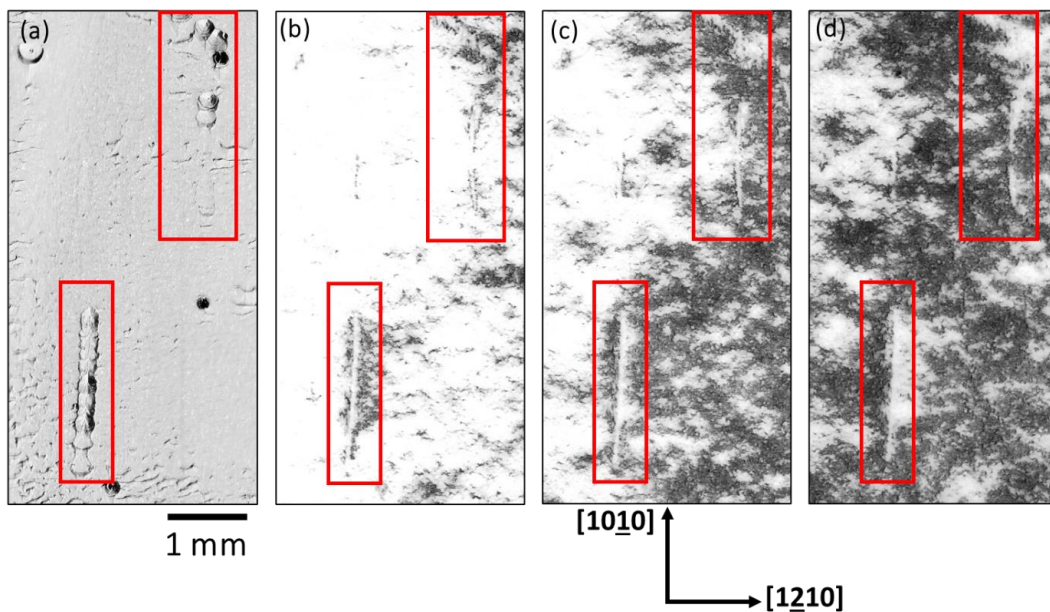
Figure 9.11. (a) Optical image of the surface of the HVPE GaN substrate without periodic cores after 28 μm of homoepitaxial growth focused on the growth features over scratches. The corresponding area imaged using X-ray topography is shown in (b), (c), and (d). Each subsequent topography image is separated by ~7" along the rocking curve axis. Diffraction at the centers of the scratches were not captured within the full range of the topography measurement (~320"). The lattice here is heavily distorted and beyond the measured range.

We have shown here that localized lattice distortion from the defects such as screw dislocations (nanopipes) and surface scratches serve as nucleation sites for macro-features to form and eventually coalesce laterally along the surface. Therefore, decreasing the density of these defects would enable us to grow thicker epilayers with smooth morphology. Assuming dot core substrates have at least 1 nanopipe at each core, the nanopipe density would be $\sim6 \times 10^2$ cm^{-2}. Compared to the substrates without periodic cores with 28 μm of epilayer grown in this work, the hazy regions have a density of $\sim3 \times 10^3$ cm^{-2} while the specular regions have an even lower density of $\sim2 \times 10^1$ cm^{-2}. Initial results of growing ~60 μm of epilayer on substrates without periodic cores is shown in Figure 9.12. Areas as large as $\sim18 \times 20$ mm^2 with smooth surfaces free of macro-terraces and macro-steps were achieved. Within this region, there are no features present, such as grown on screw dislocations or macro-terraces or macro-steps. These results are promising, which demonstrate thick epilayers required for ~kV devices are possible when growing on very low defect density (e.g., $< 10^{-1}$ cm^2 shown in Figure 9.12). Smooth surfaces not only enable the fabrication of devices, but also facilitate wafer bonding and GaN device layer transfer[30,31] to higher thermal conductivity substrates.
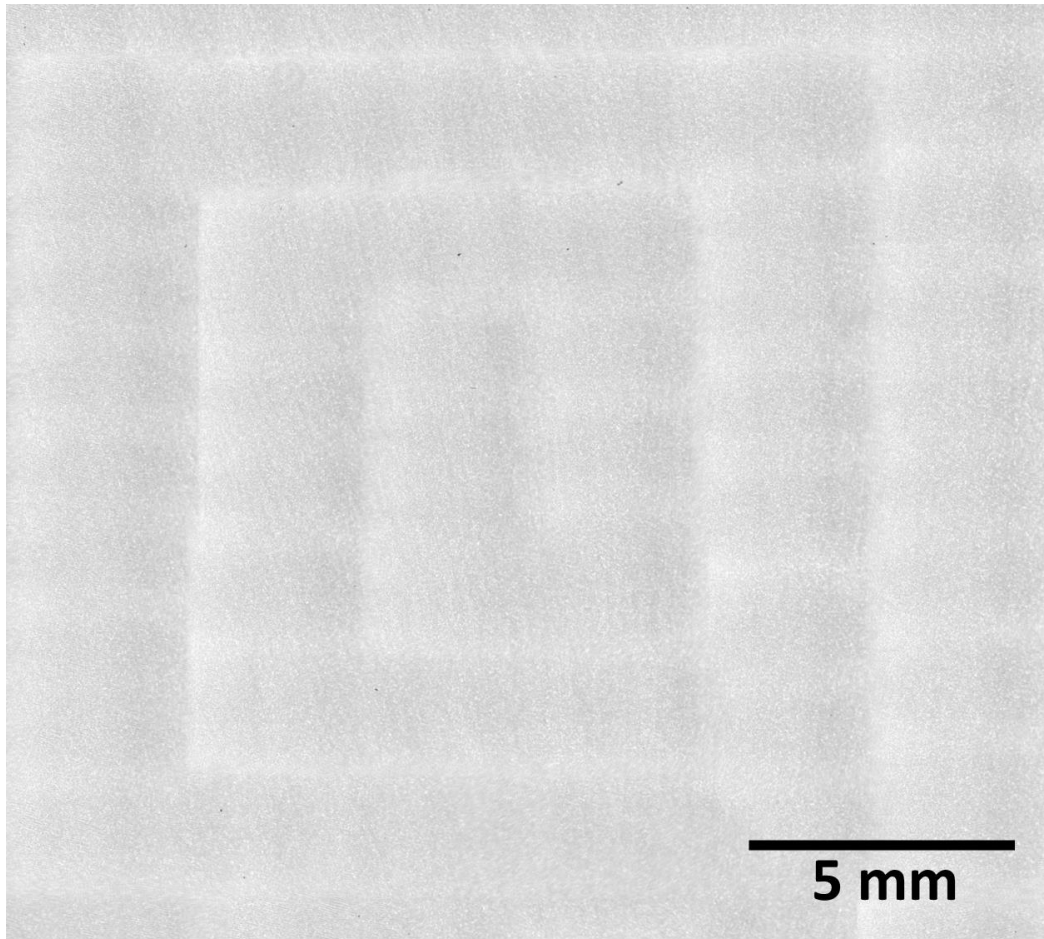
Figure 9.12. Planview optical microscope image of a GaN surface after ~60 μm of growth. Smooth surfaces were achieved over areas as large as ~18 × 20 mm^2 as shown here. Note that the vertical soft contrast lines are image stitching artifacts.

9.4 Conclusion

Thick homoepitaxial GaN layers were grown using MOCVD to study the origins of macro-steps and macro-terraces that give rise to optically hazy surfaces. Dot-core GaN substrates were used as defect-engineering samples and showed that localized lattice tilt distortions serve as nucleation sites for these macro-steps and macro-terraces to form. Growth over flat, defect-free material resulted in feature-less material, i.e. surfaces suitable for devices. Growth over a non-

dot-core GaN substrate with a threading dislocation density of $> 10^6$ cm^{-2} resulted in macro-terrace features made up of hillocks (screw dislocations or nanopipes). We observe evidence of lattice tilt distortion at these hillocks and speculate that hillocks initially form and the coalescence of neighboring hillocks form macro-terraces and macro-steps Surface scratches from polishing damage on the substrate prior to growth also serve as localized lattice tilt regions. We find that hillocks grow and align along the whole length of the scratch. Even if a substrate has flat, defect-free regions, the presence of any localized defective, lattice-tilted regions on a given substrate leads to the coalescence of macro-features that ultimately compromise the entire wafer surface. Having wafer-scale defect-free and flat substrates are crucial for achieving thick and smooth epitaxial layers necessary for high power vertical devices and to facilitate bonding and layer transfer.

9.5 References

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Chapter 10: Conclusion and Future Work

Successful developments and fundamental understanding of processing β-Ga_2O_3 and

GaN for heterogenous integration were presented in this dissertation. Smooth surfaces and

damage-free β-Ga_2O_3 were achieved with chemical mechanical polishing parameters compatible

with both epitaxy and wafer bonding and transfer of thin layers. Exfoliation along a non-

cleavage plane was demonstrated using ion implantation. Both polishing and exfoliation enabled

the application of both techniques in conjunction to bond and transfer a thin film of β-Ga_2O_3 on

4H-SiC. Model systems using simpler structure materials (cubic crystal structures) of Si|Si and

InP|InP leveraged further understanding of interfaces between materials that do not share the

same crystal structure and guided the decision of which orientations to integrate (i.e., ($\overline{2}$01) β-

Ga_2O_3 | (0001) 4H-SiC out-of-plane, with [010] β-Ga_2O_3 ∥ [11$\overline{2}$0] 4H-SiC in-plane). The origin

of surface roughening that emerges during thick homoepitaxial GaN growth (> 10 μm) was

determined to nucleate from the lattice distortions over defects. This surface roughening is

speculated to apply to β-Ga_2O_3 in the future when growth techniques develop towards the > 10

μm epitaxy regime.

To fully realize the potential of these wide bandgap materials, direct wafer bonding of β-

Ga_2O_3 without the use of interlayers should be studied. Bonding to materials such as 4H-SiC,

AlN, and diamond is expected to be technologically relevant. Furthermore, device layers such as

$(Al_xGa_{1-x})_2O_3$ should be grown on bonded and transferred β-Ga_2O_3 on 4H-SiC to develop wide

bandgap devices on so-called composite wafers (thin film of β-Ga_2O_3 on 4H-SiC substrates).

Most importantly, a fundamental analysis of defects in wide bandgap materials will be crucial for

identification and mitigation of defects detrimental to device performance.