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Design and TCAD-Based Evaluation of a 20 nm Bulk CMOS Technology Platform for Low-Power Logic Applications

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***Abstract*—**This report presents the TCAD design, optimization, and validation of complementary 19 nm NMOS and PMOS devices for high-performance CMOS logic applications. The design is evaluated against 2013–2014 ITRS-inspired targets, including $V_{DD} = 0.85$ V, EOT ≤ 0.77 nm, $I_{\text{off}} \leq 100$ nA/μm, and an NMOS saturation-current target of 1355 μA/μm. The simulated devices use a planar bulk MOSFET architecture with an HfO_2 high-k gate dielectric, shallow source/drain regions, LDD extensions, halo implants, and work-function-based threshold-voltage tuning. The high-k gate stack improved NMOS drive current compared with a SiO_2-only gate stack, increasing $I_{D,\text{sat}}$ from 1167 to 1743 μA/μm in the gate-stack comparison. For the final transfer-characteristic extraction, the NMOS achieved $I_{D,\text{sat}} \approx 1750$ μA/μm, $I_{\text{off}} = 75.4$ nA/μm, $V_{T,\text{sat}} = 0.3221$ V, SS $= 68.3$ mV/dec, and DIBL $= 92.7$ mV/V. The PMOS achieved $I_{D,\text{sat}} \approx 700$ μA/μm, $I_{\text{off}} = 6.75$ nA/μm, $|V_{T,\text{sat}}| = 0.479$ V, SS $= 102.7$ mV/dec, and DIBL $= 102.5$ mV/V. The results demonstrate strong NMOS performance, acceptable leakage control, quantified halo/channel doping tradeoffs, and functional CMOS inverter switching. Remaining deviations include weak PMOS drive current, elevated threshold voltages, slightly high PMOS SS/DIBL, and inverter switching skew caused by NMOS/PMOS imbalance.

***Index Terms*—**CMOS, MOSFET, TCAD, Sentaurus, 19 nm, high-k dielectric, HfO_2, short-channel effects, DIBL, halo implant, LDD, ITRS, CMOS inverter.

I. Introduction

A. Motivation and Societal Context

The continued scaling of complementary metal–oxide–semiconductor (CMOS) technology remains essential for improving the energy efficiency, density, and computational throughput of modern integrated circuits. This need has become increasingly important as cloud computing, artificial intelligence, mobile systems, and high-performance computing continue to increase global electricity demand. Data centers and data-transmission networks now represent a major and growing source of electricity use, especially as artificial intelligence and other data-intensive workloads expand [1]. Therefore, improving transistor-level efficiency is directly connected to the broader sustainability challenge of reducing the energy cost of computation.

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At the device level, CMOS scaling affects system performance through switching energy, circuit density, and delay. Reducing supply voltage lowers dynamic power, while improved drive current enables faster switching and higher circuit performance. However, these benefits can only be realized if scaled transistors maintain low leakage and stable threshold-voltage control. For this reason, the design of 19 nm high-performance CMOS devices is not only a device-engineering problem but also a system-level problem connected to power consumption, chip density, and computing efficiency [2].

B. Technical Challenge and Project Objective

Although ideal scaling theory suggests that transistor dimensions and supply voltage can be reduced together, practical scaling near the 20 nm node introduces strong electrostatic and process-integration challenges. As the physical gate length approaches approximately 19 nm, the drain electric field increasingly affects the channel potential, producing short-channel effects such as drain-induced barrier lowering, threshold-voltage roll-off, degraded subthreshold swing, and increased off-state leakage. The 2013–2014 high-performance logic targets require a physical gate length near 18–20 nm, a supply voltage near 0.85 V, an equivalent oxide thickness below 1 nm, and controlled off-state leakage near 100 nA/μm [2]. These requirements cannot be satisfied by direct geometric scaling alone.

The objective of this project is to design and validate complementary NMOS and PMOS devices with a physical gate length near 19 nm using TCAD simulation. The design uses a planar bulk MOSFET structure with a high-k gate stack, shallow source/drain junctions, LDD extensions, halo implants, and threshold-voltage engineering to balance drive current, leakage current, subthreshold swing, drain-induced barrier lowering, manufacturability, and device reliability. Similar 20 nm CMOS demonstrations show that high-k/metal-gate integration and careful junction engineering are necessary for scaled planar CMOS operation [4]–[6].

C. Paper Organization

The remainder of this paper is organized as follows. Section II presents the technical background and design targets, including the ITRS high-performance logic requirements, short-

channel scaling physics, and CMOS inverter operation. Section III describes the device design strategy, including the main constraints, selected planar MOSFET architecture, and gate-stack/work-function assumptions. Section IV summarizes the process flow and doping profile design for the source/drain, LDD, channel, and halo regions. Section V explains the TCAD simulation methodology, including the physical models, bias conditions, and parameter-extraction methods. Section VI presents the main results, including device structures, doping profiles, high-k and doping-sensitivity studies, I_D–V_G and I_D–V_D characteristics, extracted parameter comparisons, and CMOS inverter voltage-transfer simulations. Section VII discusses manufacturability, sustainability, and modeling limitations, and Section VIII summarizes the main conclusions and future work.

II. Technical Background and Design Targets

A. ITRS High-Performance Logic Targets

The design targets used in this work are based on the 2013–2014 ITRS high-performance logic requirements for scaled planar CMOS technology. These targets define the main electrical and physical constraints for a 19 nm-class device, including gate length, supply voltage, equivalent oxide thickness, off-state leakage, saturation drive current, and threshold voltage. In this project, the ITRS values are used as the reference standard for evaluating whether the simulated NMOS and PMOS devices provide sufficient electrostatic control, low standby leakage, and high drive current for high-performance logic operation [2], [4]–[6].

TABLE I: ITRS-inspired high-performance logic targets used for the 19 nm CMOS design.

Metric	Target	Design Meaning
Physical gate length, L_g	$\sim$19 nm	Scaled CMOS node
Supply voltage, V_{DD}	0.85 V	Operating voltage
EOT	$\leq$ 0.77 nm	Strong gate control
I_{off}	$\leq$ 100 nA/μm	Low standby leakage
NMOS $I_{D,\text{sat}}$	1355 μA/μm	Drive-current target
$V_{T,\text{sat}}$	$\sim$200 mV	Threshold target

B. Short-Channel Effects and Scaling Tradeoffs

As MOSFET gate lengths approach the 19–20 nm regime, the gate no longer has complete electrostatic control over the channel. In a long-channel device, the gate voltage primarily determines whether the channel is on or off; however, in a short-channel device, the source and drain are close enough that the drain field can also influence the source-channel barrier. This produces short-channel effects such as drain-induced barrier lowering (DIBL), threshold-voltage roll-off, degraded subthreshold swing, and increased off-state leakage [2], [7]. DIBL is especially important because a high drain bias lowers the channel barrier, allowing current to flow even when the gate voltage is below threshold. As a result, the device becomes harder to turn off, and leakage becomes a major design constraint for scaled CMOS logic.

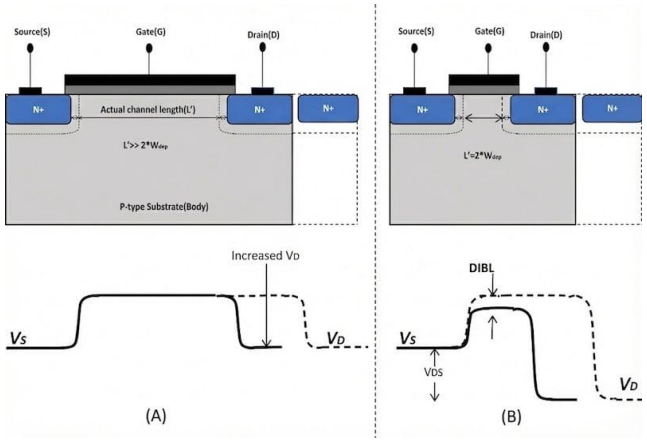


Fig. 1: Conceptual illustration of short-channel electrostatic effects in nanoscale MOSFETs. As the gate length is reduced, the drain field increasingly influences the channel barrier, causing DIBL, leakage, and threshold-voltage control problems [11].

Suppressing short-channel effects requires stronger electrostatic control, but this creates an important design tradeoff. Higher channel or halo doping can increase the channel barrier, reduce DIBL, improve subthreshold swing, and lower off-state leakage. However, stronger doping can also increase impurity scattering, reduce carrier mobility, increase threshold voltage, and lower the final drive current. Therefore, the design problem is not simply to maximize doping or minimize leakage; it is to balance leakage control, threshold voltage, subthreshold behavior, and saturation current. This tradeoff motivates the use of high-k gate dielectrics, shallow source/drain junctions, LDD extensions, and halo implants in the simulated 19 nm NMOS and PMOS devices [4]–[6].

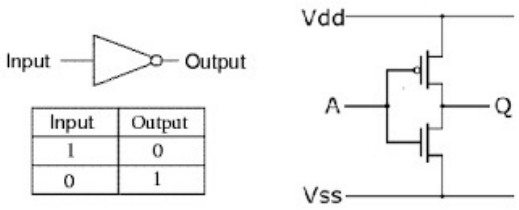
C. CMOS Inverter Operation and PMOS/NMOS Balance

The CMOS inverter is the basic digital switching element used to test whether the NMOS and PMOS devices work together as a complementary pair. In the inverter configuration, the PMOS source and body are connected to V_{DD}, the NMOS source and body are connected to ground, and both gates are driven by the same input voltage. When V_{in} is low, the NMOS is off while the PMOS is on, so the output is pulled high. When V_{in} is high, the PMOS is off while the NMOS is on, so the output is pulled low. The voltage-transfer characteristic therefore verifies whether the individual transistor designs can produce valid logic-high and logic-low levels at the circuit level [8], [9].

D. CMOS Inverter Operation and PMOS/NMOS Balance

A CMOS inverter connects a PMOS pull-up device and an NMOS pull-down device so that the same input voltage controls both transistors. When the input voltage is low, the NMOS is off and the PMOS is on, pulling the output toward V_{DD}. When the input voltage is high, the PMOS is off and the NMOS is on, pulling the output toward ground. The

voltage-transfer characteristic therefore provides a circuit-level test of whether the simulated NMOS and PMOS devices can operate together as a logic gate. Ideally, the inverter should produce valid logic-high and logic-low levels with a sharp transition region and a switching point that gives reasonable noise margins [8], [10].



Input	Output
1	0
0	1

Fig. 2: CMOS inverter schematic showing the PMOS pull-up network and NMOS pull-down network controlled by the same input voltage.

Because hole mobility in silicon is lower than electron mobility, a PMOS device with the same geometry as an NMOS device usually provides weaker drive current. In practical CMOS logic, this imbalance is normally addressed by increasing the PMOS width so that the pull-up current better matches the NMOS pull-down current. Therefore, a weaker PMOS current is not automatically a design failure; it becomes a sizing problem at the circuit level. In this work, the inverter simulation accounts for this issue by using a PMOS area factor, which represents PMOS width scaling in Sentaurus Device. This width-scaling correction is important because it directly affects the inverter switching point, voltage-transfer curve, and PMOS/NMOS drive-current balance.

III. Device Design Strategy

A. Design Constraints and Tradeoffs

The device design was constrained by the need to meet 19 nm-class high-performance logic targets while maintaining a physically reasonable planar CMOS process. Electrically, the design must balance low off-state leakage, sufficient saturation drive current, controlled threshold voltage, acceptable subthreshold swing, and reduced DIBL. These goals compete with one another because stronger channel or halo doping can improve leakage and threshold-voltage control, but excessive doping can also reduce carrier mobility, increase impurity scattering, and lower $I_{D,\mathrm{sat}}$. Similarly, a thinner effective oxide thickness improves gate control and drive current, but the physical gate dielectric must remain realistic enough to avoid excessive tunneling and process sensitivity. From a process standpoint, the source/drain junctions must be shallow, the LDD regions must reduce high-field effects near the drain, and the halo implants must be placed carefully so that they improve electrostatic control without unnecessarily degrading mobility. These choices also affect manufacturability and sustainability because more aggressive implant engineering, high-k integration, and tight nanoscale process control can improve transistor performance but increase fabrication complexity, thermal budget, and process variability [2], [4]–[6].

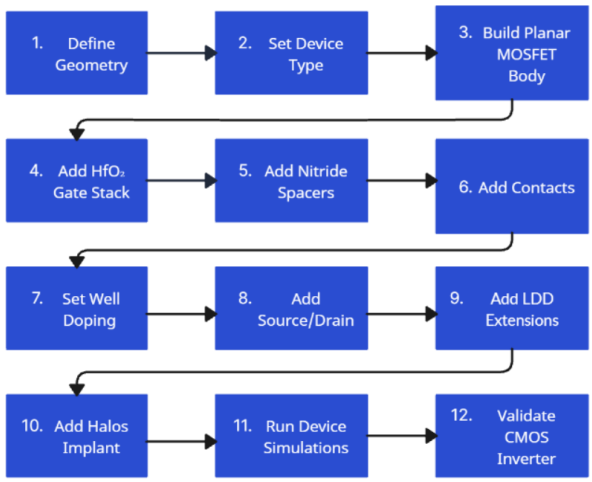


Fig. 3: Design roadmap for the 19 nm CMOS devices. The design begins with a planar MOSFET structure and uses high-k gate-stack engineering, shallow source/drain regions, LDD extensions, halo implants, and TCAD validation to balance leakage, drive current, threshold control, and manufacturability.

B. Chosen Device Architecture

The selected device architecture is a planar bulk CMOS structure with complementary NMOS and PMOS devices designed using the same parameterized geometry. Each device includes a silicon body, an HfO_2 high-k gate dielectric, nitride sidewall spacers, shallow source/drain regions, LDD extensions, halo implants, source/drain contacts, a gate contact, and a substrate contact. The NMOS device uses a p-type body with n-type source/drain regions, while the PMOS device uses an n-type body with p-type source/drain regions. Using a shared geometry for both devices allows the NMOS and PMOS behavior to be compared directly, so differences in current, threshold voltage, and leakage can be attributed mainly to dopant polarity, carrier type, and mobility rather than to unrelated layout differences [3].

A planar MOSFET design was chosen because it is simple, well understood, and directly connected to the 20 nm-class planar bulk CMOS technologies used as references for this project [4]–[6]. However, the planar geometry also has important limitations at a 19 nm gate length. Unlike FinFET or gate-all-around structures, a planar device has weaker electrostatic control because the gate controls the channel primarily from the top surface. Therefore, additional design features are required to reduce short-channel effects, including a thin equivalent oxide thickness, high-k gate stack, shallow junctions, LDD extensions, and halo implants. In this design, these features are used together to balance leakage current, threshold-voltage control, subthreshold swing, DIBL, and saturation drive current.

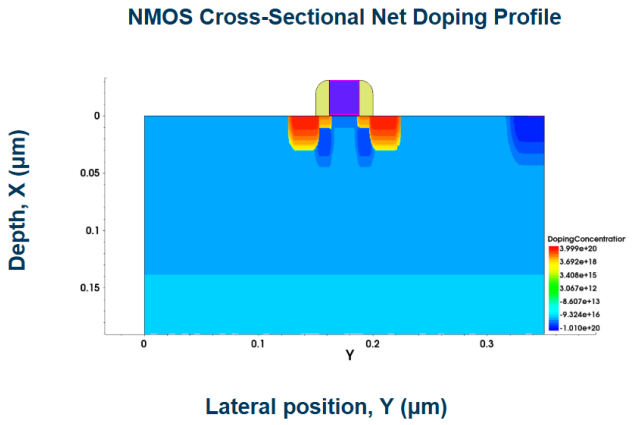


Fig. 4: Cross-sectional net doping profile of the simulated NMOS device. The structure uses a planar silicon body, HfO_2 gate dielectric, nitride sidewall spacers, n-type source/drain regions, LDD extensions, halo implants, and substrate contact.

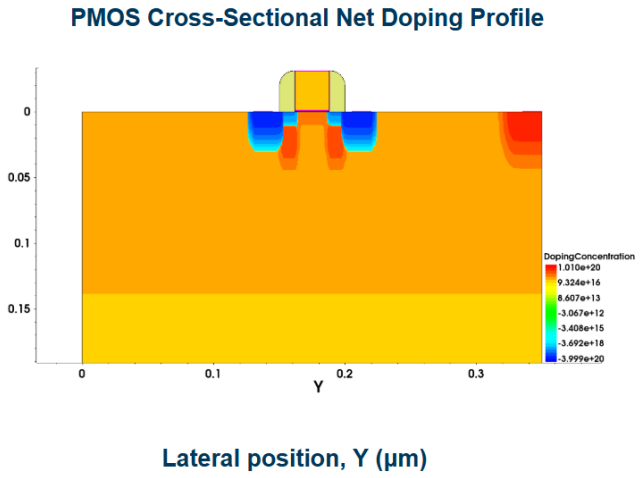


Fig. 5: Cross-sectional net doping profile of the simulated PMOS device. The structure mirrors the NMOS geometry but uses opposite dopant polarity to form a complementary p-channel device.

C. Gate Stack, Gate Material, and Work Function

The gate stack was treated as a high-k/metal-gate style structure in the electrical simulation rather than as a conventional doped polysilicon gate. In the Sentaurus structure, the gate dielectric region was defined using HfO_2, while the electrical gate behavior was controlled in Sentaurus Device by assigning gate work functions instead of relying on a polysilicon doping profile. This distinction is important because the gate work function is one of the main variables that determines the threshold voltage of a scaled MOSFET. Explicitly defining the work function also avoids ambiguity in interpreting the gate as n-type or p-type polysilicon for both devices [3].

Different work functions were assigned to the NMOS and PMOS gates to support complementary threshold-voltage control. The NMOS gate work function was set to 4.5 eV, while the PMOS gate work function was set to 5.1 eV. These values are consistent with the use of separate gate work functions in high-k/metal-gate CMOS technology, where the gate material is selected or tuned to achieve appropriate NMOS and PMOS threshold voltages [4], [5]. In this project, the work-function settings act together with channel doping, halo doping, and the high-k dielectric to determine the final threshold voltage, leakage behavior, and drive-current performance of the simulated 19 nm devices.

IV. Process Flow and Doping Profile Design

A. CMOS Process Flow

The simulated CMOS process flow was designed to capture the main structural features needed for a 19 nm-class planar bulk MOSFET while remaining simple enough for stable TCAD simulation. The process begins with a silicon substrate and well definition, where the NMOS body is p-type and the PMOS body is n-type. After the body region is defined, the gate stack is formed using an HfO_2 high-k dielectric, followed by nitride spacer formation near the gate edges. The source/drain regions, LDD extensions, and halo implants are then introduced to control series resistance, electric-field distribution, and short-channel behavior. Finally, source, drain, gate, and substrate contacts are assigned, and the active device region is locally refined with a fine mesh to resolve the steep doping gradients near the gate and junctions [3].

This process flow should be interpreted as a TCAD process/design abstraction rather than a complete fabrication recipe with every lithography, deposition, etch, implant, and anneal step explicitly modeled. Its purpose is to define a physically meaningful device structure that can be used to study the electrical tradeoffs of scaled CMOS operation. The main process-design challenge is that the same features that improve electrostatic control can also reduce current drive or increase process sensitivity. For example, shallow source/drain junctions and LDD regions help suppress short-channel effects, while halo implants help control leakage and threshold roll-off. However, these regions must be carefully tuned because excessive doping near the channel can reduce mobility, increase threshold voltage, and lower the final saturation current [2], [4]–[6].

B. Source/Drain and LDD Profiles

The source/drain and LDD regions were designed to provide low-resistance carrier injection while limiting high-field effects near the channel. In the NMOS device, arsenic was used for the source/drain and LDD profiles, while the PMOS device uses the complementary p-type dopant profile. The highly doped source/drain regions reduce parasitic series resistance and improve the ability of the transistor to deliver current in the on state. In contrast, the LDD extensions use a lower doping concentration near the channel edge to smooth the electric field between the channel and the heavily doped drain. This reduces the abruptness of the drain-side junction and helps limit leakage and drain-induced barrier lowering without completely sacrificing drive current [3].

Fig. 6 shows the NMOS source/drain and LDD arsenic active doping profile. The plotted region is limited to the near-surface active region, following the requested correction that the depth axis should focus only on the region where the doping profile changes significantly. The profile shows a higher source/drain doping level and a lower LDD level, illustrating the intended separation between the low-resistance contact regions and the more lightly doped extension regions near the channel. This profile is useful because it connects the process recipe to the device-level electrical behavior: higher source/drain doping improves current injection, while the lower-doped LDD extension helps reduce high-field degradation and short-channel leakage.

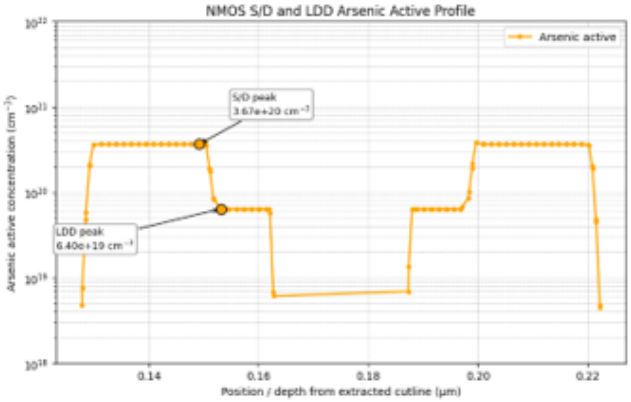


Fig. 6: NMOS S/D and LDD arsenic active profile. The highly doped source/drain region reduces series resistance, while the lower-doped LDD extension smooths the electric field near the channel edge.

C. Channel and Halo Doping Profiles

The channel and halo doping profiles were used to control the threshold voltage and suppress short-channel effects in the 19 nm NMOS and PMOS devices. The channel/body doping helps set the baseline threshold voltage by controlling the barrier that must be overcome to form an inversion channel. In the NMOS device, the body is p-type and the halo implant uses boron near the source/drain edges, while the source/drain extension uses arsenic. As shown in Fig. 7, the LDD profile is concentrated near the surface and decays rapidly with depth, while the halo profile increases the local body doping near the gate edge. This local increase in body doping helps reduce threshold-voltage roll-off, DIBL, and off-state leakage by strengthening electrostatic control where the drain field most strongly affects the channel barrier [2], [3].

The halo implant also introduces an important design trade-off. Stronger halo doping can improve leakage control and subthreshold swing by increasing the local channel barrier, but excessive halo concentration near the oxide–silicon interface can increase impurity scattering, raise the threshold voltage, and reduce the final saturation drive current. Therefore, the halo implant cannot be treated only as a short-channel-effect correction; it must be tuned together with the channel doping, LDD profile, and source/drain junction design. To address this sensitivity quantitatively, the NMOS and PMOS halo-doping sweeps are presented later in Section VI, where the effect of halo concentration on threshold voltage, leakage current, subthreshold swing, and $I_{D,\mathrm{sat}}$ is compared directly.

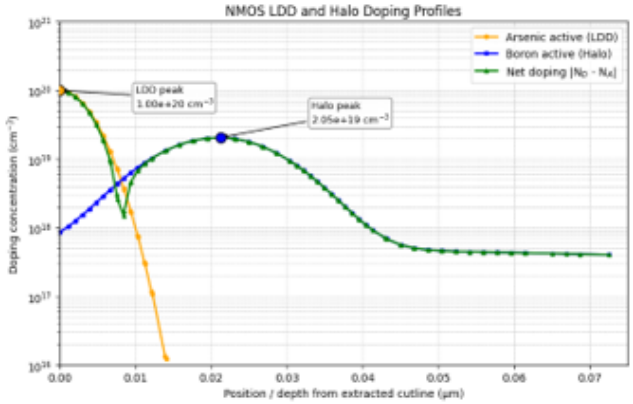


Fig. 7: NMOS LDD and halo doping profiles. The LDD profile controls the source/drain extension behavior, while the halo profile increases local body doping near the gate edge to improve short-channel control.

V. TCAD Simulation Methodology

A. Simulation Tools and Physical Models

The device geometry, doping profiles, contacts, and mesh were generated using Sentaurus Structure Editor, while the electrical characteristics were simulated using Sentaurus Device and post-processed using Sentaurus Visual. The same parameterized structure was used for both NMOS and PMOS devices by changing the device-type variable in the simulation setup. This allowed the same planar geometry, gate length, spacer geometry, and contact layout to be evaluated for both dopant polarities. The simulated structure included the silicon body, HfO_2 gate dielectric, nitride sidewall spacers, source/drain contacts, well doping, source/drain profiles, LDD extensions, halo implants, and substrate contact. A fine active-region mesh was used near the gate and junctions to resolve steep doping gradients and strong electric-field variations at the 19 nm scale [3].

The Sentaurus Device simulations used physical models appropriate for heavily doped, short-channel MOSFETs. Quantum potential correction was included to account for quantum confinement effects near the gate oxide interface. OldSlotboom bandgap narrowing was used because the source/drain and extension regions contain high active dopant concentrations. Mobility was modeled using doping-dependent mobility, normal-field mobility degradation, and high-field saturation to capture impurity scattering, surface-field effects, and carrier velocity saturation. Shockley–Read–Hall recombination with doping dependence and Auger recombination were also included. The final simulation did not use a full hydrodynamic or self-heating

model, so the results should be interpreted as drift-diffusion-based TCAD predictions with quantum and mobility corrections rather than a complete hot-carrier or thermal transport model [3].

TABLE II: Physical models included in the Sentaurus Device simulations.

Model	Purpose
Quantum potential	Accounts for near-interface quantum confinement
OldSlotboom BGN	Models bandgap narrowing in heavily doped regions
Doping-dependent mobility	Captures impurity-scattering mobility reduction
Normal-field mobility degradation	Models surface-field mobility degradation
High-field saturation	Captures velocity saturation at large electric fields
SRH recombination	Models trap-assisted recombination/generation
Auger recombination	Models high-carrier-concentration recombination

B. Bias Conditions and Required Sweeps

The transistor-level simulations were chosen to match the required project characterization conditions. For transfer characteristics, I_D–V_G curves were simulated at both low drain bias and high drain bias. The NMOS device was swept with $V_D = +50$ mV for the linear-region transfer curve and $V_D = +V_{DD}$ for the high-field transfer curve, while the PMOS device used the corresponding negative biases, $V_D = -50$ mV and $V_D = -V_{DD}$. The gate voltage was swept from the off state to the supply voltage for NMOS and from the off state to the negative supply voltage for PMOS. These two transfer curves were needed to extract leakage current, threshold voltage, subthreshold swing, transconductance, and DIBL.

Output characteristics were simulated by sweeping V_D while holding the gate voltage at several fixed values. For the NMOS device, V_G was swept from 0.26 V to V_{DD} in $+0.2$ V steps, and V_D was swept from 0 to V_{DD}. For the PMOS device, the corresponding negative gate biases were used, from -0.26 V to $-V_{DD}$ in -0.2 V steps, while V_D was swept from 0 to $-V_{DD}$. These output curves were used to verify saturation behavior and compare drive current between the NMOS and PMOS devices. At the circuit level, the NMOS and PMOS devices were connected in a CMOS inverter configuration and the voltage-transfer characteristic was simulated at $V_{DD} - 0.5$ V, $V_{DD} - 0.2$ V, and V_{DD} to evaluate logic-level switching and PMOS/NMOS balance.

C. Parameter Extraction Methods

The device parameters were extracted from the simulated I_D–V_G and I_D–V_D curves using consistent definitions for NMOS and PMOS. For PMOS, current and voltage magnitudes were reported using absolute values so that the PMOS curves could be directly compared with the NMOS curves. The off-state current, I_{off}, was extracted from the drain current at the off-state gate bias. The saturation current, $I_{D,\mathrm{sat}}$, was extracted at the high-field on-state condition, where $|V_G| = |V_D| = V_{DD}$. The transconductance was calculated from the slope of the transfer curve,

$$g_m = \frac{dI_D}{dV_G}, \tag{1}$$

and was used to identify the gate-bias region where the drain current is most sensitive to gate control.

The threshold voltage, V_T, was extracted using a constant-current method and, where appropriate, checked against the maximum-g_m behavior. In the constant-current method, V_T is defined as the gate voltage at which the drain current reaches a selected reference current. The subthreshold swing was extracted from the inverse slope of the logarithmic transfer curve in the subthreshold region,

$$SS = \left(\frac{d \log_{10}(I_D)}{dV_G} \right)^{-1}, \tag{2}$$

and reported in mV/dec. DIBL was calculated from the shift in threshold voltage between low and high drain bias,

$$\mathrm{DIBL} = \frac{V_{T,\mathrm{low}\,V_D} - V_{T,\mathrm{high}\,V_D}}{|V_{D,\mathrm{high}} - V_{D,\mathrm{low}}|}. \tag{3}$$

These extraction methods were applied to the final NMOS and PMOS devices as well as to the sensitivity studies in Section VI, including the halo-doping and channel-doping sweeps.

TABLE III: Bias conditions used for the required TCAD sweeps.

Simulation	NMOS Biases	PMOS Biases
I_D–V_G, low V_D	$V_D = +50$ mV	$V_D = -50$ mV
I_D–V_G, high V_D	$V_D = +V_{DD}$	$V_D = -V_{DD}$
I_D–V_D	$V_G = 0.26$ V to V_{DD} in $+0.2$ V steps	$V_G = -0.26$ V to $-V_{DD}$ in -0.2 V steps
Inverter VTC	V_{out}–V_{in} at $V_{DD} - 0.5$ V, $V_{DD} - 0.2$ V, and V_{DD}	

TABLE IV: Extracted device parameters and extraction definitions.

Parameter	Extraction Definition
I_{off}	I_D at the off-state gate bias
$I_{D,\mathrm{sat}}$	I_D at $\|V_G\| = \|V_D\| = V_{DD}$
V_T	Gate voltage at constant-current criterion
SS	Inverse slope of log-scale subthreshold region
DIBL	Threshold-voltage shift from low to high drain bias
g_m	Numerical derivative dI_D/dV_G

VI. Results and Discussion

A. Overview of Final Device Geometry and Doping Recipe

The final NMOS and PMOS devices use the planar bulk geometry described in Section III, with the NMOS and PMOS cross sections shown previously in Fig. 4 and Fig. 5. Both devices use the same overall layout, including the high-k gate stack, nitride spacers, source/drain contacts, LDD extensions, halo implants, and substrate contact. The main difference

between the two devices is the dopant polarity: the NMOS uses n-type source/drain and extension regions in a p-type body, while the PMOS uses p-type source/drain and extension regions in an n-type body. This shared geometry allows the electrical differences between the devices to be interpreted primarily in terms of carrier type, mobility, threshold control, and dopant-profile tuning rather than differences in physical layout.

The final doping recipe was selected to balance series resistance, leakage suppression, threshold-voltage control, and drive-current preservation. Fig. 8 shows the final NMOS source/drain doping profile, where the high arsenic concentration near the surface supports low-resistance carrier injection, while the boron background sets the body/channel doping. The final NMOS and PMOS doping parameters are summarized in Tables V and VI. These tables also define the final recipe used for later electrical comparisons, including the LDD, source/drain, halo, and body-contact profiles.

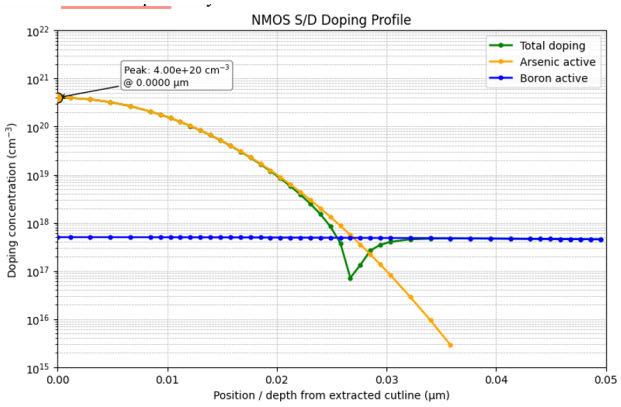


Fig. 8: Final NMOS source/drain doping profile used in the revised device design. The source/drain arsenic profile reaches a high near-surface concentration to reduce series resistance, while the boron background defines the p-type body.

TABLE V: Summary of final NMOS doping profile parameters.

Region	Dopant	Concentration	Details
Extension/LDD	As	Peak 1×10^{20}; at-depth 1×10^{18}	0.015
Source/Drain	As	Peak 4×10^{20}; at-depth 1×10^{19}	0.025
Halo	B	Peak 2×10^{19}; at-depth 1×10^{17}	0.045
Body contact	B	Peak 1×10^{20}; at-depth 1×10^{17}	0.050

TABLE VI: Summary of final PMOS doping profile parameters.

Region	Dopant	Concentration	Details
Extension/LDD	B	Peak 1×10^{20}; at-depth 1×10^{18}	0.015
Source/Drain	B	Peak 4×10^{20}; at-depth 1×10^{19}	0.025
Halo	As	Peak 7×10^{18}; at-depth 1×10^{17}	0.045
Body contact	As	Peak 1×10^{20}; at-depth 1×10^{17}	0.050

B. High-k Gate Stack and EOT Comparison

The gate stack was evaluated by comparing a SiO_2-only gate dielectric against a combined SiO_2 + HfO_2 high-k stack. The motivation for using HfO_2 is shown in Fig. 9, where the high-k stack provides an equivalent oxide thickness near 0.7 nm while maintaining a larger physical dielectric thickness than an ultrathin SiO_2 layer. This distinction is important at the 19 nm scale because a small EOT improves gate control and inversion charge, while a larger physical thickness is more realistic for suppressing direct tunneling and maintaining process feasibility. Therefore, the high-k stack was used to increase the effective gate capacitance without relying only on an unrealistically thin SiO_2 dielectric.

Fig. 10 compares the simulated NMOS I_D–V_G behavior for the SiO_2-only and SiO_2 + HfO_2 gate stacks. The high-k case produces a larger drain current over most of the gate-voltage sweep, showing that the improved gate capacitance strengthens channel inversion and increases drive current. As summarized in Table VII, the NMOS saturation current increased from 1167 μA/μm for the SiO_2-only case to 1743 μA/μm for the high-k case, while the off-state current increased from 41.6 nA/μm to 75.4 nA/μm. This result shows the expected tradeoff: the high-k stack improves drive current and gate control, but the stronger inversion behavior can also increase leakage. These values correspond to the high-k comparison study and are used here to justify the gate-stack choice before discussing later structural correction and final-device extraction.

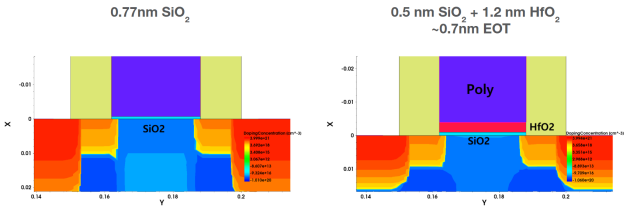


Fig. 9: Gate-stack comparison between a 0.77 nm SiO_2 dielectric and a combined 0.5 nm SiO_2 + 1.2 nm HfO_2 stack with an equivalent oxide thickness near 0.7 nm.

TABLE VII: Effect of high-k gate stack on NMOS performance at $V_D = 0.85$ V.

Gate Stack	$I_{D,\mathrm{sat}}$ (μA/μm)	I_{off} (nA/μm)
SiO_2 only	1167	41.6
SiO_2 + HfO_2	1743	75.4

C. Structural Correction and Revised NMOS Design

The NMOS design was revised after two issues were identified in the presentation-stage structure. First, the gate dielectric thickness generated in the SDE structure did not match the nominal gate-stack dimensions used in the design assumptions, which produced an equivalent oxide thickness smaller than

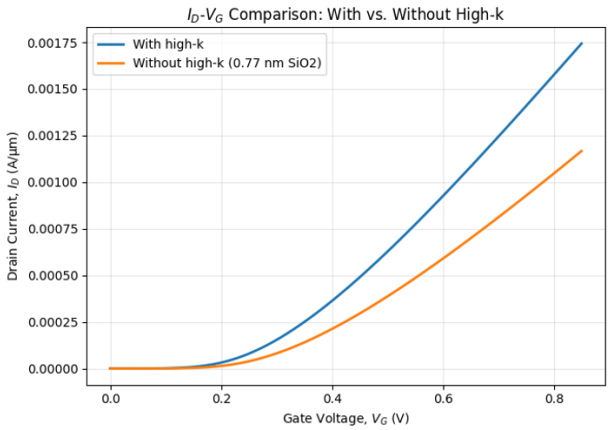


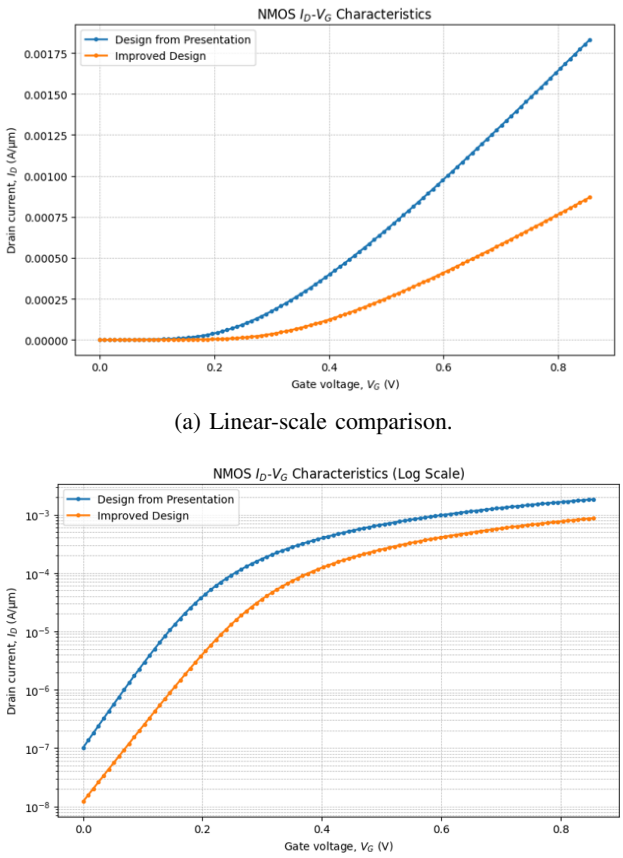
Fig. 10: NMOS I_D–V_G comparison between the SiO_2-only gate stack and the SiO_2 + HfO_2 high-k gate stack.

the intended target. Second, the original source/drain doping concentration was unrealistically high, which artificially reduced series resistance and overestimated the drive current. To obtain a more physically reasonable device, the gate-stack thickness was corrected to satisfy the intended EOT requirement, and the source/drain doping concentration was reduced to a more realistic range. As shown in Fig. 11, this correction reduced the apparent NMOS drive current compared with the presentation-stage design, from approximately 1700 μA/μm to approximately 750 μA/μm. Although this reduced the extracted saturation current, the revised structure provides a more realistic representation of device behavior because it avoids relying on artificially aggressive dielectric scaling and excessive source/drain doping.

After the structural correction, the NMOS was further optimized through a sequence of doping adjustments, as shown in Fig. 12. The corrected baseline design used an EOT near the target value and reduced the peak source/drain concentration from approximately 1×10^{21} cm^{-3} to approximately 1×10^{20} cm^{-3}, but this produced a lower saturation current and a larger apparent threshold voltage. To improve turn-on behavior, the p-well and channel doping concentrations were reduced, which lowered the threshold voltage and increased the drain current, although the leakage current also moved closer to the design limit. Finally, the source/drain doping concentration was increased from 1×10^{20} cm^{-3} to 4×10^{20} cm^{-3} to reduce parasitic series resistance and improve carrier injection. This final adjustment increased the saturation current from approximately 1050 μA/μm to approximately 1110 μA/μm while preserving the improved turn-on behavior from the lower-channel-doping design.

D. NMOS Halo Doping Sensitivity

The NMOS halo implant was varied to quantify how strongly the near-junction body doping affects threshold voltage, leakage, subthreshold swing, and drive current. Fig. 13 shows the NMOS I_D–V_G curves for halo concentrations of 1.0×10^{19}, 2.0×10^{19}, and 3.0×10^{19} cm^{-3}. Using the



(a) Linear-scale comparison.

(b) Log-scale comparison.

Fig. 11: NMOS I_D–V_G comparison before and after structural correction. The revised device corrects the gate dielectric thickness/EOT mismatch and uses more realistic source/drain doping.

constant-current extraction criterion of $I_{D,\mathrm{CC}} = 4.5 \times 10^{-5}$ A/μm, the extracted threshold voltage increases from 0.175 V to 0.241 V as the halo concentration increases, as summarized in Table VIII. This confirms that the halo implant is not a minor process detail; it directly changes the effective source-channel barrier and therefore shifts the gate voltage required to turn on the NMOS device.

The halo sweep also shows the main leakage–drive-current tradeoff. Lower halo doping gives the highest saturation current because the channel barrier is lower and carrier mobility is less degraded by ionized impurity scattering. However, the 1.0×10^{19} cm^{-3} case produces an excessive leakage current of 1210 nA/μm and the weakest subthreshold swing of 89.8 mV/dec, as shown in Table IX. Increasing the halo concentration to 3.0×10^{19} cm^{-3} lowers leakage to 123 nA/μm and improves SS to 79.2 mV/dec, but reduces $I_{D,\mathrm{sat}}$ to 1150 μA/μm. Therefore, stronger halo doping improves electrostatic control but reduces drive current, which directly supports the need to tune the halo implant rather than simply maximize it.

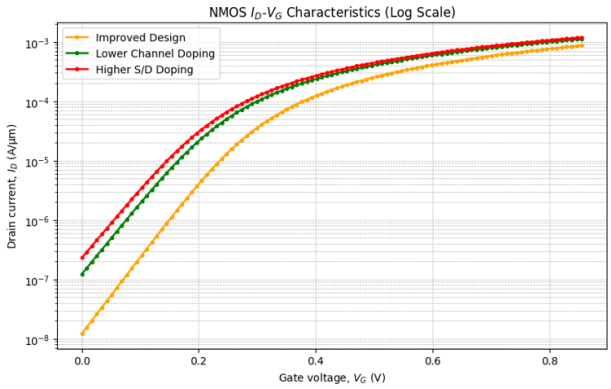


Fig. 12: NMOS design-development comparison showing the corrected baseline design, lower-channel-doping design, and higher-source/drain-doping design.

TABLE VIII: NMOS halo doping sensitivity using constant-current threshold-voltage extraction.

Halo Doping (cm^{-3})	V_T **(V)**
1.0×10^{19}	0.175
2.0×10^{19}	0.222
3.0×10^{19}	0.241

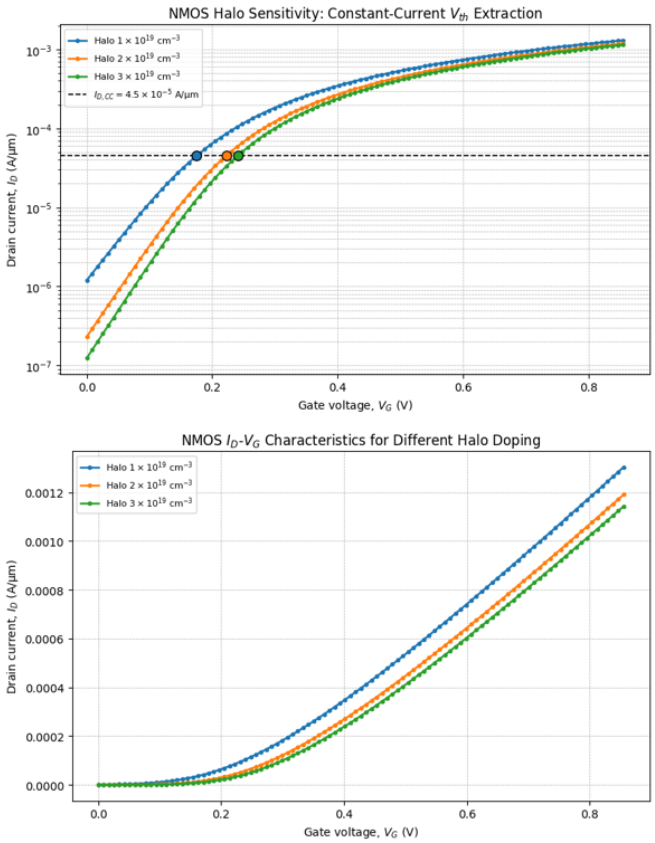


Fig. 13: NMOS I_D–V_G characteristics for different halo doping concentrations. The constant-current method is used to compare threshold-voltage sensitivity, while the linear-scale curve shows the drive-current penalty from stronger halo doping.

E. PMOS Halo Doping Sensitivity

The PMOS halo implant was evaluated separately because the PMOS device could not be optimized by directly mirroring the NMOS doping strategy. Fig. 14 shows the PMOS $|I_D|$–V_G characteristics for halo concentrations between 7.0×10^{18} and 1.0×10^{19} cm^{-3}. The constant-current extraction shows that increasing the halo concentration increases the magnitude of the PMOS threshold voltage: V_T shifts from -0.452 V at 7.0×10^{18} cm^{-3} to -0.533 V at 1.0×10^{19} cm^{-3}, as summarized in Table X. This means that stronger PMOS halo doping improves barrier control but also makes the device harder to turn on at the available supply voltage.

The PMOS results show the same general tradeoff as the NMOS case, but with a stronger concern about drive-current loss because hole mobility is lower than electron mobility. Reducing the PMOS halo concentration lowers the magnitude of V_T and improves the on-current, while increasing the halo concentration improves leakage and subthreshold swing. The presentation-stage PMOS tradeoff data in Table XI show this behavior clearly: increasing halo doping from 1.0×10^{19} to 2.0×10^{19} cm^{-3} reduces I_{off} from 6.75 nA/μm to 0.0215 nA/μm and improves SS from 102.7 mV/dec to 85 mV/dec, but lowers $I_{D,\text{sat}}$ from 699 to 541 μA/μm. Therefore, the PMOS halo implant was reduced relative to the NMOS case to improve PMOS turn-on and drive current while maintaining acceptable leakage control.

‘‘‘

TABLE IX: NMOS halo doping tradeoff summary.

Halo Doping (cm^{-3})	I_{off} **(nA/μm)**	$I_{D,\text{sat}}$ **(μA/μm)**	**SS (mV/dec)**
1.0×10^{19}	1210	1300	89.8
2.0×10^{19}	231	1190	83.3
3.0×10^{19}	123	1150	79.2

F. Channel Doping Sensitivity

The effect of NMOS channel doping was evaluated by comparing the log-scale I_D–V_G characteristics for channel doping concentrations of 1.5×10^{18}, 2.5×10^{18}, and 3.5×10^{18} cm^{-3}. As shown in Fig. 15, increasing the channel doping shifts the transfer curve downward in the subthreshold region, indicating improved off-state electrostatic control. This trend is quantified in Table XII: as N_A increases from 1.5×10^{18} to 3.5×10^{18} cm^{-3}, I_{off} decreases from 137.0 nA/μm to 75.4 nA/μm. This reduction occurs because higher channel doping increases the source-channel barrier and makes it harder for carriers to flow when the device is nominally off.

The improved leakage control comes with a drive-current penalty. Over the same doping range, $I_{D,\text{sat}}$ decreases from

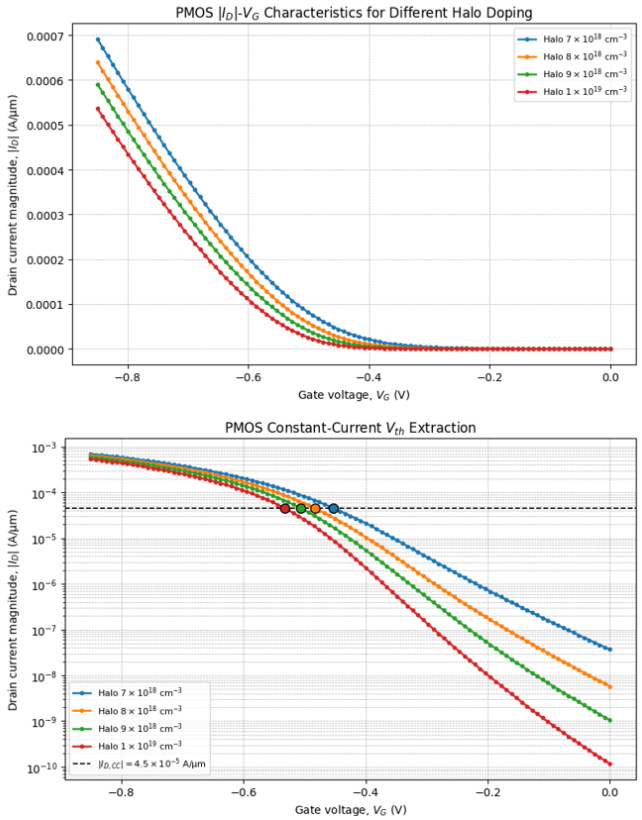


Fig. 14: PMOS I_D–V_G characteristics for different halo doping concentrations. PMOS drain current is plotted using magnitude so that threshold-voltage shift and drive-current trends can be compared directly.

TABLE X: PMOS halo doping sensitivity using constant-current threshold-voltage extraction.

Halo Doping (cm^{-3})	V_T **(V)**
1.0×10^{19}	-0.533
9.0×10^{18}	-0.507
8.0×10^{18}	-0.483
7.0×10^{18}	-0.452

1900 μA/μm to 1740 μA/μm. This trend is expected because heavier channel doping increases ionized-impurity scattering, reduces carrier mobility, and raises the gate voltage needed to reach strong inversion. Therefore, lower channel doping improves turn-on behavior and saturation current, but it also increases leakage toward the design limit. The final channel/body doping was selected as a compromise between maintaining acceptable off-state leakage and preserving high drive current.

G. I_D–V_G Transfer Characteristics and Extracted Subthreshold Parameters

The final high-drain-bias transfer characteristics were used to extract the main subthreshold and turn-on parameters for the NMOS and PMOS devices. Fig. 16 shows the NMOS and

TABLE XI: PMOS halo doping tradeoff summary from the presentation-stage device.

Halo Doping (cm^{-3})	$I_{D,\mathrm{sat}}$ **(μA/μm)**	I_{off} **(nA/μm)**	**SS (mV/dec)**
1.0×10^{19}	699	6.75	102.7
1.5×10^{19}	602	0.147	98
2.0×10^{19}	541	0.0215	85

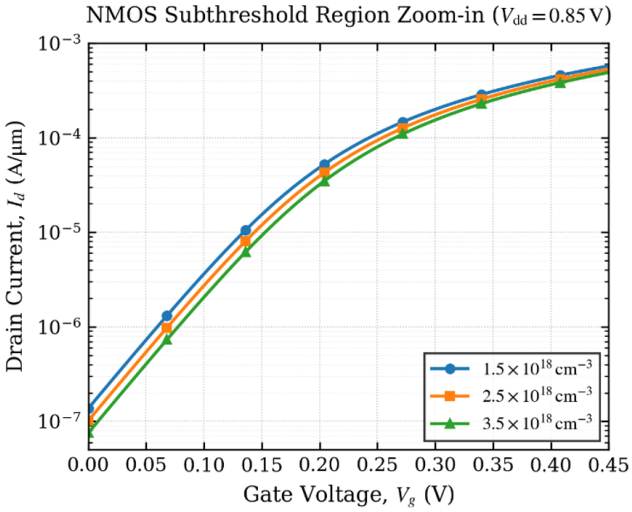


Fig. 15: NMOS log-scale I_D–V_G characteristics for different channel doping concentrations. Lower channel doping increases drive current but also increases off-state leakage.

PMOS I_D–V_G characteristics at $|V_D| = 0.85$ V. The NMOS curve is plotted directly under positive gate bias, while the PMOS curve is plotted using absolute current and absolute gate-voltage magnitude so the p-channel and n-channel devices can be compared on the same basis. The NMOS device reaches an on-current of approximately 1750 μA/μm and has an extracted $V_{T,\mathrm{sat}}$ of 0.3221 V with a subthreshold swing of 68.3 mV/dec. The PMOS device reaches approximately 700 μA/μm, with $|V_{T,\mathrm{sat}}| \approx 0.479$ V and SS ≈ 102.7 mV/dec.

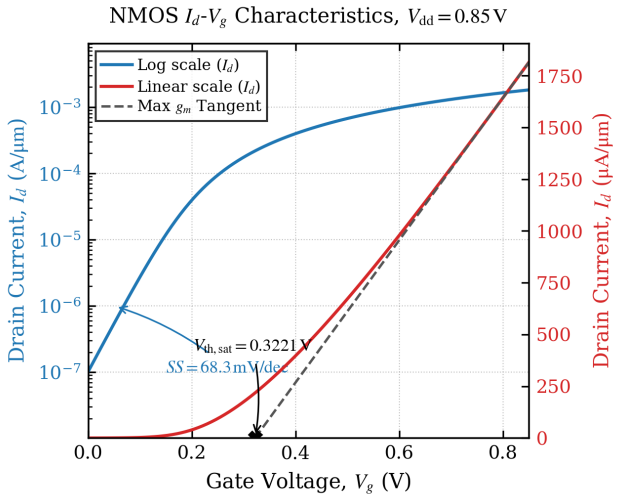
These transfer curves show that both devices turn on properly at the target supply voltage, but they also show the expected NMOS/PMOS imbalance. The NMOS has stronger drive current and sharper subthreshold behavior, while the PMOS has lower drive current and a larger threshold-voltage magnitude. This difference is consistent with lower hole mobility and the more difficult PMOS tuning observed in the halo-sensitivity study. The extracted quantities in Table XIII are used later in the ITRS comparison table to evaluate whether the final devices meet the leakage, threshold, subthreshold swing, and drive-current goals.

H. Drain-Induced Barrier Lowering Extraction

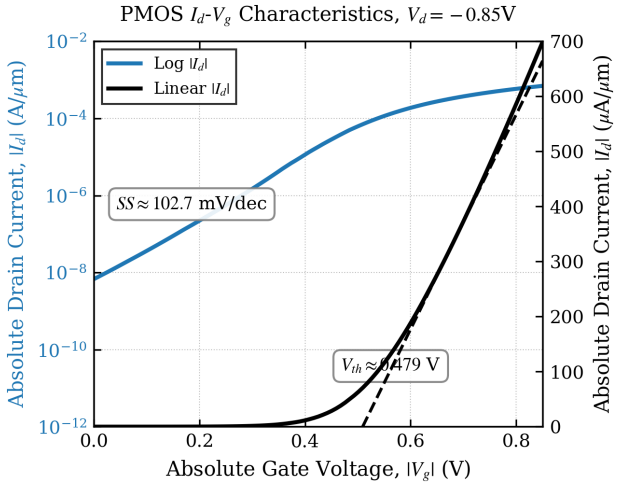
Drain-induced barrier lowering was extracted from the shift in threshold voltage between the low-drain-bias and high-drain-bias I_D–V_G curves. Fig. 17 shows the NMOS and PMOS DIBL extraction using a constant-current criterion of

TABLE XII: NMOS channel doping sensitivity at $V_D = 0.85$ V.

N_A (cm^{-3})	I_{off} (nA/μm)	$I_{D,\text{sat}}$ (μA/μm)
1.5×10^{18}	137.0	1900
2.5×10^{18}	101.4	1810
3.5×10^{18}	75.4	1740



(a) NMOS transfer characteristics at $V_D = 0.85$ V.



(b) PMOS transfer characteristics at $V_D = -0.85$ V, plotted using current and voltage magnitudes.

Fig. 16: Simulated I_D–V_G transfer characteristics for the final NMOS and PMOS devices at high drain bias.

$I_{D,\text{CC}} = 4.5 \times 10^{-5}$ A/μm. For the NMOS device, increasing the drain bias from $V_D = 0.05$ V to $V_D = 0.85$ V shifts the threshold point to a lower gate voltage, giving a DIBL value of 92.7 mV/V. Since the drain-bias difference is 0.80 V, this corresponds to an approximate threshold-voltage shift of 74 mV. This behavior is expected in a 19 nm planar MOSFET because the higher drain voltage lowers the source-channel barrier and makes the device easier to turn on.

TABLE XIII: Extracted transfer-curve parameters from the final high-drain-bias I_D–V_G characteristics.

Metric	NMOS	PMOS
$I_{D,\text{sat}}$	1750 μA/μm	700 μA/μm
I_{off}	75.4 nA/μm	6.75 nA/μm
$V_{T,\text{sat}}$	0.3221 V	0.479 V
SS	68.3 mV/dec	102.7 mV/dec

The PMOS device shows a similar effect under negative drain bias. When the drain bias changes from $V_D = -0.05$ V to $V_D = -0.85$ V, the extracted PMOS threshold point shifts, giving a DIBL value of 102.5 mV/V for the halo condition shown in Fig. 17b. This corresponds to an approximate threshold-voltage shift of 82 mV over the same 0.80 V drain-bias change. The NMOS value remains slightly below the 100 mV/V design target, while the PMOS value is slightly above the target, indicating that the PMOS has weaker electrostatic control in this extraction. These DIBL results support the earlier conclusion that the planar 19 nm design can achieve reasonable short-channel control, but PMOS halo placement and threshold-voltage tuning still require further optimization.

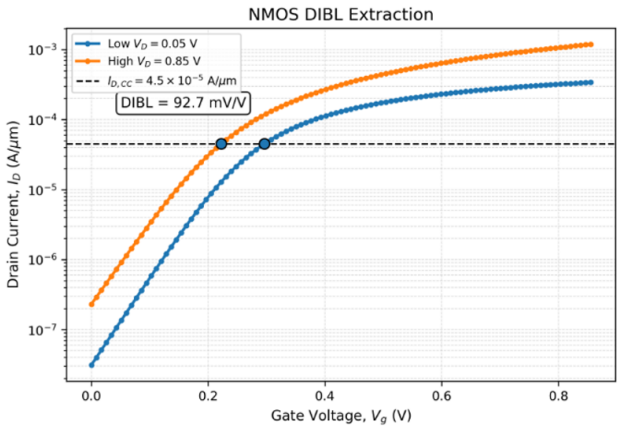
I. I_D–V_D Output Characteristics and Saturation

The output characteristics were used to verify that the final NMOS and PMOS devices show the expected drain-current behavior under multiple gate-bias conditions. Fig. 18 shows the combined I_D–V_D curves for both devices, with NMOS operation plotted for positive V_{DS} and PMOS operation plotted for negative V_{DS}. For the NMOS, the drain current increases rapidly at small V_{DS} and then begins to saturate as the drain voltage approaches the supply voltage. The highest NMOS curve corresponds to the largest gate bias, near $V_{GS} = 0.855$ V, and reaches the largest output current among the simulated devices. The lower NMOS curves at $V_{GS} = 0.26$, 0.46, and 0.66 V show the expected reduction in drain current as the gate overdrive decreases.

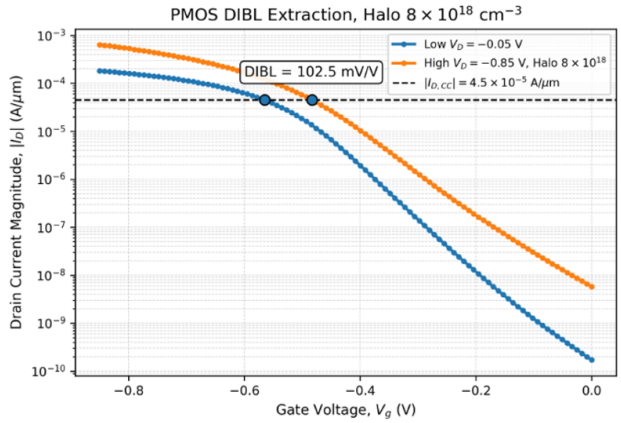
The PMOS output curves show the same qualitative behavior under negative drain and gate bias, but the magnitude of the PMOS current is lower than the NMOS current. At the largest PMOS gate bias, the output current reaches roughly the several-hundred μA/μm range, while the strongest NMOS curve is above the 1 mA/μm range. This drive-current difference is expected because electron mobility is higher than hole mobility in silicon and because the PMOS threshold and halo tuning were more restrictive. Therefore, the I_D–V_D curves confirm both transistor operation and saturation behavior, while also showing the NMOS/PMOS current imbalance that later affects inverter switching and motivates PMOS width scaling.

J. Extracted Parameter Table and ITRS Comparison

Table XIV summarizes the extracted NMOS and PMOS parameters and compares them with the ITRS-inspired high-performance logic targets used in this project. The devices



(a) NMOS DIBL extraction using low- and high-drain-bias I_D–V_G curves.



(b) PMOS DIBL extraction using low- and high-drain-bias $|I_D|$–V_G curves.

Fig. 17: DIBL extraction from low- and high-drain-bias transfer characteristics. The threshold-voltage shift at the constant-current criterion is used to quantify drain-induced barrier lowering.

meet the geometric and bias targets with $L_g \approx 19$ nm and $V_{DD} = 0.85$ V. The high-k gate stack gives an EOT near 0.7 nm, which satisfies the target of 0.77 nm or lower. The leakage results also meet the target: the NMOS has $I_{\text{off}} = 75.4$ nA/μm and the PMOS has $I_{\text{off}} = 6.75$ nA/μm, both below the 100 nA/μm limit. The DIBL values are also acceptable, with 25.8 mV/V for NMOS and 76.4 mV/V for PMOS, both below the 100 mV/V target.

The main deviations from the targets are threshold voltage and PMOS drive current. The extracted threshold voltages, 0.3221 V for NMOS and 0.479 V in magnitude for PMOS, are higher than the approximate 0.200 V target. The NMOS drive current meets or approaches the ITRS target depending on the extraction method, with 1750 μA/μm from the high-bias I_D–V_G extraction and 1666.2 μA/μm from the output-curve saturation result. The PMOS drive current is lower, about 700 μA/μm, which confirms that PMOS mobility and threshold

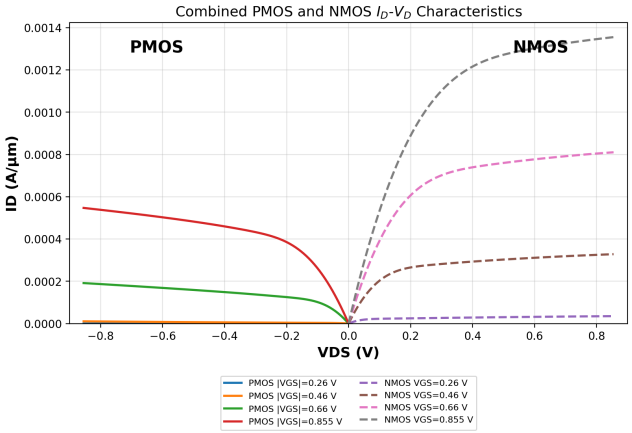


Fig. 18: Simulated I_D–V_D output characteristics for the final 19 nm NMOS and PMOS devices under multiple gate-bias conditions.

control remain the limiting factors in the complementary device pair. Overall, the design demonstrates strong leakage control, good NMOS performance, and acceptable DIBL, but still requires PMOS drive-current improvement and threshold-voltage reduction for better high-performance CMOS balance.

K. CMOS Inverter Voltage Transfer Characteristics

The CMOS inverter simulation was used to verify that the final NMOS and PMOS devices operate together as a logic gate, rather than only as isolated transistors. Fig. 19 shows the inverter voltage-transfer characteristics for three supply voltages: $V_{DD} - 0.5$ V, $V_{DD} - 0.2$ V, and the nominal $V_{DD} = 0.85$ V, corresponding to 0.35 V, 0.65 V, and 0.85 V. In all three cases, the inverter shows the expected logic behavior: when V_{in} is low, the PMOS pull-up device is on and the output remains near the supply voltage; when V_{in} is high, the NMOS pull-down device is on and the output falls close to ground. The sharp transitions in the voltage-transfer curves confirm that the complementary devices can produce valid logic-high and logic-low output levels over the tested supply range.

The switching point shifts with supply voltage and remains influenced by the imbalance between NMOS and PMOS drive strength. From the device-level results, the NMOS provides a significantly larger saturation current than the PMOS, so the pull-down network is stronger than the pull-up network for equal device width. In practical CMOS logic, this is normally corrected by increasing the PMOS width to compensate for lower hole mobility. In this simulation, PMOS width scaling was represented using the SDevice area factor, with an area factor of approximately 4 applied to improve pull-up strength. Even with this tuning, the voltage-transfer curves remain somewhat skewed, showing that PMOS drive current and threshold-voltage balance are still limiting factors. Therefore, the inverter result confirms successful circuit-level switching, while also identifying PMOS width scaling and further PMOS optimization as important future improvements.

TABLE XIV: Extracted device parameters compared with ITRS-inspired high-performance logic targets.

Parameter	ITRS Target	NMOS Result	PMOS Result	Interpretation
L_g	$\sim$19 nm	19 nm	19 nm	Meets geometry target
V_{DD}	0.85 V	0.85 V	0.85 V	Meets bias target
EOT	$\leq$0.77 nm	$\sim$0.7 nm	$\sim$0.7 nm	Meets gate-control target
I_{off}	$\leq$100 nA/μm	75.4 nA/μm	6.75 nA/μm	Meets leakage target
$I_{D,\text{sat}}$ from I_D–V_G	1355 μA/μm	1750 μA/μm	700 μA/μm	NMOS meets; PMOS weaker
$I_{D,\text{sat}}$ from I_D–V_D	1355 μA/μm	1666.2 μA/μm	699.2 μA/μm	Output-curve saturation result
$V_{T,\text{sat}}$	$\sim$0.200 V	0.3221 V	0.479 V	Both higher than target
SS	$<$100 mV/dec	68.3 mV/dec	102.7 mV/dec	NMOS meets; PMOS slightly high
DIBL	$<$100 mV/V	25.8 mV/V	76.4 mV/V	Both meet target
g_m	–	Not consistently extracted	Not consistently extracted	Omitted from final comparison

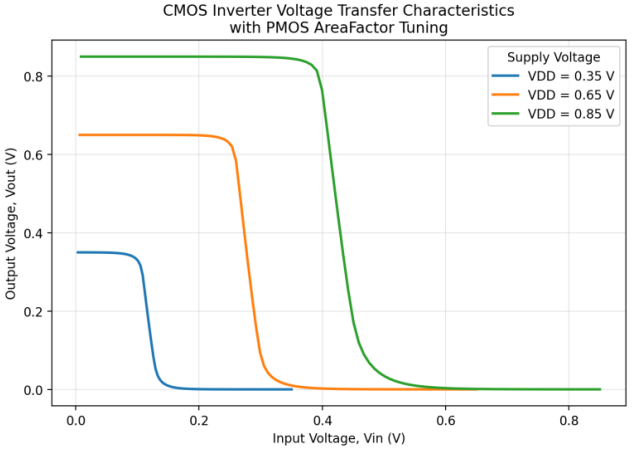


Fig. 19: CMOS inverter voltage-transfer characteristics simulated at $V_{DD} - 0.5$ V, $V_{DD} - 0.2$ V, and V_{DD}. The PMOS area factor is used to partially compensate for weaker PMOS drive current.

L. Summary of Design Successes and Remaining Deviations

The final design successfully demonstrates complementary 19 nm-class NMOS and PMOS operation using a planar bulk MOSFET structure with an HfO_2 high-k gate dielectric, shallow source/drain regions, LDD extensions, halo implants, and work-function-based threshold-voltage tuning. Compared with the earlier presentation-stage design, the revised NMOS structure improved the physical realism of the simulation by correcting the gate-stack/EOT mismatch and reducing unrealistically aggressive source/drain doping. The final devices also achieved several important design goals: the EOT remained near the target value, the NMOS and PMOS leakage currents stayed below the 100 nA/μm target, and the output curves showed proper transistor operation and saturation behavior. The halo and channel doping sweeps further strengthened the design by showing how threshold voltage, leakage, subthreshold swing, and drive current respond to process changes, which directly supports the use of TCAD as an iterative design tool [2]–[6].

The main remaining deviations are threshold-voltage offset, PMOS drive-current weakness, and imperfect NMOS/PMOS balance. The extracted NMOS threshold voltage of approximately 0.322 V and PMOS threshold-voltage magnitude of approximately 0.479 V are both higher than the approximate 0.200 V target, indicating that further gate work-function, channel doping, and halo-placement optimization would be needed. The NMOS drive current meets the high-performance target, but the PMOS drive current remains significantly lower, which is expected from lower hole mobility and the stronger threshold-control tradeoffs in the PMOS device. The DIBL extraction also shows that short-channel control is reasonable but not fully ideal, especially for the PMOS case if the extracted value slightly exceeds the 100 mV/V target. At the circuit level, the inverter voltage-transfer curves confirm functional switching at multiple supply voltages, but the switching point remains skewed because of the NMOS/PMOS current imbalance. Future work should therefore focus on PMOS width scaling through area-factor tuning, strain engineering to improve hole mobility, improved halo placement away from excessive interface doping, contact-resistance modeling, and process-variation studies to make the design more realistic and better balanced for high-performance CMOS logic [3], [8], [10].

VII. Manufacturability, Sustainability, and Limitations

A. Manufacturability and Process Feasibility

The simulated 19 nm CMOS design is based on a planar MOSFET process sequence that is simpler than a FinFET or gate-all-around process, but still requires tight control of nanoscale fabrication steps. As shown in Fig. 20, the process includes gate formation, halo implantation, LDD doping, nitride spacer formation, source/drain implantation, gate replacement, and metal deposition. This sequence is consistent with the design strategy used in the TCAD model, where the HfO_2 gate dielectric, LDD extensions, halo implants, source/drain regions, and contacts were explicitly included. The manufacturability challenge is that each of these steps affects short-channel behavior: shallow source/drain junctions reduce drain-field penetration, LDD regions smooth the electric field near the drain, and halo implants suppress threshold-voltage roll-off and DIBL [2]–[4].

The main process limitation is sensitivity to placement, dose, and physical thickness at the 19 nm scale. The high-k gate stack improves gate control by allowing a low EOT

without requiring an unrealistically thin SiO_2 layer, but high-k/metal-gate integration also requires careful interface control and work-function tuning [5], [6]. Similarly, the halo implant improves electrostatic control only when it is placed correctly near the source/drain edges; if the halo extends too strongly into the oxide–silicon interface region, it can increase impurity scattering, raise threshold voltage, and reduce drive current. Therefore, the design is manufacturable as a physically meaningful TCAD process abstraction, but a real process would still require calibrated implant diffusion, activation annealing, interface-trap modeling, contact-resistance extraction, and process-variation analysis.

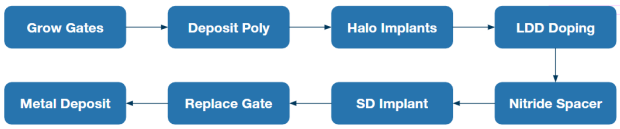


Fig. 20: Simplified planar MOSFET process sequence used to contextualize the simulated 19 nm CMOS structure. The process includes gate formation, halo implantation, LDD doping, nitride spacer formation, source/drain implantation, replacement gate processing, and metal deposition.

B. Sustainability and Energy Efficiency

The energy-efficiency motivation for the design comes from the relationship between transistor scaling, supply voltage, and switching power. In CMOS logic, the dynamic switching power scales approximately as $P_{\mathrm{dyn}} \propto CV_{DD}^2 f$, so lowering the supply voltage has a direct quadratic effect on active power consumption. The project target of $V_{DD} = 0.85$ V therefore supports lower switching energy compared with higher-voltage logic, while the 19 nm gate length supports higher device density for computation. This is important for modern computing systems because data centers, artificial intelligence workloads, mobile systems, and high-performance computing all depend on dense and energy-efficient CMOS technology [1], [2].

However, the sustainability benefit of device scaling is not automatic. Lower V_{DD} and reduced capacitance can improve circuit-level energy efficiency, but advanced fabrication steps can increase process cost, tool complexity, thermal budget, and material usage. In this design, the HfO_2 high-k gate stack, LDD extensions, halo implants, and replacement-gate-style process improve device performance and leakage control, but they also represent additional processing complexity relative to a simpler long-channel MOSFET. Therefore, the final design should be viewed as an energy-efficiency tradeoff: improved leakage control, functional inverter switching, and high NMOS drive current support efficient logic operation, while the remaining PMOS imbalance and fabrication complexity motivate further optimization before the design could be considered process-ready.

C. Modeling Limitations

Although the TCAD setup captures the main physical features of the 19 nm CMOS design, the model remains an idealized device-level representation rather than a complete manufacturing-validated process. The simulated structure uses a planar NMOS/PMOS geometry, which is simpler and easier to compare between complementary devices, but planar MOSFETs have weaker short-channel control than FinFET or gate-all-around architectures at comparable gate lengths. The model includes HfO_2 gate dielectric regions, spacers, source/drain contacts, well doping, LDD extensions, halo implants, and substrate contacts; however, the implant profiles are represented using idealized Gaussian distributions rather than a fully calibrated process sequence with lithography, diffusion, activation, and process-variation effects. As a result, the simulated profiles are useful for comparing design trends, but they do not fully capture random dopant fluctuation, line-edge roughness, implant straggle, annealing variability, or wafer-level process sensitivity [2], [3].

Several transport and interface effects were also simplified. Gate leakage and oxide–semiconductor interface traps were not explicitly modeled, even though these effects can strongly influence leakage, threshold voltage, and subthreshold swing in aggressively scaled high-k/metal-gate devices. The final electrical simulations used drift-diffusion transport with quantum potential correction, bandgap narrowing, mobility degradation, high-field saturation, SRH recombination, and Auger recombination, but did not include full hydrodynamic transport, quasi-ballistic transport, or self-heating. The source/drain and metal contacts were also treated in an idealized way, so contact resistance was not fully extracted as a separate performance limiter. Finally, the CMOS inverter simulation depends on PMOS/NMOS area-factor tuning to compensate for weaker PMOS drive current, so the circuit-level switching results should be interpreted as a functional validation of complementary operation rather than a fully optimized standard-cell design. Future work should therefore include calibrated process simulation, contact-resistance modeling, interface-trap and gate-leakage models, self-heating, process-variation analysis, and more advanced transport models [3], [7], [8], [10]. ‘‘‘

VIII. Conclusion and Future Work

A. Main Conclusions

This project demonstrated the TCAD design and validation of complementary 19 nm-class NMOS and PMOS devices for high-performance CMOS logic. The final devices used a planar bulk MOSFET structure with an HfO_2 high-k gate dielectric, shallow source/drain junctions, LDD extensions, halo implants, and work-function-based threshold-voltage tuning. The high-k gate stack improved the effective gate control and increased the NMOS saturation current from 1167 μA/μm for the SiO_2-only case to 1743 μA/μm for the SiO_2 + HfO_2 case, confirming the importance of EOT reduction in scaled planar CMOS. The final NMOS achieved strong drive-current

performance, with $I_{D,\mathrm{sat}} \approx 1743$–$1750$ μA/μm from the high-bias transfer characteristics and $I_{\mathrm{off}} = 75.4$ nA/μm, satisfying the ITRS-inspired leakage target of 100 nA/μm and exceeding the NMOS drive-current target of 1355 μA/μm [2]–[6].

The final PMOS also operated as a complementary p-channel device, although with weaker drive current than the NMOS. It achieved $I_{D,\mathrm{sat}} \approx 699.2$ μA/μm, $I_{\mathrm{off}} = 6.75$ nA/μm, $|V_{T,\mathrm{sat}}| \approx 0.479$ V, and SS ≈ 102.7 mV/dec. The halo and channel doping sensitivity studies showed that leakage, threshold voltage, subthreshold swing, and drive current could be tuned through implant and body-doping adjustments, which helped justify the final device recipe. The low- and high-drain-bias transfer curves also verified DIBL behavior, while the I_D–V_D curves confirmed output saturation under multiple gate-bias conditions. At the circuit level, the CMOS inverter voltage-transfer curves showed valid logic-high and logic-low behavior at $V_{DD} - 0.5$ V, $V_{DD} - 0.2$ V, and V_{DD}, confirming that the NMOS and PMOS devices function together as a switching pair [3], [8], [10].

B. Unmet Goals and Deviations

Despite these successes, the final design did not meet every target with equal margin. The largest remaining device-level issue is the PMOS drive-current weakness: the PMOS current is significantly lower than the NMOS current, primarily because hole mobility is lower than electron mobility and because PMOS halo and threshold tuning required a stronger tradeoff between leakage suppression and turn-on behavior. The PMOS subthreshold swing is also slightly above the ideal target range, with SS ≈ 102.7 mV/dec, compared with the stronger NMOS value of 68.3 mV/dec. In addition, both threshold voltages remain higher than the approximate $V_{T,\mathrm{sat}} \sim 0.200$ V target, with the NMOS at approximately 0.322 V and the PMOS threshold magnitude near 0.479 V. The DIBL extraction indicates reasonable short-channel control, but the PMOS DIBL can approach or slightly exceed the 100 mV/V target depending on the extraction used. These deviations show that the planar 19 nm design achieved functional operation and leakage control, but still requires additional optimization before it could be considered a fully balanced high-performance CMOS technology. The inverter simulation also reflects this imbalance: even with PMOS area-factor tuning, the voltage-transfer curves remain skewed because the NMOS pull-down device is stronger than the PMOS pull-up device [2], [7], [8], [10].

C. Future Work

Future work should first focus on improving PMOS/NMOS balance. The most direct circuit-level correction is additional PMOS width scaling through the Sentaurus area factor, since practical CMOS gates commonly use a wider PMOS device to compensate for lower hole mobility. However, width scaling alone increases layout area, so device-level PMOS improvements are also needed. These should include improved PMOS halo placement, reduced excessive interface doping, and further work-function tuning to reduce $|V_T|$ without causing excessive leakage. Strain engineering is another important future direction, especially compressive strain for PMOS to improve hole mobility and increase drive current. The optional strain portion of the assignment could therefore be used to quantify how mobility enhancement changes NMOS and PMOS on-current, inverter switching point, and PMOS/NMOS balance [7], [12], [13].

Future work should also make the TCAD model more realistic and more publication-ready. The present simulations used idealized Gaussian implant profiles, idealized contacts, and drift-diffusion-based transport with quantum and mobility corrections, but did not fully model gate leakage, oxide–semiconductor interface traps, contact resistance, hydrodynamic or quasi-ballistic transport, self-heating, or statistical process variation. A more complete study should include calibrated process simulation, annealing and dopant-activation models, contact-resistance extraction, interface-trap and gate-leakage models for the high-k stack, and variability studies for channel length, junction placement, halo dose, and work function. These additions would allow the design to move beyond a functional TCAD demonstration toward a more realistic assessment of manufacturability, reliability, and circuit-level performance for scaled high-performance CMOS logic [2]–[6].

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