UC Irvine
UC Irvine Electronic Theses and Dissertations

Title
Non-isolated High Step-Up and High Step-Down DC-DC Converters

Permalink
https://escholarship.org/uc/item/3h99k2h1

Author
Zheng, Yifei

Publication Date
2019

Peer reviewed|Thesis/dissertation

eScholarship.org Powered by the California Digital Library
University of California

UNIVERSITY OF CALIFORNIA,
IRVINE

Non-isolated High Step-Up and High Step-Down DC-DC Converters

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

by

Yifei Zheng

Dissertation Committee:
Professor Keyue Smedley, Chair
Professor Michael Green
Professor Ender Ayanoglu

2019

© 2019 Yifei Zheng

DEDICATION

To my wife

Lulu Li

and my daughter

Julia Qiyuan Zheng

TABLE OF CONTENTS

LIST OF FIGURES

Page

LIST OF TABLES

Page

ACKNOWLEDGMENTS

I would like to express my deepest gratitude to my Ph.D. advisor, Prof. Keyue Smedley, for offering me a great opportunity to pursue my degree, and for all her guidance, encouragement and support during my PhD study and research. Prof. Smedley's extensive knowledge, insightful vision and critical thinking have been of great value for my professional development. Without her continuous guidance and support, this work would not have been possible.

I am extremely grateful to my committee members, Prof. Michael Green and Prof. Ender Ayanoglu, for their time, service and valuable advices.

I would also like to thank all my colleagues in UCI Power Electronics Lab over the years, for their help, support and friendship. They are Dr. Roozbeh Naderi, Dr. Bin Wu, Dr. Shouxiang Li, Ms. Ling Jiang, Mr. Daniel Gebbran, Dr. Xiangli Kang, Mr. Wenhao Xie, Mr. Benjamin Koller, Mr. Benjamin Brown, and Dr. Anto Joseph.

I would like to thank the University of California, Irvine, for the scholarships that I received during my Ph.D. study. I would like to thank One-Cycle Control, Inc., for the funding and support of my research work.

I am deeply indebted to my parents, Tongpeng and Xiulan, and my sisters, Yiling and Yifang. Their dedication and support have allowed me to continue my education to the PhD level. I would like to express my deep gratitude to my wife, Lulu, for her love, encouragement and accompany during my hard and good times. I would like to thank my daughter, Julia, for the great happiness she brings into my life.

CURRICULUM VITAE

Yifei Zheng

EDUCATION

2019	Ph.D. in Electrical Engineering University of California Irvine, CA, USA
2012	M.S. in Electrical Engineering Xi'an Jiaotong University, Xi'an, China
2009	B.S. in Electrical Engineering Beijing Jiaotong University, Beijing, China

PUBLICATIONS

[1] **Y. Zheng**, B. Brown, W. Xie, S. Li, K. Smedley, "High Step-Up DC-DC Converter with Zero Voltage Switching and Continuous Input Current," in IEEE Transactions on Power Electronics, in review.

[2] **Y. Zheng**, K. Smedley, "Analysis and Design of a Single-Switch High Step-Up Coupled-Inductor Boost Converter," in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2019.2915348, accepted for publication.

[3] **Y. Zheng**, W. Xie and K. M. Smedley, "A Family of Interleaved High Step-Up Converters with Diode-Capacitor Technique," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2019.2907691, accepted for publication.

[4] **Y. Zheng**, K. Smedley, "Interleaved High Step-Up Converter Integrating Coupled Inductor and Switched Capacitor for Distribution Generation Systems," in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2018.2878409, accepted for publication.

[5] **Y. Zheng**, W. Xie, K. Smedley, "Interleaved High Step-Up Converter with Coupled Inductors," in IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 6478-6488, July 2019.

[6] **Y. Zheng**, S. Li and K. M. Smedley, "Nonisolated High Step-Down Converter with ZVS and Low Current Ripples," in IEEE Transactions on Industrial Electronics, vol. 66, no. 2, pp. 1068-1079, Feb. 2019.

[7] **Y. Zheng**, S. Li, S. Dey and K. Smedley, "Family of Isolated Bidirectional Resonant Converters with Duty-Cycle Control and Automatic Power Flow Transition," in IET Power Electronics, vol. 11, no. 9, pp. 1582-1590, 78 2018.

[8] S. Li, **Y. Zheng** and K. M. Smedley, "A Family of Step-Up Resonant Switched-Capacitor Converter with a Continuously Adjustable Conversion Ratio," in IEEE Transactions on Power Electronics, vol. 34, no. 1, pp. 378-390, Jan. 2019.

[9] S. Li, **Y. Zheng**, B. Wu and K. M. Smedley, "A Family of Resonant Two-Switch Boosting Switched-Capacitor Converter With ZVS Operation and a Wide Line Regulation Range," in IEEE Transactions on Power Electronics, vol. 33, no. 1, pp. 448-459, Jan. 2018.

[10] S. Li, K. Xiangli, **Y. Zheng** and K. M. Smedley, "Analysis and Design of the Ladder Resonant Switched-Capacitor Converters for Regulated Output Voltage Applications," in IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 7769-7779, Oct. 2017.

.

ABSTRACT OF THE DISSERTATION

Non-isolated High Step-Up and High Step-Down DC-DC Converters

By

Yifei Zheng

Doctor of Philosophy in Electrical Engineering

University of California, Irvine, 2019

Professor Keyue Smedley, Chair

Non-isolated high step-up and high step-down DC-DC conversions are highly demanded in many applications, including renewable energy systems, uninterrupted power supplies, data centers, high-end computers, etc. The high voltage-conversion-ratio requirement poses challenges on energy efficiency, power density, cost and reliability. This dissertation explores new high step-up and high step-down topologies for various applications.

First, a new family of interleaved high step-up converters integrating coupled-inductor and switched-capacitor are introduced for high current and ultra-high step-up applications. By integrating coupled-inductor and switched-capacitor techniques, the proposed converter achieves ultra-high step-up voltage gain without the need of extreme duty cycle or high turns ratio. Also, very low switch voltage stress can be achieved, thus low-voltage-rating MOSFETs with small on-resistance can be used to lower the conduction loss. Moreover, thanks to the interleaved operation at the input side, the input current is shared and low input current ripple is obtained. Furthermore, the coupled-inductor leakage energy can be recycled, which helps alleviate reverse recovery problem.

Second, multiphase interleaved high step-up converter with diode-capacitor voltage multiplier stages is presented, which is an extension of the previously reported two-phase current-fed Cockcroft–Walton multiplier. The multiphase configuration has flexible structure. It achieves high current handling capability, high voltage gain, low component voltage stress, low input current ripple and automatic phase current balancing. A three-phase converter in the multiphase family was analyzed and evaluated in detail.

Third, a single-phase coupled-inductor boost converter is presented for low current high boost applications. The voltage gain can be extended by the coupled inductor. Due to a independent inductor at the input, continuous input current is obtained, which significantly reduces the input capacitor, leading to increased power density and reliability. Also, the new converter has low component count, leading to low cost. Furthermore, recycled leakage energy and alleviated diode reverse recovery can be achieved.

Fourth, an improvement is proposed based on the proposed single-phase coupled-inductor boost converter. The improved converter not only retains the advantages of high voltage gain and continuous input current, but also achieves low semiconductor voltage stresses, zero-voltage switching and zero DC magnetizing current, which helps increase efficiency and power density.

Extensions of the above high step-up converters to high step-down operation are also discussed in the dissertation. Additionally, a 48V-to-1V high step-down converter is presented, where high step-down conversion is realized by an energy transfer capacitor and built-in transformer. Due to the interleaved technique, small values of output inductance can be used, leading to fast transient response. Furthermore, the use of a coupled inductor

not only reduces the number of cores but also reduces inductor current ripples, leading to lower losses. Four switches are used in the converter and all can achieve zero-voltage-switching. Grounded gate drivers and boost strap drivers can be employed, avoiding the use of complex isolated gate drivers. In addition, if one of the switches fails, the high input voltage is blocked from the output to keep the load safe.

Chapter 1 Introduction

1.1 Application Background

1.1.1 High Step-Up DC-DC Conversion

In last decades, high step-up DC-DC conversion has attracted substantial attentions in many application areas. Fig 1.1 shows an example of renewable energy based distributed generation system [1]-[2]. The renewable sources, such as photovoltaic arrays and fuel cells, generate a low output voltage, typically 20V-40V. Such low-level voltage needs to be boosted to a high DC-bus voltage (e.g. 400V or 800V) for grid connection. Hence, a frond-end high step-up DC-DC converter is required. In offshore wind energy system with medium-voltage DC (MVDC) grid, as shown in Fig. 1.2, a high step-up DC-DC converter is needed to interface the rectifier output (1kV~6kV) with the MVDC bus (30kV~60kV) [3]. In uninterrupted power supplies, the low battery voltage must be increased to a high DC voltage to support the load when there is a grid fault, as shown in Fig. 1.3 [4]. In network server power supplies, high step-up converter is needed to increase the 48V of the DC battery plant to a 380V intermediate bus voltage, as shown in Fig. 1.4 [5]-[6]. High-intensity-discharge lamp ballast for automobiles also requires a high step-up converter to boost 12 V battery voltage up to 100V to support the load, as shown in Fig. 1.5 [6].

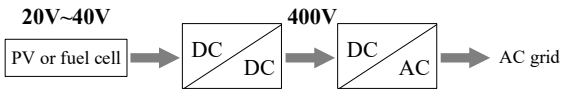


Fig. 1.1 Photovoltaic or fuel cell based distributed generation system

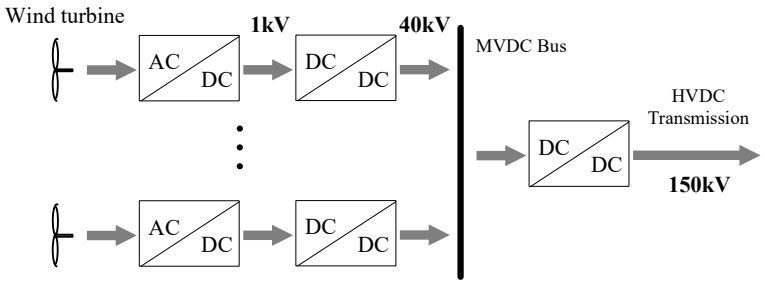


Fig. 1.2 Offshore wind energy system with MVDC grid

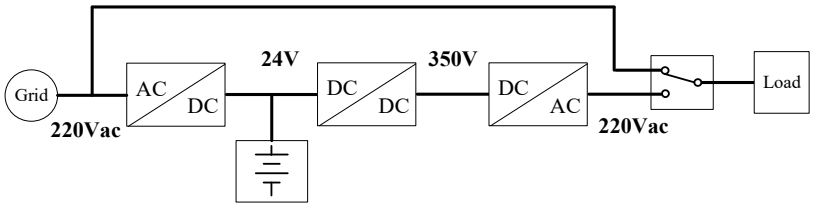


Fig. 1.3 Uninterrupted power supply

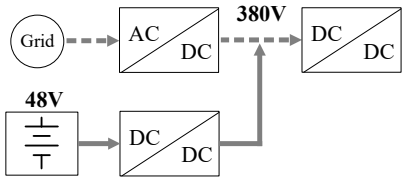


Fig. 1.4 Network server power supply

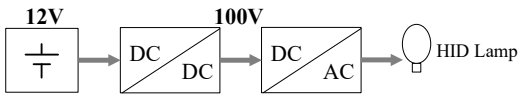


Fig. 1.5 HID lamp ballast for automobiles

1.1.2 High Step-Down DC-DC Conversion

With the development of cloud computing and big data, the power consumption in data centers is increasing dramatically. In the year of 2014, around 70 billion kWh of electricity was consumed by data centers in the U.S., representing about 1.8% of the total U.S. electricity consumption [7]. Meanwhile, most of the power supplies in data centers are

inefficient. Around half of the energy is lost in power conversion, distribution, and cooling [8]-[9]. Efficient power supply for data centers is becoming a challenging issue. Recently, Google introduced a 48V rack power architecture for data centers, as shown in Fig. 1.6. which provides a 16x reduction in power distribution loss and better conversion efficiency [10]. This power architecture requires a high step-down dc-dc converter to convert the 48V DC bus voltage down to 1V or below to power the processors. High step-down DC-DC converters are also needed in many other applications such as high-end computers, telecommunication power systems, and LED drivers [11]-[12].

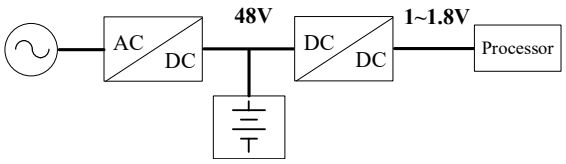


Fig. 1.6 Data center power supply

1.2 Review of High Step-Up DC-DC Topologies

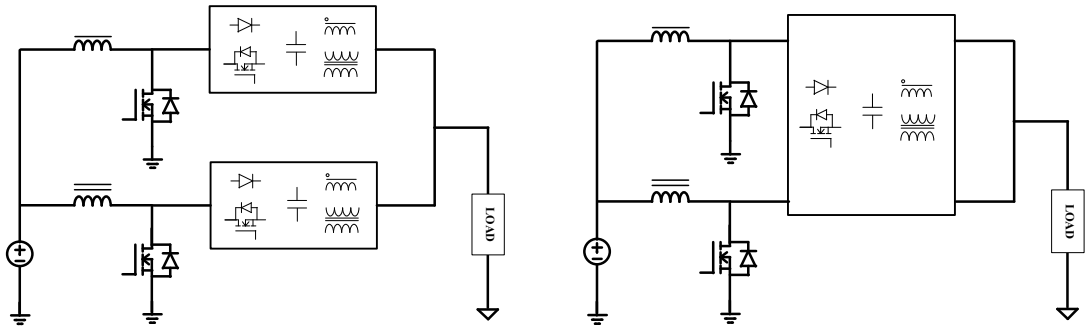
Conventional boost converter has limitation when used in high step-up applications due to extreme duty cycle, high voltage stress, high current ripple, and high switching and conduction losses. Therefore, many non-isolated high step-up DC-DC converters have been reported in the literature [13]-[14]. Generally, high step-up converters can be classified into two types: interleaved converter and single-phase converter. Features of these two types of converters are listed in Table 1.1. Interleaved high step-up converter has shared input current, distributed thermal stress, minimized current ripple and higher voltage gain. It is more suitable for high-current applications. Single-phase converter has lower component count and is more suitable for low current applications.

Table 1.1 Features of interleaved and single-phase high step-up converter

Interleaved converter	Single-phase converter
• Very high voltage gain	• High voltage gain
• Shared input current	• Single input current
• Distributed thermal stress	• High thermal stress
• Low current ripple	• High current ripple
• High component count (high cost)	• Low component count (low cost)
• More suitable for high current applications	• More suitable for low current applications

1.2.1 Interleaved High Step-Up Converters

Theoretically, multiple single-phase converters can be connected in parallel to realize interleaved operation, as shown in Fig. 1.7 (a). However, it results in high component count. Also the voltage gain and component voltage stress are not improved, remaining the same as the single-phase converter. This dissertation studies the interleaved high step-up converters with shared voltage-gain-extension components. This type of interleaved converters has fewer components, higher voltage gain and lower component voltage stress. As we know, the input current level is much higher than the output current level in high step-up converters. Hence, only input interleaved operation is needed. A generalized structure is shown in Fig. 1.7 (b). At the input side, interleaved operation is realized to handle high input current, minimize current ripple and distribute thermal stress. At the output side, shared components are utilized as a voltage multiplier (VM) to extend the voltage gain. Typically, magnetic coupling and/or switched capacitor are employed for voltage boosting in interleaved high step-up converters. Features of interleaved high step-up converters using magnetic coupling and switched capacitor are compared in Table 1.2. Both techniques have advantages and disadvantages. A review of these converters in the literature is presented in the subsections.



(a) (b)

Fig. 1.7 Interleaved high step-up structure: (a) multiple single-phase converter in parallel; (b) interleaved structure with shared components.

Table 1.2 Features of interleaved high step-up converters using magnetic coupling and switched capacitor

Interleaved high step-up converters	
Using magnetic coupling	Using switched capacitor
• Ultra-high voltage gain • Relatively low component count • Relatively high diode voltage stress • Alleviated diode reverse recovery • Relatively complicated design	• High voltage gain • High component count, especially when very high voltage gain is needed • Low diode voltage stress • Diode reverse recovery problem • Modular structure and simple design

1.2.1.1 Interleaved High Step-Up Converter with Magnetic Coupling

Utilizing magnetic coupling (coupled inductor or transformer) provides an extra degree of design freedom, along with the duty cycle, to achieve a high step-up voltage gain. However, the leakage inductance may cause large voltage spikes across the switches during the switch transient, causing high voltage stress and degraded efficiency, which must be handled carefully. Examples of interleaved high step-up converter with magnetic coupling are shown in Fig. 1.8. The converter proposed in [15]-[16] integrate the interleaved boost stage with voltage-double module via magnetic coupling, as shown in

Fig. 1.8 (a)-(b). Hence, the voltage gain is extended and interleaved input operation is maintained. The converter proposed in [17]-[18] (as shown in Fig. 1.8 (c)-(d)) added diode-capacitor voltage multiplier cell to the converter in Fig. 1.8 (b), thus the voltage gain is further extended. The converter proposed in [19] (as shown in Fig. 1.8 (e)) added diode-capacitor cell to the converter in Fig. 1.8 (a). Unfortunately, the currents in the primary windings are not shared equally, causing unbalanced current and thermal stress. The converter in [20] utilizes input-parallel and output-series connection to reduce the current ripple and extend the voltage gain, as shown Fig. 1.8 (f). However, the input and the output do not have a common ground, which has limited applications. The converter in [21] employs four active switches to achieve high step-up conversion and zero-voltage switching, as shown in Fig. 1.8 (g). The increased number of switches and gate drivers leads to high cost. The converter in [22] integrates interleaved coupled inductor boost converter with diode-capacitor voltage doubler, as shown in Fig. 1.8 (h). However, the voltage gain is low and active clamp circuits are added to deal with the leakage problem. The converters in [23]-[25] are configured by combining two boost stages, three-winding built-in transformer and diode-capacitor voltage multiplier cells. One example is shown in Fig. 1.8 (i). Unfortunately, these converters have high component count and large magnetic size. Interleaved high step-up converters employing six windings are proposed in [26]-[29]. More flexible voltage gain is obtained at the price of increased circuit complexity and high cost.

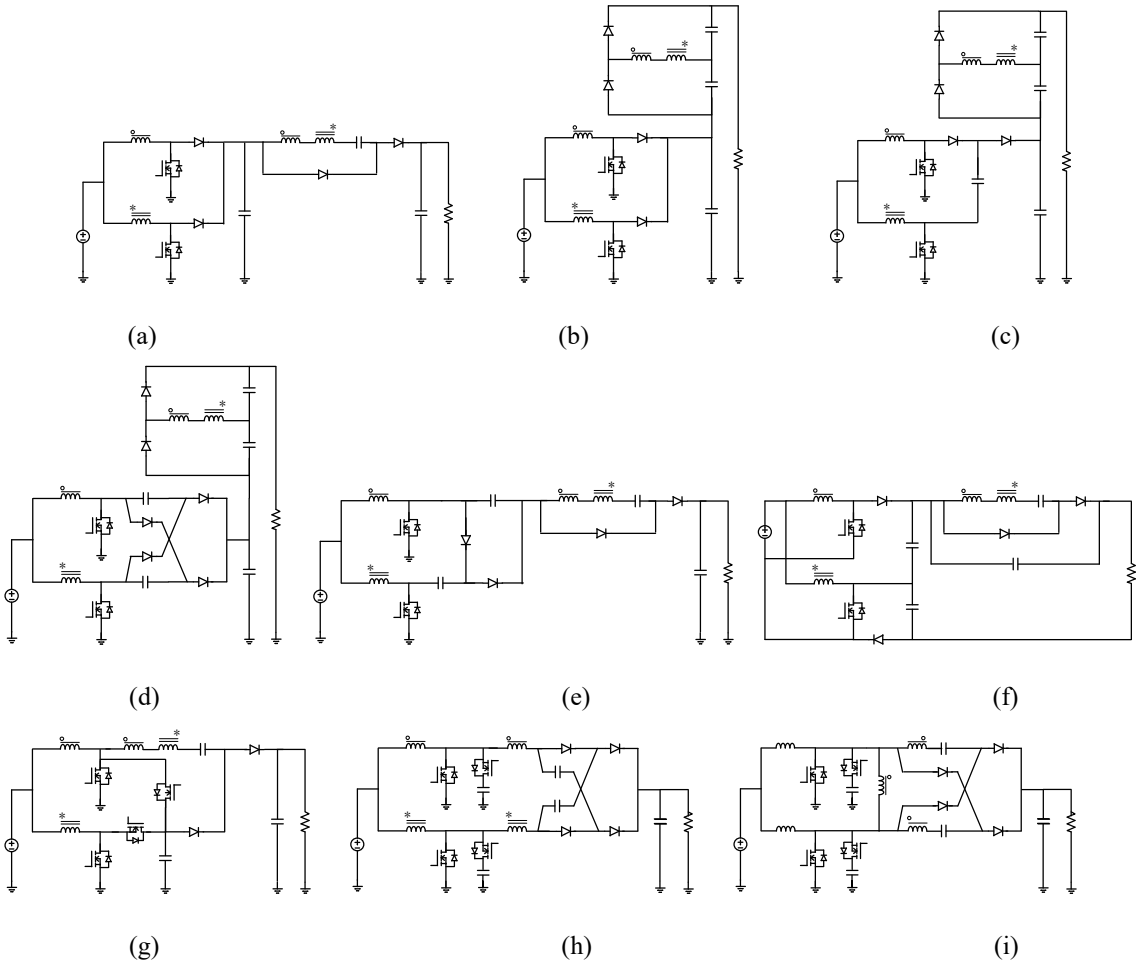


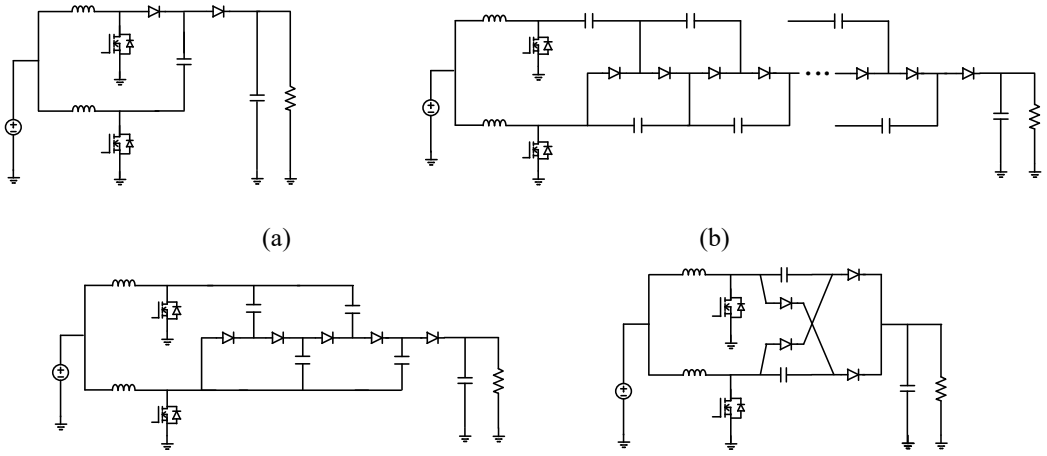
Fig. 1.8 Interleaved high step-up converters with magnetic coupling: (a) topology in [15]; (b) topology in [16]; (c) topology in [17]; (d) topology in [18]; (e) topology in [19]; (f) topology in [20]; (g) topology in [21]; (h) topology in [22]; (i) topology in [23].

1.2.1.2 Interleaved High Step-Up Converter with Switched Capacitor

Switched capacitor converter has advantages including high efficiency, high power density, low semiconductor voltage stress and flexible structure. But it has high transient charging/discharging current and poor regulation capability. The conventional boost converter has no high current spike and can be easily regulated, but it has limited voltage gain. Combining the boost stage with switched capacitor is an effective way to extend the

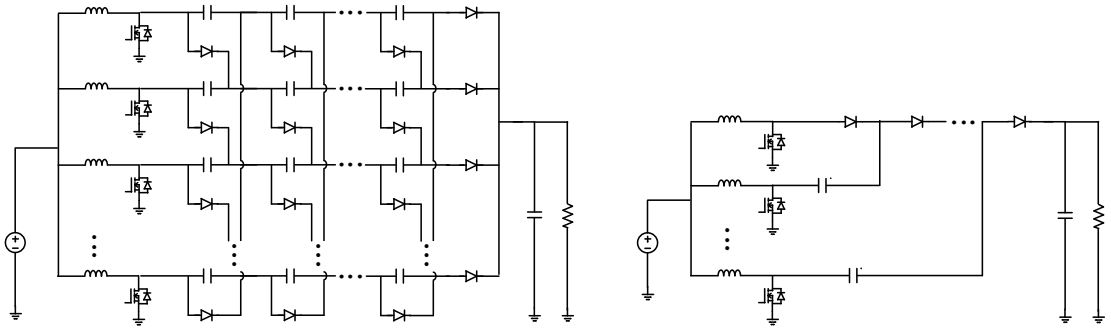
voltage gain, reduce semiconductor voltage stress, eliminate current spike and achieve easy regulation. Two-phase interleaved high step-up converters with switched capacitor have been proposed [30]-[37]. The converters in [30] integrates two-phase boost stage with voltage doubler to extend the voltage gain, as shown in Fig. 1.9 (a). The converters in [31] presents a two-phase boost stage with voltage quadrupler, but the input and the output share uncommon ground. The converter in [32] combines two-phase boost with Cockcroft–Walton (CW) multiplier, as shown in Fig. 1.9 (b). High voltage gain and low component voltage stress can be achieved with relatively small component count. The converter in [33] is also an interleaved converter based on CW multiplier, using active clamp circuit to realize soft switching. Unfortunately, the output does not share the same ground with the input. The converter in [34] integrates two-phase boost with Dickson charge pump to realize high voltage gain, as shown in Fig. 1.9 (c), but the capacitors suffer from high voltage stress. The converter in [35] integrates two-phase boost with modified Dickson charge pump. Capacitor voltage stress is reduced but the input and output are uncommon grounded. A bidirectional converter using Dickson charge pump is proposed in [36]. Dynamic frequency modulation is introduced to improve efficiency. The converters in [37] and [38] combines two-phase boost with diode-capacitor VM cells, as shown in Fig. 1.9 (d). This structure has relatively low voltage gain in comparison to its component count. The above-mentioned converters only have two phases. Interleaved converters with higher number of phases were also presented. The multiphase configuration proposed in [37], as shown in Fig. 1.10 (a), is an extension of the two-phase converter in Fig. 1.9 (e). It achieves high voltage gain at the price of high component count. A multiphase extended-duty-ratio (EDR) boost converter was presented in [39], as shown in Fig. 1.10 (b). Due to

the multiphase structure, the input current ripple can be further reduced and the power level can be increased. But the voltage gain may not be high enough for some low-input-voltage and high-output-voltage applications. The converter proposed in [40] is configured by multiphase boost stage at the input and series-connected full bridge rectifier at the output. Soft switching is realized to improve efficiency. A symmetric multiphase converter integrated with diode-capacitor VM cells was proposed in [41]. It has high component count and uncommon grounded connection between the input and the output.



(a) (b) (c) (d)

Fig. 1.9 Two-phase interleaved high step-up converters with switched capacitor: (a) topology in [30]; (b) topology in [32]; (c) topology in [34]; (d) topology in [37].



(a) (b)

Fig. 1.10 Multiphase interleaved high step-up converters with switched capacitor: (a) topology in [37]; (b) topology in [39].

1.2.2 Single-Phase High Step-Up Converters

Many single-phase high step-up converters have been reported in the literature using various boosting techniques, such as switched capacitor [42]-[48], switched inductor [47]-[52], voltage multiplier cells [53]-[54], and magnetic coupling [55]-[94]. Among them, single-phase converter with coupled inductor has attracted substantial attention because high voltage gain can be achieved by simply increasing the turns ratio of the coupled inductor. The basic coupled-inductor (or tapped-inductor) boost converter was presented in 1970s [55], as shown in Fig 1.11 (a). It has simple structure, but the leakage energy would result in large voltage spike across the switch, causing high switch voltage stress and degraded efficiency. Hence, coupled-inductor converters with passive or active clamp circuit were proposed to handle the leakage problem [56]-[57]. Typical topologies are shown in Fig. 1.11 (b)-(c). Converters integrating coupled inductor with switched-capacitor or voltage-multiplier cells were also proposed to recover the leakage energy and further increase the voltage gain [58]-[68]. Some examples are shown in Fig. 1.11 (d)-(f). Active clamp can be utilized in coupled-inductor converters to realize zero-voltage switching [69]-[75]. Examples are shown in Fig. 1.11 (g)-(h). These coupled-inductor topologies feature a pulsating input current. The peak-to-peak current ripple depends on the current level and the turns ratio. If the current level is increased or the turns ratio is increased for higher voltage gain, the input current ripple becomes even larger. The pulsating input current is detrimental to the lifetime of the low-voltage sources like batteries and fuel cells [76]-[77]. Also, in PV applications, the pulsating input current makes it hard to precisely track the true maximum power point (MPP), which can cause a severe drop in energy extraction [78]. Therefore, in practice, additional LC (or C) input

filter is required. Due to the high current stress at the input side, large electrolytic capacitor has to be employed, which is not only bulky and costly, but also has a short lifetime, hampering the reliability of the system [79]-[80].

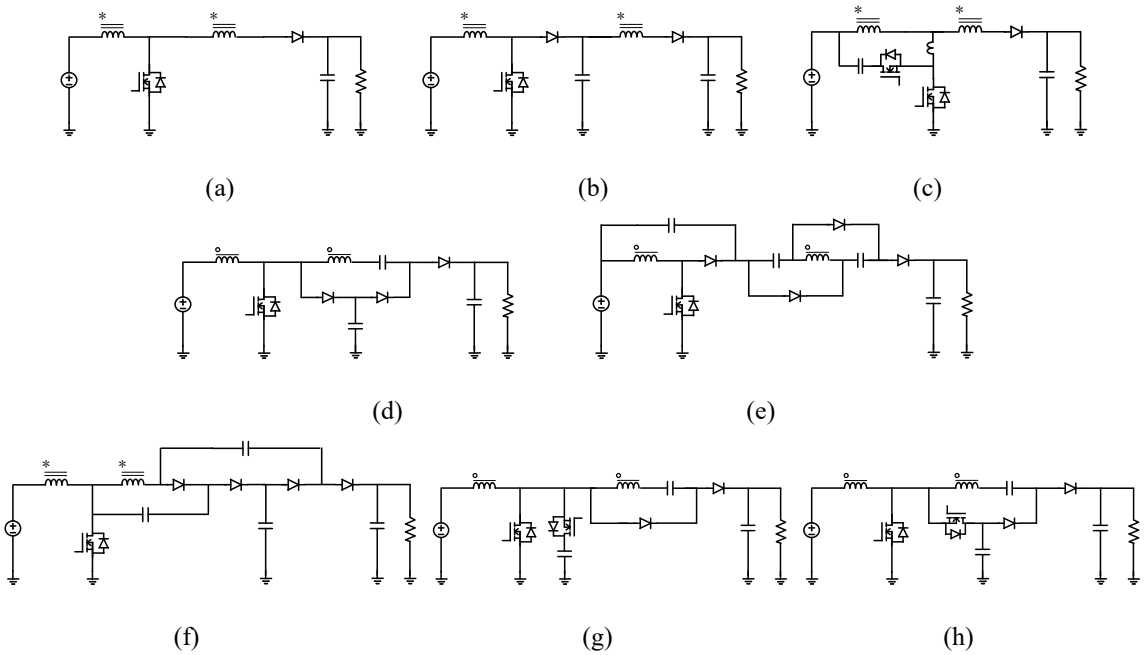


Fig. 1.11 Single-phase high step-up converters with pulsating input current: (a) topology in [55]; (b) topology in [56]; (c) topology in [57]; (d) topology in [58]; (e) topology in [59]; (f) topology in [62]; (g) topology in [70]; (h) topology in [71].

Converters with continuous input current are advantageous for battery, fuel cell and PV applications. The feature of continuous input current can significantly reduce the input capacitor or even save the input filter, which increases the power density and reliability. SEPIC-derived coupled-inductor converters have been proposed [81]-[90]. Continuous input current is obtained by a discrete inductor at the input. High voltage gain is achieved with the aid of coupled inductor. Some examples are shown in Fig. 1.12 (a)-(d). In [87]-[88], quasi-resonant operation is utilized to realize zero-current switching in order to reduce switching loss. One example is shown as in Fig. 1.12 (e). Unfortunately, conduction

loss is also increased due to quasi-sinusoidal currents. In [89]-[90], zero-voltage switching is achieved due to active clamp, as shown in Fig. 1.12 (f)-(g). However, the energy transferred through the coupled inductor comes from the capacitor in series with the primary winding rather than directly from the input, leading to larger primary conduction loss and lower voltage gain. Quadratic boost based coupled inductor converters have also been reported to achieve continuous input current [91]-[94]. Some examples are shown in Fig. 1.12 (h)-(i). Quadratic high voltage gain is obtained at the price of high cost.

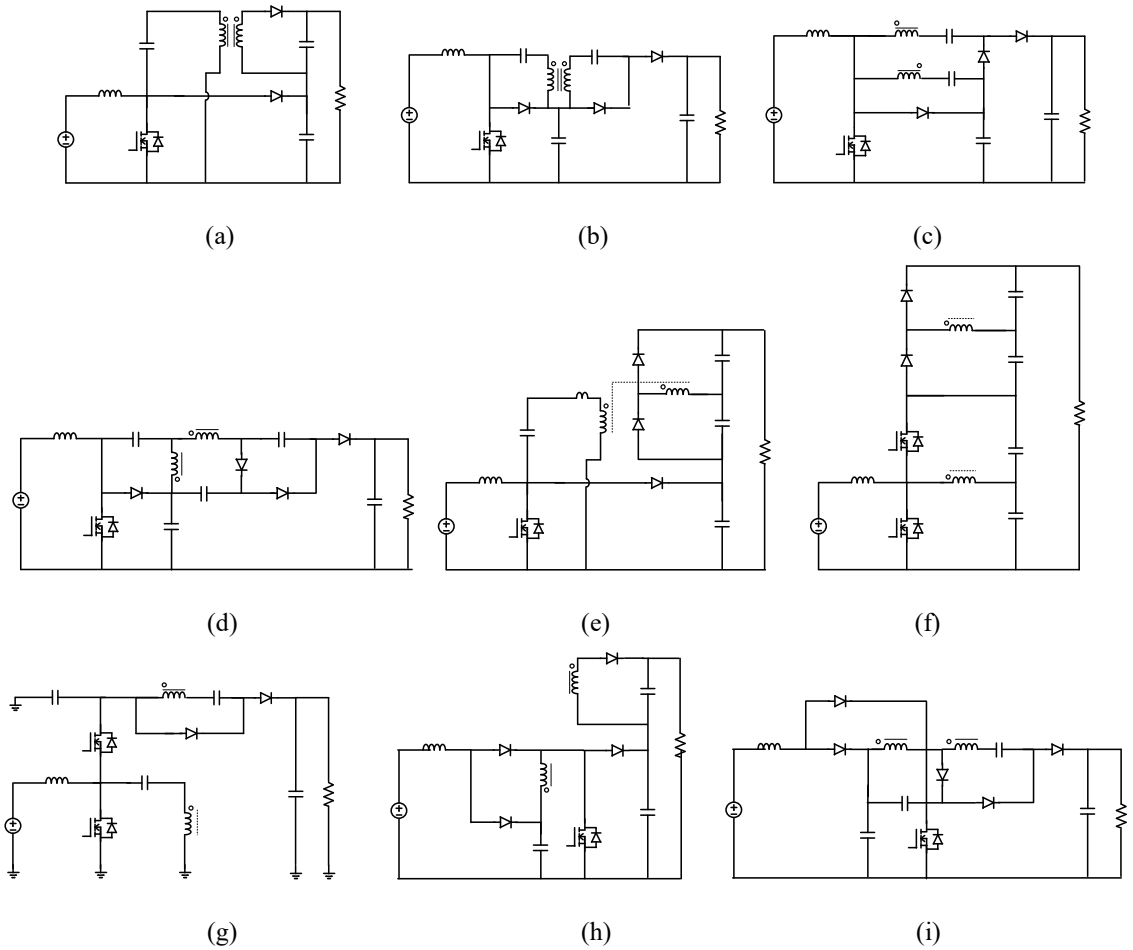


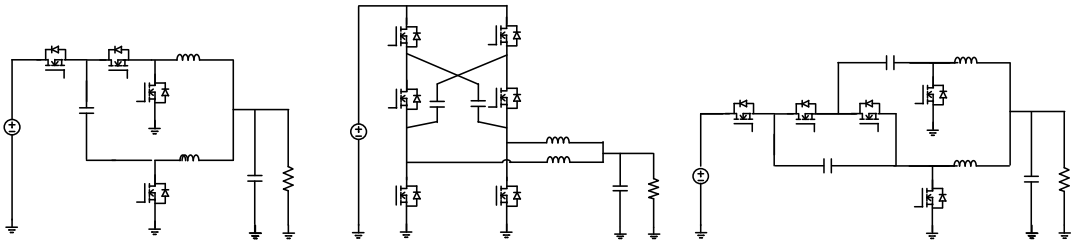
Fig. 1.12 Single-phase high step-up converters with continuous input current: (a) topology in [81]; (b) topology in [82]; (c) topology in [83]; (d) topology in [84]; (e) topology in [87]; (f) topology in [89]; (g) topology in [90]; (h) topology in [91]; (i) topology in [92].

1.3 Review of High Step-Down DC-DC Topologies

The conventional buck converter is not suitable for high step-down applications. First, the switching loss of the top switch is significant because the switching current equals the large output current. Second, as the voltage stress of the synchronous rectifier (SR) equals to the high input voltage, high voltage rating SR has to be used, leading to high conduction loss. Third, in order to reduce the output ripple, a large inductor must be used, which limits transient response. Fourth, the extreme duty cycle makes current sensing and control to be tough, especially at high frequencies.

One solution for high step-down conversion is to use a two-stage approach. The first stage converts the high input voltage to an intermediate voltage, and then the second stage converts the intermediate voltage to the low output voltage. The multiphase synchronous buck converter is typically used as the second stage to handle high output current, small ripple and fast transient response. LLC converter, switched capacitor converter, active-clamped forward converter and buck converter have been reported being used as the first stage [95]-[98]. Two-stage approach can achieve flexible control, but the overall efficiency is compromised as it equals the product of the efficiencies of each stage.

Single stage high step-down converters have also attracted substantial attentions. Transformer-less high step-down converter have been reported [99]-[105]. Some examples are shown in Fig. 1.13. This type of converters can achieve high power density. Although the duty cycle has been extended compared to conventional buck converter, it could be still small under high step-down applications (for example, 48V to 1V), which degrades the efficiency and makes the controller hard to design. Also, some of these converters may have high transient current through the switches, leading to serious EMI problem.



(a) (b) (c)

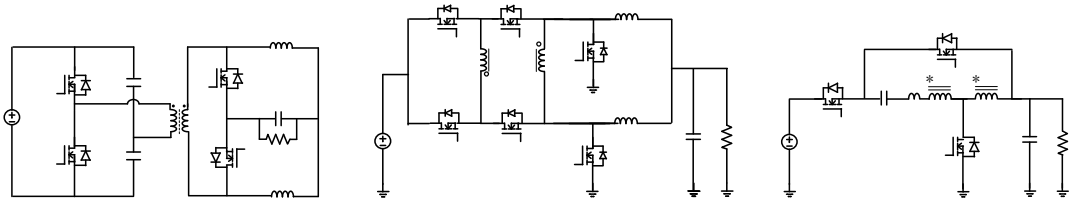
Fig. 1.13 Transformer-less high step-down converter: (a) topology in [99]; (b) topology in [100]; (c) topology in [101].

Utilizing magnetic coupling is an attractive method to extend the step-down conversion ratio. Isolated converters, such as half bridge, full bridge and forward converter, can be used in high step-down applications [106]-[108]. One typical topology is half bridge converter with current doubler, as shown in Fig. 1.14 (a). Non-isolated converter with built-in transformer were also reported [109]-[112], which can achieve smaller transformer size and reduced current stress. The phase-shift buck converter proposed in [109] is shown in Fig. 1.14 (b). High step-down conversion is achieved with the transformer and ZVS is achieved by phase shift operation, but high component count is involved. The converter in [111]-[112] have pulsating output current, leading to large capacitor size. Also, transformer-isolated or opt-isolated gate drivers are required. Quasi-parallel converters consisting of a DC/DC unregulated transformer and a buck type converter were presented in [113]-[114]. This structure can achieve large conversion ratio with high efficiency. However, many switches are used and complex isolated gate drivers are required.

In [115]-[116], the Cuk-buck converter was proposed, as shown in Fig. 1.14 (c)-(e). A hybrid transformer was utilized and a hybrid switching method was presented for the

first time, which enables a high step-down voltage conversion with remarkable high efficiency. Since the output current of Cuk-buck converter is near sinusoidal, the current ripple is relatively high. Interleaved Cuk-buck converter was presented to reduce the current ripple while achieving high efficiency at a higher component count.

In [117]-[123], converters with coupled inductor (or tapped inductor) were proposed, and additional components were used to handle the leakage energy problem. Some examples are shown in Fig. 1.14 (f)-(g). Coupled inductor can help achieve high step-down conversion with moderate duty cycle. However, the output current is typically pulsating; hence, the current ripple is very high especially when the output current increases or the turns ratio increases. In [124], coupled-inductor high step-down converters with continuous output current was proposed, as shown in Fig. 1.14 (h). A discrete inductor is used together with the coupled inductor, which makes the output current ripple much smaller. It is more suitable for low-current applications due to the single-phase structure. Coupled-inductor based high step-down converter with interleaved structure were also proposed to increase the output current [125]-[127], as shown in Fig. 1.14 (i)-(k). The converter in [125] has leakage problem, extra clamp circuit has to be added. The converter in [126] requires complex isolated gate drivers. The converter in [127] has high component count, leading to high cost. Furthermore, these converters have high current ripple through the secondary windings, leading to high conduction loss.



(a) (b) (c)

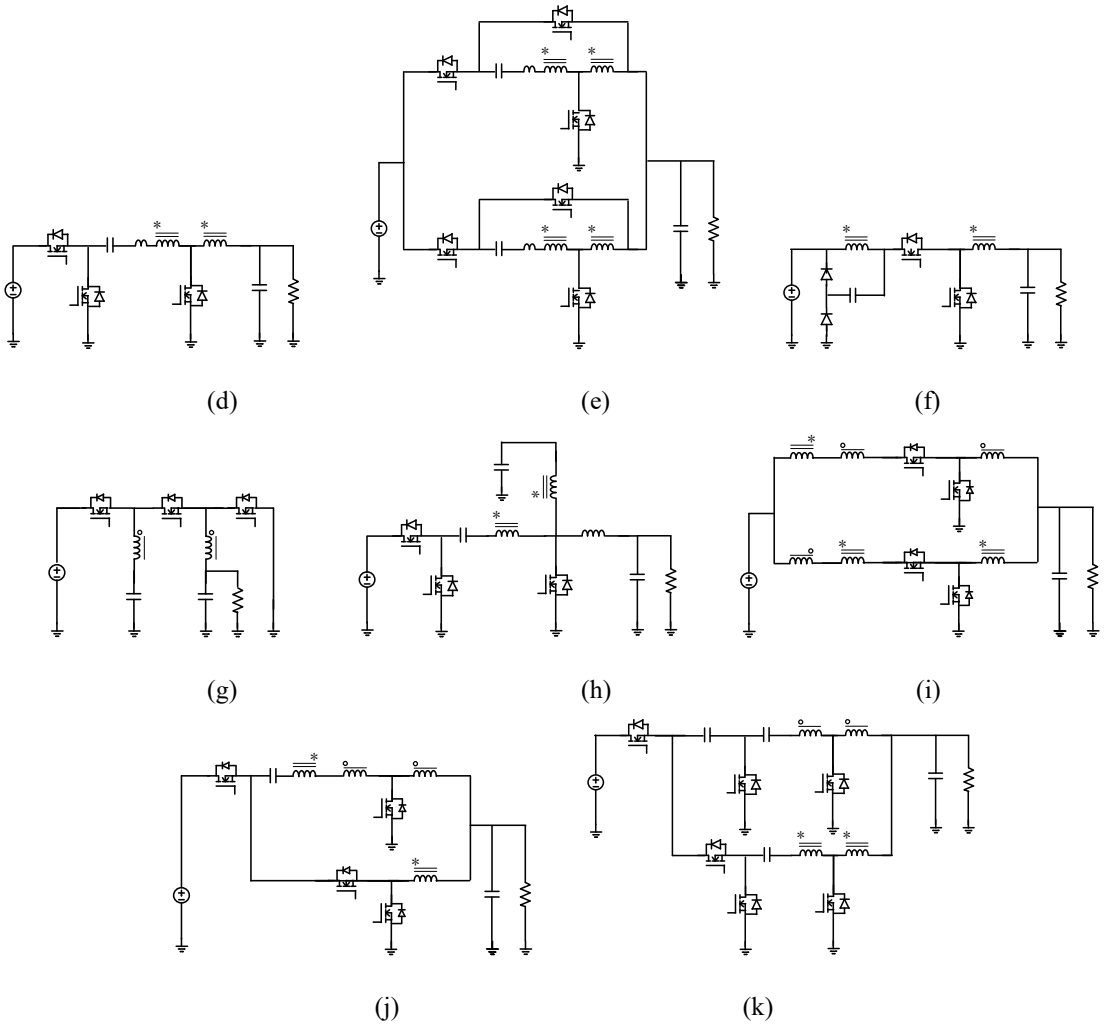


Fig. 1.14 High step-down converters with magnetic coupling: (a) topology in [106]; (b) topology in [110]; (c) topology in [115]; (d) topology in [116]; (e) topology in [115]; (f) topology in [117]; (g) topology in [118]; (h) topology in [124]; (i) topology in [125]; (j) topology in [126]; (k) topology in [127].

1.4 Motivation and Outline

Despite many merits of the existing converters, the realization of high step-up or high step-down conversion faces some challenges such as extreme duty cycle, high turns ratio of the coupled inductor or transformer, or high component count, which result in high power losses, large size and high cost. The motivation of this dissertation is to explore new

high step-up and high step-down topologies for various applications, aiming to achieve high efficiency, high power density, high step-up/step-down capability, low cost and improved reliability.

In this dissertation, new high step-up and high step-down DC-DC topologies are introduced. Interleaved high step-up converters integrating coupled inductor and switched capacitor [128] is presented in Chapter 2. Multiphase interleaved high step-up converter with diode-capacitor VM stages [129] is provided in Chapter 3. A single-phase coupled-inductor boost converter with continuous input current and low component count [130] is investigated in Chapter 4. An improved single-phase high step-up coupled-inductor boost converter with zero voltage switching and zero dc magnetizing current [131] is given in Chapter 5. The operation principles, characteristics, performance comparison, design considerations and experimental results of these converters are provided in detail. The step-down extensions of these step-up converters are also discussed. In Chapter 6, a 48V-to-1V high step-down converter with ZVS and low current ripples [132] is introduced. Performance analysis, design considerations and experimental verification are thoroughly studied. Conclusion is given in Chapter 7.

Chapter 2 Interleaved High Step-Up Converter Integrating Coupled Inductor and Switched Capacitor

In this chapter, a family of new interleaved high step-up converters integrating coupled-inductor and switched-capacitor is introduced. Interleaved operation is employed at the input side to reduce the input current ripple and increase the current level. Due to the switched capacitor and the series connection of the secondary windings, a very high step-up voltage gain can be achieved without extreme duty cycle or high turns ratio. Moreover, the proposed converter has very low switch voltage stress, thus low-voltage-rating MOSFETs with small on-resistance can be used to reduce the conduction loss. Furthermore, zero-current-switching turn-on of the switches is realized and the reverse recovery problem of the diodes is alleviated, which help reduce the switching losses. In addition, the leakage energy can be recycled, thus additional clamp circuit is not required.

The topology and operation principles of the converter are described in Section 2.1. Performance analysis are made in Section 2.2. Design considerations are discussed in Section 2.3. Experimental results are presented in Section 2.4. Topology variations are provided in Section 2.5.

2.1 Topology and Operation Principles

The proposed interleaved high step-up converter is derived by integrating two boost stages, coupled-inductor and ladder-type switched capacitor (or CW voltage multiplier), as shown in Fig. 2.1. It is composed of two coupled inductors, two switches (S_1, S_2), four

diodes (D_1-D_4), three energy transfer capacitors (C_1-C_3) and one output capacitor (C_o). The primary windings of the coupled inductors are connected in parallel and the secondary windings are connected in series. The turns ratios of the coupled inductors are the same. The coupling references are denoted by "o" and "*". Fig. 2.2 shows the equivalent circuit of the proposed converter. Both coupled inductors are modeled as an ideal transformer with magnetizing inductance (L_{m1}, L_{m2}) and leakage inductance (L_{k1}, L_{k2}). The two switches of the proposed converter are driven in an interleaved manner. The duty cycle D during steady state is larger than 0.5. The key waveforms is shown in Fig. 2.3. Eight modes are observed during one switching period. The corresponding circuits for each mode are shown in Fig. 2.4.

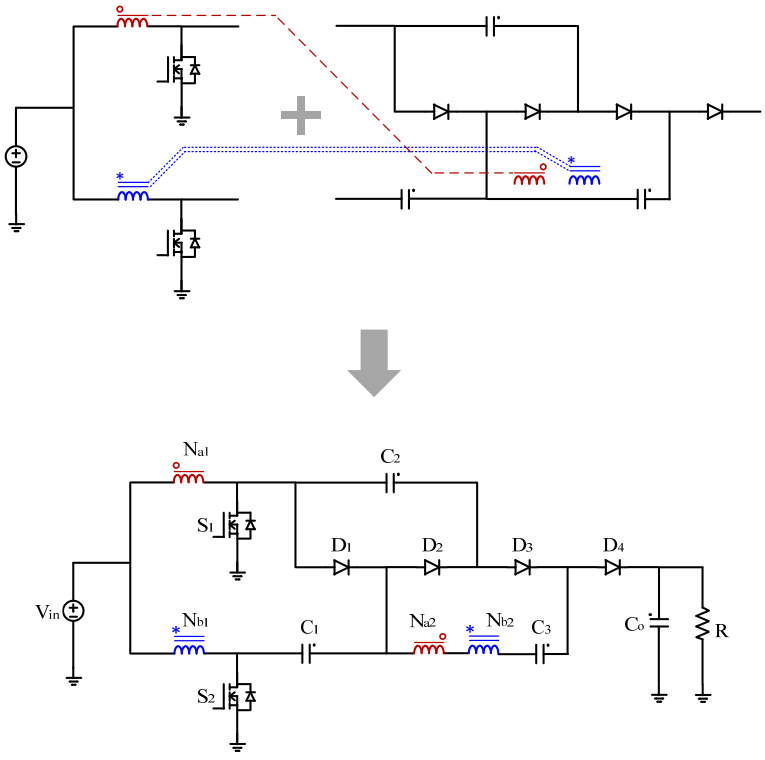


Fig. 2.1 Proposed interleaved high step-up converters integrating coupled-inductor and switched-capacitor.

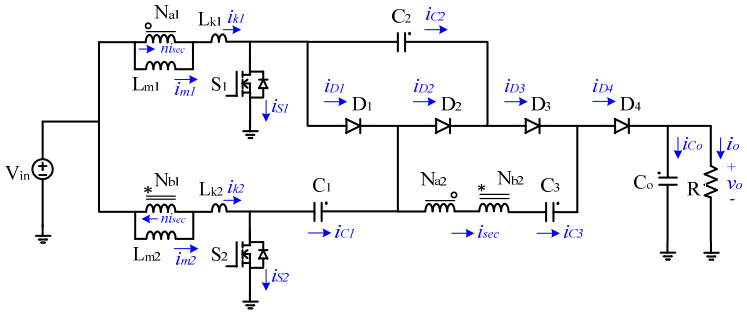


Fig. 2.2 The equivalent circuit.

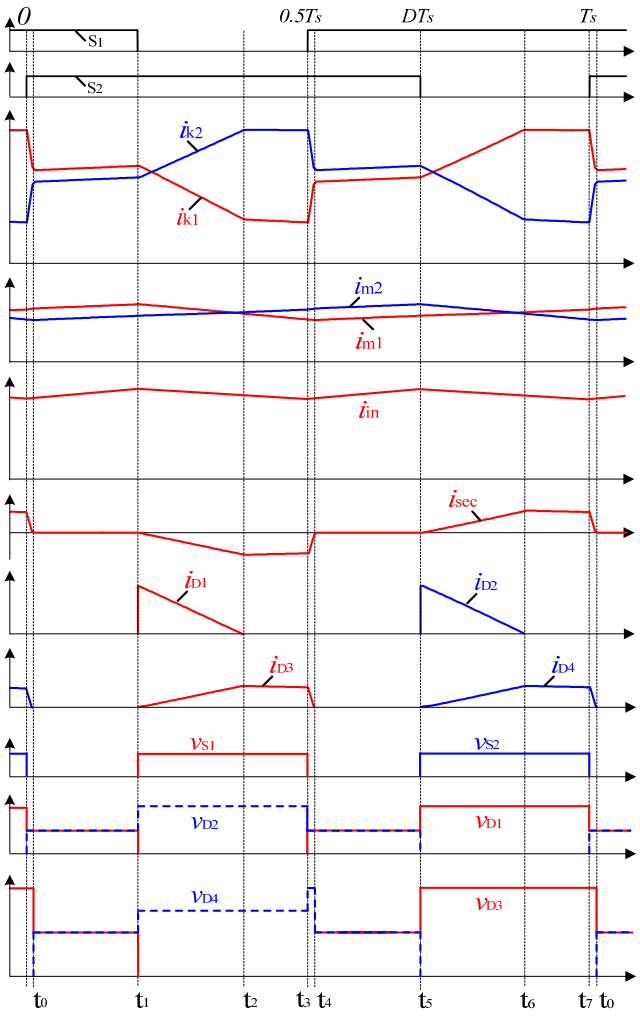


Fig. 2.3 Key waveforms

Mode 1 [t_0 - t_1]: Both switches are on, and all diodes are off, as shown in Fig. 2.4 (a). The input source is charging the magnetizing inductances and leakage inductances. As the leakage inductance is negligible compared to the magnetizing inductance, the following equations are obtained.

$$v_{m1} = V_{in} \tag{2.1}$$

$$v_{m2} = V_{in} \tag{2.2}$$

Mode 2 [t_1 - t_2]: At t_1, S_1 is turned off, which makes diodes D_1 and D_3 turned on. The input source are still charging L_{m2} and L_{k2} while L_{m1} and L_{k1} start releasing energy, as shown in Fig. 2.4 (b). The leakage current i_{k1} charges capacitor C_1. Capacitor C_2 transfers energy to C_3 and the secondary windings. The secondary current of the coupled inductors i_{sec} is increasing linearly in the opposite direction. The current through D_1 is decreasing linearly. The following equations are obtained.

$$v_{m1} = V_{in} - V_{C1} \tag{2.3}$$

$$v_{m2} = V_{in} \tag{2.4}$$

$$V_{C3} - V_{C2} - n(v_{m2} - v_{m1}) = 0 \tag{2.5}$$

$$i_{sec}(t) = -i_{D3}(t) = \frac{-nV_{C1} - V_{C2} + V_{C3}}{n^2(L_{k1} + L_{k2})}(t - t_1) \tag{2.6}$$

$$i_{k1}(t) = i_{m1}(t) + ni_{sec}(t) \tag{2.7}$$

$$i_{k2}(t) = i_{m2}(t) - ni_{sec}(t) \tag{2.8}$$

$$i_{D1}(t) = i_{k1}(t) + i_{sec}(t) = i_{m1}(t) + (n+1)i_{sec}(t) \tag{2.9}$$

where $n = N_{a2}/N_{a1} = N_{b2}/N_{b1}$.

Solving (2.3)-(2.5), the following relationship can be derived.

$$V_{C3} - V_{C2} = nV_{C1} \tag{2.10}$$

Mode 3 [t_2 - t_3]: At t_2, the current through D_1 decreases to zero and D_1 are naturally turned off. Therefore, reverse recovery problem of D_1 is alleviated. The leakage current i_{k1} becomes equal to the secondary current i_{sec}. It discharges C_2 and charges C_3 and C_1, as shown in Fig. 2.4 (c). The equations are obtained as following.

$$V_{in} = v_{m1} + V_{C1} - V_{C2} + V_{C3} - n(v_{m2} - v_{m1}) \tag{2.11}$$

$$v_{m2} = V_{in} \tag{2.12}$$

$$i_{k1}(t) = i_{m1}(t) + ni_{sec}(t) = -i_{sec}(t) \tag{2.13}$$

By manipulating (2.13), the secondary current i_{sec} can be expressed as

$$i_{sec}(t) = -i_{D3}(t) = -i_{k1}(t) = -\frac{1}{n+1} i_{m1}(t) \tag{2.14}$$

Then,

$$i_{k2}(t) = i_{m2}(\mathrm{t}) - ni_{sec}(t) = i_{m2}(t) + \frac{n}{n+1} i_{m1}(t) \tag{2.15}$$

Solving (2.10)-(2.12), v_{m1} in this mode can be derived as

$$v_{m1} = V_{in} - V_{C1} \tag{2.16}$$

Mode 4 [t_3 - t_4]: At t_3, S_1 is turned on, as shown in Fig. 2.4 (d). As the leakage inductances limit the current changing rate, ZCS of S_1 can be achieved. The current of D_3 is decreasing, and the falling rate is determined by the leakage inductances, which alleviates the reverse recovery problem of D_3. The falling rate of D_3 is given by

$$\frac{di_{D3}(t)}{dt} = -\frac{V_{C3}+V_{C1}-V_{C2}}{n^2(L_{k1}+L_{k2})} \tag{2.17}$$

Mode 5 [t_4 - t_5]: At t_4, the current of D_3 decreases to zero, and D_3 is turned off, as shown in Fig. 2.4 (e). This mode repeats mode 1.

Mode 6 [t_5 - t_6]: At t_5, S_2 is turned off, which makes diodes D_2 and D_4 turned on. The input source is charging L_{m1} and L_{k1} while L_{m2} and L_{k2} start releasing energy, as shown in Fig. 2.4 (f). The leakage current i_{k2} discharges capacitor C_1. The secondary current of the coupled inductors i_{sec} is increasing linearly. It discharges C_3 and supplies the load current. The secondary windings and capacitor C_3 serve as voltage sources to extend the voltage gain. The current through D_2 is decreasing linearly and charges C_2. The following equations are obtained.

$$v_{m1} = V_{in} \tag{2.18}$$

$$v_{m2} = V_{in} + V_{C1} - V_{C2} \tag{2.19}$$

$$V_o - V_{C2} - V_{C3} + n(v_{m2} - v_{m1}) = 0 \tag{2.20}$$

$$i_{sec}(t) = i_{D4}(t) = \frac{-V_o - nV_{C1} + (n+1)V_{C2} + V_{C3}}{n^2(L_{k1}+L_{k2})}(t - t_5) \tag{2.21}$$

$$i_{k1}(t) = i_{m1}(t) + ni_{sec}(t) \tag{2.22}$$

$$i_{k2}(t) = i_{m2}(t) - ni_{sec}(t) \tag{2.23}$$

$$i_{D2}(t) = i_{k2}(t) - i_{sec}(t) = i_{m2}(t) - (n+1)i_{sec}(t) \tag{2.24}$$

Solving (2.18)-(2.20), the following relationship can be derived.

$$V_o = (n+1)V_{C2} - \mathrm{n}V_{C1} + V_{C3} \tag{2.25}$$

Mode 7 [t_6 - t_7]: At t_6, the current through D_2 decreases to zero and D_2 are naturally turned off. Therefore, reverse recovery problem of D_2 is alleviated. The leakage current i_{k2} becomes equal to the secondary current i_{sec}. It discharges C_1 and C_3 and supplies the load current, as shown in Fig. 2.4 (g). The equations are obtained as following.

$$v_{m1} = V_{in} \tag{2.26}$$

$$V_{in} = v_{m2} - V_{C1} + n(v_{m2} - v_{m1}) - V_{C3} + V_o \tag{2.27}$$

$$i_{k2}(t) = i_{m2}(\mathrm{t}) - ni_{sec}(t) = i_{sec}(t) \tag{2.28}$$

By manipulating (2.28), the secondary current i_{sec} can be expressed as

$$i_{sec}(t) = -i_{D4}(t) = -i_{k2}(t) = \frac{1}{n+1} i_{m2}(t) \tag{2.29}$$

Then,

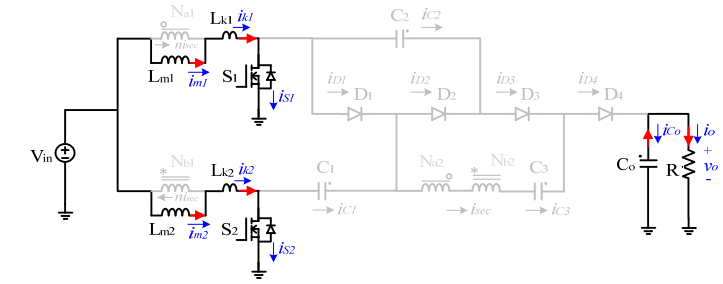
$$i_{k1}(t) = i_{m1}(t) + ni_{sec}(t) = i_{m1}(t) + \frac{n}{n+1} i_{m2}(t) \tag{2.30}$$

Solving (2.25)-(2.27), v_{m2} in this mode can be derived as

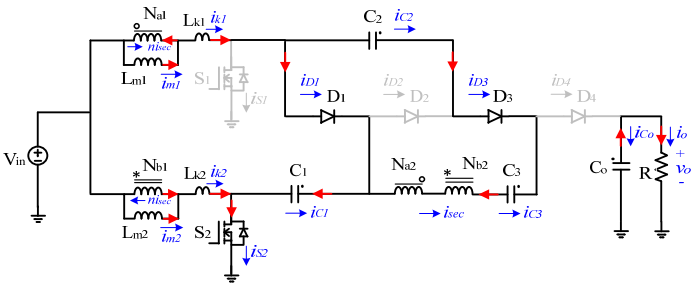
$$v_{m2} = V_{in} + V_{C1} - V_{C2} \tag{2.31}$$

Mode 8 [t_7 - t_0]: At t_7, S_2 is turned on, as shown in Fig. 2.4 (h). As the leakage inductances limit the current changing rate, ZCS of S_2 can be achieved. The current of D_4 is decreasing, and the falling rate is determined by the leakage inductances, which alleviates the reverse recovery problem of D_4. The falling rate of D_4 is given by

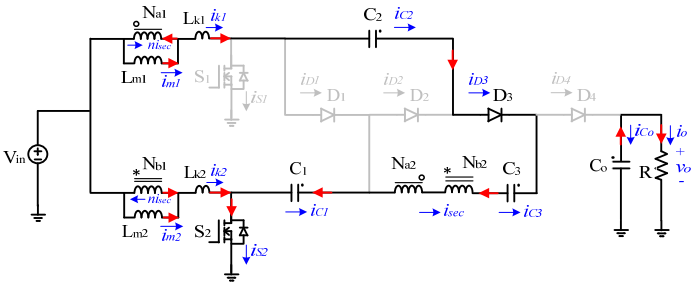
$$\frac{di_{D4}(t)}{dt} = -\frac{V_o - V_{C1} - V_{C3}}{n^2(L_{k1} + L_{k2})} \tag{2.32}$$


Na1
Lk1
ik1
C2
iC2
nsec
Lm1
im1
S1
iS1
iD1
D1
iD2
D2
iD3
D3
iD4
D4
Vin
iCo
io
Co
R
vo
Nb1
Lk2
ik2
C1
Na2
Nb2
C3
Lm2
im2
S2
iS2
iC1
isec
iC3

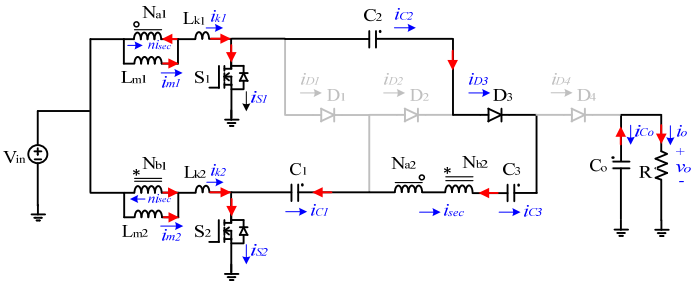
(a)


Na1
Lk1
ik1
C2
iC2
nsec
Lm1
im1
S1
iS1
iD1
D1
iD2
D2
iD3
D3
iD4
D4
Vin
iCo
io
Co
R
vo
Nb1
Lk2
ik2
C1
Na2
Nb2
C3
Lm2
im2
S2
iS2
iC1
isec
iC3

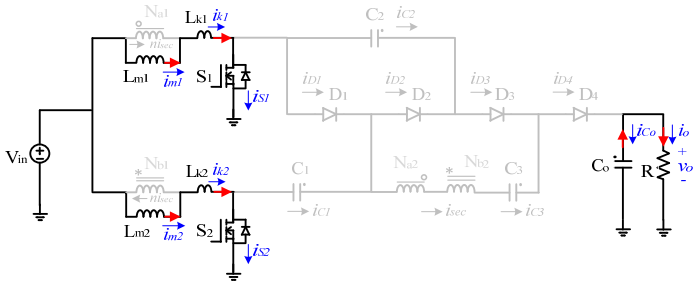
(b)


Na1
Lk1
ik1
C2
iC2
nsec
Lm1
im1
S1
iS1
iD1
D1
iD2
D2
iD3
D3
iD4
D4
Vin
iCo
io
Co
R
vo
Nb1
Lk2
ik2
C1
Na2
Nb2
C3
Lm2
im2
S2
iS2
iC1
isec
iC3

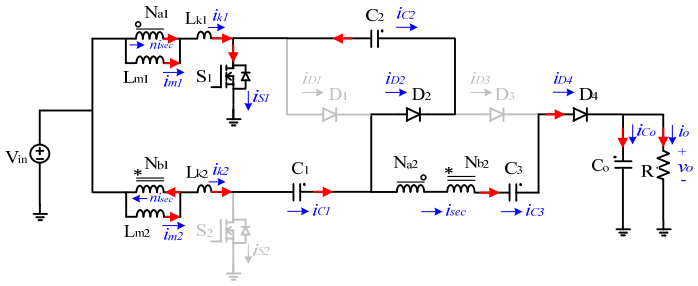
(c)


Na1
Lk1
ik1
C2
iC2
nsec
Lm1
im1
S1
iS1
iD1
D1
iD2
D2
iD3
D3
iD4
D4
Vin
iCo
io
Co
R
vo
Nb1
Lk2
ik2
C1
Na2
Nb2
C3
Lm2
im2
S2
iS2
iC1
isec
iC3

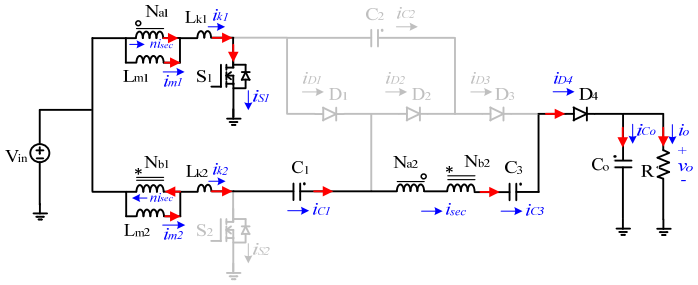
(d)



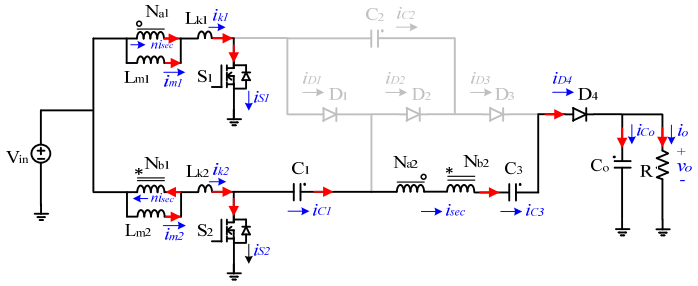
(e)



(f)



(g)



(h)

Fig. 2.4 Operation modes: (a) Mode 1 [t_0 - t_1]; (b) Mode 2 [t_1 - t_2]; (c) Mode 3 [t_2 - t_3]; (d) Mode 4 [t_3 - t_4]; (e) Mode 5 [t_4 - t_5]; (f) Mode 6 [t_5 - t_6]; (g) Mode 7 [t_6 - t_7]; (h) Mode 8 [t_7 - t_0].

2.2 Performance Analysis

A. Voltage gain

By applying the voltage-second balance principle to L_{m1} and L_{m2}, the following equations are obtained.

$$V_{in}D + (V_{in} - V_{C1})(1 - D) = 0 \quad (2.33)$$

$$V_{in}D + (V_{in} + V_{C1} - V_{C2})(1 - D) = 0 \quad (2.34)$$

Solving (2.33)-(2.34), the voltages V_{C1} and V_{C2} can be expressed as

$$V_{C1} = \frac{V_{in}}{1-D} \quad (2.35)$$

$$V_{C2} = \frac{2V_{in}}{1-D} \quad (2.36)$$

Substitute (2.35)-(2.36) to (2.10), V_{C3} can be derived as

$$V_{C3} = \frac{(n+2)V_{in}}{1-D} \quad (2.37)$$

Substitute (2.35)-(2.37) to (2.25), the voltage gain is derived as

$$M = \frac{V_o}{V_{in}} = \frac{2n+4}{1-D} \quad (2.38)$$

Fig. 2.5 shows the curves of the voltage gain versus duty cycle under different turns ratios. It can be seen that the proposed converter has a high step-up voltage gain without extreme duty cycle or high turns ratio.

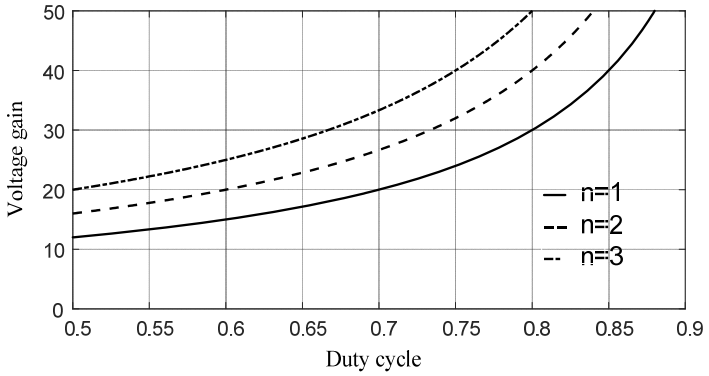


Fig. 2.5 Voltage gain versus duty cycle under different turns ratios

B. Voltage stress

The voltage stresses of the capacitors are given by

$$V_{C1} = \frac{V_o}{2n+4}; V_{C2} = \frac{V_o}{n+2}; V_{C3} = \frac{V_o}{2} \tag{2.39}$$

The voltage stresses of the switches can be derived as

$$V_{S1} = V_{S2} = \frac{V_{in}}{1-D} = \frac{1}{2n+4} V_o \tag{2.40}$$

It can be seen that the switch voltage stress is only one-sixth of the output voltage if the turns ratio is one. It becomes even lower when the turns ratio increases. The low voltage stress results in low switching loss. Furthermore, low-voltage-rating MOSFETs with small on-resistance are allowed to lower conduction loss.

The voltage stresses of the diodes are determined by the capacitor voltages. They are given by

$$V_{D1} = V_{D2} = \frac{1}{n+2} V_o; V_{D3} = V_{D4} = \frac{n+1}{n+2} V_o \tag{2.41}$$

The normalized voltage versus turns ratios are shown in Fig. 2.6. It can be seen that the switch voltage stress becomes lower as the voltage gain is extended by increasing the turns ratio. The voltage stresses on D_1 and D_2 also decreases as the turns ratio increases. The voltage stresses on D_3 and D_4 increases as the turns ratio increases, but they are always lower than the output voltage. The voltage stress on C_3 is always half of the output voltage. The voltage stresses on C_1 and C_2 decreases as the turns ratio increases.

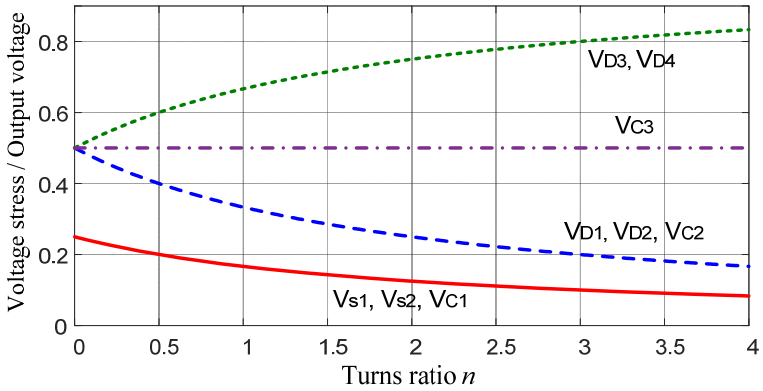


Fig. 2.6 Normalized voltage stress versus turns ratios

C. Current sharing

The average magnetizing currents are assumed as I_{m1} and I_{m2} by applying small-ripple approximation. Let $t_2 - t_1 = D_a T_s$ and $t_6 - t_5 = D_b T_s$. Ignoring mode 4 and mode 8, the current waveforms of the capacitors are shown in Fig. 2.7. According to the charge balance of capacitor C_1~C_3, the following equations are obtained.

$$\frac{1}{2}\left(I_{m1} + \frac{I_{m1}}{n+1}\right)D_a + \frac{I_{m1}}{n+1}(1 - D - D_a) = \frac{1}{2}\left(I_{m2} + \frac{I_{m2}}{n+1}\right)D_b + \frac{I_{m2}}{n+1}(1 - D - D_b) \quad (2.42)$$

$$\frac{1}{2}\cdot\frac{I_{m1}}{n+1}D_a + \frac{I_{m1}}{n+1}(1\text{-}D\text{-}D_a) = \frac{1}{2}I_{m2}D_b \quad (2.43)$$

$$\frac{1}{2}\cdot\frac{I_{m1}}{n+1}D_a + \frac{I_{m1}}{n+1}(1\text{-}D\text{-}D_a) = \frac{1}{2}\cdot\frac{I_{m2}}{n+1}D_b + \frac{I_{m2}}{n+1}(1\text{-}D\text{-}D_b) \quad (2.44)$$

Solving (2.42)-(2.44), the following relationships can be obtained.

$$I_{m1} = I_{m2} \tag{2.45}$$

$$D_a = D_b = \frac{2}{n+2}(1-D) \tag{2.46}$$

It can be seen that the magnetizing currents of the two coupled inductors are balanced due to the charge balance of the capacitors.

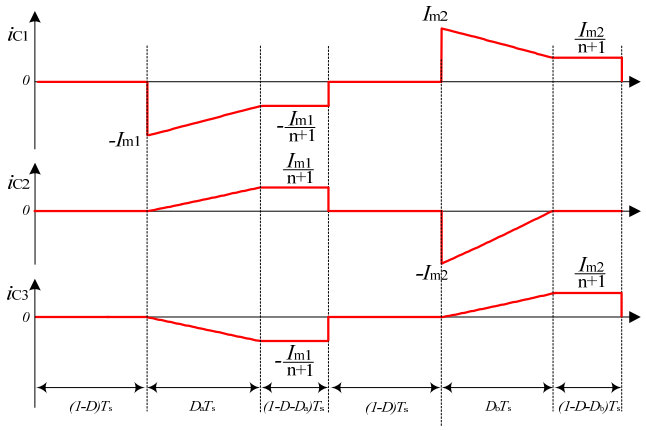


Fig. 2.7 Current waveforms of the capacitors

Assume $I_{m1} = I_{m2} = I_m$. The following equation can be derived according to the charge balance of C_o.

$$\left(\frac{1}{2}\cdot\frac{I_m}{n+1} - I_o\right)D_b + \left(\frac{I_m}{n+1} - I_o\right)(1-D-D_b) = I_o D \tag{2.47}$$

Substitute (2.46) to (2.47), the magnetizing current can be expressed as

$$I_m = \frac{n+2}{1-D} I_o \tag{2.48}$$

The secondary windings of the coupled inductors are connected in series in the proposed converter, thus they share the same secondary current. The average current flowing through L_{k1} can be evaluated as

$$I_{Lk1} = \frac{1}{T_s}\left(\int_0^{(D-0.5)T_s} i_{m1}dt + \int_{(D-0.5)T_s}^{0.5T_s}(i_{m1} + ni_{sec})dt + \int_{0.5T_s}^{DT_s} i_{m1}dt + \int_{DT_s}^{T_s}(i_{m1} + ni_{sec})dt\right) = I_m \quad (2.49)$$

The average current flowing through L_{k2} can be evaluated as

$$I_{Lk2} = \frac{1}{T_s}\left(\int_0^{(D-0.5)T_s} i_{m2}dt + \int_{(D-0.5)T_s}^{0.5T_s}(i_{m2} - ni_{sec})dt + \int_{0.5T_s}^{DT_s} i_{m2}dt + \int_{DT_s}^{T_s}(i_{m2} - ni_{sec})dt\right) = I_m \quad (2.50)$$

From (2.49) and (2.50), it can be seen that the primary currents of the coupled inductors are balanced.

D. Input current ripple

The input current of the proposed converter equals to the sum of the primary currents of the coupled inductors. Since the coupled inductors share the same secondary current, the input current can be derived as

$$i_{in} = (i_{m1} + ni_{sec}) + (i_{m2} - ni_{sec}) = i_{m1} + i_{m2} \quad (2.51)$$

From the operation principle, it can be seen that the magnetizing currents have an interleaved feature. The frequency of the input current ripple is twice of the switching frequency. Therefore, the input current is continuous and the ripple is significantly reduced.

The peak-to-peak ripple of the magnetizing current is given by

$$\Delta i_{Lm} = \frac{V_{in}D}{L_m f_s} \quad (2.52)$$

The peak-to-peak ripple of the input current is given by

$$\Delta i_{in} = \frac{V_{in}(2D-1)}{L_m f_s} \tag{2.53}$$

The input current ripple normalized to the magnetizing current ripple is illustrated in Fig. 2.8. It can be seen that smaller duty cycle results in better ripple cancellation effect. Also as seen from (2.52) and (2.53), smaller duty cycle leads to lower magnetizing current ripple and input current ripple. Thus, the size of the coupled inductor can be reduced and the current stress of the input capacitor can be alleviated, which help improve the power density.

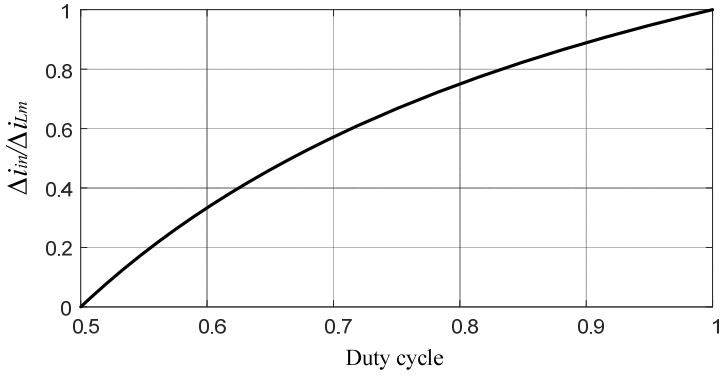


Fig. 2.8 Normalized input current ripple versus duty cycle

E. Voltage gain considering parasitic elements

Similar to the conventional boost converter, the voltage gain of the proposed converter would deviate from the ideal value if parasitic elements are considered, especially under extreme duty cycles. The equivalent circuit including parasitic elements is illustrated in Fig. 2.9. In order to simplify calculation, it is assumed that the two switches have identical on-resistance r_{on}, the two coupled inductors have identical primary resistance r_{pri} and identical secondary resistance r_{sec}, all capacitors have the same equivalent series resistance

r_c, and all diodes have the same forward voltage drop V_d. Besides, small ripple approximation is used and mode 4 and mode 8 are ignored in the calculation.

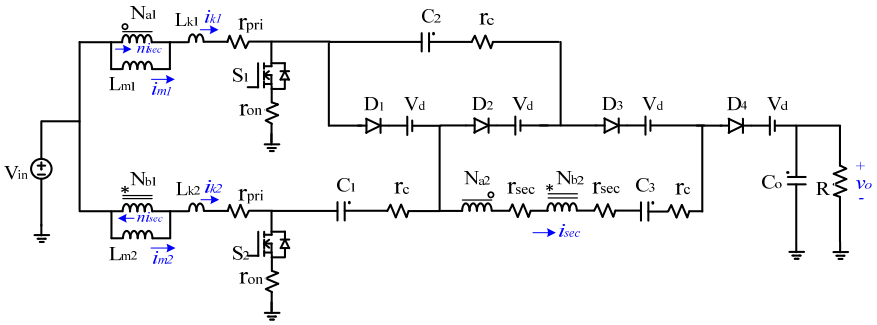


Fig. 2.9 Equivalent circuit including parasitic elements

By applying the voltage-second balance principle to L_{m1} and L_{m2}, the voltage gain considering parasitic elements can be solved as

$$\frac{V_o}{V_{in}} = \frac{\frac{2n+4}{1-D} - \frac{4V_d}{V_{in}}}{1+\frac{n+2}{(n+1)^2(1-D)}\left(U\frac{r_{on}}{R}+V\frac{r_{pri}}{R}+W\frac{r_{sec}}{R}+Z\frac{r_c}{R}\right)} \tag{2.54}$$

where

$$U = 7n^3 + 23n^2 + 28n + 11 + \frac{2(n+1)^2(n+2)(2D-1)}{1-D}$$

$$V = 8n^3 + 18n^2 + 20n + 8 + \frac{2(n+1)^2(n+2)(2D-1)}{1-D}$$

$$W = 4n + 2$$

$$Z = 1.5n^2 + 10n + 6$$

As discussed earlier, the ideal voltage gain of the proposed converter is independent of the load conditions. However, if the parasitic elements are considered, under given

parasitic parameters, the voltage gain would decrease as the load increases, and the voltage gain would collapse under extreme duty cycles, as shown in Fig. 2.10.

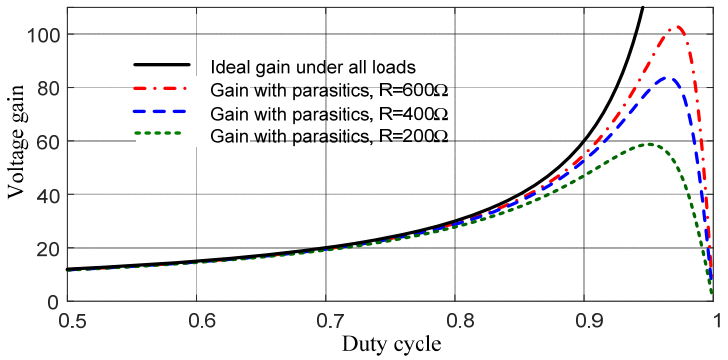


Fig. 2.10 Voltage gain with parasitic elements ($r_{on} = 7.5m\Omega$, $r_{pri} = 20m\Omega$, $r_{sec} = 45m\Omega$, $r_c = 8m\Omega$, $V_d = 0.75V$, $n = 1$, V_{in}=20V)

F. Comparison

The proposed converter is compared with other similar converters in the literature. All the converters have an input interleaved operation and can be used in high step-up applications. The voltage gain, normalized voltage stresses of the switches and diodes, the number of components, common ground connection, and current sharing performance are listed in Table 2.1.

It can be seen from Table 2.1 that the proposed converter achieves highest voltage gain with low component count among its counterparts. Also, lowest switch voltage stress is achieved, hence, low-voltage-rating MOSFETs with small on-resistance are allowed to lower the conduction loss. Furthermore, the proposed converter has the features of common ground connection and balanced current sharing, which are important in real applications such as renewable energy system. and UPS systems.

Table 2.1 Comparison with other interleaved coupled-inductor converters

Topology	Switch	/Diode	/Core	/Winding	/Cap.	Voltage gain	Switch voltage stress	Max. diode voltage stress	Common ground?	Balanced current sharing?
[15]	2	4	2	4	3	$\frac{2n+1}{1-D}$	$\frac{1}{2n+1}$	$\frac{2n}{2n+1}$	Yes	Yes
[16]	2	4	2	4	3	$\frac{2n+1}{1-D}$	$\frac{1}{2n+1}$	$\frac{2n}{2n+1}$	Yes	Yes
[17]	2	4	2	4	4	$\frac{2n+2}{1-D}$	$\frac{1}{2n+2}$	$\frac{2n}{2n+2}$	Yes	Yes
[18]	2	6	2	4	5	$\frac{2n+2}{1-D}$	$\frac{1}{2n+2}$	$\frac{2n}{2n+2}$	Yes	Yes
[19]	2	4	2	4	4	$\frac{2n+3}{1-D}$	$\frac{1}{2n+3}$	$\frac{2n+1}{2n+3}$	Yes	No
[20]	2	6	2	4	4	$\frac{2n+2}{1-D}$	$\frac{1}{2n+2}$	$\frac{2n}{2n+2}$	No	Yes
[21]	4	2	2	4	3	$\frac{2n+2}{1-D}$	$\frac{1}{2n+2}$	$\frac{2n+1}{2n+2}$	Yes	Yes
[22]	4	4	2	4	5	$\frac{(1+D)n+2}{1-D}$	$\frac{1}{(1+D)n+2}$	--	Yes	Yes
[23]	4	4	3	5	5	$\frac{2n+2}{1-D}$	$\frac{1}{2n+2}$	1	Yes	Yes
[24]	2	6	3	5	5	$\frac{2n+2}{1-D}$	$\frac{1}{2n+2}$	$\frac{2n+1}{2n+2}$	Yes	Yes
[25]	2	4	3	5	3	$\frac{n+2}{1-D}$	$\frac{1}{n+2}$	1	Yes	Yes
[26]	2	4	2	6	3	$\frac{n+1}{1-D}$	$\frac{1}{n+1}$	$\frac{2n}{n+1}$	Yes	Yes
[27]	2	6	2	6	5	$\frac{2n+2}{1-D}$	$\frac{1}{2n+2}$	$\frac{2n+1}{2n+2}$	Yes	Yes
[28]	2	6	2	6	5	$\frac{(1+D)n+2-D}{1-D}$	$\frac{1}{(1+D)n+2-D}$	$\frac{n}{(1+D)n+2-D}$	Yes	Yes
[29]	4	6	2	6	5	$\frac{2n+2}{1-D}$	$\frac{1}{2n+2}$	$\frac{2n+1}{2n+2}$	Yes	Yes
Proposed	2	4	2	4	4	$\frac{2n+4}{1-D}$ (highest)	$\frac{1}{2n+4}$ (lowest)	$\frac{2n+2}{2n+4}$ (medium)	Yes	Yes

2.3 Design Considerations

A. Coupled-inductor design

From the aforementioned analysis, the duty cycle should be selected greater than 0.5. Extreme duty cycle must be avoided since the voltage gain could collapse. Once proper duty cycle is selected, the turns ratio of the coupled inductors is determined by the required voltage gain. It is given by

$$n = \frac{V_o}{V_{in}} \cdot \frac{1-D}{2} - 2 \tag{2.55}$$

The magnetizing inductances of the coupled inductors can be designed based on the magnetizing current ripple, which is also closely related to the input current ripple. The magnetizing inductance can be calculated by

$$L_m = L_{m1} = L_{m2} = \frac{V_{in}D}{\Delta i_{Lm} f_s} = \frac{V_{in}(2D-1)}{\Delta i_{in} f_s} \tag{2.56}$$

The converter is designed to be operated in CCM. The minimum magnetizing inductance value for the CCM operation is given by

$$L_m > L_{m\_crit} = \frac{V_{in}D(1-D)}{2(n+2)I_o f_s} \tag{2.57}$$

The leakage inductances of the coupled inductors help alleviate the diode reverse recovery problem. Thus, the leakage inductances can be designed based on the current falling rate of the diodes, which are given by

$$L_k = L_{k1} = L_{k2} = \frac{(n+1)V_o}{4n^2(n+2)\frac{di_{D3}}{dt}} = \frac{(n+1)V_o}{4n^2(n+2)\frac{di_{D4}}{dt}} \tag{2.58}$$

The peak currents of the coupled inductors are given by

$$I_{k1\_pk} = I_{k2\_pk} = \frac{(2n+1)}{(n+1)} I_m = \frac{(2n+1)(n+2)}{(n+1)(1-D)} I_o \tag{2.59}$$

The RMS currents of the primary windings are given by

$$I_{k1\_RMS} = I_{k2\_RMS} = \frac{n+2}{1-D} I_o \sqrt{\frac{2(6n^3+14n^2+15n+6)(1-D)}{3(n+2)(n+1)^2} + 2D - 1} \quad (2.60)$$

The RMS currents of the secondary windings are given by

$$I_{sec\_RMS} = I_o \sqrt{\frac{2(n+2)(3n+2)}{3(n+1)^2(1-D)}} \quad (2.61)$$

B. Semiconductor selection

The switches and diodes are chosen based on the voltage and current stresses. The voltage stresses of the switches and diodes can be calculated from (2.40) and (2.41). The RMS current stresses of the switches are given by

$$I_{S1\_RMS} = \frac{n+2}{1-D} I_o \sqrt{2D - 1 - \frac{(1-D)(4n^3+12n^2+13n+4.67)}{(n+2)(n+1)^2}} \quad (2.62)$$

$$I_{S2\_RMS} = \frac{n+2}{1-D} I_o \sqrt{3 - 2D} \quad (2.63)$$

The average currents flowing through the diodes are given by

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_o \quad (2.64)$$

C. Capacitor design

The capacitors are used to transfer energy from the input to the output. They are designed based on the voltage ripple $r\%$ and the output power P_o. The calculations of the capacitors are given by

$$C_1 = \frac{(2n+4)P_o}{r\%{V_o}^2 f_s}; C_2 = \frac{(n+2)P_o}{r\%{V_o}^2 f_s}; \; C_3 = \frac{2P_o}{r\%{V_o}^2 f_s} \quad (2.65)$$

Generally, capacitors with low ESR are preferred in order to reduce power losses. It is a favorable solution that film capacitors or multilayer chip-type ceramic capacitors are adopted. Moreover, multiple capacitors can be connected in parallel to reduce ESR.

2.4 Experimental Results

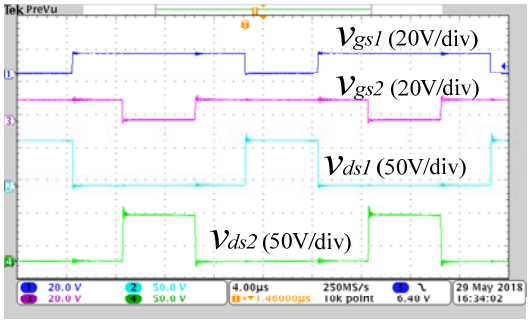
A prototype with 20V input and 400V output was built in order to verify the performance of the proposed converter. The key parameters of the prototype are listed as in Table 2.2.

Table 2.2 Key parameters of the prototype

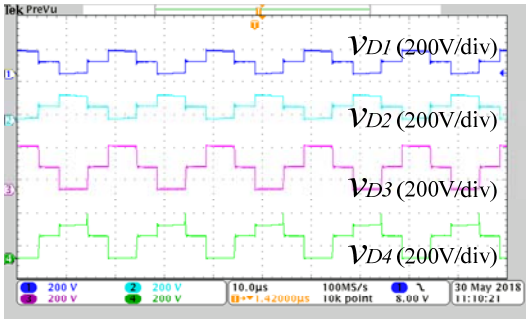
Parameters	Value/Description
Input voltage	20V
Output voltage	400V
Input current	16A
Switching frequency	50kHz
Switches S_1-S_2	IPA075N15N3 (150V)
Diodes D_1, D_2	STPS20200CT (200V)
Diodes D_3, D_4	TST20H300CW (300V)
Coupled inductors	Turns ratio = 1:1 Magnetizing inductance = 100uH Leakage inductance = 3.5uH
Capacitor C_1	22uF Film capacitor
Capacitor C_2, C_3	8.2uF Film capacitor
Capacitor C_o	2 ×56uF electrolytic capacitor

Fig. 2.11 (a) shows the interleaved driving signals and the drain-to-source voltages of the switches. The duty cycles of the switches are around 0.7. The voltage stresses of the switches are clamped at around 68V, which is much lower than the output voltage. Fig. 2.11 (b) shows the voltages of the diodes. As can be seen, the blocking voltages of D_1 and D_2 are around 136V and the blocking voltages of D_3 and D_4 are around 268V, which match the calculations from (2.41). Fig. 2.11 (c) shows that the input voltage is 20V and

the output voltage is 400V. Therefore, high voltage gain is achieved even when the turns ratio is 1. Fig. 2.11 (d) shows the voltages across the capacitors. It can be seen that V_{C1}, V_{C2} and V_{C3} are around 68V, 136V and 200V, respectively, which are consistent with the calculations from (2.39). Fig. 2.11 (e) shows the currents through the diodes. It can be seen that the reverse recovery problems of the diodes are alleviated. Fig. 2.11 (f) gives the primary currents of the coupled inductors and the input current. It can be seen that balanced primary current sharing is achieved. The frequency of the input current ripple is twice the switching frequency, and the input current ripple is significantly reduced due to the interleaved operation. The measured efficiency of the prototype is shown in Fig. 2.11 (g). The peak efficiency is 94.9%. At full load, the efficiency is 94.7%. Loss breakdown based on the prototype at full load is provided in Fig. 2.11 (h). It can be seen that the dominant power losses are the coupled-inductor loss, the diode loss and the switch loss. More coppers can be used in the coupled inductor to further improve the efficiency of the proposed converter.



(a)



(b)

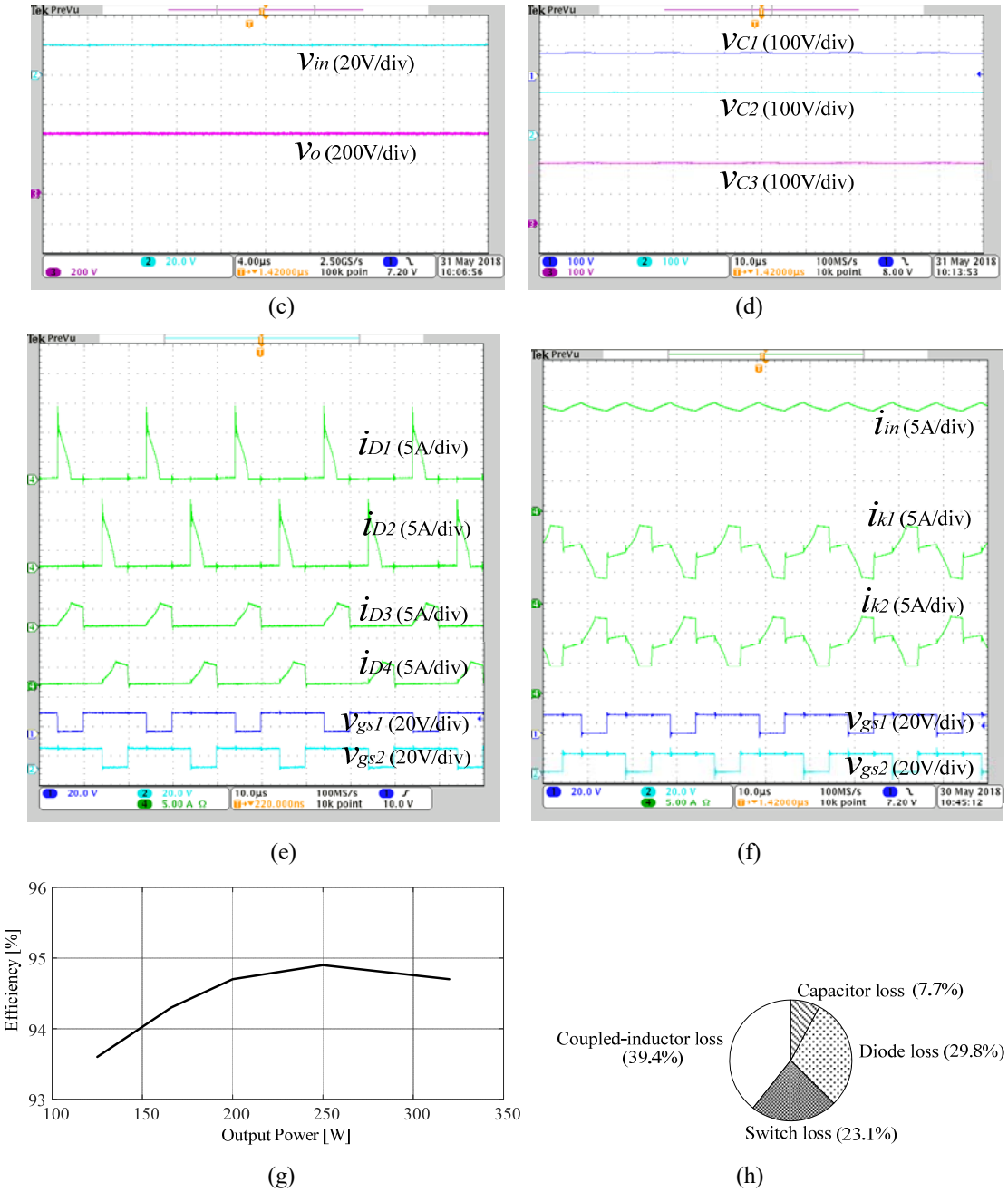


Fig. 2.11 Experimental results: (a) driving signals and switch voltages; (b) diode voltage; (c) input and output voltages; (d) capacitor voltages; (e) diode currents; (f) primary currents of coupled inductors and the input current; (g) efficiency; (h) loss breakdown.

2.5 Topologies Extensions and Variations

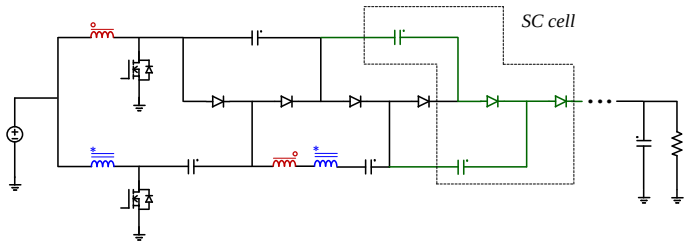
In higher step-up applications, switched capacitor (SC) cells shown in Fig. 2.12 (a) can be added to the basic topology in order to further extend the voltage gain and reduce the switch voltage stress. If one SC cell is added, the new voltage gain can be expressed as

$$\frac{V_o}{V_{in}} = \frac{4n+6}{1-D} \tag{2.66}$$

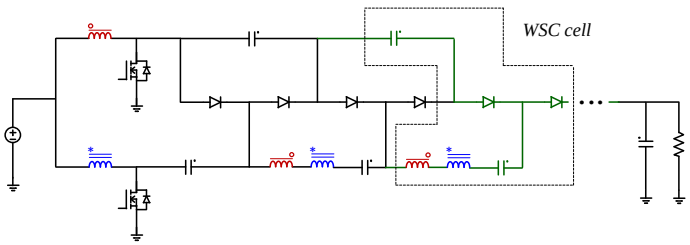
Another extension is to employ coupled inductor with multiple windings. Winding-based switched-capacitor (WSC) cell shown in Fig. 2.12 (b) can be added. The extra windings provide an extra degree of freedom, thus more flexible voltage gain can be achieved. If one WSC cell is added, the new voltage gain can be expressed as

$$\frac{V_o}{V_{in}} = \frac{4n+2n'+6}{1-D} \tag{2.67}$$

where $n = N_{a1}/N_{a0} = N_{b1}/N_{b0}$ and $n' = N_{a2}/N_{a0} = N_{b2}/N_{b0}$.



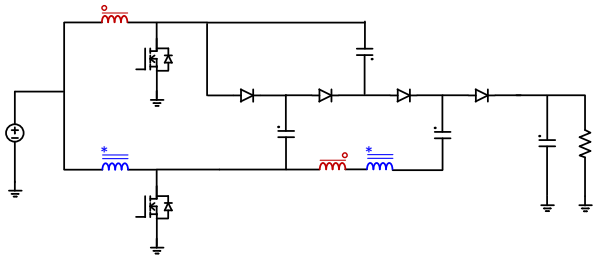
(a)



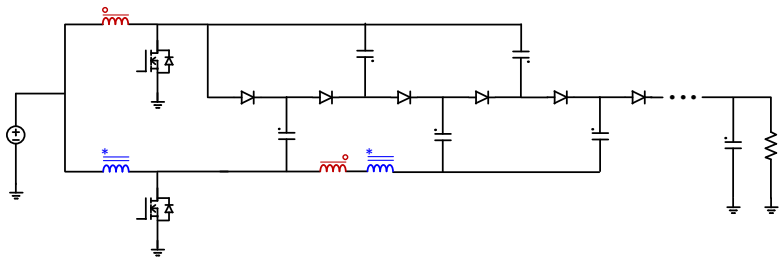
(b)

Fig. 2.12 Topology extension: (a) by adding SC cells; (b) by adding WSC cells.

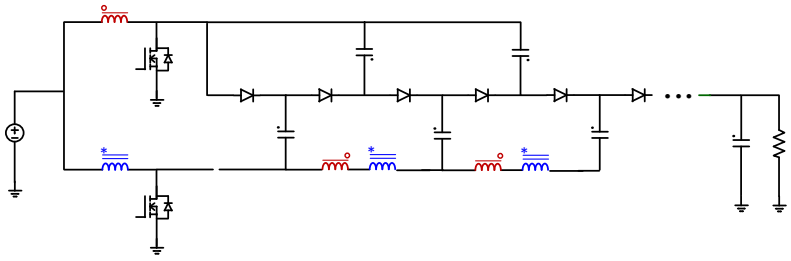
The secondary windings and the capacitors can also be placed in different positions, which leads to different topology variations, as shown in Fig. 2.13-Fig 2.15. All these topologies can easily achieve high voltage gain without extreme duty cycle or high turns ratio. Also, low semiconductor voltage stresses are obtained, thus, low-voltage-rating semiconductor devices can be used to reduce the conduction loss and switching loss. Moreover, balanced input current sharing and low input current ripple can be achieved. In addition, the leakage energy can be recycled and additional clamp circuit is not required.



(a)

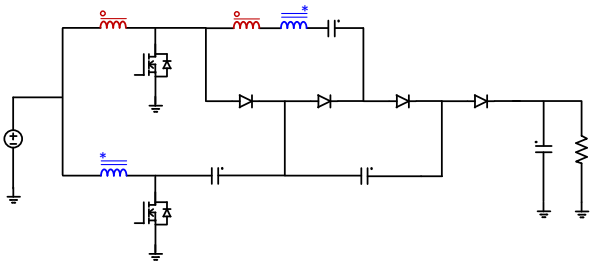


(b)

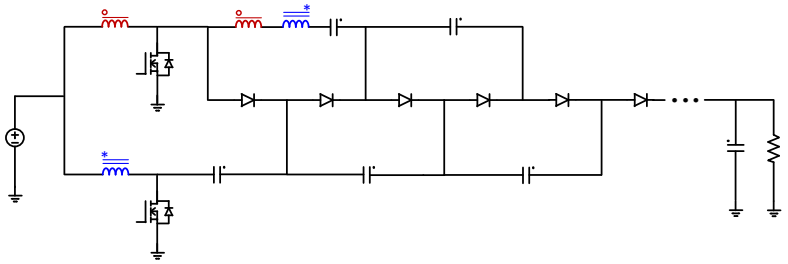


(c)

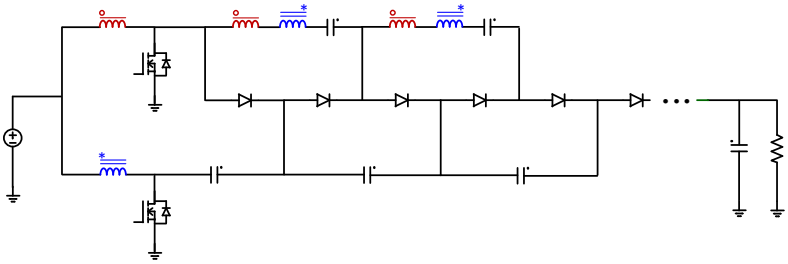
Fig. 2.13 Topology variation 1



(a)

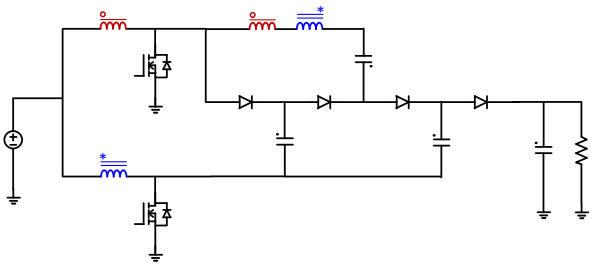


(b)

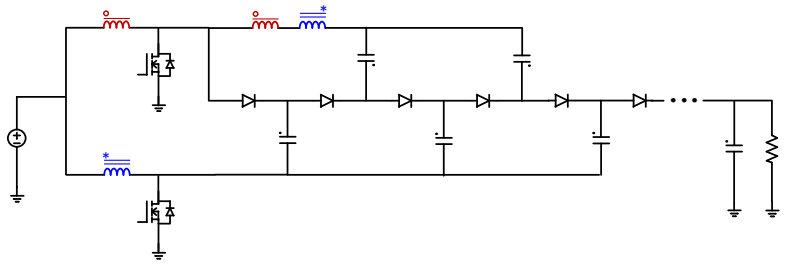


(c)

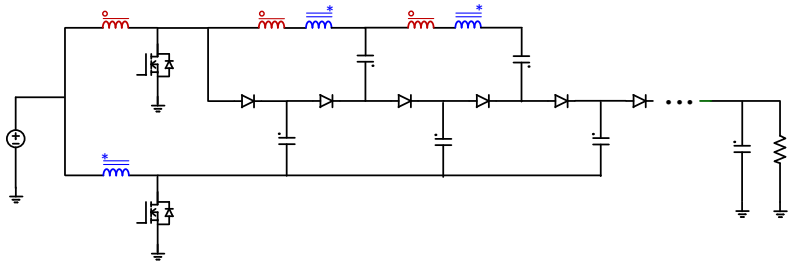
Fig. 2.14 Topology variation 2



(a)



(b)



(c)

Fig. 2.15 Topology variation 3

2.6 High Step-Down Extension

The proposed high step-up family can be extended to high step-down operation by replacing all the diodes with switches. One example is shown in Fig. 2.16. The power source is connected at high side and the load is connected at low side. Switch S_1~S_2 are triggered by interleaved PWM. Switch Q_1 and S_2 are driven complementary with a dead time, so are switch Q_2 and S_1. Switch Q_3 and Q_1 are driven synchronously, so are switch Q_4 and Q_2. With such a modulation scheme, a high step-down conversion can be achieved.

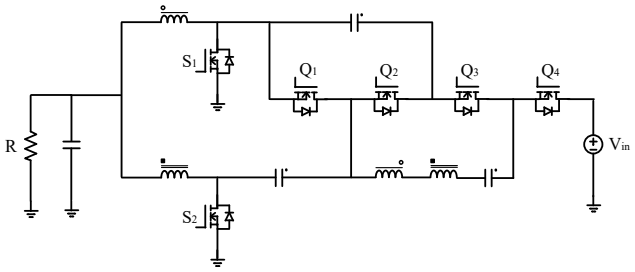


Fig. 2.16 One example of high step-down extension

Chapter 3 Multiphase Interleaved High Step-Up Converter with Diode-Capacitor Voltage Multiplier Stages

In this chapter, multiphase diode-capacitor based high step-up converters (DCHSC) is presented. It is derived by integration of the multiphase EDR boost converter with diode-capacitor VM stages. It can also be viewed as an extension of the current-fed CW multiplier [32] to multiphase (phase number >2) configuration. The family has the following features: 1) multiphase interleaving structure at the input side reduces the input current ripple and increases the current handling capability; 2) diode-capacitor voltage multiplier stages at the output side help achieve a high step-up voltage gain; 3) the switches and diodes have low voltage stresses, leading to reduced switching loss and facilitating the use of low-voltage-rating semiconductor devices to lower the conduction loss; 4) automatic current balancing among the phases can be achieved, thus extra current sharing circuit is not required; 5) soft charging and discharging of the energy transfer capacitors are achieved. In comparison to [32], the multiphase extension achieves higher voltage gain, higher current handling capability, lower switch voltage stress and lower current ripple.

A three-phase converter in the family is analyzed and evaluated in detail in this chapter. The topology and operation principles are described in Section 3.1. Performance

analysis is made in Section 3.2. Design considerations are discussed in Section 3.3. Simulation and experimental results are presented in Section 3.4.

3.1 Topology and Operation Principles

The proposed *n*-phase *m*-stage (*n*P*m*S) DCHSC is shown in Fig. 3.1 (a). It is configured by an *n*-phase extended-duty-ratio boost stage integrated with *m* diode-capacitor VM stages, where *n*=2, 3, 4, … and *m*=1, 2, 3, …. Each VM stage is shown in Fig. 1 (b). It is composed of *n* basic diode-capacitor cells as in Fig. 1 (c): in each VM stage, the *n* diodes are connected in series and one terminal of each capacitor is connected to each phase. The *n*P*m*S DCHSC consists of *n* inductors, *n* low-side switches, *n*(*m*+1) diodes, *n*-1 series capacitors in the series capacitor boost stage, $n \times m$ flying capacitors in the VM stages and one output filter capacitor. The number of phases shall be determined according to the current rating of the applications. The number of VM stages shall be determined by the voltage gain required in the applications. The switches are operated in an interleaved manner, i.e. the gate signals are phase shifted by $360^{o}/n$. In this chapter, the 3P1S DCHSC, as shown in Fig. 3.2, is analyzed and evaluated in detail. Similar analysis can be expanded to *n*P*m*S DCHSC in the family. To facilitate the explanation of the circuits' operation, assume the filter capacitor is large enough so that the output can be modeled as a voltage source V_o.

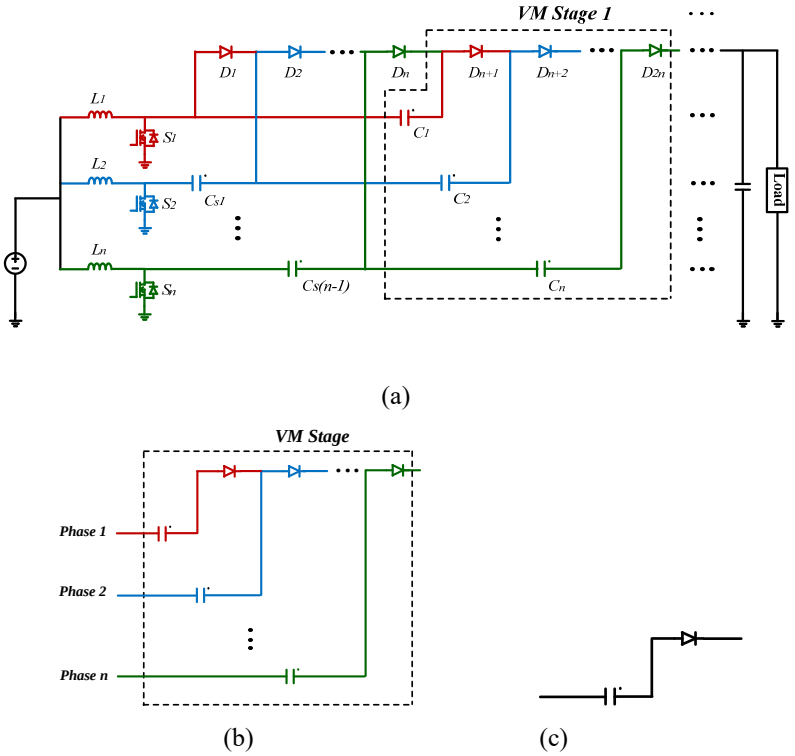


Fig. 3.1 Proposed configuration: (a) nPmS DCHSC; (b) one VM stage; (c) basic diode-capacitor cell.

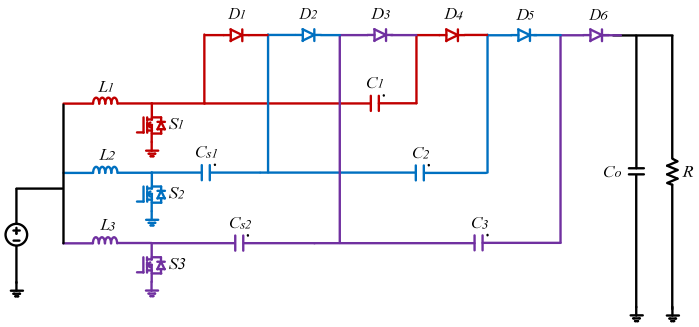


Fig. 3.2 3P1S DCHSC.

In order to simplify analysis, the following assumptions are made: 1) all the capacitors are large enough so that the voltages across them are constant with negligible ripples; 2) all switches and diodes are ideal; 3) the duty cycle *D* of all switches are the same; 4) the converter is operating in continuous conduction mode (CCM).

A. 2/3<*D*<1

The switching signals of 3P1S DCHSC with 2/3<*D*<1 are shown in Fig. 3.3. Six modes can be observed in one switching period.

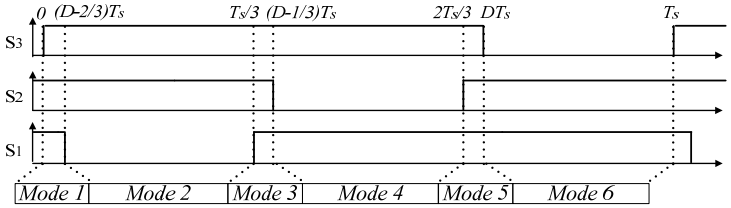


Fig. 3.3 Switching signals of 3P1S DCHSC when 2/3<D<1.

Mode 1: All switches are on. All inductors are charged by the input source. All diodes are reversed-biased. All series capacitor and flying capacitors are floating. The equivalent circuit is shown in Fig. 3.4 (a). The following equations can be obtained.

$$V_{in} = L_1 \frac{di_{L1}}{dt} \tag{3.1}$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} \tag{3.2}$$

$$V_{in} = L_3 \frac{di_{L3}}{dt} \tag{3.3}$$

Mode 2: Switch S_1 is turned off, and S_2 and S_3 are on. Inductor L_2 and L_3 are charged by the input source while inductor L_1 is releasing energy, as shown in Fig. 3.4 (b). Charges from L_1 flow through D_1 and D_4, thereby, capacitor C_1 is discharged, and capacitor C_2 and C_{s1} are charged. The following equations can be obtained.

$$V_{in} = L_1 \frac{di_{L1}}{dt} + V_{Cs1} \tag{3.4}$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} \tag{3.5}$$

$$V_{in} = L_3 \frac{di_{L3}}{dt} \tag{3.6}$$

$$V_{C1} = V_{C2} \tag{3.7}$$

Mode 3: This mode repeats mode 1.

Mode 4: Switch S_2 is turned off, and S_1 and S_3 are on. Inductor L_1 and L_3 are charged by the input source while inductor L_2 is releasing energy, as shown in Fig. 3.4 (c). Charges from L_2 flow through D_2 and D_5, thereby, capacitor C_{s1} and C_2 are discharged, and capacitor C_3 and C_{s2} are charged. The following equations can be obtained.

$$V_{in} = L_1 \frac{di_{L1}}{dt} \tag{3.8}$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} - V_{Cs1} + V_{Cs2} \tag{3.9}$$

$$V_{in} = L_3 \frac{di_{L3}}{dt} \tag{3.10}$$

$$V_{C2} = V_{C3} \tag{3.11}$$

Mode 5: This mode repeats mode 1.

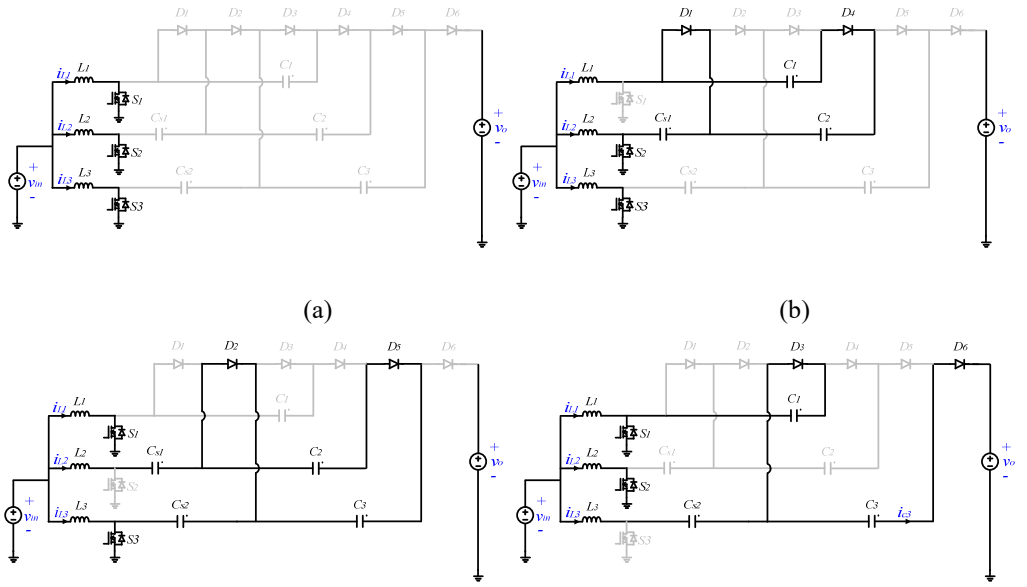
Mode 6: Switch S_3 is turned off, and S_1 and S_2 are on. Inductor L_1 and L_2 are charged by the input source while inductor L_3 is releasing energy, as shown in Fig. 3.4 (d). Charges from L_3 flow through D_3 and D_6, thereby, capacitor C_{s2} and C_3 are discharged, and capacitor C_1 is charged. The following equations can be obtained.

$$V_{in} = L_1 \frac{di_{L1}}{dt} \tag{3.12}$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} \tag{3.13}$$

$$V_{in} = L_3 \frac{di_{L3}}{dt} - V_{Cs2} + V_{C1} \tag{3.14}$$

$$V_o = V_{C1} + V_{C3} \tag{3.15}$$



(a) (b)

(c) (d)

Fig. 3.4 Operation of 3P1S DCHSC with 2/3<D<1: (a) Mode 1, 3 and 5; (b) Mode 2; (c) Mode 4; (d) Mode 6.

By applying the voltage-second balance principle to the three boost inductors of 3P1S DCHSC, the voltage gain of 3P1S DCHSC is derived as

$$\frac{V_o}{V_{in}} = \frac{6}{1-D}, (2/3<D<1) \tag{3.16}$$

The capacitor voltages can be obtained as

$$V_{Cs1} = \frac{V_{in}}{1-D} = \frac{V_o}{6} \tag{3.17}$$

$$V_{Cs2} = \frac{2V_{in}}{1-D} = \frac{V_o}{3} \tag{3.18}$$

$$V_{C1} = V_{C2} = V_{C3} = \frac{3V_{in}}{1-D} = \frac{V_o}{2} \tag{3.19}$$

The voltage stress of the switches can be calculated as

$$V_{S1} = V_{S2} = V_{S3} = \frac{1}{6}V_o \tag{3.20}$$

The voltage stress of the diodes are determined by the capacitor voltages. It is given by

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{D5} = V_o/3;\ V_{D6} = V_o/6 \tag{3.21}$$

B. *1*/3<*D*<2/3

The switching signals of 3P1S DCHSC with 1/3<*D*<2/3 are shown in Fig. 3.5. Six modes can be observed in one switching period.

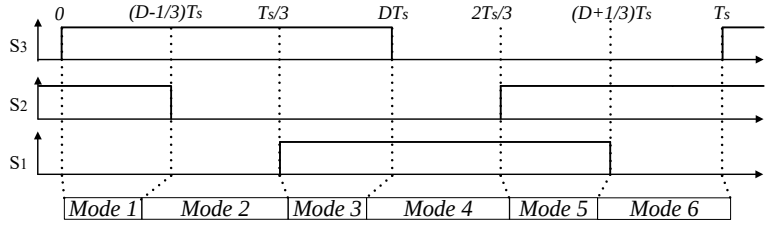


Fig. 3.5 Switching signals of 3P1S DCHSC when 1/3<*D*<2/3.

Mode 1: Switch S_1 is off, and S_2 and S_3 are on. Inductor L_2 and L_3 are charged by the input source while inductor L_1 is releasing energy, as shown in Fig. 3.6 (a). Charges from L_1 flow through D_1 and D_4. The following equations can be obtained.

$$V_{in} = L_1 \frac{di_{L1}}{dt} + V_{Cs1} \tag{3.22}$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} \tag{3.23}$$

$$V_{in} = L_3 \frac{di_{L3}}{dt} \tag{3.24}$$

$$V_{C1} = V_{C2} \tag{3.25}$$

Mode 2: Switch S_1 and S_2 are off, and S_3 is on. Inductor L_3 is charged by the input source while inductor L_1 and L_2 are releasing energy, as shown in Fig. 3.6 (b). Charges

from L_1 flow through D_1, D_2, D_4 and D_5, and charges from L_2 flow through D_2 and D_5. The following equations can be obtained.

$$V_{in} = L_1 \frac{di_{L1}}{dt} + V_{Cs2} \tag{3.26}$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} - V_{Cs1} + V_{Cs2} \tag{3.27}$$

$$V_{in} = L_3 \frac{di_{L3}}{dt} \tag{3.28}$$

$$V_{C1} = V_{C2} = V_{C3} \tag{3.29}$$

Mode 3: Switch S_2 is off, and S_1 and S_3 are on. Inductor L_1 and L_3 are charged by the input source while inductor L_2 is releasing energy, as shown in Fig. 3.6 (c). Charges from L_2 flow through D_2 and D_5. The following equations can be obtained.

$$V_{in} = L_1 \frac{di_{L1}}{dt} \tag{3.30}$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} - V_{Cs1} + V_{Cs2} \tag{3.31}$$

$$V_{in} = L_3 \frac{di_{L3}}{dt} \tag{3.32}$$

$$V_{C2} = V_{C3} \tag{3.33}$$

Mode 4: Switch S_2 and S_3 are off, and S_1 is on. Inductor L_1 is charged by the input source while inductor L_2 and L_3 are releasing energy, as shown in Fig. 3.6 (d). Charges from L_2 flow through D_2, D_3, D_5 and D_6, and charges from L_3 flow through D_3 and D_6. The following equations can be obtained.

$$V_{in} = L_1 \frac{di_{L1}}{dt} \tag{3.34}$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} - V_{Cs1} + V_{C1} \tag{3.35}$$

$$V_{in} = L_3 \frac{di_{L3}}{dt} - V_{Cs2} + V_{C1} \tag{3.36}$$

$$V_o = V_{C1} + V_{C3} \tag{3.37}$$

Mode 5: Switch S_3 is off, and S_1 and S_2 are on. Inductor L_1 and L_2 are charged by the input source while inductor L_3 is releasing energy, as shown in Fig. 3.6 (e). Charges from L_3 flow through D_3 and D_6. The following equations can be obtained.

$$V_{in} = L_1 \frac{di_{L1}}{dt} \tag{3.38}$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} \tag{3.39}$$

$$V_{in} = L_3 \frac{di_{L3}}{dt} - V_{Cs2} + V_{C1} \tag{3.40}$$

$$V_o = V_{C1} + V_{C3} \tag{3.41}$$

Mode 6: Switch S_1 and S_3 are off, and S_2 is on. Inductor L_2 is charged by the input source while inductor L_1 and L_3 are releasing energy, as shown in Fig. 3.6 (f). Charges from L_1 flow through D_1 and D_4, and charges from L_3 flow through D_6. The following equations can be obtained.

$$V_{in} = L_1 \frac{di_{L1}}{dt} + V_{Cs1} \tag{3.42}$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} \tag{3.43}$$

$$V_{in} = L_3 \frac{di_{L3}}{dt} - V_{Cs2} - V_{C3} + V_o \tag{3.44}$$

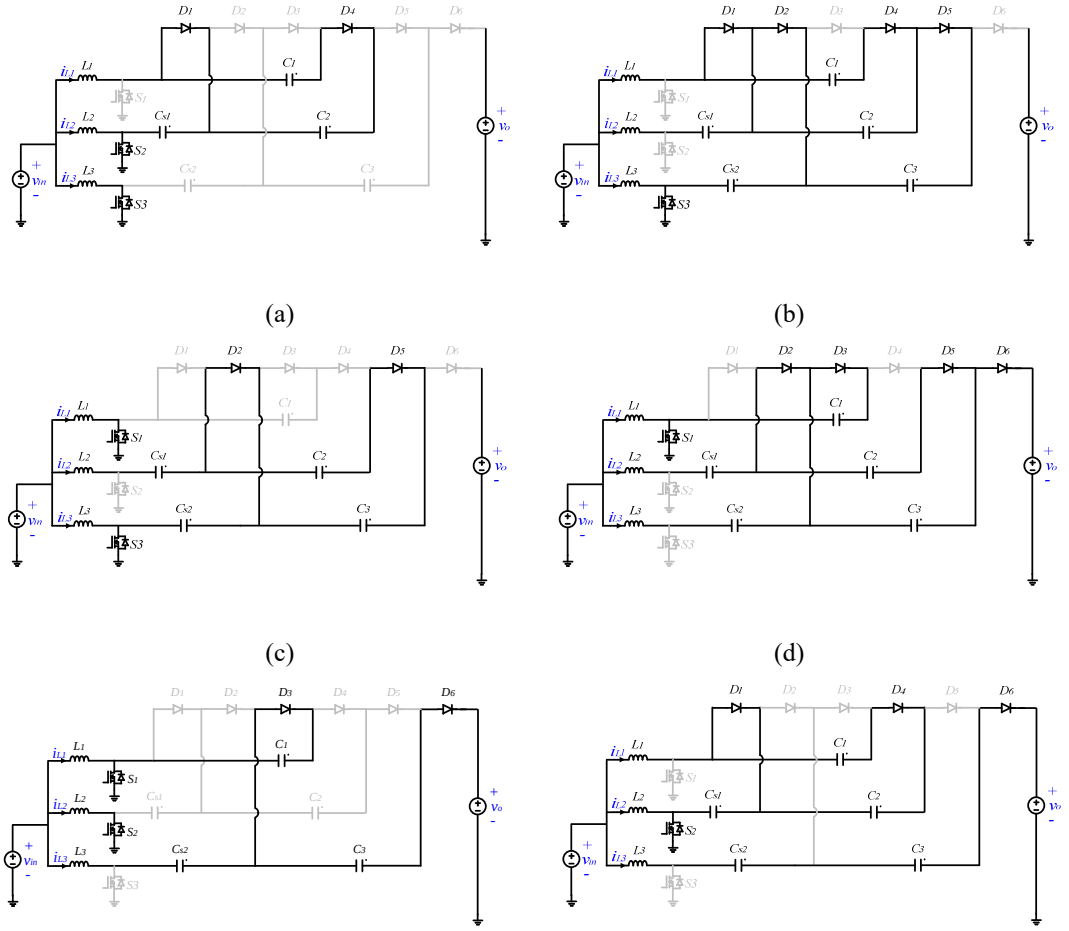


Fig. 3.6 Operation of 3P1S DCHSC with 1/3<*D*<2/3: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5; (f) Mode 6.

By applying the voltage-second balance principle to the three boost inductors of 3P1S DCHSC, the voltage gain of 3P1S DCHSC is derived as

$$\frac{V_o}{V_{in}} = \frac{4}{1-D} + \frac{2}{9(1-D)^3}, \ (1/3<D<2/3) \tag{3.45}$$

The capacitor voltages can be obtained as

$$V_{Cs1} = \left(\frac{1}{1-D} - \frac{2-3D}{9(1-D)^3}\right) V_{in} = \frac{9(1-D)^2-(2-3D)}{36(1-D)^2+2} V_o \tag{3.46}$$

$$V_{Cs2} = \left(\frac{1}{1-D} + \frac{1}{9(1-D)^3}\right) V_{in} = \frac{9(1-D)^2+1}{36(1-D)^2+2} V_o \tag{3.47}$$

$$V_{C1} = V_{C2} = V_{C3} = \left(\frac{2}{1-D} + \frac{1}{9(1-D)^3}\right) V_{in} = \frac{1}{2} V_o \tag{3.48}$$

The voltage stress of the switches can be calculated as

$$V_{S1} = V_{Cs2} = \frac{9(1-D)^2+1}{36(1-D)^2+2} V_o \tag{3.49}$$

$$V_{S2} = V_{C1} - V_{Cs1} = \frac{9(1-D)^2+3(1-D)}{36(1-D)^2+2} V_o \tag{3.50}$$

$$V_{S3} = V_{C1} - V_{Cs2} = \frac{9(1-D)^2}{36(1-D)^2+2} V_o \tag{3.51}$$

The voltage stress of the diodes are determined by the capacitor voltages. It is given by

$$V_{D1} = V_{D3} = V_{D4} = \frac{1}{2} V_o \tag{3.52}$$

$$V_{D2} = V_{D5} = \frac{9(1-D)^2+3(1-D)}{36(1-D)^2+2} V_o \tag{3.53}$$

$$V_{D6} = \frac{9(1-D)^2}{36(1-D)^2+2} V_o \tag{3.54}$$

In order for 3P1S DCHSC to operate normally, one of the switches must be ON at any point of time. Thus, the duty cycle cannot be lower than 1/3. 3P1S DCHSC with $2/3<D<1$ achieves better performance like higher voltage gain, lower voltage stress and automatic current sharing compared to the operation in other ranges. More details about 3P1S DCHSC with $2/3<D<1$ will be discussed in the following.

3.2 Performance Analysis

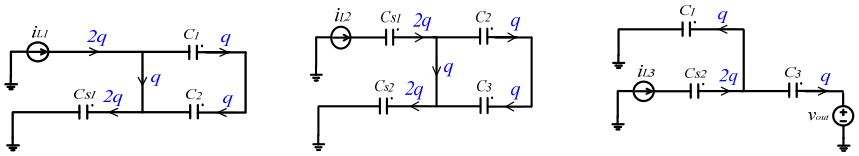
In this section, the current stress, automatic current balancing, boundary condition and comparison of 3P1S DCHSC are analyzed.

A. Current stress

The capacitors in the converter must be charged and discharged in order to transfer charges from the input to the output. Assume that the charge flowing to the load in one switching period is defined as q. The capacitor charge flows of 3P1S DCHSC are illustrated as in Fig. 4.7. Based on the operation principle, the following are obtained. The charge through the diode D_6 equals to the charge flowing out of the capacitor C_3. The charge through D_5 equals to the charge flowing out of C_2. The charge through D_4 equals to the charge flowing out of C_1. The charge through D_3 equals to the charge flowing into C_1. The charge through D_2 equals to the charge flowing out of C_{s1} subtract the charge through D_5. The charge through D_1 equals to the charge flowing into C_{s1} subtract the charge through D_4. Therefore, the average diode currents are expressed as

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5} = I_{D6} = q/T_s = I_o \qquad (3.55)$$

where I_o is the average output current and T_s is the switching period.



(a) (b) (c)

Fig. 3.7 Capacitor charge flows of 3P1S DCHSC: (a) in mode 2; (b) in mode 4; (c) in mode 6.

Based on the charge flow analysis, the average currents through the switches can be expressed as

$$I_{S1} = \frac{2I_L(1-D)T_S - I_O T_S + I_L(2D-1)T_S}{T_S} = I_L - I_o = \frac{1}{3}I_{in} - I_o \quad (3.56)$$

$$I_{S2} = \frac{2I_L(1-D)T_S + I_L(2D-1)T_S}{T_S} = I_L = \frac{1}{3}I_{in} \quad (3.57)$$

$$I_{S3} = \frac{2I_L(1-D)T_S + I_L(2D-1)T_S}{T_S} = I_L = \frac{1}{3}I_{in} \quad (3.58)$$

where I_L is the current through the inductors and I_{in} is the input current.

Similarly, for *n*P*m*S DCHSC, the average currents of the diodes can be evaluated as

$$I_{D1} = \cdots = I_{Dn(m+1)} = I_o \quad (3.59)$$

The average currents of the switches can be evaluated as

$$I_{S1} = \frac{1}{n}I_{in} - I_o;\ I_{S2} = \cdots = I_{Sn} = \frac{1}{n}I_{in} \quad (3.60)$$

B. Automatic current balancing

When the duty cycle is greater than 2/3, the inductor current in each phase can be automatically balanced due to the charge balance of the series capacitors. During mode 2, the inductor current I_{L1} charges the series capacitor C_{s1}. During mode 4, the inductor current I_{L2} discharges C_{s1}. According to charge balance of C_{s1}, the following equation is obtained.

$$I_{L1}(1 - \mathrm{D})T_s = I_{L2}(1 - D)T_s \quad (3.61)$$

During mode 4, the inductor current I_{L2} charges the series capacitor C_{s2}. During mode 6, the inductor current I_{L3} discharges C_{s2}. According to charge balance of C_{s2}, the following equation is obtained.

$$I_{L2}(1-D)T_s = I_{L3}(1-D)T_s \tag{3.62}$$

Then the relationship between i_{L1}, i_{L2} and i_{L3} is expressed as

$$I_{L1} = I_{L3} = I_{L3} \tag{3.63}$$

Therefore, automatic current balancing is obtained due to the presence of the series capacitors.

C. Boundary condition

For *n*P*m*S DCHSC, the average inductor current can be calculated as

$$I_L = \frac{m+1}{1-D}\frac{V_o}{R_o} \tag{3.64}$$

The current ripple of the inductor is

$$\Delta i_L = \frac{V_{in}}{2L}DT_s \tag{3.65}$$

Therefore, the CCM condition is

$$\frac{m+1}{1-D}\frac{V_o}{R_o} > \frac{V_{in}}{2L}DT_s \tag{3.66}$$

The criteria can be manipulated as

$$L > \frac{D(1-D)^2R_o}{2n(m+1)^2f_s} \tag{3.67}$$

The curves of boundary condition are shown in Fig. 3.8. It can be seen that when the number of VM stage increases, it is easier to achieve CCM condition.

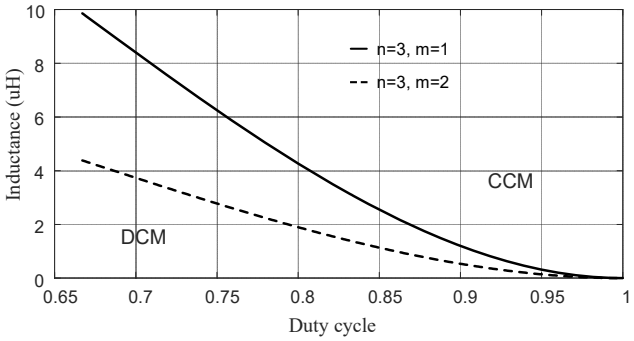


Fig. 3.8 Boundary condition (when $f_s = 100kHz$ and $R_o = 320Ohm$)

D. Comparison

Table 3.1 Comparison with other 3-phase diode-capacitor based converters

Topologies	[37] with P=3, M=2	[40] with P=3, N=1	[41] with j=3, k=1	**3P1S DCHSC**
Phases	3	3	3	3
Magnetics	3	6	6	3
Switches	3	6	6	3
Diodes	9	6	14	6
Capacitors	7	5	8	6
Voltage gain	$\frac{3}{1-D}$	$\frac{2}{1-D}$	$\frac{3+D}{1-D}$	$\frac{6}{1-D}$
Switch voltage stress	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{3+D}$	$\frac{1}{6}$
Max. diode voltage stress	1	$\frac{1}{2}$	$\frac{2}{3+D}$	$\frac{1}{3}$
Automatic current balancing	No	No	No	Yes

The 3P1S DCHSC is compared with other three-phase interleaved converters introduced in the literature. The component count, voltage gain, switch voltage and maximum diode voltage stress are listed in Table 3.1. In order for a fair comparison, the voltage stresses are normalized by the output voltage. As can be seen, compared to the other converters, the 3P1S DCHSC achieves higher voltage gain under the same duty

cycle. Also, lower switch voltage stress and diode voltage stress are achieved. As a result, low-voltage-rating semiconductor devices can be used to lower the conduction loss. In addition, the 3P1S DCHSC features automatic current balancing; thus, extra current sharing circuit is not required.

3.3 Design Considerations

In this section, design considerations of the key components are discussed. As a design example, a 20V to 400V 3P1S DCHSC is to be considered. The rated power is 500W, and the switching frequency f_s is chosen as 100kHz.

A. Inductor design

The inductor design is similar to that of a conventional boost converter. The inductor values are selected based on the ripple of the inductor current. In this design example, the peak-to-peak inductor current ripple $\gamma\%$ is set to 18%. Then the inductance can be calculated as

$$L_1 = L_2 = L = \frac{V_{in}D}{\gamma\% I_L f_s} > 93.4uH \tag{3.68}$$

Finally, the value of the inductors is selected as 100uH.

B. Energy transfer capacitor design

The capacitors can be designed based on the voltage ripple and the output power. In this design example, the voltage ripples of the capacitors $r\%$ is set to 2%, and the output power P_o is 500W. Then the capacitances can be calculated as

$$C_{s1} > \frac{12P_o}{r\%{V_o}^2 f_s} = 18.75uF \tag{3.69}$$

$$C_{s2} > \frac{6P_o}{r\%{V_o}^2 f_s} = 9.38uF \tag{3.70}$$

$$C_1 = C_2 = C_3 > \frac{2P_o}{r\%{V_o}^2 f_s} = 3.12uF \tag{3.71}$$

Finally, the capacitance of the series capacitors (C_{s1}, C_{s2}) is selected as 22uF. The capacitance of the flying capacitors ($C_1 \sim C_3$) is selected as 8.5uF.

Generally, capacitors with low ESR are preferred in order to reduce power losses. It is a favorable solution that film capacitors or multilayer chip-type ceramic capacitors are adopted. Moreover, multiple capacitors can be connected in parallel to reduce ESR.

C. Semiconductor selection

The switches and diodes are selected according to their voltage stresses. The voltage stresses of the switches and diodes can be calculated from (3.20) and (3.21). In practice, considering the voltage overshoot and ringing, the voltage rating of the switches and diodes should be higher than the calculated values. Finally, MOSFET with 150V voltage rating is selected for S_1 and S_2. Schottky diode with 200V voltage rating is selected for $D_1 \sim D_6$.

3.4 Simulation and Experimental Results

A. Simulation

A simulation model of 3P1S DCHSC is built in PSIM to verify the theoretical analysis. The specifications and component parameters used in simulation are shown in Table 3.2. The simulated waveforms are given in Fig. 3.9. The simulation results show that: 1) 20 times step-up voltage gain is achieved with $D = 0.7$; 2) interleaved operation is

achieved; leading to small input current ripple; 3) the switch voltage stress is one-sixth of the output voltage; 4) the voltage stress of D_1-D_5 is one-third of the output voltage and the voltage stress of D_6 is one-sixth of the output voltage.

Table 3.2 Key parameters of the prototype

Parameter	Value/Description
Input voltage	20V
Output voltage	400V
Output power	500W
Input current	25A
Switching frequency	100kHz
Switches S_1-S_3	IPA075N15N3 (150V, r_{ds}=7.5mΩ)
Diodes D_1-D_6	STPS20200CT (200V, $V_F = 0.7V$)
Inductor L_1-L_3	L=100uH, r_L=12mΩ
Capacitor C_{s1}, C_{s2}	22uF film capacitor, r_C=8mΩ
Capacitor C_1-C_3	8.2uF film capacitor, r_C=8mΩ
Capacitor C_o	2×120uF electrolytic capacitor in parallel, r_{Co}=100mΩ

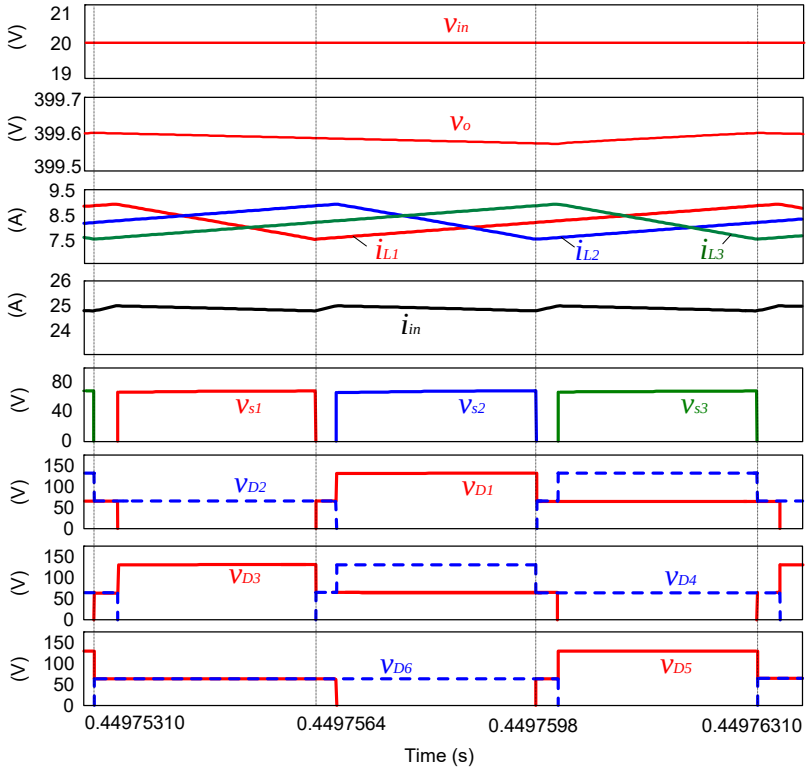


Fig. 3.9 Simulated waveforms.

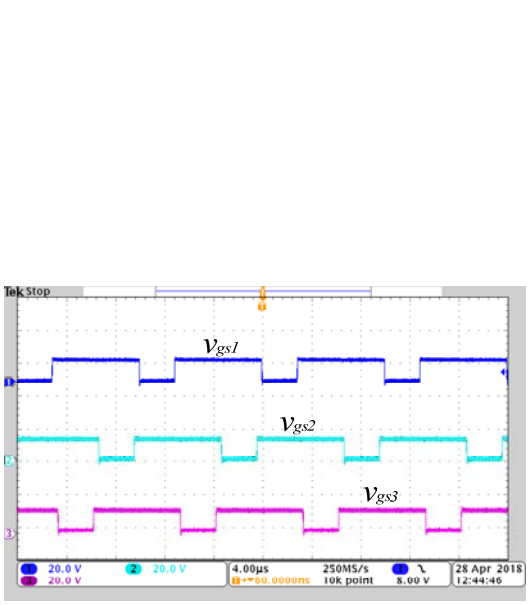
B. Experimental verification

A 3P1S DCHSC prototype with 20V input, 400V output and 500W power rating is built to verify the theoretical analysis. The switching frequency is 100 kHz. The duty cycles of the switches are around 0.7. The key parameters of the prototype are shown in Table 3.2.

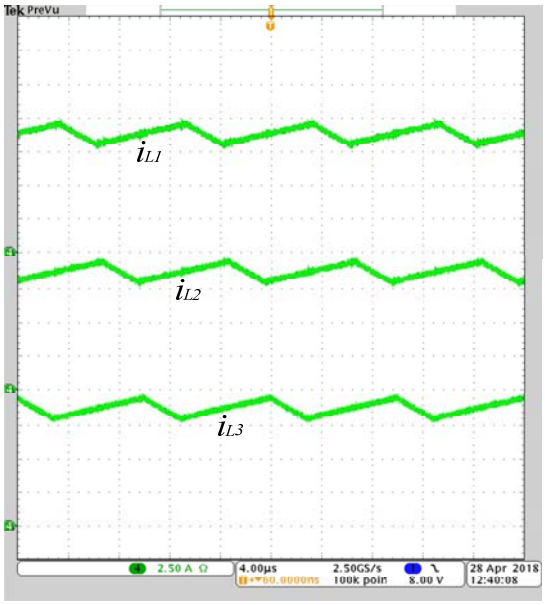
Fig. 3.10 (a) shows the gate signals of the switches and Fig. 3.10 (b) shows the inductor current waveforms. It is clear that the inductor currents have an interleaved feature. Therefore, the input current ripple can be reduced. Also, the three inductor currents are equal, which indicates that automatic uniform current sharing is achieved. Fig. 3.10 (c) shows the input and output voltages. It can be seen that the input voltage is 20V and output voltage is 400V, indicating that high voltage gain is achieved under moderate duty cycles. Fig. 3.10 (d) shows the drain-source voltages of the switches. As can be seen, the blocking voltage of the switches is around 68V, which matches the calculation from (3.20). Fig. 3.10 (e)-Fig. 3.10 (f) show the diode voltages v_{D1}~v_{D6}. The blocking voltage of the diodes D_1 - D_5 is around 136V and the blocking voltage of D_6 is around 68V, which are in accordance with the calculations from (3.21). Fig. 3.10 (f) also shows the series capacitor voltages. The voltage of C_{s1} is around 68V, and the voltage of C_{s2} is around 136V. Fig. 3.10 (g) shows the flying capacitor voltages v_{c1}~v_{c3}. The flying capacitor voltages are equal and measured as 200V, which matches the calculations from (3.17)-(3.19). Fig. 3.10 (h) shows the load transient response due to step load increase from 40% load to 100% load, and Fig. 3.10 (i) shows load transient response due to step load decrease from 100% load to 40% load. The efficiency versus output power is measured as in Fig. 3.10 (j). The

peak efficiency is 94.6%, which is achieved at 330W output power. The efficiency at full load is measured as 93.8%.

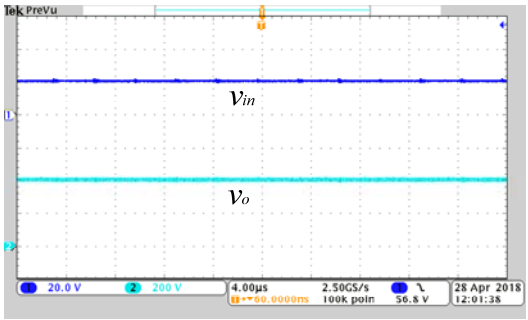
A theoretical loss analysis is performed based on the selected components of the hardware prototype. The power loss distribution of 3P1S DCHSC at full load is shown in Fig. 3.19. It is observed that dominant power losses are diode and switch loss. The calculated efficiency at full load is 96.9%, compared to the measured efficiency 93.8% at full load. The discrepancy could be caused by the ringing of the diode reverse recovery, the small ripple approximation and the measurement error.



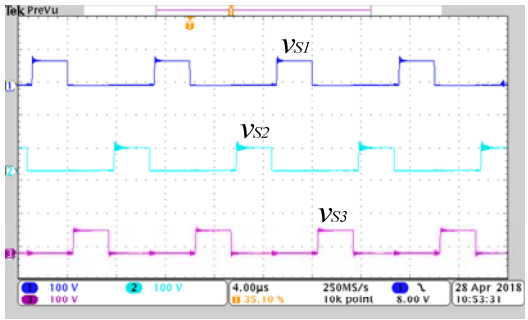
(a)



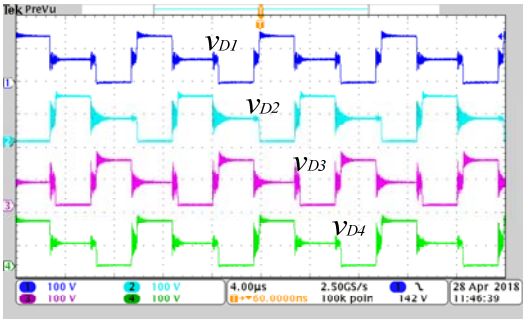
(b)



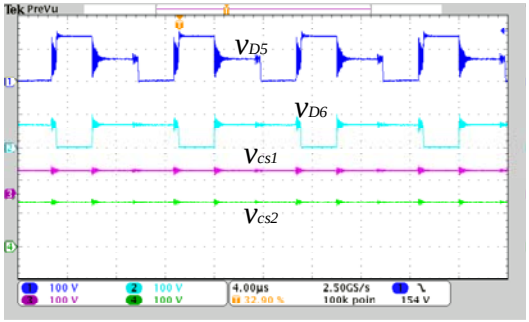
(c)



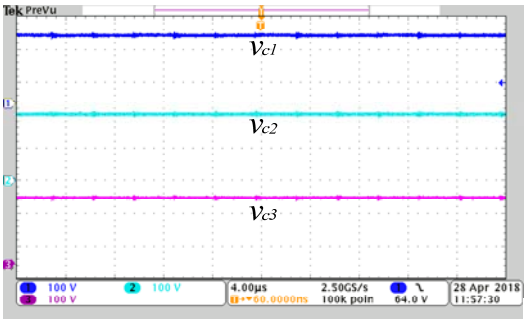
(d)



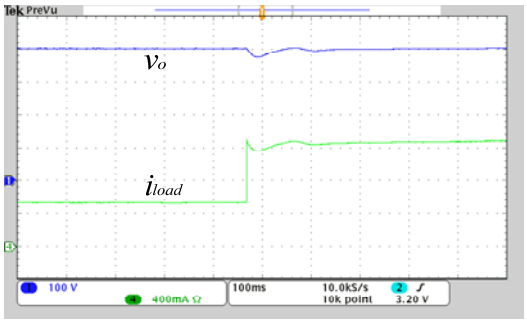
(e)



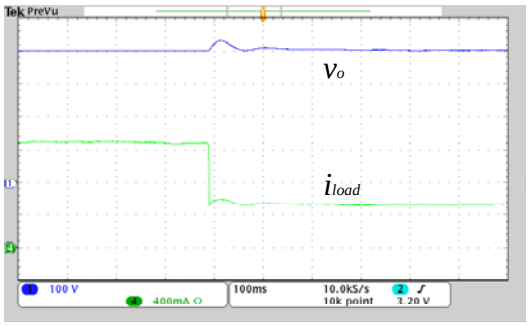
(f)



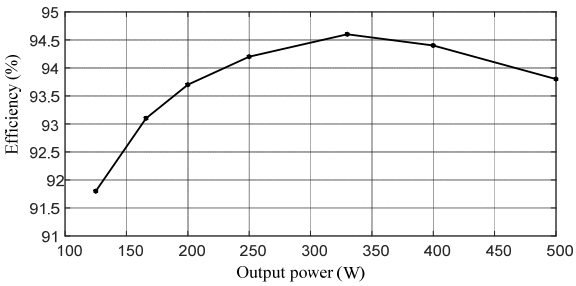
(g)



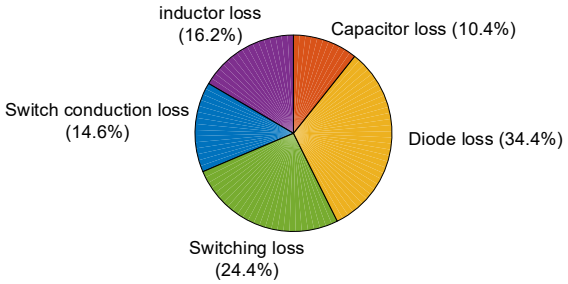
(h)



(i)



(j)



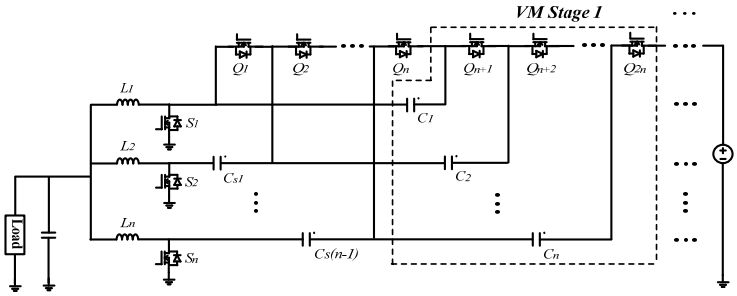
(k)

Fig. 3.10 Experimental results: (a) driving signals; (b) inductor currents; (c) input and output voltages; (d) switch voltages; (e) diode voltages (v_{D1}, v_{D2}, v_{D3}, v_{D4}); (f) diode voltages (v_{D5}, v_{D6}) and series capacitor

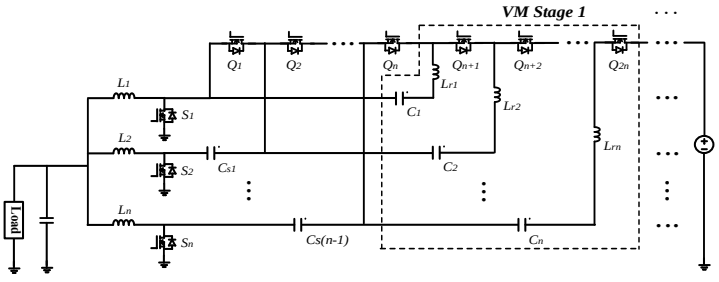
voltages; (g) flying capacitor voltages; (h) dynamic waveform at load increase; (i) dynamic waveform at load decrease; (j) measured efficiency; (k) loss breakdown.

3.5 High Step-Down Extension

The *n*P*m*S DCHSC topology can be extended to step-down operation by replacing all the diodes with switches, as shown in Fig 3.11 (a). The power source is connected at high side and the load is connected at low side. Switch S_1~S_n are triggered by interleaved PWM signals. Switch Q_i is driven complementary with S_i (i=1, 2, …, n). With such a modulation scheme, the buck-version DCHSC can achieve a high step-down conversion ratio. The converter in Fig, 3.11 (a) has high transient current through the switches and flying capacitors due to capacitor charging/discharging in parallel. Resonant inductor can be inserted to limit the high transient current, as shown in Fig, 3.11 (b).



(a)



(b)

Fig. 3.11 Extension of nPmS DCHSC to buck operation.

Chapter 4 Single-Phase Coupled-Inductor Boost Converter with Continuous Input Current and Low Component Count

In this chapter, a single-phase coupled-inductor boost converter is analyzed and designed. High voltage gain is achieved with the aid of the coupled inductor. Due to a discrete inductor at the input, continuous input current is obtained, which significantly reduces or even save the input electrolytic capacitor, leading to increased power density and reliability. Also, the new converter has low component count, leading to low cost. Furthermore, recycled leakage energy and alleviated diode reverse recovery can be achieved.

The proposed converter and its operation principles are described in Section 4.1. Performance analysis are analyzed in Section 4.2. Design considerations are discussed in Section 4.3. Experimental results are presented in Section 4.4.

4.1 Topology and Operation Principles

Fig. 4.1 shows the proposed single-switch high step-up coupled-inductor boost converter. It is composed of one input inductor, one coupled inductor, one switch, two diodes, two energy transfer capacitors, and one output capacitor. Fig. 4.2 shows the equivalent circuit. The coupled inductor is modeled as an ideal transformer with magnetizing inductance (L_m) and leakage inductance (L_k).

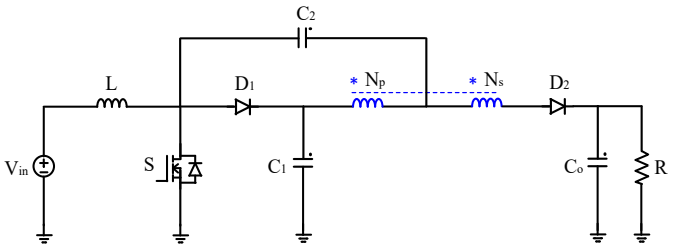


Fig. 4.1 Proposed single-phase coupled-inductor boost converter.

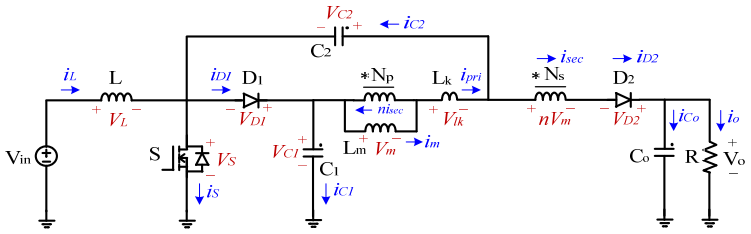


Fig. 4.2 The equivalent circuit.

In order to simplify the analysis, the following assumptions are made: 1) all semiconductor devices are considered ideal; 2) all the capacitors are large enough so that the voltages across them are constant without ripples.

When the input inductor current (i_L) is above zero throughout the switching cycle and the output diode current (i_{D2}) is above zero throughout the switch off time, the converter is operating in continuous conduction mode (CCM). Discontinuous conduction mode (DCM) occurs when 1) the input current ripple is large so that i_L reaches zero, or 2) the magnetizing current ripple is large, which makes diode D_2 reverse-biased before the end of the switching period. As one main feature of the proposed converter is continuous input current, DCM operation with i_L reaching zero is not desired. Only DCM operation with D_2 reverse-biased before the end of the switching period is discussed in this chapter.

A. CCM Operation

Fig. 4.3 shows the key waveforms of the proposed converter in CCM. Four modes are observed during one switching period. The corresponding circuits of each mode are shown in Fig. 4.4.

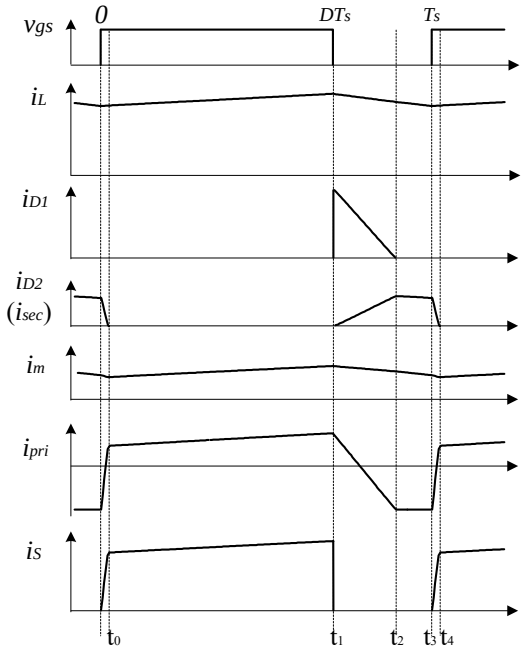


Fig. 4.3 Key waveforms in CCM

Mode 1 [t_0 - t_1]: The switch is on, and all diodes are reverse-biased, as shown in Fig. 4.4 (a). The input inductor is charged linearly by the input source. The capacitor C_1 is delivering energy to the coupled inductor and capacitor C_2. The primary voltage of the coupled inductor is $V_{C1} - V_{C2}$, and the coupled inductor is magnetized. The output capacitor supports the load. As the leakage inductance is negligible compared to the magnetizing inductance, the following equations are obtained.

$$v_L = V_{in} \tag{4.1}$$

$$v_m = V_{C1} - V_{C2} \tag{4.2}$$

$$i_{Co} = -I_o \tag{4.3}$$

$$-i_{C1} = i_{C2} = i_{pri} = i_m \tag{4.4}$$

Mode 2 [t_1 - t_2]: At t_1, the switch is turned off, which makes diodes D_1 and D_2 turned on, as shown in Fig. 4.4 (b). The input inductor starts releasing energy. The capacitor C_1 is being charged. The primary voltage of the coupled inductor is clamped to $-V_{C2}$, and thus the coupled inductor is demagnetized. The secondary current of the coupled inductor i_{sec} is increasing linearly, and the current through D_1 is decreasing linearly. The equations in this mode are obtained as following.

$$v_m = -V_{C2} \tag{4.5}$$

$$V_{in} = v_L - V_{C2} - v_m + V_{C1} \tag{4.6}$$

$$V_{C1} = (\mathrm{n} + 1)v_m + V_o \tag{4.7}$$

$$i_{pri} = i_m - ni_{sec} \tag{4.8}$$

$$i_{D2} = i_{sec} = \frac{V_{C1}+(n+1)V_{C2}-V_o}{n^2 L_k}(t - t_1) \tag{4.9}$$

$$i_{Co} = i_{sec} - I_o \tag{4.10}$$

$$i_{C2} = i_{pri} - i_{sec} = i_m - (n + 1)i_{sec} \tag{4.11}$$

$$i_{D1} = i_L + i_{C2} = i_L + i_m - (n + 1)i_{sec} \tag{4.12}$$

$$i_{C1} = i_{D1} - i_{pri} = i_L - i_{sec} \tag{4.13}$$

Solving (4.6) and (4.7), the following can be obtained.

$$v_L = V_{in} + V_{C2} - \frac{n}{n+1}V_{C1} - \frac{1}{n+1}V_o \tag{4.14}$$

$$v_m = \frac{1}{n+1}(V_{C1} - V_o) \tag{4.15}$$

Mode 3 [t_2 - t_3]: At t_2, the current through D_1 decreases to zero and D_1 is naturally turned off. Therefore, D_1 has no reverse recovery problem. As shown in Fig. 4.4 (c), the inductor current i_L discharges C_2, and the primary current of the coupled inductor i_{pri} charges C_1. The difference of i_L and i_{pri} is delivered to the load. Equation (4.6)-(4.8) and (4.14)-(4.15) still hold in this mode, and the following equations are obtained.

$$i_{C2} = -i_L \tag{4.16}$$

$$i_L + i_{pri} = i_{sec} \tag{4.17}$$

Substituting (4.8) to (4.17), i_{sec} is evaluated as

$$i_{sec} = \frac{1}{n+1}(i_L + i_m) \tag{4.18}$$

Then,

$$i_{D2} = \frac{1}{n+1}(i_L + i_m) \tag{4.19}$$

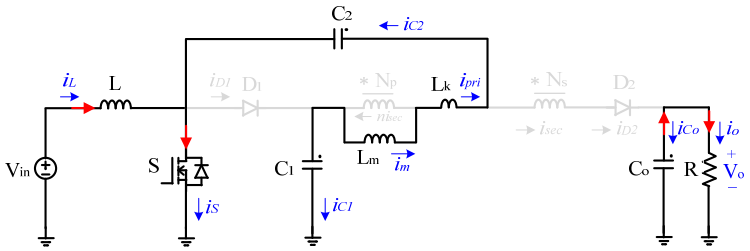
$$i_{C1} = -i_m + ni_{sec} = \frac{n}{n+1}i_L - \frac{1}{n+1}i_m \tag{4.20}$$

$$i_{Co} = i_{sec} - I_o = \frac{1}{n+1}(i_L + i_m) - I_o \tag{4.21}$$

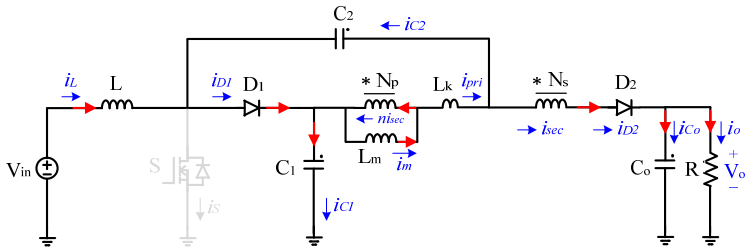
Mode 4 [t_3 - t_4]: At t_3, the switch is turned on, as shown in Fig. 4.4 (d). As the leakage inductance limits the current changing rate, the switch current is increasing gradually after the switch is turned on, which helps reduce the switching loss. The current of diode D_2 is decreasing, and the falling rate is determined by the leakage inductance.

Thus, the reverse recovery problem of D_2 is alleviated. This mode ends when the current through D_2 becomes zero and then turned off. The falling rate of D_2 is given by

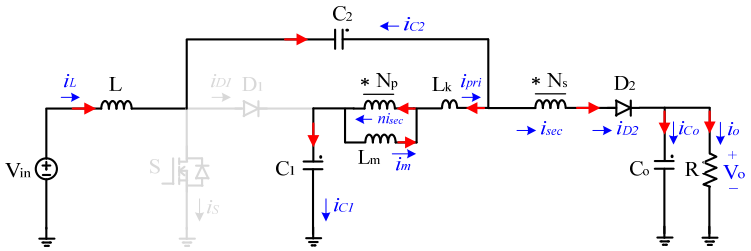
$$\frac{di_{D2}}{dt} = -\frac{V_o+nV_{C1}-(n+1)V_{C2}}{n^2L_k} \tag{4.22}$$



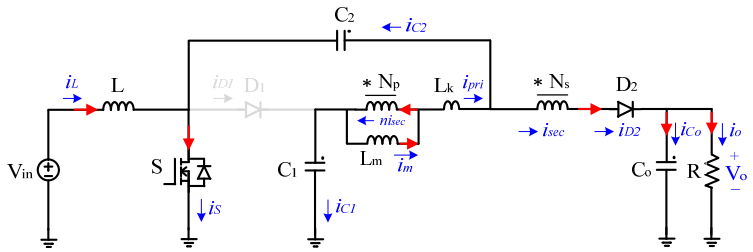
(a)



(b)



(c)



(d)

Fig. 4.4 Operation modes of the proposed converter in CCM: (a) Mode 1 [t_0 - t_1]; (b) Mode 2 [t_1 - t_2]; (c) Mode 3 [t_2 - t_3]; (d) Mode 4 [t_3 - t_4].

B. DCM Operation

Fig. 4.5 shows the key waveforms of the proposed converter in DCM. Four modes are observed during one switching period.

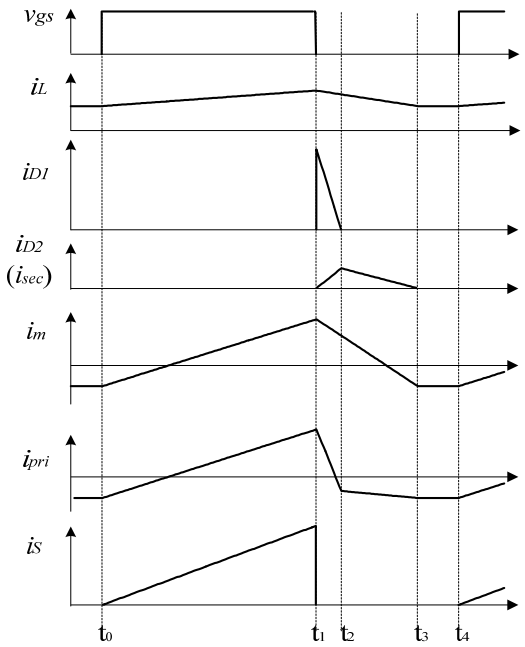


Fig. 4.5 Key waveforms in DCM

Mode 1 [t_0 - t_1]: The switch is on, and all diodes are reverse-biased. The corresponding circuit is the same as in Fig. 4.4 (a). The input current is increasing linearly. The primary voltage of the coupled inductor is clamped at $V_{C1} - V_{C2}$, and thus the magnetizing current is increasing linearly.

Mode 2 [t_1 - t_2]: The switch is turned off, and diodes D_1 and D_2 are forward-biased. The corresponding circuit is the same as in Fig. 4.4 (b). The input current is decreasing linearly. The primary voltage of the coupled inductor is clamped to $-V_{C2}$, and thus the magnetizing current is decreasing linearly. The secondary current is increasing, and the current through D_1 is decreasing.

Mode 3 [t_2 - t_3]: At t_2, the current through D_1 decreases to zero and D_1 is naturally turned off. The corresponding circuit is the same as in Fig. 4.4 (c). The input current and the magnetizing current keep decreasing. The current through D_2 in this mode can be expressed as in (19). It is a fraction of the sum of the input current and magnetizing current. As the magnetizing inductance is small under DCM, the magnetizing current has large ripple. Small ripple assumption cannot be applied. Thus, the current through D_2 is decreasing as well.

Mode 4 [t_3 - t_4]: At t_3, the current through D_2 decreases to zero and D_2 is naturally turned off. The corresponding circuit in this mode is shown in Fig. 4.6. All the switch and diodes are in the off state. The input current becomes equal to the magnetizing current in magnitude but opposite in direction. At t_4, the switch is turned on, and mode 1 starts again.

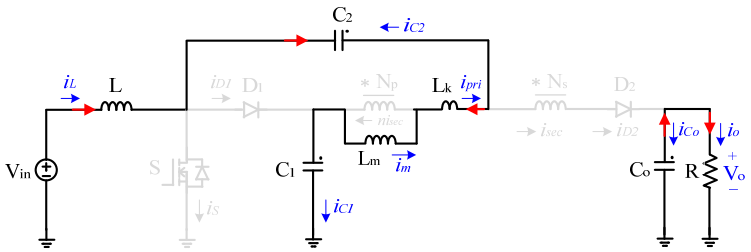


Fig. 4.6 Mode 4 of the proposed converter in DCM

Similar to flyback converter, the voltage gain of the proposed converter in DCM is dependent to the load, and the peak and RMS currents in the windings and switches become higher compared to the CCM operation. This is not favorable for high current applications. In this paper, only analysis and design of the proposed converter in CCM will be discussed.

4.2 Performance Analysis

A. Voltage gain

By applying the voltage-second balance principle to L and L_m, the following equations are obtained.

$$V_{in}D + \left(V_{in} + V_{C2} - \frac{n}{n+1}V_{C1} - \frac{1}{n+1}V_o\right)(1-D) = 0 \qquad (4.23)$$

$$(V_{C1} - V_{C2})D + \frac{1}{n+1}(V_{C1} - V_o)(1-D) = 0 \qquad (4.24)$$

Solving (4.5) to (4.7), the following relationship is derived.

$$V_{C1} + (n+1)V_{C2} = V_o \qquad (4.25)$$

Solving (4.23)-(4.25), the voltage gain of the proposed converter is derived as

$$M = \frac{V_o}{V_{in}} = \frac{1+(n+1)D}{1-D} \tag{4.26}$$

The voltages of C_1 and C_2 are derived as

$$V_{C1} = \frac{V_{in}}{1-D} = \frac{V_o}{1+(n+1)D} \tag{4.27}$$

$$V_{C2} = \frac{DV_{in}}{1-D} = \frac{DV_o}{1+(n+1)D} \tag{4.28}$$

Fig. 4.7 shows the curves of the voltage gain versus duty cycle under different turns ratios. It can be seen that the proposed converter can achieve a high voltage gain by adjusting the duty cycle and turns ratio.

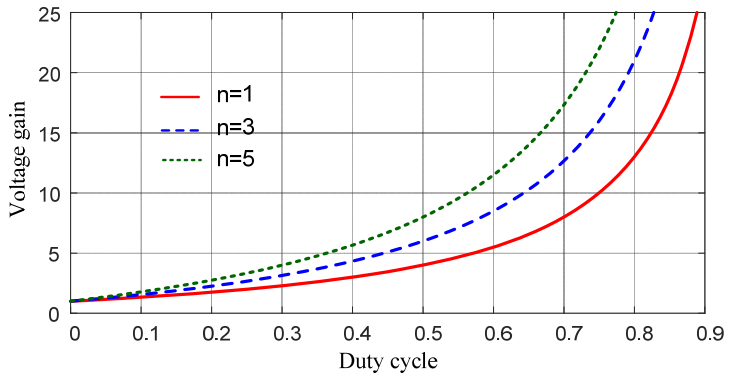


Fig. 4.7 Voltage gain versus duty cycle under different turns ratios

B. Voltage and current stress

The voltage stresses of the capacitors are given by (4.27) and (4.28). The voltage stress of the switch can be derived as

$$V_S = \frac{1}{1+(n+1)D} V_o \tag{4.29}$$

It can be seen that the switch voltage stress is much lower than the output voltage. It decreases as the voltage gain is extended by either increasing the duty cycle or the turns

ratio. Therefore, low-voltage-rating MOSFETs with small on-resistance can be adopted to reduce the conduction loss.

The voltage stresses of the diodes are obtained as

$$V_{D1} = \frac{1}{1+(n+1)D} V_o \tag{4.30}$$

$$V_{D2} = \frac{n+1}{1+(n+1)D} V_o \tag{4.31}$$

By applying small-ripple approximation, the input inductor current is assumed to be I_L and the magnetizing current of the coupled inductor is assumed to be I_m. Let $t_2 - t_1 = D_a T_s$, and then $t_3 - t_2 = (1 - D - D_a)T_s$. Ignoring the transitional mode, the simplified current waveforms of the capacitors is shown in Fig. 4.8.

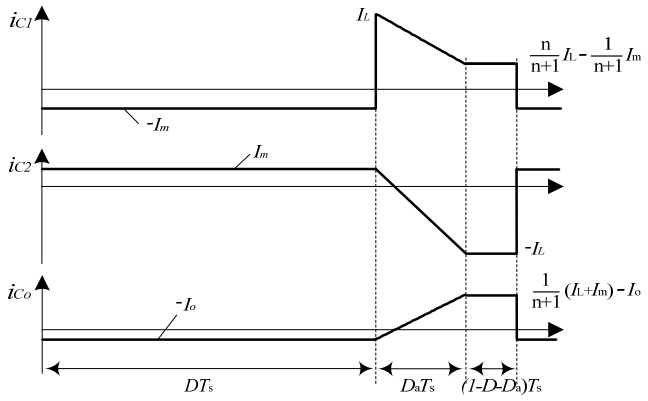


Fig. 4.8 Simplified current waveforms of the capacitors

According to the charge balance of C_1, C_2 and C_o, the following equations are obtained.

$$-I_m D + \frac{1}{2}\left(I_L + \frac{nI_L}{n+1} - \frac{I_m}{n+1}\right) D_a + \left(\frac{nI_L}{n+1} - \frac{I_m}{n+1}\right)(1 - D - D_a) = 0 \tag{4.32}$$

$$I_m D + \frac{1}{2}(I_m - I_L) D_a - I_L)(1 - D - D_a) = 0 \tag{4.33}$$

$$-I_o\,D+\frac{1}{2}\left(-I_o+\frac{I_m+I_L}{n+1}-I_o\right)D_a+(\frac{I_m+I_L}{n+1}-I_o)(\,1-D-D_a)=0 \qquad (4.34)$$

Solving (4.32)-(4.34), the following is derived.

$$I_L=\frac{1+(n+1)D}{1-D}I_o \qquad (4.35)$$

$$I_m=\frac{(n+1)(1-D)}{1+(n+1)D}I_L=(n+1)I_o \qquad (4.36)$$

$$D_a=\frac{2}{n+2}(1-D) \qquad (4.37)$$

Since the average currents of capacitors in one switching period are zero, according to the operation principles, the average current of the diodes can be evaluated as

$$I_{D2\_avg}=I_{Co\_avg}+I_o=I_o \qquad (4.38)$$

$$I_{D1\_avg}=I_{C1\_avg}+I_{C2\_avg}+I_{D2\_avg}=I_o \qquad (4.39)$$

The RMS current stress of the switch can be expressed as

$$I_{S\_rms}=(I_L+I_m)\sqrt{D}=\frac{(n+2)\sqrt{D}}{1-D}I_o \qquad (4.40)$$

The RMS current of the primary winding of the coupled inductor is given by

$$I_{pri\_rms}=\sqrt{D{I_m}^2+\frac{(1-D)}{(n+2)(n+1)}\left(\frac{2}{3}I_m\big((n+2)I_m-nI_L\big)+\frac{n+\frac{2}{3}}{n+1}(I_m-nI_L)^2\right)} \qquad (4.41)$$

The RMS current of the secondary winding of the coupled inductor is given by

$$I_{sec\_rms}=\frac{n+2}{n+1}\sqrt{\frac{n+\frac{2}{3}}{(n+2)(1-D)}}I_o \qquad (4.42)$$

The current stresses of the capacitors are given by

$$I_{C1\_rms} = \sqrt{DI_m{}^2 + \frac{1-D}{n+2}\left(\frac{2}{3}I_L\left(\frac{2n+1}{n+1}I_L - I_o\right) + (n+\frac{2}{3})(\frac{n}{n+1}I_L - I_o)^2\right)} \quad (4.43)$$

$$I_{C2\_rms} = \sqrt{DI_m{}^2 + \frac{1-D}{n+2}\cdot(\frac{2}{3}I_m(I_m - I_L) + \left(n+\frac{2}{3}\right)I_L{}^2)} \quad (4.44)$$

$$I_{Co\_rms} = \sqrt{DI_o{}^2 + \frac{1-D}{n+2}(\frac{2}{3}I_o(I_o - \frac{I_L}{n+1}) + \frac{\left(n+\frac{2}{3}\right)I_L{}^2}{(n+1)^2})} \quad (4.45)$$

C. Input current ripple

Due to the presence of a discrete inductor at the input side, the input current of the proposed converter is continuous. The current ripple can be evaluated as

$$\Delta i_L = \frac{V_{in}D}{Lf_s} = \frac{V_oD(1-D)}{Lf_s(1+(n+1)D)} \quad (4.46)$$

The continuous input current makes the proposed converter beneficial to extend the lifetime of the low-voltage sources like batteries and fuel cells. Also in PV applications, the feature of the continuous input current can significantly reduce the input capacitor, which helps increase the power density and reliability.

D. Influence of the leakage inductance

As can be seen from the operation principles, the current of the leakage inductance partly goes through the capacitor C_2 and partly goes to the load when the switch is turned off. Thus, the leakage energy can be recycled and no additional components are needed.

During mode 2, due to the presence of the leakage inductance, the current of the diode D_1 decreases linearly and then naturally turns off. Thus, D_1 has no reverse recovery problem. During mode 4, the current falling rate of the diode D_2 is limited by the leakage

inductance, which can significantly alleviate the reverse recovery of D_2. Also, with the aid of the leakage inductance, the switch current rises gradually when the switch is turned on, which helps reduce the switching loss.

The leakage inductance can also have an effect on the voltage gain. Considering the rising slope of the secondary current i_{sec}, the following equation can be written.

$$\frac{V_{C1}+(n+1)V_{C2}-V_o}{n^2L_k} = \frac{i_L+i_m}{(n+1)D_aT_s} \tag{4.47}$$

Substituting (4.35)-(4.37) to (4.47), the following equation is obtained.

$$V_{C1} + (n+1)V_{C2} = (\frac{n^2(n+2)^2}{2(n+1)(1-D)^2}Q + 1)V_o \tag{4.48}$$

where $\mathrm{Q} = L_k/(RT_s)$.

As the average voltages of the inductances are zero during steady state, the following equation can be obtained according to KVL.

$$V_{in} = -V_{C2} + V_{C1} \tag{4.49}$$

Due to the voltage-second principle of the input inductor, the following equation can be written.

$$V_{in}D + (V_{in} - V_{C1})D_a + (V_{in} + V_{C2} - V_{C1} + \frac{V_{C1}-V_o}{n+1})(1 - D - D_a) = 0 \tag{4.50}$$

Solving (4.48)-(4.50), the voltage gain with the effect of the leakage inductance is expressed as

$$M = \frac{V_o}{V_{in}} = \frac{1+(n+1)D}{(1-D)(1+\frac{n^2(n+2)^2}{2(n+1)^2(1-D)^2}Q)} \tag{4.51}$$

The voltage gain with the effect of the leakage inductance is plotted in Fig. 4.9. It can be seen that the voltage gain is not very sensitive to the leakage inductance. If the leakage inductance is ignored, (4.51) will be equal to (4.26).

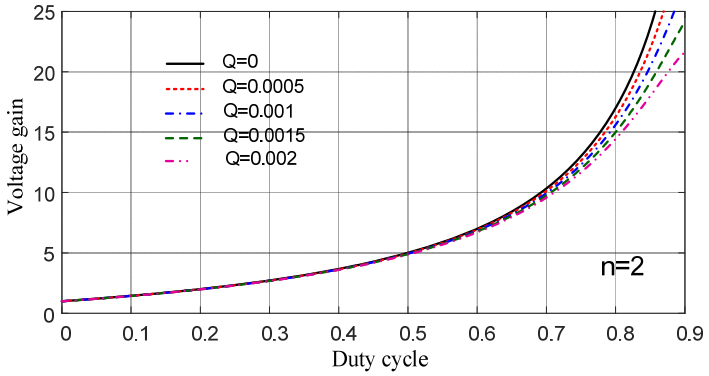


Fig. 4.9 Voltage gain considering the effect of the leakage inductance

E. Boundary condition

The aforementioned analysis is under CCM condition. In order to ensure CCM condition, the input inductor current must be above zero throughout the switching cycle and the diode current of D_2 must be above zero throughout the switch off time, which yields

$$i_{L.min} = I_L - \frac{\Delta i_L}{2} = \frac{1+(n+1)D}{1-D} I_o - \frac{V_{in}D}{2Lf_s} > 0 \qquad (4.52)$$

$$i_{D2.min} = \frac{1}{n+1}\left(I_L - \frac{\Delta i_L}{2} + I_m - \frac{\Delta i_m}{2}\right) = \frac{1}{n+1}\left(\frac{n+2}{1-D} I_o - \frac{V_{in}D}{2Lf_s} - \frac{(V_{C1}-V_{C2})D}{2L_m f_s}\right) > 0 \qquad (4.53)$$

Define $k_L = 2Lf_s/R$ and $k_{Lm} = 2L_m f_s/R$. By solving (4.52) and (4.53), the CCM criteria are obtained as following.

$$k_L > K_{L.crit} = \frac{D(1-D)^2}{(1+(n+1)D)^2} \qquad (4.54)$$

$$k_{Lm} > K_{Lm.crit} = \frac{D(1-D)^2}{(1+(n+1)D)(n+1)(1-D)} \tag{4.55}$$

The dependence of $K_{L.crit}$ and $K_{Lm.crit}$ on the duty cycle and turns ratio are plotted in Fig. 4.10. It can be seen that when the turns ratio increases, it is easier to achieve CCM condition.

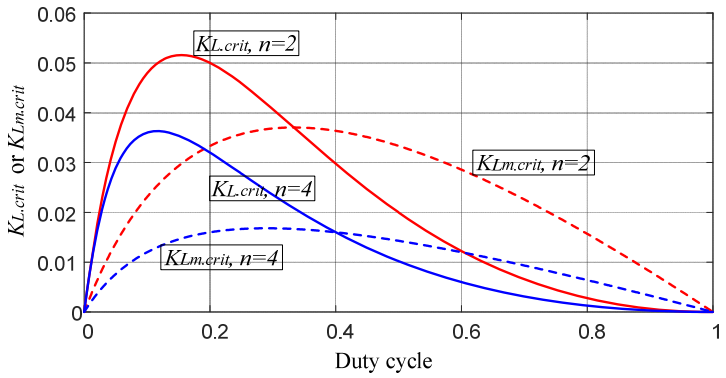


Fig. 4.10 Boundary condition of the proposed converter

F. Voltage gain considering parasitic elements

Similar to the conventional boost converter, the voltage gain of the proposed converter would deviate from the ideal value if parasitic elements are considered, especially under extreme duty cycles. The equivalent circuit including parasitic elements is illustrated in Fig. 4.11, where r_{on} is the on-resistance of the switch, r_L is the resistance of the input inductor, r_{pri} and r_{sec} are the resistances of the primary winding and secondary winding of the coupled inductor, respectively, and V_d is the forward voltage drop of all diodes. The leakage inductance and the equivalent series resistance of the capacitors are ignored in order to simplify calculation.

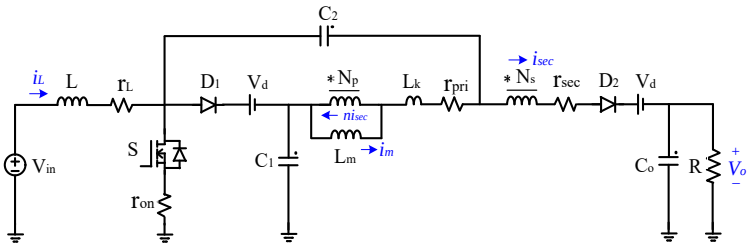


Fig. 4.11 Equivalent circuit including parasitic elements

By using KVL and voltage-second balance of the input inductance and magnetizing inductance, the voltage gain considering parasitic elements can be derived as

$$\frac{V_o}{V_{in}} = \frac{\frac{1+(n+1)D}{1-D} - 2\frac{V_d}{V_{in}}}{1+\frac{1}{1-D}\left(A\frac{r_{on}}{R}+B\frac{r_L}{R}+C\frac{r_{pri}}{R}+\frac{r_{sec}}{R}\right)} \tag{4.56}$$

where

$$A = (n+2)(n+1+1/(1-D))$$

$$B = (1+(n+1)D)^2/(1-D)$$

$$C = (n+2)(n+1)(1-D)$$

The voltage gain considering parasitic elements at different loads is shown in Fig. 4.12. Under given parasitic parameters, the voltage gain would decrease as the load increases. Also the voltage gain with parasitic elements would collapse under extreme duty cycles.

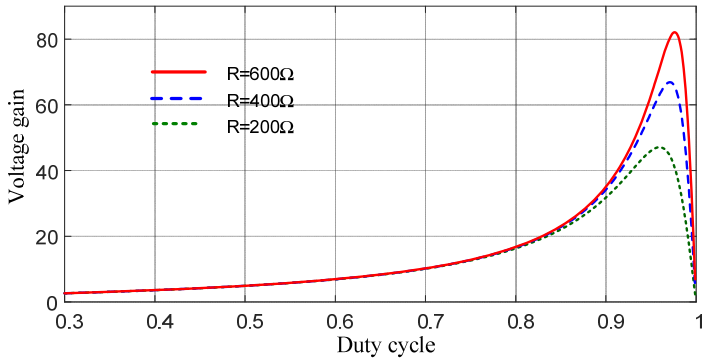


Fig. 4.12 Voltage gain with parasitic elements ($r_{on} = 7.5m\Omega$, $r_L = 20m\Omega$ $r_{pri} = 20m\Omega$ $r_{sec} = 100m\Omega$, $V_d = 0.7V$, $n = 2$, $V_{in} = 20V$)

4.3 Design Considerations

In this section, design considerations of the key components will be discussed. As a design example, a 200W 20V-input 200V-output converter is to be considered. The switching frequency is set to 100kHz.

A. Coupled-inductor design

The voltage gain is determined by the duty cycle and the turns ratio. A larger duty cycle would result in larger current ripple and increased switch voltage stress. A smaller duty cycle leads to high turns ratio, which increases the size of the coupled inductor. Hence, a compromise should be considered. In this design example, $D = 0.693$ and $n = 2$ are selected based on (4.26).

The magnetizing inductance of the coupled inductor can be designed based on the ripple ($\delta_m\%$) of the magnetizing current. The average magnetizing current I_m is calculated as 3A according to (4.36). Considering a peak-to-peak magnetizing current ripple to be less than 50% of the magnetizing current, the magnetizing inductance can be calculated as

$$L_m = \frac{V_{in}D}{\delta_m\%I_m f_s} > 92uH \tag{4.57}$$

Finally, the value of the magnetizing inductance is selected as 100uH.

The peak magnetizing current is calculated by

$$I_{m\_pk} = I_m + \frac{1}{2}\delta_m\%I_m = 4.5A \tag{4.58}$$

The leakage inductance of the coupled inductor helps limit the current falling rate and thus alleviate the diode reverse recovery problem. In order to effectively reduce the reverse recovery, di/dt of the diode should be less than 100A/us. Therefore, the minimum leakage inductance for alleviating the reverse recovery is given by

$$L_k = \frac{(n+1)V_o}{(1+(n+1)D)n^2\frac{di_{D2}}{dt}} > 0.49uH \tag{4.59}$$

On the other hand, if the leakage inductance is too large, the voltage gain becomes lower, hence the duty cycle has to be increased for compensation, which increases conduction losses. Therefore, a compromise should be considered when choosing the leakage inductance.

The design procedure of the coupled inductor in the proposed converter follows the flyback transformer design method, as they both have a two-winding structure and store DC energy. Powder cores are made of materials with evenly distributed air gap, which offers advantages of soft saturation, better temperature stability and lower fringing losses compared to ferrite cores with discrete air gap. Therefore, powder cores are used in the design. MPP core C055089A2 is chosen. The primary number of turns is selected as 25 and the secondary number of turns is 50.

B. Input inductor design

The input inductor is designed based on the required input current ripple ($\delta_{in}\%$). Considering the peak-to-peak input current ripple to be less than 15% of the input current, the input inductor can be calculated by

$$L = \frac{V_{in}D}{\delta_{in}\%I_{in}\,f_s} > 92uH \tag{4.60}$$

Finally, the value of the input inductance is selected as 100uH.

C. Semiconductor selection

The switches and diodes are selected according to their voltage and current stresses. The voltage stresses of the switch and diodes can be calculated from (4.29)-(4.31). The current stresses of the switch and diodes are given by (4.38)-(4.40). Considering the voltage overshoot and ringing in real applications, the voltage ratings of the selected devices should be higher than the calculated values.

D. Capacitor design

The capacitors can be designed based on the voltage ripple ($\delta_c\%$) and the output power P_o. Considering the voltage ripple to be less than 3% of the capacitor voltage. The calculations of the capacitors are given by

$$C_1 = \frac{(1+(n+1)D)(n+1)DP_o}{\delta_c\%{V_o}^2 f_s} > 10.7uF \tag{4.61}$$

$$C_2 = \frac{(1+(n+1)D)(n+1)((n+2)^2D+(n+1)(1-D)^2)P_o}{\delta_c\%(n+2)^2D{V_o}^2 f_s} > 17.4uF \tag{4.62}$$

$$C_o = \frac{(n+2)^2((n+2)^2D+(n+1)(1-D)^2)P_o}{\delta_c\%{V_o}^2 f_s} > 1.3uF \tag{4.63}$$

The voltage stresses of the energy transfer capacitors (C_1-C_2) can be calculated by (4.27)-(4.28), which are 65V and 45V, respectively. The voltage stress of the output capacitor is equal to the output voltage. The ripple currents of the capacitors can be calculated by (4.43)-(4.45), which are 4.5A, 5.0A and 1.6A, respectively.

Finally, 22uF film capacitors are selected for the energy transfer capacitors C_1 and C_2. In practice, considering the voltage overshoot during the load transient, larger output capacitor may be needed. In this design example, 56uF electrolytic capacitor is selected for the output capacitor C_o.

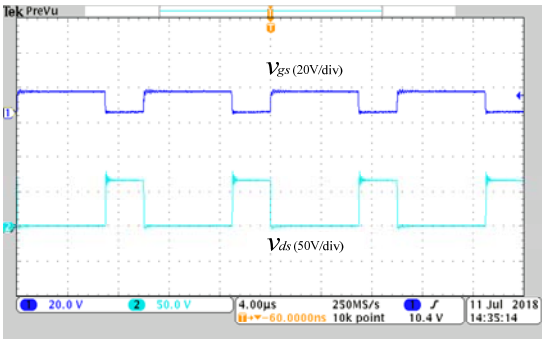
4.4 Experimental Results

In order to verify the performance of the proposed converter, a 200W 20V-input 200V-output prototype is built and tested. The switching frequency is set to 100kHz. The duty cycle of the switch is around 0.69. The key parameters of the prototype are listed as in Table 4.2.

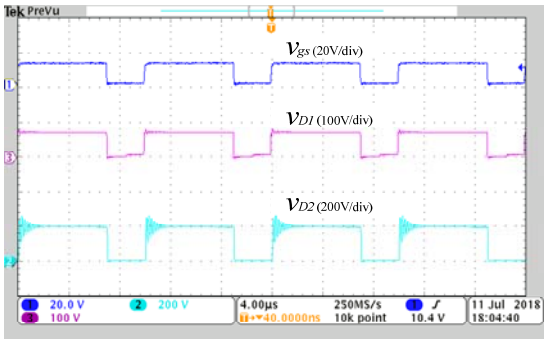
Table 4.2 Key parameters of the prototype

Parameters	VALUE/DESCRIPTION
Input voltage	20V
Output voltage	200V
Output power	200W
Switching frequency	100kHz
Switch	IPA075N15N3
Diodes D_1	STPS20200CT
Diodes D_2	STTH20L03C
Coupled inductor	Turns ratio = 25:50 Magnetizing inductance = 100uH Leakage inductance = 3.2uH
Input inductor	100uH
Capacitor C_1, C_2	22uF Film capacitor
Capacitor C_o	56uF electrolytic capacitor

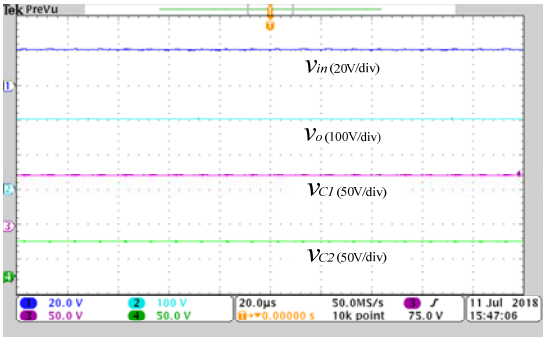
Fig. 4.13 (a) shows the driving signal and the drain-to-source voltage of the switch. It can be seen that extreme duty cycle is avoided. The voltage stress of the switch is at around 68V, which matches the calculation from (4.29). Fig. 4.13 (b) shows the voltages of the diodes. As can be seen, the blocking voltages of D_1 and D_2 are around 68V and 200V, respectively, which match the calculations from (4.30) and (4.31). Fig. 4.13 (c) shows that the input voltage is 20V and the output voltage is 200V. The capacitor voltages V_{C1} and V_{C2} are around 68V and 48V, respectively, which are consistent with the calculations from (4.27) and (4.28). Fig. 4.13 (d) shows the input current. It can be seen that continuous input current is achieved. Fig. 4.13 (e) shows the switch current and the primary current of the coupled inductor, which are consistent with the theoretical analysis. Fig. 4.13 (f) shows the currents through the diodes. It can be seen that reverse recovery problems of the diodes are alleviated. Fig. 4.13 (g) shows the measured efficiency curve. The measured peak efficiency is 94.1%, which is achieved at 125W. At the full load, the measured efficiency is 93.8%.



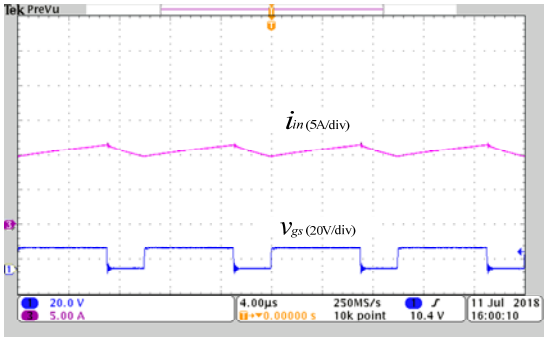
(a)



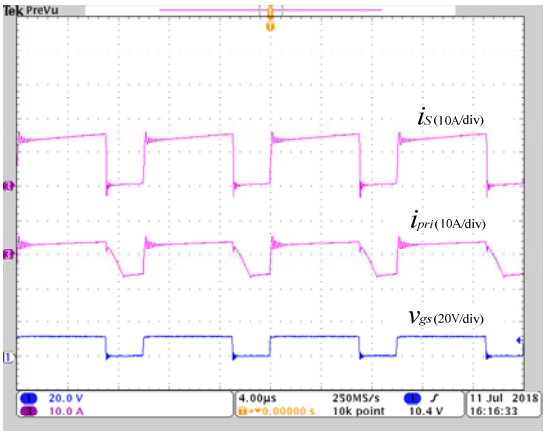
(b)



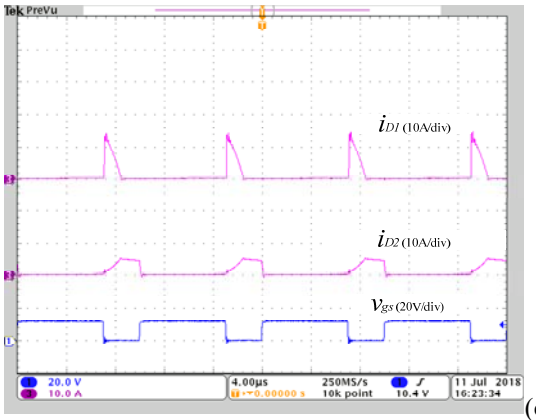
(c)



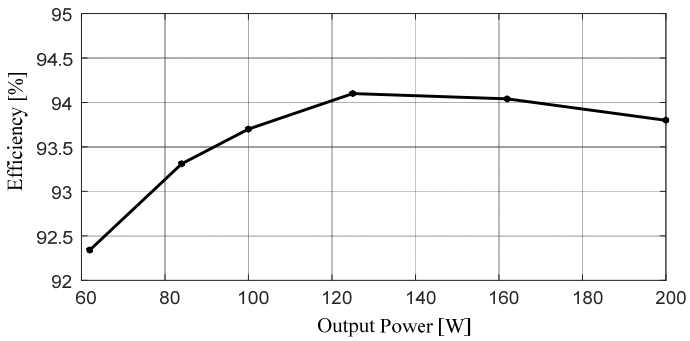
(d)



(e)



(f)

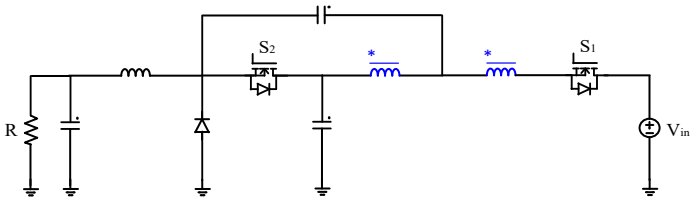


(g)

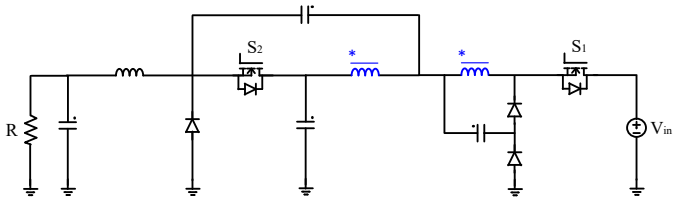
Fig. 4.13 Experimental results: (a) driving signal and drain-to-source voltage of the switch; (b) diode voltages; (c) input and output voltages and the capacitor voltages; (d) input current; (e) switch current and the primary current of the coupled inductor; (f) diode currents; (g) measured efficiency.

4.5 High Step-Down Extension

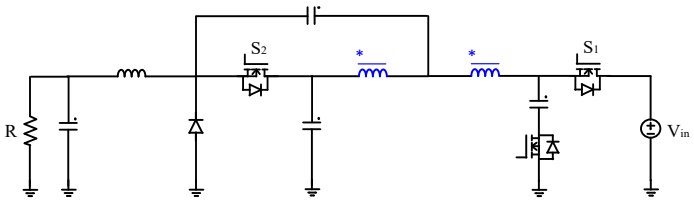
The proposed topology can be extended to high step-down operation as shown in Fig. 4.14 (a). Switch S_1 and S_2 are driven synchronously. However, the converter in Fig. 4.14 (a) has leakage problem. Passive clamp or active clamp circuit may be added to recycle the leakage energy, as shown in Fig. 4.14 (b) and (c), respectively.



(a)



(b)



(c)

Fig. 4.14 High step-down extension

Chapter 5 Improved Single-Phase Coupled-Inductor Boost Converter with Zero Voltage Switching and Zero Magnetizing Current

The single-phase converter presented in Chapter 4 has advantages like extended voltage gain, low component count, continuous input current and alleviated diode reverse recovery. However, the coupled inductor stores DC energy and the switch is turned on under hard switching. In order to overcome the shortcomings, an improved single-phase high step-up converter is introduced in this chapter. The new converter not only retains the continuous input current, but also achieves higher voltage gain and lower component voltage stress. Also the coupled inductor has no DC bias, resulting in small magnetic size and low core losses. Furthermore, zero-voltage switching of the switches is realized, leading to low switching losses.

The proposed converter and its operation principles are described in Section 5.1. Performance analysis are analyzed in Section 5.2. Design considerations are discussed in Section 5.3. Experimental results are presented in Section 5.4.

5.1 Topology and Operation Principles

The proposed converter is shown in Fig. 5.1. It is composed of one input inductor, one coupled inductor, two switches, two diodes, three energy transfer capacitors and one output capacitor. The two switches are driven complementary with dead time. Fig. 5.2 shows the equivalent circuit of the proposed converter. The coupled inductor is modeled as an ideal

transformer with magnetizing inductance (L_m) and leakage inductance (L_k). In order to simplify the analysis, the following assumptions are made: 1) all switches are composed of an ideal switch in parallel with its body-diode and drain-source capacitance; 2) all capacitors are large enough so that the voltages across them are constant without ripples; 3) the converter is operating in continuous conduction mode. The key waveforms of the proposed converter are shown in Fig. 5.3. Eight modes are observed during one switching period. The corresponding circuits in each mode are shown in Fig. 5.4.

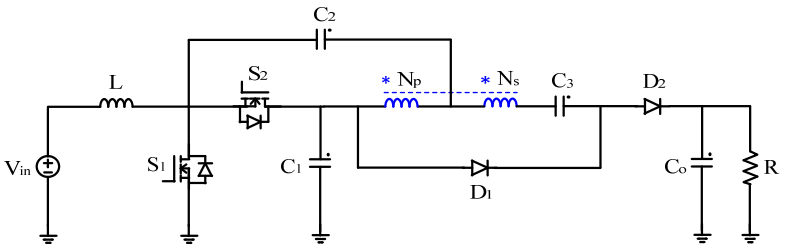


Fig. 5.1 Improved single-phase high step-up converter.

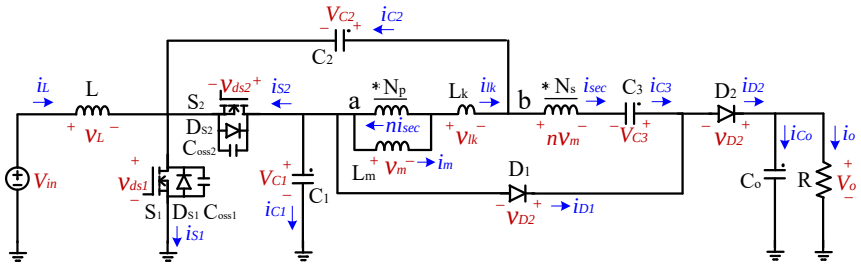


Fig. 5.2 The equivalent circuit.

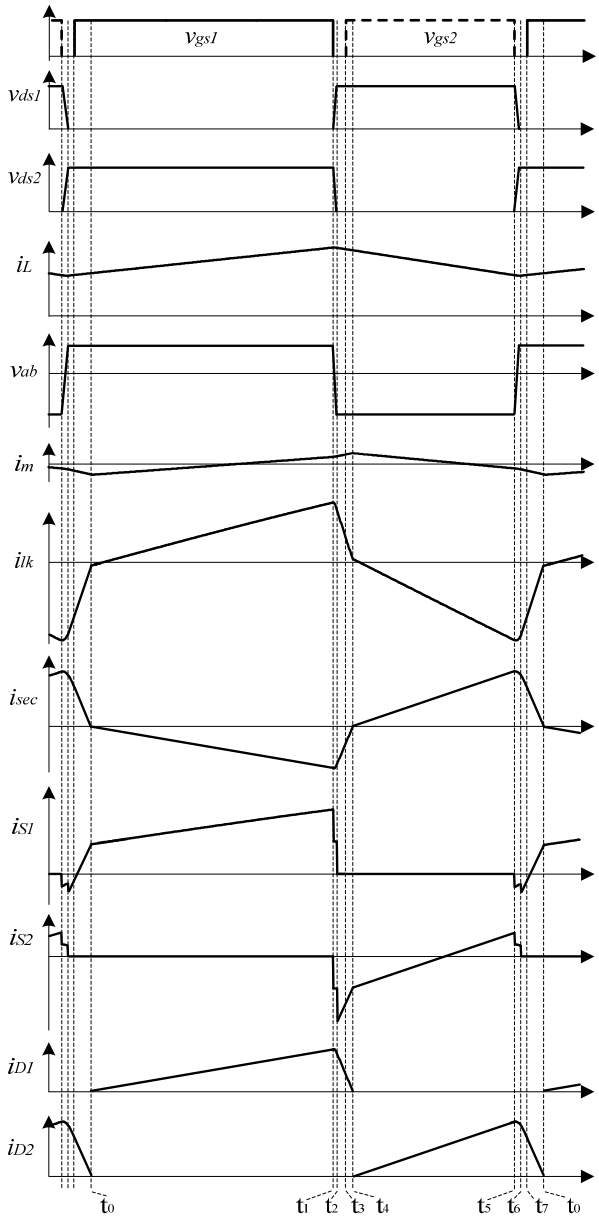


Fig. 5.3 Key waveforms

Mode 1 $[t_0$ - $t_1]$: Switch S_1 is on, and switch S_2 is off. The current flow paths are shown in Fig. 5.4 (a). The input inductor is being charged. The primary side of the coupled inductor is clamped at $V_{C1} - V_{C2}$, and the coupled inductor is magnetized. Capacitor C_1 is transferring a portion of its energy to C_2, and meanwhile, delivering the other portion of

the energy from primary winding N_p to secondary winding N_s to charge capacitor C_3 through diode D_1. The output capacitor releases energy to the load. The following equations can be obtained in this mode. As the leakage inductance is very small compared to the magnetizing inductance, the voltage of the leakage inductance has been neglected in the equations.

$$v_L = V_{in} \tag{5.1}$$

$$v_m = V_{C1} - V_{C2} \tag{5.2}$$

$$(n+1)v_m = V_{C3} \tag{5.3}$$

$$i_{D1}(t) = -i_{sec}(t) = \frac{(n+1)(V_{C1}-V_{C2})-V_{C3}}{n^2 L_k} t \tag{5.4}$$

Mode 2 [t_1 - t_2]: At t_1, switch S_1 is turned off. The output capacitances (C_{oss1}/C_{oss2}) of the switches are being charged/discharged, as shown in Fig. 5.4 (b). The voltage v_{ds1} across S_1 is increasing and the voltage v_{ds2} across S_2 is decreasing. This mode ends when v_{ds1} rises to V_{C1} and v_{ds2} drops to zero.

Mode 3 [t_2 - t_3]: At t_2, as v_{ds2} becomes zero, the body-diode of S_2 conducts, as shown in Fig. 5.4 (c). A voltage of $-V_{C2}$ is applied to the primary side of the coupled inductor. Therefore, i_{lk} is decreasing linearly, which makes i_{D1} decreasing linearly. The current changing rate is controlled by the leakage inductance of the coupled inductor. The following equation can be obtained in this mode.

$$i_{D1} = -i_{sec} = i_{D1}(t_2) - \frac{V_{C3}+(n+1)V_{C2}}{n^2 L_k} t \tag{5.5}$$

Mode 4 [t_3 - t_4]: At t_3, switch S_2 is turned on under ZVS, as shown in Fig. 5.4 (d). The other circuit conditions are the same as in the last mode. Equation (5.5) still holds.

Mode 5 [t_4 - t_5]: At t_4, i_{D1} decreases to zero and then D_1 is naturally turned off, which alleviates the reverse recovery problem. The secondary current i_{sec} changes its direction and diode D_2 starts conducting. The primary side of the coupled inductor is still clamped at $-V_{C2}$, and the coupled inductor is demagnetized. The current flow paths are shown in Fig. 5.4 (e). The boost inductor together with the input source is delivering energy to capacitor C_1. At the same time, capacitor C_2 is releasing energy via the coupled-inductor windings to the load. Meanwhile, the primary and secondary windings are linked in series with C_1 and C_3 to support the load. The following equations can be obtained in this mode.

$$v_L = V_{in} - V_{C1} \tag{5.6}$$

$$v_m = -V_{C2} \tag{5.7}$$

$$-(n+1)v_m + V_{C1} + V_{C3} = V_o \tag{5.8}$$

$$i_{D2} = i_{sec} = \frac{V_{C1}+(n+1)V_{C2}+V_{C3}-V_o}{n^2 L_k} t \tag{5.9}$$

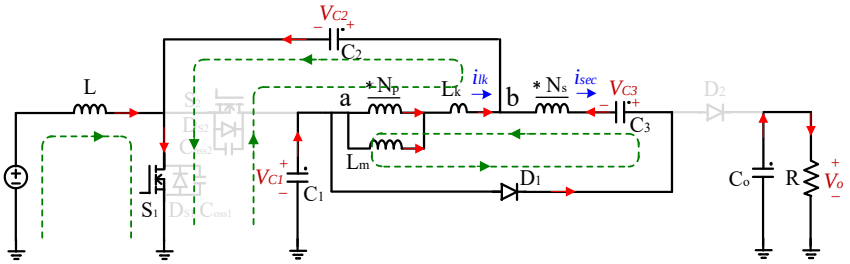
Mode 6 [t_5 - t_6]: At t_5, switch S_2 is turned off. The output capacitances (C_{oss1}/C_{oss2}) of the switches are being discharged/charged, as shown in Fig. 5.4 (f). v_{ds2} is increasing and v_{ds1} is decreasing. This mode ends when v_{ds2} rises to V_{C1} and v_{ds1} drops to zero.

Mode 7 [t_6 - t_7]: At t_6, as v_{ds1} becomes zero, the body-diode of S_1 conducts, as shown in Fig. 5.4 (g). A voltage of $V_{C1} - V_{C2}$ is applied to the primary side of the coupled inductor. Therefore, i_{lk} is decreasing linearly in the opposite direction, which makes i_{D2}

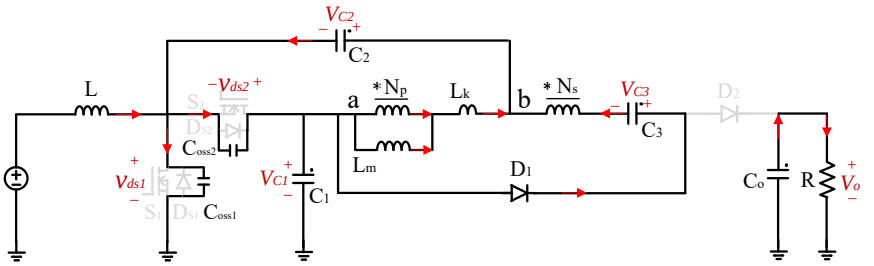
decreasing linearly. The current changing rate is controlled by the leakage inductance of the coupled inductor. The following equation can be obtained in this mode.

$$i_{D2} = i_{sec} = i_{D2}(t_6) - \frac{nV_{C1}+V_o-(n+1)V_{C2}-V_{C3}}{n^2 L_k} t \qquad (5.10)$$

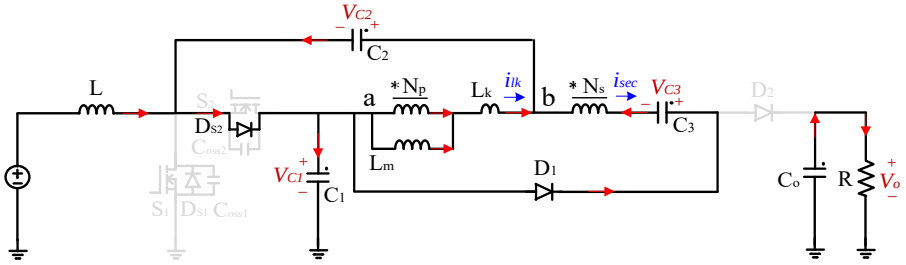
Mode 8 [t_7 - t_0]: At t_7, switch S_1 is turned on under ZVS, as shown in Fig. 5.4 (h). The other circuit conditions are the same as in the last mode. Equation (5.5) still holds. This mode ends when i_{D2} decreases to zero. At t_0, D_2 is naturally turned off, which alleviates the reverse recovery problem. After t_0, mode 1 begins.



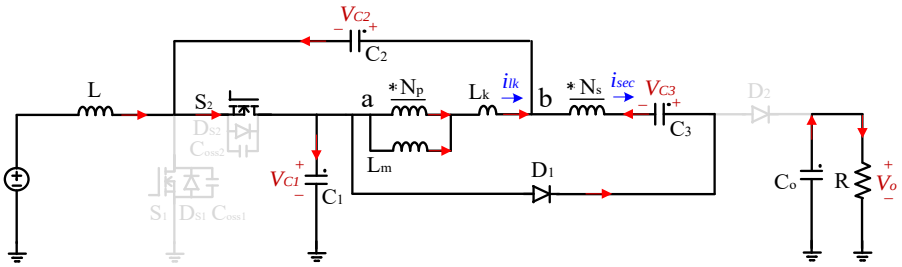
(a)



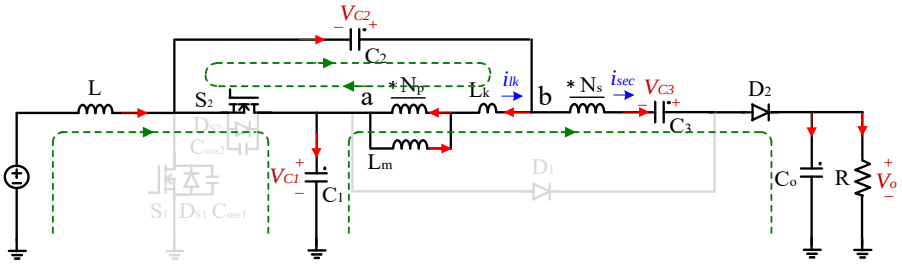
(b)



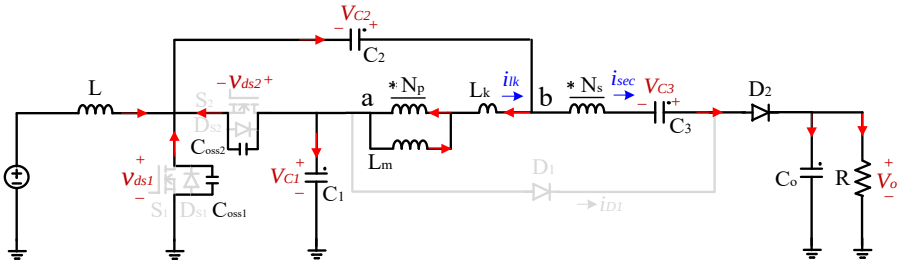
(c)


VC2
C2
L
S2
a
*Np
Lk
ilk
b
*Ns
isec
VC3
C3
D2
Ds2
Coss2
Lm
D1
VC1
C1
S1
Ds1
Coss1
Co
R
Vo

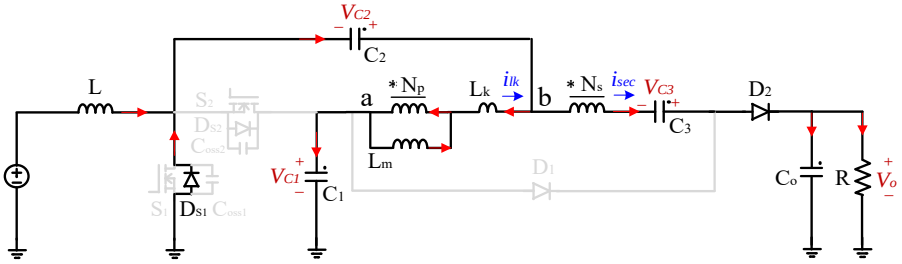
(d)


VC2
C2
L
S2
a
*Np
Lk
ilk
b
*Ns
isec
VC3
C3
D2
Ds2
Coss2
Lm
D1
VC1
C1
S1
Ds1
Coss1
Co
R
Vo

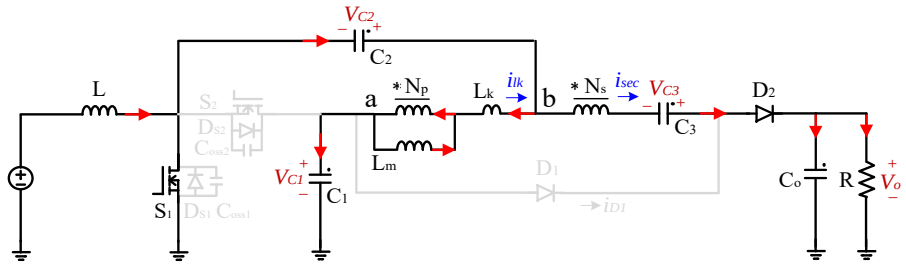
(e)


VC2
C2
L
−Vds2+
S2
a
*Np
Lk
ilk
b
*Ns
isec
VC3
C3
D2
Ds2
Coss2
Lm
D1
Vds1
VC1
C1
S1
Ds1
Coss1
iD1
Co
R
Vo

(f)


VC2
C2
L
S2
a
*Np
Lk
ilk
b
*Ns
isec
VC3
C3
D2
Ds2
Coss2
Lm
D1
VC1
C1
S1
Ds1
Coss1
Co
R
Vo

(g)



(h)

Fig. 5.4 Operation modes: (a) Mode 1 [t_0 - t_1]; (b) Mode 2 [t_1 - t_2]; (c) Mode 3 [t_2 - t_3]; (d) Mode 4 [t_3 - t_4]; (e) Mode 5 [t_4 - t_5]; (f) Mode 6 [t_5 - t_6]; (g) Mode 7 [t_6 - t_7]; (h) Mode 8 [t_7 - t_0].

5.2 Performance Analysis

A. Voltage Gain

In order to derive the ideal voltage gain, the effect of the leakage inductance and the transitional modes are neglected. By applying the voltage-second balance principle to L and L_m, the following equations are obtained.

$$V_{in}D + (V_{in} - V_{C1})(1 - D) = 0 \tag{5.10}$$

$$(V_{C1} - V_{C2})D - V_{C2}(1 - D) = 0 \tag{5.12}$$

Solving (5.10) and (5.12), the voltages of C_1 and C_2 are obtained as

$$V_{C1} = \frac{V_{in}}{1-D} \tag{5.13}$$

$$V_{C2} = \frac{DV_{in}}{1-D} \tag{5.14}$$

Solving (5.2) and (5.3), the voltage relationship between the capacitors is derived as

$$(n + 1)(V_{C1} - V_{C2}) = V_{C3} \tag{5.15}$$

Substituting (5.13) and (5.14) to (5.15), the voltage of C_3 is obtained as

$$V_{C3} = (n+1)V_{in} \tag{5.16}$$

Solving (5.7) and (5.8), the following relationship is derived.

$$V_{C1} + (n+1)V_{C2} + V_{C3} = V_o \tag{5.17}$$

Substituting (5.13), (5.14) and (5.16) to (5.17), the voltage gain of the proposed converter can be expressed as

$$M = \frac{V_o}{V_{in}} = \frac{n+2}{1-D} \tag{5.18}$$

The curves of the ideal voltage gain are plotted as in Fig. 5.5. High voltage gain can be achieved by adjusting turns ratio and duty cycle.

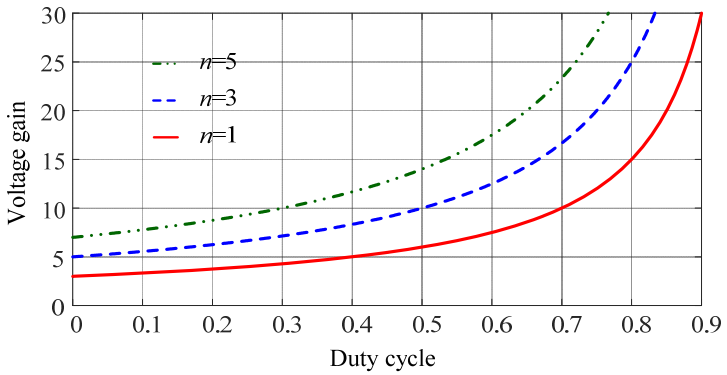


Fig. 5.5 Voltage gain versus turns ratio and duty cycle

In order to add the leakage inductance effect into the voltage gain, the diode current waveforms should be evaluated as the leakage inductance determines the slopes of the diode currents. Due to the charge balance of the output capacitor C_o, the average current of D_2 equals to the output current, which is given by

$$I_{D2\_avg} = I_{Co\_avg} + I_o = I_o \tag{5.19}$$

Due to the charge balance of capacitor C_3, the average current of D_1 equals to the average current of D_2, which is given by

$$I_{D1\_avg} = I_{D2\_avg} - I_{C3\_avg} = I_o \tag{5.20}$$

As the switching transitional intervals are very short compared to the power delivery modes, they are neglected in order to simplify calculation. Then from the diode current waveforms, the following equations are obtained.

$$\frac{1}{2} DT_s \cdot \frac{(n+1)(V_{C1}-V_{C2})-V_{C3}}{n^2 L_k} \cdot DT_s = I_o T_s \tag{5.21}$$

$$\frac{1}{2}(1-D)T_s \cdot \frac{V_{C1}+(n+1)V_{C2}+V_{C3}-V_o}{n^2 L_k} \cdot (1-D)T_s = I_o T_s \tag{5.22}$$

In addition, according to KVL, the following relationship is obtained.

$$-V_{in} + V_{L\_avg} - V_{C2} - V_{lk\_avg} - V_{m\_avg} + V_{C1} = 0 \tag{5.23}$$

where V_{L_avg}, V_{lk_avg} and V_{m_avg} are the average voltages of the inductances in one switching period. According to the voltage-second balance principle, they are equal to zero. Hence, (5.23) can be rewritten as

$$V_{C1} - V_{C2} = V_{in} \tag{5.24}$$

By applying the voltage-second balance to the boost inductor, V_{C1} still holds as in equation (5.13).

Solving (5.21), (5.22), (5.24) and (5.13), the voltage gain considering the leakage inductance can be expressed by

$$M = \frac{V_o}{V_{in}} = \frac{n+2}{1-D} \cdot \frac{1}{1+2n^2 Q\left(\frac{1}{D^2}+\frac{1}{(1-D)^2}\right)} \tag{5.25}$$

where $\mathrm{Q} = L_k f_s / R$.

Fig. 5.6 shows the voltage gain with the effect of the leakage inductance. It can be seen that as the leakage inductance increases, the voltage gain decreases, especially at high duty cycles. If the leakage inductance is ignored, (5.25) will be equal to (5.18).

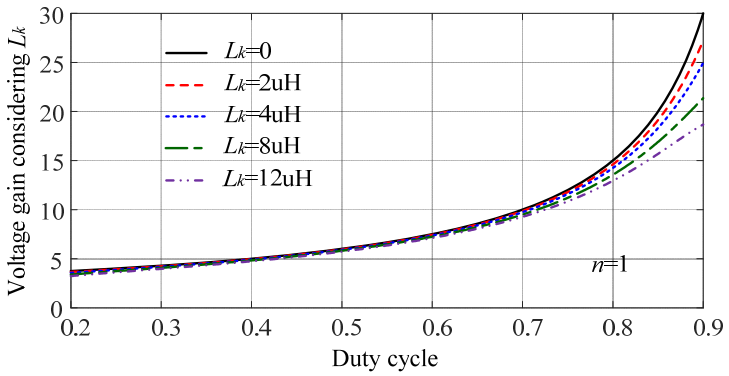


Fig. 5.6 Voltage gain considering the effect of leakage inductance (when $f_s = 100\text{kHz}$, $R_o = 400\Omega$).

B. Voltage and Current Stresses

From the steady-state operation, it can be seen that the voltages of the two switches are clamped by V_{C1}. Thus, the voltage stress of the switches is expressed as

$$V_{S1} = V_{S2} = \frac{1}{1-D} V_{in} = \frac{1}{n+2} V_o \tag{5.26}$$

The voltage stress of the switches is only a small fraction of the output voltage. Therefore, low-voltage-rating MOSFETs with small on-resistance can be adopted to lower the conduction loss.

From the steady-state operation, it can be seen that the voltages of the two diodes are clamped by $V_o - V_{C1}$. Thus, the voltage stresses of the diodes are given by

$$V_{D1} = V_{D2} = \frac{n+1}{1-D} V_{in} = \frac{n+1}{n+2} V_o \tag{5.27}$$

The semiconductor voltage stress normalized to the output voltage under different turns ratios are plotted in Fig. 5.7. It can be seen that the switch voltage stress becomes lower as the voltage gain is extended by increasing the turns ratio. The diode voltage stress increases with the turns ratio, but they are always lower than the output voltage.

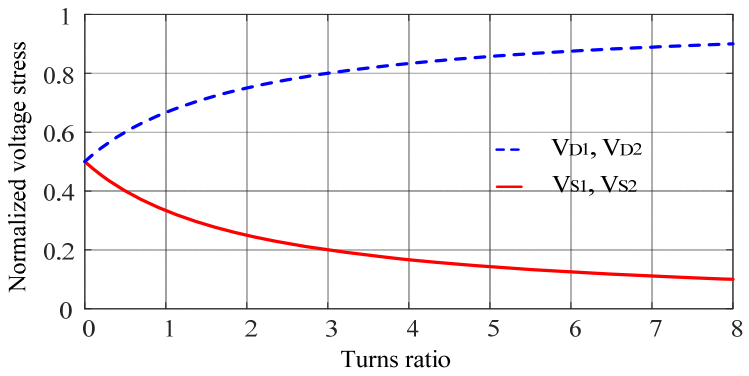


Fig. 5.7 Normalized semiconductor voltage stresses

As the average currents of the diodes equal to the output current, the peak currents of the diodes can be expressed by

$$I_{D1\_peak} = \frac{2I_o}{D} \tag{5.28}$$

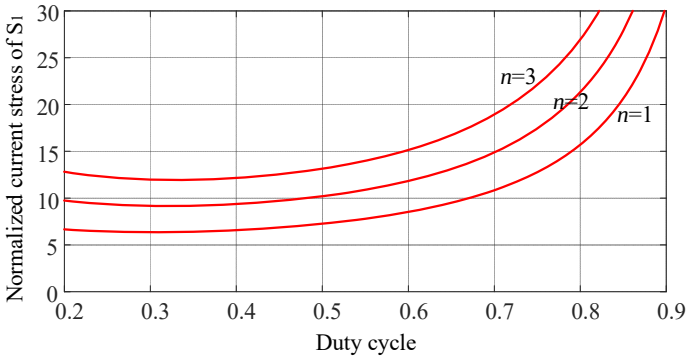
$$I_{D2\_peak} = \frac{2I_o}{1-D} \tag{5.29}$$

. From the steady-state analysis, the RMS currents of the switches can be evaluated as

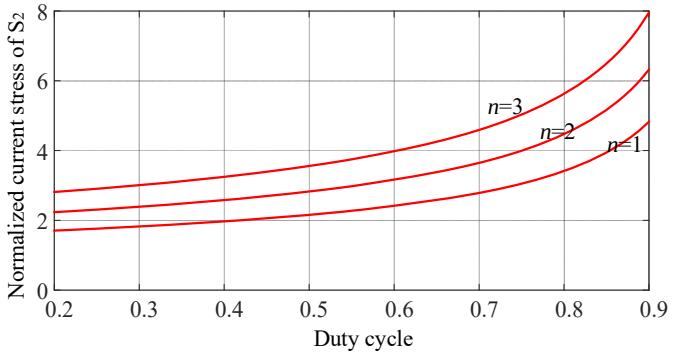
$$I_{S1\_rms} = I_o\sqrt{\frac{4(n+1)^2}{3D} + \frac{2(n+1)(n+2)}{1-D} + \frac{D(n+2)^2}{(1-D)^2}} \tag{5.30}$$

$$I_{S2\_rms} = I_o\sqrt{\frac{4(n+1)^2-3n(n+2)}{3(1-D)}} \tag{5.31}$$

The switch RMS currents normalized by the output current are plotted Fig. 5.8. It can be seen that the switch current stress increases by increasing the turns ratio or decreasing the duty cycle.



(a)



(b)

Fig. 5.8 Switch RMS current stress normalized by I_o versus duty cycle under different turns ratio and different voltage gain: (a) S_1; (b) S_2.

The RMS currents through the windings of the coupled inductor can be evaluated as

$$I_{lk\_rms} = \frac{2nI_o}{\sqrt{3D(1-D)}} \tag{5.32}$$

$$I_{sec\_rms} = \frac{2I_o}{\sqrt{3D(1-D)}} \tag{5.33}$$

C. DC offset of the magnetizing current

As the secondary winding of the coupled inductor is connected in series with capacitor C_3, the average secondary current is given by

$$I_{sec\_avg} = I_{C3\_avg} = 0 \tag{5.34}$$

The relationship between the primary current and the secondary current of the coupled inductor can be written as

$$I_{pri\_avg} = I_{m\_avg} - nI_{sec\_avg} \tag{5.35}$$

$$I_{pri\_avg} - I_{sec\_avg} = I_{C2\_avg} \tag{5.36}$$

Solving (5.35)-(5.36) and considering the charge balance of capacitor C_2, the average magnetizing current can be evaluated as

$$I_{m\_avg} = (n+1)I_{sec\_avg} + I_{C2_{avg}} = 0 \tag{5.37}$$

It can be seen that the coupled inductor in the proposed converter has no DC-bias flux density due to the charge balance of the capacitors, operating like an ac transformer. Therefore, un-gapped cores can be employed, and small magnetic size and low core loss are achieved.

D. ZVS condition

The proposed converter is capable of achieving ZVS of the switches, which reduces the switching loss. ZVS turn-off is realized due to the output capacitances of the switches, which limit the rising rate of the switch voltage at the turn-off instant. ZVS turn-on can be achieved by gating on the switch while the body-diode is conducting.

According to mode 2, ZVS of switch S_2 is always achieved because the input inductor current helps charge/discharge the output capacitances.

According to mode 6, in order to achieve ZVS of switch S_1, the following two conditions must be satisfied. 1) $i_L(t_5) + i_{C2}(t_5)$ must be smaller than zero in order to discharge C_{oss1} and charge C_{oss2}. 2) The inductive energy available must be sufficient so that $i_L + i_{C2}$ will still remain negative after C_{oss1}/C_{oss2} are completely discharged/charged. Then the current could flow through the body-diode of S_1 and thus ZVS can be achieved.

$i_L(t_5) + i_{C2}(t_5)$ can be written as

$$i_L(t_5) + i_{C2}(t_5) = i_L(t_5) + i_m(t_5) - (n+1)i_{sec}(t_5)$$

$$= I_L - \frac{\Delta i_L}{2} - \frac{\Delta i_m}{2} - (n+1)I_{D2_{peak}} \quad (5.38)$$

where Δi_L and Δi_m are the peak-to-peak current ripple of the boost inductor and magnetizing inductance, respectively, They are given by

$$\Delta i_L = \frac{V_{in}D}{Lf_s}; \quad \Delta i_m = \frac{V_{in}D}{L_m f_s} \quad (5.39)$$

Neglecting the power losses, the inductor current is given by

$$I_L = \frac{n+2}{1-D} I_o \quad (5.40)$$

Substituting (5.29), (5.39) and (5.40) to (5.38), the following is obtained.

$$i_L(t_5) + i_{C2}(t_5) = -\frac{nI_o}{1-D} - \frac{V_{in}D}{2f_s}\left(\frac{1}{L} + \frac{1}{L_m}\right) < 0 \quad (5.41)$$

It can be seen from (5.41) that the first condition for ZVS of S_1 is always achieved. In order to satisfy the second condition, the following can be obtained.

$$\frac{1}{2}L_k(nI_{D2_{peak}})^2 - \frac{1}{2}L_k\left(\frac{n}{n+1}I_L\right)^2 > \frac{1}{2}(C_{oss1} + C_{oss2})\,{V_{C1}}^2 \quad (5.42)$$

Substituting (5.13), (5.29) and (5.40) to (5.42), the ZVS condition can be rewritten as

$$(4 - \frac{(n+2)^2}{(n+1)^2})n^2 L_k {I_o}^2 > (C_{oss1} + C_{oss2}){V_{in}}^2 \quad (5.43)$$

It can be seen from (5.43) that the ZVS region is related to the leakage inductance, output current and turns ratio. The leakage inductance versus output current under different turns ratio is plotted in Fig. 5.9. As can be seen, larger turns ratio or larger leakage inductance lead to wider ZVS range. Also, it is easier to achieve ZVS when the output current increases. This scenario is practically workable. Since at heavy load, ZVS is achieved to minimize the switching losses, while at light load, even the soft switching is lost, the total losses are still manageable.

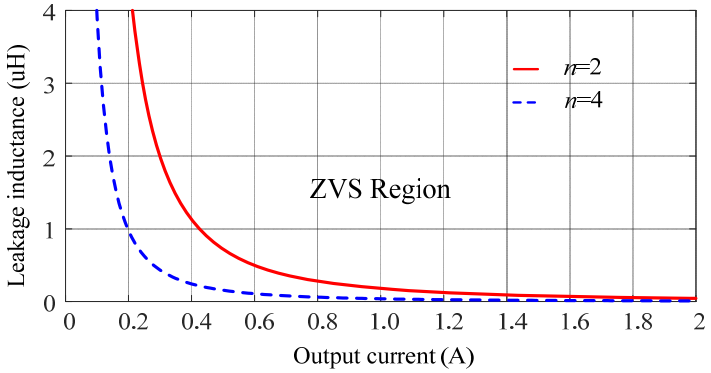


Fig. 5.9 ZVS condition (when $V_{in} = 40V$, $C_{oss1} = C_{oss2} = 0.5nF$).

5.3 Design Considerations

The design specifications are given as the following. V_{in} is the input voltage, V_o is the output voltage, P_o is the output power, f_s is the switching frequency, $r_L\%$ is the input

current ripple, $r_{c1}\%, r_{c2}\%, r_{c3}\%,$ and $r_{co}\%$ are the capacitor voltage ripple of C_1, C_2, C_3 and C_o, respectively.

A. Input inductor design

The input inductor is designed based on the input current ripple requirement. Considering a peak-to-peak current ripple of Δi_{in}, the boost inductor can be calculated by

$$L = \frac{V_{in}D}{r_L\%I_L f_s} \tag{5.44}$$

B. Coupled inductor design

The turns ratio of the coupled inductors is determined by the required voltage gain and the duty cycle. A large duty cycle results in low turns ratio, which would increase the switch voltage stress, leading to a use of higher voltage rating MOSFETs with larger on-resistance. On the other hand, if the duty cycle is too small, a high turns ratio is needed, which causes high conduction loss and large leakage inductance. Therefore, a compromise should be considered when selecting the duty cycle according to the particular applications. One proper duty cycle is chosen, the turns ratio can be calculated by from (5.18).

The leakage inductance of the coupled inductor determines the boundary of the ZVS region for the switches. Given the minimum load to achieve ZVS, the required leakage inductance can be calculated from (5.43).

C. Semiconductor selection

The switches and diodes are selected according to their voltage and current stresses. The voltage stresses of the switch and diodes can be calculated from (5.26)-(5.27). The

current stresses of the switch and diodes are given by (5.28)-(5.31). Considering the voltage overshoot and ringing in practice, the voltage ratings of the selected devices should be higher than the calculated values.

D. Capacitor design

The capacitors can be designed based on the voltage ripple and the output power. The calculations of the capacitors are given by

$$C_1 = \frac{(n+1)I_o}{\Delta V_{c1} f_s} = \frac{(n+1)(n+2)P_o}{r_{c1}\%{V_o}^2 f_s} \tag{5.45}$$

$$C_2 = \frac{(n+1)I_o}{\Delta V_{c2} f_s} = \frac{(n+1)(n+2)P_o}{r_{c2}\%D{V_o}^2 f_s} \tag{5.46}$$

$$C_3 = \frac{I_o}{\Delta V_{c3} f_s} = \frac{(n+2)P_o}{r_{c3}\%(n+1)(1-D){V_o}^2 f_s} \tag{5.47}$$

$$C_o = \frac{DI_o}{\Delta V_o f_s} = \frac{DP_o}{r_{co}\%{V_o}^2 f_s} \tag{5.48}$$

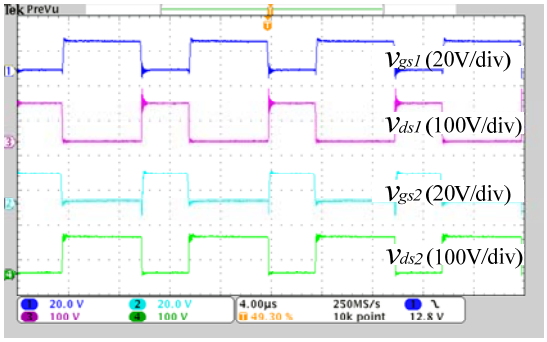
5.4 Experimental Results

Table 5.1 Key parameters of the prototype

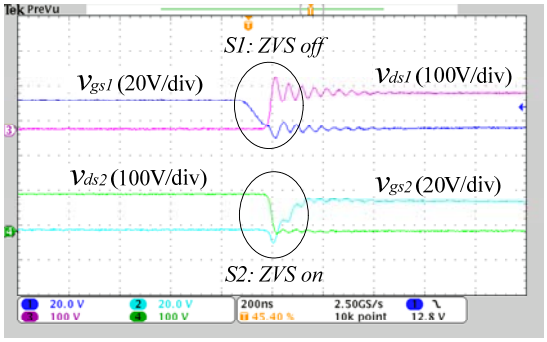
Components	PARAMETERS
Switch S_1-S_2	IPA075N15N3
Diode D_1-D_2	MUR1640CT
Coupled inductor	Turns ratio = 2 Magnetizing inductance = 208uH Leakage inductance = 2.6uH
Input inductor	100uH
Capacitor C_1-C_3	30uF film capacitor
Capacitor C_o	2×56uF electrolytic capacitor

In order to verify the performance of the proposed converter, a 400W 40V-input 400V-output prototype was built and tested. The switching frequency is 100kHz. The duty cycle is around 0.6. The key parameters of the prototype are listed as in Table 5.1.

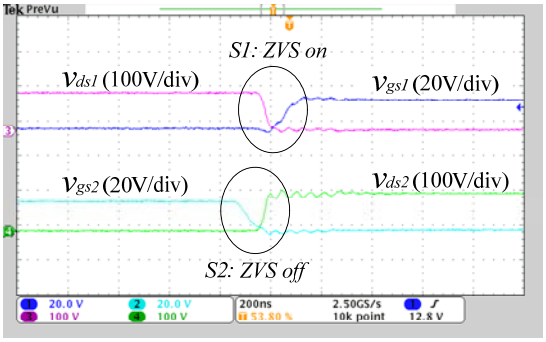
Fig. 5.10 (a) shows the gate signals and drain-to-source voltages of the switches. It can be seen that the blocking voltage of the switches is around 100V, which is consistent with the calculation from (5.26). The horizontally enlarged waveforms at the switching transitions are provided in Fig. Fig. 5.10 (b) and (c). It can be seen that the switches are turned on and turned off under zero voltage. Therefore, ZVS of the switches are achieved. Fig. 5.10 (d) shows the voltages of the diodes. It can be seen that the blocking voltage of the diodes is around 300V, which is consistent with the calculation from (5.27). Fig. 5.10 (e) shows the current waveforms of the diodes. It can be seen that the reverse recovery problem of the diodes is significantly alleviated. Fig. 5.10 (f) and (g) shows the primary current, the secondary current and the primary voltage of coupled inductor, which are consistent with the theoretical analysis. Fig. 5.10 (g) also shows the voltages across the capacitors C_1-C_3. It can be seen that V_{C1}, V_{C2} and V_{C3} are around 100V, 63V and 120V respectively, which agree with the calculations from (5.13), (5.14) and (5.16). Fig. 5.10 (h) shows the input current of the proposed converter. It can be seen that continuous input current is achieved, which is beneficial to most applications. The measured efficiency versus output power is shown in Fig. 5.10 (i). The peak efficiency is 95.2%, which is achieved at 250W. The efficiency at the full load is measured as 94.8%.


Tek PreVu
v_{gs1} (20V/div)
v_{ds1} (100V/div)
v_{gs2} (20V/div)
v_{ds2} (100V/div)

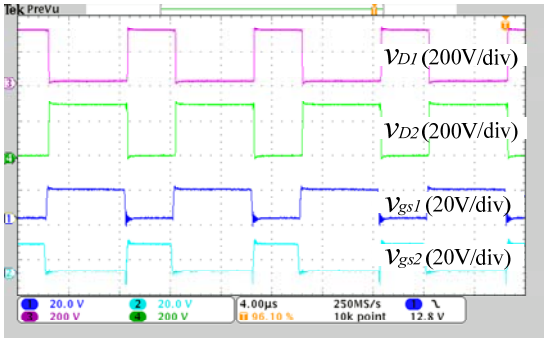
(a)


Tek PreVu
S1: ZVS off
v_{gs1} (20V/div)
v_{ds1} (100V/div)
v_{ds2} (100V/div)
v_{gs2} (20V/div)
S2: ZVS on

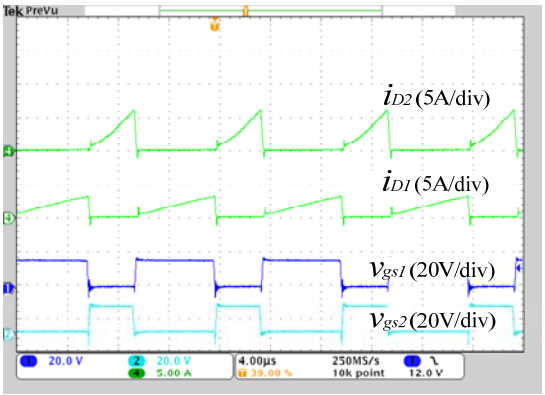
(b)


Tek PreVu
S1: ZVS on
v_{ds1} (100V/div)
v_{gs1} (20V/div)
v_{gs2} (20V/div)
v_{ds2} (100V/div)
S2: ZVS off

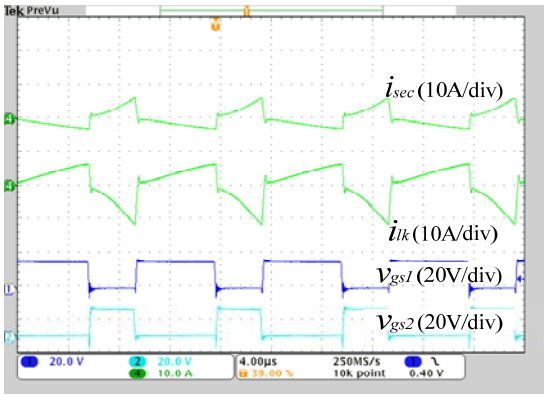
(c)


Tek PreVu
v_{D1} (200V/div)
v_{D2} (200V/div)
v_{gs1} (20V/div)
v_{gs2} (20V/div)

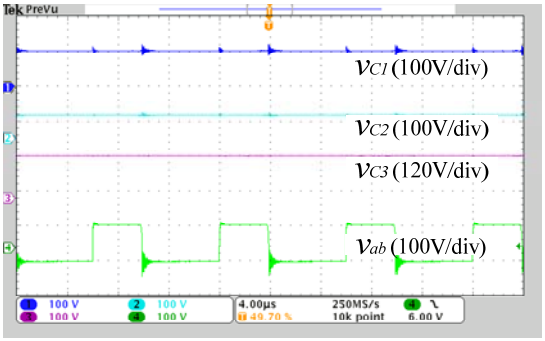
(d)


Tek PreVu
i_{D2} (5A/div)
i_{D1} (5A/div)
v_{gs1} (20V/div)
v_{gs2} (20V/div)

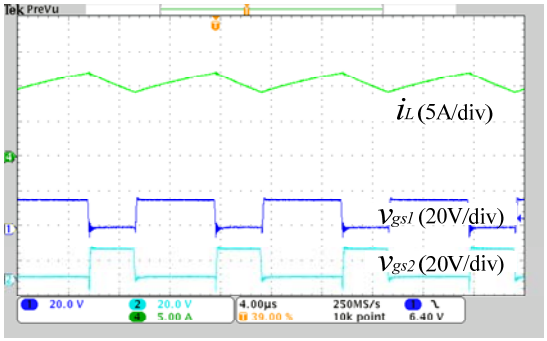
(e)


Tek PreVu
i_{sec} (10A/div)
i_{lk} (10A/div)
v_{gs1} (20V/div)
v_{gs2} (20V/div)

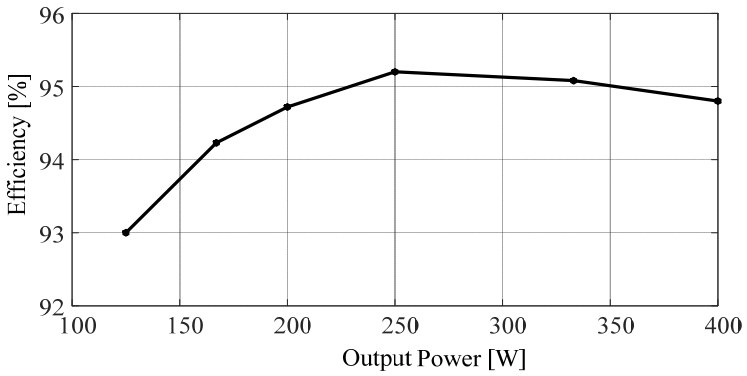
(f)


Tek PreVu
v_{C1} (100V/div)
v_{C2} (100V/div)
v_{C3} (120V/div)
v_{ab} (100V/div)

(g)


Tek PreVu
i_L (5A/div)
v_{gs1} (20V/div)
v_{gs2} (20V/div)

(h)



(i)

Fig. 5.10 Experimental results: (a) Gate signals and drain-to-source voltages of the switches; (b) ZVS off of S_1 and ZVS on of S_2; (c) ZVS on of S_1 and ZVS off of S_2; (d) Diode voltages; (e) Diode currents; (f) The primary current (i_{lk}) and the secondary current (i_{sec}) of the coupled inductor; (g) Capacitor voltages ($v_{C1} - v_{C3}$) and the primary voltage (v_{ab}) of the coupled inductor; (h) Input current; (i) Measured efficiency versus output power.

5.5 High Step-Down Extension

The proposed topology can be extended to high step-down operation, as shown in Fig. 5.11. Switch S_1 and S_2 are driven complementary with a dead time. Switch S_3 and S_1 are driven synchronously. This step-down structure is slightly different from the step-up one in Fig. 5.1. Switch S_2 becomes grounded instead of floating. Such a change helps recycle the leakage energy; thus, no additional snubber is needed.

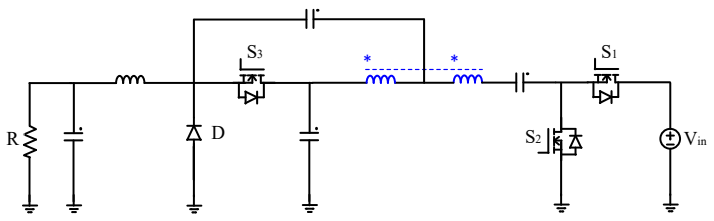


Fig. 5.11 High step-down extension

Chapter 6 High Step-Down Converter with Zero-Voltages Switching and Low Current Ripples

In this chapter, a non-isolated high step-down converter is introduced. Energy transfer capacitor and built-in transformer are employed to achieve a very high step-down conversion ratio. Due to the interleaved technique, small values of output inductance can be used, leading to fast transient response. Furthermore, the use of a coupled inductor reduces inductor current ripples, which implies lower losses. Two main switches and two synchronous rectifiers are used in the converter and all can achieve zero-voltage-switching. As no floating switches are employed, grounded gate drivers and boost strap drivers can be used, avoiding the use of complex isolated gate drivers. In addition, if one of the switches fails, the high input voltage does not appear at the output, thus the load is protected.

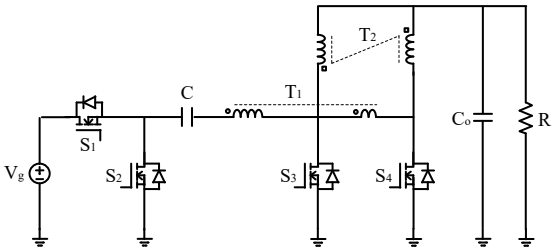
The proposed converter and its operation principles are described in Section 6.1. Performance analysis are analyzed in Section 6.2. Design considerations are discussed in Section 6.3. Experimental results are presented in Section 6.4.

6.1 Topology and Operation Principles

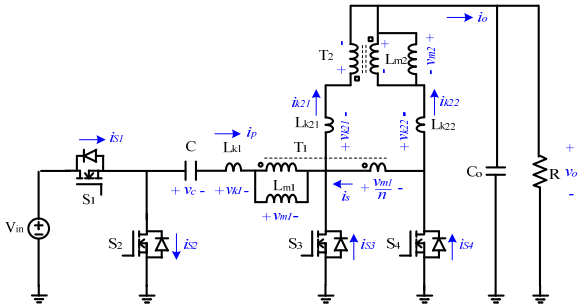
Fig. 6.1 (a) shows the proposed converter, which contains two main switches S_1, S_2, two synchronous rectifiers S_3, S_4, one energy transfer capacitor C, one output capacitor C_o, one transformer T_1 and one coupled inductor T_2. The equivalent circuit of the proposed converter is shown in Fig. 6.1 (b). Both T_1 and T_2 are modeled as an ideal transformer with magnetizing inductance and leakage inductance. The secondary-side leakage inductance of

T_1 can be neglected as it is very small. The magnetizing current of T_1 can be both positive and negative, thus T_1 operates with bidirectional magnetic flux and stores little energy. It is a transformer. The leakage inductance of T_2 is large compared to its magnetizing inductance, thus it stores energy and it is a coupled inductor.

Switches S_1 and S_2 are driven complementary with a dead time, while S_2 and S_3 are driven synchronously, and so are S_4 and S_1. S_1 and S_2 can be driven by a simple bootstrap gate driver, while S_3 and S_4 can be driven by low-side gate drivers.



(a)



(b)

Fig. 6.1 Proposed high step-down converter: (a) main structure; (b) equivalent circuit.

In order to simplify the analysis, the following assumptions are made: 1) all switches are ideal except for their body-diode; 2) C and C_o are large enough so that the voltages across them are constant; 3) turns ratio of the coupled inductor T_2 is 1:1 and it is assumed that $L_{k21} = L_{k22} = L_{k2}$; 4) turns ratio of the transformer T_1 is n:1.

The key waveforms of the proposed converter are shown in Fig. 6.2. The operation in one switching cycle can be divided into six modes. The corresponding circuits for each mode are shown in Fig. 6.3.

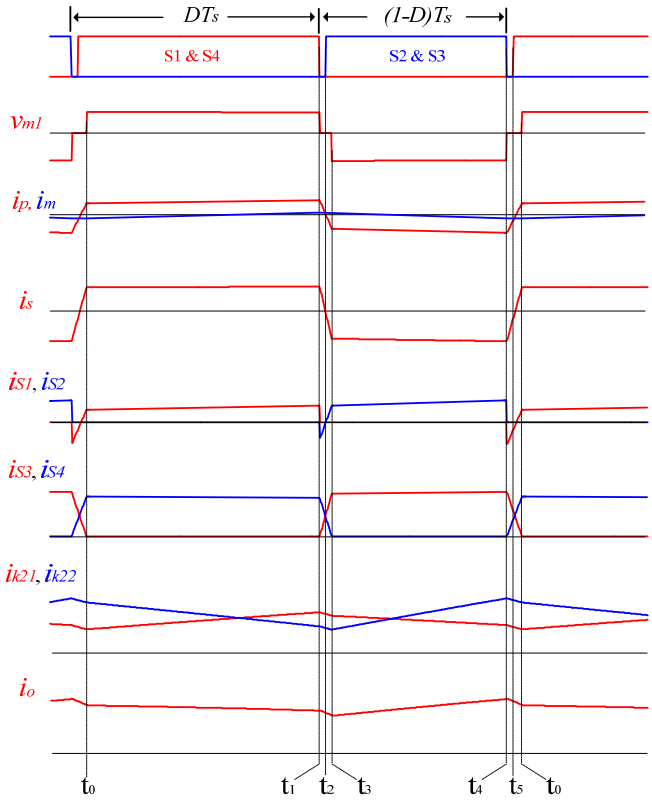


Fig. 6.2 Key waveforms of the proposed converter

Mode 1 $[t_0 - t_1]$: As shown in Fig. 6.3 (a), S_1 and S_4 are on, while S_2 and S_3 are off. The energy transfer capacitor C is being charged. The transformer T_1 is magnetized. i_{k21} and i_{k22} are currents in the two windings of the coupled inductor. i_{k21} is increasing while i_{k22} is decreasing. v_{k1} is negligible here as i_p is almost constant. Then the following equations can be obtained.

$$V_{in} - V_C = v_{m1} + v_{m1}/n \tag{6.1}$$

$$i_p + n(i_p - i_m) = i_{k21} \tag{6.2}$$

$$L_{k2}\frac{\mathrm{d}i_{k21}}{\mathrm{dt}} = v_{k21} = v_{m1}/n - v_{m2} - V_o \tag{6.3}$$

$$L_{k2}\frac{\mathrm{d}i_{k22}}{\mathrm{dt}} = v_{k22} = v_{m2} - V_o \tag{6.4}$$

$$v_{m2} = L_{m2}\frac{\mathrm{d}i_{m2}}{\mathrm{dt}} = L_{m2}\left(\frac{\mathrm{d}i_{k21}}{\mathrm{dt}} - \frac{\mathrm{d}i_{k22}}{\mathrm{dt}}\right) \tag{6.5}$$

Substituting (6.3) and (6.4) into (6.5), v_{m2} can be solved as

$$v_{m2} = \frac{L_{m2}}{L_{k2}+2L_{m2}} \cdot \frac{V_{in}-V_C}{n+1} \tag{6.6}$$

Mode 2 [t_1 - t_2]: At t_1, S_1 and S_4 are turned off. Due to presence of the leakage inductance L_{k1}, the body diode of S_2 turns on, and then the body diodes of S_3 and S_4 are both forward-biased, as shown in Fig. 6.3 (b). Therefore, ZVS conditions of S_2 and S_3 are achieved. During this mode, v_{m1} becomes zero. $-V_C$ is imposed to the leakage inductance L_{k1}, causing i_p to decrease. i_s is decreasing as well. Both i_{k21} and i_{k22} are decreasing.

$$L_{k1}\frac{\mathrm{d}i_p}{\mathrm{dt}} = -V_C \tag{6.7}$$

$$L_{k2}\frac{\mathrm{d}i_{k21}}{\mathrm{dt}} = -v_{m2} - V_o \tag{6.8}$$

$$L_{k2}\frac{\mathrm{d}i_{k22}}{\mathrm{dt}} = v_{k22} = v_{m2} - V_o \tag{6.9}$$

Substituting (6.8) and (6.9) into (6.5), v_{m2} can be solved as

$$v_{m2} = 0 \tag{6.10}$$

Mode 3 [t_2 - t_3]: At t_2, both S_2 and S_3 are turned on under ZVS. S_1 still keeps off and the body diode of S_4 still keeps on, as shown in Fig. 6.3 (c). v_{m1} remains zero, and i_p and i_s remains decreasing. Both i_{k21} and i_{k22} are decreasing. Equations (6.7)-(6.10) still hold.

Mode 4 [t_3 - t_4]: At t_3, i_s rises in the negative direction to i_{k22}, and the current in the body diode of S_4 decreases to zero and then the body diode turns off. S_2 and S_3 keep on and S_1 keeps off, as shown in Fig. 6.3 (d). During this mode, the capacitor *C* is releasing energy. The transformer is demagnetized. i_{k21} is decreasing while i_{k22} is increasing. The following equations can be obtained.

$$-V_C = v_{m1} \tag{6.12}$$

$$n\left(i_p - i_m\right) = -i_{k22} \tag{6.12}$$

$$L_{k2}\frac{\mathrm{d}i_{k21}}{\mathrm{dt}} = v_{k21} = -v_{m2} - V_o \tag{6.13}$$

$$L_{k2}\frac{\mathrm{d}i_{k22}}{\mathrm{dt}} = v_{k22} = v_{m2} - V_o - v_{m1}/n \tag{6.14}$$

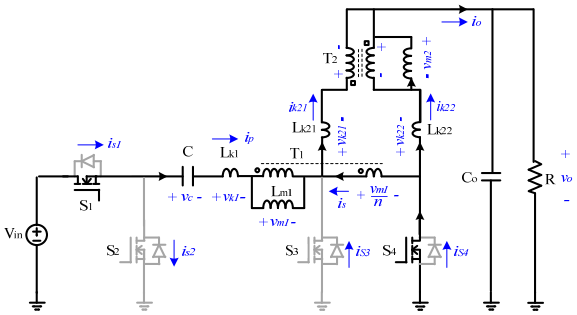
Substituting (6.13) and (6.14) into (6.5), v_{m2} can be solved as

$$v_{m2} = \frac{L_{m2}}{L_{k2}+2L_{m2}} \cdot \frac{-V_C}{n} \tag{6.15}$$

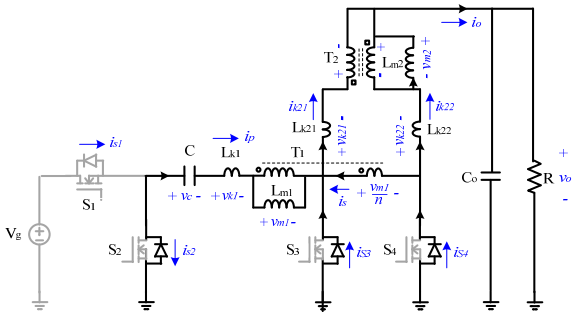
Mode 5 [t_4 - t_5]: At t_4, S_2 and S_3 are turned off. Due to presence of L_{k1}, the body diode of S_1 turns on, and then the body diodes of S_3 and S_4 are both forward-biased, as shown in Fig. 6.3 (e). Therefore, ZVS conditions of S_2 and S_3 are achieved. During this mode, v_{m1} becomes zero. $V_{in} - V_C$ is imposed to the leakage inductance L_{k1}, causing i_p to increase. i_s is increasing as well. Both i_{k21} and i_{k22} are decreasing. Equations (6.8)-(6.10) are satisfied and the following equation can be obtained.

$$L_{k1}\frac{\mathrm{d}i_p}{\mathrm{dt}} = V_{in} - V_C \tag{6.16}$$

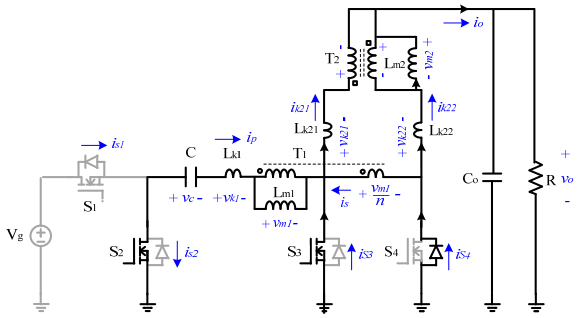
Mode 6 [t_5 - t_0]: At t_5, both S_1 and S_4 are turned on under ZVS. S_2 still keeps off and the body diode of S_3 still keeps on, as shown in Fig. 6.3 (f). v_{m1} remains zero, and i_p and i_s remains increasing. Both i_{k21} and i_{k22} are decreasing. This mode ends at t_0. At t_0, $i_p + i_s$ rises in the positive direction to i_{k21}, and the current in the body diode of S_3 decreases to zero and then turns off. Then mode 1 begins. Equations (6.8)-(6.10) and (6.16) still hold.



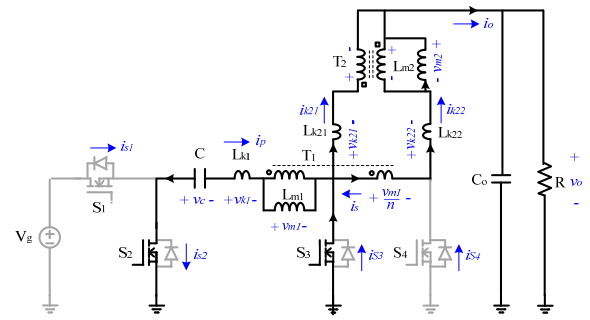
(a)



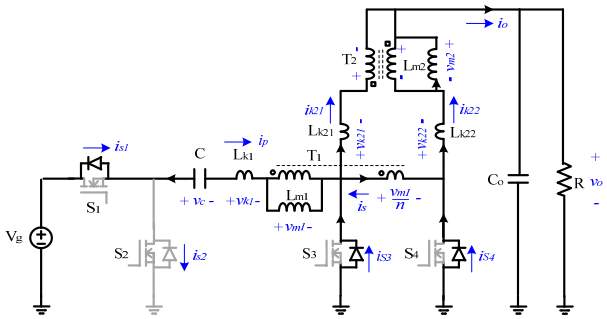
(b)



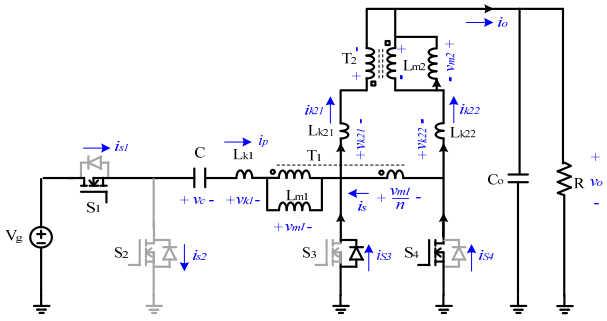
(c)



(d)



(e)



(f)

Fig. 6.3 Corresponding circuits for each mode: (a) mode 1; (b) mode 2; (c) mode 3; (d) mode 4; (e) mode 5; (f) mode 6.

6.2 Performance Analysis

A. Voltage gain

To derive the voltage gain of the proposed converter, only mode 1 and mode 4 are considered. The duty cycle of S_1 is defined as D. By applying the voltage-second balance principle to L_{m1}, the following equation can be obtained:

$$\frac{n}{n+1}(V_{in} - V_C)D - V_C(1 - D) = 0 \tag{6.17}$$

Based on (6.17), the capacitor voltage V_C can be expressed as

$$V_C = \frac{nD}{n+1-D}V_{in} \tag{6.18}$$

By applying the voltage-second balance principle to L_{k22}, the following equation can be obtained:

$$\left(\frac{L_{m2}}{L_{k2}+2L_{m2}} \cdot \frac{V_{in}-V_C}{n+1} - V_o\right)D + \left(\frac{L_{m2}}{L_{k2}+2L_{m2}} \cdot \frac{-V_C}{n} - V_o + \frac{V_C}{n}\right)(1 - D) = 0 \tag{6.19}$$

Substitute (6.18) to (6.19), the voltage gain can be expressed as

$$\frac{V_o}{V_{in}} = \frac{(1-D)D}{n+1-D} \tag{6.20}$$

Fig. 6.4 shows the curves of the voltage gain versus duty cycle with different transformer turns ratios. In order to effectively control the voltage, the regulating range of the duty cycle should be [0, D_{crit}] or [D_{crit}, 1], where

$$D_{crit} = n + 1 - \sqrt{(n+1)n}. \tag{6.21}$$

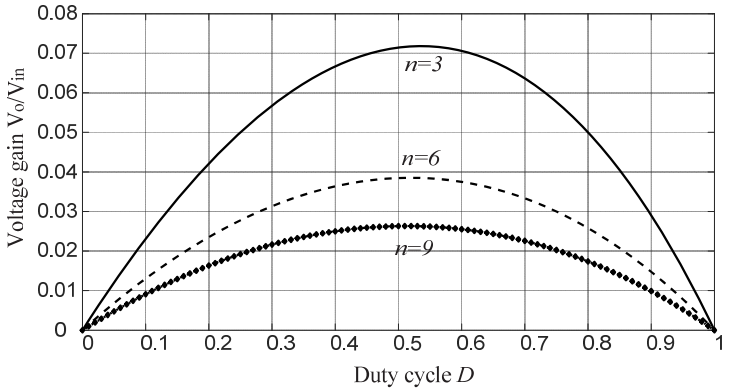


Fig. 6.4 Voltage gain versus duty cycle with different turns ratios

Fig. 6.5 shows the curve of D_{crit} versus transformer turns ratio n. It is clear that when n is high, D_{crit} is close to 0.5. Fig. 6.6 shows the voltage gain of the proposed converter compared with converters when $n = 6$,. It is shown that high step-down conversion ratio is achieved.

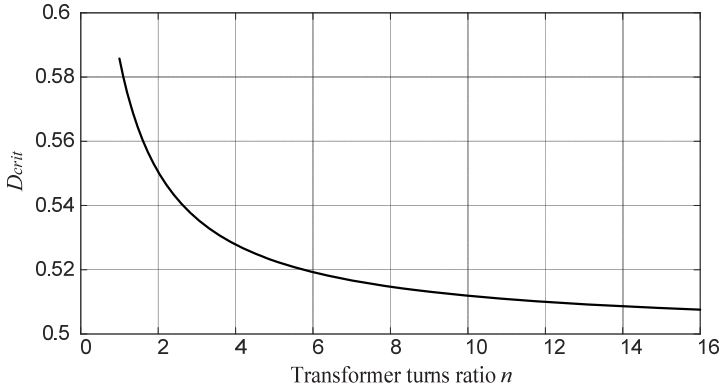


Fig. 6.5 D_{crit} versus transformer turns ratio

B. Influence of transformer leakage inductance

As can be seen from Fig. 6.3, when S_1 is turned off, the current in transformer leakage inductance L_{k1} goes through the capacitor C and the body diode of S_2 so that the leakage energy is stored in the capacitor C. When S_2 is turned off, the current in L_{k1} goes through

the body diode of S_1 so that the leakage energy is delivered to the input source. Therefore, the leakage energy can be recycled and no snubbers are required. As an added benefit, ZVS conditions are realized with the assistance of leakage inductance.

As shown in Fig. 6.2, during $[t_1 - t_3]$ and $[t_4 - t_0]$, the transformer leakage inductance limits the rising or decaying slope of i_p, making v_{m1} clamped at zero. Therefore, these two periods cause duty cycle loss. Duty cycle loss during $[t_1 - t_3]$ and $[t_4 - t_0]$ can be calculated, respectively, as

$$D_{L1} = \frac{t_3 - t_1}{T_s} = \frac{I_o L_{k1} f_s}{(n+1)V_C} \tag{6.22}$$

$$D_{L2} = \frac{t_0 - t_4}{T_s} = \frac{I_o L_{k1} f_s}{(n+1)(V_{in} - V_C)} \tag{6.23}$$

where I_o is the output current and f_s is switching frequency.

Considering the duty cycle losses caused by transformer leakage inductance, equation (6.17) and (6.19) can be modified, respectively, as

$$\frac{n}{n+1}(V_{in} - V_C)(D - D_{L2}) - V_C(1 - D - D_{L1}) = 0 \tag{6.24}$$

$$\left(\frac{L_{m2}}{L_{k2}+2L_{m2}} \cdot \frac{V_{in} - V_C}{n+1} - V_o\right)(D - D_{L2}) + \left(\frac{L_{m2}}{L_{k2}+2L_{m2}} \cdot \frac{-V_C}{n} - V_o + \frac{V_C}{n}\right)(1 - D - D_{L1}) -$$

$$V_o(D_{L1} + D_{L2}) = 0 \tag{6.25}$$

Solving (6.24) and (6.25), the output voltage is expressed as

$$V_o = \frac{(1-D)DV_{in}}{n+1-D} - \frac{I_o L_{k1} f_s}{(n+1-D)(n+1)} \tag{6.26}$$

As observed from (6.26), the presence of transformer leakage inductance lowers the output voltage. If L_{k1} is ignored, (6.26) will be equal to (6.20).

At the duty cycle loss intervals, the currents are freewheeling. No energy is delivered to the output. The freewheeling currents would cause conduction loss, which may degrade the efficiency.

C. Current ripple

According to the operation principle, the current ripples in the two windings of the coupled inductor can be calculated as

$$|\Delta i_{k21}| = \left|\frac{L_{m2}}{L_{k2}+2L_{m2}} - (1-D)\right| \cdot \frac{V_o}{L_{k2} f_s} \tag{6.27}$$

$$|\Delta i_{k22}| = \left|\frac{L_{k2}+L_{m2}}{L_{k2}+2L_{m2}} - (1-D)\right| \cdot \frac{V_o}{L_{k2} f_s} \tag{6.28}$$

Based on the coupled inductor theory, L_{k2} and L_{m2} can be expressed as

$$L_{k2} = (1-\alpha)L_s \tag{6.29}$$

$$L_{m2} = \alpha L_s \tag{6.30}$$

where α is coupling coefficient and L_s is self-inductance of the coupled inductor. Substitute (6.29) and (6.30) to (6.27) and (6.28), current ripples of the coupled inductor can be rewritten as

$$|\Delta i_{k21}| = \left|\frac{\alpha}{1+\alpha} - (1-D)\right| \cdot \frac{V_o}{L_{k2} f_s} \tag{6.31}$$

$$|\Delta i_{k22}| = \left|\frac{1}{1+\alpha} - (1-D)\right| \cdot \frac{V_o}{L_{k2} f_s} \tag{6.32}$$

Since α varies from 0 to 1, the current ripples have the following relationship

$$\begin{cases} |\Delta i_{k21}| > |\Delta i_{k22}|, & \text{when D} < 0.5 \\ |\Delta i_{k21}| < |\Delta i_{k22}|, & \text{when D} > 0.5 \end{cases} \tag{6.33}$$

Assuming the base value is $V_o/L_{k2}f_s$, the normalized maximum coupled inductor current ripple versus coupling coefficient under different duty cycles is shown in Fig. 6.7. When the coupling coefficient goes to zero (no coupling), the current ripples of the coupled inductor are the highest under a given inductance, which means highest switching losses and I^2R losses. As coupling coefficient increases, the inductor current ripples reduce, which helps improve the efficiency. When coupling coefficient approaches one (perfect coupling), maximum current ripple reduction can be achieved. On the other hand, it is also clear that the coupled inductor current ripples become smaller as duty cycle D converges to 0.5. Particularly, when $D = 0.5$ and $\alpha = 1$, ripple-free coupled inductor currents can be achieved.

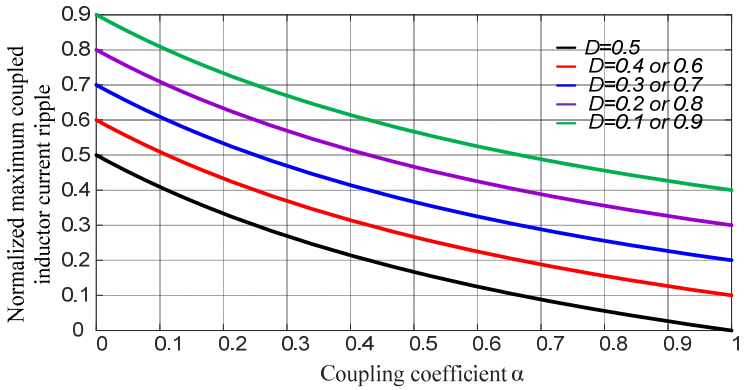


Fig. 6.7 Normalized maximum coupled inductor current ripple versus coupling coefficient under different duty cycles

The output current ripple can be calculated as

$$|\Delta i_o| = |\Delta i_{k21} + \Delta i_{k22}| = |2D - 1| \cdot \frac{V_o}{L_{k2}f_s} \qquad (6.34)$$

The normalized output current ripple versus duty cycle is shown in Fig. 6.8. The output current ripple is not related to coupling coefficient and it is reduced as duty cycle D converges to 0.5. Particularly, when $D = 0.5$, ripple-free output current can be achieved.

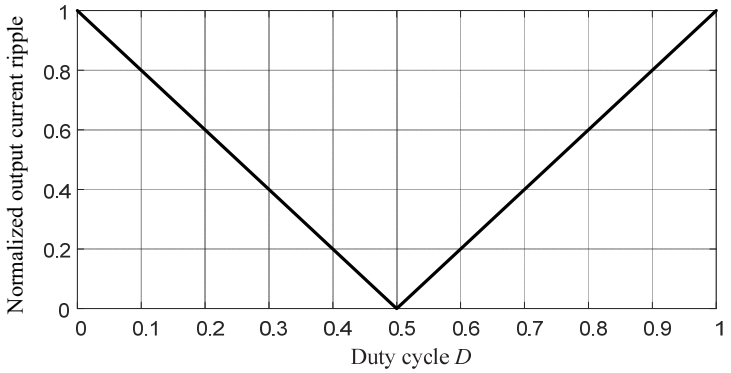


Fig. 6.8 Normalized output current ripple versus duty cycle

Table 6.1 Calculated and simulated current ripples with different α

α	Calculated			Simulated		
	$\lvert\Delta i_{k21}\rvert$	$\lvert\Delta i_{k22}\rvert$	$\lvert\Delta i_o\rvert$	$\lvert\Delta i_{k21}\rvert$	$\lvert\Delta i_{k22}\rvert$	$\lvert\Delta i_o\rvert$
0	1.66A	4.49A	2.83A	1.70A	4.48A	2.88A
0.25	0.43A	3.26A	2.83A	0.48A	3.27A	2.88A
0.47	0.31A	2.52A	2.83A	0.36A	2.53A	2.88A
0.75	0.98A	1.85A	2.83A	1.00A	1.88A	2.88A
1	1.415A	1.415A	2.83A	1.44A	1.44A	2.88A

In order to further illustrate the characteristics of the current ripples, calculated and simulated results (under V_{in}=48V, V_o=1V, L_{k2}=3.25uH, f_s=50kHz) with different coupling coefficient are provided in Table 6.1. The simulated current waveforms are given in Fig. 6.9. As can be seen, when there is no coupling ($\alpha = 0$), the inductor current ripples have an interleaved feature, thus the output current ripple is reduced due to the proposed structure. When the coupling coefficient increases, the output current ripple stays constant, however, the maximum inductor current ripple decreases. Therefore, the employment of

the coupled inductor helps reduce the inductor current ripple. As shown in Table 6.1, the simulated results are consistent with the analysis. The slight discrepancy is caused by the dead time and duty cycle loss.

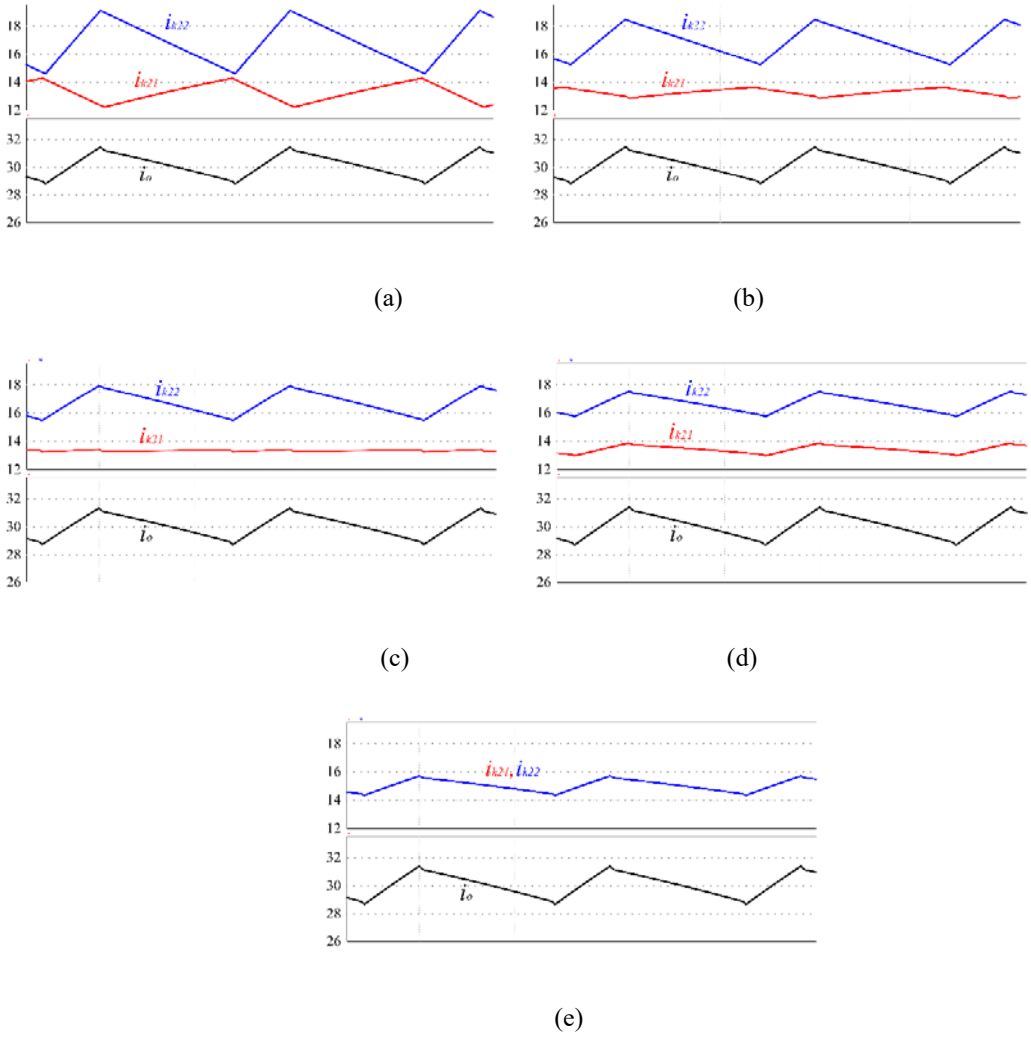


Fig. 6.9 Simulated current ripples: (a) α=0; (b) α=0.25; (c) α=0.47; (d) α=0.75; (e) α=1.

D. ZVS conditions

S3 and S4 are synchronous rectifiers, thus ZVS of S3 and S4 are always achieved. When analyzing ZVS conditions of S1 and S2, the output capacitance C_{oss} of the switches

are considered. In order to realize ZVS, the energy stored in the leakage inductance has to be large enough to fully charge/discharge the output capacitance of the switches. Therefore, the ZVS condition for S2 is given as

$$L_{k1}[i_p(t_1)]^2 > 2C_{oss} \cdot (\frac{nD}{n+1-D} V_{in})^2 \qquad (6.35)$$

where $i_p(t_1) = \frac{1-D}{n+1-D} i_o$.

The ZVS condition for S1 is given as

$$L_{k1}[i_p(t_4)]^2 > 2C_{oss} \cdot (\frac{(n+1)(1-D)}{n+1-D} V_{in})^2 \qquad (6.36)$$

where $i_p(t_4) = \frac{D}{n+1-D} i_o$.

6.3 Design Considerations

In this section, design considerations of key components of the proposed converter will be discussed. As a design example, a 48V to 1V high step-down converter is to be considered. The rated load current is set to 30A.

A. Design of duty cycle and transformer turns ratio

In this design example, duty cycle is limited to [D_{crit}, 1] because the difference of RMS currents in the two SRs would be smaller. As can be seen in Fig. 6.7 and Fig. 6.8, when duty cycle is closer to 0.5, smaller current ripples are obtained. On the other hand, the lower the turns ratio, the smaller the leakage inductance and size of the transformer. Based on these considerations, *n*=9 and *D*=0.73 would be a preferred combination according to (6.20). Then D_{crit} is calculated as 0.51 according to (6.21). In practice,

considering the power loss and duty cycle loss, the real duty cycle would be smaller than 0.73 since $D \in [0.51, 1]$.

B. Coupled inductor design

In this design example, the peak-to-peak ripple of i_o is designed to be less than 10% of the rated output current at the nominal condition. According to (6.34), the leakage inductance of coupled inductor is calculated as

$$L_{k2} = \frac{|2D-1|V_o}{\Delta i_o f_s} > 3.06\text{uH}. \tag{6.37}$$

Finally, the value of L_{k2} is set to 3.2uH.

As shown in Fig. 6.7, the higher the coupling coefficient, the lower the inductor current ripple, which means lower losses and better efficiency. However, if the coupling coefficient is too high, the flux in the magnetic core would be large, resulting in large volume of the coupled inductor. Therefore, a compromising coupling coefficient is desired

The windings and core structure of the designed coupled inductor are shown in Fig. 6.10. The winding structure is symmetric. The coupling coefficient is determined by the lengths of air gaps in the outer and center legs. In this design example, the ferrite EE core used are OP-44721-G009 (with a 9 mil gap in the center leg) from Magnetics. The air gap in the outer legs is designed to 9.2 mil. The turn number of each winding is set to 4. The measured parameters of the built coupled inductor are $L_{k2} = 3.25uH$, $L_{m2} = 2.89uH$ and thus $\alpha = 0.47$.

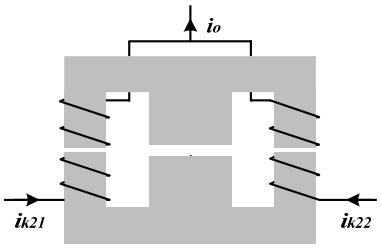


Fig. 6.10 Windings and core structure of the designed coupled inductor

C. Energy transfer capacitor design

The capacitor C is used to transfer energy from the input to the output. It is assumed in Section 6.1 that C is large enough so that the capacitor voltage is constant. However, if the capacitance is too large, the dynamic response will be slow. Therefore, it is recommended to choose the capacitance so that the voltage ripple on the energy transfer capacitor is below 10% of its nominal voltage. The voltage ripple on the capacitor is calculated as

$$\Delta V_c = \frac{1}{C}\int_0^{DT_s} i_p\, dt \approx \frac{I_o D}{2(n+1)Cf_s} \tag{6.38}$$

In this design example, according to (6.18), $V_c = 34V$. Then set $\Delta V_c < 3.4V$. According to (6.35), $C >$7.5uF. Finally, the energy transfer capacitor is selected as 10uF.

D. Switch selection

The blocking voltages across the switches can be evaluated as

$$V_{S1} = V_{S2} = V_{in} = 48V \tag{6.39}$$

$$V_{S3} = \frac{(1-D)V_{in}}{n+1-D} = 1.4V \tag{6.40}$$

$$V_{S4} = \frac{DV_{in}}{n+1-D} = 3.8V \tag{6.41}$$

Considering voltage overshoot and ringing, the voltage rating of the switches should be higher than the calculated values. Finally, MOSFET with 75V voltage rating is selected for S_1 and S_2. MOSFET with 25V voltage is selected for S_3 and S_4.

E. Transformer design

In the design example, the leakage inductance of the transformer is designed to guarantee ZVS operation from 40%-load to 100%-load. Then based on (6.35) and (6.36), the leakage inductance can be calculated as $L_{k1} > 6.1uH$. In order to minimize the secondary-winding conduction loss, a single-turn copper foil is used for the secondary winding. Then the primary winding is 9 turns. A pair of EE ferrite core 0R44022 from Magnetics is selected. The measured parameters of the built transformer are $L_{k1} = 6.5uH$ and $L_{m1} = 488uH$.

F. Output capacitor design

The minimum output capacitance depends on the current ripple Δi_o and the output voltage ripple Δv_o. Considering the output voltage ripple to be 0.8% of the output voltage, the output capacitance can be calculated as

$$C_o > \frac{\Delta i_o}{8\Delta v_o f_s} = \frac{10\%\times 30}{8\times 0.8\%\times 1\times 50k} = 937uF \qquad (6.42)$$

Finally, two 560uF OSCON capacitors are connected in parallel for the output capacitor.

G. Control scheme

The control scheme of the proposed converter is shown in Fig. 6.11. A digital-signal-processor (DSP) TMS320F28335 is adopted to implement the close-loop control. In the control scheme, a conventional PI controller is used to regulate the output voltage, a limiter

is used to limit the variation range of the duty cycle. In this design example, since the duty cycle is limited to [0.51, 1], a negative unity is needed in order to configure a negative feedback loop.

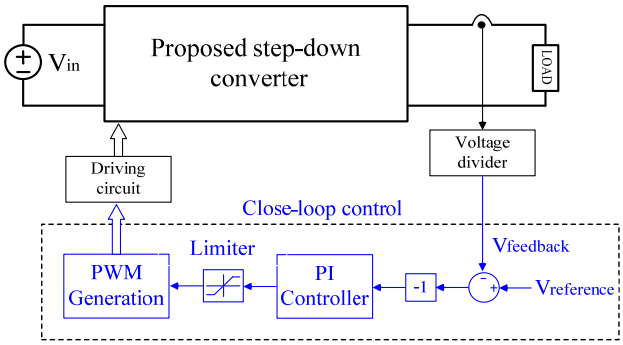


Fig. 6.11 The control scheme of the proposed converter

6.4 Experimental Results

A 48V/1V 30A prototype was built to verify the performance of the proposed converter. The switching frequency is 50kHz. The key parameters of the prototype are listed as in Table 6.2.

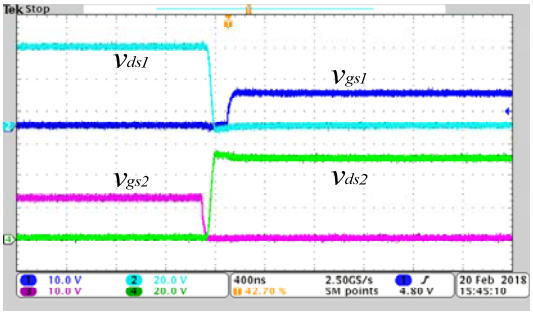
Table 6.2 Key parameters of the prototype

Components	Parameters
Input side switches S_1, S_2	IRFS3207ZTRRPBF
SRs S_3, S_4	Three PSMN1R2-25YLD in parallel
Transformer	turns ratio=9:1 Magnetizing inductance=488uH Leakage inductance=6.5uH
Coupled inductor	turns ratio=1:1 Magnetizing inductance=2.89uH Leakage inductance=3.25uH Coupling coefficient=0.47
Energy transfer capacitor	63VDC 10uF Film Capacitor
Output capacitor	Two 6.3V 560uF OSCON Capacitor

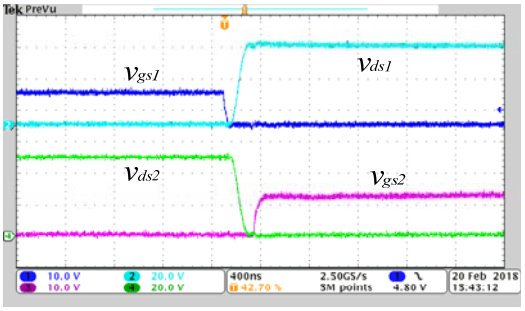
Fig. 6.12 (a)-(d) show the gate signals and the drain-to-source voltages for all the four switches at full load. It is clear that ZVS of all switches are achieved. It is also observed that the drain-to-source voltages of S_1 and S_2 are clamped at 48V, equal to the input voltage. The drain-to-source voltages of S_3 and S_4 are less than 4V, thus MOSFETs with low voltage rating and low on-resistance can be used. As the output capacitance of low-voltage-rating SRs resonates with the transformer leakage inductance, voltage rings exist on the waveforms of v_{ds3} and v_{ds4}.

Fig. 6.12 (e)-(f) shows the output current i_o and coupled inductor currents i_{k21} and i_{k22}. Due to the effect of the coupled inductor, the inductor current ripples are even smaller than the output current ripple. Fig. 6.12 (g) shows load transient response due to step load increase from 45% load to 100% load, and Fig. 6.12 (h) shows load transient response due to step load decrease from 100% load to 45% load.

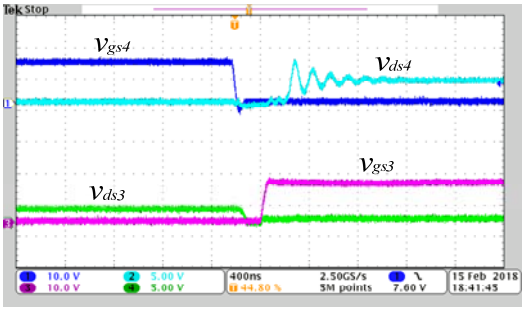
If the input of the converter is unregulated, different voltage levels can be imposed on the converter. Considering a variation percentage of 12.5%, the input voltage varies from 42V to 54V. The efficiency of the prototype versus output current under different input voltages was measured and shown Fig. 6.12 (i). As can be seen, at the nominal input voltage 48V, the peak efficiency is 94.7%, the efficiency at full load is 93.1%. When the input voltage is 42V, the efficiency is higher, with a peak efficiency of 95.1%. This is because the duty cycle becomes smaller, resulting in smaller current ripple and lower turn-off losses. When the input voltage is 54V, the efficiency is lower, with a peak efficiency of 94.2%. This is because the duty cycle becomes larger, resulting in higher current ripple and higher turn-off losses.


Tek Stop
v_{ds1}
v_{gs1}
v_{gs2}
v_{ds2}

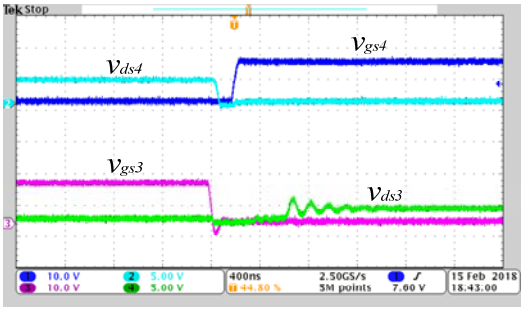
(a)


Tek PreVu
v_{gs1}
v_{ds1}
v_{ds2}
v_{gs2}

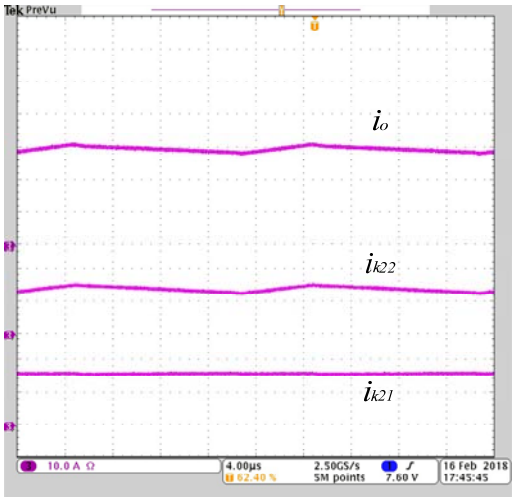
(b)


Tek Stop
v_{gs4}
v_{ds4}
v_{gs3}
v_{ds3}

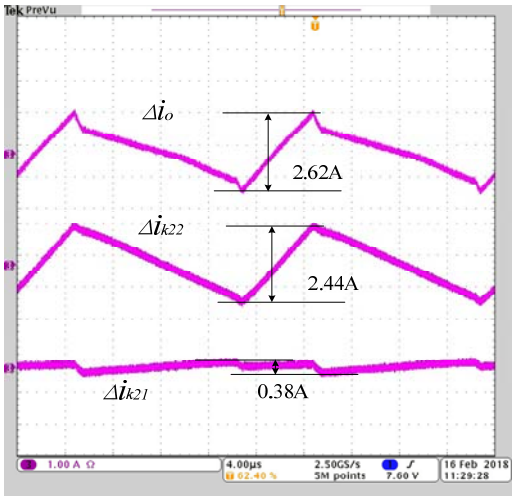
(d)


Tek Stop
v_{ds4}
v_{gs4}
v_{gs3}
v_{ds3}

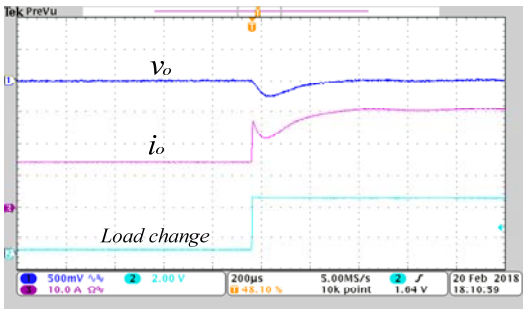
(c)


Tek PreVu
i_o
i_{k22}
i_{k21}

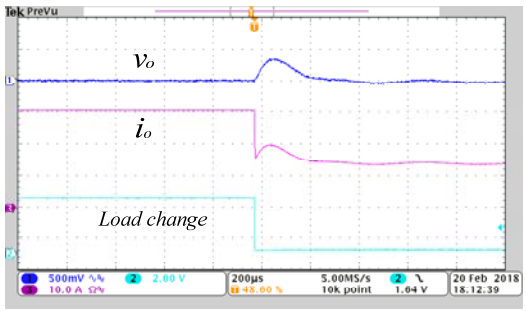
(f)


Tek PreVu
Δi_o
2.62A
Δi_{k22}
2.44A
Δi_{k21}
0.38A

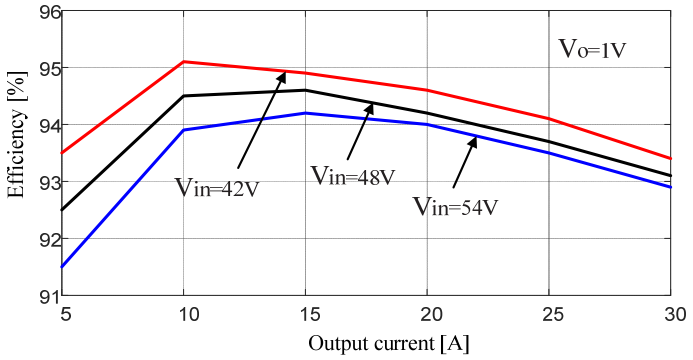
(e)


Tek PreVu
v_o
i_o
Load change

(g)


Tek PreVu
v_o
i_o
Load change

(h)



(i)

Fig. 6.12 Experimental results: (a) Gate signals and drain-to-source voltages at the rising edge of v_{gs1}; (b) Gate signals and drain-to-source voltages at the rising edge of v_{gs2}; (c) Gate signals and drain-to-source voltages at the rising edge of v_{gs3}; (d) Gate signals and drain-to-source voltages at the rising edge of v_{gs4}; (e) Output current i_o and coupled inductor currents i_{k21}, i_{k22} (dc coupling measurement); (f) Output current i_o and coupled inductor currents i_{k21}, i_{k22} (ac coupling measurement); (g) Load transients due to step load increase; (h) Load transients due to step load decrease; (i) Measured efficiency under different input voltages.

Chapter 7 Conclusion

Many applications call for non-isolated high step-up and high step-down DC-DC converters. This dissertation investigates new high step-up and high step-down topologies for various applications, aiming to achieve high efficiency, high power density, high step-up/step-down voltage gain, low cost and improved performance.

A new family of interleaved high step-up converters integrating coupled-inductor and switched-capacitor has been introduced for high current and ultra-high step-up applications in Chapter 2. A typical topology is re-shown in Fig. 7.1. It achieves ultra-high voltage gain, low switch voltage stress, balanced input current sharing, low input current ripple, high input current handling capability, alleviated diode reverse recovery, recycled leakage energy and common ground connection between the input and the output. Topology extensions and variations have also been discussed.

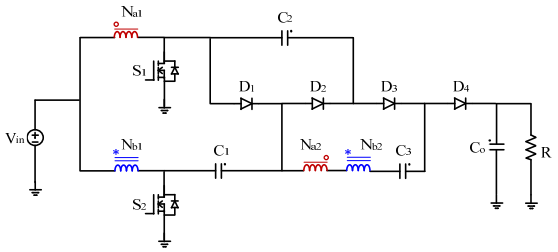


Fig. 7.1 Interleaved high step-up converter integrating coupled-inductor and switched-capacitor

In Chapter 3, multiphase interleaved high step-up converters with diode-capacitor VM stages has been presented, which is an extension of the previously reported two-phase current-fed Cockcroft–Walton multiplier. The multiphase configuration is re-shown in Fig.

7.2. It features high input current handling capability, high voltage gain, low component voltage stress, low input current ripple and automatic phase current balancing.

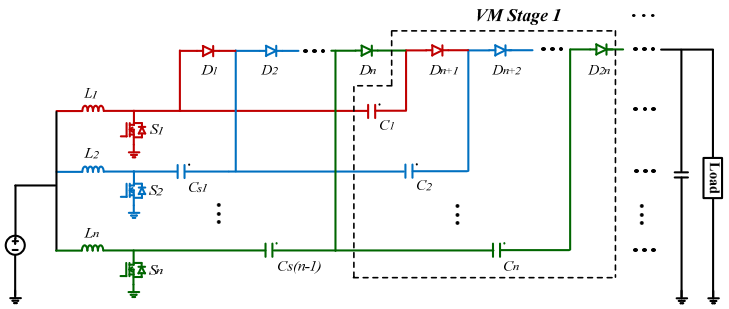


Fig. 7.2 Multiphase interleaved high step-up converter with VM stages.

These two types of interleaved high step-up converters are more suitable for high current applications. Compared to their counterparts, they achieve higher voltage gain and lower switch voltage stress with low component count. Comparison of the features of these two converters is provided in Table 7.1. Which type of converter to choose depends on the specific application requirements, such as the voltage gain, current level, the expected size and cost.

Table 7.1 Comparison of the two new interleaved high step-up converters

Fig. 7.1	Fig. 7.2
• Two-phase	• Multiphase
• Ultra-high voltage gain	• High voltage gain
• Relatively low component count	• High component count especially at very high voltage gain
• Alleviated diode reverse recovery	• Diode reverse recovery problem
• High diode voltage stress	• Low diode voltage stress
• Relatively complicated design	• Flexible structure and simple design

In Chapter 4, a single-phase coupled-inductor boost converter has been introduced for low input current applications. The topology is re-shown in Fig. 7.3 (a). The proposed converter achieves high voltage gain with the aid of the coupled inductor. Also, it features low component count, continuous input current and alleviated diode reverse recovery.

Based on the single-phase coupled-inductor boost converter, an improved converter has been introduced in Chapter 5. The topology is re-shown in Fig. 7.3 (b). It retains continuous input current and achieves higher voltage gain and lower semiconductor voltage stress. Furthermore, it achieves zero-voltage switching and zero DC magnetizing current.

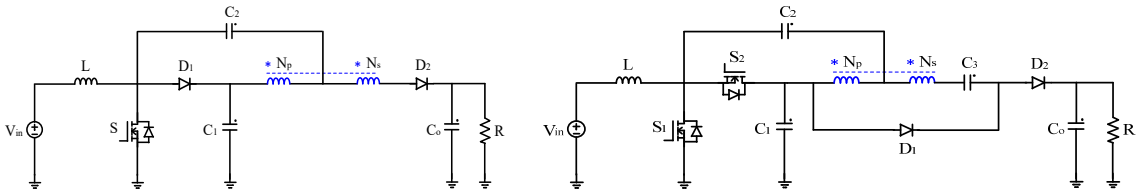


Fig. 7.3 Single-phase coupled-inductor boost converter: (a) basic converter; (b) improved converter.

The two new single-phase high step-up converters are more suitable for low current applications. Comparison of the features of the two converters is provided in Table 7.2.

Table 7.2 Comparison of the two new single-phase high step-up converters

Fig. 7.3(a)	Fig. 7.3(b)
• Continuous input current	• Continuous input current
• High voltage gain	• Higher voltage gain
• Low switch and diode voltage stress	• Lower switch and diode voltage stress
• Hard switching	• Zero voltage switching
• DC energy stored in coupled inductor	• No DC energy stored in coupled inductor
• Low component count	• Relatively high component count

In Chapter 5, a high step-down converter with zero voltage switching and low current ripples was presented. The topology is re-shown in Fig. 7.4. High step-down voltage conversion is achieved with the aid of energy transfer capacitor and built-in transformer. Also, the employment of interleaved structure and coupled inductor results in small current ripples. Furthermore, two main switches and two synchronous rectifiers are utilized and all can achieve zero-voltage switching. Only grounded gate drivers and boost strap drivers are needed, avoiding the use of complex isolated gate drivers. Finally, when one of the switches fails, the high input voltage is blocked from the output to keep the load safe.

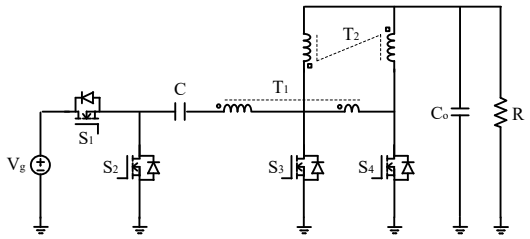


Fig. 7.4 High step-down converter with ZVS and low current ripples

The system design optimization of the proposed converters could be one of the future work. How to optimize the inductances and capacitances to achieve high efficiency, small size and light weight could be important for commercial applications. The modeling method of the high step-up/high step-down converters is another direction of the future work. Since high step-up/high step-down converters adopt more magnetics and capacitors for high voltage gain, a large number of state variables and state equations are involved in the modeling, leading to increased complexity. How to reduce the order of the modeling could also be an interesting topic.

REFERENCES

[1] F. Blaabjerg, Zhe Chen and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," in IEEE Transactions on Power Electronics, vol. 19, no. 5, pp. 1184-1194, Sept. 2004.

[2] W. Li and X. He, "Review of Nonisolated High-Step-Up DC/DC Converters in Photovoltaic Grid-Connected Applications," in IEEE Transactions on Industrial Electronics, vol. 58, no. 4, pp. 1239-1250, April 2011.

[3] W. Chen, A. Q. Huang, C. Li, G. Wang and W. Gu, "Analysis and Comparison of Medium Voltage High Power DC/DC Converters for Offshore Wind Energy Systems," in IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 2014-2023, April 2013.

[4] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli and R. Gules, "Voltage Multiplier Cells Applied to Non-Isolated DC–DC Converters," in IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 871-887, March 2008.

[5] L. Huber and M. M. Jovanovic, "A design approach for server power supplies for networking applications," APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition, New Orleans, LA, USA, 2000, pp. 1163-1169 vol.2.

[6] Q. Zhao and F. C. Lee, "High-efficiency, high step-up DC-DC converters," in IEEE Transactions on Power Electronics, vol. 18, no. 1, pp. 65-73, Jan 2003.

[7] Shehabi A, Smith S, Sartor D, Brown R, Herrlin M, Koomey J et al. United States Data Center Energy Usage Report. Lawrence Berkeley National Laboratory, Berkeley, California, 2016.

[8] A. Pratt, P. Kumar, T. V. Aldridge, “Evaluation of 400V DC distribution in telco and data centers to improve energy efficiency,” in 29th International Telecommunications Energy Conference, Sept. 30 2007-Oct. 4, 2007, pp. 32-39.

[9] A. Pratt, P. Kumar, K. Bross, T. Aldridge, “Powering compute platforms in high efficiency data centers,” IBM Technology Symposium, 2006.

[10] White paper, “48V: An Improved Power Delivery System for Data Centers”, 2017, available online:

http://www.wiwynn.com/usr_files/48V_An_Improved_Power_Delivery_System_for_Data_Centers_20170626_final.pdf

[11] F. C. Lee and Q. Li, "High-Frequency Integrated Point-of-Load Converters: Overview," in IEEE Transactions on Power Electronics, vol. 28, no. 9, pp. 4127-4136, Sept. 2013.

[12] L. Hu, X. Wei, Y. Luo and J. Ma, "Synchronous High Step-Down Ratio Non-Isolated LED Constant Current Driver Based on Improved Watkins-Johnson Topology," in IEEE Access, vol. 7, pp. 18345-18353, 2019.

[13] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg and B. Lehman, "Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques,

Topologies, and Applications," in IEEE Transactions on Power Electronics, vol. 32, no. 12, pp. 9143-9178, Dec. 2017.

[14] H. Liu, H. Hu, H. Wu, Y. Xing and I. Batarseh, "Overview of High-Step-Up Coupled-Inductor Boost Converters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 2, pp. 689-704, June 2016.

[15] W. Li, Y. Zhao, Y. Deng and X. He, "Interleaved Converter With Voltage Multiplier Cell for High Step-Up and High-Efficiency Conversion," in IEEE Transactions on Power Electronics, vol. 25, no. 9, pp. 2397-2408, Sept. 2010.

[16] G. A. L. Henn, R. N. A. L. Silva, P. P. Praça, L. H. S. C. Barreto and D. S. Oliveira, "Interleaved-Boost Converter With High Voltage Gain," in IEEE Transactions on Power Electronics, vol. 25, no. 11, pp. 2753-2761, Nov. 2010.

[17] K.-C. Tseng, C.-C. Huang, W.-Y. Shih, "A high step-up converter with a voltage multiplier module for a photovoltaic system", IEEE Trans. Power Electron., vol. 28, no. 6, pp. 3047-3057, Jun. 2013.

[18] K. C. Tseng and C. C. Huang, "High Step-Up High-Efficiency Interleaved Converter With Voltage Multiplier Module for Renewable Energy System," in IEEE Transactions on Industrial Electronics, vol. 61, no. 3, pp. 1311-1319, March 2014.

[19] X. Hu, G. Dai, L. Wang and C. Gong, "A Three-State Switching Boost Converter Mixed With Magnetic Coupling and Voltage Multiplier Techniques for High Gain Conversion," in IEEE Transactions on Power Electronics, vol. 31, no. 4, pp. 2991-3001, April 2016.

[20] X. Hu and C. Gong, "A High Gain Input-Parallel Output-Series DC/DC Converter With Dual Coupled Inductors," in IEEE Transactions on Power Electronics, vol. 30, no. 3, pp. 1306-1317, March 2015.

[21] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti and F. Blaabjerg, "High-Efficiency High Step-Up DC–DC Converter With Dual Coupled Inductors for Grid-Connected Photovoltaic Systems," in IEEE Transactions on Power Electronics, vol. 33, no. 7, pp. 5967-5982, July 2018.

[22] D. Wang, X. He and R. Zhao, "ZVT Interleaved Boost Converters with Built-In Voltage Doubler and Current Auto-Balance Characteristic," in IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 2847-2854, Nov. 2008.

[23] W. Li, X. Xiang, C. Li, W. Li and X. He, "Interleaved High Step-Up ZVT Converter With Built-In Transformer Voltage Doubler Cell for Distributed PV Generation System," in IEEE Transactions on Power Electronics, vol. 28, no. 1, pp. 300-313, Jan. 2013.

[24] W. Li, W. Li, X. Xiang, Y. Hu and X. He, "High Step-Up Interleaved Converter With Built-In Transformer Voltage Multiplier Cells for Sustainable Energy Applications," in IEEE Transactions on Power Electronics, vol. 29, no. 6, pp. 2829-2836, June 2014.

[25] K. Tseng, C. Cheng and C. Chen, "High Step-Up Interleaved Boost Converter for Distributed Generation Using Renewable and Alternative Power Sources," in IEEE

Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 2, pp. 713-722, June 2017.

[26] W. Li, X. He, "An interleaved winding-coupled boost converter with passive lossless clamp circuits", IEEE Trans. Power Electron., vol. 22, no. 4, pp. 1499-1507, Jul. 2007.

[27] W. Li, Y. Zhao, J. Wu and X. He, "Interleaved High Step-Up Converter With Winding-Cross-Coupled Inductors and Voltage Multiplier Cells," in IEEE Transactions on Power Electronics, vol. 27, no. 1, pp. 133-143, Jan. 2012.

[28] K. Tseng, J. Chen, J. Lin, C. Huang and T. Yen, "High Step-Up Interleaved Forward-Flyback Boost Converter With Three-Winding Coupled Inductors," in IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 4696-4703, Sept. 2015.

[29] L. He and Y. Liao, "An Advanced Current-Autobalance High Step-Up Converter With a Multicoupled Inductor and Voltage Multiplier for a Renewable Power Generation System," in IEEE Transactions on Power Electronics, vol. 31, no. 10, pp. 6992-7005, Oct. 2016.

[30] Y. Jang, M. M. Jovanovic, "Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end", IEEE Trans. Power Electron., vol. 22, no. 4, pp. 1394-1401, Jul. 2007.

[31] C. T. Pan, C. F. Chuang and C. C. Chu, "A Novel Transformer-less Adaptable Voltage Quadrupler DC Converter with Low Switch Voltage Stress," in IEEE Transactions on Power Electronics, vol. 29, no. 9, pp. 4787-4796, Sept. 2014.

[32] L. Müller and J. W. Kimball, "High Gain DC–DC Converter Based on the Cockcroft–Walton Multiplier," in IEEE Transactions on Power Electronics, vol. 31, no. 9, pp. 6405-6415, Sept. 2016.

[33] S. Lee, P. Kim, S. Choi, "High step-up soft-switched converters using voltage multiplier cells", IEEE Trans. Power Electron., vol. 28, no. 7, pp. 3379-3387, Jul. 2013.

[34] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga and M. Ferdowsi, "A DC–DC Converter With High Voltage Gain and Two Input Boost Stages," in IEEE Transactions on Power Electronics, vol. 31, no. 6, pp. 4206-4215, June 2016.

[35] B. P. Baddipadiga and M. Ferdowsi, "A High-Voltage-Gain DC–DC Converter Based on Modified Dickson Charge Pump Voltage Multiplier," in IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7707-7715, Oct. 2017.

[36] J. Chen, D. Sha, Y. Yan, B. Liu and X. Liao, "Cascaded High Voltage Conversion Ratio Bidirectional Nonisolated DC–DC Converter With Variable Switching Frequency," in IEEE Transactions on Power Electronics, vol. 33, no. 2, pp. 1399-1409, Feb. 2018.

[37] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, R. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters", IEEE Trans. Power Electron., vol. 23, no. 2, pp. 871-887, Mar. 2008.

[38] F. L. Tofoli, D. de Souza Oliveira, Jr., R. P. T. Bascope, and Y. J. A. Alcazar, “Novel nonisolated high-voltage gain dc-dc converters based on 3SSC and VMC,” IEEE Trans. Power Electron., vol. 27, no. 9, pp. 3897–3907, Sep. 2012.

[39] J. Roy and R. Ayyanar, "Sensor-Less Current Sharing Over Wide Operating Range for Extended-Duty-Ratio Boost Converter," in IEEE Transactions on Power Electronics, vol. 32, no. 11, pp. 8763-8777, Nov. 2017.

[40] S. Park, Y. Park, S. Choi, W. Choi and K. B. Lee, "Soft-Switched Interleaved Boost Converters for High Step-Up and High-Power Applications," in IEEE Transactions on Power Electronics, vol. 26, no. 10, pp. 2906-2914, Oct. 2011.

[41] M. Maalandish, S. H. Hosseini, S. Ghasemzadeh, E. Babaei and T. Jalilzadeh, "A Novel Multi-Phase High Step-Up DC/DC Boost Converter with Lower Losses on Semiconductors," in IEEE Journal of Emerging and Selected Topics in Power Electronics. doi: 10.1109/JESTPE.2018.2830510

[42] R. D. Middlebrook, “Transformerless DC-to-DC converters with large conversion ratios,” IEEE Trans. Power Electron., vol. 3, no. 4, pp. 484–488, Oct. 1988.

[43] W. Bin, L. Shouxiang, L. Yao, and K. M. Smedley, “A new hybrid boosting converter for renewable energy applications,” IEEE Trans. Power Electron., vol. 31, no. 2, pp. 1203–1215, Feb. 2016.

[44] C. M. Young, M. H. Chen, T. A. Chang, C. C. Ko and K. K. Jen, "Cascade Cockcroft–Walton Voltage Multiplier Applied to Transformerless High Step-Up DC–DC Converter," in IEEE Transactions on Industrial Electronics, vol. 60, no. 2, pp. 523-537, Feb. 2013.

[45] B. Axelrod, G. Golan, Y. Berkovich, A. Shenkman, "Diode–capacitor voltage multipliers combined with boost-converters: Topologies and characteristics", IET Power Electron., vol. 5, no. 6, pp. 873-884, Jul. 2012.

[46] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, “A DC–DC multilevel boost converter,” IET Power Electron., vol. 3, no. 1, pp. 129–137, Jan. 2010.

[47] B. Axelrod, Y. Berkovich and A. Ioinovici, "Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC–DC PWM Converters," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 55, no. 2, pp. 687-696, March 2008.

[48] Y. Tang, T. Wang and D. Fu, "Multicell Switched-Inductor/Switched-Capacitor Combined Active-Network Converters," in IEEE Transactions on Power Electronics, vol. 30, no. 4, pp. 2063-2072, April 2015.

[49] Y. Jiao, F. L. Luo, M. Zhu, "Voltage-lift-type switched-inductor cells for enhancing DC-DC boost ability: principles and integrations in Luo converter", IET Power Electron., vol. 4, no. 1, pp. 131-142, 2011.

[50] H. Liu, F. Li, "A novel high step-up converter with a quasi active switched-inductor structure for renewable energy systems", IEEE Trans. Power Electron., vol. 31, no. 7, pp. 5030-5039, Jul. 2015.

[51] L. S. Yang, T. J. Liang, J. F. Chen, "Transformerless DC-DC converters with high step-up voltage gain", IEEE Trans. Ind. Electron., vol. 56, no. 8, pp. 3144-3152, Aug. 2009.

[52] Y. Tang, D. Fu, T. Wang, Z. Xu, "Hybrid switched-inductor converters for high step-up conversion", IEEE Trans. Ind. Electron., vol. 62, no. 3, pp. 1480-1490, Mar. 2015.

[53] E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, A. A. Fardoun, "A family of single-switch PWM converters with high step-up conversion ratio", IEEE Trans. Circuits Syst. I Reg. Papers, vol. 55, no. 4, pp. 1159-1171, May 2008.

[54] Y. Berkovich, B. Axelrod, A. Shenkman, "A novel diode-capacitor voltage multiplier for increasing the voltage of photovoltaic cells", Proc. IEEE 11th Workshop Control Model. Power Electron., pp. 1-5, 2008.

[55] R.D. Middlebrook, “A continuous model for the Tapped-inductor boost converter”, IEEE PESC, 1975.

[56] Qun Zhao and F. C. Lee, "High-efficiency, high step-up DC-DC converters," in IEEE Transactions on Power Electronics, vol. 18, no. 1, pp. 65-73, Jan 2003.

[57] T. F. Wu, Y. S. Lai, J. C. Hung, and Y. M. Chen, “Boost converter with coupled inductors and buck–boost type of active clamp,” IEEE Trans. Ind. Electron., vol. 55, no. 1, pp. 154–162, Jan. 2008.

[58] Rong-Jong Wai and Rou-Yong Duan, "High step-up converter with coupled-inductor," in IEEE Transactions on Power Electronics, vol. 20, no. 5, pp. 1025-1035, Sept. 2005.

[59] Y.-P. Hsieh, J.-F. Chen, T.-J. Liang, L.-S. Yang, "A novel high step-up DC–DC converter for a microgrid system", IEEE Trans. Power Electron., vol. 26, no. 4, pp. 1127-1136, Apr. 2011.

[60] A. Ajami, H. Ardi, A. Farakhor, "A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications", IEEE Trans. Power Electron., vol. 30, no. 8, pp. 4255-4263, Aug. 2015.

[61] Y. P. Siwakoti and F. Blaabjerg, "Single Switch Nonisolated Ultra-Step-Up DC–DC Converter With an Integrated Coupled Inductor for High Boost Applications," in IEEE Transactions on Power Electronics, vol. 32, no. 11, pp. 8544-8558, Nov. 2017.

[62] J. Ai and M. Lin, "Ultralarge Gain Step-Up Coupled-Inductor DC–DC Converter With an Asymmetric Voltage Multiplier Network for a Sustainable Energy System," in IEEE Transactions on Power Electronics, vol. 32, no. 9, pp. 6896-6903, Sept. 2017.

[63] G. Wu, X. Ruan and Z. Ye, "High Step-Up DC–DC Converter Based on Switched Capacitor and Coupled Inductor," in IEEE Transactions on Industrial Electronics, vol. 65, no. 7, pp. 5572-5579, July 2018.

[64] Y. Ye, K. W. E. Cheng and S. Chen, "A High Step-up PWM DC-DC Converter With Coupled-Inductor and Resonant Switched-Capacitor," in IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7739-7749, Oct. 2017.

[65] B. Gu, J. Dominic, J. S. Lai, Z. Zhao, C. Liu, "High boost ratio hybrid transformer dc–dc converter for photovoltaic module applications", IEEE Trans. Power Electron., vol. 28, no. 4, pp. 2048-2058, Apr. 2013.

[66] B. R. Lin and J. Y. Dong, "New zero-voltage switching DC-DC converter for renewable energy conversion systems," in IET Power Electronics, vol. 5, no. 4, pp. 393-400, April 2012.

[67] Y.-P. Hsieh, J.-F. Chen, T.-J. Liang, L.-S. Yang, "Novel high step-up DC–DC converter with coupled-inductor and switched-capacitor techniques for a sustainable energy system", IEEE Trans. Power Electron., vol. 26, no. 12, pp. 3481-3490, Dec. 2011.

[68] H. Liu, F. Li, J. Ai, "A novel high step-up dual switches converter with coupled inductor and voltage multiplier cell for a renewable energy system", IEEE Trans. Power Electron., vol. 31, no. 7, pp. 4974-4983, Jul. 2016.

[69] H. Seong, H. Kim, K. Park, G. Moon and M. Youn, "High Step-Up DC-DC Converters Using Zero-Voltage Switching Boost Integration Technique and Light-Load Frequency Modulation Control," in IEEE Transactions on Power Electronics, vol. 27, no. 3, pp. 1383-1400, March 2012.

[70] Y. Zhao, W. Li and X. He, "Single-Phase Improved Active Clamp Coupled-Inductor-Based Converter With Extended Voltage Doubler Cell," in IEEE Transactions on Power Electronics, vol. 27, no. 6, pp. 2869-2878, June 2012.

[71] B. Gu, J. Dominic, B. Chen, L. Zhang and J. Lai, "Hybrid Transformer ZVS/ZCS DC–DC Converter With Optimized Magnetics and Improved Power Devices Utilization for Photovoltaic Module Applications," in IEEE Transactions on Power Electronics, vol. 30, no. 4, pp. 2127-2136, April 2015.

[72] L. He, Z. Zheng and D. Guo, "High Step-Up DC–DC Converter With Active Soft-Switching and Voltage-Clamping for Renewable Energy Systems," in IEEE Transactions on Power Electronics, vol. 33, no. 11, pp. 9496-9505, Nov. 2018.

[73] S. Sathyan, H. M. Suryawanshi, B. Singh, C. Chakraborty, V. Verma and M. S. Ballal, "ZVS–ZCS High Voltage Gain Integrated Boost Converter for DC Microgrid," in IEEE Transactions on Industrial Electronics, vol. 63, no. 11, pp. 6898-6908, Nov. 2016.

[74] S. Sathyan, H. M. Suryawanshi, M. S. Ballal and A. B. Shitole, "Soft-Switching DC–DC Converter for Distributed Energy Sources With High Step-Up Voltage Capability," in IEEE Transactions on Industrial Electronics, vol. 62, no. 11, pp. 7039-7050, Nov. 2015.

[75] G. Spiazzi, D. Biadene, S. Marconi and A. Bevilacqua, "Nonisolated High-Step-up DC–DC Converter With Minimum Switch Voltage Stress," in IEEE Transactions on Power Electronics, vol. 34, no. 2, pp. 1470-1480, Feb. 2019.

[76] K. Uddin, A. D. Moore, A. Barai, and J. Marco, “The effects of high frequency current ripple on electric vehicle battery performance,” Appl.Energy, vol. 178, pp. 142–154, Sep. 2016.

[77] Heon-Hee Kim, Hee-Jun Lee, Soo-Chul Shin, Young-Sang Ko, Min-Ho Shin and Chung-Yuen Won, "Minimization of input current ripple in 2-level full-bridge converter for fuel cell power system," Proceedings of The 7th International Power Electronics and Motion Control Conference, Harbin, 2012, pp. 1910-1914.

[78] A. H. El Khateb, N. A. Rahim, J. Selvaraj and B. W. Williams, "DC-to-DC Converter With Low Input Current Ripple for Maximum Photovoltaic Power Extraction," in IEEE Transactions on Industrial Electronics, vol. 62, no. 4, pp. 2246-2256, April 2015.

[79] S. Kjaer, J. Pedersen, and F. Blaabjerg, “A review of single-phase gridconnected inverters for photovoltaic modules,” IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[80] H. Ma, J. Lai, Q. Feng, W. Yu, C. Zheng and Z. Zhao, "A Novel Valley-Fill SEPIC-Derived Power Supply Without Electrolytic Capacitor for LED Lighting Application," in IEEE Transactions on Power Electronics, vol. 27, no. 6, pp. 3057-3071, June 2012.

[81] K. B. Park, G. W. Moon, and M. J. Youn, “Non-isolated high step-up boost converter integrated with SEPIC converter,” IEEE Trans. Power Electron., vol. 25, no. 9, pp. 1791–1801, Sep. 2010.

[82] R. Gules, W. M. dos Santos, F. A. dos Reis, E. F. R. Romaneli and A. A. Badin, "A Modified SEPIC Converter With High Static Gain for Renewable Applications," in IEEE Transactions on Power Electronics, vol. 29, no. 11, pp. 5860-5871, Nov. 2014.

[83] H. Ardi, A. Ajami and M. Sabahi, "A Novel High Step-Up DC–DC Converter With Continuous Input Current Integrating Coupled Inductor for Renewable Energy Applications," in IEEE Transactions on Industrial Electronics, vol. 65, no. 2, pp. 1306-1315, Feb. 2018.

[84] H. Ardi and A. Ajami, "Study on a High Voltage Gain SEPIC-Based DC–DC Converter With Continuous Input Current for Sustainable Energy Applications," in IEEE Transactions on Power Electronics, vol. 33, no. 12, pp. 10403-10409, Dec. 2018.

[85] J. Yao, A. Abramovitz and K. M. Smedley, "Analysis and Design of Charge Pump-Assisted High Step-Up Tapped Inductor SEPIC Converter With an Inductorless, Regenerative Snubber," in IEEE Transactions on Power Electronics/, vol. 30, no. 10, pp. 5565-5580, Oct. 2015.

[86] S. Lee and H. Do, "Zero-Ripple Input-Current High-Step-Up Boost–SEPIC DC–DC Converter With Reduced Switch-Voltage Stress," in IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 6170-6177, Aug. 2017.

[87] K. B. Park, G. W. Moon and M. J. Youn, "High Step-up Boost Converter Integrated With a Transformer-Assisted Auxiliary Circuit Employing Quasi-Resonant Operation," in IEEE Transactions on Power Electronics, vol. 27, no. 4, pp. 1974-1984, April 2012.

[88] Y. Deng, Q. Rong, W. Li, Y. Zhao, J. Shi and X. He, "Single-Switch High Step-Up Converters With Built-In Transformer Voltage Multiplier Cell," in IEEE Transactions on Power Electronics, vol. 27, no. 8, pp. 3557-3567, Aug. 2012.

[89] H. Do, "A Soft-Switching DC/DC Converter With High Voltage Gain," in IEEE Transactions on Power Electronics, vol. 25, no. 5, pp. 1193-1200, May 2010.

[90] W. Li, W. Li, Y. Deng and X. He, "Single-Stage Single-Phase High-Step-Up ZVT Boost Converter for Fuel-Cell Microgrid System," in IEEE Transactions on Power Electronics, vol. 25, no. 12, pp. 3057-3065, Dec. 2010.

[91] S. M. Chen, T. J. Liang, L. S. Yang and J. F. Chen, "A Cascaded High Step-Up DC–DC Converter With Single Switch for Microsource Applications," in IEEE Transactions on Power Electronics, vol. 26, no. 4, pp. 1146-1153, April 2011

[92] X. Hu and C. Gong, "A High Voltage Gain DC–DC Converter Integrating Coupled-Inductor and Diode–Capacitor Techniques," in IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 789-800, Feb. 2014.

[93] P. Saadat and K. Abbaszadeh, "A Single-Switch High Step-Up DC–DC Converter Based on Quadratic Boost," in IEEE Transactions on Industrial Electronics, vol. 63, no. 12, pp. 7733-7742, Dec. 2016.

[94] S. W. Lee and H. L. Do, "High Step-Up Coupled-Inductor Cascade Boost DC–DC Converter With Lossless Passive Snubber," in IEEE Transactions on Industrial Electronics, vol. 65, no. 10, pp. 7753-7761, Oct. 2018.

[95] C. Fei, M. H. Ahmed, F. C. Lee and Q. Li, "Two-Stage 48 V-12 V/6 V-1.8 V Voltage Regulator Module With Dynamic Bus Voltage Control for Light-Load Efficiency Improvement," in IEEE Transactions on Power Electronics, vol. 32, no. 7, pp. 5628-5636, July 2017.

[96] M. H. Ahmed, C. Fei, F. C. Lee and Q. Li, "48-V Voltage Regulator Module With PCB Winding Matrix Transformer for Future Data Centers," in IEEE Transactions on Industrial Electronics, vol. 64, no. 12, pp. 9302-9310, Dec. 2017.

[97] J. Sun, “Investigation of Alternative Power Architectures for CPU Voltage Regulators,” Ph.D dissertation, Virginia Polytechnic Inst. State Univ., Blacksburg, VA, 2008.

[98] S. Xiong, S. Wong, S. Tan and C. K. Tse, "A Family of Exponential Step-Down Switched-Capacitor Converters and Their Applications in Two-Stage Converters," in IEEE Transactions on Power Electronics, vol. 29, no. 4, pp. 1870-1880, April 2014.

[99] Y. Jang and M. Jovanovic, “Non-isolated power conversion system having multiple switching power converters”, U. S. Patents US20060087295A1, Oct. 2004.

[100] J. Yungtaek, M.M. Jovanovic, and Y. Panov, “Multiphase buck converters with extended duty cycle,” in Proc. IEEE Applied Power Electron. Conf., 2006, pp. 38- 44.

[101] O. Kirshenboim and M. M. Peretz, "High-Efficiency Nonisolated Converter With Very High Step-Down Conversion Ratio," in IEEE Transactions on Power Electronics, vol. 32, no. 5, pp. 3683-3690, May 2017.

[102] K. K. Leong, G. Deboy, K. Krischan, and A. Muetze, “A single stage 54V to 1.8V multi-phase cascaded buck voltage regulator module,” Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC, vol. 2015–May, no. May, pp. 1966–1973, 2015.

[103]M. Esteki, B. Poorali, E. Adib and H. Farzanehfard, "Interleaved Buck Converter With Continuous Input Current, Extremely Low Output Current Ripple, Low Switching Losses, and Improved Step-Down Conversion Ratio," in IEEE Transactions on Industrial Electronics, vol. 62, no. 8, pp. 4769-4776, Aug. 2015.

[104]C. T. Pan, C. F. Chuang and C. C. Chu, "A Novel Transformerless Interleaved High Step-Down Conversion Ratio DC–DC Converter With Low Switch Voltage Stress," in IEEE Transactions on Industrial Electronics, vol. 61, no. 10, pp. 5290-5299, Oct. 2014.

[105]C. Chuang, C. Pan and H. Cheng, "A Novel Transformer-less Interleaved Four-Phase Step-Down DC Converter With Low Switch Voltage Stress and Automatic Uniform Current-Sharing Characteristics," in IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 406-417, Jan. 2016.

[106]Y. Panov and M. M. Jovanovic, "Design and performance evaluation of low-voltage/high-current DC/DC on-board modules," in IEEE Transactions on Power Electronics, vol. 16, no. 1, pp. 26-33, Jan 2001.

[107]Mao Ye, Peng Xu, Bo Yang and F. C. Lee, "Investigation of topology candidates for 48 V VRM," APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335), Dallas, TX, 2002, pp. 699-705 vol.2.

[108]M. Xu, Y. Ren, J. Zhou, and F. C. Lee, “1-MHz self-driven ZVS full bridge converter for 48-V power pod and dc/dc brick,” IEEE Trans. Power Electron., vol. 20, no. 5, pp. 997–1006, 2005.

[109]Jia Wei, Fred C. Lee, “Step-Down Buck Converter With Full Bridge Circuit,” U.S. Patent US6757184B2, Jun 29, 2004.

[110]K. Yao, Y. Ren, J. Wei, M. Xu and F. C. Lee, "A family of buck-type DC-DC converters with autotransformers," Applied Power Electronics Conference and Exposition, 2003.

[111]S. Ye, W. Eberle and Y. F. Liu, "A Novel Non-Isolated Full Bridge Topology for VRM Applications," in IEEE Transactions on Power Electronics, vol. 23, no. 1, pp. 427-437, Jan. 2008.

[112]Z. Zhang, W. Eberle, Y. F. Liu and P. C. Sen, "A Nonisolated ZVS Asymmetrical Buck Voltage Regulator Module With Direct Energy Transfer," in IEEE Transactions on Industrial Electronics, vol. 56, no. 8, pp. 3096-3105, Aug. 2009.

[113]M. Ahmed, C. Fei, F. C. Lee, Q, Li, “High-efficiency high-power-density 48/1V sigma converter voltage regulator module.” in Proc. Applied Power Electron. Conf. Expo., 2017.

[114]T. B. G. Vangalapudi and D. Kastha, "Quasi-Parallel Voltage Regulator Topology for Powering Laptop Processors," in IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7805-7815, Oct. 2017.

[115]Cuk, Slobodan, “Step-Down Converter Having A Resonant Inductor, A Resonant Capacitor And A Hybrid Transformer,” U.S. Patent US7915874 B1, Mar 29, 2011.

[116]Cuk, Slobodan, “Hybrid-switching Step-down Converter with a Hybrid Transformer,” U.S. Patent Application US20120249102A1, Oct 04, 2012.

[117]K. Yao, M. Ye, M. Xu and F. C. Lee, "Tapped-inductor buck converter for high-step-down DC-DC conversion," in IEEE Transactions on Power Electronics, vol. 20, no. 4, pp. 775-780, July 2005.

[118]K. Jin, M. Xu, F. C. Lee, "A switching-capacitor PWM dc-dc converter and its derivative", IEEE Trans. Power Electron., vol. 25, no. 1, pp. 24-32, Jan.-Feb. 2010.

[119]K. I. Hwu, W. Z. Jiang and Y. T. Yau, "Ultrahigh Step-Down Converter," in IEEE Transactions on Power Electronics, vol. 30, no. 6, pp. 3262-3274, June 2015.

[120]Y. T. Yau, W. Z. Jiang and K. I. Hwu, "Ultrahigh Step-Down Converter With Wide Input Voltage Range Based on Topology Exchange," in IEEE Transactions on Power Electronics, vol. 32, no. 7, pp. 5341-5364, July 2017.

[121]R. J. Wai and J. J. Liaw, "High-Efficiency Coupled-Inductor-Based Step-Down Converter," in IEEE Transactions on Power Electronics, vol. 31, no. 6, pp. 4265-4279, June 2016.

[122]H. L. Do, "Zero-Voltage-Switching Synchronous Buck Converter With a Coupled Inductor," in IEEE Transactions on Industrial Electronics, vol. 58, no. 8, pp. 3440-3447, Aug. 2011.

[123]L. Jiang, C. C. Mi, S. Li, C. Yin and J. Li, "An Improved Soft-Switching Buck Converter With Coupled Inductor," in IEEE Transactions on Power Electronics, vol. 28, no. 11, pp. 4885-4891, Nov. 2013.

[124]K. I. Hwu, W. Z. Jiang and Y. T. Yau, "Nonisolated Coupled-Inductor-Based High Step-Down Converter With Zero DC Magnetizing Inductance Current and Nonpulsating Output Current," in IEEE Transactions on Power Electronics, vol. 31, no. 6, pp. 4362-4377, June 2016.

[125]K. Yao, Y. Qiu, M. Xu and F. C. Lee, "A novel winding-coupled buck converter for high-frequency, high-step-down DC-DC conversion," in IEEE Transactions on Power Electronics, vol. 20, no. 5, pp. 1017-1024, Sept. 2005.

[126]F. Marvi, E. Adib and H. Farzanehfard, "Efficient ZVS Synchronous Buck Converter with Extended Duty Cycle and Low-Current Ripple," in IEEE Transactions on Industrial Electronics, vol. 63, no. 9, pp. 5403-5409, Sept. 2016.

[127]K. I. Hwu, W. Z. Jiang and P. Y. Wu, "An Expandable Two-Phase Interleaved Ultrahigh Step-Down Converter With Automatic Current Balance," in IEEE Transactions on Power Electronics, vol. 32, no. 12, pp. 9223-9237, Dec. 2017.

[128]Y. Zheng, K. Smedley, "Interleaved High Step-Up Converter Integrating Coupled Inductor and Switched Capacitor for Distribution Generation Systems," in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2018.2878409, accepted for publication.

[129] Y. Zheng, W. Xie, K. Smedley, "A Family of Interleaved High Step-Up Converters with Diode-Capacitor Technique," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2019.2907691, accepted for publication.

[130] Y. Zheng, K. Smedley, "Analysis and Design of a Single-Switch High Step-Up Coupled-Inductor Boost Converter," in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2019.2915348, accepted for publication.

[131] Y. Zheng, B. Brown, W. Xie, S. Li, K. Smedley, "High Step-Up DC-DC Converter with Zero Voltage Switching and Continuous Input Current," in IEEE Transactions on Power Electronics, in review.

[132] Y. Zheng, S. Li and K. M. Smedley, "Nonisolated High Step-Down Converter with ZVS and Low Current Ripples," in IEEE Transactions on Industrial Electronics, vol. 66, no. 2, pp. 1068-1079, Feb. 2019.