UNIVERSITY OF CALIFORNIA,
IRVINE

Ultra-Wideband Random Data Generators For mm-Wave Transmitters

THESIS

submitted in partial satisfaction of the requirements.
for the degree of

MASTER OF SCIENCE

in Electrical and Computer Engineering

by

Youssef Osama Hassan

Thesis Committee:
Professor Payam Heydari, Chair
Professor Ozdal Boyraz
Assistant Professor Hamidreza Aghasi

2023

DEDICATION

To

my parents and friends

in recognition of their worth

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ABSTRACT OF THE THESIS

Ultra-Wideband Random Data Generators For mm-Wave Transmitters

by

Youssef Osama Hassan

Master of Science in Electrical and Computer Engineering

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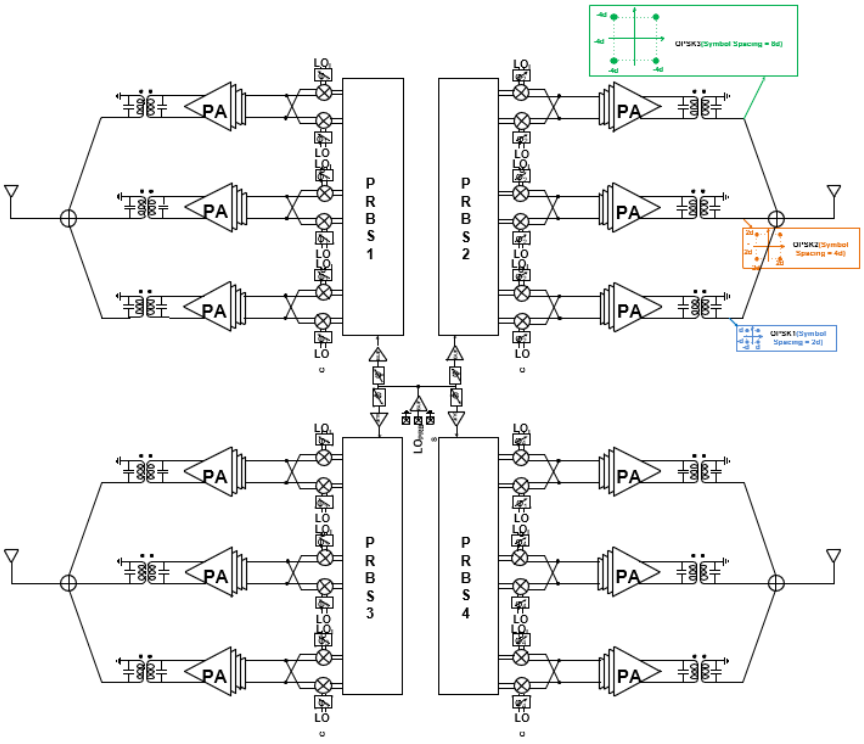
Professor Payam Heydari, Chair

This research presents a wide band pseudo random bit sequence generator (PRBS) that is used for data generation in mm-Wave transmitters, the goal was to design 6 separate loops with accurate time shift to generate the data input needed for the 3 QPSK transmitters combined together for the purpose of generating high order QAM signals from basin QPSK transmitters as in [1], the output of PRBS is then distributed and amplified to be sent to 4 array element each of them consists of 3 I/Q transmitters as mentioned for 64 QAM generation, the full circuit schematic for the PRBS loop, the amplification stages, the control unit and the array distribution network are presented, and also the full layout with post extraction results is presented at the end, the chip was fabricated in 45nm GFSOI technology with expected arrival date on July 2023.

INTRODUCTION

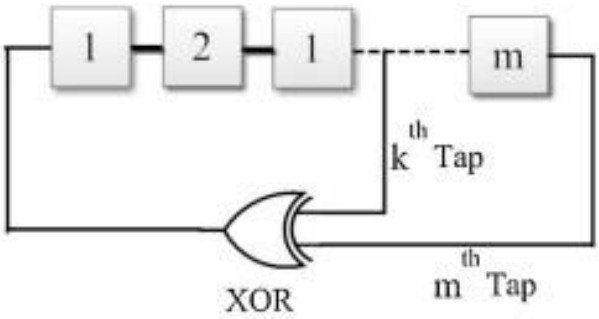
The swift advancements in wireless communication technology, specifically the transition from 4G to 5G and the impending arrival of 6G, have prompted a surge in demand for higher data rates and broader bandwidths. To cater to these needs, the focus has shifted towards millimeter-wave (mm-wave) bands, especially the frequency range of 30 GHz to 300 GHz, leading to the emergence of mm-wave transceivers [2]. These devices are integral in high-frequency communication systems, enabling both the transmission and reception of signals. A key component of these systems is the generation of test signals, a task where the Pseudo-Random Binary Sequence (PRBS) proves highly effective [3,4].

Figure 1 full TX diagram



A PRBS is a sequence of binary digits that appears statistically random, but is, in fact, generated by deterministic processes, often via a linear feedback shift register (LFSR) or other similar hardware structures [5,6]. These sequences are commonly characterized by their length, typically expressed as 2^n - 1, where n is the number of stages in the LFSR. PRBSs are widely used in communication systems for various purposes, such as channel estimation, synchronization, and system identification [7].

Figure 2 simple PRBS diagram



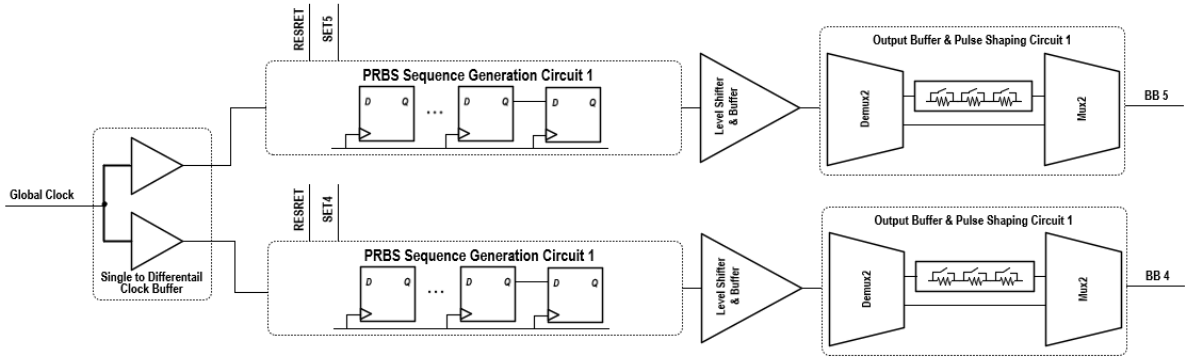
In mm-wave transceivers, PRBS signals can be used for a variety of purposes, including channel estimation, equalization, and bit error rate (BER) testing. For example, PRBS signals can be used to estimate the channel frequency response and to perform equalization to compensate for the distortion caused by the channel. In addition, PRBS signals can be used to measure the BER of the system, which is a critical performance metric that indicates the error rate in data transmission.

One of the key advantages of using PRBS signals in mm-wave transceivers is that they can provide a standardized method for evaluating system performance. This can be particularly

useful for system designers and manufacturers, as it allows them to compare the performance of different systems and to ensure that their systems meet the required performance specifications.

Pseudorandom binary sequences (PRBS) are not only useful for testing and evaluating communication systems, but they can also serve as data generators in mm-wave transceivers see Figure . In this context, PRBS signals can be used to generate a stream of digital data that can be transmitted over the mm-wave frequency range, providing a reliable and high-speed data transmission solution [8].

Figure 3 PRBS system implemented in this TX.



In mm-wave transceivers, PRBS signals can be used as a source of data for various applications, including high-speed wireless communication systems [9], radar systems [10], and imaging systems [11]. PRBS signals can be modulated onto a carrier frequency and

transmitted over the mm-wave frequency range, providing a high bandwidth and low latency data transmission solution.

Moreover, PRBS signals offer several advantages as data generators in mm-wave transceivers. One of the primary benefits is their ability to provide a wide range of data patterns that can simulate different types of data, such as audio, video, and other digital signals. Furthermore, PRBS signals are generated using a mathematical algorithm and do not require the storage of large amounts of data, which can be a significant advantage in applications where storage space is limited.

In addition, PRBS signals can be used to generate data with a low probability of repeating, which is particularly useful in applications where data redundancy can lead to errors or interference. The length of the PRBS sequence can be adjusted to achieve the desired level of randomness, and the autocorrelation properties of the signal can be carefully chosen to avoid interference with other signals.

However, there are also some limitations to the use of PRBS signals in mm-wave transceivers. For example, PRBS signals are not suitable for testing the effects of interference or noise, as they do not accurately reflect real-world data patterns. In addition, the use of PRBS signals can sometimes be computationally intensive and the analog circuits implementation may dissipate high power.

In conclusion, the use of PRBS signals as data generators in mm-wave transceivers provides a reliable and high-speed data transmission solution. PRBS signals offer several advantages, including the ability to provide a wide range of data patterns, generate data with low probability of repeating, and requiring less storage space. However, their limitations should also be taken into consideration when selecting the appropriate data generation technique for a given application, and for this research work we are focusing mainly on the use of PRBS as data generator for the mm-Wave transmitters testing and characterization, and the thesis is organized as follows, chapter I is an introduction, chapter II we start discussing the circuits implementation and results after schematic simulations, chapter III we show the full layout of the circuit along with post extraction simulation results and finally in chapter IV we have the conclusion.

Chapter 1. Proposed Wideband PRBS

In this chapter we focus on presenting the full circuit schematic for our PRBS system, the system is divided into 3 main sub systems which we will address independently next.

The first system is the PRBS loop, it consists of the PRBS generation, and amplification and this is the core of the design.

The second system is the control unit that is responsible for the generation of 6 start signals for the 6 different PRBS loops, and the reason why we want them to start from different time initials is that we are trying to decrease the correlation between the loops for more uniform QAM constellation at the output of the TX, ideally we would love to generate totally random signals but the PRBS output codes start repeating (they are periodic) and the length of the period depends on the length of the LFSR used, we choose to have 9 bits LFSR for our loop design and it was sufficient for low enough correlation between the output codes.

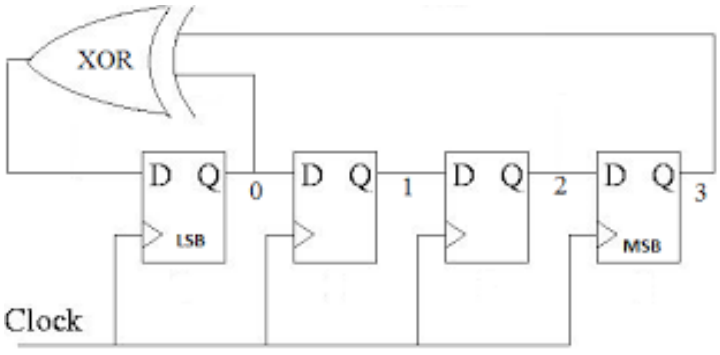
And finally, the PRBS output distribution network, and this network is responsible of sending the 6 PRBS outputs to the 24 total QPSK transmitters at exactly the same time and the layout had to minimize the Group Delay difference between the outputs, so we implemented layout techniques for that purpose, and we simulated the whole network on Sonnet EM simulator.

1.1. The main PRBS loop

A pseudorandom binary sequence (PRBS) is a sequence of bits that approximate the properties of random numbers. A PRBS appears random but, because it's generated by a deterministic system, it will repeat after a certain length.

PRBS is often generated using a linear feedback shift register (LFSR). An LFSR is a cascade of flip-flops, sharing the same clock, in which the output of one stage is the input of the next. The last output is fed back to the first input after being processed by a logic function. This function is usually XOR (exclusive OR), although other functions can be used. The feedback path in an LFSR is defined by a polynomial, referred to as the "feedback polynomial" or "generator polynomial". This polynomial also defines the sequence length, which is 2^n - 1, where n is the number of bits in the LFSR [12], and you can see in Figure 2 and example of 4-bit LFSR used as PRBS.

Figure 2 example of 4-bit PRBS



PRBS has several important properties that make it useful for various applications

[13]:

Balanced Sequence: In a complete cycle, the number of '1's is one more than the number of '0's. This property makes PRBS useful in communication systems where DC balance is important.

Autocorrelation: PRBS has a strong autocorrelation peak. This means that, when a PRBS is correlated with a time-shifted version of itself, the correlation is maximum when the time shift is zero and minimum otherwise. This property is exploited in synchronization and spread spectrum communication systems.

Power Spectrum: The power spectrum of a PRBS is flat, akin to white noise, making it an excellent tool for system testing across a wide range of frequencies.

And now we are going to share our schematic for the PRBS loop Figure 3 shows the top-level schematic of our PRBS system, the inputs are mainly a 20 Ghz clock for the control unit and for the DFFs in the LFSR, and the control signals for the control unit, current mirror and the RC networks inside the loop.

Another output for our system in addition to the PRBS signals is the clock needed to generate these signals, as it is also needed for the retiming block at the input of the mixer in the TX.

Figure 3 Top level schematic

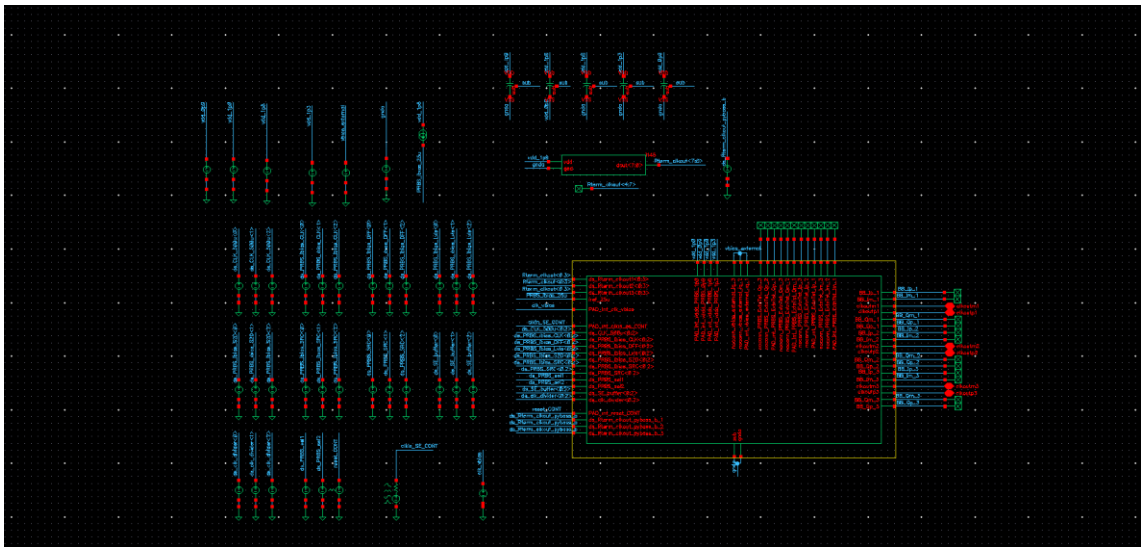
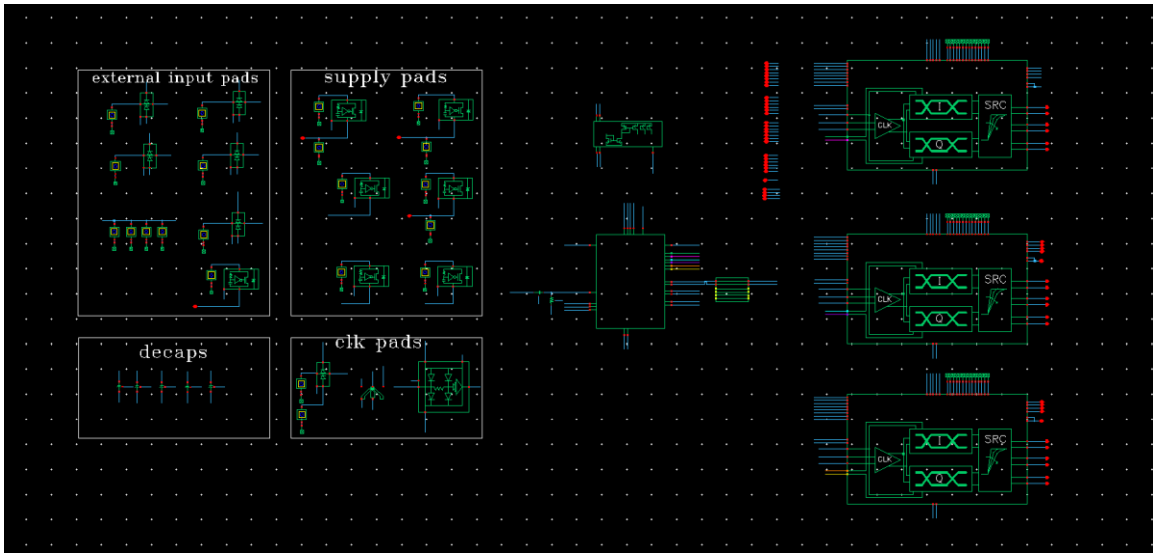


Figure 4, shows the full schematic of the PRBS system, we have on the left 3 I/Q PRBS loops every block responsible for generation and amplification of I/Q PRBS, in the middle we have the control unit along with the global programmable current mirrors, and finally we have the full PAD schematic required for the whole PRBS.

Figure 4 the full schematic for the PRBS system



In this sub-section we will focus on the main I/Q PRBS loop shown in Figure 5.

Figure 5 shows the top level of the loop including the programmable current mirrors and level shifters required for the control signals, it also has the triple clock buffer block required to strengthen the block to be able to drive the DFFs, the Buffers block is shown in Figure 6 with the detailed schematic in Figure 7.

Figure 5 The I/Q PRBS generation loop top.

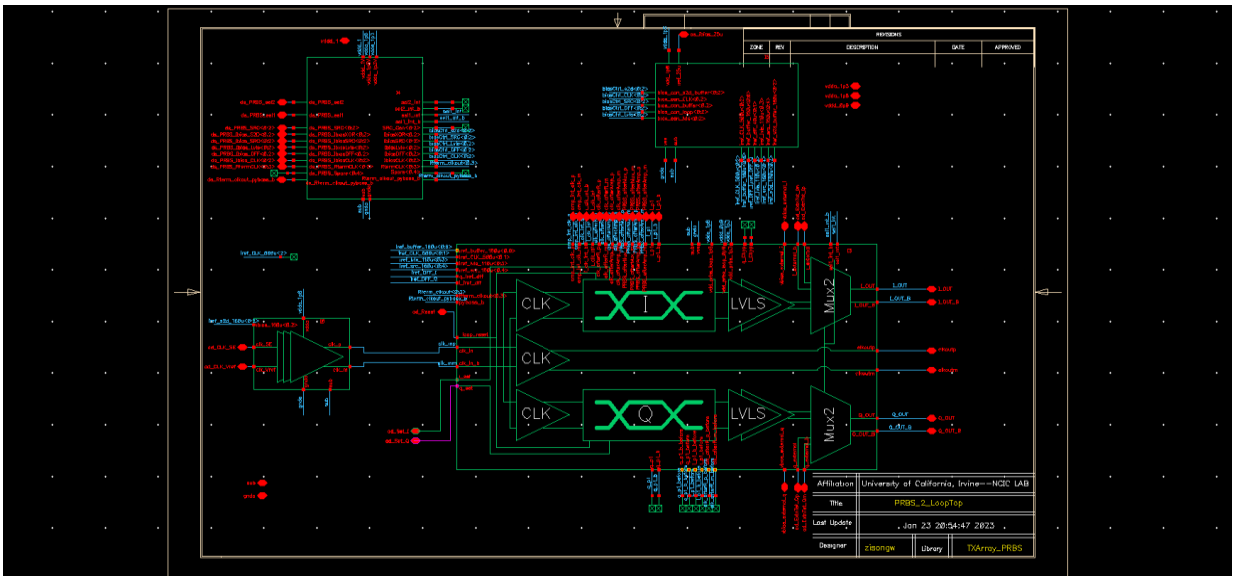


Figure 6 the clock buffers and amplifiers top

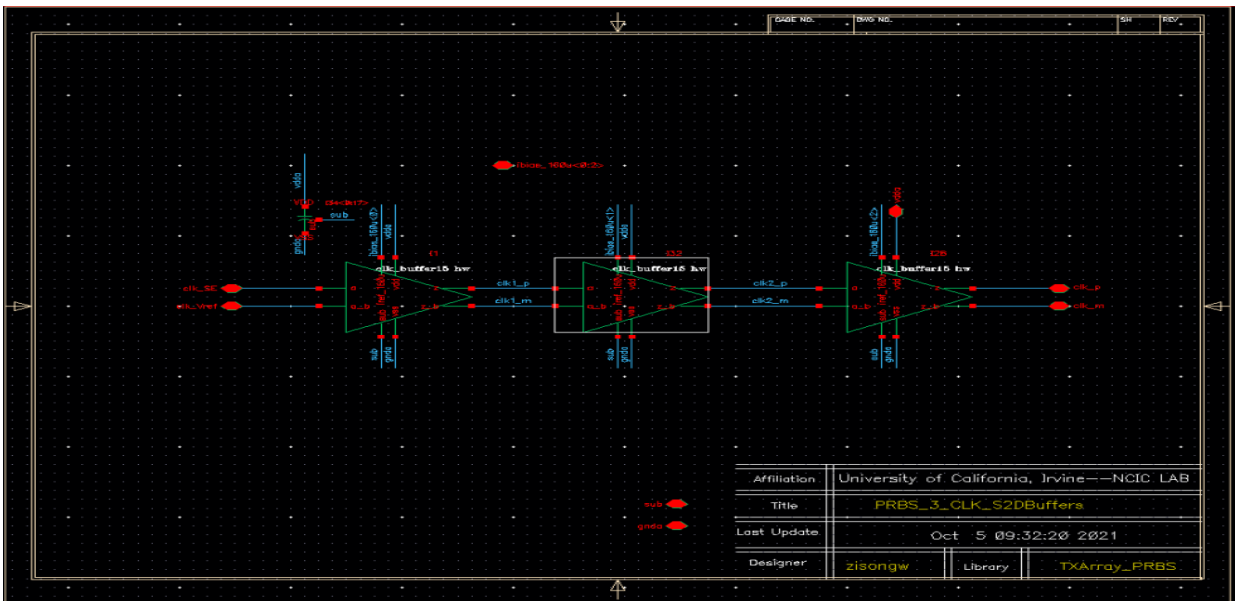
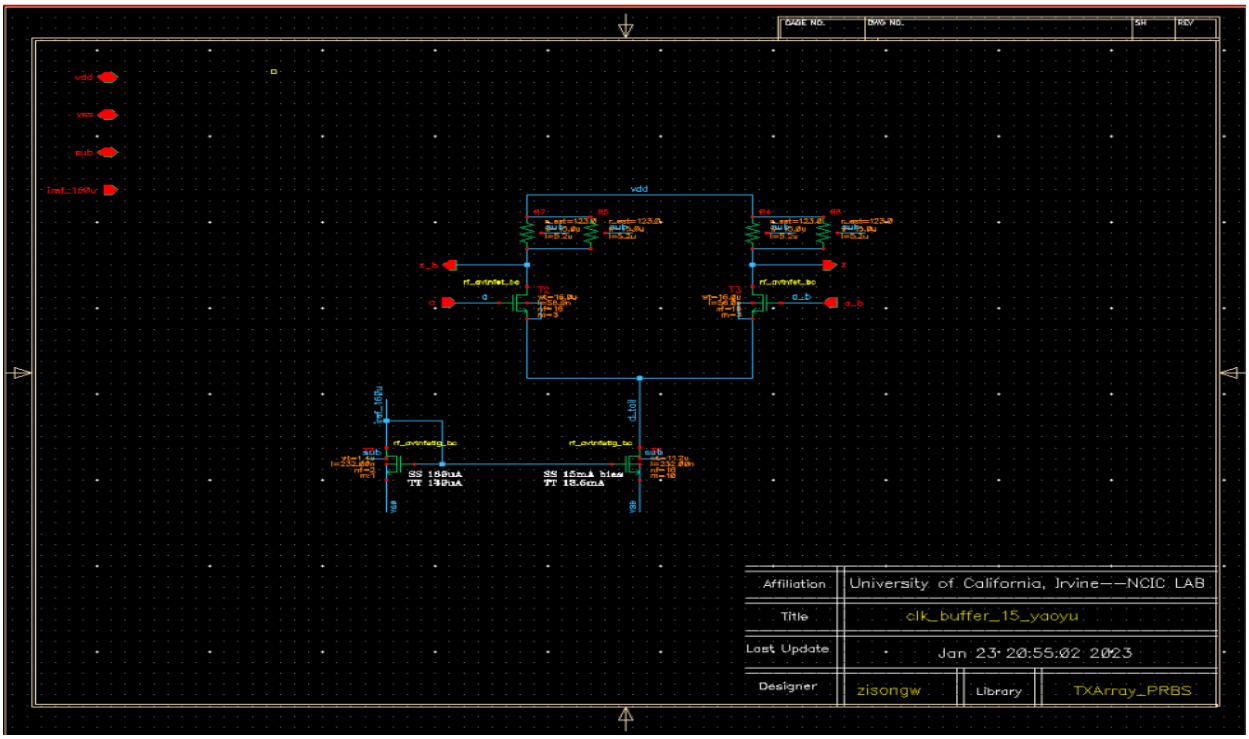
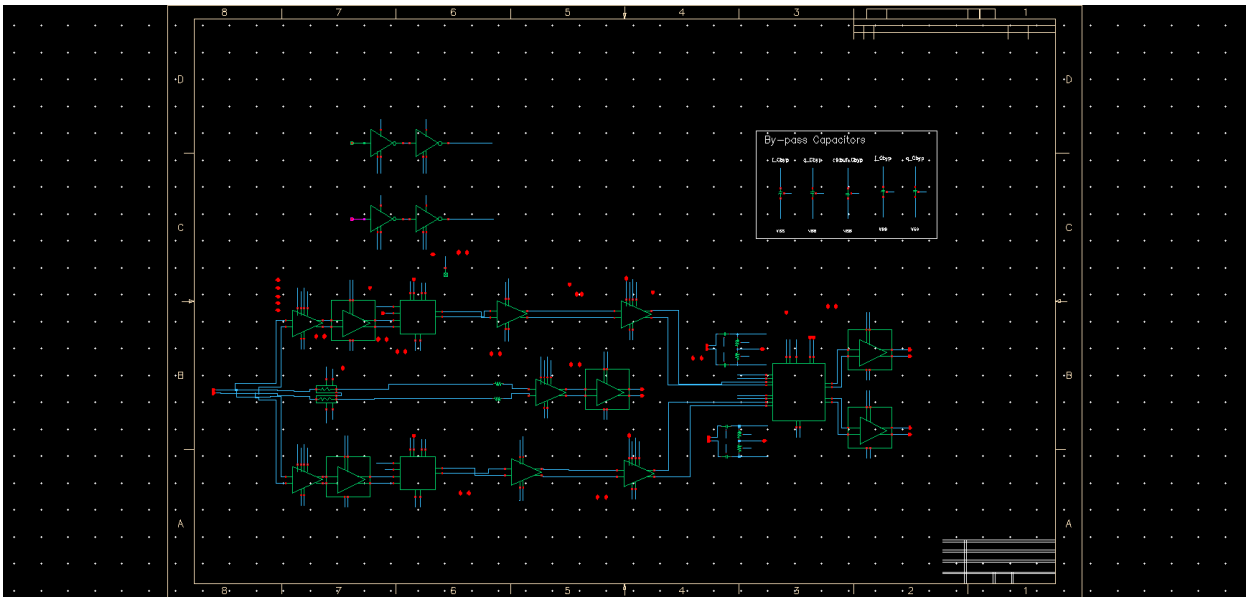


Figure 7 clock buffer schematic



And the I/Q PRBS amplification system is shown in Figure 8 where we can divide it into 3 main sub sections:

Figure 8 I/Q PRBS Loop



Section 1 Figure 9: it has the main LFSR that generates the random sequence and the initial amplifiers level shifters for the PRBS output.

And in Figure 10 we show the LFSR schematic with the CML based DFFs

Figure 9 section 1 in the I/Q PRBS loop

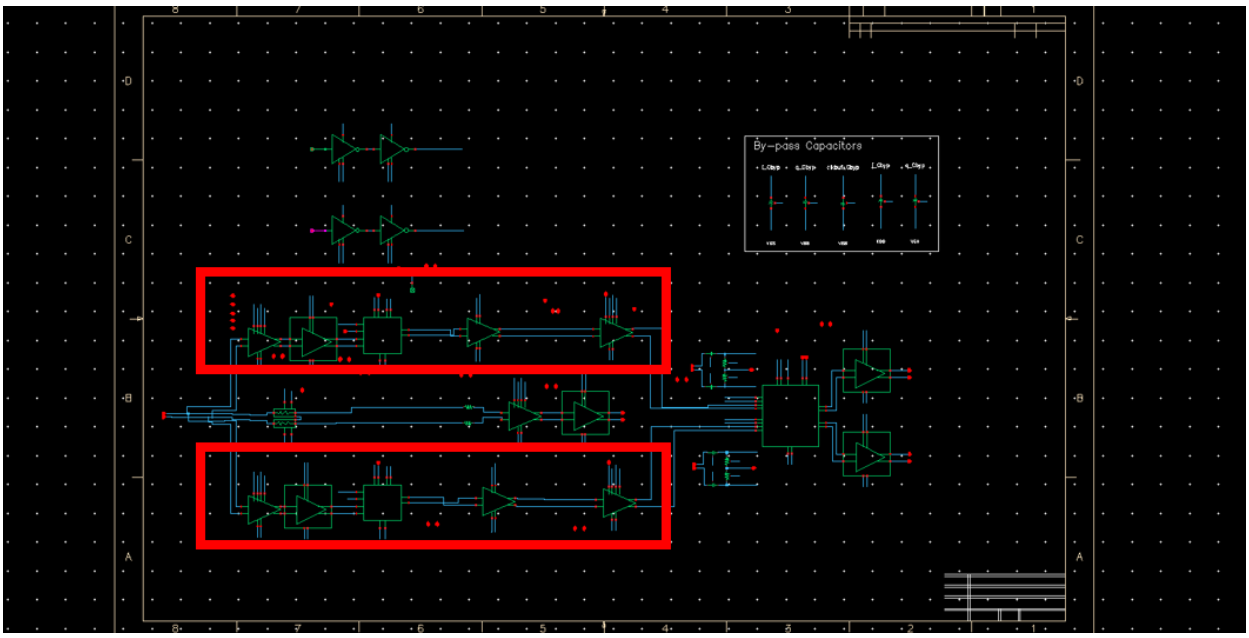
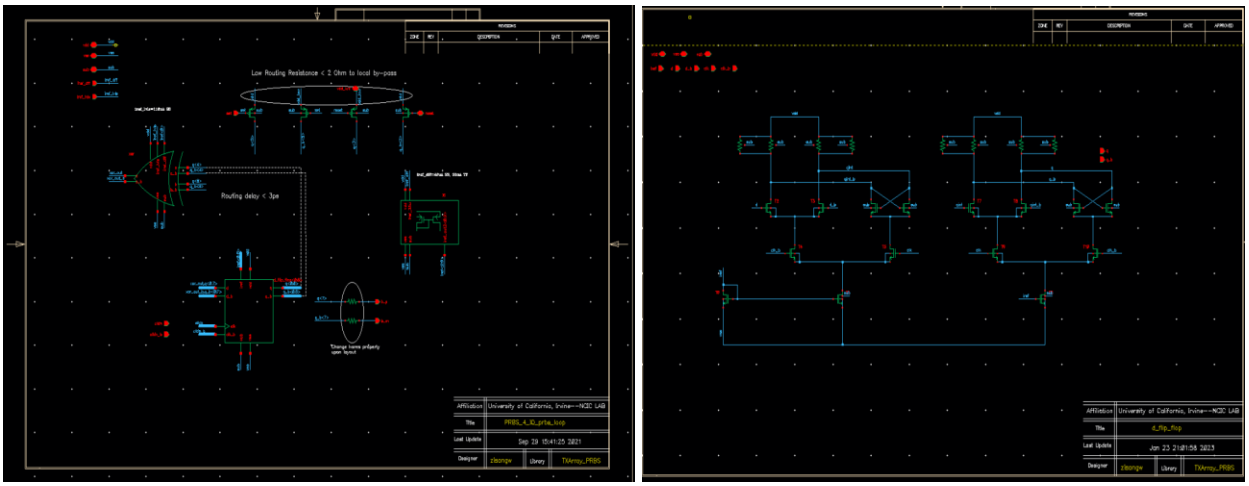


Figure 10 (a) the LFSR loop (b) the CML based DFF.



(a) (b)

Section 2 Figure 11: it has clock amplifiers and the RC delay control circuit we use to adjust the clock delay manually for accurate retiming of the PRBS output.

And in Figure 12 we show the Resistor control circuit and the buffers for the clock.

Figure 11 section 2 in the I/Q PRBS loop

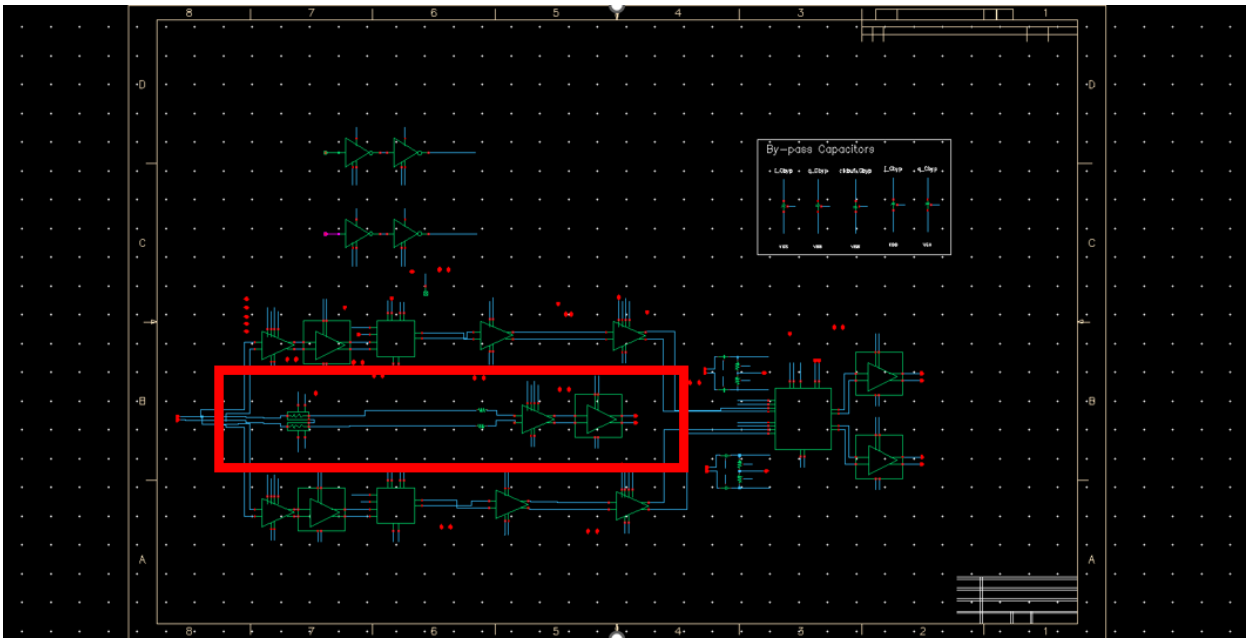
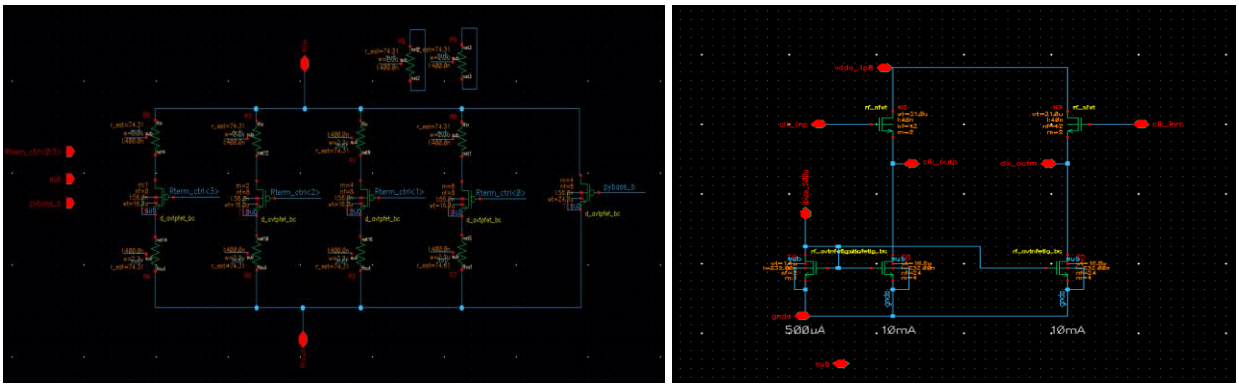


Figure 12 (a) the resistor control circuit (b) the buffer for the clock



(a) (b)

Section 3: it has the PRBS analog output multiplexer, and the need for is to use the same path of PRBS as an input for an external sinusoidal wave for the mixers for the sake of testing the capability of the TX chain under different frequencies and for some image rejection tests for the TX.

And in Figure 14 we show the analog multiplexer for output multiplexing of the PRBS.

Figure 13 section 3 in the I/Q PRBS loop

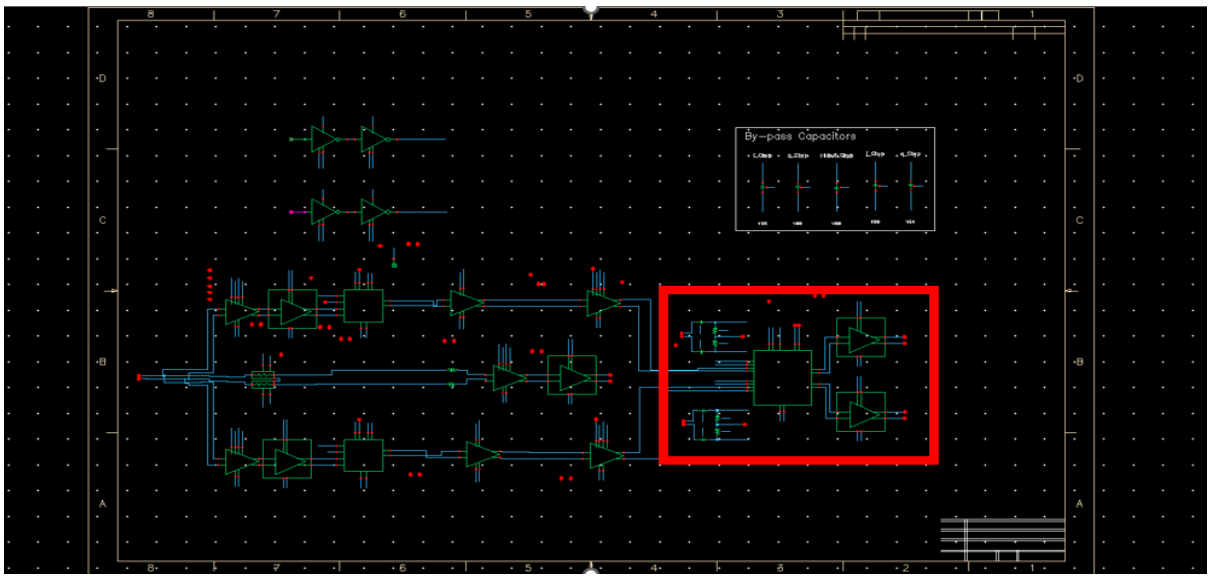
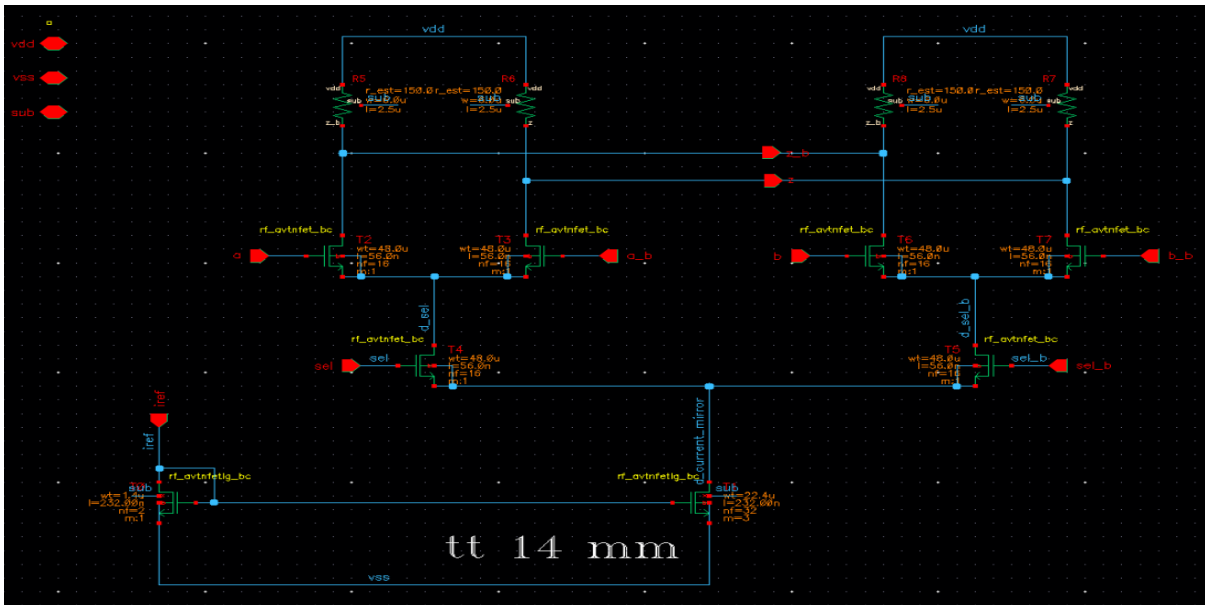


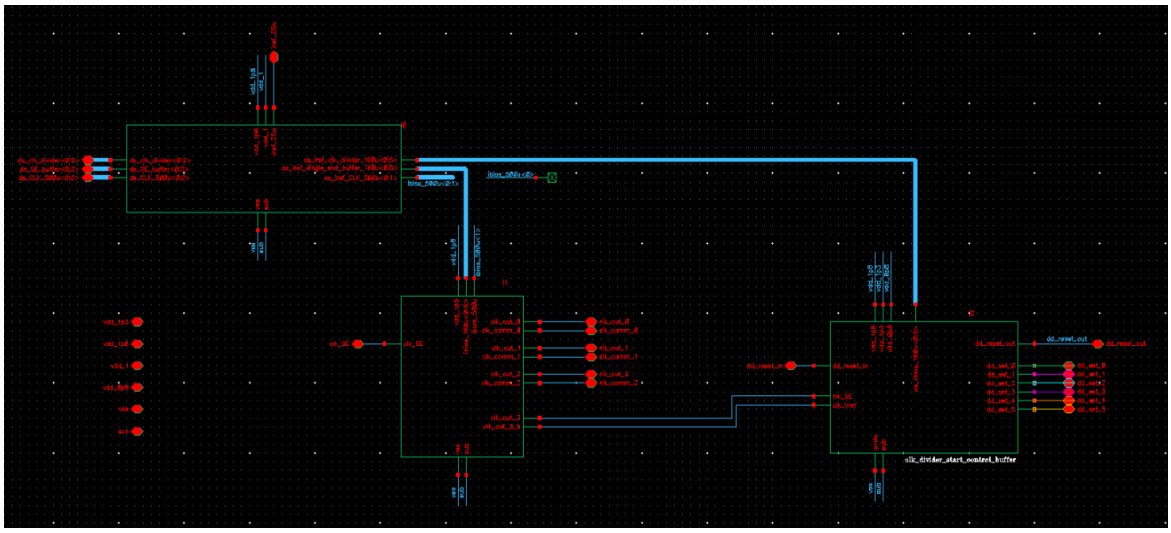
Figure 14 output multiplexer



1.2. The start control unit

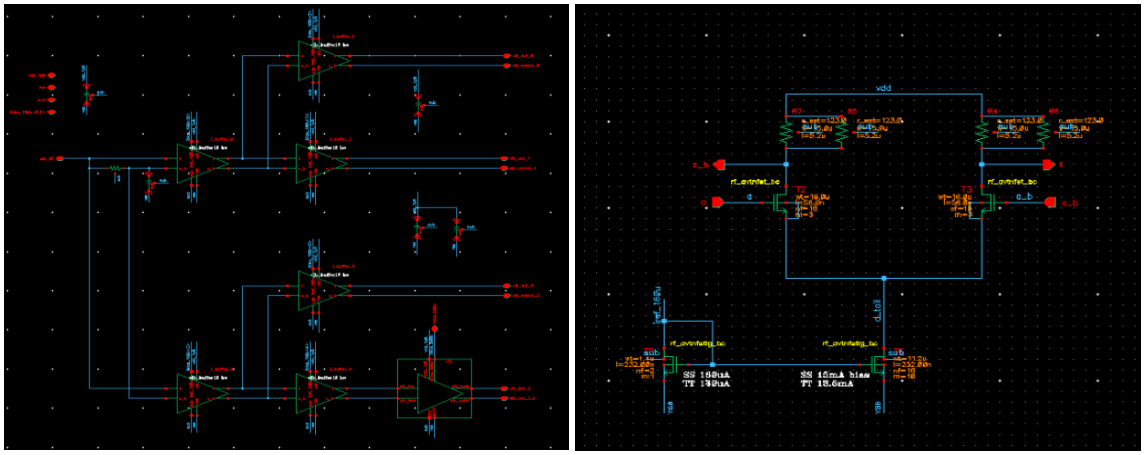
The start control unit is the block responsible for sending the start signal to the various PRBS loops, the need for different start timing was to minimize the correlation between the loops to get more uniform output constellation with equal symbols probability, the run length for our 9-bit PRBS is 510 bits and it repeats after that, the role of the start control unit is to send a start logic based on a clocked counter every 85 bit to 1 one of the 6 PRBS to start the PRBS loop and the schematic of the top level control unit is shown in Figure 15.

Figure 15 top level of the start control unit



In the top level we have 3 main blocks the top block is the controlled current mirrors, the bottom left is the clock buffers Figure 16, it receives a single ended clock from outside signal generator through a pad at 20 GHz and then turn the clock to be differential through an active balun before sending it to the various PRBS loops and finally, on the bottom right is the logic used to implement the delayed start signals.

Figure 16 (a) the clock active balun and buffering (b) active balun schematic



(a) (b)

In Figure 17 we show the start control logic top level with the DFF based clock divider and in Figure 18 we show the control unit, it is a counter based control unit that runs at lower clock frequency and receives the clock after passing by a divide by 8 DFF based divider and the counters are shown in Figure 19 and the divider is shown in Figure 20.

Figure 17 start control logic top level.

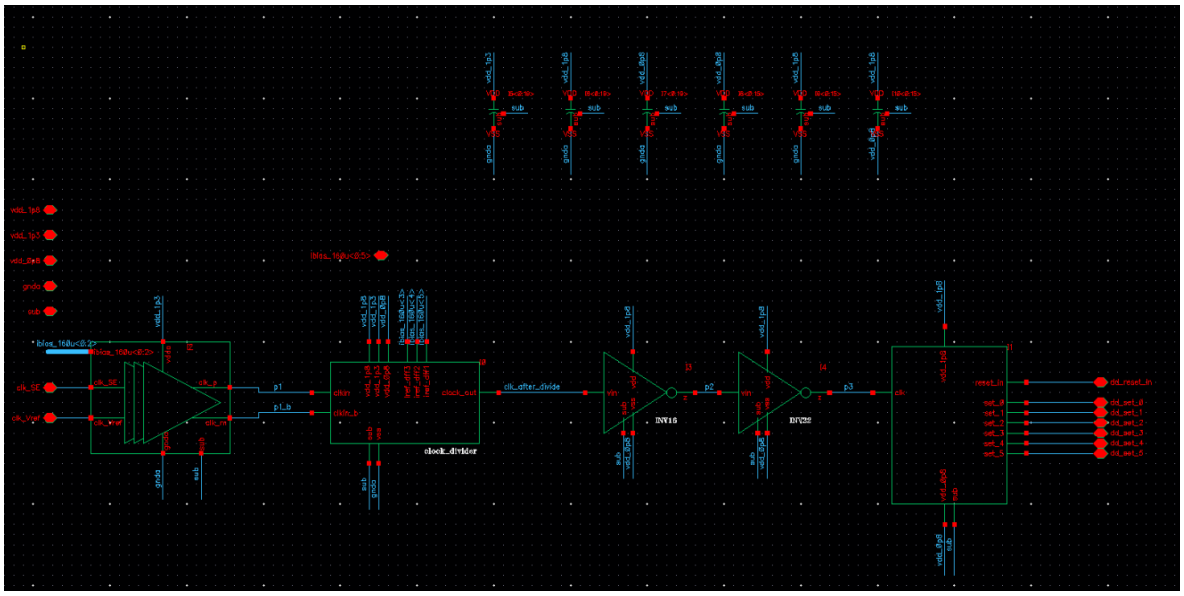


Figure 18 control unit

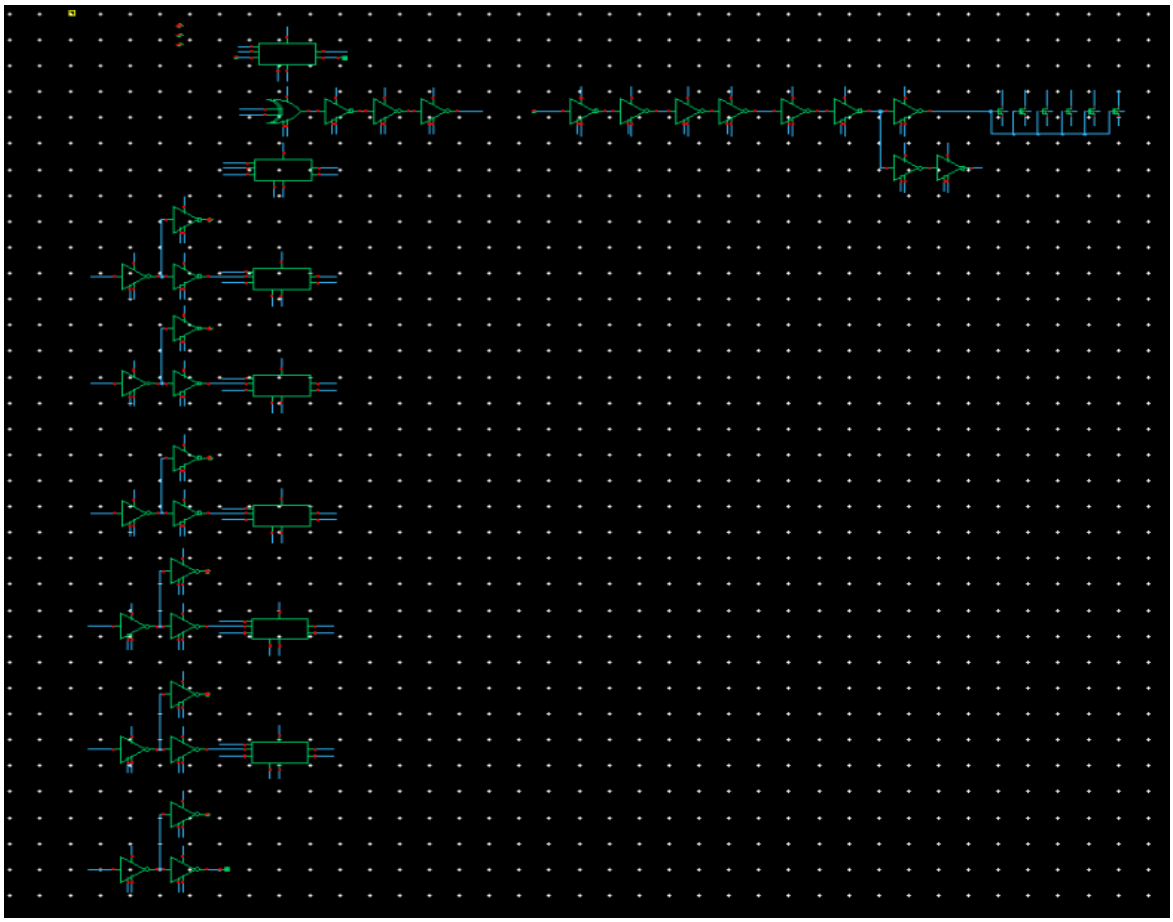


Figure 19 counter unit

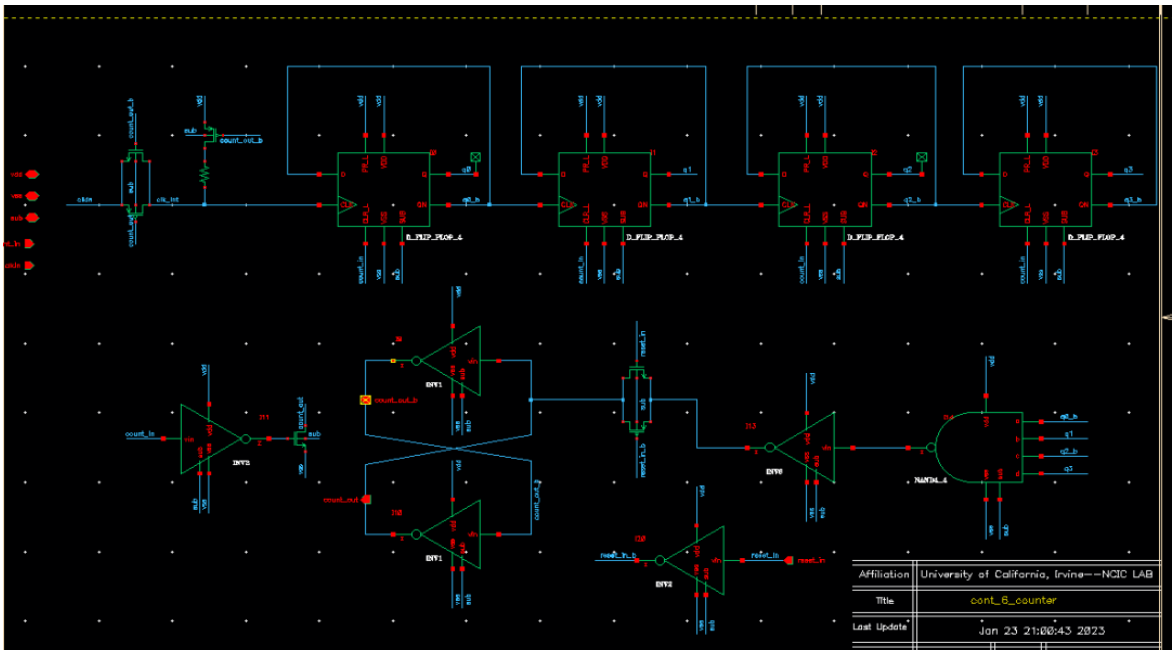
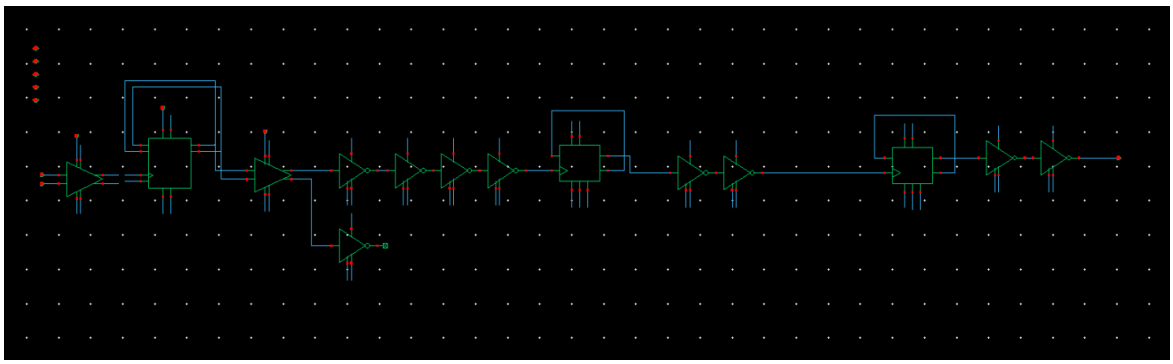


Figure 20 divide by 8 DFF based divider.



1.3. The PRBS output distribution network

AS mentioned before the goal of PRBS is to send random data to a TX array that is comprised of 4 array elements every element is a 3 QPSK transmitters combined together to generate a higher order QAM constellation, and for that to happen we need to distribute the PRBS and the clock used to generate that PRBS output across the whole chip which is 5x5 mm squared evenly with the minimum group delay difference for the integrity of the constellation and to accurately retime it again at the Mixer input, and also to minimize the loss and attenuation caused by this huge network and to buffer the signal again if needed and in Figure 21 and Figure 22 we share the full distribution network before going in to details, and all these structures are EM simulated using Sonnet software.

Figure 21 top level distribution network schematic

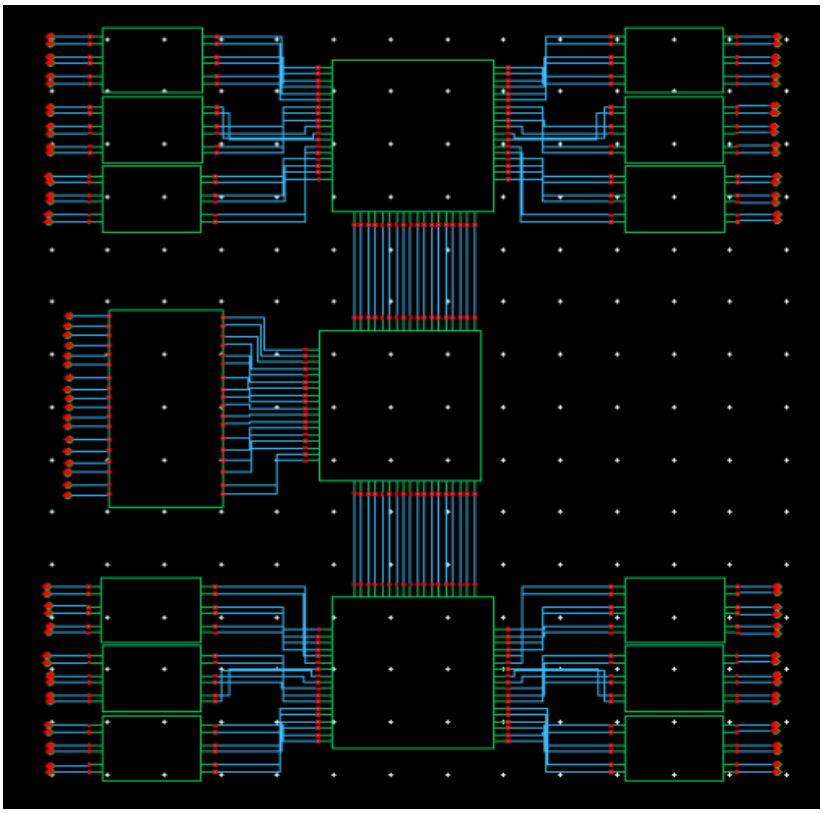
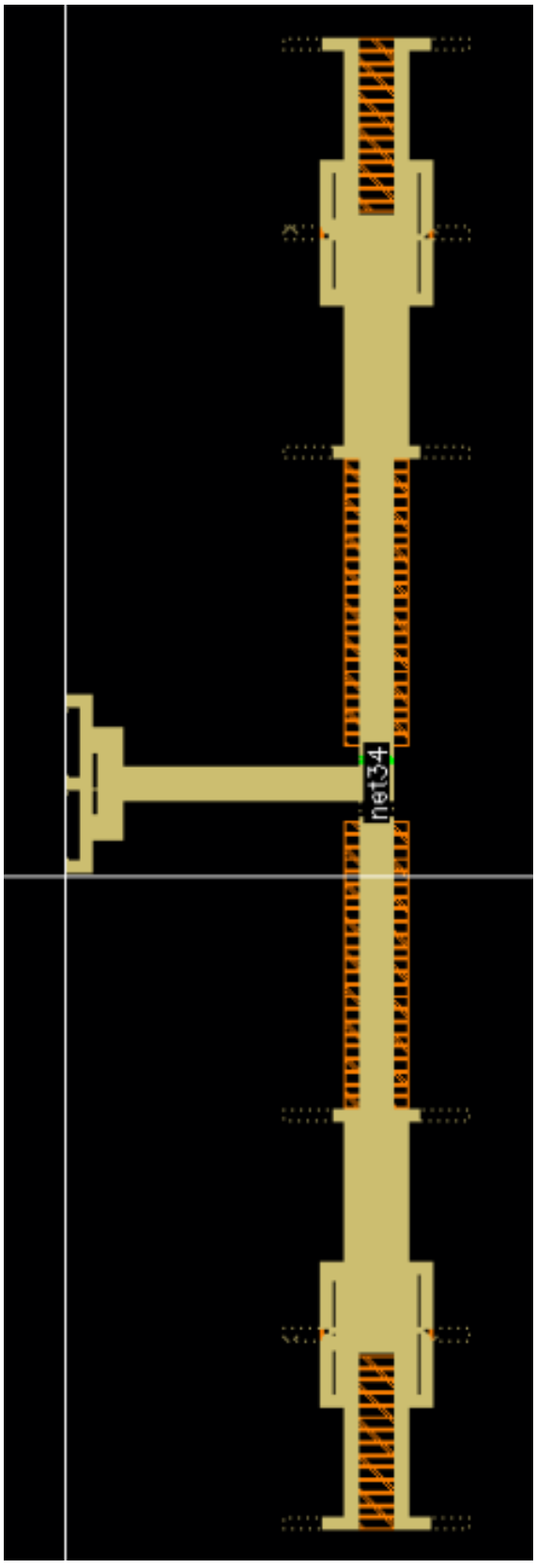


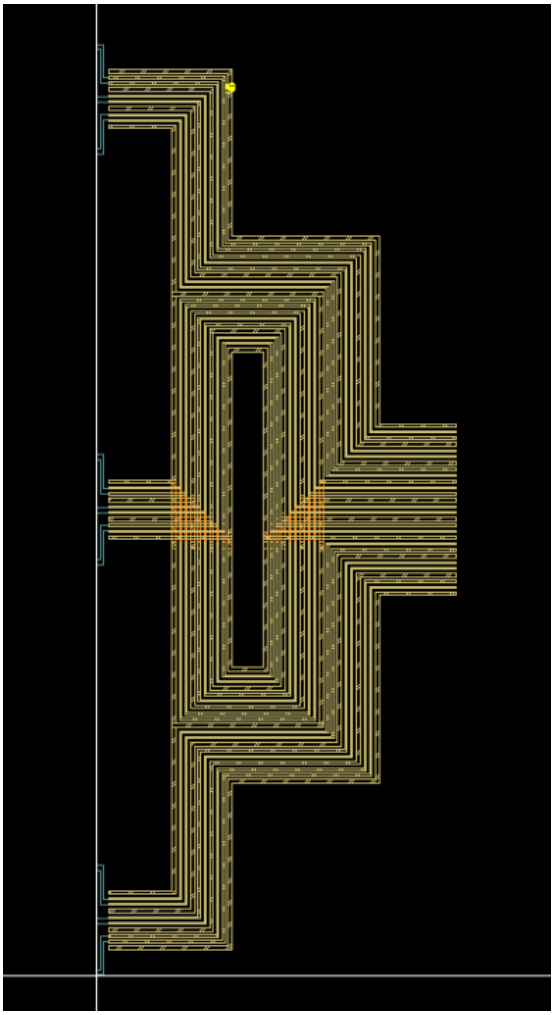
Figure 22 top level of distribution network.



The distribution network can be divided into 3 main parts:

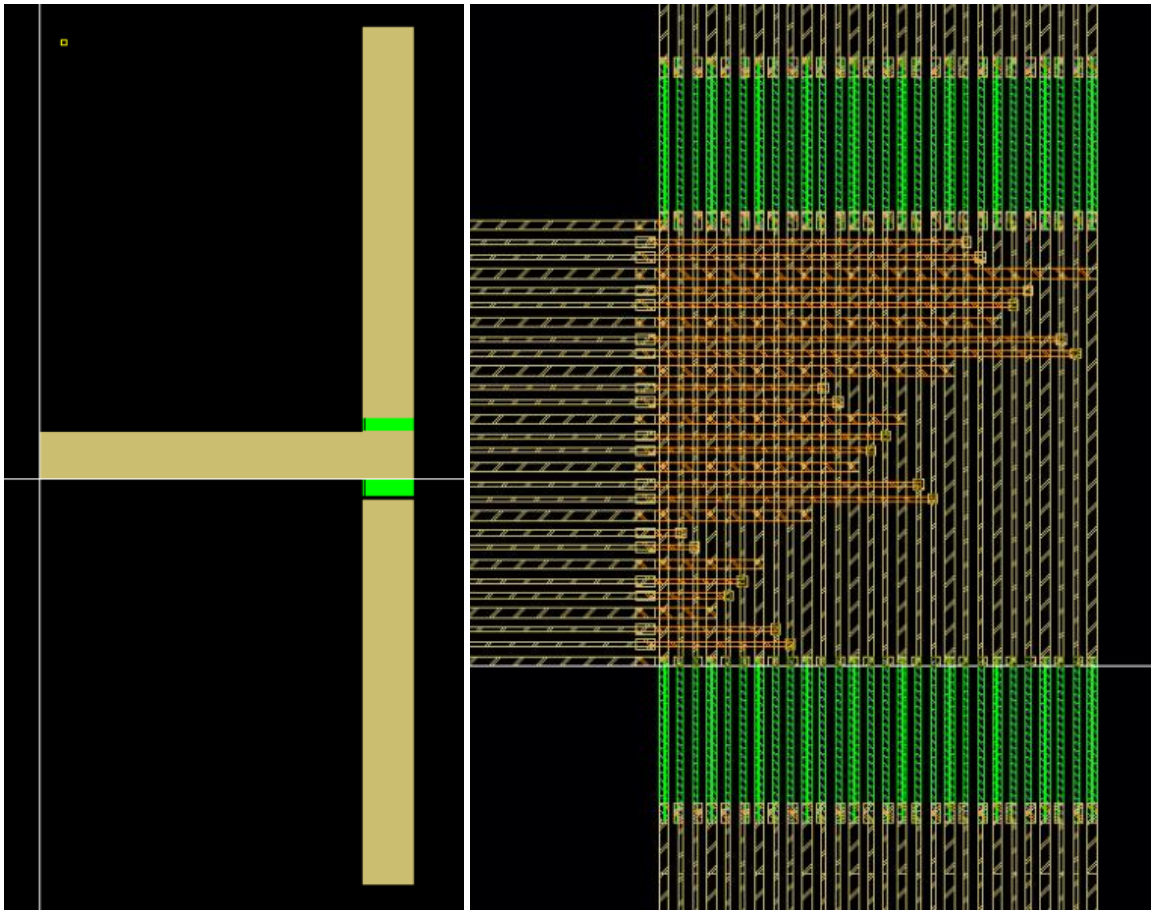
Part 1 Figure 23: is the input to the distribution network and this part was challenging in designing the middle loop so that the 3 inputs of it reach its output with the same group delay < 2ps group delay for our 50ps period PRBS signal, and the core of the design is the dimensions of the loop in the middle that accounts for the added delay to the middle path to be the same as the 2 identical paths from top and the bottom.

Figure 23 Part 1 of distribution network



Part 2 Figure 24: is the T matrix is responsible for distributing the signals to the correct QPSK transmitter, there is no problem of group delay mismatch here as all routes are identical, but the challenge was to minimize the attenuation to the signal due to the long routes.

Figure 24 (a) the full T matrix (b) the T matrix connections

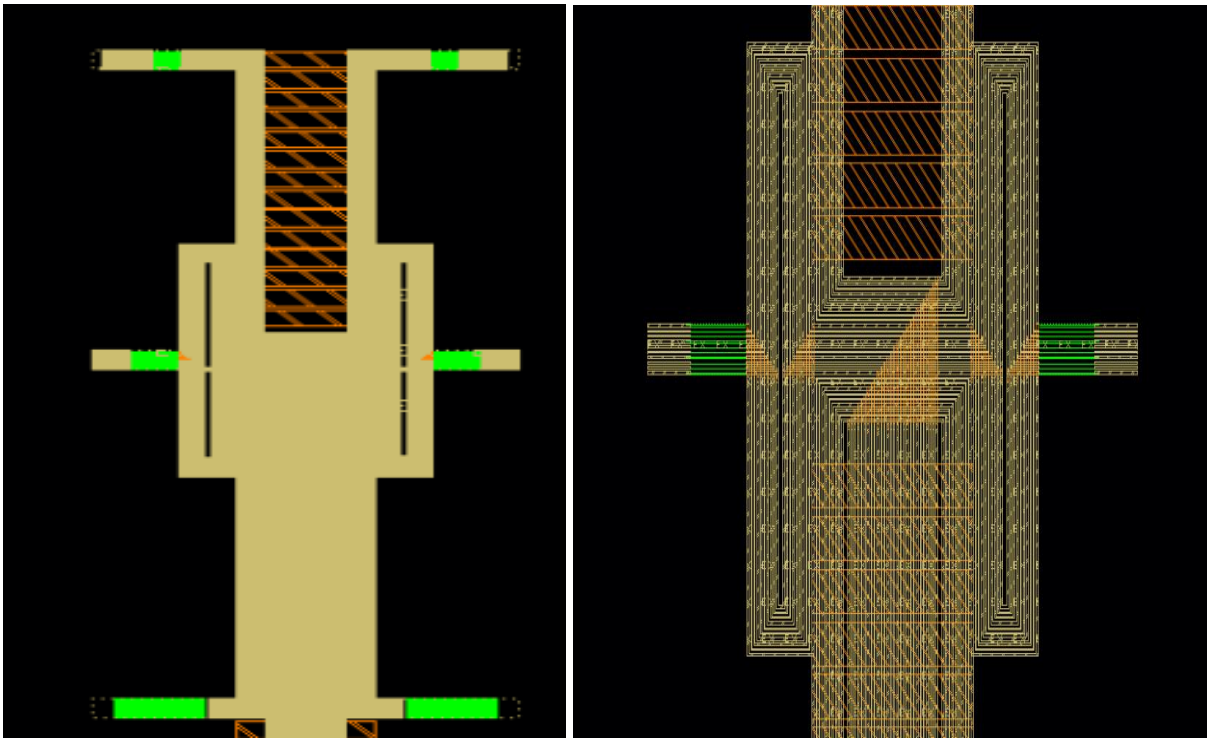


(a) (b)

Part 3 Figure 25: part 3 is the hardest to design part because now we have to equally

branch both left and right for the same PRBS output in addition to keeping the group delay difference as low as possible as mention in part 1, another special issue that arouse during our design was the intersection with LO signals as we are not getting closer to the array elements which we solved using these green bridges shown in the figure while making sure that these bridges does not affect the goals of the distribution network that we mentioned before.

Figure 25 (a) Part 3 the ending of the distribution network (b) zoomed in version of part3



(a) (b)

1.4. The Simulation Results

In this section we share the schematic simulation results, we start by the PRBS output at 20 GHz and the clock output as well we share the transient and eye diagram as shown in Figure 26 and Figure 27

Figure 26 PRBS output transient and eye diagram.

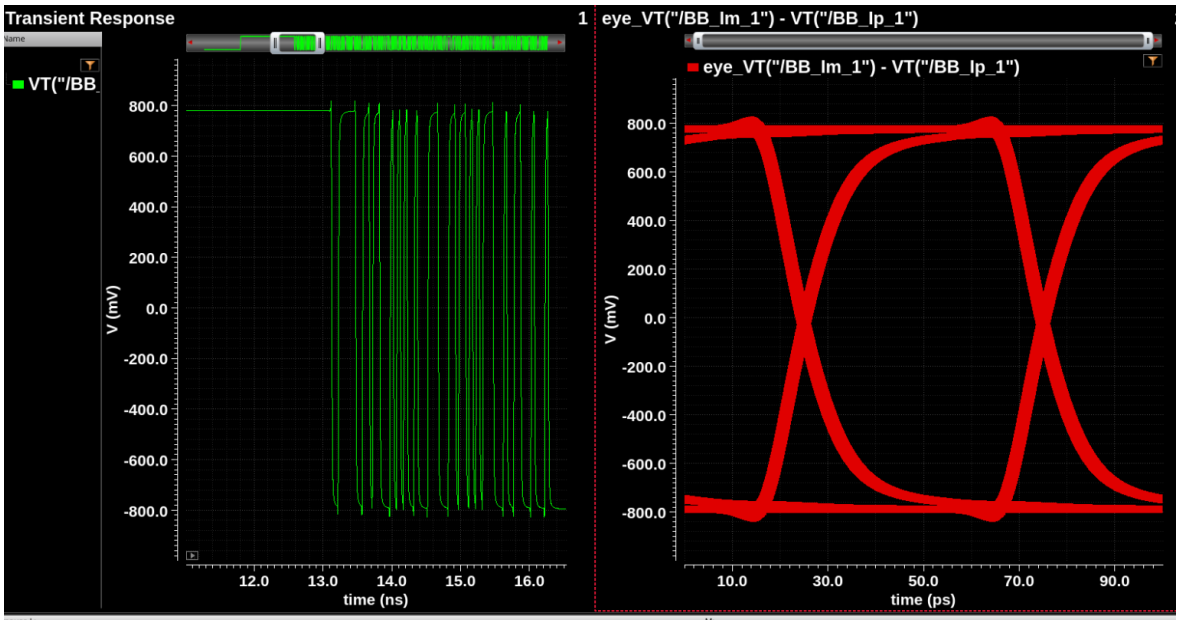
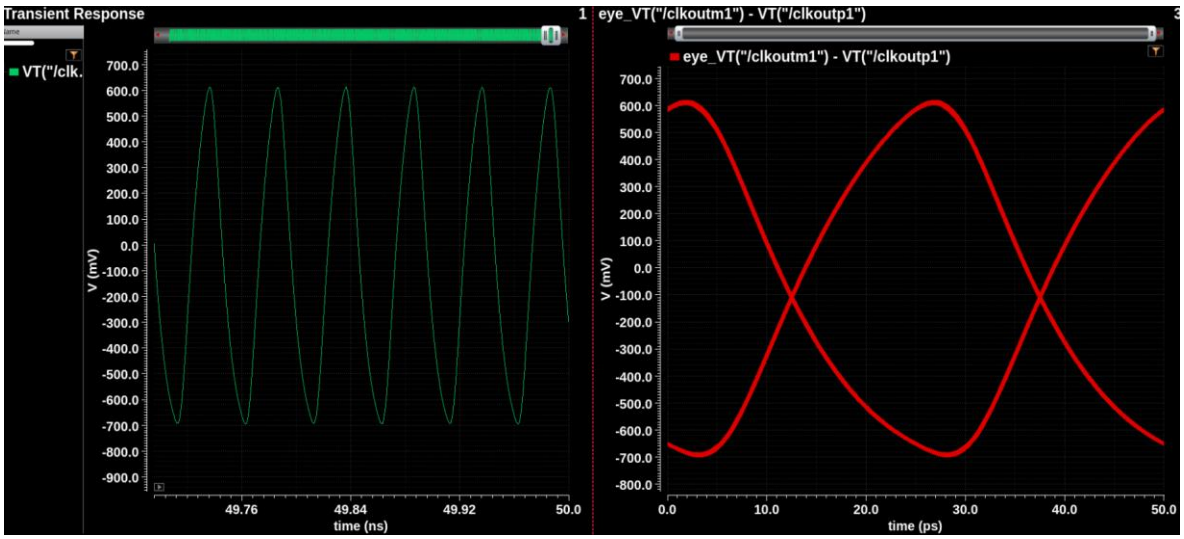


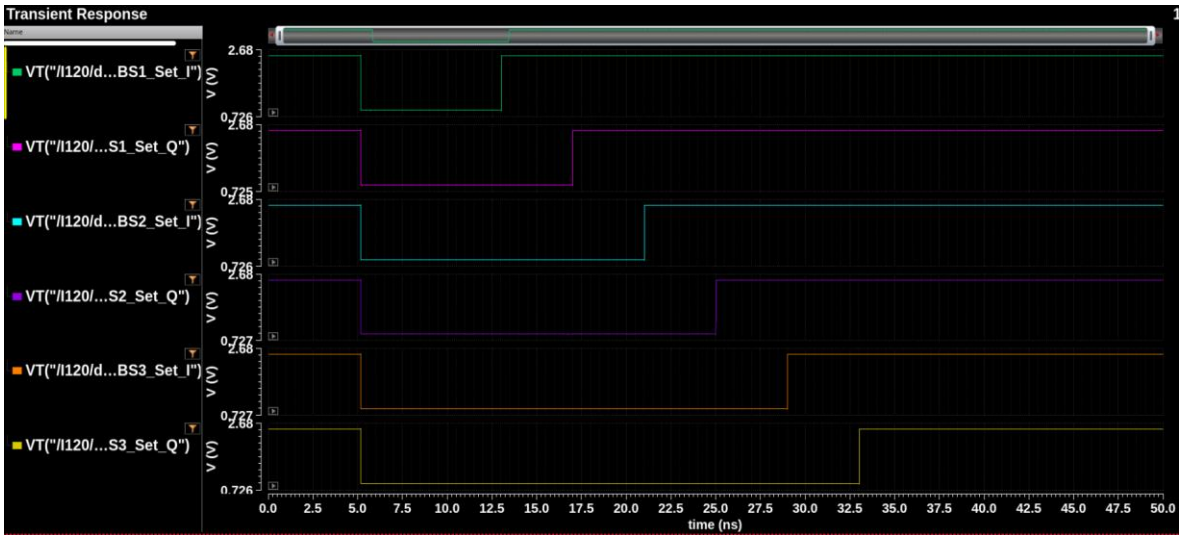
Figure 27 Figure 28 PRBS clock output transient and eye diagram.



We share the output of the control logic as well to see the different start sequences sent to the different PRBS loops to verify the control unit operation.

So as seen in Figure 28 the start signal sent to every PRBS loop arrive at a different time and they are ~ 85 bits apart which is equal to around 4.2 ns difference in time to assure that the correlation between the output random codes is as low as possible.

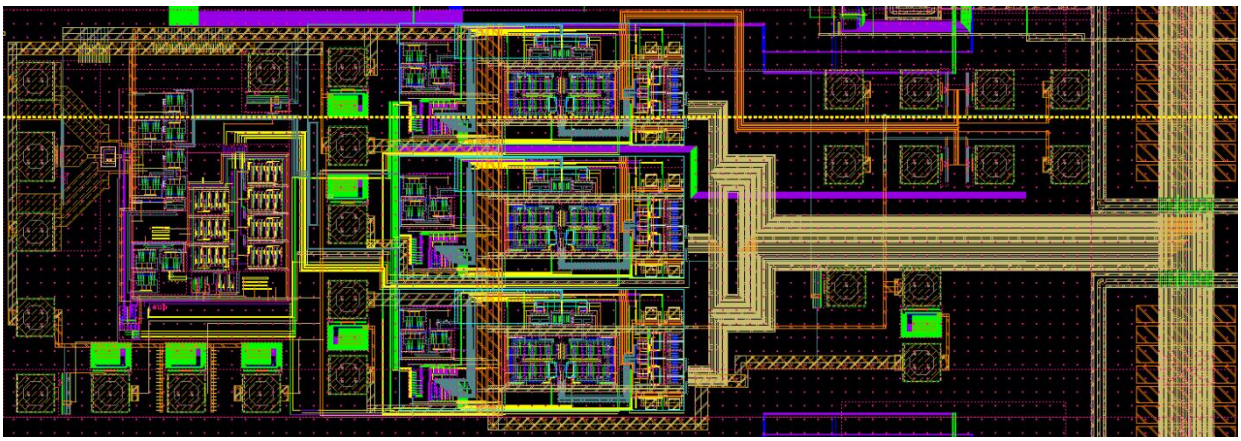
Figure 28 control unit set signal.



Chapter 2. Layout of the PRBS

In this chapter we present the Layout of the PRBS along with the post layout simulation results. In **Error! Reference source not found.** we show the top level of the PRBS layout including the flip chip pads. The area is 1.2 mm x 0.8 mm, and the details for the layout are presented next.

Figure 29 PRBS top layout



2.1. The PRBS loop layout

In this section we share the PRBS loops layout, in Figure 30 we share the top level connecting the 3 PRBS loops and in Figure 31 we share the details of every loop.

Figure 30 The 3 I/Q PRBS loops layout

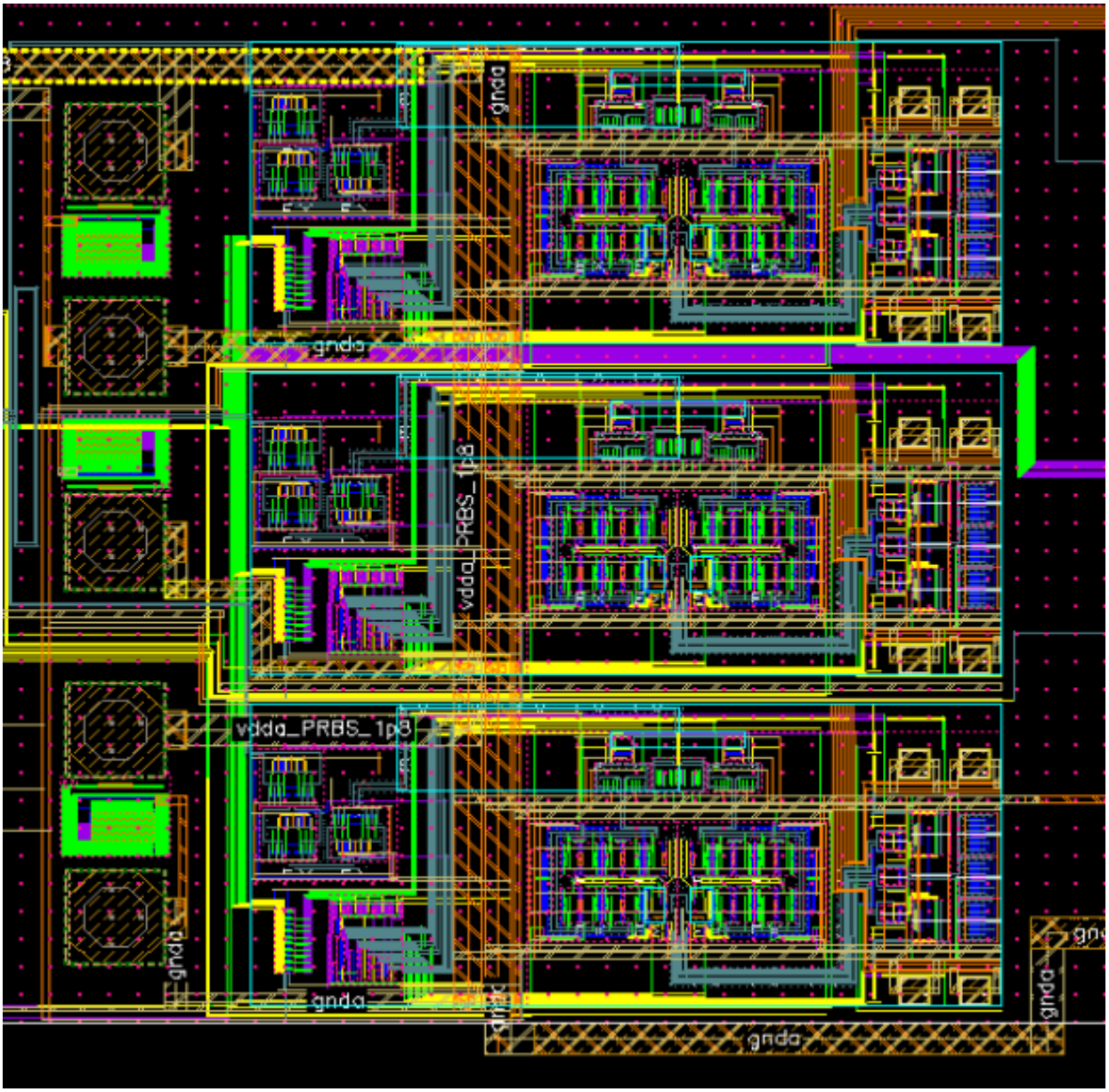
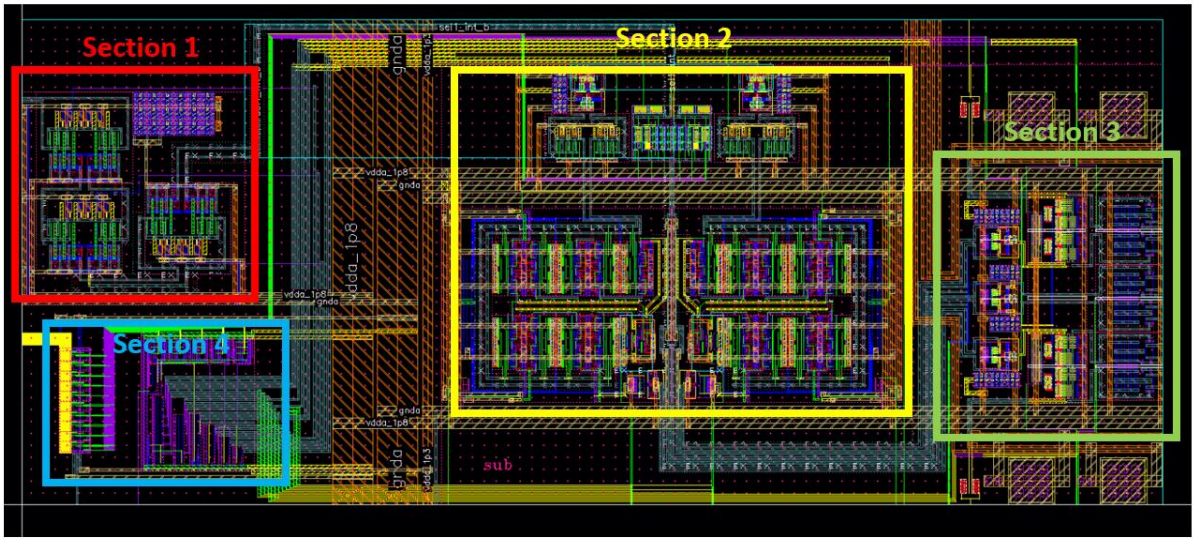


Figure 31 Detailed single loop layout.



Section 1: is the clock buffers for the clock signals as shown in Figure 6.

Section 2: is the main PRBS loop generation and amplification loop including the clock RC delay control circuit as shown in Figure 8.

Section 3: is the output multiplexer and the output buffer for the PRBS output as in Figure 8.

Section 4: is the PRBS controlled current mirrors that was mentioned in Figure 5.

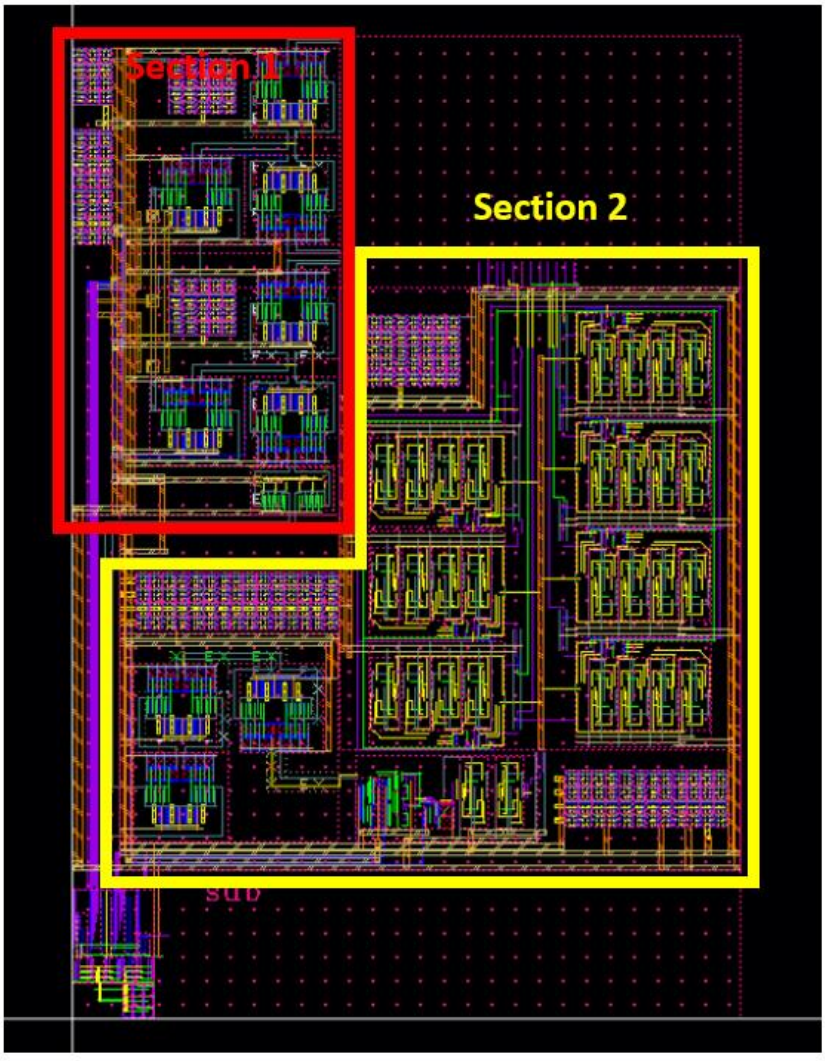
2.2. The control unit layout

In this section we share the control unit layout in Figure 32.

Section 1: is the clock buffers for the clock signals.

Section 2: is the main counter-based control unit for the set signal of the various PRBS.

Figure 32 Control unit Layout



2.3. Post layout extraction results.

In this section we share the post-Layout extraction results. We can see clearly the output eye diagram at 17 Ghz, 20 Ghz and 23 Ghz in Figure 33, Figure 34 and Figure 35 respectively. At the different clock frequencies, we had to increase the VDD for overclocking the PRBS, which in turn increase the LFSR DFF driving capability, so that the loop does not enter an ambiguous state where the output turns out to be only periodic and it loses the randomicity of the PRBS sequence.

Figure 33 PRBS output after PEX at 17 Ghz and 1.8V supply

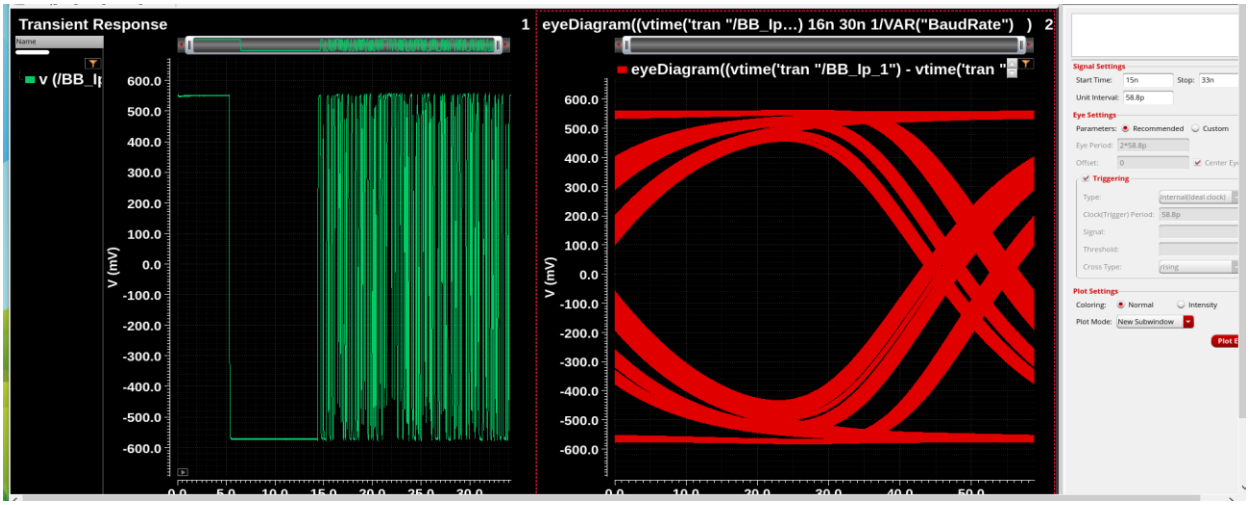


Figure 34 PRBS output after PEX at 20 Ghz and 2.5V supply

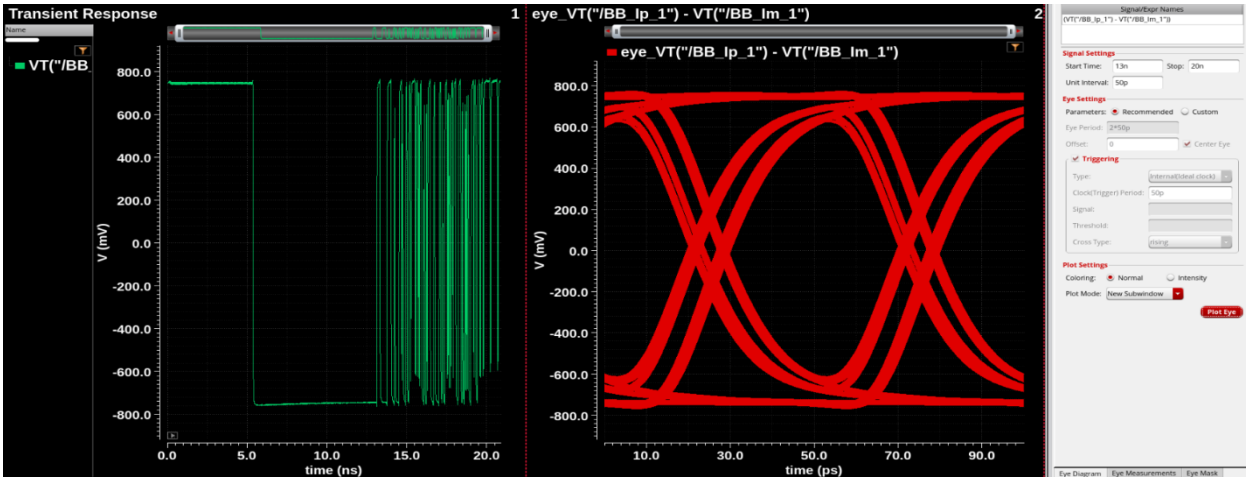
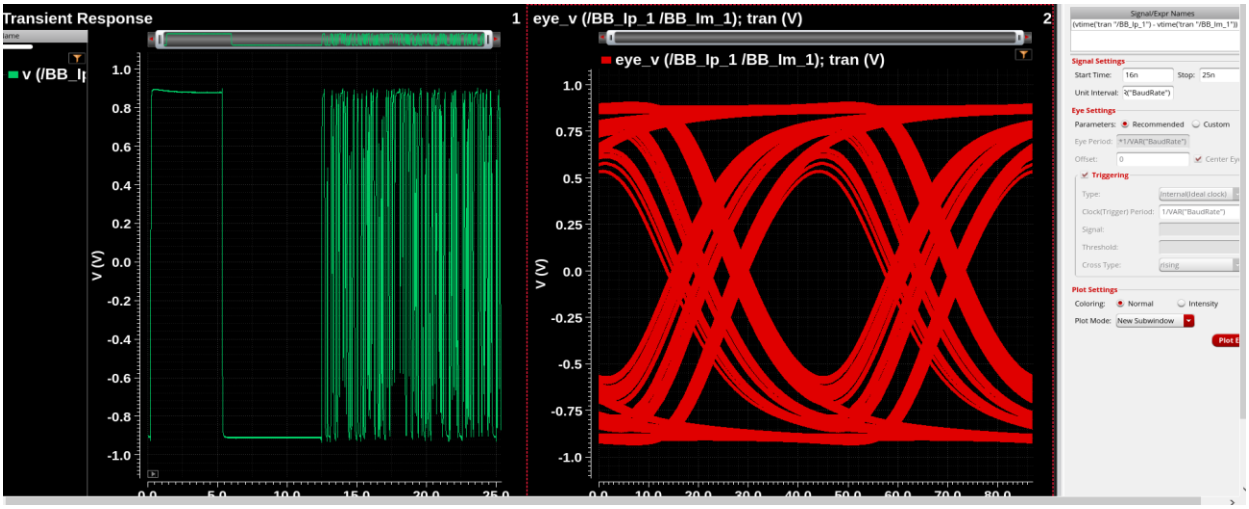


Figure 35 PRBS output after PEX at 23 Ghz and 3V supply



Chapter 3. CONCLUSION

In this work we presented a high speed PRBS working at nominally 20 GHz clock, for the use as a random data generator for mm-Wave transceivers, we presented out the system and its implementation in our 64 QAM transmitter, we also shared all the schematics and simulation results for our system including our routing integration for the TX array, and finally we shared the layout of the system along with detailed description of every layout sub-system within our main system and also shared our post-layout extraction results with the ability of overclocking the system with increasing the supply voltage.

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