Title
PEP-4 MUON PROPORTIONAL WIRE CHAMBER

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Publication Date
1979-11-01

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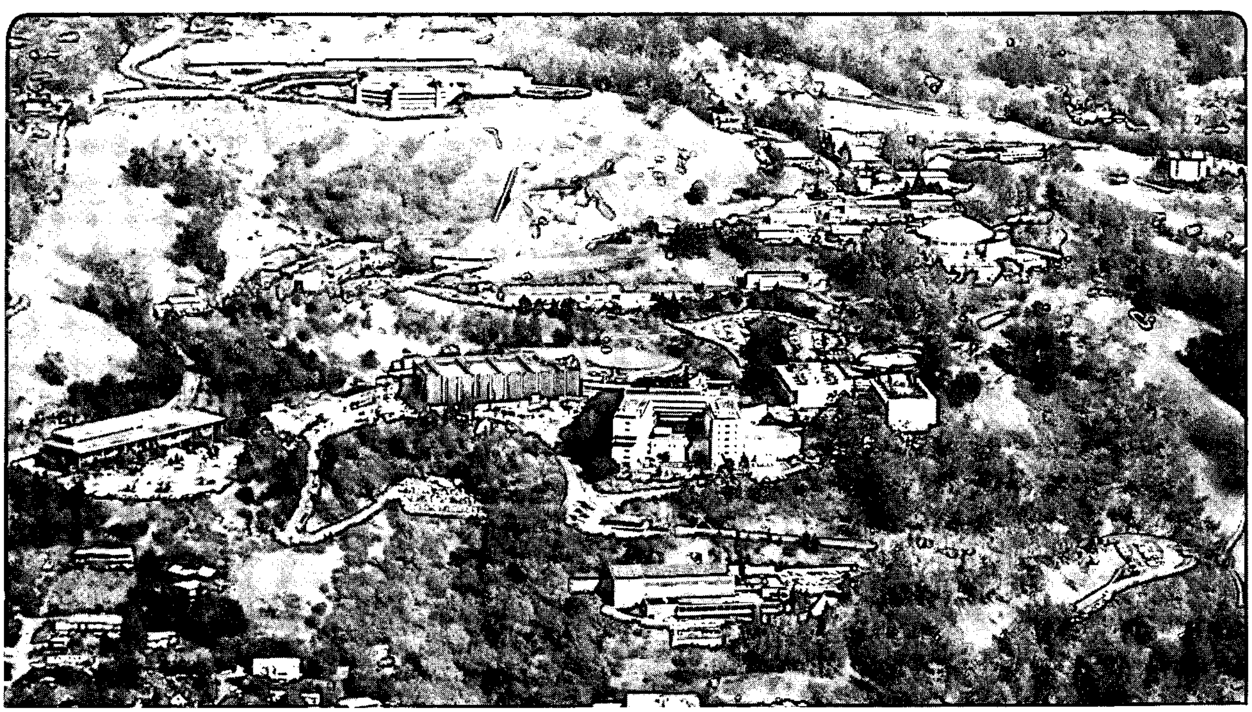

DISCLAIMER

SUBJECT: PEP-4 MUON PROPORTIONAL WIRE CHAMBER
NAME: M.Nakamura, S.Olson, R.Jared, B.Barnett
DATE: March 1, 1978

This engineering note describes the mechanical and electrical configuration of the muon proportional wire chamber (PWC's) to aid in the design and development of the electronic system to be employed with the muon detectors. It is assumed that the reader is familiar with the PEP-4 proposal [1,2] and its general principles.

The Muon Detectors

The high momenta muons can be detected by using thick iron filters surrounding the Time Projection Chamber (TPC) and the Liquid Argon Calorimeter. Two layers of muon PWC's will be mounted parallel to the beam at 204 cm and 250 cm respectively from the beam center line. The inner muon detector will have 330 wires while the middle muon detector will have 402 wires. At approximately 300 cm from the beam center line, muon x-y planes are located with 474 parallel (to beam line) wires and 672 perpendicular wires. See Fig. 1.

One pair of x-y planes and one separate vertical plane are located at each end outside the pole tips. The planes of these muon detectors are perpendicular to the beam. Figure 2 shows a plane of vertical PWC's indicating the number of extrusions needed in the plane. Each extrusion contains 8 wires for a total of 272/plane. Figure 3 shows the accompanying horizontal plane containing 288 wires. The vertical array plane will be located just outside the pole tips on each end of the PEP-4 detector. The x-y planes are to be placed outside the vertical wire plane and separated from it by 20 cm of iron filter.

Eight (8) equilateral, triangular-shaped extrusions formed together to form a single unit are shown in Fig. 4. This configuration lends itself to rugged, self-supporting, economical construction and modular configurations as shown in Fig. 1. Each side of the triangle will be 8 cm. The groups of 8 are also convenient from an electronic standpoint since we will have 8 or 16 amplifiers/board. This note is written for 8 amplifiers per board. A grand total of 3542 wires will be required. The chambers will be filled with argon-methane mixture at atmospheric pressure. The muon chambers will be electrically insulated from their supports.

Electrical and Electronic Characteristics of the Muon PWC's

The electrical characteristics of the chamber (based on calculations for an inscribed circle within the equilateral triangle) are as follows:

Wire diameter	50	μm
DC resistance	8.2	Ω/ft
Capacitance	2.5	pF/ft = 8 pF/m
Inductance	.4	μH/ft = 1.4 μH/m
Characteristic Impedance	410	Ω

The maximum drift time from the corners of any PWC is 2.3 μs. Eighty percent of the charge will be collected within the first 500 ns in most instances. The signal level will be about 0.5 pC dependent on the gas gain.

The preamplifier should have a rise time of the order of 100±50 ns and an output level of about 100 mV. The preamplifier should be capable of driving 100 ft. of terminated cable.

The preamplifiers will be mounted directly on the PWC's. Some of the preamplifiers will be relatively inaccessible so high reliability components must be used. Test points will be used to monitor signals--when access is possible.

To check out the di-muon trigger, ≈ 42 test pulses are required. A di-muon trigger requires a coincidence between one resolution unit (ru) on one of the outer pole tip x-y muon PWC's and one-of-nine ru's on the opposite pole tip x-y muon PWC. One resolution unit is 1 meter x 1/3 meter.

Calibration pulses will be sent to all PWC's. Broken wires can be partially detected with the calibration pulses, but a "frequency-of-hits" determination with real data can detect broken wires by the absence of hits.

Chamber High Voltage System

The chamber high voltage will be limited to 3200 V maximum. If a daisy-chain distribution system is used, it will be designed to minimize the possibility of a bad connection at any one point from affecting the voltage at other points. The voltage will be monitored by the computer but will be adjusted manually. Circuits will be provided for automatically cutting off the high voltage if the current exceeds a preset level.

The possibility of a sense wire breaking (and grounding) should be taken into account in the design of the distribution and protection system. A ground on one wire should not impair the proper operation of other channels.

Cabling, Preamplifier Output

The cabling from the preamplifier outputs to the digitizer boards will be coaxial, tentatively flat, mass-terminated type with ten lines per assembly with eight used for wire signals. The cable conductors may fan out directly to the preamplifier output connectors (single), or they may pass through a transition connector between the individual lines from the preamplifiers and the flat cables to the digitizer boards. The first approach would be desirable from reliability and material cost considerations. The second approach would be easier to work with during original cabling and assembly operations.

Digitizer Board

The preamplifier output signals will be received at the digitizer board (8 or 16 channels per board) in the counting area. (See Fig. 5) A comparator per channel will provide a stop signal to the time digitizing circuit. A bus will supply a centrally adjustable threshold voltage to all comparators. The digitizer will provide four bits of non-linear resolution with the higher resolution at the shortest drift paths. To provide this the digitizer clock "period" will increase in a binary progression, i.e., the ratio of 1, 2, 4, 8, 16, etc. The sum of the periods will cover at least the maximum drift time of 2.3 μs. Tentatively the minimum period will be 50 ns.

Digitized data (4 bits) and address data (13 bits) will be read onto an output bus on command from the controller. The bus will be part of a daisy chain cable linking all muon detector readout electronics to the Large Data Buffer. The daisy chain cable will also have control lines carrying signals between the controller and muon digitizer electronics bins. (See Fig. 6) A summary of signal lines is given below:

Digitizer Board Input and Output Signals

Digitizer board signal exit and entry will be via a card edge connector on a motherboard (or other backplane arrangement), and a transition header to a cable connector for signals coming from the preamplifiers at the chambers. The signals and their function and characteristics are listed below:

1. CHØ-CH7 $\triangleq$ eight channel signals from the preamplifiers via a transition header mounted on the digitizer board.

2. TEST $\triangleq$ a signal to all channels which will cause all discriminators to trigger.

(The following signals all utilize the printed circuits edge connector mounted on the backplane. Signals are TTL negative-true levels unless otherwise indicated.)

3. DIGITIZER CLOCK $\triangleq$ a clock-pulse train to be used in the digitizer circuits. Tentatively, a differential signal.

4. C/O $\triangleq$ a timing signal that specifies when there has been a beam crossing. Tentatively, a differential signal.

5. MASTER CLEAR $\triangleq$ resets all circuits on the card.

6. HOLD $\triangleq$ prevents discriminators from triggering.

7. RESET $\triangleq$ resets all circuits on the card except the discriminator level register if used.

8. BOARD LOCATION CODE $\triangleq$ four lines providing a unique binary address at each digitizer card socket.

(The following signal lines are in the readout bus system.)

9. Data, T_0-T_3 $\triangleq$ binary count representing the length of the time measurement. (4 bits, non-linear)

10. Address, A_0-A_{12} $\triangleq$ binary count representing the address or location of the channel of the digitizer being readout. (13 bits)

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11. DATA PRESENT $\triangleq$ a signal line active whenever there is any data in any of the digitizer card registers. It originates on the digitizer cards and is used in the controller.

12. ENABLE $\triangleq$ this signal is generated by the controller and is used on the digitizer cards to place data onto the readout data bus lines T_0-T_3 and A_0-A_{12}. The signal progresses from digitizer cards with low addresses to those with higher addresses. It advances on command from the controller.

13. ADVANCE $\triangleq$ this pulse is generated by the controller to clear a word just read from a digitizer register and cause the digitizer board readout control circuits to advance to the next register having valid data.

14. MUOR $\triangleq$ this signal is used by the trigger to make up the 1 meter x 1/3 meter resolution unit.

References

1. "Proposal for a PEP Facility Based on the Time Projection Chamber," PEP-4, December 30, 1976, JHU, LBL, UCLA, UCR, and Yale U.

2. "The Time Projection Chamber Facility at PEP and Prospects," a collaborative group of JHU, LBL, UCLA, UCR, and Yale U, presented at Nucl. Sci. Symposium San Francisco, October 1977.

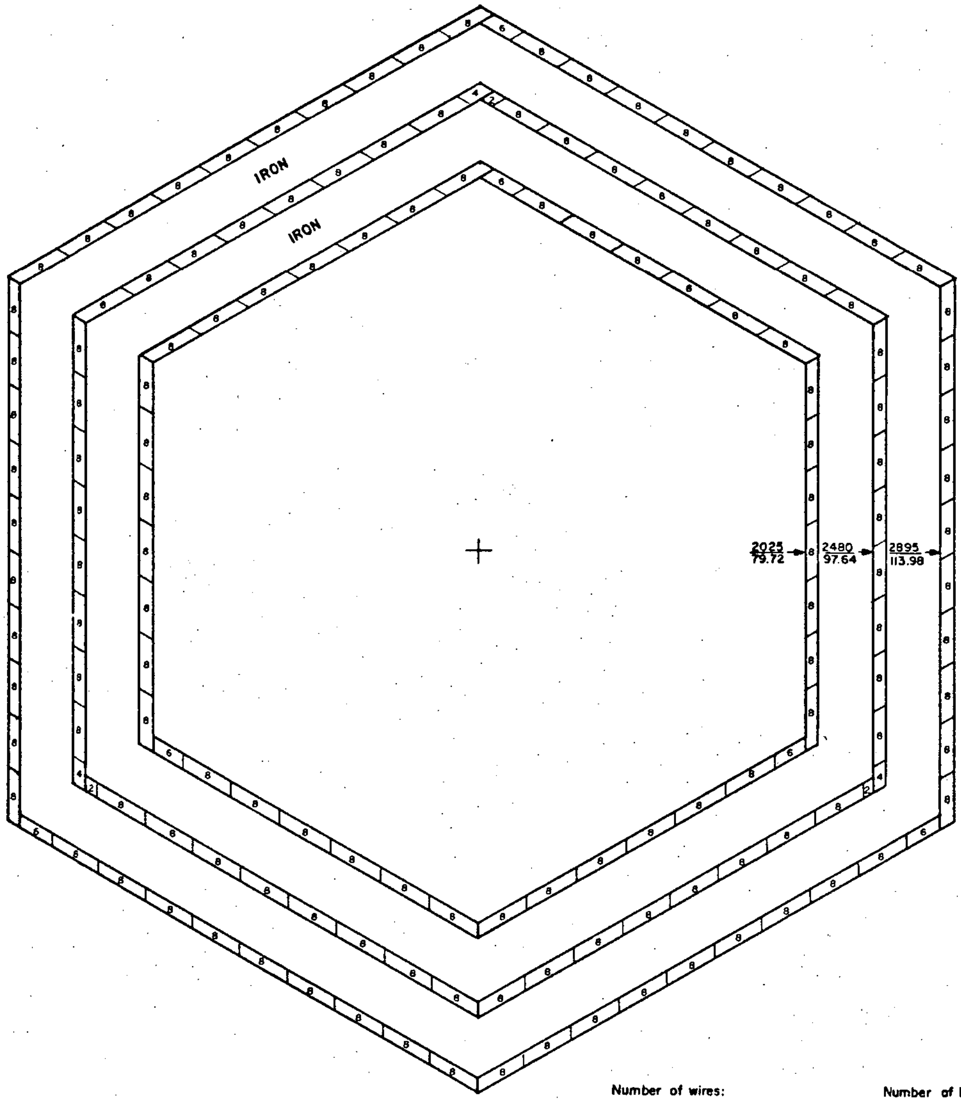

FIGURE I
HEXAGONAL DRIFT CHAMBER ARRAY
The System shown above allows 34.3cm per 8 wire module.
This must include the Intra Module Gap and Insulation.

Number of wires:

Inner	330	Total : 1878
Middle	402	
Outer (parll)	474	
Outer (perp)	672	

Number of PWC's (before cutting)

Inner	48
Middle	51
Outer (parll)	60
Outer (perp)	85 (15/side)

Drawing is not to Scale.
All Measurements are $\frac{\text{mm}}{\text{Inches}}$

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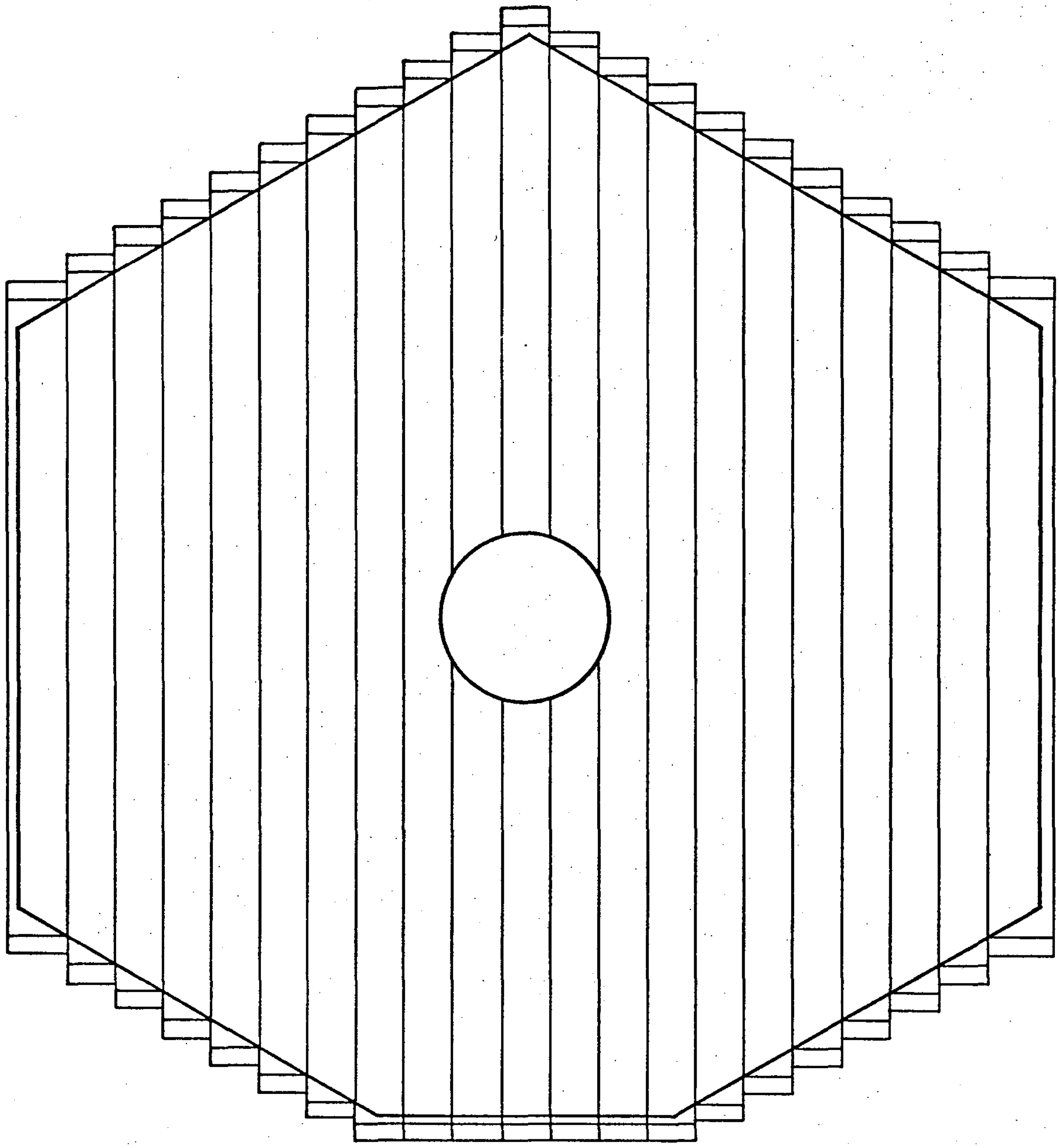

FIGURE 2
VERTICAL (X) END ARRAY
24 Extrusions/Plane x 4 Planes = 96 Extrusions
192 Wires / Planes x 4 Planes = 768 Wires
Approximately 132 meters of Extrusion required per Plane.

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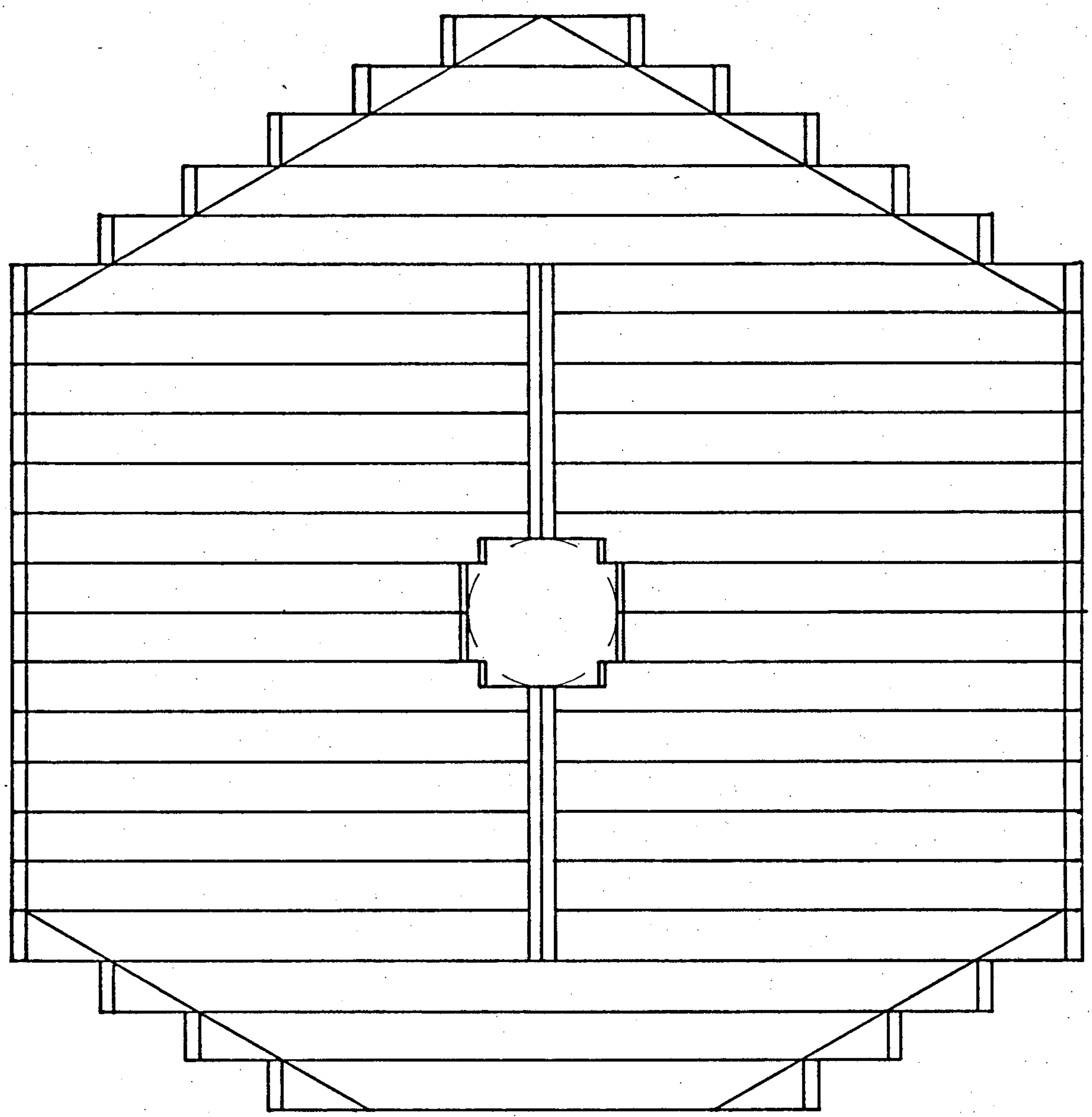
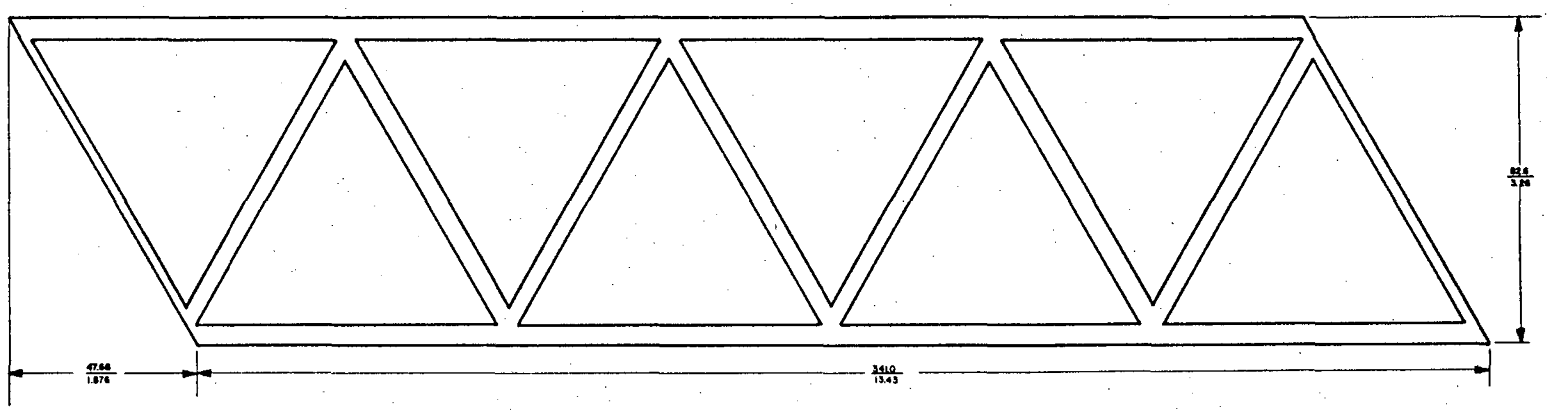


FIGURE 3
HORIZONTAL (Y) END ARRAY
36 Extrusions/Plane x 2 Planes = 72 Extrusions
288 Wires/Plane x 2 Planes = 576 Wires
Approximately 132 meters of Extrusion required per Plane

XBL 783-7709



NOT TO SCALE
ALL MEASUREMENTS $\frac{\text{mm}}{\text{inches}}$

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FIGURE 4
CHAMBER EXTRUSION DETAIL

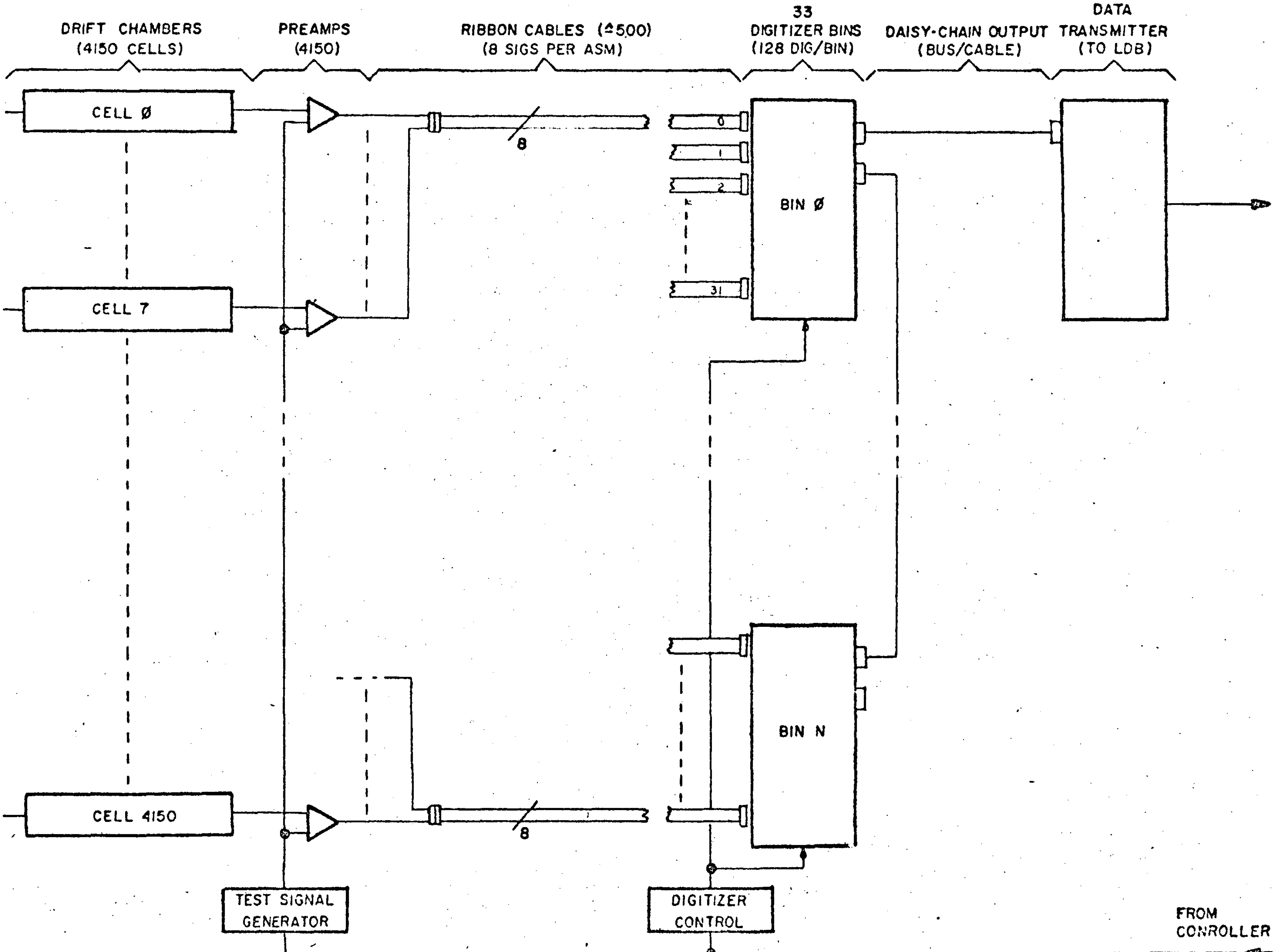

Figure 5 MUON DETECTOR READOUT SYSTEM GENERAL DIAGRAM

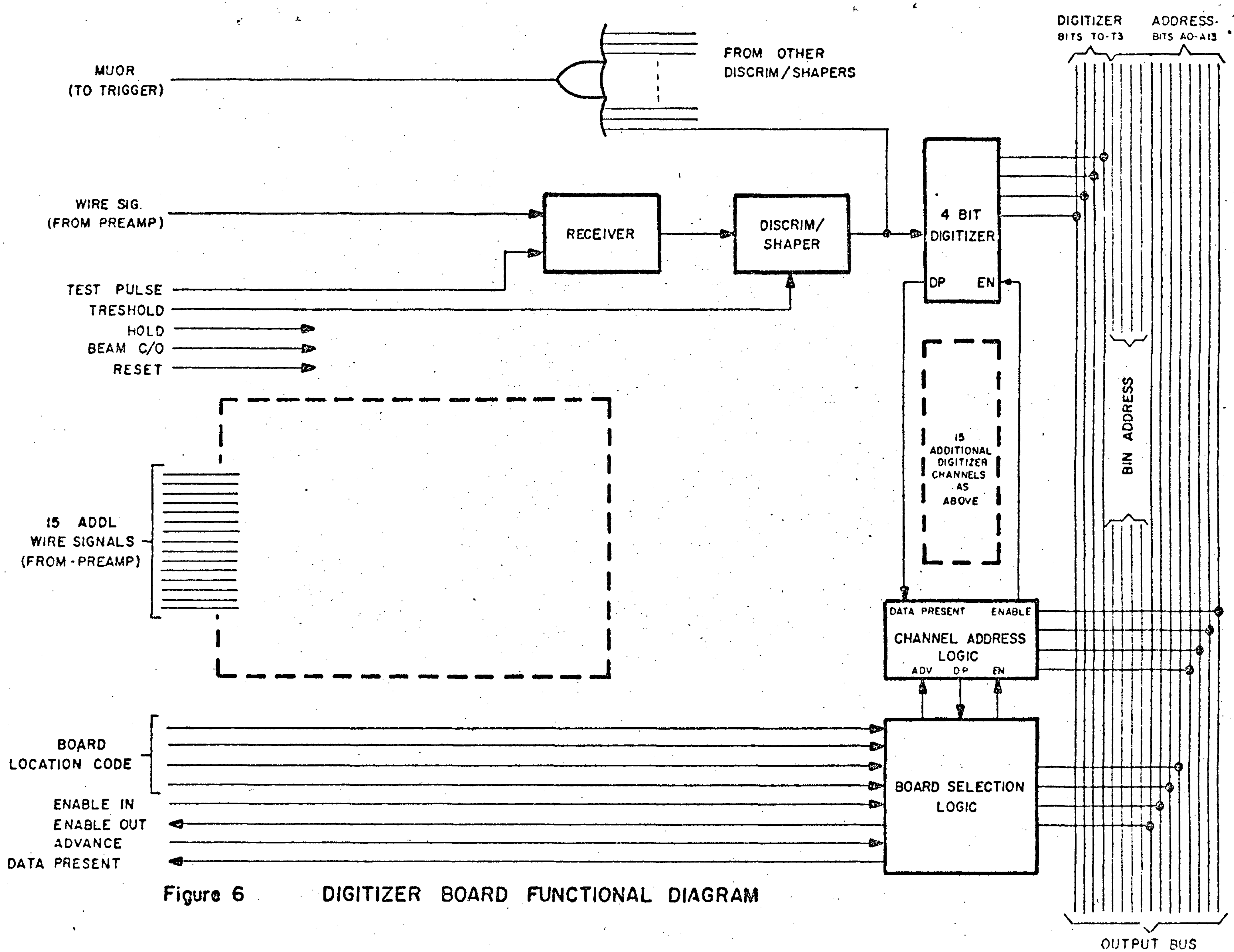

Figure 6 DIGITIZER BOARD FUNCTIONAL DIAGRAM

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