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Cleave Engineered Layer Transfer for III-V Devices via
Electrochemical Etched Porous Indium Phosphide

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in Materials Science and Engineering

by

Xiaolu Kou

2014

ABSTRACT OF THE DISSERTATION

Cleave Engineered Layer Transfer for III-V Devices via
Electrochemical Etched Porous Indium Phosphide

by

Xiaolu Kou

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2014

Professor Mark S. Goorsky, Chair

Cleave Engineered Layer Transfer (CELT) is a technique which enables transferring large scale high quality epitaxial layers and devices onto alternative substrates through mechanically engineered substrates. The objective of this dissertation was to formulate a methodology to understand whether the formation of a porous III-V layer, with focus here on indium phosphide,

can be feasibly employed to transfer III-V device layers with preserved crystallinity from the host substrate. The porous structures were prepared on (001) oriented InP substrates by electrochemical etching in diluted hydrochloride acid (HCl). The porosity of the layers was reproducibly controlled by etching parameters, such as current density and electrolyte concentration, and a numerical relationship between layer porosity, p and its Young's modulus, E as $E = 87(1-p)^4$ was determined. This relationship was important for relating the etching parameters to the mechanical strength of the buried layer. Annealing (temperature range 450 °C- 650 °C and time range 10 min- 8 hours) modified the porous layer morphology and was found to be beneficial for subsequent epitaxial growth and layer fracture. The morphology of the porous layers was monitored by scanning electron microscopy (SEM) and the epitaxial layers were studied by high resolution X-ray diffraction (XRD) and transmission electron microscopy (TEM). Nano-indentation was used to measure the Young's modulus of the porous InP layers. In some cases, dual porous layers were produced by changing electrolyte concentration and current density during the porous formation process. The top layer is less porous than the buried layer, with a surface pore fraction of less than 30%. The deeper, more porous buried layer was shown to facilitate fracture in the deeper layer and not through the denser, near surface layer, thus controlling the layer fracture formation through the buried layer only.

Epitaxial deposition of InP on the dual layer porous structure was achieved. The overlying epitaxial InP layer was found to possess a low threading dislocation density and demonstrated complete coalescence of the InP lattice. Specifically, TEM analysis showed the epitaxial layers were single crystalline and lattice registered to the porous layer, and neither grain boundaries nor threading locations were detected over a $35 \mu\text{m}^2$ sampling areas, indicating a threading dislocation density lower than $3 \times 10^6 \text{ cm}^{-2}$. In addition, the porous structure was sufficiently

weakened after growth and /or annealing to promote facile transfer of the top layer to alternative substrates. Over 1 cm² InP layers (the entire porous region formed) were successfully transferred onto both flexible PDMS substrates and glass substrates. Finally, fractured porous materials on both sides was shown to be readily removed by chemical mechanical polishing, indicating a pathway for employing the CELT process in a reusable process to mitigate the high costs of InP and other III-V substrates.

The dissertation of Xiaolu Kou is approved.

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2014

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Chapter 1 Introduction

1.1 III-V layer transfer for heterogeneous integration

For the past few decades, layer transfer technologies have attracted wide attention of both academic and industrial groups as the product of the thriving development of semiconductor industry [1-4]. These techniques enable epitaxial device structures fabricated on the growth substrates to be transferred onto final handle substrates w to explore new possibilities in product design. In practice, there are many occasions when substrate substitution becomes an essential necessity, especially for III-V based devices. Owing to their direct bandgap, high carrier mobility and smaller electron effective mass, III-V semiconductors provide advantages over silicon for many applications, ranging from high efficiency photovoltaic devices to high frequency electronics, in particular in optoelectronics [5,6]. For such applications, the substrates often serve as heat sink, window layer, isolation media or mechanical support, so that properties such as high thermal conductivity, optical transparency, electrical insulation and mechanical strength are demanded. In most cases, these specific properties are not available from the growth substrates [7-10], and transferring the devices onto suitable substrates is a feasible solution. In the meanwhile, because of the demand for bio-compatible electronics and portable electronics, flexible and stretchable substrates are also intensively studied as targets for layer transfer [11-13]. More interestingly, when III-V devices are integrated with common substrates such as silicon and glass, it defines the prototype of hybrid circuits to achieve multifunctional system on a single chip [14-16].

Another incentive for the development of layer transfer technology is economics. Conventionally, when the device layer is bonded to the handle substrate, the growth substrate

must be removed either by etching or backside grinding [17-19]. That is to say, to fabricate a device layer only couple microns thick may cost a few hundreds microns substrate material and this wastes expensive III-V materials. Compared to Si, which is an earth abundant element with well-established wafer manufacturing process, the costs of III-V semiconductor wafers are much higher not only because of raw material supply but also the complexity in wafer manufacturing. As a result, despite superior device performance, the marketing of III-V devices is constrained. Fortunately, with layer transfer technologies, the manufacturing cost could be significantly lowered due to substrates reuse after device layer separation. In other words, layer transfer technologies benefit the III-V semiconductor industry in both practical and economical aspects, and have the potential to make an impressive impact on future daily lives.

1.2 Current development of layer transfer technologies

A number of ingenious methods have been developed to achieve layer transfer of thin films. There are two key steps for layer transfer: i) wafer bonding and ii) layer splitting. Wafer bonding can be either fulfilled by adding adhesive layers in between or by direct bonding [20-23]. Depend on the role of the substrates and the ease of processing, different wafer bonding methods can be chosen freely to combine with the subsequent layer splitting step. Among the existing layer splitting techniques, this chapter will cover Epitaxial Lift Off (ELO) [3], “Smart cut” [1], Controlled Spalling Technology (CST) [24] and Cleave Engineered Layer Transfer (CELT) [2,4].

1.2.1 Epitaxial lift off

ELO is a technique that enables releasing an epitaxial thin film from the growth substrate. It takes advantage of the difference in etching rate to conduct highly selective etching of a sacrificial intermediate layer to accomplish the film separation. Figure 1.1 shows an example of

how an $\text{Al}_x\text{Ga}_{1-x}\text{As}$ epitaxial layer is released from the (001) oriented GaAs substrate by dissolving a sacrificial intermediate AlAs layer in dilute HF. The HF etch selectivity of AlAs to $\text{Al}_x\text{Ga}_{1-x}\text{As}$ was measured to be more than 10^7 , with the onset of etching occurring at aluminum composition about 40%-50%. One of the byproduct during etching is hydrogen gas, and because of the difficulty for gas diffusion through the narrow channel between $\text{Al}_x\text{Ga}_{1-x}\text{As}$ and GaAs substrate, the etch may stop once the trapped hydrogen bubbles completely isolate the etch front from the etchant. A modified structure with a tensile strained supporting layer (e.g. Black wax) on top would help to lift up the edges of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ film and increase the etch rate to about 1 mm per hour. However, it still takes more than 24 hours to complete ELO on a 4" wafer [3].

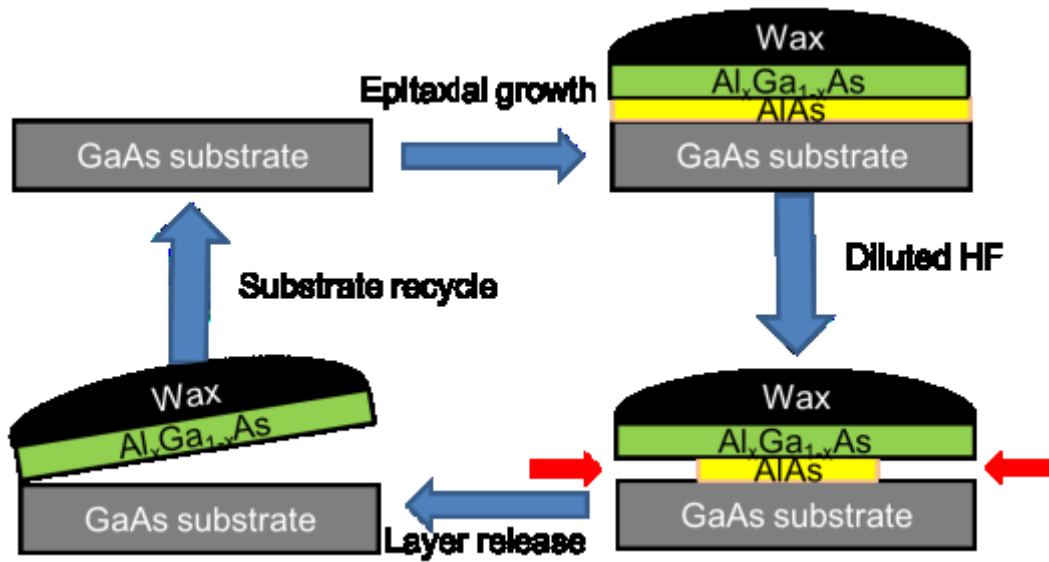


Figure 1.1: Schematic diagram of ELO process to separate an AlGaAs layer from GaAs substrate.

Overall, ELO is a known means to release and transfer high quality III-V thin films. However, the procedure involves handling of dangerous chemicals such as HF and its general usage is restricted by the availability of sacrificial layers with high etch selectivity. More

importantly, even with the modified structure, the etch rate is still unsatisfying and limits its application in large scale layer transfer.

1.2.2 Smart cut

Smart cut was first invented by Brueel of CEA-Leti in 1990s and quickly becomes one of the standard methods to achieve layer transfer in semiconductor society. All kinds of semiconductor materials, including Si, Ge, GaAs, InP etc. have demonstrated successful layer transfer via this ion implantation method [25-28]. The main steps have been illustrated in Figure 1.2. Hydrogen or Helium ions are implanted with calculated energy to mostly reside within a certain depth of the substrate, and these ions will coalesce with each other during the annealing step to form firstly small platelets and then merging into micron-length cracks within the substrate. By further coalescence of these cracks, the substrate will eventually split off and leave the device layer transferred onto the handle substrate.

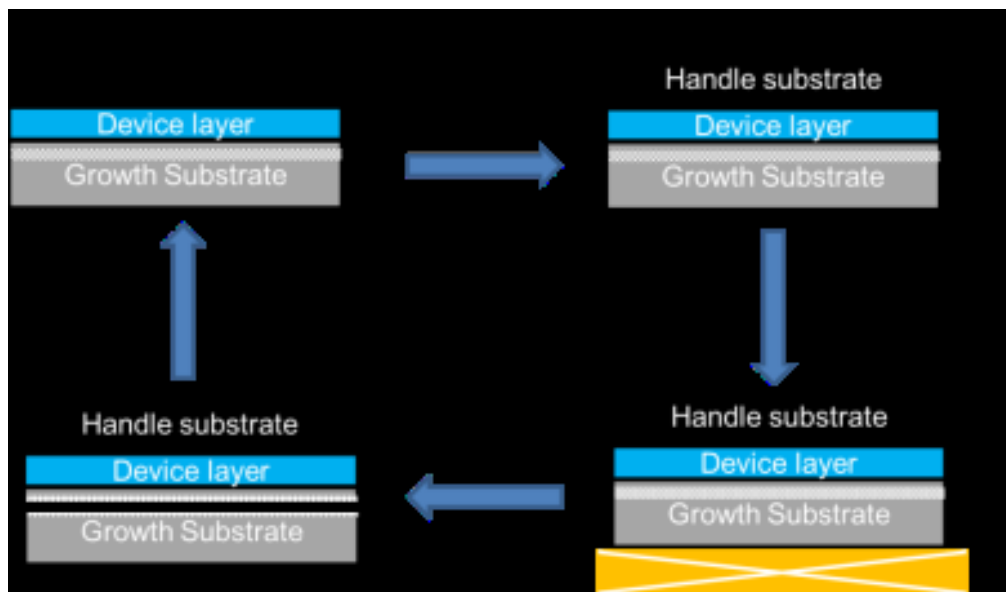


Figure 1.2: Key steps of smart cut process to lift off and transfer the device layer from an ion implanted substrate.

Owing to its high reliability and material independence, Smart Cut has been adopted by a number of groups to fulfill their layer transfer purposes. However, the device layer modification during ion implantation and annealing should not be neglected. Although low temperature processing methods have been studied [29], a tradeoff between transfer efficiency and device quality has been posed for Smart Cut process. Besides, the thickness of the transferred layer is defined by the penetration depth of H^+ ions, which is typically less than 1 μm [30]. However, Lin reported a transferred Si/Ge/Si thin film of 1.5 μm for solar cell fabrication, and achieved 13% efficiency [31].

1.2.3 Controlled Spalling technology (CST)

Layer transfer by spalling in a controlled manner is a quite recent concept introduced by Bedell group in 2012 [24]. Spontaneous substrate spalling happens during the cooling down of a heterogeneous layer deposited at high temperatures, and although it could also be applied to release a thin film from the substrate [32], the high processing temperature and fracture spontaneity set severe restrictions to transfer prefabricated devices. For CST, they engineered the tensile stress into an as-deposited Ni layer using either dc magnetron sputtering or electroplating, so that spalling could happen at room temperature. By modifying the thickness and stress of the stressor layer, fracture of the substrate will only happen when a flexible handle substrate is applied to initiate the fracture from a single point near the edge of the wafer. Figure 1.3 shows the main steps of CST process.

Transfer of up to 4 inch Ge and Si layers have been demonstrated and layer qualities were characterized by the test results of subsequently fabricated solar cells. However, they also noted that there is always some residual stress and slight curvature within the thin film associated with

the spalling process, and handling stressed thin films is still quite a challenge and may compromise the yield of such layer transferring process. Also, due to the polar nature of III-V bonds, unstable fracture with jigsaw surface was found on some spalling results of III-V substrates, such as <100> GaAs.

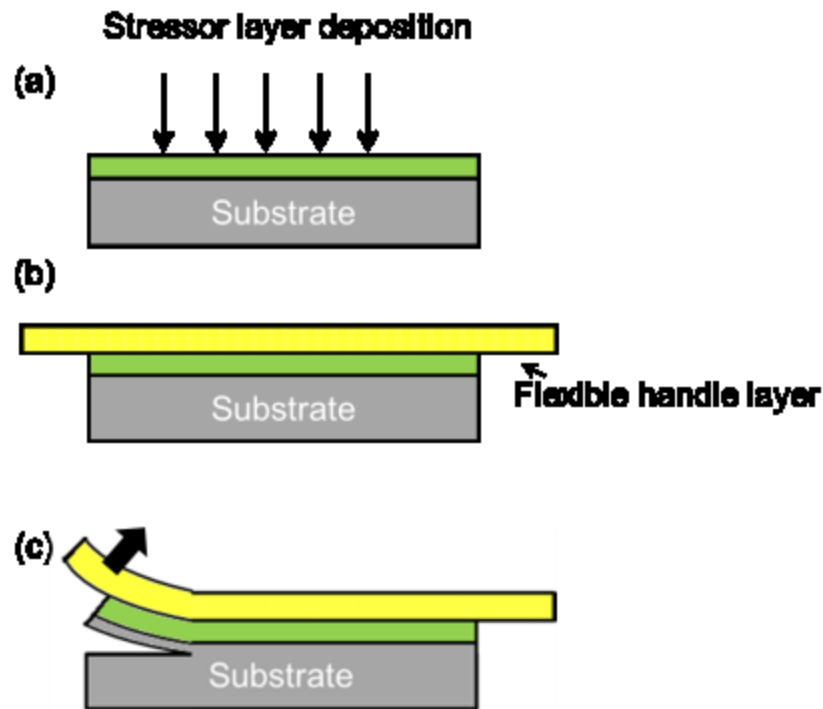


Figure 1.3: Controlled spalling Process. (a) Tensile stressed layer deposition. (b) Flexible handle layer is applied to control the propagation of (c) surface fracture.

1.2.4 Cleave Engineered Layer Transfer (CELT)

Cleave Engineered Layer Transfer focuses on modifying the substrate itself to assist the layer separation process, it appeared to be an improved version of Cleavage of Lateral Epitaxial Films for Transfer (CLEFT) brought up by McClelland etc. in 1980 [2]. More than a decade ago, a Japanese group proposed a method, later known as ELTRAN (Epitaxial Layer TRANSfer), to fabricate high quality SOI (silicon on insulator) wafers [4]. They used a porous layer prepared by

electrochemical etching of Si substrate as epitaxial seed layer to grow defect free Si for SOI structure. The porous layer was later fractured and etched off to achieve SOI structure transferring onto the handle substrate. The entire process is shown in Fig. 1.4. So far, 44.5 μm Silicon solar cell with an efficiency of 16.6% has been successfully made by porous Si layer transfer [33].

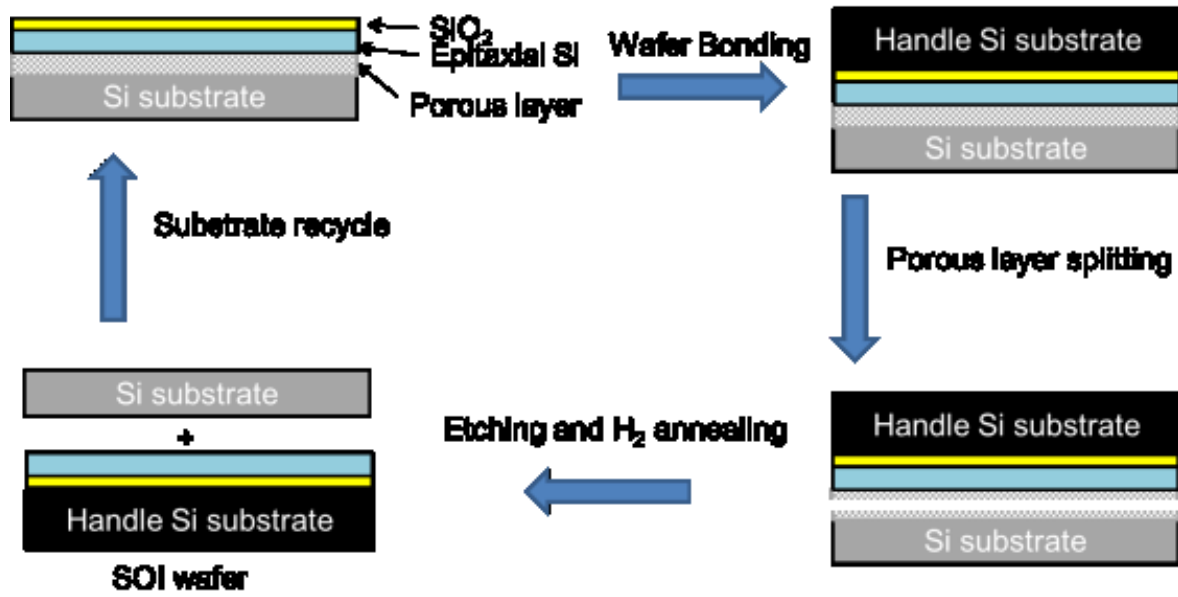


Figure 1.4: ELTRAN (Epitaxial Layer TRANSfer) process to fabricated high quality SOI wafers and Si substrate recycle.

An attempt was made to transfer III-V semiconductors using the similar concept [31]. Instead of growing epitaxial silicon on the porous Si substrate, an ion-implanted InP substrate was wafer bonded to the porous Si substrate to transfer an InP seed layer by smart-cut process. The subsequent steps are similar (not same temps, etc) as ELTRAN and eventually InP based epitaxial structure can be transferred onto handle substrate via porous Si fracture. The use of a non-native Si substrate with the InP (or other III-V) seed layer is less appealing than using a

native substrate for the layer separation; thus the separation of a III-V based device layer from a III-V substrate via a porous layer would be preferable.

1.3 Objectives of this work

The goal of this work is to apply CELT for III-V materials. In other words, the present work aims to demonstrate the ability to transfer III-V thin films onto handle substrates by utilizing some porous structures pre-engineered into the growth substrate which is normally lattice matched to the subsequently deposited epitaxial layer while maintaining the mono crystallinity of the transferred films. In particular, InP is chosen as an representative of all zinc-blende composite semiconductors due to its wide popularity and high wafer cost.

The ultimate process flow for the transfer of an InP-based device layer is shown in Figure 1.5. First, a dual porous layer is prepared on the InP substrate by anodic electrochemical etching. Ideally, the top layer is made denser than the buried layer and its surface will become more coalesced upon appropriate annealing, but this has not been demonstrated for InP or other III-Vs. Second, an epitaxial structure is grown on the porous surface. Metalorganic Chemical Vapour Deposition (MOCVD) is applied in this case. Third, the sample is bonded to an alternative substrate which will offer mechanical support to the epitaxial structures once the InP substrate is removed. Layer separation is achieved through the controlled fracture of the porous region. Finally, fractured porous material is removed by chemical mechanical polishing (CMP) so that the InP substrate will be reused. While this process sounds straightforward, none of the individual steps has been addressed for a III-V process. It is the aim of this thesis to determine the materials issues surrounding the approach to assess whether it is feasible for subsequent device development.

An initial analysis into this process requires some benchmarks that are based on research in other materials (primarily silicon). For example, the target pore size is expected to be in the range of meso- and macro-pore diameters (> 2 nm), thus the morphology of porous structure was intensively examined by scanning electron microscopy (SEM) and the surface roughness was measured using atomic force microscopy (AFM). High resolution X-ray diffraction (HRXRD) and cross section and plan-view transmission electron microscopy (TEM) were employed on as-etched, annealed and epitaxially grown samples to show the feasibility of high device layer growth on porous InP. Other than pore size, porosity is the most important property of a porous material, and relating layer porosity to its mechanical strength will help modifying the etching recipes to prepare porous structures suitable for the controlled fracture step. Thus, the Young's moduli of porous layers measured by nano-indentation tests were obtained as an indication of fracture toughness which cannot be acquired as directly.

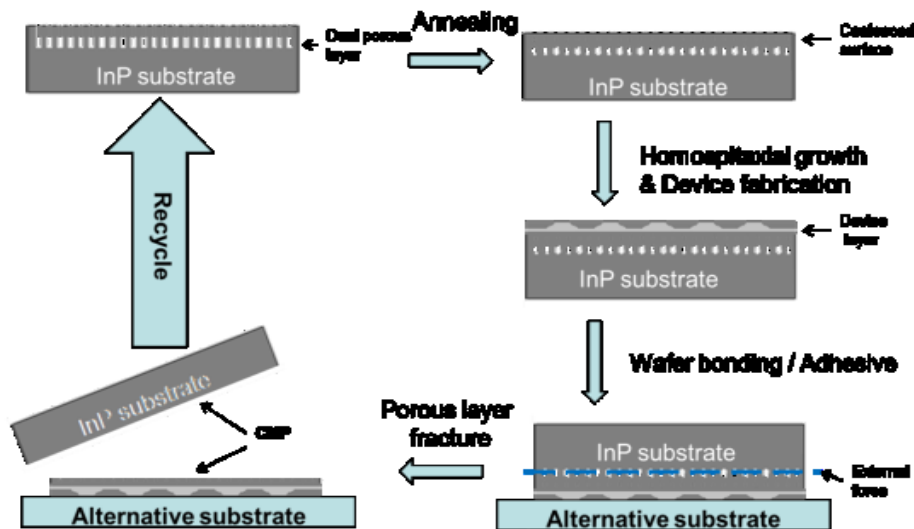


Figure 1.5. Schematic of the proposed device transfer through porous layer fracture.

1.4 Dissertation outline

The motivation of studying layer transfer for III-Vs and the history of layer transfer by other means has been covered in Chapter 1. Chapter 2 reviews the basics of porous formation by electrochemical etching. The first part describes the experimental setups, porous Si features and the mechanism of porous Si formation; the second part emphasizes the difference for III-V materials and how these differences are addressed.

Chapter 3 describes the importance of thermal treatment of porous material. It begins from the reports of porous Si annealing results and the attempted explanations. In addition, the mechanical properties of porous Si and how they change upon annealing are discussed. The second part lists the differences between porous Si annealing and porous III-V annealing and briefly reviews on epitaxial growth on porous III-V substrates.

Chapter 4 elaborates all the experimental details of layer transfer by porous InP. The fabrication of porous InP thin films, the setup for annealing porous InP, the processes for layer transfer demonstrations, and all the characterization techniques applied in this work are all presented in this chapter.

Chapter 5 moves onto the results of porous InP fabrication. The etching results under various etching conditions are shown as well as the dual porosity layer preparation. The relationships between layer porosity and layer properties, such as surface roughness, mechanical strength, strains and crystallinity, are discussed.

Chapter 6 gives the annealing results of porous InP and epitaxial growth on top. It shows how the as-etched porous layer transforms upon different annealing conditions and how these changes can affect the layer fracture process. For the epitaxial growth part, it mainly focuses on

the characterization of the epitaxial layer to assess whether it is of high crystalline quality maintained crystallinity.

Chapter 7 presents demonstrations of InP thin film transferred onto two handle substrates, Polydimethylsiloxane (PDMS) and glass. The importance of the annealing process for the controlled layer fracture is discussed.

Chapter 8 summarizes the dissertation and proposes the future improvements that could lead to practical adoption of this method to fabricate heterogeneous integrated device systems.

Chapter 2 Electrochemical etching and porous semiconductors

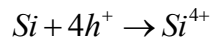
2.1 Porous semiconductor formation and mechanism of electrochemical etching

The basis of porous III-V materials starts with porous Si. Porous Si, which forms near the crystalline Si surface in hydrofluoric acid (HF) due to chemical or electrochemical etching was first discovered by Uhler in 1956 and later discussed in details by Turner in 1958 [35,36]. Originally, it was mainly studied for FIPOS (Full Isolation by Porous Oxidized Silicon) technology for its fast oxidization rate [37]. Later, researchers began to take interest in porous Si since 1990 when strong room temperature photoluminescence was found [38], driven by the expectation to add optical functionality to silicon microelectronic chips. Nowadays, porous silicon has been obtained from both n- and p-type doping, as well as different crystalline orientations with the dimensions and morphologies of these porous films adjustable over a wide range. Many models have been put forward to explain the pore formation mechanism and a few of them are more widely accepted, such as the space charge model, and the current burst model [39-42]. The work on porous Si provides a solid theoretical background for porous III-V formation.

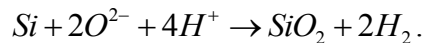
2.1.1 Electrochemical etching

As the hypothesis for this work is that porous III-V properties can be extrapolated from porous silicon, the electrochemical etching of porous silicon is important. The typical solution for porous silicon formation includes HF diluted in either deionized water or ethanol; ethanol has been proved to be an effective surfactant to induce layer homogeneity in both lateral and vertical directions and to promote the removal of the hydrogen bubbles generated as etching byproducts. The general reactions during the porous Si etching are as follows [43, 44]:

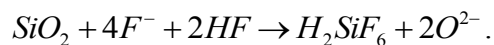
1. Direct dissolution of Si by the injection of holes:



2. Oxidation on the surface with the assistant of holes:



3. Oxide removal by chemical dissolution in HF:



Eventually, the pore wall surfaces are passivated by Si-H bonds. It is obvious that for both n-type and p-type Si wafers, supplying of holes at the silicon / electrolyte interface during the anodic etching is necessary to promote the reaction. In fact, the etching can be performed by either controlling the anodic current (galvanostatic) or potential (potentiostatic), and generally it is preferable to work with the anodic current since it allows more straightforward monitoring of the reaction rate.

There are various designs of the etching cells to prepare porous Si. The simplest one is involves a Teflon beaker (Figure 2.1). The backside of the Si wafer usually has a deposited ohmic metal contact to serve as the anode, and the cathode is generally made of acid resistive metals with good conductivity. While a reference electrode is not always used, it is often adopted in potentiostatic etchings in order to improve the reproducibility [43]. Despite the simplicity of the setup, the potential drop along the silicon wafer leads to inhomogeneity of both the layer thickness and porosity, making it less desirable for research purpose [45].

The second type of etching cell (Figure 2.2) is generally referred as single cell etcher. In this etcher, the exposed etching area is defined by an O-ring seal, and the backside of the wafer is

sometimes deposited with metal contacts, which is crucial for high resistivity wafers to guarantee layer uniformity. This type of etcher is well-received due to its relative simplicity, high layer uniformity and availability to accommodate front-side illumination.

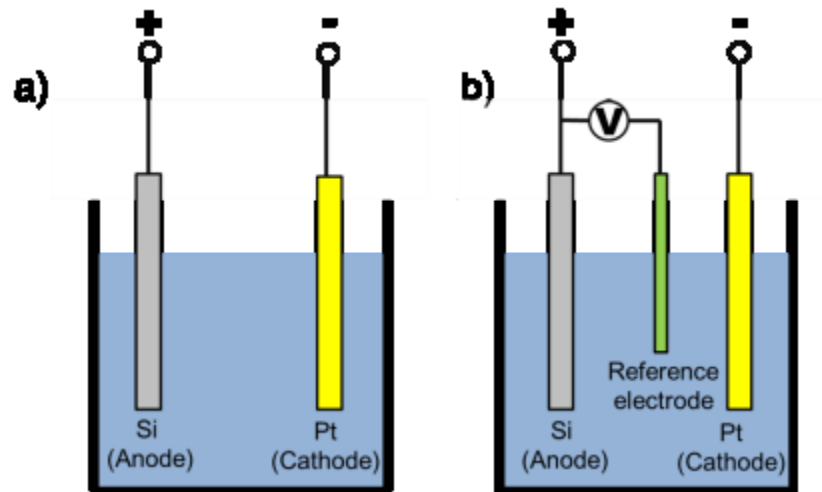


Figure 2.1: Cross-section view of lateral etching cells (a) with and (b) without a reference electrode.

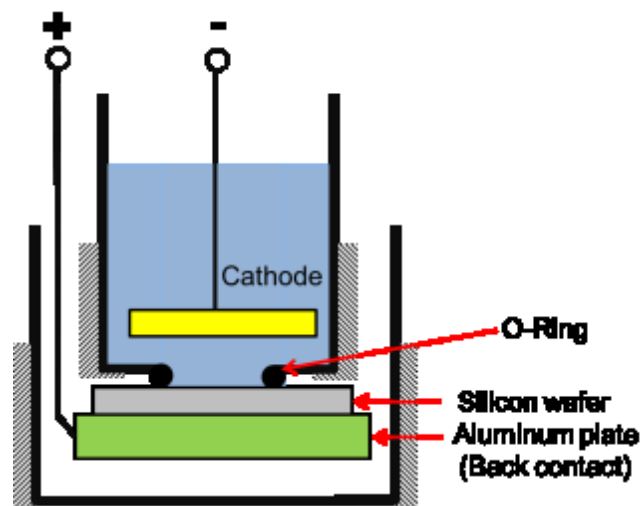


Figure 2.2: Cross-section view of a single cell etcher.

The third type is a double cell etcher (Figure 2.3) and it provides a means to achieve both front and back-side illumination during the etching process and doesn't require any metal contact on the wafer backside. HF circulation is usually added to the double cell etcher. Although stirring doesn't have a major effect on the layer quality, it helps to prevent depth nonuniformity which had been a major drawback when the wafer is placed vertically.

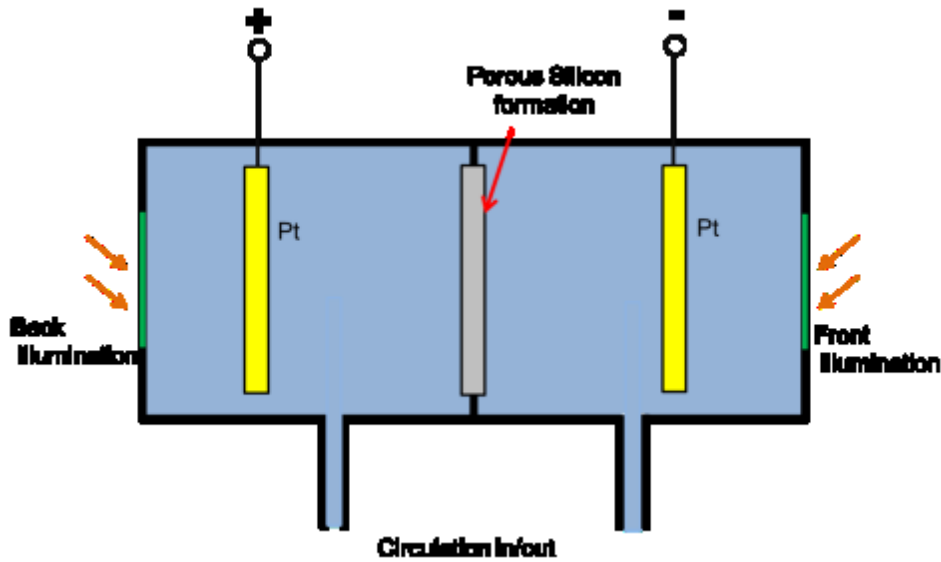


Figure 2.3: Cross-section view of a double cell etcher.

2.1.2 Porous Si

Porous silicon is usually classified by the resulting pore size whether microporous (diameter $\leq 2\text{nm}$), mesoporous ($2\text{ nm} < \text{diameter} \leq 50\text{ nm}$) or macroporous (diameter $> 50\text{ nm}$). N-type porous Si and p-type porous Si also exhibit different properties. Table 2.1 lists the porosity and etch rate due to HF concentration, current density and wafer doping concentration. Generally, an increase in HF concentration leads to a drop in porosity, and it is explained under the assumption that the surfaces are effectively passivated by H^+ ions [46, 47]. Higher current

density always results in higher layer porosity and etch rate, which is more straightforward to understand regarding to the increased hole supply and stronger electrical field, but detailed explanations are a case by case situation mostly dependent on the doping type [48].

Table 2.1: Effects of anodic etching conditions on porous layer formation.

An increase of ... yields a ...	Porosity	Etch rate
HF concentration	Decreases	Decreases
Current density	Increases	Increases
N-type doping conc.	Increases	Increases
P-type doping conc.	Decreases	Increases

To better illustrate the doping effect on the morphology of the porous layer, Figure 2.4 shows four porous Si layers: n- type, n⁺-type, p-type and p⁺-type [49, 50]. For p-type samples (10^{14} - 10^{19}cm^{-3}), when the doping concentration increases, both pore size and pore spacing increase, but remain in the micro- or meso-pores region. For lightly n-type silicon ($<10^{16}\text{cm}^{-3}$) without illumination, the porosity can be very low (1-10%) with the pore size in micrometer range. Higher n-type doping and photon-assisted etching process can eventually achieve macro- or meso-pores, similar to the p-type doped porous structure.

The orientation of Si wafers is typically $\langle 001 \rangle$ so that the etching channels tend to propagate along $\langle 001 \rangle$. According to CBM, porous Si etching starts with a dissolution process, where the surface Si-H bonds are substituted by Si-F bonds. The Si-F bonds cause a weakening of the Si back bonds, which now become prone to be broken by further HF attack. Figure 2.5 shows how the Si surface bonds are arranged on the three most common planes and since the (100) planes present the most sterically favored geometry, etching is fastest for $\{100\}$ surfaces [41, 49, 50].

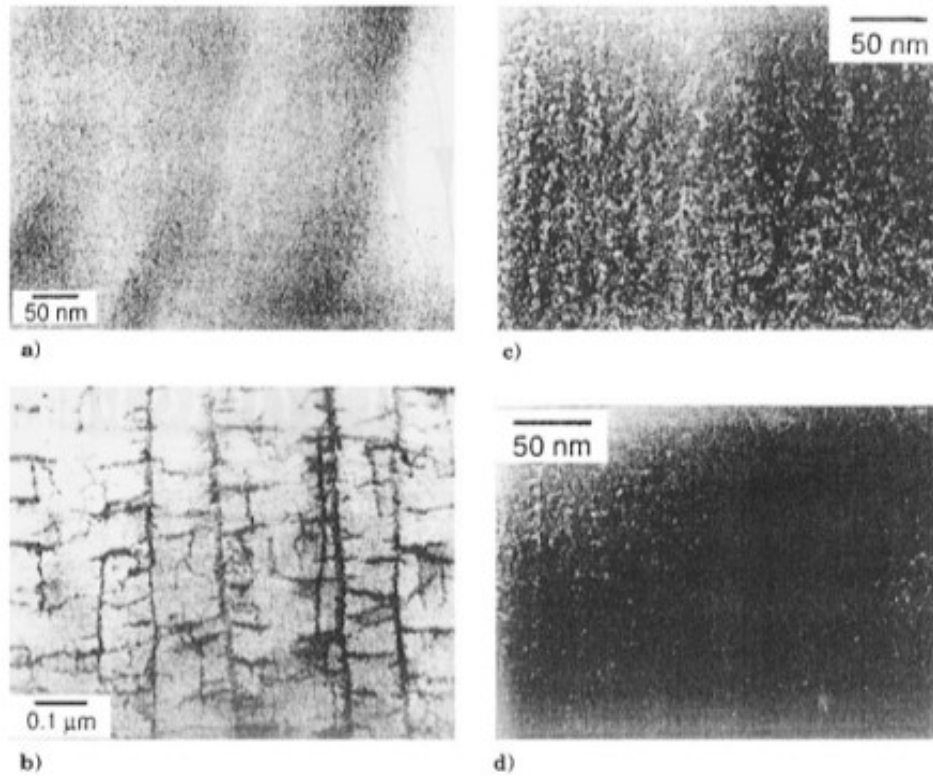


Figure 2.4: Cross-sectional TEM images showing the basic differences in morphology among different types of Si samples: (a) p- type silicon; (b) n-type silicon; (c) p-type silicon; (d) n-type silicon. Ref [50].

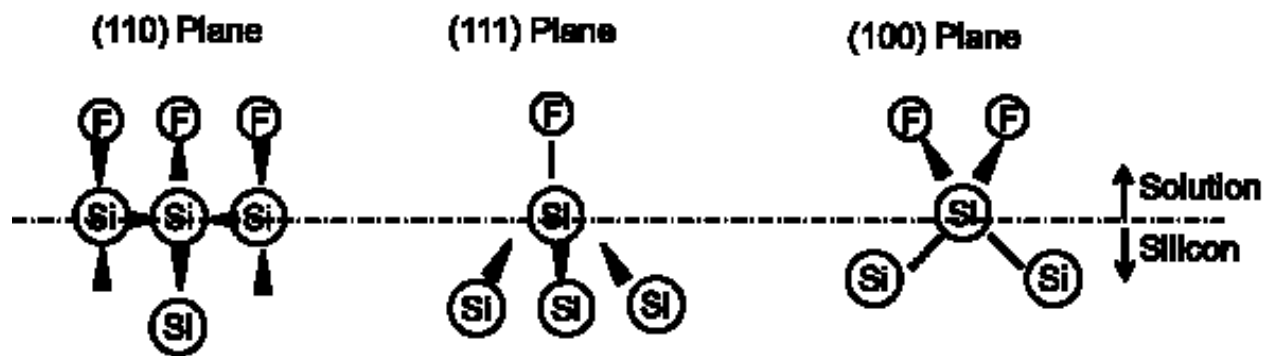


Figure 2.5: Bond orientation for three common crystal planes. Si-F bonds are arbitrarily chosen to represent silicon bonds projecting into solution, although in reality S-H are more

probable. Of all possible crystal planes, only the (100) plane presents two symmetric silicon bonds directed into the solution. Ref [50].

2.1.3 Mechanism of porous layer formation

There are many models proposed to explain the mechanism of porous layer formation [50, 42, 51-53], here will briefly summarize the ones that focus to explain the pore nucleation on the surface and the morphology dependence on the etching conditions, especially for n-type silicon since most III-V etchings are performed on n-type wafers. The discussion in this section is aimed to cover sufficient background to help understand the pore formation in III-V semiconductors.

For pore nucleation, it is generally accepted that pores initiate from defects and irregularities on the silicon surface, and it is consistent with the observations made by Bellin and Zwicker [54] that channels and dislocation networks are often found around defects for n⁻-type silicon. However, even polished samples show porous formation after anodization. The explanation of pore nucleation independent of surface defects was first proposed by Theunissen [42]. They discovered that only above a certain doping concentration could porous silicon result on n-type, defect-free samples, so they claimed that the pore initiation is attributed to the space charge layer breakdown. Unlike p-type silicon, n-type silicon does not have an abundant supply of holes to support the silicon dissolution, so that charge carriers have to be generated either by illumination or avalanche breaking down by strong electric field. When etching is conducted in dark with low current, dissolution still happens slowly due to the thermal generation of charge carriers and results in nano-sized pits on the surface. If the geometry of the pits satisfies the critical radius [55], trenches will propagate due to high electric field at the pore tips. Since every pore tip itself is the source of hole generation, this theory nicely explains the dendrite structure formation on n⁻-type silicon, shown in Figure 2.4(b). Also, when the doping concentration is high,

the space charge region becomes narrow enough to allow tunneling of the charge carriers, so that high density of homogeneously distributed mesopores (typical for p-type porous silicon) are also observed for n^+ -type silicon (Figure 2.4(d)).

The Space Charge Region (SCR) model was first proposed by Lehmann and Föll [40, 41] regarding the major parameters responsible for the morphology of macropores in n-type silicon. The principles of the SCR model are depicted in Figure 2.6. The pore walls are fully depleted of holes due to the space charge region at the solid-electrolyte interface, which makes the etching a self-limited process. The continuing development of the pores is prompted by the localized generation of electron-hole pairs exclusively at the tip of the pores either by backside illumination or space charge layer breaking down.

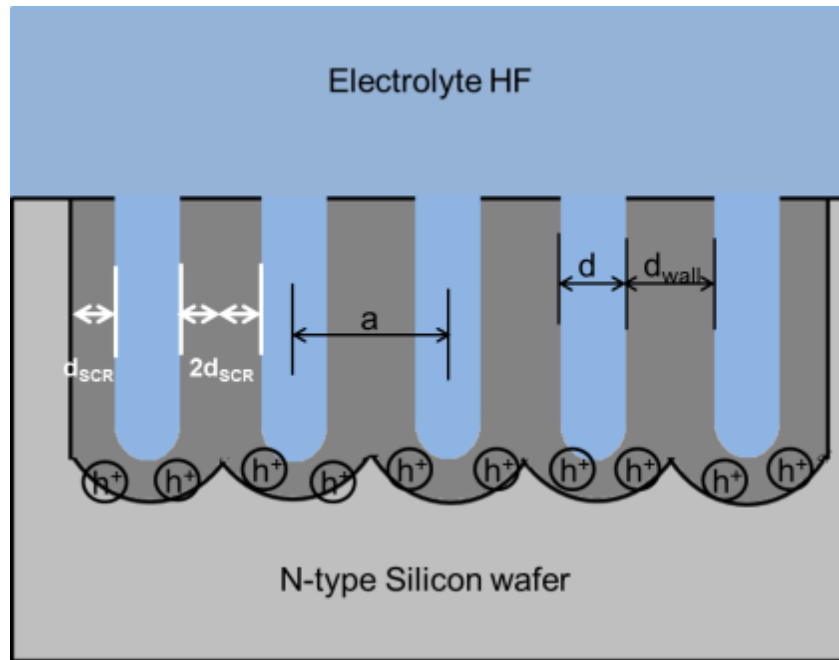


Figure 2.6: Principles of space charge region model. The holes are only available to sustain pore formation at pore tips, either by backside illumination or space charge layer breaking down.

The most important parameters defining the pore morphology are pore size (d) and pore spacing (d_{wall}) for the column shaped porous structure. From Figure 2.6, the thickness of the pore walls is equal to two times of the space charge region thickness, so

$$d_{wall} = 2 \times d_{SCR} = 2 \sqrt{\frac{2\varphi\epsilon}{qN_D}}$$

where φ is the potential drop across the interface, ϵ is dielectric permittivity and N_D is doping concentration of the silicon wafer. Lehmann also proposed a simple formula to relate the pore size with current density,

$$\left(\frac{d}{a}\right)^2 = \frac{j}{j_{PSL}}$$

where a is the center to center distance of two neighboring pores and j_{PSL} is the critical current density, above which electropolishing occurs [56].

However, the SCR model is only suitable to explain n-type porous silicon formation since the hole abundance in p-type silicon is expected to cause complete dissolution of the substrate, while the Current Burst Model (CBM) was developed as a general model for Si and other semiconductors like III-Vs [57]. CBM is built under the assumption that pore walls/tips are passivated by the hydrogen species from the electrolyte, so that the degree and speed of porous layer formation depends on the ability of a given electrolyte to remove the interface states by covering a freshly etched surface with hydrogen. CBM successfully explains the observed current vibration phenomena [39] during electrochemical etching since the two major etching steps, oxide formation and oxide dissolution, cannot occur simultaneously. The assumption of this model is also consistent with the decreased etching rate due to the higher electrolyte

concentration. Moreover, CBM can quantitatively determine the etching rate and prediction of pore morphology [57, 58], but these analyses are not further assessed here.

2.2 Porous III-V semiconductors

Shortly after the discovery of electrochemical etched porous Si, research interest extended to porous III-V semiconductors due to their new and even more interesting properties beyond the bulk materials. The anodization of III-V material has been reported as early as 1972 [59, 60], while significant progress has been made within the recent decades when the optical properties of these porous materials have been explored, largely due to their high aspect ratio and quantum effects [61-63]. Porous III-V formation, although somewhat based on models borrowed from porous Si, differences which account for some unique features must be addressed.

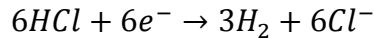
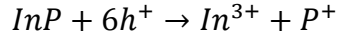
2.2.1 General survey of electrochemical etching of III-Vs

III-V compounds, in general, exhibit the zinc-blende structure, (except nitrides). For zinc-blende structure, the most obvious difference compared to diamond cubic structure is the distinction between group III and group V atoms. For III-V materials like GaAs, InP and GaP, since they are all zinc-blende structure, it is expected to find common features among their electrochemical etching results.

Although porous layer ranging from micro- to macro-pores have been prepared in both n-type and p-type **silicon**, no successfully etching of p-type III-V compounds have been reported to obtain porous material, and the pore size has been limited to only meso- and macro- pores [64]. The experimental observation in III-V etchings appears better matched with the SCR model, since electropolishing, which doesn't occur on p-type silicon, prevails for p-type III-Vs. Also,

the quantitative prediction of the pore diameter and pore wall thickness by SCR is proved on InP porous crystals [65].

For etching, the electrolyte is typically prepared from acids (HCl, H₂SO₄ or H₃PO₄) diluted with water, occasionally KOH is also used. Although for porous Si etching, surfactants like ethanol are routinely added, they are not considered helpful for III-V compounds [64]. Also, the only gas product from porous Si etching is H₂, while it may not be the case for III-Vs. For example, cathodic etching of InP will produce toxic gas PH₃, and since the backside of the wafer basically in the cathodic regime, so that double cell etcher should probably be avoided for safety concerns. Two main components are required in electrolytes suitable for electrochemical etching: nucleophilic species and oxide dissolving species [66]. For example, the anodic etching reaction of porous InP used in this study can be written as



where the holes works as nucleophilic species and the acid works as oxide dissolving species.

As for illumination, although it works well to supply holes for n-type Si, it is not generally recommended for III-V compounds. For back-side illumination, since the diffusion length of the minority carriers in III-Vs is too small to travel from the back-side of the wafer to the etching front, it is completely useless. Front-side illumination is only helpful at the pore nucleation stage [67], and continuing illuminating the front surface will lead to electropolishing due to uniform charge carrier generation. This also implies that, for n-type III-V compounds, the only source of charge carriers is space charge layer breaking down, and it coincides with the

knowledge that only heavily doped (10^{16} - 10^{18} cm⁻³) n-type wafers are suitable for porous formation [68]. The CBM models also apply here when considering the avalanche break down as a cyclical process determined by oxide formation and dissolution.

Porous layer homogeneity is more difficult to achieve for III-V compounds. Unlike Si, these compounds usually contain higher density of crystal defects, and since these defects are sources for electron-hole pair generation under strong electric field, pores are more likely to develop in separate domains [64, 69]. Efforts have been made to enhance nucleation homogeneity, such as damage introduction by ion implantation, surface roughening by HF dip and etch initiation by high current pulse [70- 72]. Interestingly, obtaining a homogenous pore nucleation is relatively easier for InP, so no additional treatments are required [73].

As explained in the previous section, pores in Si grow in <001> direction, however, III-V compounds do not exhibit this property. First, III-V compounds tend to form two totally different porous structure depend on etching conditions, one is called current-line oriented pores and the other is called crystallographically oriented pores. Second, although pore growth does follow a certain direction for the later type, the favored direction is <111>B instead of <001>. The details and explanations of these two types of pores are presented in the following sections. All the aspects discussed above are summarized in Table 2.2.

Table 2.2 The survey of the differences regarding porous formation among GaAs, GaP , InP and Si. Ref [62].

	Si	GaAs	InP	GaP
Structure	Diamond cubic	Zinc-blende	Zinc-blende	Zinc-blende
Doping	n- and p- type 10^{14} - 10^{19} cm ⁻³	n-type 10^{16} - 10^{18} cm ⁻³	n-type 10^{16} - 10^{18} cm ⁻³	n-type 10^{16} - 10^{18} cm ⁻³

Pore size	Micro, meso, macro	Macro	Macro, meso	Macro, mesa
Electrolyte	HF + ethanol	Acid + water	Acid + water	Acid + water
Hole supply	P-type, illumination, breakdown	Breakdown	Breakdown	Breakdown
Homogeneity	Good	Poor	Good	Poor
Growth direction	<001>	<111>B, current-line	<111>B, current-line	<111>B, current-line

2.2.2 Crystallographically oriented pores

To understand the morphology of porous III-Vs, it is important to examine their lattice structure first. Figure 2.7 shows a typical lattice cell of a zinc-blende structure. Similar to the diamond cubic structure, the zincblende crystal consists of two cubic, surface-centered sub-lattices being shifted relative to each other by a translational vector $(1/4, 1/4, 1/4)$. However, since each sub-lattice is occupied by either group III or group V atoms, the zinc-blende structure shows an additional anisotropy compared to diamond structure.

For electrochemical etching of III-V compounds, the pore formation can be considered as a process which continuing dissolves a double atomic layer structure, so that the etch rate is determined by how fast all the bonds of a double layer are broken. The bonds between the double layer structures are arranged in its own way for a certain crystal orientation, which in turn, leads to a distinct dissolution behavior. For silicon, it is reasonable to think the highest density plane will result in the lowest dissolution rate, and it explains why pores never develop along <111> direction. However, in III-V compounds, an additional factor contributing to the anisotropy is

related to different chemical properties of the atoms from group III and group V. The different arrangements on (111) and (100) planes are illustrated in Figure 2.8.

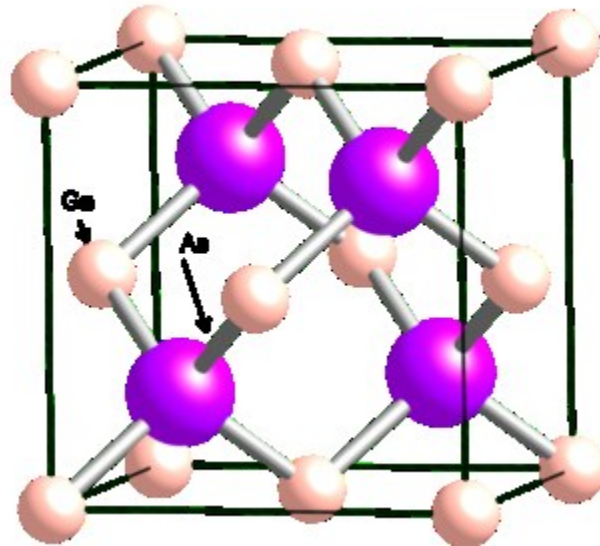


Figure 2.7: Schematic of a typical Zinc-Blende lattice structure.

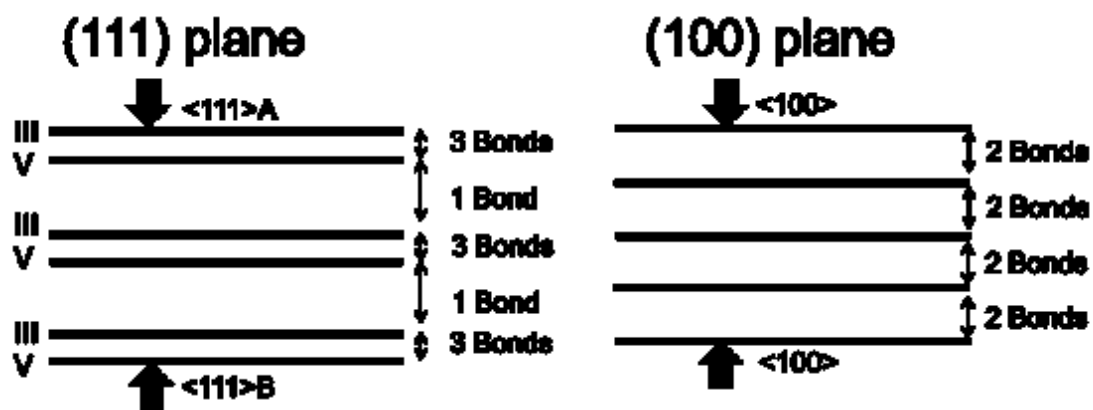


Figure 2.8: The double layer structure: see from (111) planes and (100) planes.

Let's assume the time to free a bonded group III atom is t_1 , and the time to free a bonded group V atom is t_2 . From Figure 2.8, the total time required to remove a double layer along the

$\langle 111 \rangle$ A direction is $3t_1+t_2$, along the $\langle 111 \rangle$ B direction is t_1+3t_2 , and $2t_1+2t_2$ if along the $\langle 100 \rangle$ direction. We know that the electronegativity of group V is higher than group III, so the electronic cloud is polarized towards group V atoms, making it easier to be attacked by the electrolyte species. In other word, t_1 should be longer than t_2 , resulting in the fastest dissolution speed along the $\langle 111 \rangle$ B direction [74].

Because of this, if a $\langle 001 \rangle$ oriented III-V wafer is electrochemically etched, the pores will develop 54° away from the vertical direction; If a $\langle 111 \rangle$ A oriented wafer is etched, 70.5° away; If a $\langle 111 \rangle$ B oriented wafer is etched, the pores will be in the form of “columns” perpendicular to the wafer surface. The differences are summarized in Figure 2.9 [64, 73].

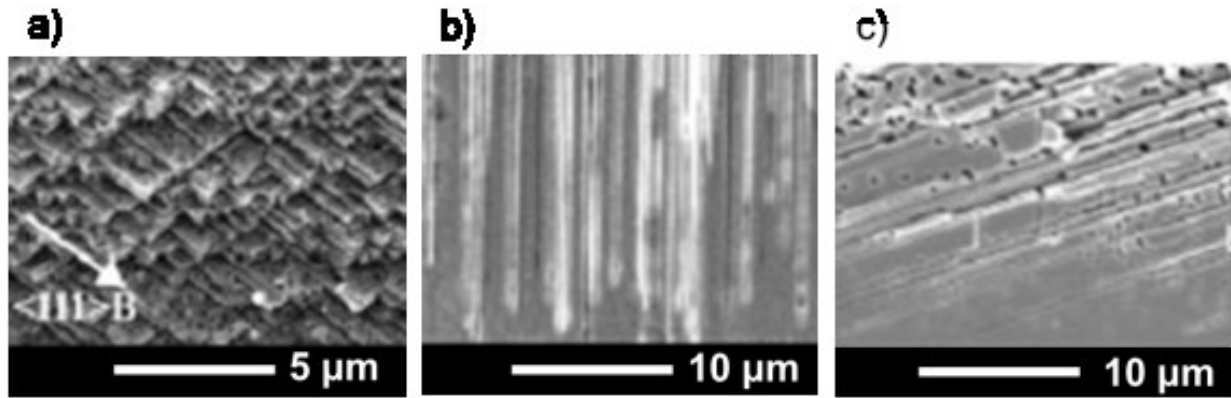


Figure 2.9: The cross-section SEM image of crystallographically oriented pores etched from a) (100) n-InP, b) (111) B n-GaAs and c) (111) A n-GaAs. Ref [64, 73]

Take (001) oriented wafers for example. The 3D architect of crystallographically oriented pores can be speculated from the plan-views on the surface and the cross-section views on the cleavage planes (Figure 2.10). Unlike Si which dissolves isotropically and forms rounded pores in macro-pores regime, the difference in dissolution rate between $\{111\}$ A and $\{111\}$ B facets in III-Vs strongly influences the shaped and growth direction of pores. As shown in Figure 2.10(a),

a pore nucleates from a pyramid-like pit on the surface, which can be obtained after an anodization pulse (1-2 sec). It extends along $\langle 111 \rangle$ direction and be terminated by slow dissolving $\{111\}$ A planes. As the pit grows with further anodization current, it develops two sharp tips along the $\langle 111 \rangle$ B directions, which point from B to A planes along the shortest distance. The small radius of curvature of these sharp tips helps to enhance the electric field to meet the condition for avalanche breakdown and supports continuous etching. The pores formed by this mechanism have triangular shapes, and since they grow in $\langle 111 \rangle$ B direction, the pore walls are $\{112\}$ planes. As a result, the cross-section views shown in Figure 2.10 are evidently different in (110) and $(1\bar{1}0)$ planes: (110) is mainly exposing the channels of the pores, whereas $(1\bar{1}0)$ is exposing the triangular shape of the pores. The schematic representation of pore growth from a nucleation pit is depicted in Figure 2.11.

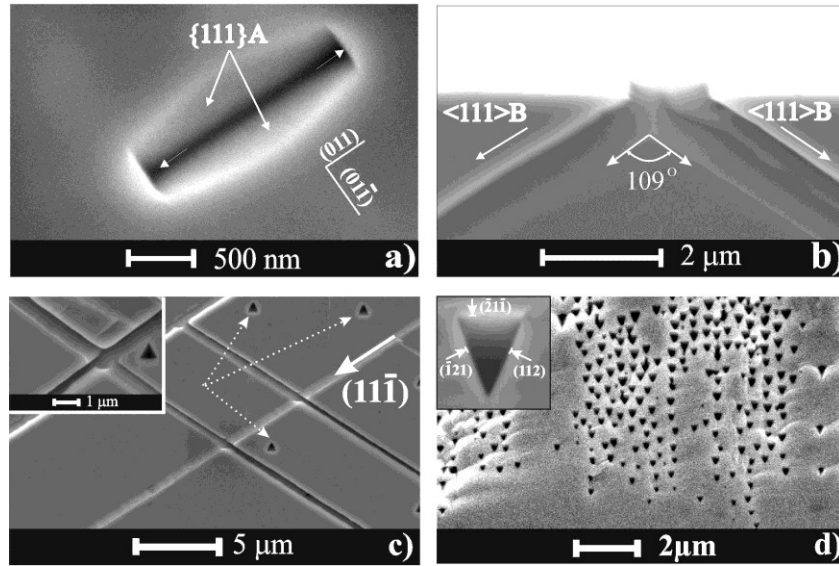


Figure 2.10: Nucleation and growth of crystallographically oriented pores in (100) -oriented GaAs, ($n=10^{17} \text{ cm}^{-3}$), anodized at $j=4 \text{ mA/cm}^2$ in 5 % HCl; a) Plan-view of the pyramid-like cavity stretched along $\langle 111 \rangle$ B direction and terminated by $\{111\}$ A planes; b,c) (110) cross-section view; d) $(1\bar{1}0)$ cross section view. Ref [66].

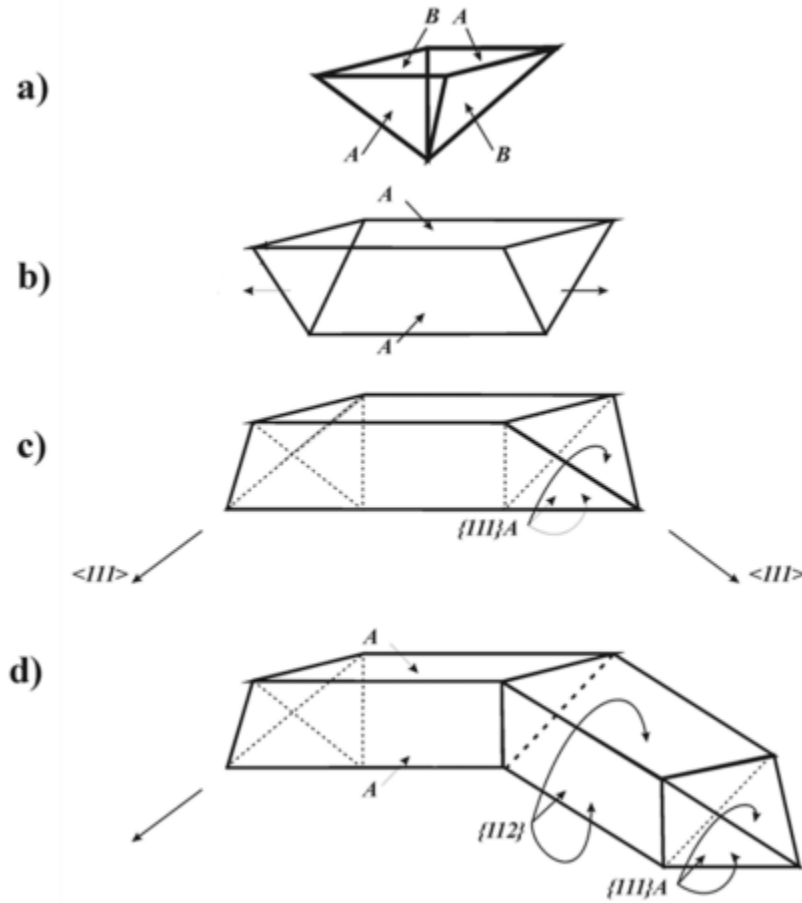


Figure 2.11: A schematic representation of the nucleation of crystallographically oriented pores in III-V compounds. Ref [66].

2.2.3 Current line oriented pores

When a much higher current density or potential is applied, the anisotropic dependence on crystal orientation disappears, and another type of porous structure forms: current-line oriented pores. For current-line oriented pores, the pore always develops along the electrical field, regardless of the wafer orientation. Figure 2.12(a) shows how the pores grow following the direction of current lines, resulting in mostly vertical development and curved features under the O-ring area. Changing current density alone could result in the transition between these two types of pores, as shown in Figure 2.12(b). Besides the orientation difference, the growth rate of

current-line oriented pores is much higher than that of crystallographically oriented pores, up to 15 $\mu\text{m}/\text{min}$. The dimension of such porous structure is a perfect representative of SCR model, where lattice constants between 50-500 nm have been obtained as a function of doping concentration [64].

The favored pore tip growth direction is probably due to the attempt to reduce ohmic losses caused by high current density. According to CBM, pore growth initiates from dissolution process and continues as a result of alternating processes of oxide formation and removal. For crystallographically oriented pores, the strong dependence on crystal orientation is induced by direct dissolution of III-V material. However, if the dissolution via amorphous oxide layer is dominating, such dependence will be compromised, as in the case of current-line oriented pores.

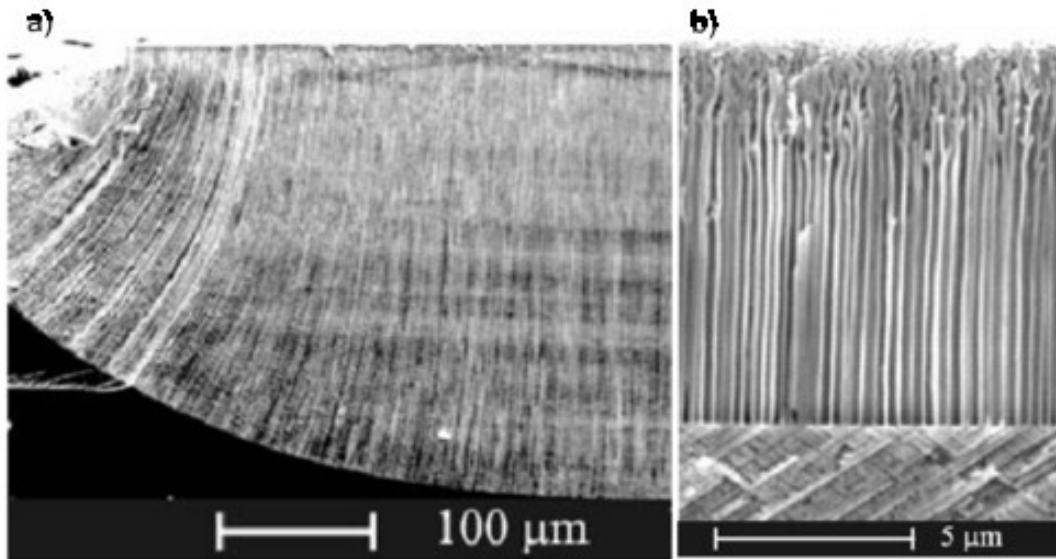


Figure 2.12: The cross-section SEM image of (a) current-line oriented pores and (b) transition between current-line oriented pores and crystallographically oriented pores in n-InP. Ref [75].

Chapter 3 Thermal treatment of the porous structure

3.1 Introduction

As introduced in Chapter 1, an annealing step is typically part of the layer transfer process (Figure 1.5). Due to the high aspect ratio and sharp curvature of the porous structure, its morphology is subject to change via mass diffusion driven by surface energy minimization. Because of this, it is important to assess whether the porous structure evolves significantly during the thermal treatment from epitaxial growth, or even obtain some structural changes which could be beneficial for the subsequent epitaxial growth and layer fracture.

For porous Si, a great deal of work has been done to study its changes under various thermal annealing conditions [76-79]. In contrast, the annealing study of porous III-V is still in its infant stage, so that the knowledge gained from porous Si annealing is important to help predict and understand the annealing results of porous III-V material. Since epitaxial growth involves an annealing process as well, the current status of epitaxial growth on porous III-V substrates will also be discussed in this chapter.

3.2 Porous Si annealing

The study of the microstructure of porous Si and its evolution under thermal treatment helps to fully understand the porous property and explore new application possibilities. One of the pioneering works on porous Si annealing by Herino in 1984 [76] showed that the annealing in high vacuum (10^{-7} Torr) under relatively low temperatures (300 – 900 °C) resulted in enlargement pore size and formation of large cavities of several hundred angstroms, aiming to improve the processing technology of SOI wafers, which the insulator is consisted of oxidized porous Si. More recently, Ott and Müller [77-79] devoted a great deal of effort on porous Si

annealing to promote layer transfer. They studied the annealing effects on both uniform porous structures and dual layer porous structures, and claimed that the changes in morphology, if properly controlled, make beneficial contribution to both the epitaxial growth and the layer fracture processes.

3.2.1 Morphology change of annealed porous Si

There are two major observations after porous Si annealing related to layer transfer technology. One is a void-free thin film formation at the porous layer surface and at the interface between two porous layers. The other is the enlargement of pores, which is more severe in the higher porosity buried layer of the dual layer structure than a monolayer structure. The former change makes the porous surface smooth and pore free, which is ideal for epitaxial growth; the latter change is good for layer fracture with details discussed in 3.2.2.

In Figure 2.4, we see that the pores in p-type Si are in the micro-or meso-pore size domains and they are interconnected by open pore channels. It is found that these pores tend to transform into elongated closed pores after annealing. Figure 3.1 shows what the pores look like after 30 min annealing at 1050 °C in hydrogen atmosphere. Due to different amount of diffusion required to achieve equilibrium states, various features are obtained in layers with different porosity. For the same amount of annealing, in 20% porosity sample, faceted pores showed up while in 30% porosity sample, the majority of pores are spherical. In the samples with 40% and 50% porosity, the pores exist in elongated closed form or still open channels with thicker pore walls. The diffusion is driven by total surface energy reduction, first by forming spherical pores to reduce the total surface area and then by forming facets which have lowest surface energy [80]. The faceted pores are terminated by {100} and {111} facets connected by {110} and {311}

planes. The activation energy for faceting is calculated to be 2.3 ± 0.1 eV [78], which is similar to the activation energy for surface diffusion over steps in silicon (2.3 eV) [81].

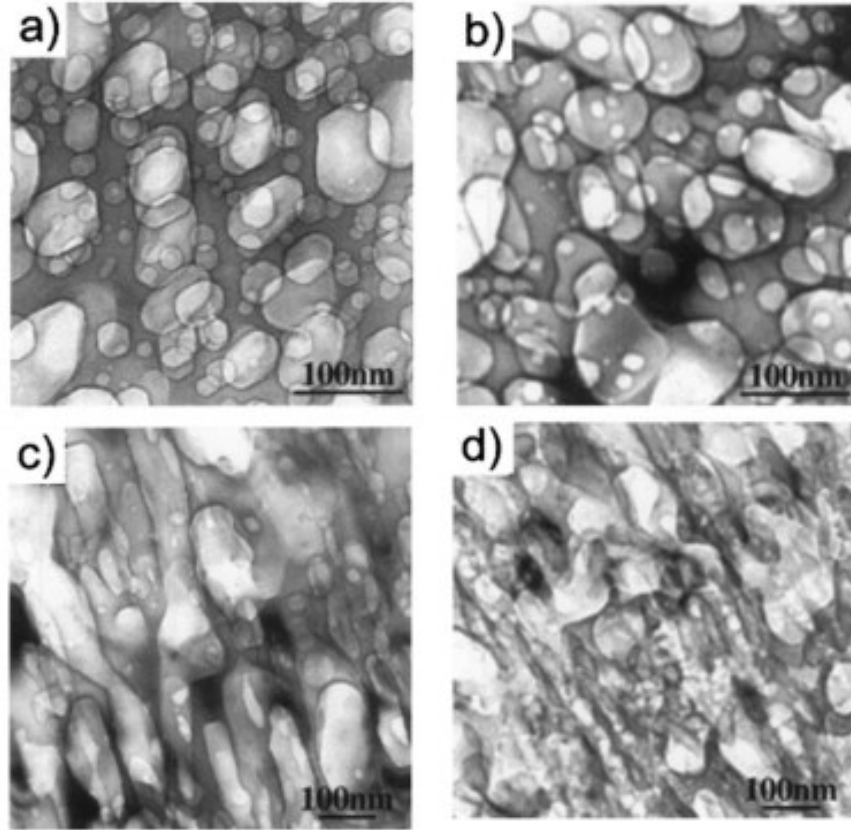


Figure 3.1: .Bright field x-TEM of pore structure of porous silicon monolayers with different porosities after anneal for 30 min at 1015°C. a) 20% porosity, closed, mostly faceted pores, b) 30% porosity, closed spherical pores, c) 40% porosity, elongated pores with some interconnections, and d) 50% porosity, elongated pores with lots of interconnections. Ref [77].

Most interestingly, the annealing often results in a continuous monocrystalline thin film (~ 20 nm), free of pores on the surface of the porous layer (Figure 3.2). To grow an epitaxial layer on the porous Si, Sato reported that the major defects are stacking faults due to the porous features [82]. Fortunately, it was found that raising the H_2 prebake temperature to 1040 °C could

significantly reduce the stacking fault density from over 10^6 cm^{-2} to $10^3\text{-}10^4 \text{ cm}^{-2}$, primarily owing to the surface thin film formation during the H_2 prebake. The thin film is also found between the top and buried layer in the dual layer structures. According to the classical sintering theory, both free surface and high porosity buried layer act as vacancy sinks [83, 84]. The pores near the vacancy sinks dissolve through vacancy diffusion, and resulting in a region free of pores. Also, the smooth surface is a common result of annealing uneven Si surface in hydrogen atmosphere [85].

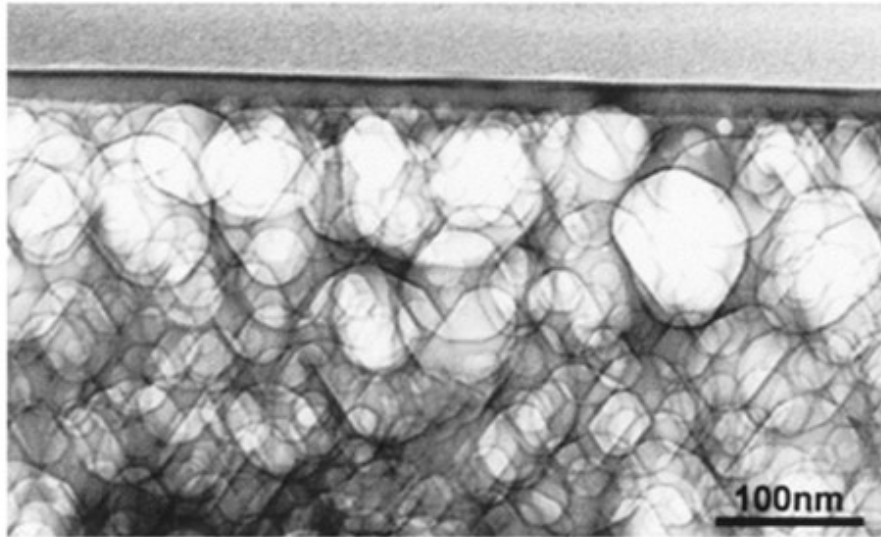


Figure 3.2: .Bright field x-TEM of monocrystalline layer (20 nm) free of pores and crystal defects that has formed at the surface during annealing. Ref [77].

In general, the pore size increases with higher temperature and longer annealing time and layers with different porosity results in morphology change to different extents. Figure 3.3 compares a dual layer structure before and after annealing. The original porosity of the top layer is 20% and, for the buried layer, 40%. A major feature of the annealed sample is the enormous void formation in the buried high porosity layer. Also, it is noteworthy to point out that the

average pore size inside the buried layer appears to be much higher than the 40% porosity monolayer structure under same annealing conditions (Figure 3.1(c)). If the classical sintering theory is applied, the high porosity layer serves as vacancy sinks which are responsible for the formation of monocrystalline thin film between two porous layers. As a result, the porosity of the buried layer increased to approximately 80%, with only a few thin walls supporting the connection between the substrate and the top layer. This transformation inside the buried layer is quite appealing for the layer fracture process. More quantitative analyses are made based on the agreement between experimental results and Monte Carlo simulations of 2D and 3D constructions of thermally activated Si atomic diffusion, and readers can refer to Ref [79] for more details.

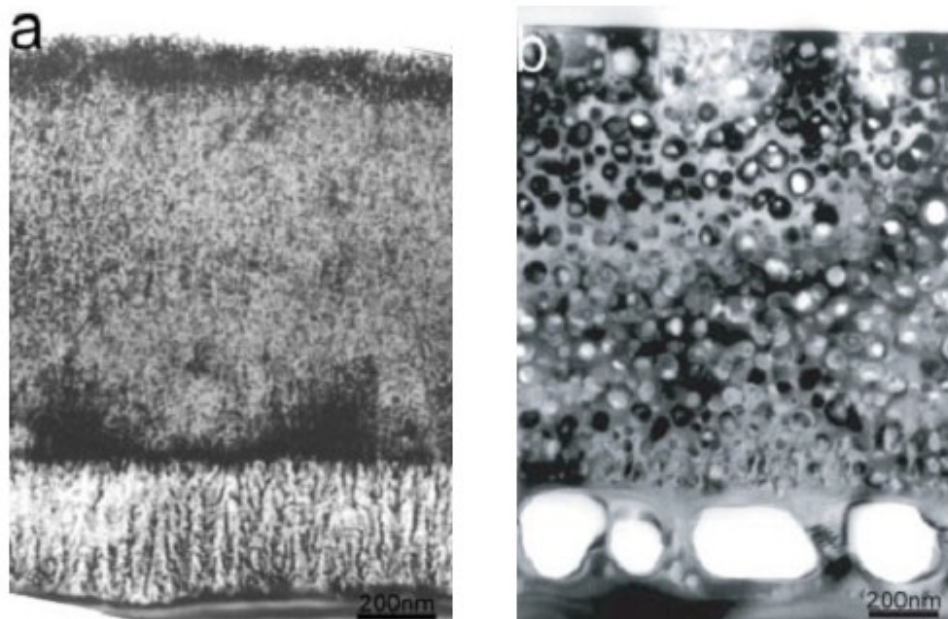


Figure 3.3: Bright field x-TEM of porous silicon double layer with a starting layer (porosity 20%) and a clearly separated separation layer (porosity 40%) before a) and after b) annealing in hydrogen atmosphere for 30 min at 1015 °C. Ref [78].

3.2.2 Mechanical property dependence on porosity and layer fracture

Fracture toughness is a quantitative way of expressing a material's resistance to brittle fracture under tensile stress, and that of the porous layer defines how easy the layer and substrate can be separated for layer transfer [86]. Therefore, it is important to address the dependence of fracture toughness on the porosity.

The Gibson and Ashby model is frequently used to understand the mechanical behavior of porous Si [87, 88]. Since there is no easy way to measure fracture toughness, Young's modulus is normally used to represent the mechanical strength. As suggested by Oliver and Pharr, the Young's modulus of porous Si can be directly measured by nanoindentation [89], using the expression

$$E_p = \left(\frac{1 - \nu^2}{2} \right) S \sqrt{\frac{\pi}{A}},$$

where ν is the Poisson ratio of porous silicon, S is the slope of the unloading curve of the force-displacement data, and A is the projected area of the indenter at maximum load. Bellet measured

the Young's modulus of porous Si layers with porosities ranging between 36% to 90%, and found a good agreement between the experimental data and the predicted value using the open cell model proposed by Gibson and Ashby [88] (Figure 3.4). According to the open cell model, the Young's modulus E_p can be calculated by $A(1-p)^2$, where p is the porosity of the layer and A

is a constant equals to the Young's modulus of bulk material, which is 120 GPa for Si.

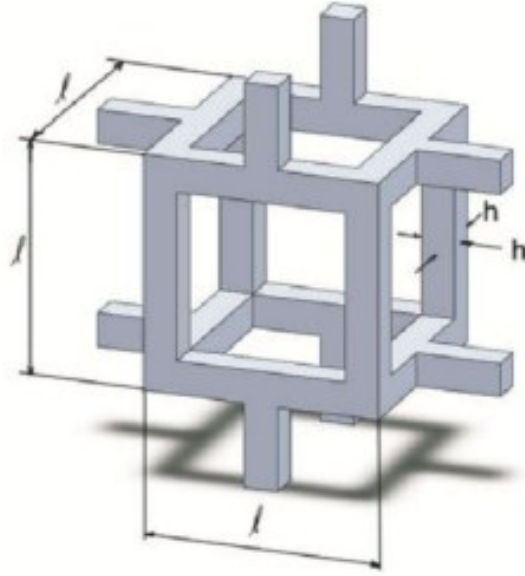


Figure 3.4: The open cell model of porous material. Ref [84].

The same model is used to calculate fracture toughness K_{Ic} of porous Si. As proposed by Ashby, the expression for fracture toughness is

$$K_{Ic} = C(1 - p)^{\frac{3}{2}} \sigma_{fs} \sqrt{\pi l},$$

where σ_{fs} is the ultimate tensile strength when the edges start to fail, l is the cell size labeled in Figure 3.4, and C is a constant. C is empirically determined to be 0.65 for various porous materials [90- 92]. ***It is obvious that porosity is one of the most important parameter to determine the fracture toughness: higher porosity means lower Young's modulus, as well as lower fracture toughness.***

However, as discussed in 3.2.1, once the porous Si is annealed, the morphology undergoes dramatic changes. Unlike interconnected pores in as-etched porous Si, the appearance of closed pores in the annealed samples means the usage of open cell model is no longer appropriate. So far, there are no data on the mechanical properties of the annealed porous Si [93], so that the quantitative comparison of the mechanical strength of porous layer before and after annealing cannot be made. Empirically, the

annealed samples with closed pores show more facile fracture results during layer transfer process, while as-etched samples often result in wafer de-bonding or substrate breakage [94, 95]. The observed porosity change from 40 % to 90 % in the buried porous layer definitely contributes to the ease of fracture of the latter sample, while more work needs to be done to understand the reasons for fracture other than porosity change.

3.3 Porous III-Vs

3.3.1 Annealing of porous III-Vs

Although considerable research is related to the fabrication of porous III-V materials, much less attention has been paid to their annealing effects. It has been learned from porous Si that annealing induces a significant morphology change at temperatures much lower than the melting temperature (1412 °C), and the major driven force for mass transport is surface energy reduction. Similarly for porous III-Vs, the high aspect ratio and sharp edges make them also susceptible to morphology changes upon annealing, leading to a reduction in the total surface energy. For example, Grym found that the crystallographically oriented pores in electrochemical etched GaAs substrate changed shape after epitaxial layer overgrowth [96]. The original hexagonal cross-section pores acquired a more rounded shaped after 400 nm of InGaAs overgrown at 560 °C with a 10 min substrate treatment at 600 °C under AsH₃ flow, and even became hollow cavities under a higher temperature treatment at 700 °C. The mass transportation during annealing has also been observed in porous InP [97]. It was reported that both current-line oriented pores and crystallographically oriented pores transformed into hollow cavities after annealing at 640 °C for 30 min in hydrogen atmosphere with phosphorus overpressure, and they claimed that the transportation mechanism is connected with Ostwald ripening. However, in neither of those cases, were the mechanical properties of the porous III-V materials assessed.

There are several differences in annealing porous III-Vs that are noteworthy. Since III-Vs are compound materials, it is important to preserve their stoichiometry during annealing, especially when group V atoms are known to be more volatile. Generally, the As or P overpressure is required when annealing GaAs or InP wafers over 400 °C [98, 99], and the critical temperature may be even lower for rough surfaces and porous structures. In addition, an N₂ or H₂ purge is usually adopted to avoid oxidation. Also, the melting temperatures of InP (1062 °C) and GaAs (1238 °C) are lower than Si, so lower annealing temperatures might be expected to induce similar morphology change in porous InP and GaAs. As for the annealing results, since only meso- or macro pores exist, complete surface coalescence – which is observed in micro-porous Si – may not be possible for porous III-Vs. The unique crystallographic orientation of III-V pores compared to the silicon pores could also lead to differences during annealing.

3.3.2 Epitaxial growth on porous III-V surface

Although there has been a lack of study on the annealing phenomena of porous III-V substrate, the idea to grow epitaxial layer on porous substrate is not new. It was first brought up by Luryi and Suhir to grow Si_xGe_{1-x} on silicon substrate [100] and later formulated by Zubia and Hersee [101] in the theory of “nanoheteroepitaxy” in 1988 to discuss the advantages of growing a hetero-epitaxial layer on nano-porous (10-100 nm) surfaces to reduce dislocation densities induced by lattice mismatch. According to nanoheteroepitaxy, the epitaxial layer first nucleates as an array of isolated islands on the porous surface, and later coalesces into a continuous layer through lateral growth after a sufficient layer thickness is grown. Unlike the conventional planar growth which the epilayer can only deform vertically to accommodate mismatch stress, the porous layer and the island structure allows deformation to occur in both vertical and lateral

directions to distribute the mismatch strain. As a result, it was theorized that the epitaxial layer can remain coherent beyond the critical thickness and has much lower dislocation defect density. However, due to the relative high surface roughness and discontinuity of the starting surface, the pore size is critical to the surface planarity of the epitaxial layer since the distance between the isolated nucleates must small enough to be compensated by subsequent lateral growth.

The growth of epitaxial layers on porous III-V substrates due to the demand for more sophisticated and powerful device applications has produced successful preliminary results [97, 102-105]. However, further investigations are necessary due to the lack of characterization on the epitaxial layer crystallinity and defect density, which are crucial to demonstrate the suitability of epitaxial growth on porous substrates for III-V layer transfer.

Chapter 4 Experimental methods

4.1 Porous InP etching

A Teflon etcher was used for the electrochemical etching of porous InP. The design (Figure 4.1) is very similar to the single cell etcher introduced in Chapter 2, so no need to worry about the toxic PH_3 gas formation on the cathode side, and the layers are of uniform thickness without stirring. The etcher can accommodate 100 mm diameter wafers, but most of the etch experiments were performed with an O-ring sealed aperture inserted between the wafer and the electrolyte to optimize material utilization. The cathode is made of Au plated mesh to evenly distribute the electric field over the etching area. The gap between the cathode and wafer surface is about 5 mm. The backside of the wafer is in contact with an aluminum foil wrapped 4" Si wafer which is supported by an array of metal springs standing on the anode pad. The springs help to secure the O-ring seal. The backside of the InP wafer was originally deposited with an ohmic contact Au/Ni/AuGe, but subsequently, it was determined that the metallization step was unnecessary for good electrical contact.

A DC power supply in constant current mode was used. With a 0.65" diameter O-ring, the effective etching area is about 2 cm^2 , so a current ranging between 6 mA and 0.4 A corresponded to a current density of 3 mA/cm^2 and 200 mA/cm^2 . The electrolyte was prepared from concentrated HCl (37%) diluted by DI water. The diluted HCl concentration differed from 2 v/v % to 40 v/v %.

(001) oriented, n-type sulfur doped ($3\text{-}8 \times 10^{18} \text{ cm}^{-3}$) InP wafers were used in this study. No surface cleaning was used before etching for as-received wafers, and simple solvent rinse was used on the wafers if they had been exposed to the clean room environment multiple times.

All the etchings were performed under normal lighting conditions, so the effect of photon generated charge carriers is negligible. The most important variables controlling the layer properties during electrochemical etching are current density, electrolyte concentration, and etching time. A few second to a few minutes etching time were required to form a porous layer thickness on the order of a few μm . After the etch, the porous layers were rinsed sequentially with isopropyl alcohol (IPA) and DI water for several minutes to eliminate any HCl in the porous structure, followed with N_2 dry. If two different HCl solutions were used for the double layer etching, a cleaning and drying step was also performed after the top layer formation.

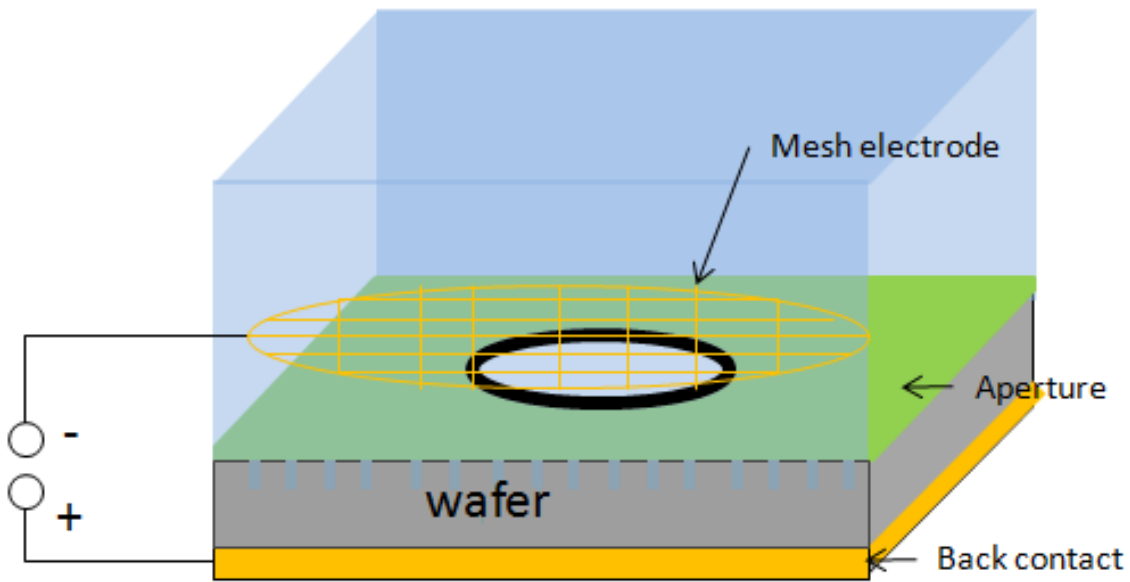


Figure 4.1: Schematic drawing of electrochemical etching system.

4.2 Porous InP annealing and layer deposition

Three parameters were varied for thermal annealing of porous InP wafers: annealing temperature, annealing environment and annealing time.

The epitaxial growth temperature for InP is between 550 °C and 650 °C, depending on the growth system. Also, based on the literature studies of porous Si, an annealing temperature of 1015 °C was shown to be important for annealing. As an initial comparison, given that the melting temperature of Si is 1685 K and InP is 1335 K, the equivalent temperature for InP annealing should be 1028 K, which is about 750 °C.

A hot plate provides a straightforward means to anneal at relatively low temperatures (≤ 450 °C) in ambient. The phosphorus loss can be compensated by placing another InP wafer on the porous layer. The temperature fluctuation is less than ± 3 °C on the hot plate. The samples were placed on the hot plate at 450 °C, and cooled to room temperature after annealing.

In order to avoid oxidation during annealing, an N₂ purged chamber was also used. Still, InP cap wafers were employed to maintain layer stoichiometry. The temperature was monitored by a thermal couple when the annealing temperature was lower than 650 °C. Otherwise, an in situ pyrometer was used. Two banks of tungsten-halogen lamps inside the chamber could quickly (~ 30 °C/sec) ramp the temperature to the pre-programmed annealing temperature, and cooling was achieved by the continuous flow of N₂ and the cooling water system. Temperatures between 500 °C and 750 °C were assessed using samples with different porosities. Most of the annealing tests of dual layer structure were done in the N₂ purged chamber.

To deposit the epitaxial layer on porous InP, the samples were transferred into a metalorganic chemical vapor deposition (MOCVD) chamber. The growth temperature for InP is 650 °C and a 2 micron thick layer was grown (approximately 30 min). One subset of the wafers was used for epitaxial growth so that both tertiarybutylphosphine (TBP) and trimethylindium

(TMIn) precursors were carried by H_2 into the chamber for layer growth [106]. The other subset was annealed under the same thermal budget with TBP in H_2 .

4.3 Porous layer transfer

One transfer method used polydimethylsiloxane (PDMS) as host substrates for the transferred thin films. Only annealed samples with double layer structure were used for transfer purpose. The PDMS substrates were made from Sylgard 184 silicone elastomer manufactured by Dow Corning. To start, the elastomer base and curing agent were mixed with the weight ratio 10 to 1. A 2-5 mm thick PDMS layer was produced. Then, the film was placed into a vacuum bell jar for 30 min to eliminate gas bubbles in the PDMS before the cure at 75 °C. It was found that after about 15 min on the hotplate, the surface of the PDMS substrate is rather sticky and the bulk substrate is solid enough to withstand the weight of InP pieces, so the bonding is performed at this point by gently putting the InP piece onto the curing PDMS surface. Depending on the layer thickness, 30 min to 2 hours are required to completely cure the substrate.

Once the curing was finished, the flexible PDMS substrate was peeled from the InP sample, and the high porosity buried layer would fracture and transfer from the substrate to the PDMS. Figure 4.2 shows schematically the process flow of this layer transfer method.

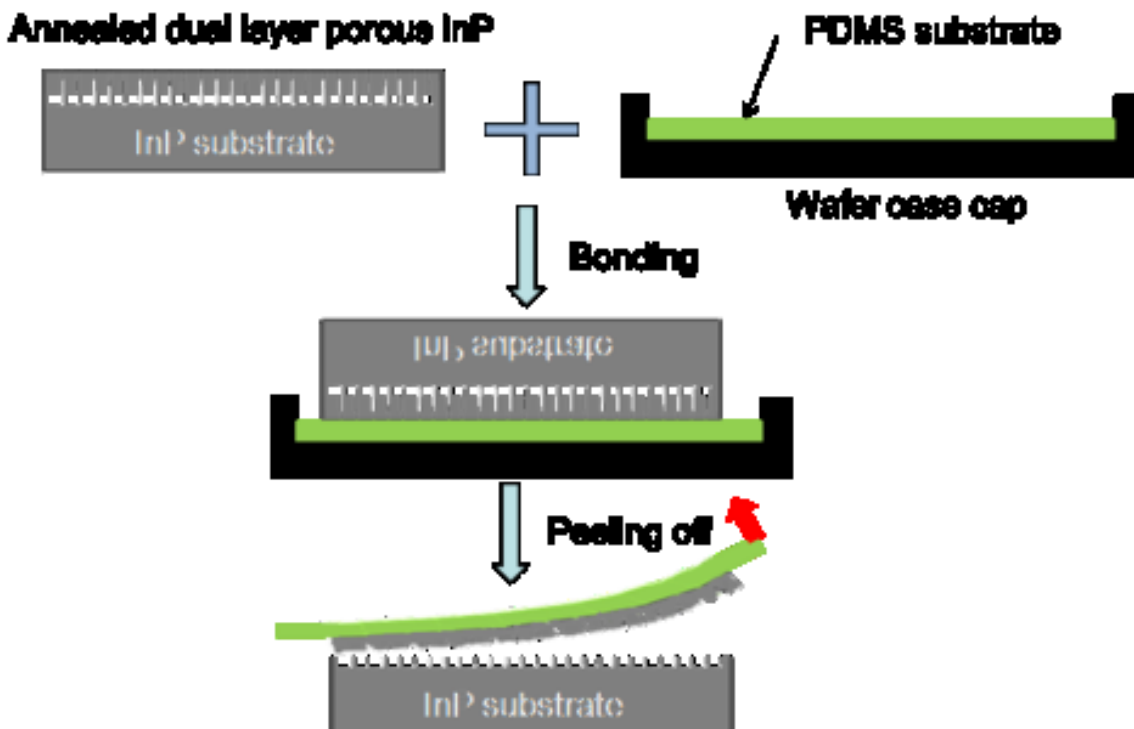


Figure 4.2: Schematic drawing of the layer transfer process onto PDMS substrate.

A second method used epoxy glue as the bonding agent between the InP samples and glass slides. Both as-etched and annealed samples with double layer structure were used in this method. Figure 4.3 illustrates the structure of the bonded sample and how the layer transfer is induced. Before bonding the InP sample to a glass slide, a 100 nm SiN layer was deposited by plasma enhanced chemical vapor deposition (PECVD). The SiN layer was used to prevent penetration of epoxy glue into the porous layer. In addition, it adds a yellowish color to the transferred layer whenever it is too thin to be seen.

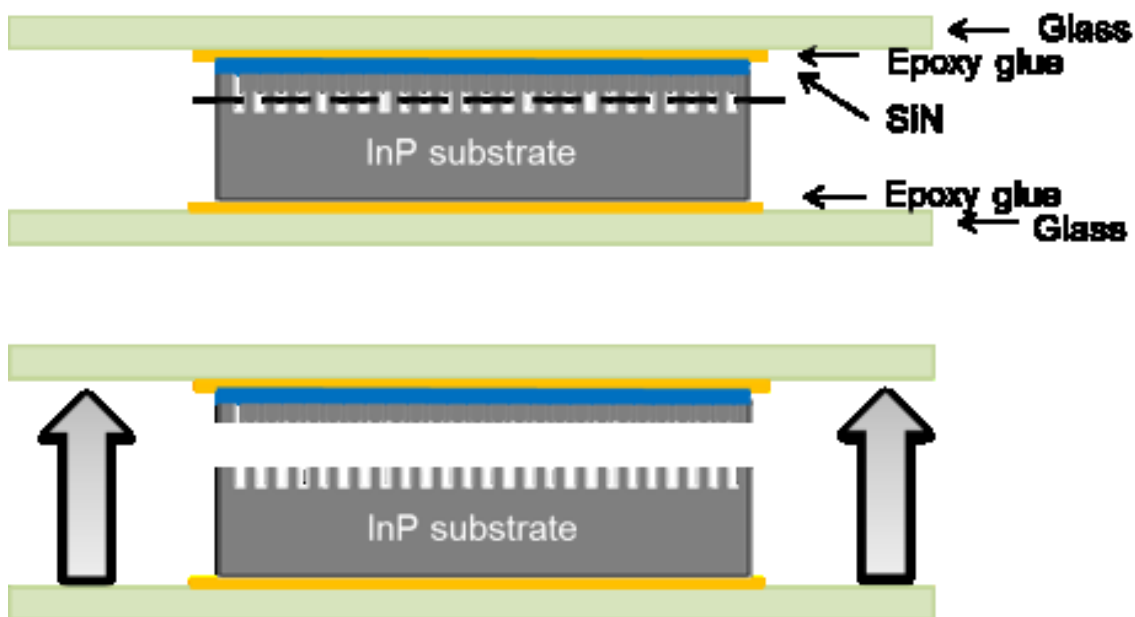


Figure 4.3: Schematic description of the layer transfer process onto glass slides.

The porous materials on both sides after layer splitting were removed by chemical mechanical polishing (CMP). In order to obtain a surface roughness lower than 10 Å with minimum material loss, abrasive free CMP with only citric acid and sodium hypochlorite (NaOCl) was used [107, 108], since standard polishing processes are too aggressive and remove material at rates on the order of microns per minute. Mixture of NaOCl and citric acid works as the oxidizer, the corrosive inhibitor, and etchant. By creating an oxide layer on the InP surface, it first protect the surface from chemical attack and can later be removed by the polishing process to expose the InP again. For a rough surface consists of hills and valleys, due to fast material removal rate on the hills, the surface can be smoothed by continuously reducing the height difference between hills and valleys, and the smoothing rate is determined by the chemical composition, the rotation speed of the pad, the pressure applied and the pad surface. A Logitech PM5 CMP tool was used. The solutions were 5 v/v% NaOCl and 25 v/v% citric acid, both

diluted with water. The polishing pad was a polyurethane pad and the rotation speed was kept at 30 RPM. Pressure was set at 8kPa at first to quickly remove the majority of porous material and lowered to 4 kPa for surface smoothing. The removal rate at 4 kPa is about 5 nm per min.

4.4 Characterization methods

Various characterization methods were employed in this study, including scanning electron microscopy (SEM), transmission electron microscopy (TEM), high resolution X-ray diffraction (HRXRD), nanoindentation, atomic force microscopy (AFM), etc.

4.4.1 Layer morphology characterization

The most frequently used technique is SEM. It was applied to check the morphology of porous layers in both plan-view and cross-section view. For crystallographically oriented pores, the cross-section views include both (110) and ($1\bar{1}0$) cleavage planes. All the images were taken in the high-resolution mode (immersion mode) at 30 kV. Energy-dispersive X-ray spectroscopy (EDX) is part of the SEM, so composition analyses were also performed after porous layer formation and annealing. According to the Kanaya-Okayama equation [109], the penetration depth of the electron beam at 30 keV is a few microns, about the thickness of the porous layer, so that EDX provided an accurate quantification of the layer composition. By assuming the porosity is uniform throughout the entire layer, the porosity is determined by the ratio between pore area and solid area on 2D plan-view images of the surface.

The surface roughness was determined by AFM. A Quesant Q250 microscope was used in tapping mode, with a resolution less than 0.1 nm. The scan size ranged from $40 \times 40 \mu\text{m}^2$ to $50 \times 50 \text{ nm}^2$, and the root-mean-square (RMS) roughness of each scan was recorded for quantitative comparison.

4.4.2 X-ray diffraction

X-ray diffraction (XRD), as a non-destructive characterization method, is widely applied to determine lattice structure of crystalline samples. Two diffraction techniques are discussed in this section: HRXRD and X-ray topography. HRXRD is mainly used to check the crystallinity of the porous layer and the in-plane and out-of-plane strain within the layer, and X-ray topography is a powerful tool to map the micro strain inside wafers.

A schematic drawing of a Bede D³ high-resolution diffractometer used for HRXRD is shown in Figure 4.4. X-ray radiation is generated from a copper target excited by an electron beam accelerated at 40 kV. The filament current is 30 mA.

HRXRD encompasses triple axis diffraction (TAD) because it consists of three sets of diffracting crystals. The first axis is composed of two beam conditioning crystals. In this case, a two-bounce channel-cut (111) Si collimator and a (111) Si monochromator in a (+, -, -) configuration. The outgoing X-ray beam from the first axis is a highly collimated monochromatic radiation of Cu-K α_1 with the wavelength 1.5406 Å. Next, it is directed to the second axis, the sample. The sample stage rotates or translates in six directions, and the most important one is ω , which corresponds to the angle between X-ray incident beam and sample surface. The third axis consists of a detector and a third crystal which is a four-bounce (220) channel-cut Si crystal. By placing this third crystal in front of the detector, high angular resolution is achieved due to the narrowed acceptance angle.

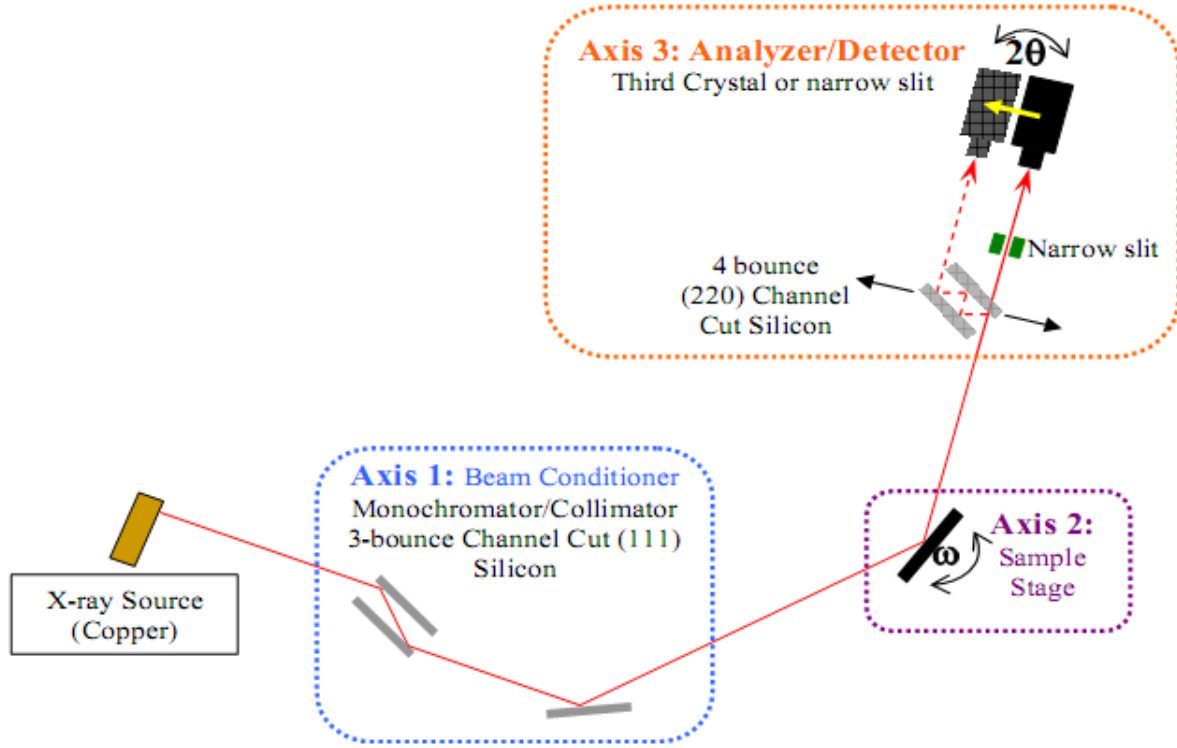


Figure 4.4: Schematic of Bede D3 X-ray diffractometer.

To interpret XRD data, first, it is important to appreciate reciprocal space. As in Figure 4.5, a 2D reciprocal space of a zinc blende structure is represented by a group of points called reciprocal lattice points (REL P). Each point corresponds to a certain set of planes named by (h k l). The distance between a REL P and the origin (000) represents the inverse of the interplanar spacing and the relative positions of the RELPs are related to the interplanar angles. In the cubic system, the interplanar spacing $d_{(hkl)}$ can be calculated from lattice constant **a** by

$$d_{(hkl)} = \frac{a}{\sqrt{h^2 + k^2 + l^2}}.$$

In general, there are two scan directions to obtain data from HRXRD. The rocking curve scan, also known as ω –scan, is performed by rotating the sample stage without changing the

detector position. The motion path for the ω –scan in reciprocal space is a small arc centered at the origin (000). Since defects can tilt the lattice planes, which is equivalent to rotating the reciprocal space about the origin, the full width half maximum (FWHM) of the rocking curve scan peak is often used to quantify the crystallinity of the sample. Another type of scan, ω - 2θ scan, is primarily used to determine the lattice constant or measure the layer strain in heterogeneous structures. In an ω - 2θ scan, the detector (2θ) moves twice as much as the sample stage, so that it scans in a straight line pointing towards the origin in reciprocal space. For the (004) RELP, by converting the detector angle 2θ into interplanar spacing using Bragg's law ($2d\sin\theta = \lambda$, where λ is radiation wavelength), the out-of-plane lattice constants of the substrate and the layers can be obtained.

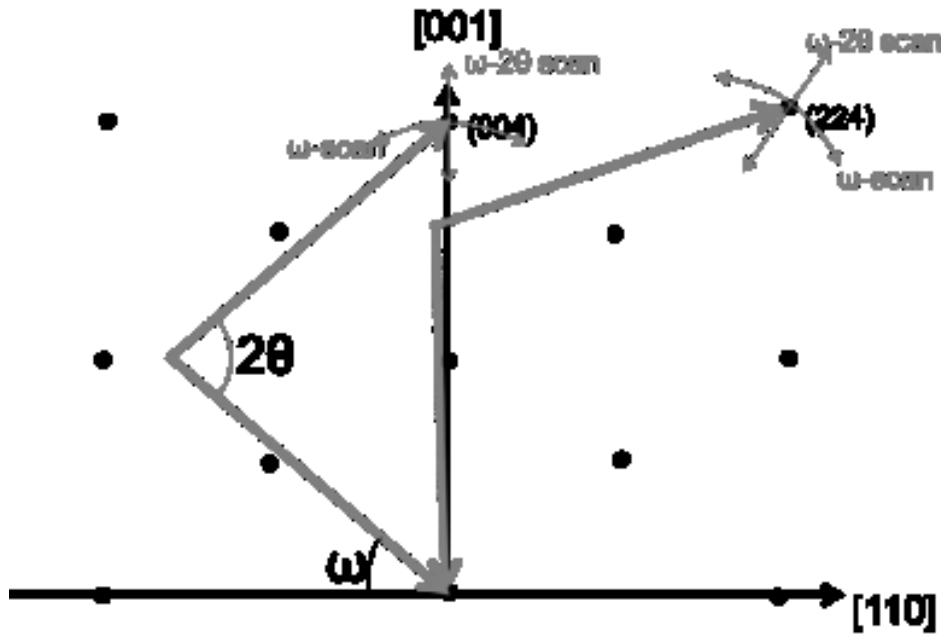


Figure 4.5: Schematic of a 2D slice of the reciprocal space of a zinc-blend crystal. The surface orientation is (001) and the x axis is in $\langle 110 \rangle$ direction. The scan directions of rocking curve scans (ω - scan) and ω - 2θ scans are drawn on (004) and (004) reciprocal lattice points.

However, planes parallel to the surface such as (004) do not provide any information about the in-plane lattice geometry. For epitaxial growth, it is important to know whether the layer is constrained to the substrate without relaxation through dislocations. RELPs (224) and (115) are usually used to reveal such in-plane features. Figure 4.6 shows the reciprocal space of a layer and a substrate. From the relative position of (004) points, the out-of-plane lattice constant of the layer is bigger than that of the substrate. If two (224) points are vertically aligned, there is no difference between the in-plane lattice constants, so that the epitaxial layer is pseudomorphic; if the (224) layer point falls on the relaxed line marked in Figure 4.6, the layer is fully relaxed; any place in between means partial relaxation. Occasionally, a reciprocal space map (RSM) is produced by a series of consecutive ω - 2θ scans with a few arc seconds offset in ω . It is best used to describe the details of multilayered structures, when single scans are insufficient to use.

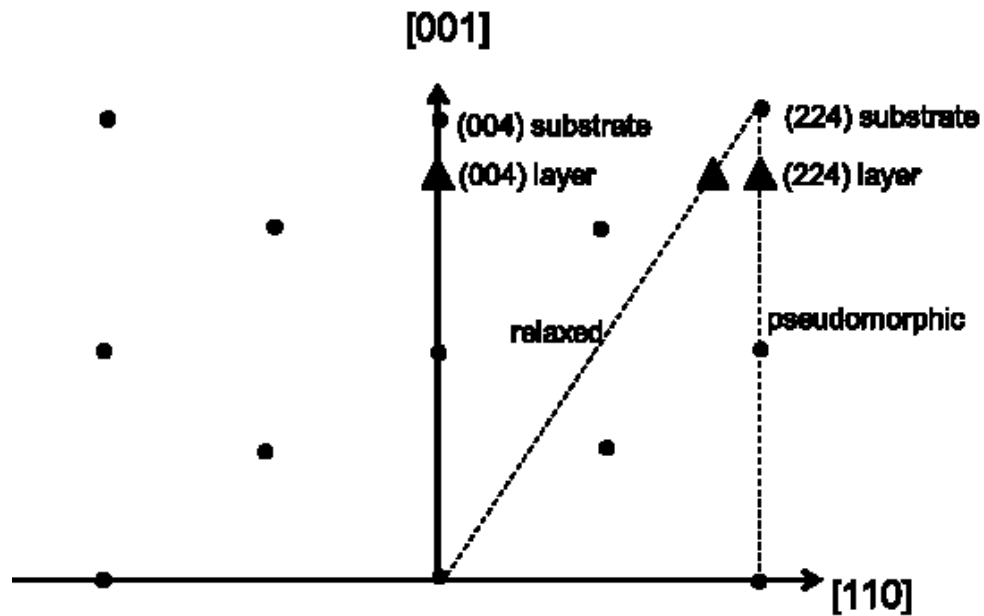


Figure 4.6: Simplified reciprocal space of a cubic structure substrate with an epitaxial layer. The position of (224) layer point corresponds to the relaxation status of the epi-layer.

X-ray topography maps the strains caused by dislocations or dopants [110]. In this study, it was applied to check the doping profile of InP wafers and its relationship to the porous layer morphology. As proposed by Köhler [111], the setup of X-ray topography in this study is shown in Figure 4.7. The X-ray radiation used is Cu K α . The diffraction plane of the 1st crystal is Si (224), and it is mainly used to expand the incident beam. Since the match of Bragg angles between the 1st crystal and the sample is recommended and the Bragg angle for Si (224) is 44.0°, InP (115) is used, which has a Bragg angle of 43.0°. To obtain better contrast, the exposure was taken at ¼ maximum intensity. Kodak SR1 X-ray film was used, with the maximum resolution of 800 dpi (the grain size is about 30 μm).

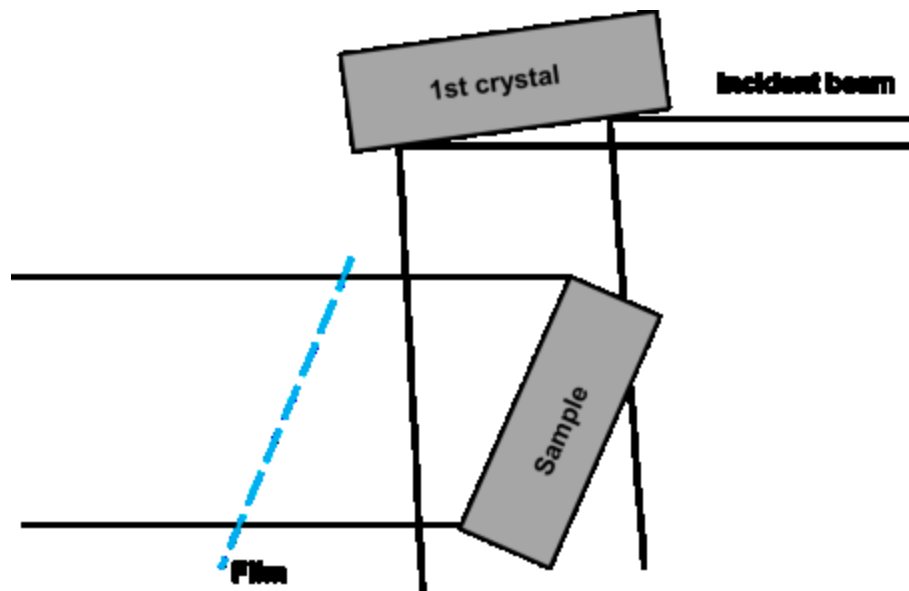


Figure 4.7: Schematic setup of X-ray topography.

4.4.3 Transmission electron microscopy

TEM is a power tool capable of imaging the atomic structure and identifying the defects due to diffraction contrast. The accelerating voltage is usually much higher than that of SEM, so the resolution for TEM is essential higher due to the shorter electron wavelength. Special sample

preparation is required to make the sample thin enough for the electron beam to transmit. For semiconductor materials, the typical sample thickness is 100 nm. An FEI Titan 80-300 kV in high tension mode (300 kV) was used in this study.

To prepare TEM samples, an FEI Nova 600 DualBeamTM system was used, in which both the electron beam for the SEM and the ion beam for focused ion beam (FIB) cutting are installed. The ion beam is made of Ga⁺ ions. To make a TEM sample, a thick (2-3 μm) sample piece, usually 20 μm $\times$ 10 μm , was first extracted out from the bulk sample by fast ion milling (30 kV, 20 nA) and transferred onto a TEM copper grid by a fine tungsten wire operated by a micromanipulator. The piece was then thinned down to the desired thickness using a process with much lower ion beam energy (10 kV, 1 nA). Ga⁺ ion cutting is known to produce an amorphous layer on the sample surface, and normally, every 10 kV accelerating voltage corresponds to a 10 nm thick amorphous layer [112]. Therefore, lowering the beam energy from 30 kV to 10 kV helps to reduce the amorphous ratio in a 100 nm thick sample from 60% to 20%. Besides, in order to protect the sample from damage by the scattered ion beam, Pt protection layers are usually deposited. Cross-section TEM (x-TEM) samples were made from both as-etched samples and epitaxially grown samples to check the crystal structures, and plan-view TEM (pv-TEM) samples were made from the epitaxial layer to quantify the defect density.

The basic configuration of the TEM is shown in Figure 4.8. By changing the condensing power of the intermediate lens, TEM is able to switch between imaging mode and diffraction mode. A scanning coil can be added into the system to allow scanning transmission electron microscopy (STEM). STEM enables the composition analysis from EDX by focusing the beam into a narrow spot which is scanned over the sample. A selective area aperture was used to

generate diffraction pattern from a chosen area as small as 150 nm in diameter. The diffraction pattern in TEM is essentially a planar intersection of the reciprocal space and it is often taken in an on-axis position, meaning a certain zone axis of the sample overlaps with the optical axis of the TEM system. By tilting the sample slightly from the on-axis position, one of the diffraction spots becomes as bright as the transmitted spot and the so-called two beam condition is achieved. Under this condition, if the objective aperture is placed around the transmitted beam, a bright field (BF) image appears on the viewing screen; if the objective aperture is placed around the diffracted beam, the image shown on the viewing screen is referred to as the dark field (DF) image. Since BF and DF images are associated with a certain diffraction spot, they are best used to observe dislocations and determine the directions of dislocation Burgers vectors. Atomic resolution in HRTEM is obtained when the sample is kept on-axis with no objective aperture inserted.

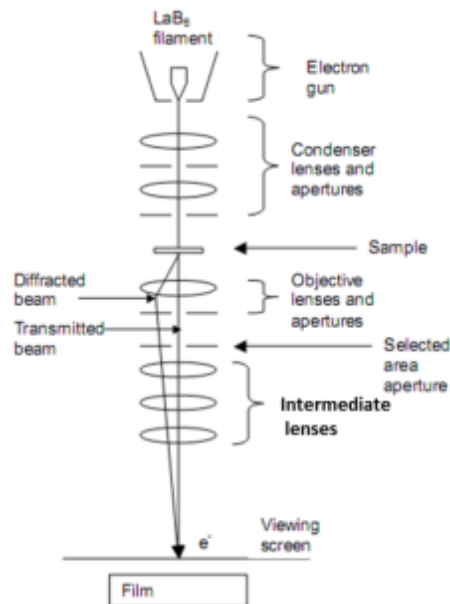


Figure 4.8: Schematic description of the configuration of a conventional TEM.

4.4.4 Nano-indentation

The Nano-indentation test was used to calculate the Young's modulus of the porous material. The nanoindenter probe features an inverted-pyramid-shaped tip. During indentation, a vertical force is gradually applied until the probe penetrates into the material to a predetermined depth. The original output information includes the real time force and the tip displacement. A typical force-displacement plot is shown in Figure 4.9. An MTS Nanoindenter XP was used in this experiment, and the indentation depth was limited to 20% of the porous InP layer thickness in order to avoid substrate interaction [103].

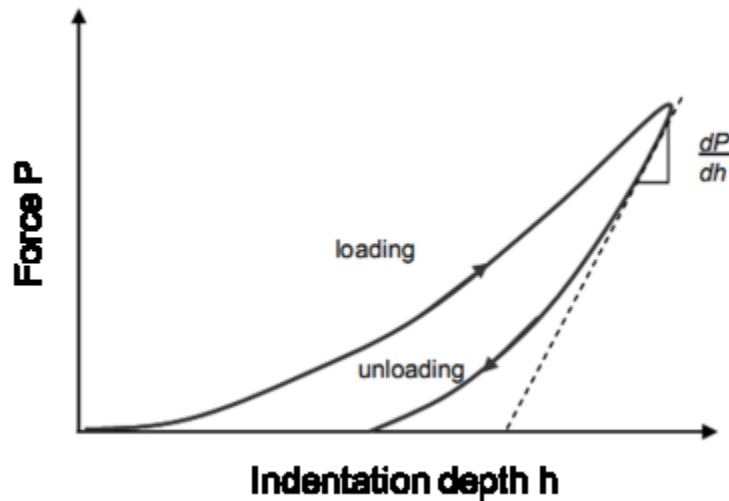


Figure 4.9: Representative graphic of a typical force-displacement plot in nano-indentation test.

Chapter 5 Formation of porous InP

5.1 Etching parameters

The control of porous layer morphology through etching parameters is one of the most advantageous traits of electrochemical etching. The pore size, pore density, and layer thickness are all dependent on the etching conditions. Rather than etch an entire wafer under a specific set of conditions, the aperture in the electrochemical etcher was used to define areas of 2 cm² so several different sets of conditions could be studied using a single wafer. Figure 5.1 shows four different porous InP layers etched on a 2” diameter wafer. In this section, a systematic analysis on the effect of various etching parameters is presented.

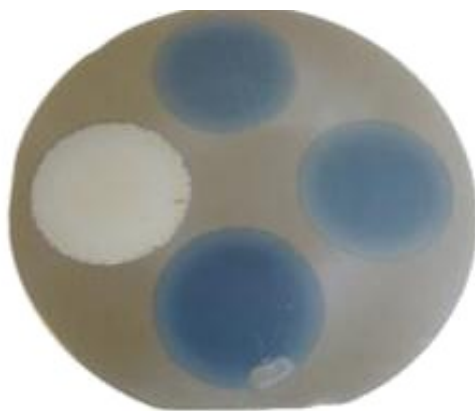


Figure 5.1: Photograph of porous InP spots with different etching parameters on a 2-inch diameter wafer.

5.1.1 Etching current density

For galvanostatic etching, the etching current density essentially determines the strength of the electric field at the electrolyte-sample interface. As discussed in Chapter 2.2, a low current density (<100 mA/cm², 5% HCl), induces a weak electric field, resulting in the formation of

crystallographically oriented pores; while a high current density ($> 100 \text{ mA}$, 5% HCl), leads to current-line oriented pores.

Etching in 5% HCl at 200 mA/cm^2 for 60 sec leads to a columnar, current-line oriented pore morphology. Figure 5.2 shows the basic features of current-line oriented pores in both cross-section and plan-view. At this current density, the strong electric field drove the etching direction perpendicular to the sample surface, and formed the column shaped pores. The wavy profiles result from the fact that for heavily doped ($> 10^{18} \text{ cm}^{-3}$) InP wafers etched at 200 mA/cm^2 , the pore walls are too thin to stand without curving, while straighter profiles were observed on other samples with lower current density (e.g. 100 mA/cm^2). The etch rate should be more than $10 \text{ }\mu\text{m}$ per min, but because the porous layer was very weak, the layer collapsed to various extent during the etching. As a result, for cross-section SEM, even at the thickest region, the thickness of the remaining layer was no more than $5 \text{ }\mu\text{m}$. Another consequence of layer collapse is poor surface topography, since the roughness is on the order of microns. From the plan-view image (Figure 5.2 (b)), there is hardly any flat region for an epitaxial layer to nucleate, so the current-line oriented porous layer is by no means suitable for layer transfer. Therefore, the current-line oriented pore structures are in general discarded in this study due to their high surface roughness and fragility.

On the contrary, the crystallographically oriented pores possess many desirable properties for layer transfer. As seen from the plan-view image in Figure 5.3, the pore nucleation on the porous layer is homogenous throughout the entire etching area and the size of the pores is much smaller ($< 100 \text{ nm}$) than the current-line oriented pores. According to nanoheteroepitaxy (Ch. 3.3.2), a surface with pores between 10 nm and 100 nm is expected to be suitable for lateral

growth of the epitaxial layer. The cross-section views of the two preferred cleavage planes (110) and (1 $\bar{1}$ 0) are different since the pores develop along the $\langle 111 \rangle_B$ direction, as also shown in Figure 2.9(a). The surface of the crystallographically oriented pores resembles a “mesa” topography, with considerable flat regions separated by the pores.

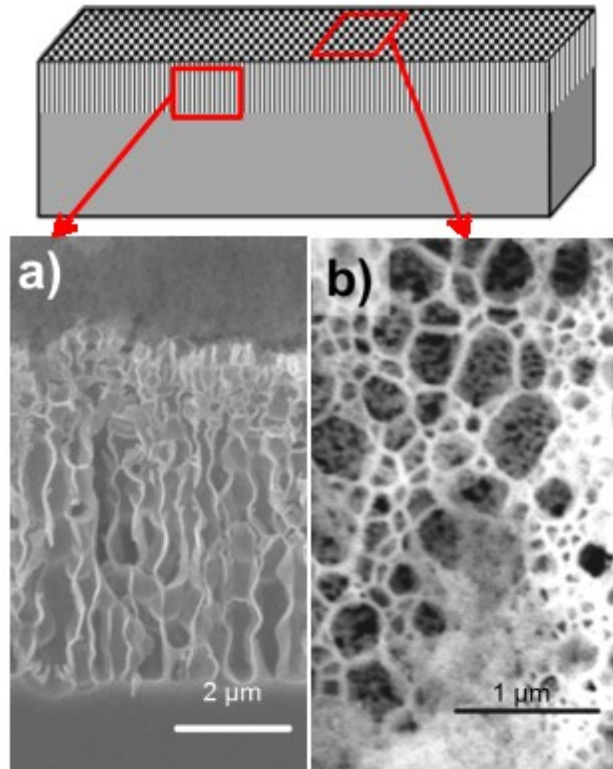


Figure 5.2: SEM of current line oriented porous InP etched at $J= 200 \text{ mA/cm}^2$, 5 % HCl for 60 seconds. a) Cross-section view 60° tilt angle); b) plan-view.

Within the field of crystallographically oriented pores, current density is related to the layer porosity and etch rate. Since charge carriers for porous layer growth are generated by the space charge region break down, surface defects are preferential sites for pores to nucleate. Higher current density makes more defects ‘qualified’ for such pore nucleation and results in higher porosity of the layer. As shown in Figure 5.4, two samples were made on the same wafer

after 120 sec etching in 5% HCl with different current densities. A current density of 12 mA/cm^2 produced a layer with 60% porosity and a thickness of $1.45 \text{ }\mu\text{m}$. Approximately doubling the current density to 25 mA/cm^2 produced a layer with 75% porosity and a thickness of $2.46 \text{ }\mu\text{m}$. The increased etch rate with higher current density is a result of faster charge carrier supply, which is consisted with the assumption that porous etching is reaction limited in this regime.

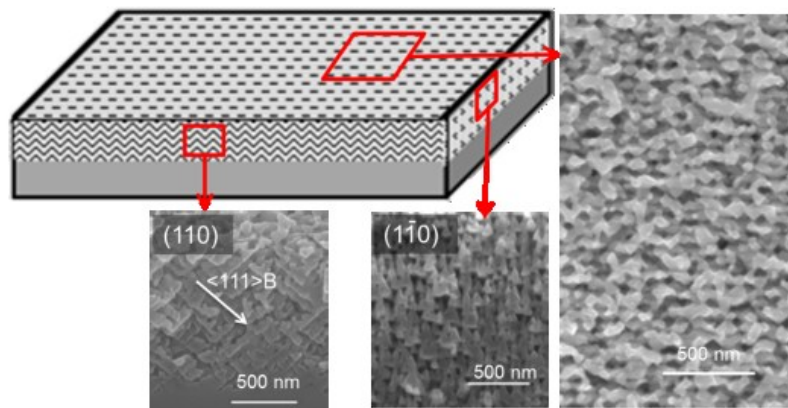


Figure 5.3: SEM of crystallographically oriented porous InP etched at $J = 25 \text{ mA/cm}^2$, 5 % HCl.

The two cross-section views were taken at tilt angle 60° .

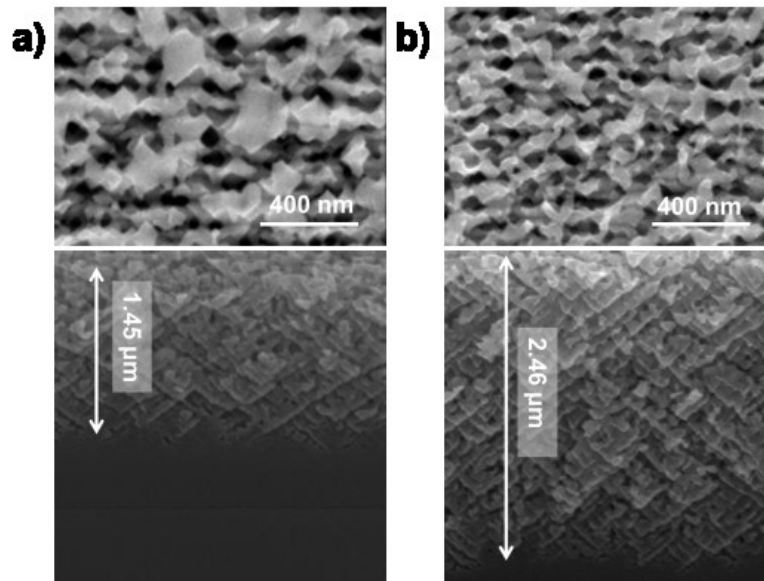


Figure 5.4: Plan-view (top) and corresponding cross-section (bottom) SEM images of porous InP after 120 sec etching in 5% HCl with current densities: (a) 12 mA/cm² and (b) 25 mA/cm².

5.1.2 Electrolyte concentration

While current density has a major effect on the pore nucleation density, the electrolyte concentration plays a stronger role in the pore size. Smaller pores are more favorable for the lateral growth of epitaxial growth and to reduce the surface RMS roughness.

Figure 5.5 shows the role of electrolyte. Here, all layers were etched with the same current density of 6 mA/cm² for 240 sec. By using different HCl concentrations (from 10% to 40%), the average pore size decreased from 110 nm to 20 nm. As a result, the porosity of the layers changed from 36% to 18%. As mentioned in Chapter 2.1.1, the porosity change with electrolyte concentration is general attributed to the passivation behavior of H⁺ ions. However, a more specific explanation from etching mechanism is yet to be made for its relationship with pore size. In addition, it is worth mentioning that all the SEM plan-view images were taken with the bottom edge of the samples being (110). Several pores may join together in the lateral direction, so the pore sizes were determined from their vertical dimensions.

5.1.3 Wafer doping concentration

Another important parameter that determines the porosity is the doping concentration of the wafer. Although doping concentration is not intentionally varied in this study, interesting results were obtained. Wafers from different sources were used. Wafers from one source produced uniform porous structures, Figure 5.1 above is a good example of that. Figure 5.6(a), however, displays an interesting swirl pattern with visible striations in an optical photograph. Figure 5.6(c) shows an SEM plan view micrograph of the surface which reveals a difference in

the pore structure; these regions of high and low porosity correspond to the contrast observed in the optical swirl image. Prior to etching, the wafer surface appeared uniform and, in addition, similar etching conditions using substrates from a different manufacturer produced uniform porous areas.

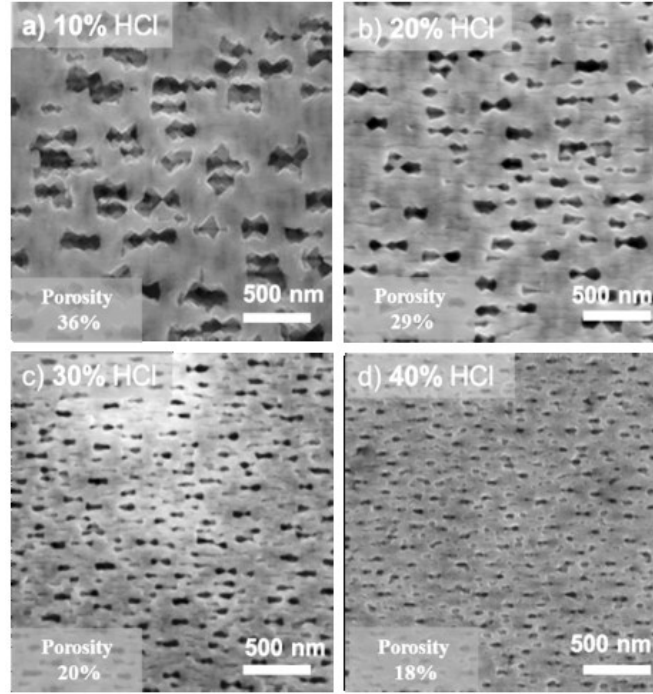


Figure 5.5: Plan view SEM of porous InP prepare etched at 6 mA/cm^2 for 240 sec with different HCl concentrations. Note: (a) 10% HCl and 36% porosity (b) 20% HCl and 29% porosity (c) 30% HCl and 20% porosity (d) 40% HCl and 18% porosity.

To assess whether this swirl pattern was due to doping striations in the wafer, a wafer was first imaged using high resolution x-ray topography [110]. The unetched topograph image shows the same striation pattern as the subsequently etched piece. The origin of the striations in the x-ray topography image is due to changes in the lattice parameter (or tilt between one region and the adjacent region but tilt was ruled out [114] through a series of topograph images). The

InP wafer are n-type ($3-8 \times 10^{18} \text{ cm}^{-3}$) and doped with sulfur. The addition of sulfur to InP is known to change the lattice parameter [115-117]. The intensity change observed in the topograph (which corresponds to the InP (115) reflection) corresponds to a shift of approximately 2 arcsec. This represents a lattice parameter strain (from dark to light regions) of approximately 1×10^{-5} which is consistent with a change in S from $5 \times 10^{18} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$. If the substrate is non-uniformly doped, as is the one in Figure 5.6(a), striations will appear after etching due to the difference in refractive indices of the layer where the porosity changes. In contrast, the wafer shown in Figure 5.1 has more uniform doping and thus the porous layers are more uniform.

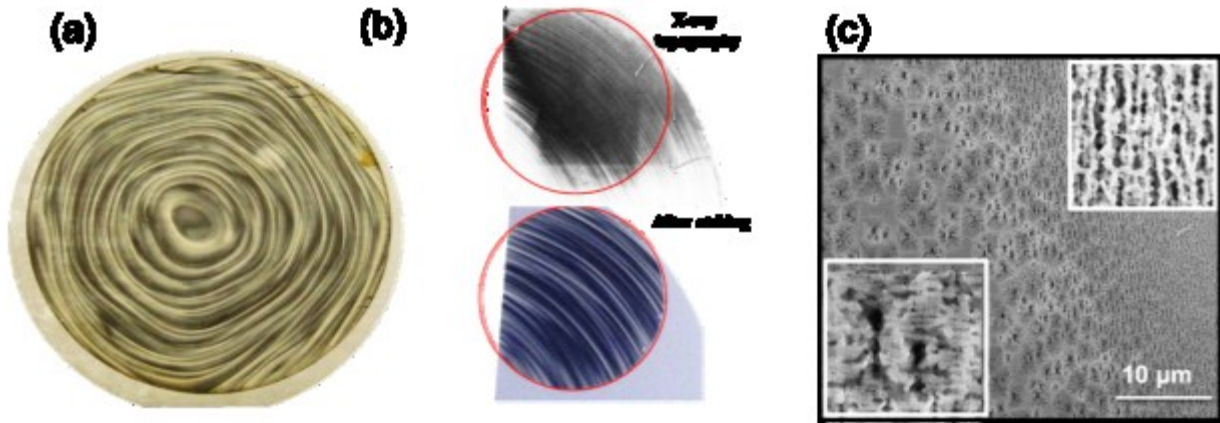


Figure 5.6: (a) Doping striations present on a 2 inch electrochemical etched InP wafer indicating the close relationship between doping concentration and porosity. (b) SEM image showing the reason of visible difference within micron range.

According to the SCR model discussed in Chapter 2.1.3, the distance between adjacent pores is inversely proportional to the square root of the wafer doping concentration. Therefore, higher doping concentration leads to closer pore spacing, and thus higher porosity. Figure 5.6(c) shows the porosity transition due to the difference in doping concentration within the wafer. The

pore distance (2 μm) in the lower left area is about 2.2 times longer than the one in the upper right region (0.9 μm), indicating the difference in doping concentration is approximately 5 times.

5.2 Dual porous layer preparation

To achieve layer transfer, it is desirable to adopt a dual porous layer structure which consists of a denser top layer suitable for the epitaxial growth and a weaker, less dense buried layer dedicated to the layer fracture. In addition, it was suggested by Yonehara that a dual layer structure acts to protect the seed wafer and epitaxial layer during the ELTRAN layer transfer process, by confining the fracture plane within the porous layer [118].

Electrochemical etching is a self-limited process. Therefore, multi-layer structure can be prepared sequentially by using different etching recipes for each layer. For a substrate that is uniformly doped, the porosity is mainly controlled by the current density and electrolyte concentration. An example of a dual layer structure is shown in Figure 5.7. The top layer was etched first with a low current density of 9 mA/cm^2 , followed by the formation of the buried layer, which was etched with a higher current density of 88 mA/cm^2 . The difference in layer porosity is shown in cross-section images. The top layer has a typical morphology of crystallographically oriented pores with the pore propagation along the $\langle 111 \rangle_{\text{B}}$ direction. However, the buried layer shows a sign of transition into the current-line oriented morphology due to the high current density. The change of pore angle along with the current density for crystallographically oriented pores has been plotted as a linear function in Ref [97]: the higher the current density is, the steeper the pore wall will be.

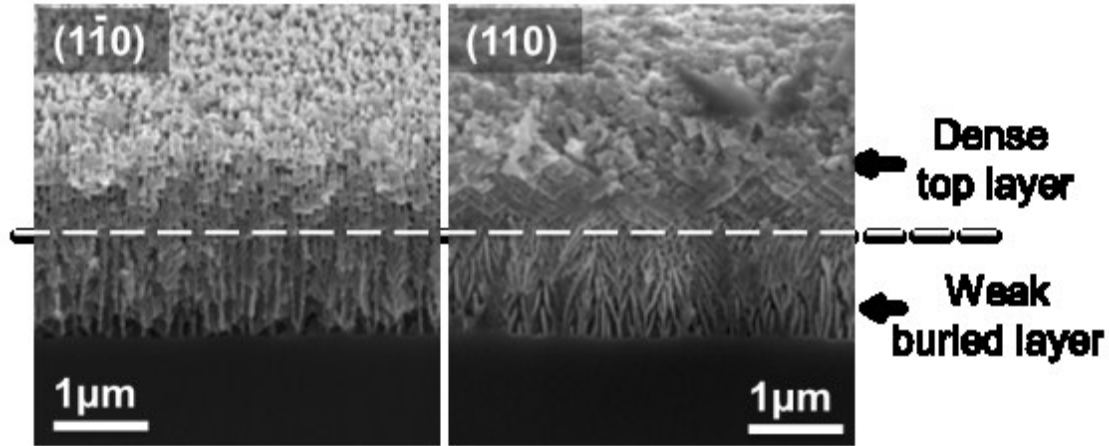


Figure 5.7: Cross-section SEM of a dual porosity layer along the $(1\bar{1}0)$ and (110) faces. The top layer was etched with $J=9 \text{ mA/cm}^2$ for 120 sec and the buried layer was etched with $J=88 \text{ mA/cm}^2$ for 20 sec. The HCl concentration was kept at 5% for both layers.

5.3 Porous InP characterization

5.3.1 Surface roughness

The surface roughness of the porous layers was determined by AFM. For crystallographically oriented porous layers, the RMS roughness ranges between 40 Å to 250 Å from $10 \times 10 \text{ μm}^2$ scans with corresponding porosities of 18% and 75%. It was found that reducing the pore size most effectively lowers the surface roughness. For epitaxial growth, it is anticipated that a smooth surface roughness is preferred. Figure 5.8 shows the AFM scans on a representative dense top layer. The layer was etched with 6 mA/cm^2 current density in 30% HCl, and the porosity was 20%. $10 \times 10 \text{ μm}^2$ scans were applied in this study to give RMS values since they scanned over enough area to average out any local variations, while $1 \times 1 \text{ μm}^2$ scans were used to reveal detailed pore features such as pore size.

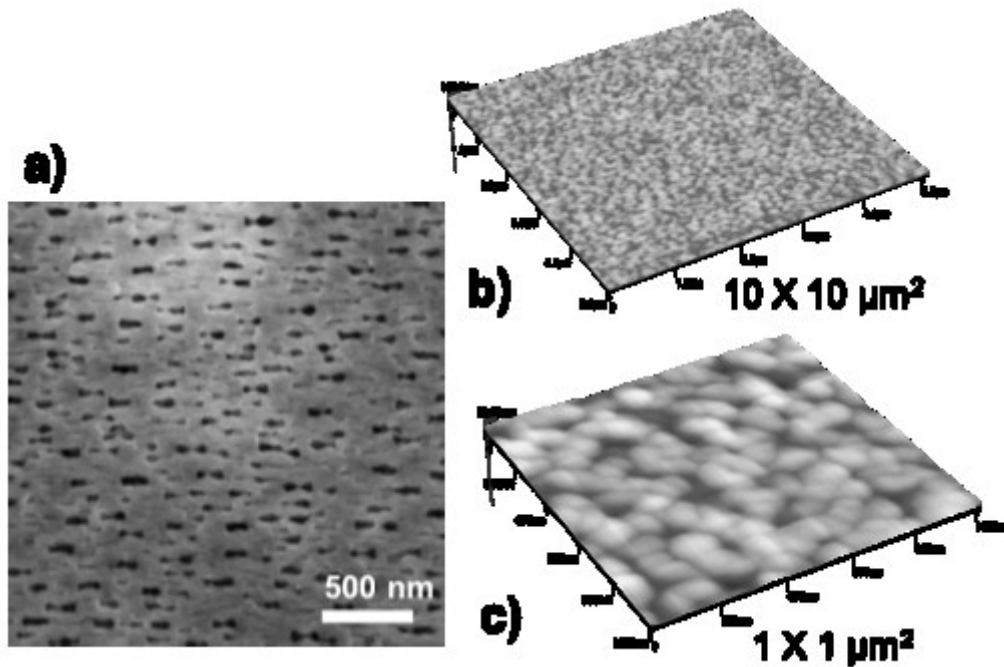


Figure 5.8: Surface morphology of a porous InP layer prepared by $J=6 \text{ mA/cm}^2$, 30%. a) Plan-view SEM; b) AFM scan over a $10 \times 10 \mu\text{m}^2$ area, with the RMS roughness $58 \text{ \AA}$; c) AFM scan over a $1 \times 1 \mu\text{m}^2$ area, with the RMS roughness $47 \text{ \AA}$.

The surface topography is comparable to a “mesa” for most of the crystallographically oriented layers, so that the roughness of the flat top was measured from a $50 \times 50 \text{ nm}^2$ scan, as shown in Figure 5.9. In general, the RMS roughness obtained from a polished surface is about 1-3 $\text{\AA}$. The RMS roughness of the flat area is $2.4 \text{ \AA}$, so it is reasonable to assume that the flat area was part of the original surface of the InP wafer. The assumption was supported by the fact that there is no height difference across the O-ring area on the etched samples, so no electropolishing happened during the porous layer formation.

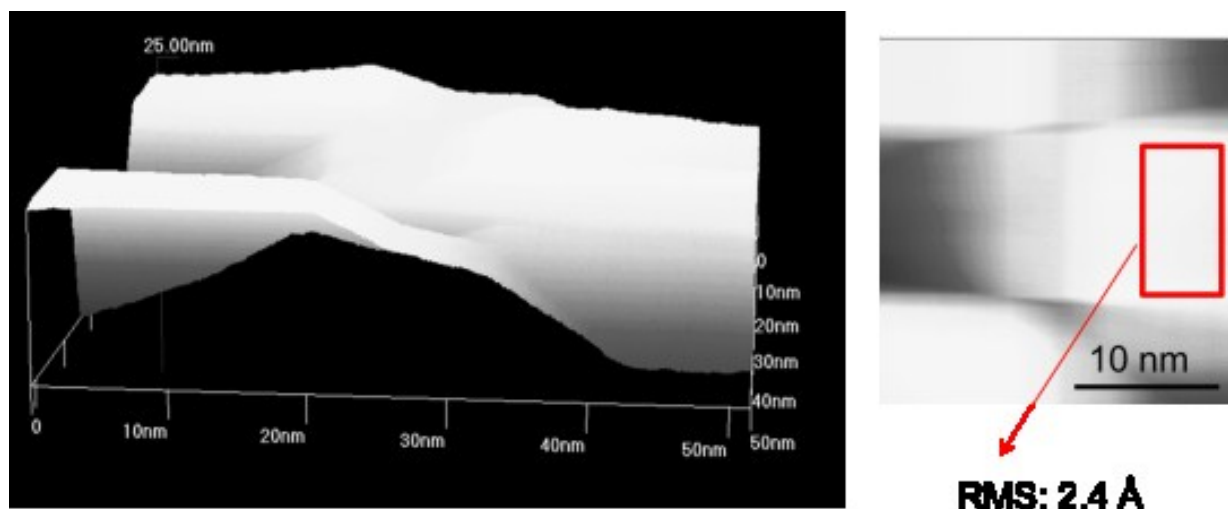


Figure 5.9: AFM scan of 50 X 50 nm² on a porous InP surface. The flat region has a RMS roughness as low as 2.4 Å.

5.3.2 Mechanical properties

The Young's modulus, measured from nano-indentation, provides some insight into the fracture toughness of the porous layers. Since the Young's modulus is calculated from the slope of the unloading curve in the force-displacement plot shown in Figure 4.9, the calculated value of Young's modulus can also be plotted as a function of indentation depth as shown in Figure 5.10 (a). The measured elastic modulus for bulk InP is 87 GPa [119]. It can be seen that all the porous layers have a lower elastic modulus than the bulk InP.

Normally, the elastic modulus is independent of the indentation depth and appears as a flat line like the bulk InP. The apparent increase in the Young's modulus as the indentation tip goes deeper into the porous layers is explained in Figure 5.10 (b). Once the porous structure was compressed by the indentation tip, the density of the underlying layer would increase, so the elastic modulus increases accordingly. If the tip goes even deeper, the modulus of these porous layers would approach that of the bulk material [120]. Thus, the most accurate value of the

elastic modulus is obtained immediately after the tip engagement on the sample surface, which is highlighted (arrow) in Figure 5.10(a). For the layers etched with $6\text{mA}/\text{cm}^2$ for 240 sec, the mechanical strength reduces when HCl concentration changed from 30% to 20%, which is consistent with the previous conclusion that lower electrolyte concentration results in higher layer porosity. Also, the porous layers etched with higher current density tend to be weaker. Under same etching conditions, thicker layer prepared with longer etching time also shown to be weaker due to less substrate effect.

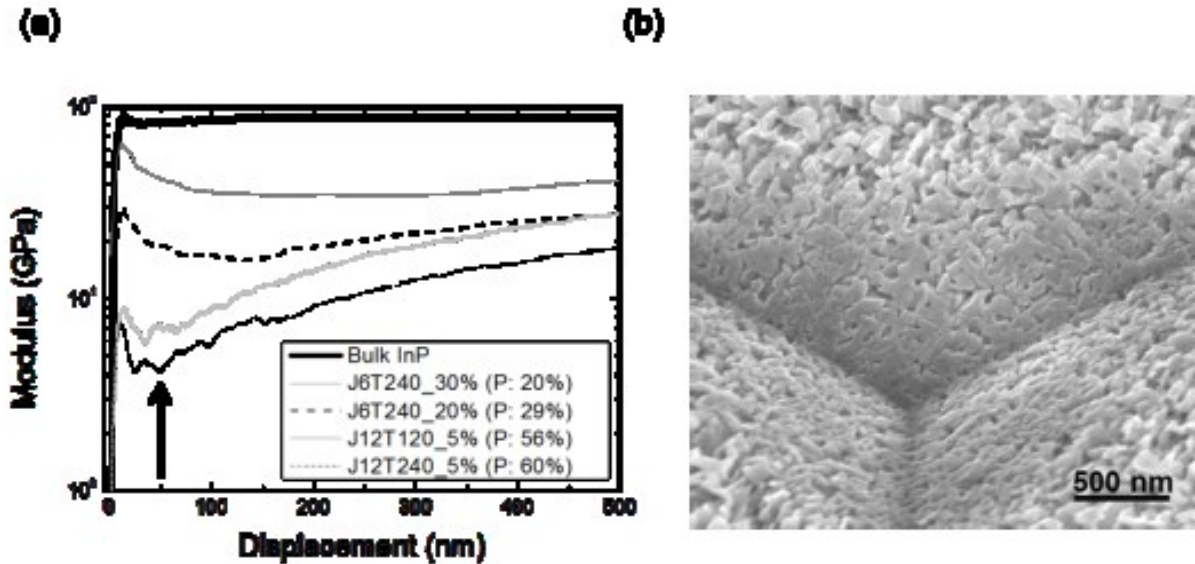


Figure 5.10: (a) Young's modulus of different porosity samples measured by nano-indentation test. (b) Cross-section of an indentation pit, showing porous layer deformation as a result of indentation.

Chapter 3.2.2 noted that the mechanical property of porous Si can be simulated using the Gibson-Ashby open cell model, so that the relationship between the elastic modulus and the layer porosity follows $E = A(1 - P)^2$, where A is 120 GPa, which is the elastic modulus of bulk Si [88, 121]. For porous InP, the Young's modulus can also be plotted to fit a polynomial function of the layer density, as shown in Figure 5.11. However, the open cell model doesn't fit

so well for porous InP. Instead, $E = 87(1 - P)^4$ gives a better description of the relationship between layer porosity and the Young's modulus for porous InP.

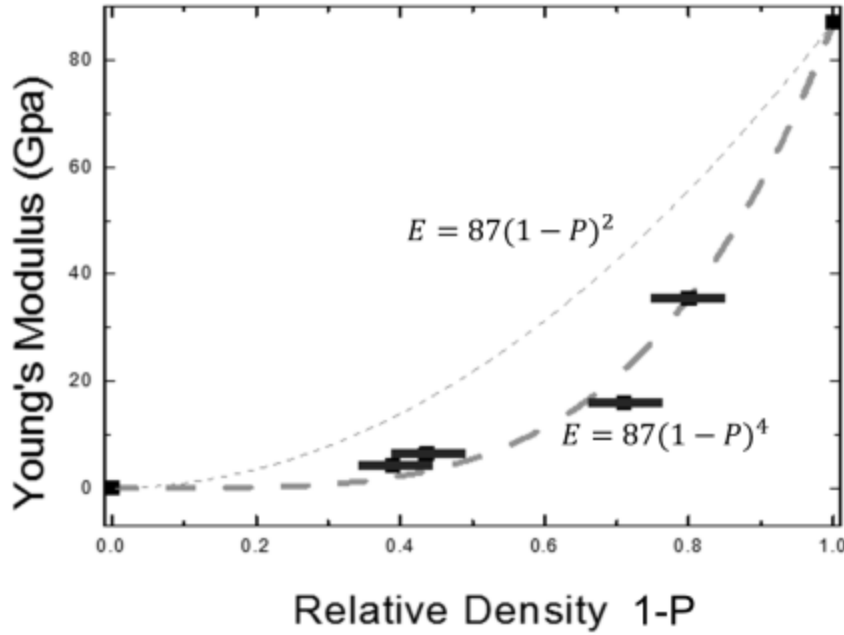


Figure 5.11: The Young's modulus is plotted with relative density of the layer, where P is porosity. The uncertainty of the layer porosity is $\pm 5\%$, marked by the short bars.

5.3.3 Crystallinity and composition

Cross-section TEM samples of the porous layers were prepared by FIB along the (110) cleavage plane. Figure 5.12(a) shows a bright field image of a TEM sample. The over-saturated regions are the pore areas where transmitted beam is not absorbed. Selective area diffraction was taken from both the porous layer and the substrate with a 150 nm diameter aperture. The two diffraction patterns overlap perfectly with each other, indicating the porous layer to be single crystalline with the same crystal orientation as the substrate.

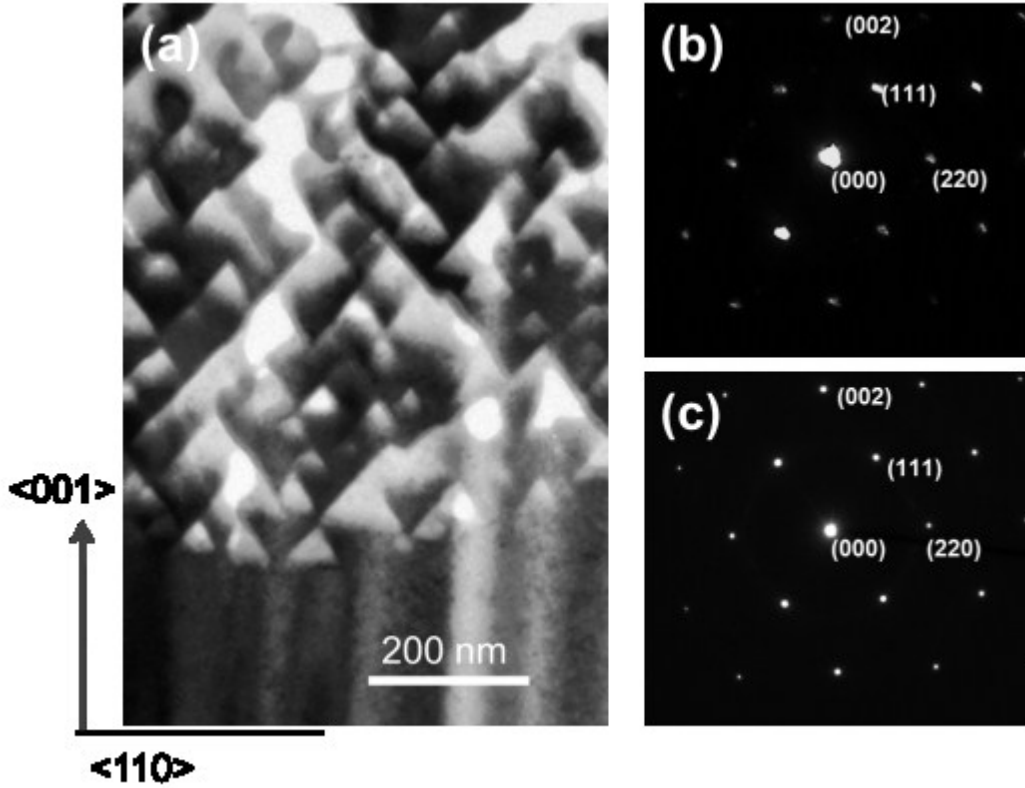


Figure 5.12: Bright field TEM (a) of an as-etched porous InP sample and diffraction patterns from the porous layer (b) and the bulk substrate (c).

More detailed analysis was made with HRXRD. Figure 5.13(a) shows two ω - 2θ scans at (004) diffraction position. The substrate peaks are calibrated at zero, and the two porous layer peaks are shifted from the substrate peak due to out-of-plane strains. Between these two samples, the one with 67% porosity has a compressive strain of 0.65%, while the one with 54% porosity has a compressive strain of 0.54%. This is speculated to be associated with dangling bond formation during the etching process due to material removal, and re-association of these dangling bonds leads to lattice distortion. The more material being removed, the higher the porosity of the layer is and the higher the strain will be. On the contrary, Strain was also observed for porous Si [34,122]. In that case, a tensile strain present in as-etched porous Si was

attributed to the absorption of hydrogen atoms during the anodization process, and this tensile strain can eventually transform into compressive strain by annealing as a result of desorption.

As explained in Chapter 4.4.2, the FWHM of a rocking curve scan is usually applied to quantify the crystallinity of the sample. Figure 5.13(b) and (c) shows the rocking curve scans of the substrate and the layer for the 67% porosity sample. Both of them show a FWHM of 9 arcsec, which indicates good crystallinity of the porous layer, comparable to the substrate. At FW0.01M, the porous layer peak (28 arcsec) becomes broader than the substrate (19 arcsec) due to diffuse scattering from the porous structure [123,124].

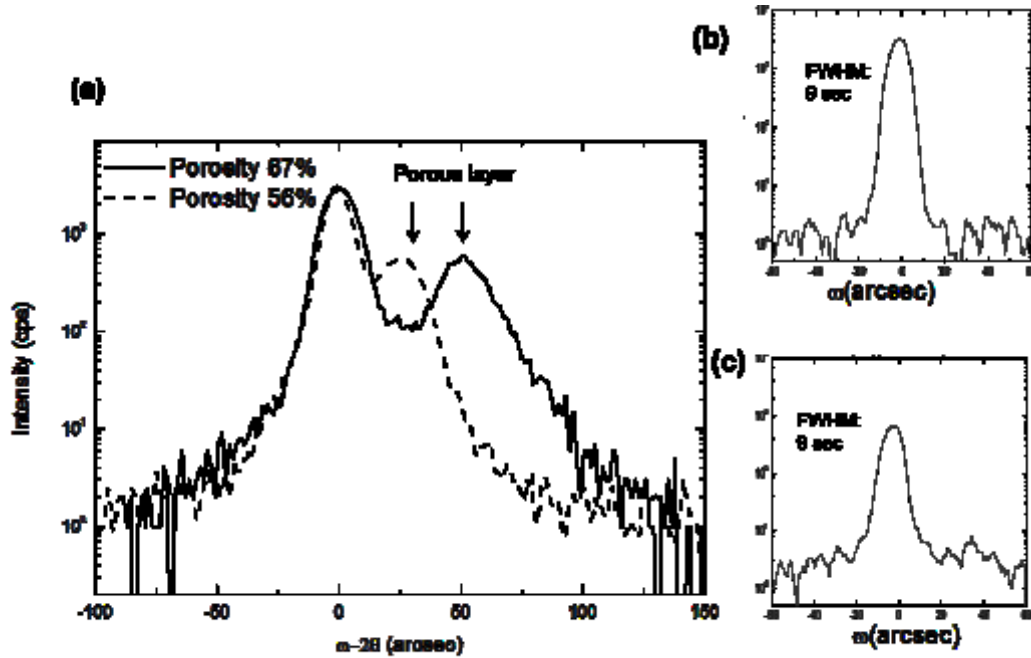


Figure 5.13: HRXRD of as-etched porous InP samples at (004). (a) ω -2 θ scans of porous InP layers with 67% and 56% porosities. The offset of porous layer peaks from the substrate peak indicates out-of-plane strains within the porous layers. (b) and (c) are rocking curve scans of the substrate and the layer with 67% porosity.

The in-plane strain was also assessed for the as-etched porous samples. From the (224) RSM shown in Figure 5.14, the out-of-plane strain is indicated by the vertical displacement of the layer peak relative to the substrate peak. However, no in-plane strain exist in the porous layer since there is no displacement in the lateral direction, which means the porous layer remains constrained to the substrate despite the out-of-plane strain.

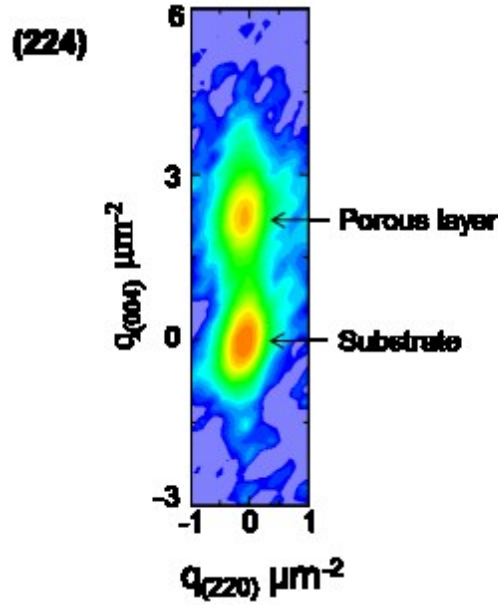


Figure 5.14: High resolution RSM at (224) diffraction spots of an as-etched porous InP sample.

It was observed that the strain eventually evolves away for samples which have been put aside for several weeks or after annealing. Unlike a heterogeneous structure, where strain relaxation happens through dislocations, the strain inside the porous layer can relax by surface passivation, as is the case for silicon. The rate of relaxation is highest right after etching, so that all the XRD measurements on as-etched samples were done within 2 hours after sample preparation. Figure 5.15 shows how the strain evolved in atmosphere after 11 weeks.

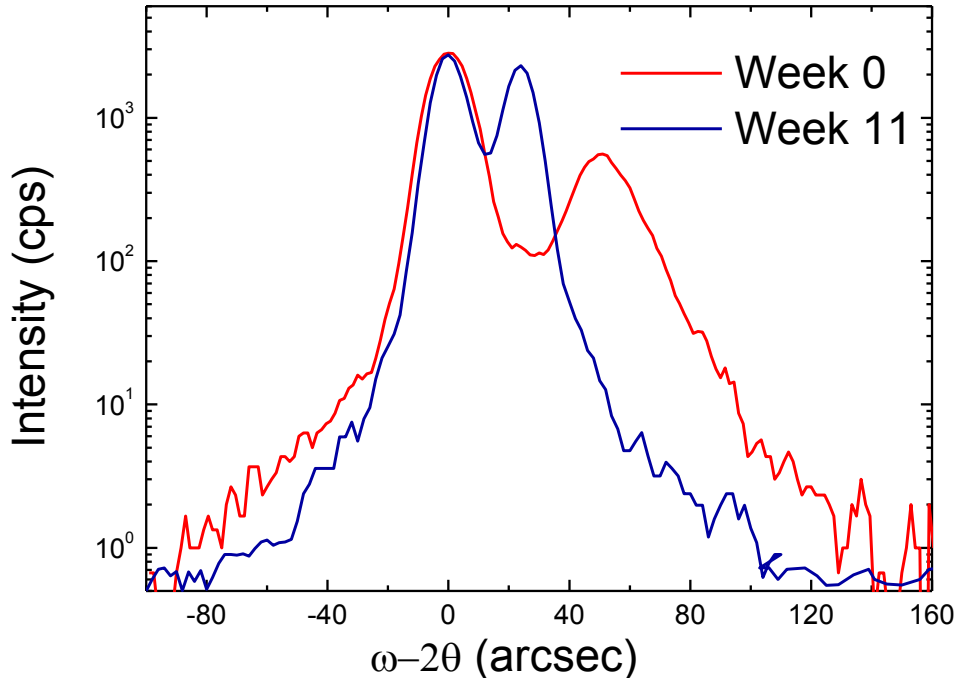


Figure 5.15: HRXRD ω - 2θ scans to show the strain evolution within a porous layer.

The layer composition was checked by EDX. For moderate etching conditions ($< 30\%$ HCl and $< 100 \text{ mA/cm}^2$), the stoichiometry of the porous layer is preserved (Figure 5.15 (a)). However, significant indium loss was found in some of the porous InP layers. A typical case is shown in Figure 5.15(b), where the top layer (on the right) was etched with 4 mA/cm^2 in 40% HCl and the buried layer was etched with 50 mA/cm^2 in 4% HCl. From the EDX results, the top layer (point 1) basically becomes depleted of indium, and the buried layer also suffers from severe indium loss. A similar observation of gallium loss was reported in GaAs and GaP etching [125-128], and it was explained by the formation of an As or As_2O_3 overlayer on the porous structure due to facilitated reduction of dissolved As species in certain etching conditions. The diffraction pattern from the buried layer (point 3) is still crystalline, which indicates that there is a P-rich overlayer on the InP core. This may be useful since an excess group V elements is potentially beneficial for epitaxial growth.

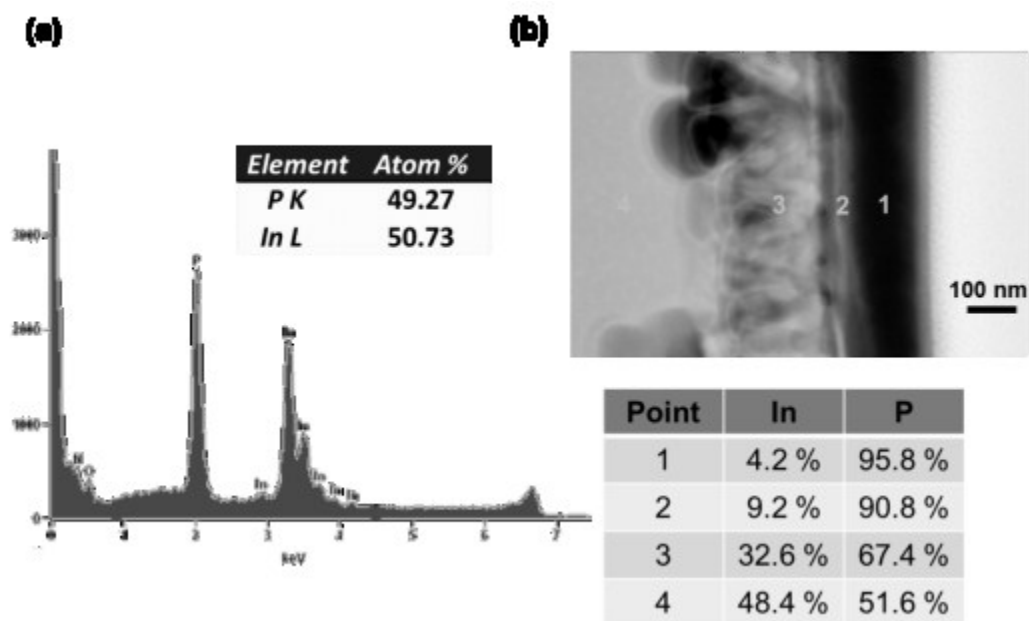


Figure 5.16: Composition analysis by EDX of porous InP samples. (a) EDX spectrum of an porous InP sample etched with 9 mA/cm^2 in 5% HCl, which shows preserved stoichiometry of InP. (b) STEM image of a dual layer sample etched with 4 mA/cm^2 in 40% HCl followed by 50 mA/cm^2 in 4% HCl. The table shows the atom% of Indium and phosphorus at each point.

Chapter 6 Porous InP annealing and epitaxial growth

6.1 Annealing results

The necessity of annealing porous InP was explained in Chapter 3, and the experimental setups for annealing were covered in Chapter 4.2. Two questions need to be addressed from the annealing results: whether the porous surface could fully coalesce or at least show improved surface roughness, and whether the porosity would change to alter the mechanical properties of the porous layer.

For annealing on the hotplate at 450 °C, single layer samples (with InP proximity caps) were used to focus on the issue of surface coalescence. Figure 6.1 shows the plan-view SEM images of a sample, which was etched at 25 mA/cm² in 5% HCl for 120 sec, annealed at 450 °C with different annealing times, from 10 min to 8 hours. On the as-etched sample, the pores exhibit a rhombus shapes, with rather homogenous spacing between each lateral row of pores. The condition didn't change much after two hours annealing, while noticeable changes started to show after 4 hours. In order to reduce the total surface energy, the edges of each pore become more rounded. After 8 hours, smaller pores joined together to form larger pores and the flat surface ratio increased from 40% for as-etched sample to approximately 70%. It was also observed that after 8 hours annealing, some voids appeared at the interface between the porous layer and the substrate (Figure 6.2), and parts of the layer even exfoliated. One possible explanation is that similar surface coalescence process also happened at the interface, where small pores merged into larger voids in order to reduce the total surface area. However, it should be noted that voids formation was not a common observation on every annealed single layer sample, so the layer porosity must also play a role in it. Therefore, major efforts were devoted to

study the transformation behavior of porous layer, not only as a function of thermal budget, but also as a function of layer porosity.

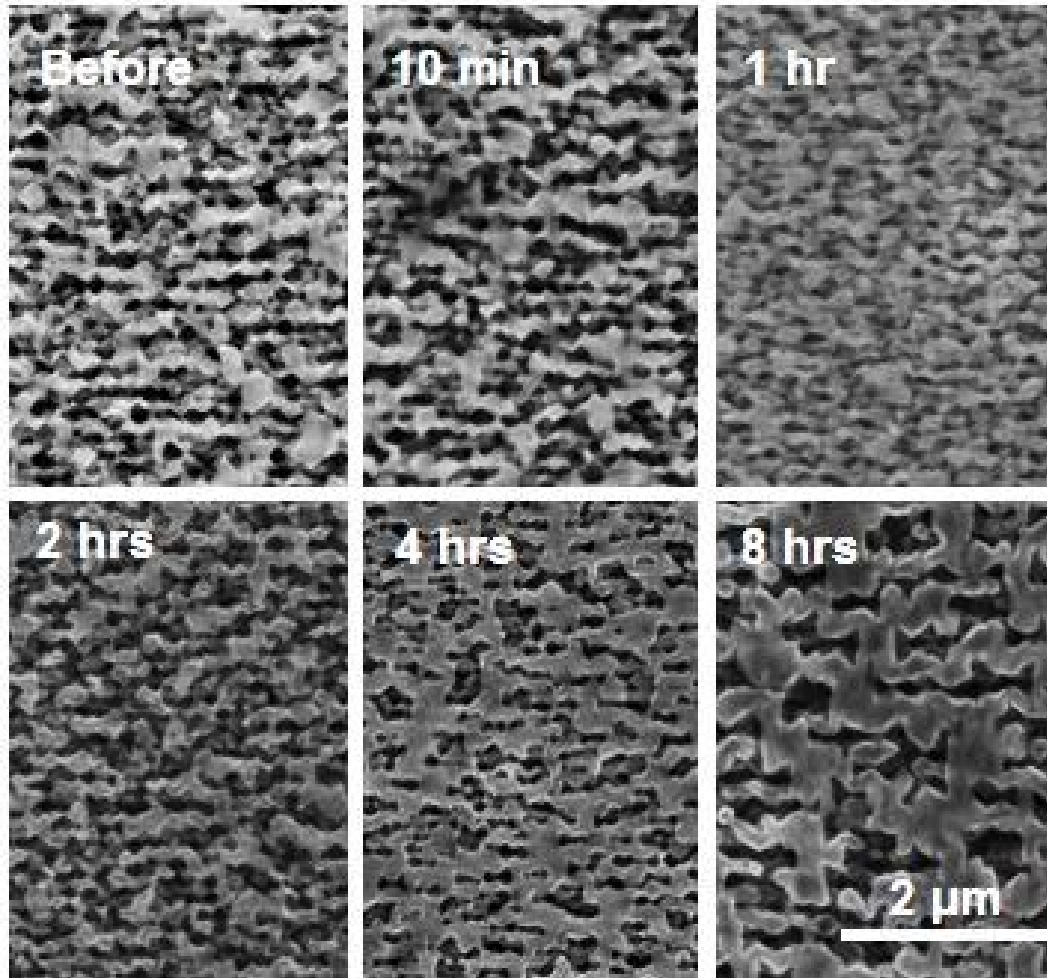


Figure 6.1: SEM plan-view of a porous InP samples annealed with different annealing times. The sample was etched with $J= 25 \text{ mA/cm}^2$, in 5% HCl for 120 sec.

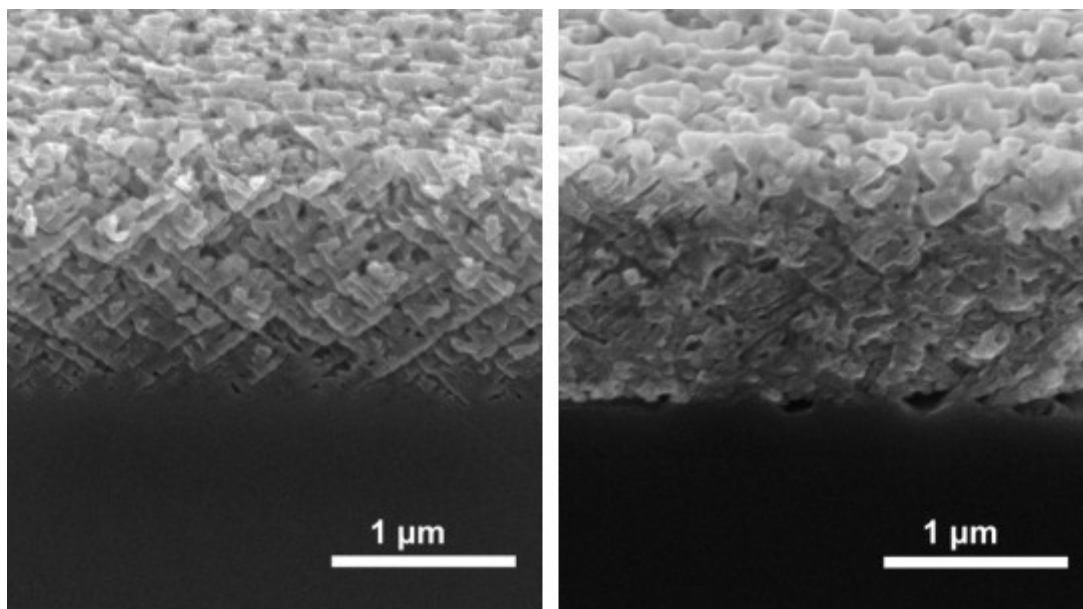


Figure 6.2: SEM cross-section view of the porous InP samples shown in Figure 6.1 (a) without annealing and (b) after 8 hours of annealing at 450 °C on hotplate.

Despite of the convenience of hotplate annealing, there is one drawback when annealing in atmosphere: layer oxidation. Figure 6.3 shows the EDX spectrums of a porous sample before and after annealing. The ratio between In and P changed only slightly, indicating the usage of an InP capping wafer prevents most of the P loss. However, due to the high surface ratio of the porous structure, oxidation took place after 2 hours annealing in atmosphere, with 74 % oxygen detected. Formation of an oxide overlayer may delay or prevent further morphology change during annealing, and some of the observed change may be attributed to the oxide growth other than diffusion [76]. Therefore, the following two annealing experiments were performed in purged environments, one with N₂ and the other with H₂. Both of the purged annealing environments proved capable of preserving InP composition, so this point will not be restated in this chapter.

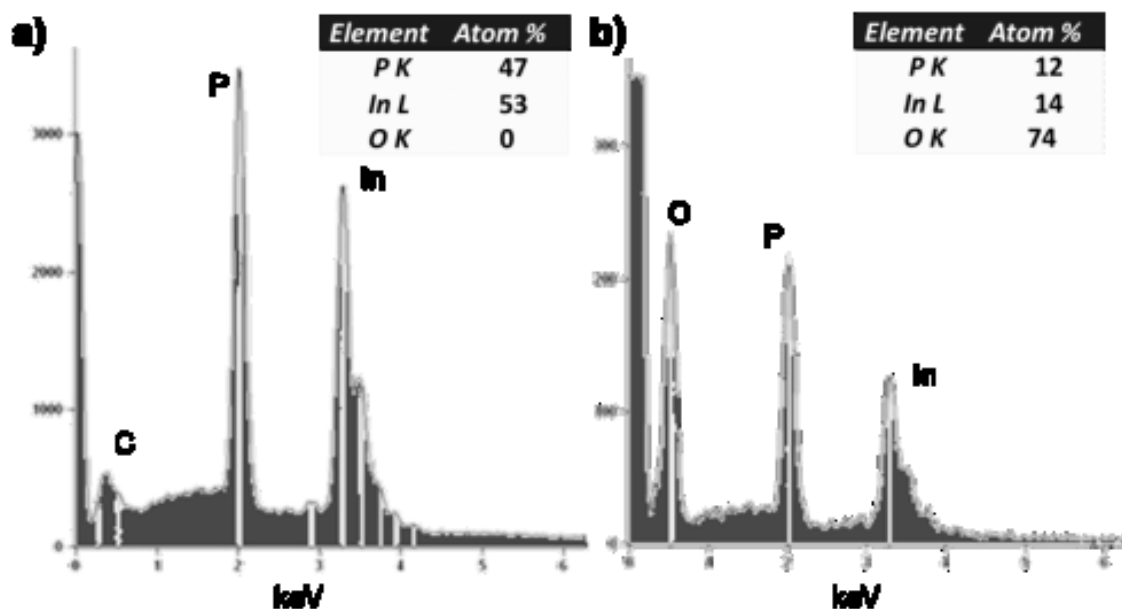


Figure 6.3: EDX spectrum from plan-view SEM on a porous InP sample a) before and b) after 2 hours annealing on hotplate.

It has been noted that annealing at 550 °C mimics the epitaxial growth temperature (typically from 500 °C – 650 °C for MOVPE InP, and 480 °C – 560 °C for MBE InP) and 750 °C is the equivalent annealing temperature for porous InP as 1015 °C for porous Si (the ratio of the annealing temperature to the melting point in both cases is 0.77), which showed complete surface coalescence [77]. The annealing results at these two temperatures with N₂ purging on a dual layer structure are shown in Figure 6.4. At 550 °C, the structural change was very similar to what happened at 450 °C on the hot plate, only shorter time (30 min vs. > 4 hr) was applied. Plan-view images in Figure 6.4 (a) and (b) were taken from the same location on the sample for better comparison. The general features didn't change much, but nano scale bumps and pits shown on the surface of the as-etched sample were no longer visible on the annealed sample. For the cross-section images, voids were observed at the interface between the high porosity buried layer and

the substrate, and the presence of these voids should be accountable for the ease of layer fracture of the annealed samples. It should be noted that the porous layer morphology change in this cross-section image doesn't accurately reflect what happened inside the porous layer since the sample was cleaved before annealing, which makes the cleavage planes essentially another surface during annealing.

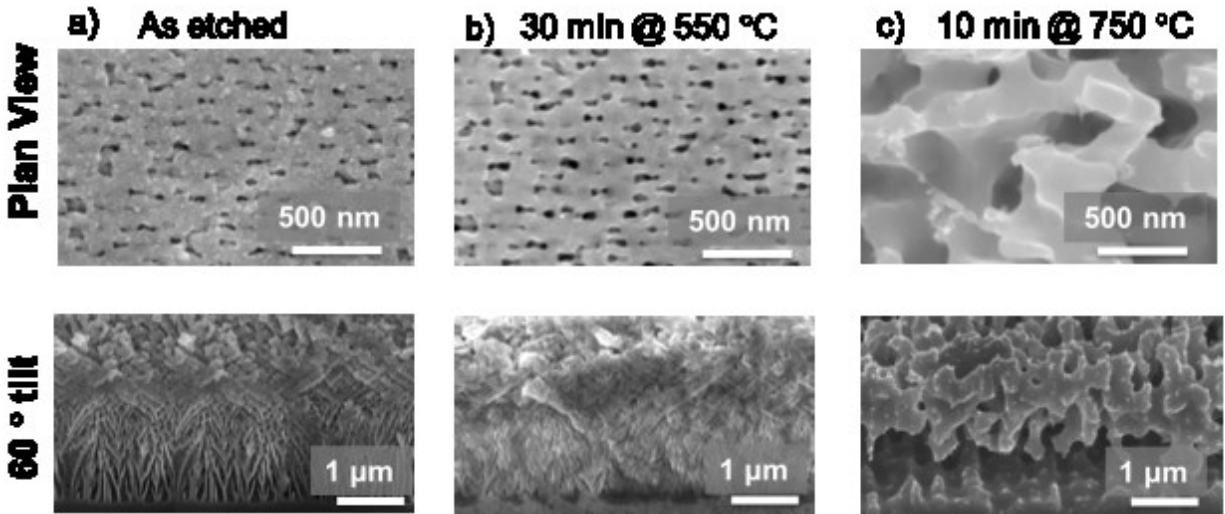


Figure 6.4: Plan-view (top row) and cross-section (bottom row) images of a dual layer porous InP structure. a) Without annealing; b) after 30 min annealing at 550 °C with N₂ purge; c) after 10 min annealing at 750 °C with N₂ purge. The top layer was etched with 9 mA/cm² in 5% HCl for 120 sec and the buried layer was etched with 88 mA/cm² in 5% HCl for 20 sec.

Contrary to what has been expected at 750 °C, significant changes occurred to the porous structure after only 10 min annealing in N₂ purged chamber, instead of surface coalescence. Large voids formed throughout the entire buried layer, so the connection between the top layer and the substrate was significantly weakened. However, not all porous samples failed to withstand the 750 °C annealing, but it is not yet fully understood which porous property plays a major role in here. For example, sample A and B in Figure 6.5 were etched with 6 mA/cm² for

240 sec, in 20% HCl and 30% HCl respectively. Since only the electrolyte concentration was changed, according to the conclusion drawn in Chapter 5.1.2, sample A is of higher porosity (29% vs. 20%) with larger pore size (50 nm vs. 23 nm). After annealing at 750 °C, sample A was able to maintain its porous structure but showed significant morphology change with surface ratio dropped from 71% to 42%. Also, from the AFM scans on $40 \times 40 \mu\text{m}^2$ area, the surface roughness increased from 47 Å to 206 Å. In comparison, for sample B with lower porosity, the morphology change turned out to be more drastic, as shown in Figure 6.5 (c) and (d).

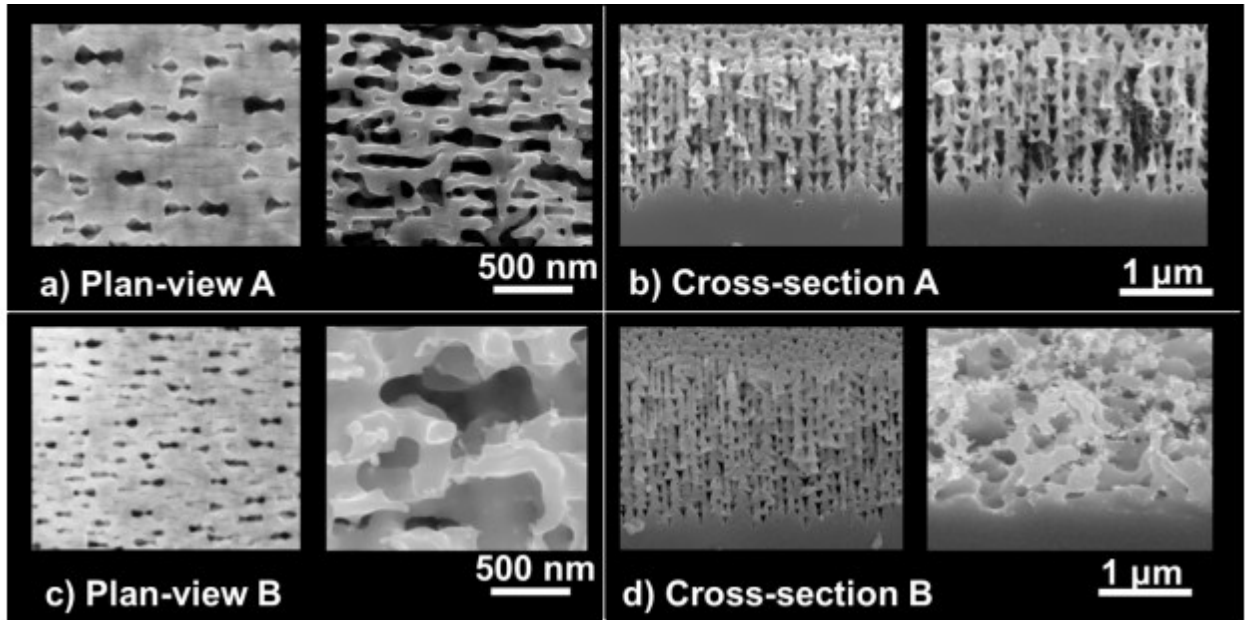


Figure 6.5: SEM images of sample A and B before (left) and after (right) annealing at 750 °C.

Sample A and B were etched with 6 mA/cm^2 for 240 sec with 20% and 30% HCl respectively.

Various combinations of layer structure and annealing condition were tested in search of a situation when annealing results in improved surface roughness and weaker buried layer. One successful case is shown in Figure 6.6. Although the flat surface ratio reduced from 77% to 57% due to pore size enlargement of $\sim 10\%$, the overall surface roughness obtained from AFM did not

deteriorate for the annealed sample. The original surface roughness was measured to be 28 Å ($40 \times 40 \mu\text{m}^2$) and 48 Å ($5 \times 5 \mu\text{m}^2$), and reduced to 26 Å and 42 Å, respectively. From the cross-section images, the separation between the top layer and the buried layer was marked with a dashed line. Rough estimates of the layer porosities were made on different sections from the cross-section image. The porosity change within the top layer was about 7% and it was much smaller compared to the change within the buried layer, which increased from 53% to 75%. No large voids were found at the interface between the porous layer and the substrate, while the higher porosity buried layer also proved helpful during the fracture process.

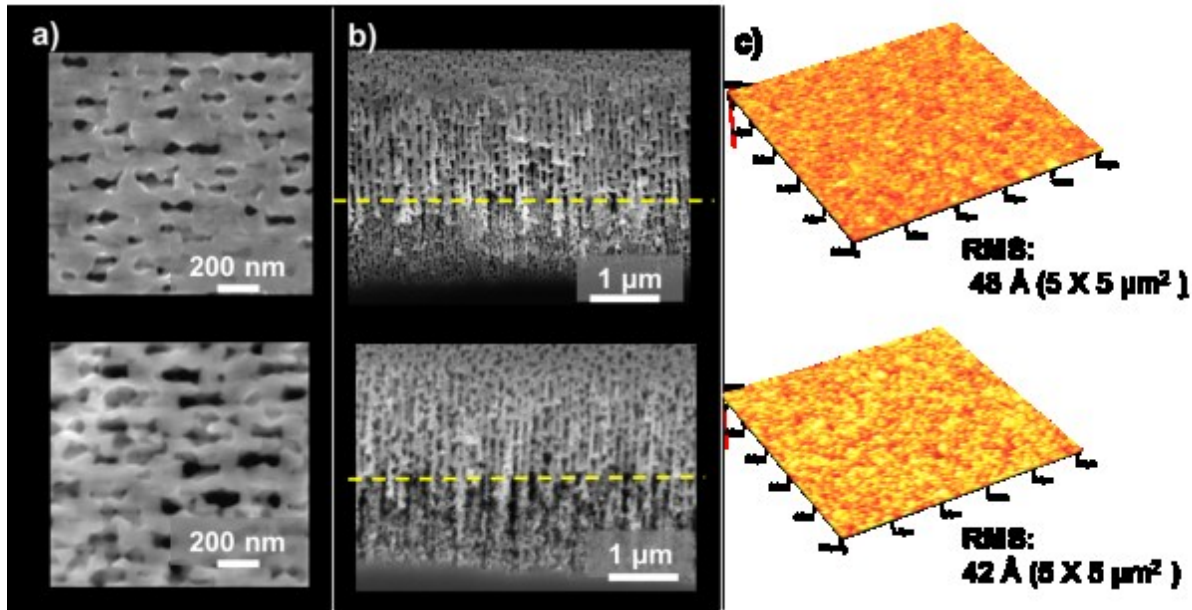


Figure 6.6: SEM images (a,b) and AFM scans (c) of a dual porous layer before (top row) and after (bottom row) annealing at 650 °C for 20 min. The sample was etched with 6 mA/cm² in 30% HCl for 180 sec followed by 25 mA/cm² in 4% HCl for 60 sec.

6.2 Epitaxial layer growth

Epitaxial layers were grown on porous InP in an MOCVD chamber at 650 °C for 30 min. If no TMIn precursor was supplied, only layer reconstruction happened by annealing. The comparison before and after annealing on a single layer sample etched with 12 mA/cm² in 10% HCl for 240 sec is shown in Figure 6.7. Similar to the annealing results at 650 °C discussed in the previous section, the pores in the annealed sample have more rounded edges and show size enlargements, but not as dramatic as what happened at 750 °C.

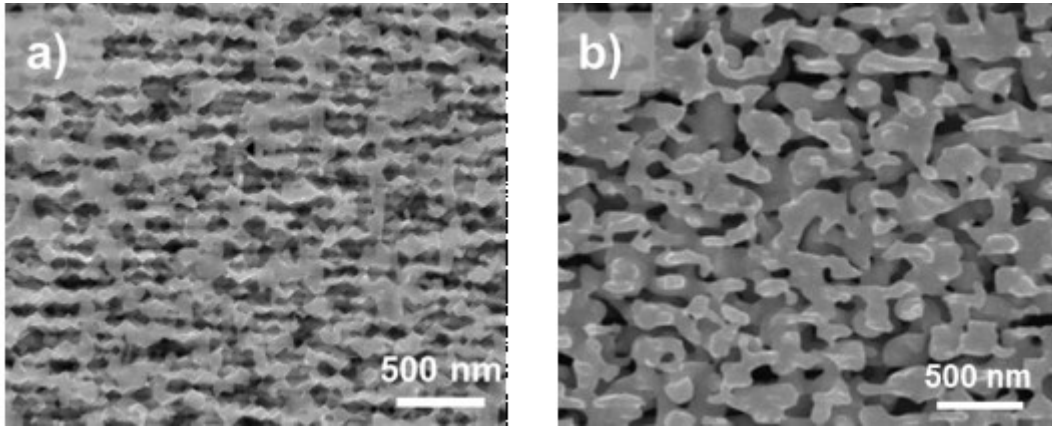


Figure 6.7: Plan-view SEM images of a porous InP sample (a) before and (b) after 30 min annealing at 650 °C in MOCVD chamber with TBP carried H₂. The sample was etched with 12 mA/cm² for 240 sec in 10% HCl.

The differences among the as-etched, annealed and epitaxial grown samples on (1 $\bar{1}0$) cross-section planes are shown in Figure 6.8. It is obvious that the porous material coalesced similarly in both annealed and grown samples, with adjacent pores merged together forming larger voids and thicker pore walls. Such mass transportation eliminated most of the sharp corners within the porous layer, reduced total surface area, so that the surface energy was lowered. It is worth pointing out that, the cross-section views in both Figure 6.8(b) and (c) were

prepared by FIB. The over layers shown in Figure 6.8(b) corresponds to the Pt protective layers deposited in the FIB tool to protect the sample surface, different from the over layer on the grown sample. In Figure 6.8(c), the InP epitaxial layer fills the surface voids and grows into a continuous layer within a few nanometers of layer thickness. The quality of the epitaxial layer will be discussed separately in the next section.

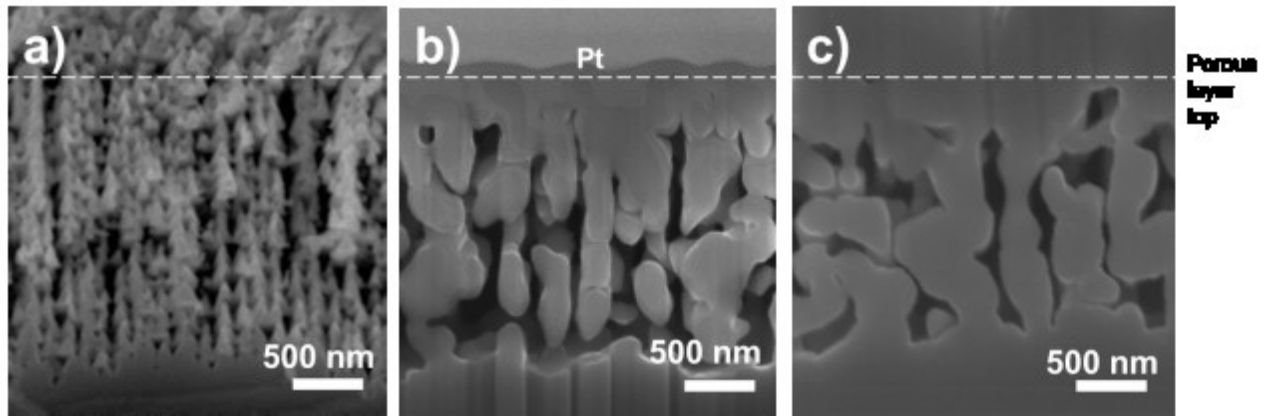


Figure 6.8. Cross-section SEM images of the porous layer for (a) as-etched, (b) post annealing and (c) after epitaxial growth.

6.3 Characterization of the epitaxial layer

The requirement to fabricate high performance devices is good single crystallinity of the epitaxial layer, so it is important to characterize the quality of the layer grown on porous surface.

TEM was employed to determine whether the deposited layer was epitaxial or not and to assess the crystalline quality in terms of defect concentration. From the (110) bright field XTEM shown in Figure 6.9(a), there are three regions: the InP substrate, the porous layer and the deposited layer. Thus, a selective area aperture was inserted to take the diffraction pattern exclusively from the deposited layer area and it is shown in Figure 6.9(b). The well-defined diffraction spots indicate the layer to be single crystalline and the labeled (002) point shows the

out-of-plane orientation is $[001]$ which is fully aligned with the substrate. Overlapping the epitaxial layer diffraction pattern with the one obtained from the substrate reveals no discernible point shift, which indicates that the strain within the epitaxially deposited layer is below the resolution of the technique.

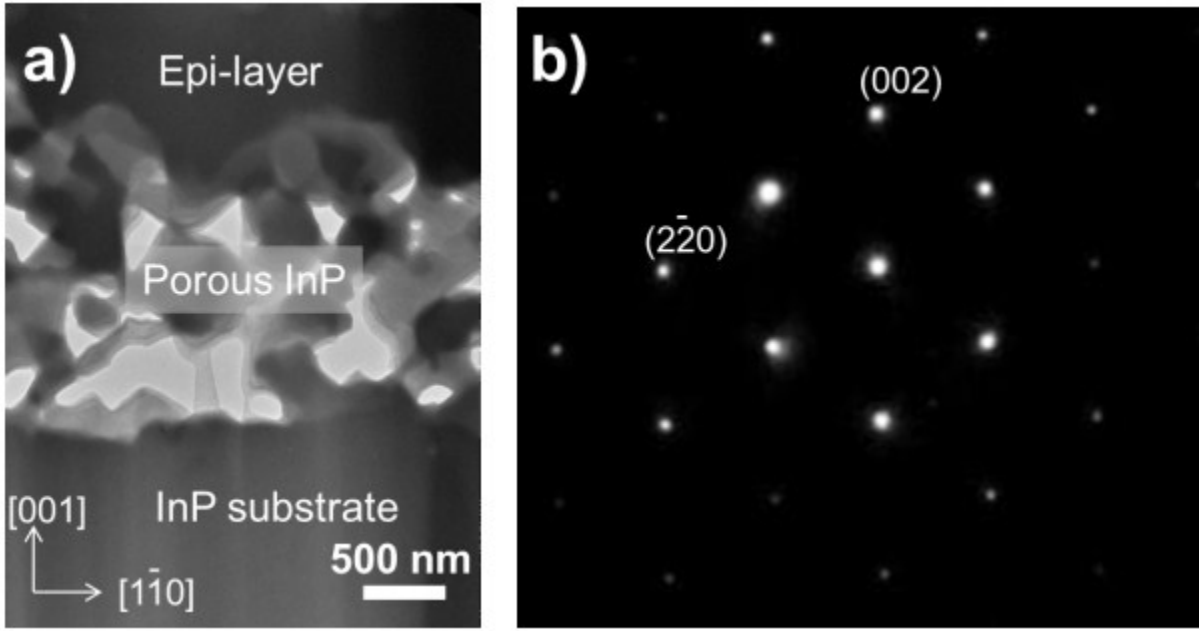


Figure 6.9: (a) Bright field XTEM of the post growth sample and (b) the diffraction pattern of the deposited epitaxial layer.

In order to check the lattice registration between the epitaxial layer and the porous layer, a HRTEM image shown in Figure 6.10 was taken at the interface. Due to the existence of pores inside the porous layer, the interface could be pinpointed by the thickness contrast. In Figure 6.10, since the epitaxial layer shares the same zone axis $[110]$ with the porous layer, good atomic resolution is achieved on both sides, and clear lattice registration along $(1\bar{1}1)$ planes are observed.

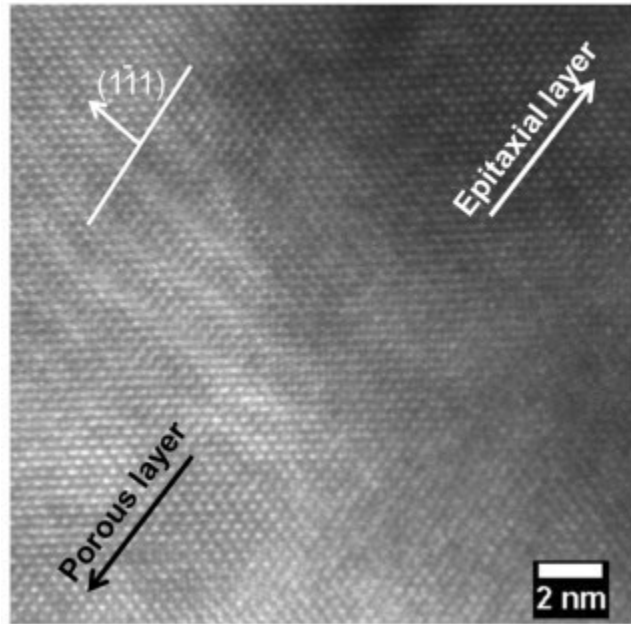


Figure 6.10: HRTEM at the interface between porous layer and epitaxial layer showing full atomic registry between the porous and epitaxial layers.

In addition to XTEM, pv-TEM samples of the epitaxial layer were also prepared by FIB. The entire pv-TEM sampling area is about $35 \mu\text{m}^2$, and images taken at various two beam conditions did not reveal any dislocation defects [129], which indicates a dislocation density less than approximately $3 \times 10^6 \text{ cm}^{-2}$. Figure 6.11(a) shows a STEM image of a magnified area of the plan-view sample compared with an equally size SEM image of the as-etched porous surface. Technically, any grain boundaries should be visible at this magnification, but in the STEM image, it appears to be a continuous layer with no lines or other defect features. Thus, the epitaxial layer was obviously able to cover the porous surface through lateral growth without forming grain boundaries. The low defect density and absence of grain boundaries make the epitaxial layer desirable for high performance device fabrication.

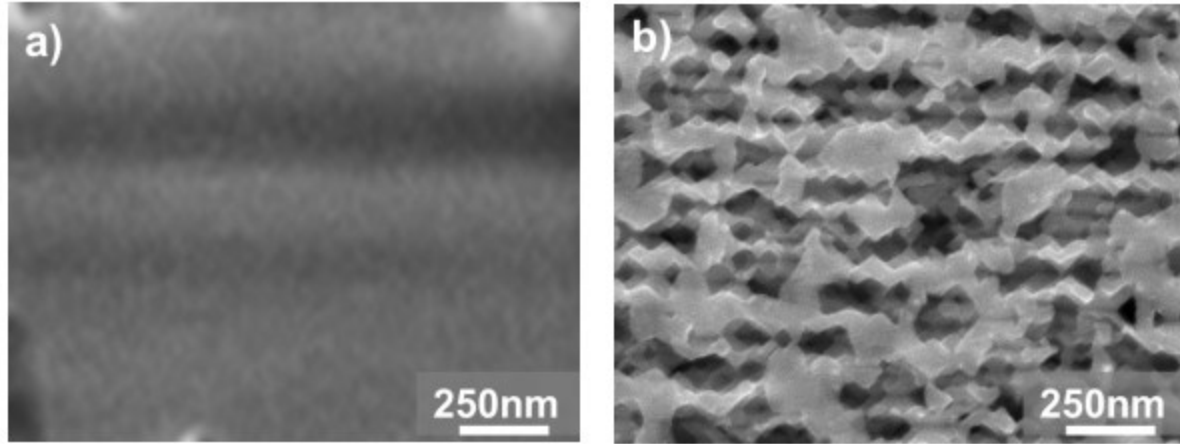


Figure 6.11: Plan view (a) STEM of epitaxial layer and plan view (b) SEM of the porous layer surface prior to deposition at the same magnification.

To avoid any misleading interpretations that come from the drawback of the tiny sampling area of TEM, HRXRD with a 1 mm diameter beam was also applied to characterize the samples. The configuration of the X-ray diffractometer used here is similar to what has been described in Chapter 4.4.2, with an addition of a MaxFluxTM specular mirror to enhance the incident beam intensity [130]. The as-received InP wafer was used as the reference and (004) rocking curve scans were taken using triple axis diffraction (TAD) to check if the processing steps introduce any peak broadening. It can be seen from Figure 6.12 that, the formation of the porous layer does not modify the rocking curve scan until the intensity drops to about 0.1% of the maximum intensity. This little broadening at the tail of the rocking curve scan can be explained by the diffuse scattering from the porous structure [123, 124]. Both annealed and epitaxially deposited samples showed similar extent of the tail broadening after mass diffusion and surface passivation. All four scans have the same full width at half maximum (FWHM) of 11 arcsec [131], which sufficiently confirmed preserved material quality throughout the entire process. The values of other FWXMs are listed in Table 6.1.

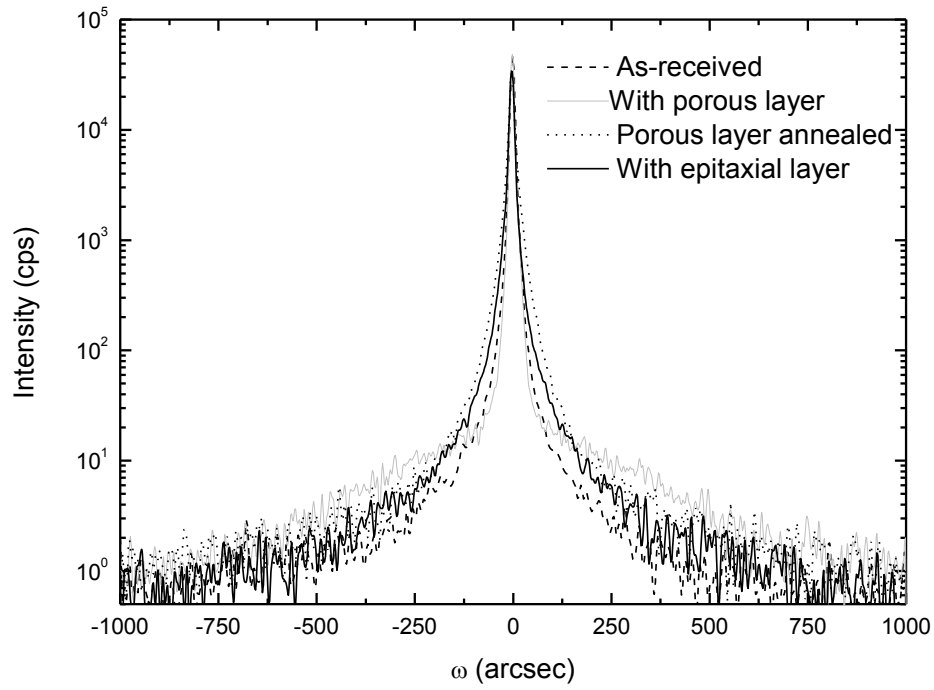


Figure 6.12: TAD 004 rocking curve of bare InP wafer (black dash), with porous layer (grey solid), with annealed porous layer (black dotted) and with epitaxial layer (black solid).

Table 6.1: The list of FWXMs of the rocking curve scans in Figure 6.12.

TAD Rocking curve	FW0.5M	FW0.1M	FW0.01M	FW0.0001M
As-received wafer	11	20	48	353
With porous layer	11	22	42	693
Porous layer annealed	11	25	96	521
With epitaxial layer	11	24	67	537

Chapter 7 Layer transfer via porous InP structure

7.1 Controlled layer splitting

As noted in Chapter 1.2, the two key steps for layer transfer technologies are layer splitting and wafer bonding. These layer transfer technologies are applied under various conditions to engineer the seed substrate, such as ion implantation, essentially aiming to promote the layer splitting step. Spontaneous layer splitting during electrochemical etching of porous material was applied by Zhang to prepare free standing GaN thin films ($> 0.5 \mu\text{m}$) over a macroscopic area ($\geq \text{cm}^2$) [132, 133]. The free standing layers were transferred onto glass slides directly from the electrolyte. However, in this study, the layer splitting process must be compatible with epitaxial growth, so this spontaneous process is not appealing. Therefore, for porous InP samples, our goal is to induce layer splitting in a controlled manner after the epitaxial growth.

In order to control the layer fracture process, it is reasonable to adopt a mechanism to induce the layer splitting whenever needed. Water jet splitting and wedge insertion are all available options, but a better way would be directly by the annealing process. Ideally, if the entire thermal budget of the annealing and the epitaxial growth is known prior to porous layer etching, the porous layer etching can be designed so that the porous structure will be readily fractured after device fabrication.

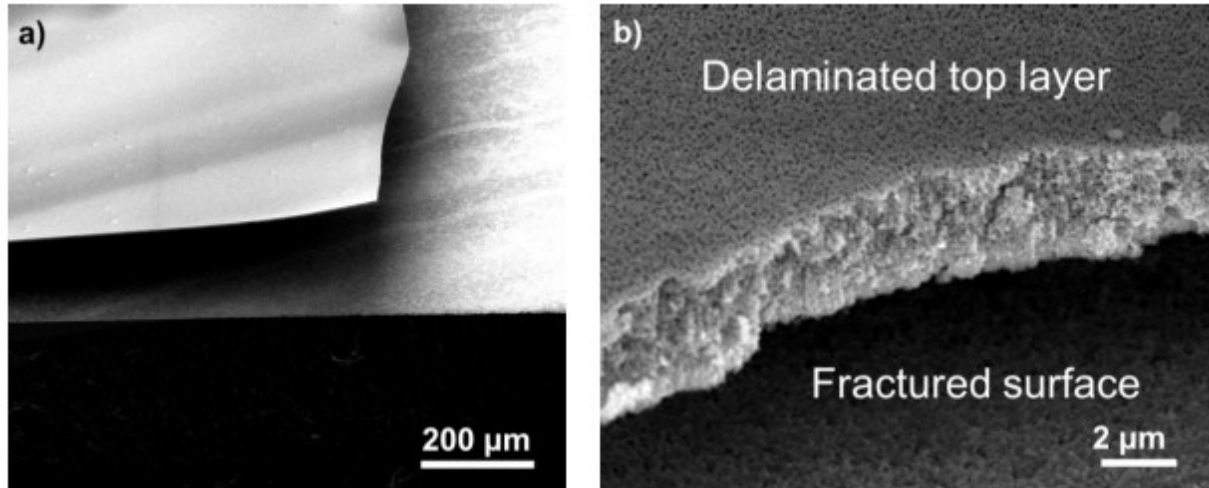


Figure 7.1: SEM images showing the layer splitting on an annealed dual layer structure induced by wafer cleaving. The sample was etched at 25 mA/cm² for 120 sec in 10% HCl followed by a 60 sec etching in 3% HCl at same current density.

Figure 7.1 shows a dual layer sample which edges of the top layer are delaminated from the substrate after 4 hours annealing at 450 °C. The sample was etched with 25mA/cm² in 10% and 3% HCl subsequently. The buried layer did not spontaneously exfoliate during or after the annealing. The delaminated edges were only observed after cleaving the sample in the purpose of revealing cross-section.

7.2 Demonstrations of layer transfer results

Two methods were used to transfer the top layers by fracturing the buried layers in dual layer structures. Different wafer bonding mechanisms were applied: (i) flexible PDMS substrate and (ii) transparent glass substrate. The details of layer transfer process were explained in Chapter 4.3, and the results are presented in this section.

7.2.1 Layer transfer onto PDMS

PDMS was selected because of its wide use as a handle substrate in flexible electronics [134-137]. When the PDMS substrate deposited on the InP and the curing process is complete, the bonding with the InP sample is completed as well. At this stage, peeling off the PDMS layer from the InP sample separates the top layers (e.g. top, more dense porous InP and subsequent epitaxy) through the fracture of the high porosity buried layer, as shown in Figure 7.2(a).

The bond strength between the PDMS and the sample surface must be higher than the strength of the buried porous layer, so that fracture occurs before de-bonding the two substrates. As a result, an entire 2 μm thick film of InP was transferred. So far, no restrictions on the layer size or layer thickness were found when transferring these samples. Figure 7.2(b) is a picture of the transferred InP film on the PDMS substrate.

Larger scale ($> 10 \text{ cm}^2$) transferred films were made on samples etched with a 2” diameter aperture. The major causes accountable for the occasionally less than 100% transfers are (i) insufficient annealing time and (ii) unsuitable porosity, especially at the sample edges (under the O-ring area) where the layer porosity was always lower.

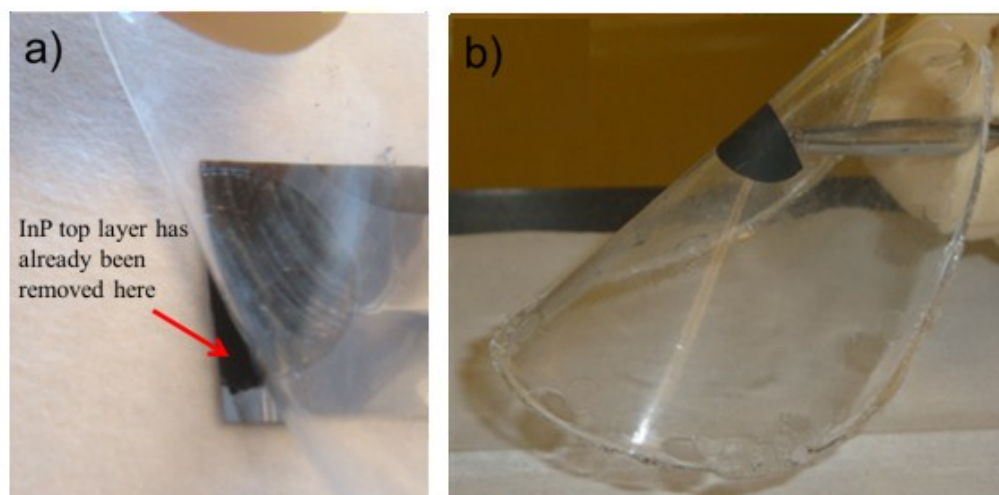


Figure 7.2: Layer transfer of InP thin film ($\sim 2 \mu\text{m}$) onto PDMS substrate.

7.2.2 Layer transfer onto glass substrate

Figure 7.3 shows the results of transferred InP thin films on the glass slides, where the left one of each pair is the transferred film and the right one is the remaining substrate. In a manner that is the same as the PDMS substrate transfer, successful 100% layer transfer was achieved over 1 cm^2 but there do not appear to be any reasons that larger areas could not be transferred.

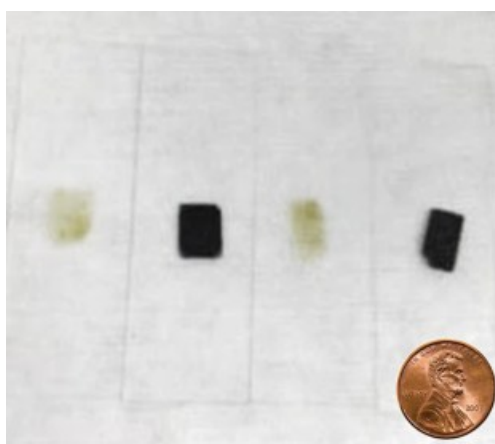


Figure 7.3: Two Layer transfers of InP thin films ($\sim 1 \mu\text{m}$) onto glass slides. The lightly colored areas are the transferred films with 100 nm SiN cap layer. The penny is used as a reference to demonstrate the transferred area is about 1 cm^2 .

Both as-etched and annealed samples were used to perform layer transfer onto glass slides. Take the sample shown in Figure 6.6 for example. The sample was etched with 6 mA/cm^2 in 30% HCl for 180 sec followed by 25 mA/cm^2 in 4% HCl for 60 sec, and then annealed in an N_2 purged chamber at 650°C for 20 min.

The fracture result of the as-etched sample is shown in Figure 7.4(a). The separation between the top glass slide and the InP substrate induced a small portion ($< 40\%$) of the porous layer fracture. However, the rest of the separation was completed by de-bonding between the sample surface and epoxy layer. The magnified cross-section image in Figure 7.4(b) shows similar layer structure as the as-etched cross-section image in Figure 6.6(b), with $1.46 \mu\text{m}$ top layer and $1.31 \mu\text{m}$ buried layer. Note that there was a SiN layer deposited on top of the sample. Judging from the thickness of the remaining layer over the fractured plane as well as the thickness of the porous layer below the fracture plane on the sample edge, the fracture propagated in approximately the middle of the total porous structure, at the interface between the two porous layers. However, similar to what has been found for fracturing a single porous layer [118], the fracture path within the as-etched dual layer sample deviated into the top layer and sometimes even the substrate, and led to poor transfer results. Figure 7.4(c) and (d) are plan-view images of the original top surface and the fractured surface. The fractured surface clearly shows denser pores than the top surface, indicating the fracture plane is within the high porosity buried layer.

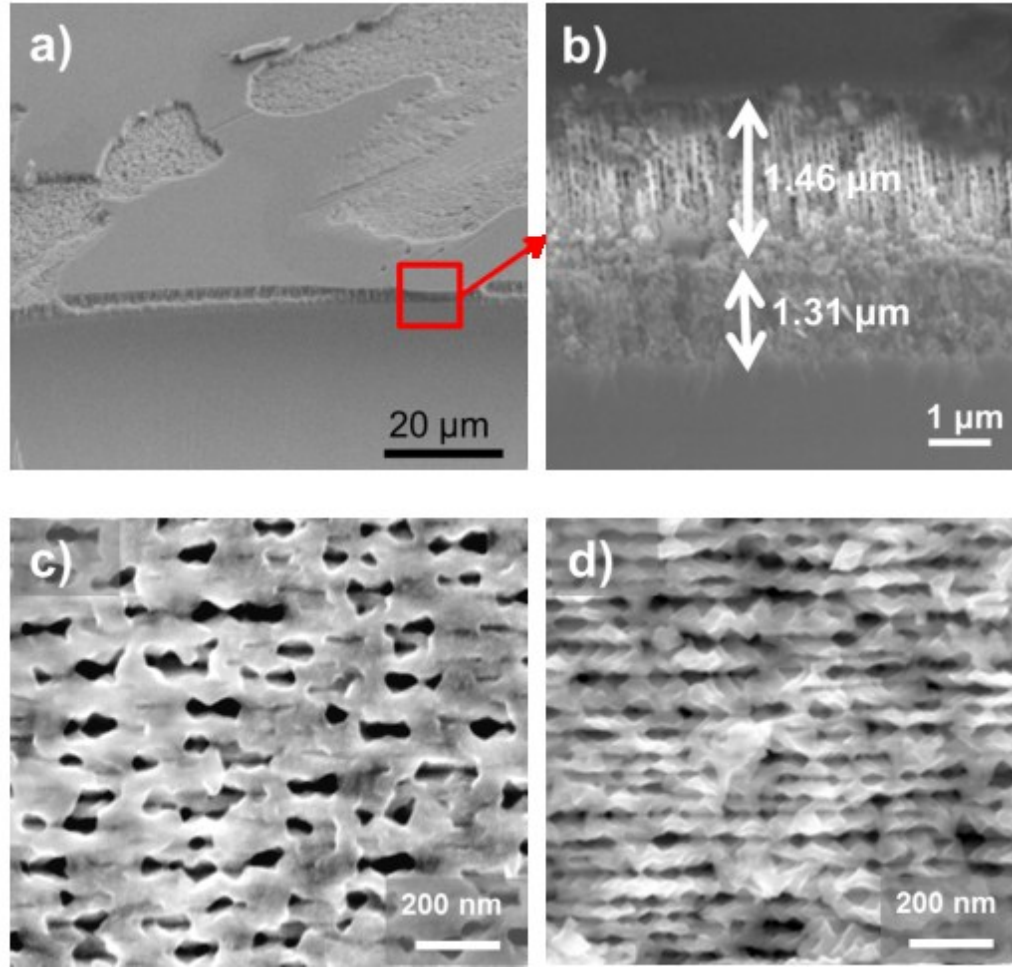


Figure 7.4: Fracture results of an as-etched sample. (a) and (b) are cross-section SEM images taken with 60° tilt with different magnifications. (c) is the plan-view SEM image of the as-etched top surface and (d) is the plan-view from the fractured part on the InP substrate.

Much more successful transfer results were obtained from the annealed samples. After 20 min annealing at 650 °C, the porosity of the buried layer increased from 53% to 75% (Chapter 6.1), indicating lowered mechanical strength of the porous layer. Figure 7.5(a) is the SEM image showing 100% layer transfer from the annealed sample. The diagonal black lines extended in the same direction as the propagation of fracture, and they were found to be tiny ridges less than 2 nm high. At the sample edge, the thickness of the remaining porous layer was measured to be

1.27 μm (Figure 7.5(b)), more or less the same as the thickness of the buried layer. The plan-view comparison (Figure 7.5(c) and (d)) between the annealed layer surface and the fractured surface further confirmed that the fracture plane is within the high porosity layer. Also, the porosity value obtained from the fractured surface is 73%, consistent with the quantification result (75%) from the cross-section image.

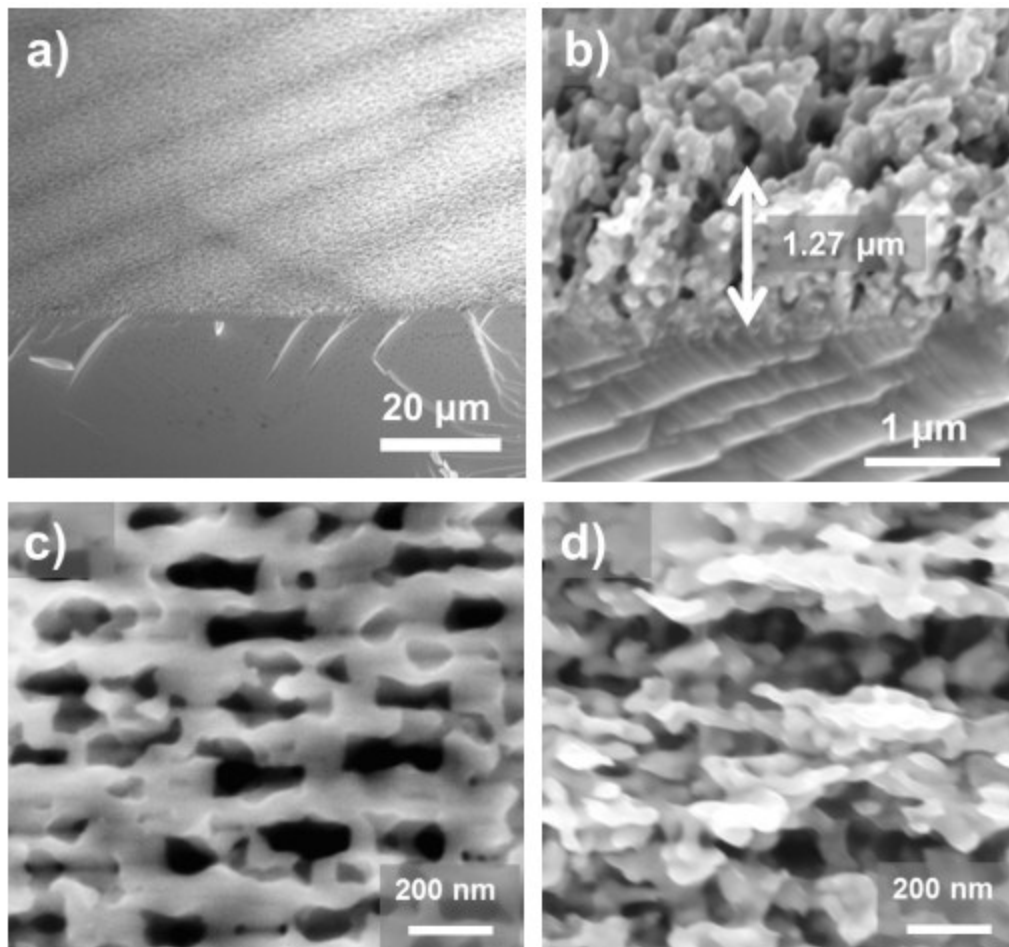


Figure 7.5: Fracture results of an annealed sample. (a) and (b) are cross-section SEM images taken with 60° tilt with different magnifications. (c) is the plan-view SEM image of the annealed top surface and (d) is the plan-view of the fractured surface.

7.3 Surface finish with chemical mechanical polishing

The last step of this layer transfer process is porous layer removal of the original substrate by chemical mechanical polishing (CMP), in order to reuse the seed substrate and allow further processing on the transferred structure.

Figure 7.6(a) shows an as-etched dual layer sample which top layer was mostly exfoliated due to spontaneous splitting. The remaining fractured surface was used to perform polishing for the porous structure. Citric acid and sodium hypochlorite were applied alternatively onto the polishing pad for the so-called abrasive free polishing [107,108]. Slight pressure (8 kPa) was applied for the first 20 min of polishing since high polishing rate is needed to quickly remove the porous layer without worrying too much about the surface roughness yet. The AFM scan of a $40 \times 40 \mu\text{m}^2$ area after 20 min polishing is shown in Figure 7.6(c). No satisfying AFM scans were obtained prior to the polishing process due to high roughness of the fractured surface. In Figure 7.6(c), a few ($< 10^6 \text{ cm}^{-2}$) 1 or 2 μm diameter pits are still visible on the sample surface, resulting in a surface roughness of 108 Å, but the porous layer is basically gone. According to Ref [107], the roughness of InP samples can be reduced to lower than 10 Å by abrasive free CMP at 4 kPa, and reducing the RMS roughness from 100 Å to 7 Å requires about 80 min at this pressure. Therefore, an additional 60 min polishing at 4 kPa was applied on the same piece and a roughness as low as 6 Å was obtained (Figure 7.6(d)). Figure 7.6(b) is a photographic image of the sample after 80 min polish. No discernable difference can be made between the original porous region and the un-etched area. The remaining features on the surface came from the O-rings contamination, and can be later removed by organic solvents.

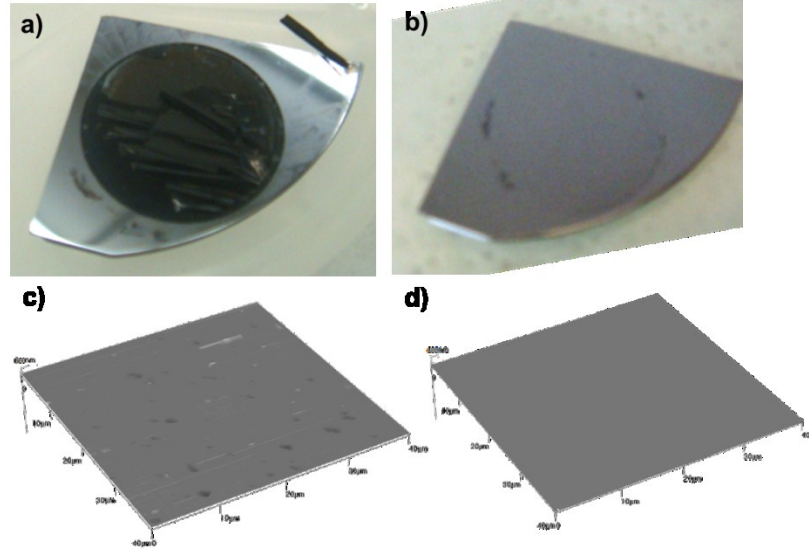


Figure 7.6: Chemical mechanical polishing results of fractured porous InP substrate. a) Photograph of the as-etched sample with the top layer readily exfoliated; b) Photograph of the sample after 20 min polishing at 8 kPa (step 1) plus 60 min polishing at 4 kPa (step 2); c) AFM of the porous surface after step1, showing a RMS roughness of 108 Å; d) AFM of the porous surface after step 2, showing a RMS roughness of 6 Å.

Chapter 8 Conclusion and future work

This study addressed the feasibility of employing porous InP for the fabrication of heterogeneous integrated system by the cleave engineered layer transfer technique. The similar concept has been employed by ELTRAN with porous Si, but not yet used on III-V semiconductors. The current layer transfer technologies for III-V layer transfers either suffer from slow processing (ELO) or layer damage (smart cut), while the method in this study proved to be an efficiency way to transfer high quality epitaxial structures with good reproducibility. Electrochemical etching prepares porous InP layers with controllable porosity and these porous structures are capable of fracture after annealing and epitaxial growth under controlled conditions. The seed wafers used for porous layer formation and epitaxial growth remain intact after surface smoothing with only a few microns material loss during the layer transfer process, so that multiple layer transfers are attainable to save substrate cost.

8.1 Porous InP layer fabrication

Porous InP layers with porosities ranges from 15% to 90% were fabricated by electrochemical etching. The morphology of the porous layers is found to be strongly dependent on the current density and electrolyte concentration, so that dual layer structures were prepared by successive etching with different recipes. In this case, the top layer is of lower porosity than the buried layer. The surface roughness was successfully lowered to less than 5 nm RMS ($40 \times 40 \mu\text{m}^2$ AFM) by reducing the pore size and pore density. The mechanical properties of the porous layers are represented by the Young's modulus measured by nano-indentation, which showed a quartic dependence on the layer density. Therefore, the high porosity buried layers in the dual layer structure are expected to have lower mechanical strength and are essentially where

the fracture initiates during layer splitting. Compressive out-of plane strains were found in as-etched samples but would gradually evolve away during the annealing process by surface passivation. The porous layers with preserved single crystallinity and slight phosphorus rich composition provide the prerequisites for high quality epitaxial layer growth.

8.2 Porous InP annealing and epitaxial growth

Upon annealing between 450 °C and 750 °C, the porous InP structure undergoes a morphology change driven by the surface energy reduction. Although full surface coalescence has not yet been achieved with porous InP annealing, smoother surfaces with stable flat surface ratio were realized with appropriate annealing conditions. More importantly, the annealing process is responsible to the formation of large voids within the porous layer and to the increased porosity of the buried layer. That is to say, by combining an annealing condition with a suitable porous structure, it is possible to calculate by how much the mechanical strength has been lowered due to the annealing process and perform controlled fracture of the porous layer accordingly.

In addition, despite of the porous features, fully coalescence epitaxial layers were grown on the porous InP substrates. Neither threading dislocations nor grain boundaries were found on pv-TEM sample area over 35 μm^2 , indicating a defect density of less than $3 \times 10^6 \text{ cm}^{-2}$. The high crystallinity of the epitaxial layer was also confirmed by HRXRD, which showed an equal FWHM as the as-received substrate in (004) rocking curve scans.

8.3 Layer transfer

Layer splitting using a dual porosity structure were achieved in two ways to demonstrate the potential of layer transfer applications. By bonding with flexible substrates such as PDMS,

the thin films above the high porosity buried layers were easily peeled off from the InP substrate, provided that the mechanical strength of the buried layers have been sufficiently weakened during the annealing process so that the layer fracture can occur prior to the de-bonding of the substrates.

Both as-etched and post annealed dual layer samples were tried with glass handle substrates. Without annealing, the transferred area was much smaller ($< 40\%$) compared to the 100% transferred area of the annealed samples. All fractures happened in the buried layers, judging from the high porosity feature on the fractured planes. The remaining porous layers were polished away by abrasive free CMP and achieved good surface roughness ($< 10 \text{ \AA}$), making the substrate ready for reuse.

8.4 Future work

The suitability of epitaxial device growth and device transfer onto foreign substrates has been demonstrated, but the actually devices have yet to be made to test whether the device performance can be preserved after the layer transfer process. Also, since this study focused on only two variables, which are electrolyte concentration and current density, to change the porous layer morphology, more interesting results might be obtained by varying the substrates' doping concentration and illumination conditions during the etching process. Besides, other than InP, porous GaAs, porous GaN, and porous GaP have all been successfully fabricated with electrochemical etching, and they all share some common features as porous InP. Therefore, the extension of the layer transfer method introduced in this work onto other III-V substrates is a promising path to enable more flexibility of heterogeneous device fabrications.

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