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Two-Dimensional, Individually-Addressable Nanostructure Arrays

by

Chu-Yeu Peter Yang

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Mechanical Engineering

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Liwei Lin, Chair

Professor Lydia Sohn

Professor Oscar D. Dubon

Spring 2010

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by Chu-Yeu Peter Yang

Abstract

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Assembly and integration of vertically-oriented, one-dimensional nanostructures into a two-dimensional array platform has been demonstrated. This 2D architecture is realized using top-down semiconductor and microelectro-mechanical system (MEMS) processes as well as bottom-up catalyst-assisted 1D nanostructure synthesis methods. Two prototype demonstrations include: (1) a 15×12 carbon nanotube (CNT) array and (2) a 2×5 ZnO nanowire array systems.

Arrays based on CNT structures have been developed to verify the feasibility of the 2D architecture using vertically-oriented nanostructures. A trench process is conducted by dry etching into a silicon substrate. A CNT growth process follows to fill the trenches while top electrodes are defined by metallization with a shadow mask. Measurement results show that the average resistance value from the 15×12 CNT electrodes with a contact area of $500 \times 400 \mu\text{m}^2$ was several tens of ohms. To get a better understanding for the electrical characteristics of the as-fabricated CNT structures, a single $1 \mu\text{m}$ -long CNT sample with measured diameter of 30 nm was attached to two nanoprobe tips inside a scanning electron microscope. Its resistivity was characterized as $0.056 \Omega\text{-m}$ and the overall resistance value of the CNT nodes in the 2D array was estimated at 41Ω . This result correlates well with measured resistance values from the CNT nodes, suggesting that there are successful electrical connections between the top and bottom electrodes through the CNT bundles.

Individual-addressability of the 2D architecture has been enabled by replacing the metallic CNTs with semiconducting ZnO nanowires and creating rectifying, Schottky diodes at the array nodes. A 2×5 array featuring asymmetric bottom platinum-nZnO Schottky junctions and top nZnO-titanium/gold ohmic contacts was fabricated. ZnO nanowires were first synthesized atop of metal electrodes on a silicon substrate. After applying spin-on-glass, the tips of the nanowires were exposed by plasma etching and top metal electrodes were deposited. The I-V characteristics of a $150 \times 500 \mu\text{m}^2$ node under forward and reverse biases with and without a $40 \mu\text{m}$ -wide UV laser beam were tested. It is found that a photogenerated current is detectable from the 2D array with an estimated responsivity of $3 \times 10^{-4} \text{ A/W}$. Moving the laser beam to neighboring nodes did not result in an increased current from the interrogated node, demonstrating the individual-addressability of the 2D ZnO nanowire array and its capability for discrete pattern recognition as a UV photodetector.

This marks the first successful demonstration of vertically integrating ZnO nanowires into an individually-addressable 2D array for possible ultrahigh-density applications in nanoelectronic memory, information displays, photodetectors, and nano-lithography.

To my lovely wife, Elaine, and our dearest family and friends.

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ACKNOWLEDGMENTS

The pursuit of my degree began when Elaine first joined Sandia National Laboratories in Livermore and attended an infosession for the Doctoral Studies Program one afternoon. Although I had been thinking of participating, I never had the motivation to follow through and seriously consider going back to school again. When I found out she was also considering going back to school within a few years, I immediately embraced the idea whole-heartedly for some reason. After applying for the program and being accepted after a few major hurdles, my academic journey back at U.C. Berkeley resumed after almost 10 years from my undergraduate studies and the rest is history. I am therefore greatly appreciative of the opportunity and financial support that the Sandia Doctoral Studies Program has provided me over the last three years. I also want to thank Elaine for starting me on this journey and for her continued support and push towards its conclusion.

My research interest and direction were brought on by Alec Talin, a knowledgeable and resourceful research scientist at Sandia who was the PI of the “Discovery Platform for Nanowire Electronics and Photonics” project on which I was a contributing member. His inputs and novel ideas towards my research and experiments are greatly appreciated.

I also want to thank Professor Liwei Lin, my research advisor, for giving me the opportunity to join his MEMS/NANO group and pursue my degree at Berkeley. I am grateful for the independence that I was given, as well as his assistance and guidance whenever they were needed. Fellow students in the LinLab family also provided many valuable discussions and process-development pow-wows that have helped me tremendously along my journey. Many thanks to all.

CHAPTER 1 – INTRODUCTION

1.1 Significance and Motivation

The semiconductor industry has been systematically decreasing the feature size of silicon transistors and increasing the computing power of integrated circuits (IC) in an exponential fashion such that every two years the number of transistors per unit area will double according to the widely-adopted Moore's Law [1]. Many challenging problems arise such as quantum tunneling through the gate oxide, short-channel effects, increasing power consumption, as well as the exponential increase in IC manufacturing costs [2]. In order to overcome the obstacles associated with silicon IC technology, many research groups have developed nanoscale devices based on nanostructures for the possibility of replacing the traditional silicon transistors.

Nanostructures, defined as materials with at least one dimension measuring in the range of 1 to 100 nm, are classified according to their dimensionality [3]. For example, zero-dimensional (0D) nanostructures include spherical nanoparticles and quantum-dots. The small size of these 0D-nanostructures leads to the quantum confinement of electrons and holes in all three dimensions in the material and results in different electrical and optical properties from their bulk counterparts. Cadmium selenide nanocrystals/quantum-dots have been utilized as active elements in single-electron transistors [4] while indium arsenide quantum dots have been demonstrated as room-temperature optical memory storage devices [5].

One-dimensional (1D) nanostructures, such as nanotubes, nanorods, nanowires, and nanobelts, have two quantum confinement directions in the radial dimension. The remaining, unconfined direction along the axial dimension has been shown to exhibit ballistic electron transport for single-walled carbon nanotube-based field-effect transistors [6]. Single-crystal silicon and gallium nitride semiconducting nanowires have been used as nanoscale building blocks to form logic gate structures for future nanoelectronic systems [7].

Two and three-dimensional (2D, 3D) nanostructures, lastly, are assemblies of lower-dimensional building blocks that form higher-level structures such as 2D fiber-layer films and 3D bulk matrices [3]. The direct, systematic assembly and integration of nanoscale building blocks into functional devices and systems, however, are formidable challenges in the field of nanoscale science and technology. In order to bridge the length scales between the nanoscopic, microscopic, and mesoscopic domains, many research groups are figuring out ways to construct micro-to-nano contacts with nanostructures. This necessitates the precise placement and configuration of the nanoscale building blocks. Some of these techniques use electric fields [8], magnetic fields [9], contact printing [10], microfluidic channel flows [11], or the Langmuir-Blodgett alignment technique [12] to orient and control the placement of nanowires to form planar, 2D hierarchical devices. Because these assembly processes are often time-consuming and hard to scale up for the mass production of inexpensive devices, the precise placement and configuration of nanoscale building blocks at the desired location will need to be incorporated into the overall systems design and fabrication flow similar to the IC manufacturing process.

The goal of the research presented in this dissertation is to address the issue of assembly and integration of one-dimensional nanoscale building blocks into functional devices and nanosystems. Specifically, a two-dimensional and individually-addressable nanostructure array is proposed by directly integrating vertically-oriented 1D nanostructures into the device platform during the overall device fabrication flow, without the need for post-growth assembly processes. Utilizing the 2D individually-addressable nanostructure array platform together with the vertical-

integration of 1D zinc-oxide nanowires, ultra-violet (UV) photodetection was demonstrated with discrete 2D pattern discrimination. A two-dimensional photodetector array based on the vertical-integration of individually-addressable zinc-oxide nanowires, to the best of the author's knowledge, has not been demonstrated as photodetector devices. Before the details of the present research are introduced, some of the most state-of-the-art assembly and integration methods for 1D nanostructures are presented.

1.2 Literature Review

1.2.1 Current Nanostructure Assembly and Integration Methods

Planar Assembly and Integration Methods

Many research groups have devised various integration and assembly methods to create innovative nanoelectromechanical systems (NEMS) with one-dimensional nanostructures. These methods, briefly introduced in Section 1.1, utilize electric fields [8], magnetic fields [9], contact printing [10], microfluidic channel flows [11], or the Langmuir-Blodgett alignment technique [12] to orient and place nanowires in specific arrangements to form planar 2D hierarchical devices and functional systems. The two assembly strategies that are most-capable of parallel, large-scale integration of nanostructure building blocks into complex systems are the Langmuir-Blodgett and contact printing techniques.

The solution-based Langmuir-Blodgett (LB) approach for the bottom-up assembly of nanoscaled building blocks is capable of controlling the organization and hierarchy of 1D nanowires or nanotubes over large areas across a number of different substrates. The 1D nanostructures being assembled with this flexible LB technique could be made of virtually any material and synthesized from any growth processes [13]. The 1D nanostructures are first diluted and dispersed into a solvent solution to make a stable colloid. This solution is then deposited onto the liquid surface in a Teflon-coated Langmuir-Blodgett trough (Figure 1-1), resulting in a film of nanostructures (dark blue region) at the air-water interface. While monitoring the surface pressure with a Wilhelmy pressure sensor, the mobile barriers are moved to compress the film controllably to form a monolayer of uniaxially-aligned nanostructures with the desired density.

At the onset of film compression where the surface pressure is low, individual 1D BaCrO₄ nanorods have been shown to form groups of three to five nanorod aggregates (Figure 1-2a) while a uniform layer of parallel, aligned nanorods results from further film compression (Figure 1-2b) [13]. Once it reaches the desired density, this monolayer of aligned nanostructures is transferred to a substrate by a Langmuir-Schaeffer horizontal lift technique in which a substrate is brought into contact with the monolayer film horizontally, inclined to approximately 10°, and moved up away from the liquid surface [14]. This one-step process results in parallel

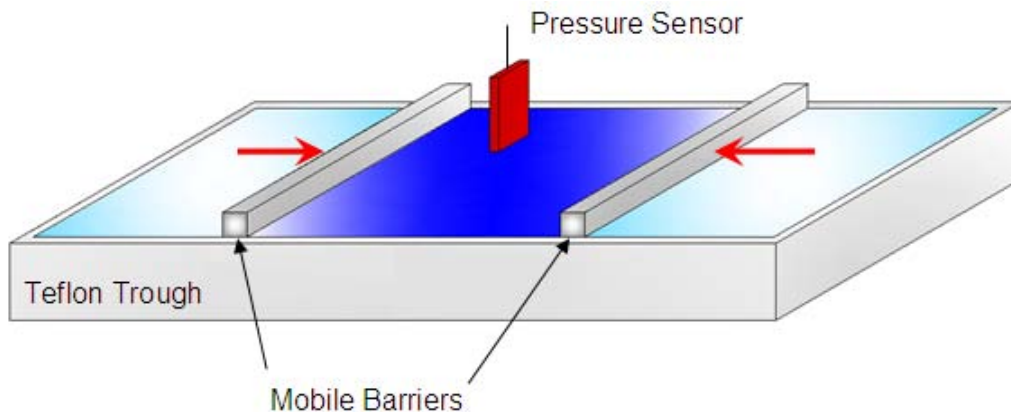


Figure 1-1. Illustration of the Langmuir-Blodgett trough. Red arrows show the uni-directional compression of the nanostructure-dispersed film (dark blue) by the mobile barriers.

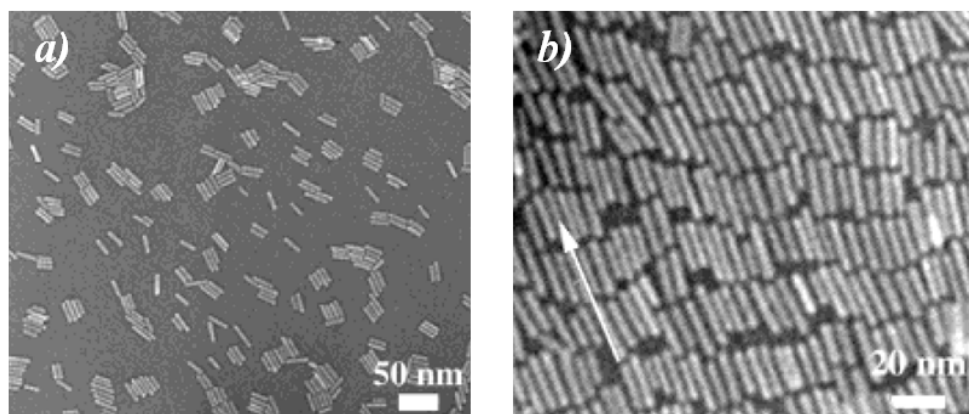


Figure 1-2. TEM images of BaCrO₄ nanorod assemblies at the water-air interface. *a)* Aggregates of nanorods at the onset of compression, *b)* uniform layer of aligned, parallel nanorods resulting from further compression [13].

1D nanostructures across the entire substrate surface. Standard photolithography processes could then be used to cover the substrate with photoresist and pattern arrays of planar devices such as field-effect transistors with single-crystal silicon nanowires (Figure 1-3b,c) [15]. The nanowires uncovered after photoresist development and outside of the pattern area are subsequently removed by sonication, leaving periodic arrays of aligned nanostructures with predetermined dimensions and spacing (Figure 1-3a). This sequence of steps could finally be repeated with nanostructures made of different materials and in varying orientations to form functional and integrated nanosystems.

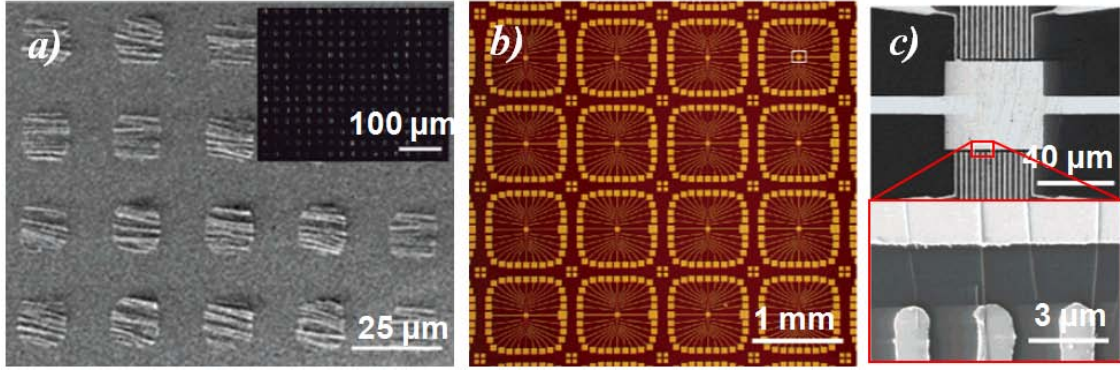


Figure 1-3. Periodic arrays of parallel silicon nanowires fabricated by the Langmuir-Blodgett method and photolithography. *a)* SEM images of $10\ \mu\text{m} \times 10\ \mu\text{m}$ nanowire assemblies, while inset is a large-area, dark-field optical image of the pattern [12]. *b)* Optical and *c)* SEM images of patterned metal electrode arrays over silicon nanowires to form field-effect transistors [15].

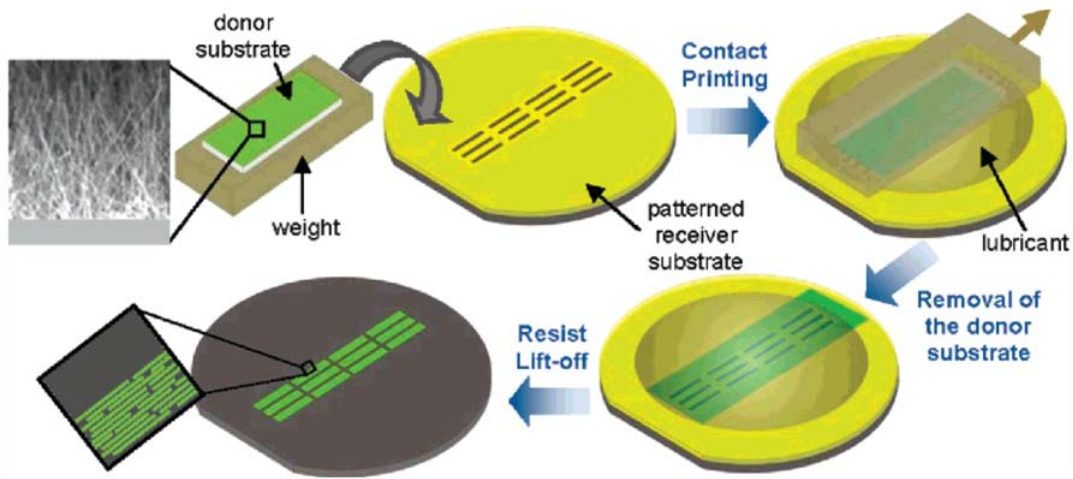


Figure 1-4. Process flow for the direct contact printing of aligned nanostructures [17].

Contact printing is another method capable of assembling one-dimensional, nanostructured building blocks into complex, functional devices and adaptable to the parallel, large-scale integration for the economic VLSI production of nanosystems. This printing process, presented in Figure 1-4, involves the unidirectional sliding of an as-grown, nanostructure-covered growth substrate over a device substrate that is pre-patterned with photoresist structures. Similar to the solution-based Langmuir-Blodgett (LB) assembly, the contact printing method is based upon the transfer of 1D nanostructures from the growth substrate to the device substrate [16]. Instead of dispersing the nanostructures into a LB trough and controlling their spacing or density by surface compression and pressure controls, density control in contact printing is achieved during the nanostructure synthesis step (germanium nanowires in this example) on the “donor” substrate by controlling the surface density of the catalytic nanoparticles from which the nanostructures are grown via the vapor-liquid-solid (VLS) process. A typical surface density

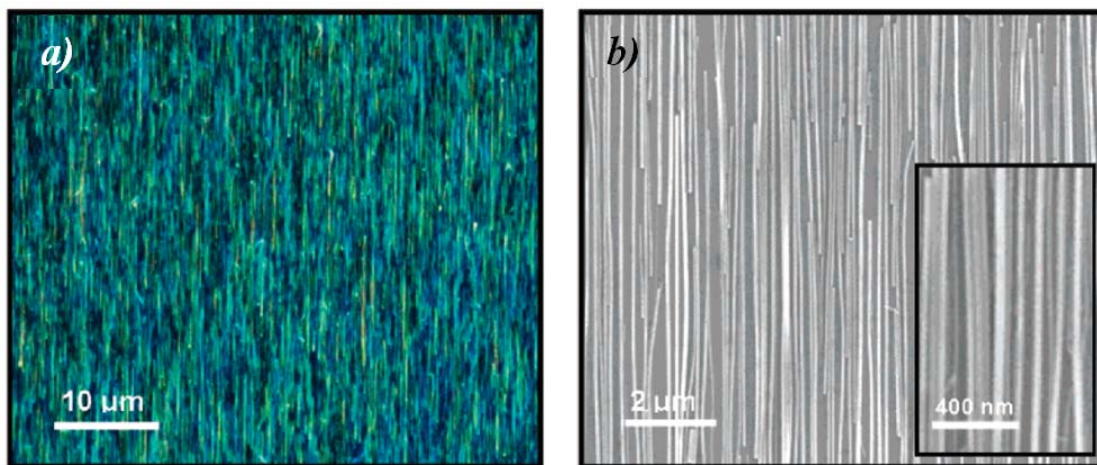


Figure 1-5. a) Dark field optical and b) SEM images of germanium nanowires after contact printing on an oxide-coated Si wafer [17].

value for the mono-dispersed gold nanoparticles is approximately $20 \mu\text{m}^{-2}$, which results in approximately eight aligned Ge nanowires (NWs) per micrometer after the printing process as shown in Figure 1-5 [17].

In order to have strong as-grown nanowire-to-substrate interaction and efficient nanowire transfer, the “receiver” device substrate requires additional surface chemical modifications. Device substrates coated with a monolayer of $-\text{CF}_3$ terminations are shown to result in poor Ge nanowire transfer from the growth substrate (less than 10^{-3} NW/ μm) due to the hydrophobic, “non-sticky” nature of the fluorinated surfaces. Device substrates coated a monolayer of $-\text{NH}_2$ or $-\text{N}(\text{Me})_3^+$ terminations, on the other hand, yield highly-dense NW transfers (approximately 8 NWs/ μm) due to the strong van der Waals interactions with the nanowire surfaces [17]. After surface chemical modification, a photolithography step is performed on the receiver substrates to define the device and assembly patterns.

Once the nanostructure growth and receiving device substrates are prepared, the device substrate is covered with a lubricating mixture of octane and mineral oil and brought into contact with the growth substrate. The contact printing process then proceeds by the uni-directional sliding of the growth substrate (covered with as-grown nanostructures) over the device substrate with patterned photoresist structures via a micro-manipulator. The nanostructures are, in effect, pulled off from the growth substrate as they become attached to the chemically-modified surfaces of the device substrate through strong van der Waals interactions, resulting in the direct printing of aligned nano-structures. The nanostructures outside of the targeted device regions are removed during the photoresist lift-off process, while metal contacts to the 1D nanostructure devices are finally fabricated with another photolithography step. Field-effect transistors based on single and multiple nanowires were successfully fabricated with the contact printing process (presented in Figure 1-6a). This assembly strategy could also be repeated several times after the deposition of insulating oxide buffer layers, with contact-printed device layers stacked vertically on top of each other to form 3D multi-functional electronics (shown in Figure 1-6b) [16].

The flexibility of the direct contact printing and the solution-based Langmuir-Blodgett (LB) assembly methods is what differentiates them from other strategies as a viable approach for the large-scale organization of 1D nanostructures into integrated systems. Because these

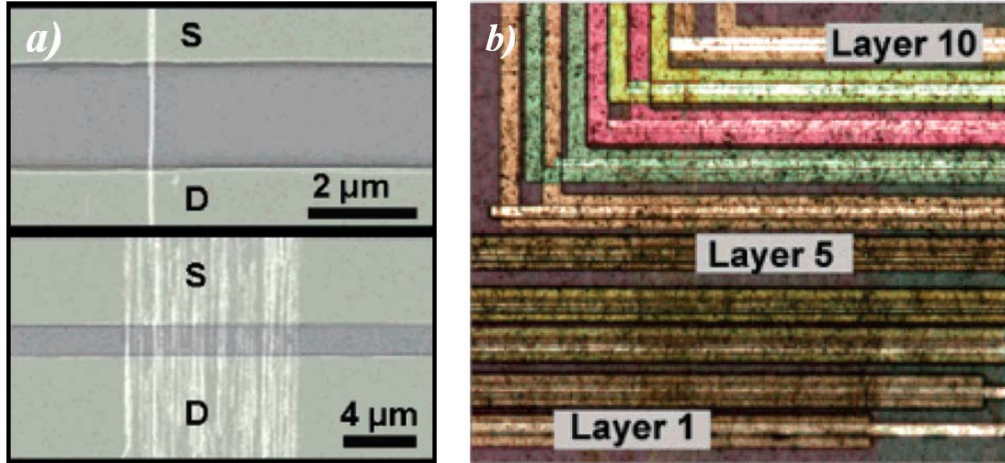


Figure 1-6. Optical images of *a)* FETs based on single and multiple Ge NWs spanning the source (S) and drain (D) electrodes [18], and *b)* 3D nanowire FETs formed with 10 stacked layers contact-printed devices [16].

assembly processes are independent of other device fabrication steps, the contact printing and LB method could be repeated many times with controlled orientations to yield highly-complex, multi-layered nanostructure device architectures. These independent assembly processes also open possibilities for new substrate materials beyond traditional semiconductors, including flexible plastic membranes such as Kapton, since they involve only low-temperature assembly and fabrication steps and are separate from the high-temperature, VLS nanostructure synthesis step. Their ability to handle 1D nanostructures made of different materials also contributes to the flexibility and attractiveness of the contact printing and LB methods for the integration of nanoscale building blocks into functional nanosystems. Contact printing, however, has a slight edge over the Langmuir-Blodgett method due to the fact that it is capable of transferring the small-diameter (less than 15 nm) nanowires that are problematic for the LB technique [16].

The contact printing and solution-based Langmuir-Blodgett (LB) assembly methods for large-scale organization of 1D nanostructures into integrated systems suffer from several drawbacks. These strategies for organizing nanostructures are inherently assembly processes that requires multiple, time-consuming steps to integrate the patterned layers into functional devices. The 1D nanostructure synthesis is separate from the LB organization process and requires extra transfer procedures to remove the as-grown nanostructures from the growth substrate and disperse them into the Langmuir-Blodgett trough. The uniaxial compression of the 1D nanostructures in the LB trough is also another complicated organization process that requires extensive surface pressure monitoring, precise barrier movement control, as well as the expensive LB trough system itself (which could cost upwards of \$15k or more [18]). As evidenced by the images of Figure 1-3, the precise separation and location of each individual nanostructure are hard to achieve, leading to approximately 80% of the 3000 possible electrodes (Figure 1-3b) being successfully connected to the nanowires for the fabrication of field-effect transistors [15].

Although the as-grown 1D nanostructures are directly transferred onto the device substrate in the contact printing method, the receiving substrate requires surface chemical modification treatments that constitute additional steps to the overall assembly process. The

effectiveness of these surface treatments on other substrate materials, besides the demonstrated Si/SiO₂ examples, is also unknown and requires additional optimization and tuning for each substrate material. Since the degree of nanostructure-to-substrate interaction governs the detachment and transfer of nanostructures from the growth substrate to the device substrate and varies across the samples, the locations where the nanostructures break is not controlled precisely. The length of the printed nanostructures, therefore, is not well-controlled.

Single-element field-effect transistors based on 1D nanowires were successfully fabricated following the Langmuir-Blodgett organization and contact-printing transfer processes, using electron-beam lithography to pattern a series of metal electrodes that contacted nanowires in parallel arrays. This lithographic process, however, is a serial, time-consuming process that is unsuitable for large-scale integration and production of functional, highly-complex nanosystems.

Vertical Assembly and Integration Methods

Unlike the planar assembly and integration strategies detailed above, the vertical integration of one-dimensional nanostructures into innovative nanoelectromechanical systems (NEMS) incorporates the nanostructure synthesis and assembly steps directly into the device fabrication process. This not only eliminates the need for time-consuming assembly processes and their associated complexities, but also presents the possibility for vertical devices with ultra-high packing density as well as their manufacture at the industrial VLSI scale. These vertical integration schemes usually involve predefining the features into which the 1D nanostructures will be integrated, either by photolithography [19], electron-beam lithography [20], or by anodically-etched porous aluminum oxide membranes [21], to name a few. One such vertical integration method that has the potential for large-scale integration of 1D nanoscale building blocks into functional nanosystems, detailed in Figure 1-7, combines traditional top-down semiconductor processing techniques with the bottom-up synthesis of epitaxial silicon nanowires [19].

First, a silicon-on-insulator (SOI) wafer (Figure 1-7a) is structured by photolithography, reactive-ion etching (RIE), and wet buffered hydrofluoric acid (BHF) etch to form a cantilevered silicon beam (Figure 1-7b). Gold nanoparticles measuring 80 nm in diameter are then introduced in solution to the etched structure and directed below the silicon beam by a dielectrophoretic, electric field-assisted assembly process (Figure 1-7c). Silicon nanowires are subsequently grown from the gold nanoparticle catalysts via the vapor-liquid-solid (VLS) synthesis process in a chemical vapor deposition chamber at 500°C (Figure 1-7d). An atomic layer deposition (ALD) process is used to coat the nanowires with aluminum oxide and platinum to form the gate structures surrounding the nanowires, while the platinum gates are finally patterned and structured by photolithography and wet etching in an aqua regia solution to complete the vertical surround-gated silicon nanowire field-effect transistor devices (Figure 1-8).

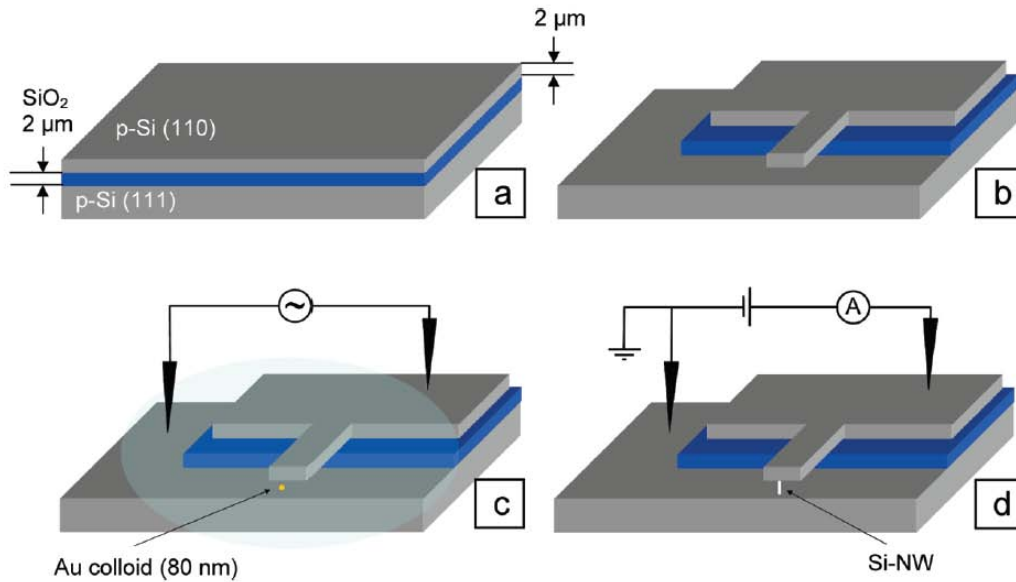


Figure 1-7. Fabrication process flow for the vertical integration of silicon nanowires [19].

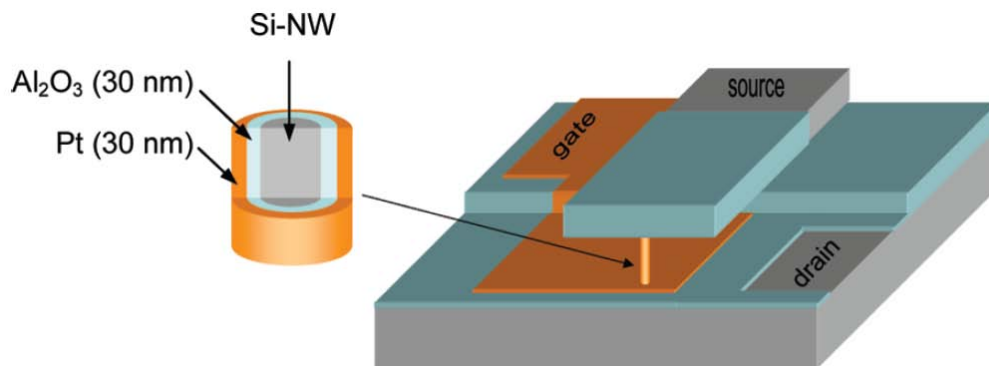


Figure 1-8. Schematic of the silicon nanowire FET structure formed between the cantilever beam and the substrate, showing the surround oxide and gate layers on the nanowire [19].

The direct vertical integration and self-assembly of 1D nanostructures into the designed hierarchical structure detailed above is an attractive process capable of creating large arrays of functional devices. The conventional IC manufacturing processes used in this device fabrication method are highly parallel in nature and are capable of being scaled across the entire wafer. Figure 1-9 illustrates this capability by presenting a scanning-electron microscope image of vertical silicon nanowires integrated into an array of 20 pre-fabricated electrodes. Because the gold nanoparticle locations are rationally pre-determined, the nanostructures could be grown directly from the catalysts in a designed configuration and terminated automatically on the overhanging surface of the cantilever structures. No post-nanowire growth assembly and

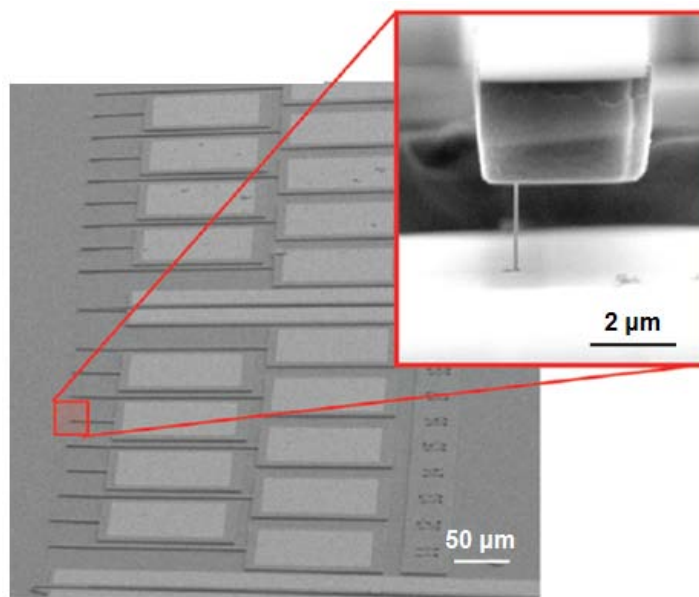


Figure 1-9. Parallel integration of vertical silicon nanowires into an array of 20 electrodes [19].

fabrication procedures are required to align the nanostructures and form electrical contacts. Reproducibility in performance of the nanowire-based FET is also an important quality-assurance criterion for the large-scale production of integrated nanosystems. This could be affected by the channel length of the nanowire FETs, which is highly-uniform since it is determined by the cantilever-to-substrate separation and is in turn governed by the thickness of the high-quality buried oxide in the SOI wafer itself.

This direct integration strategy for the self-assembly of 1D nanostructures into pre-fabricated structures suffers from a few drawbacks. The dielectrophoretic deposition process of gold nanoparticle catalysts to the area directly below the overhanging cantilever is not well-controlled, resulting in single or multiple nanoparticles being deposited. Single-element FET devices are, therefore, problematic to fabricate reproducibly across large wafer scales. Because the 1D silicon nanowires are synthesized directly on the device substrate with a relatively high-temperature VLS growth method, the material suite available for the device structure excludes inexpensive, flexible plastic substrates. The fabrication steps and device architecture of this integration method are also highly specific to field-effect transistors and are, therefore, not flexible enough to accommodate the co-location of other devices with different functionalities such as light-emitting diodes or photodetectors on the same substrate.

The versatile, two-dimensional (2D) nanostructure array architecture and fabrication processes presented in this dissertation share similar advantages to the various assembly and integration methods detailed above. The drawbacks of the proposed 2D architecture and fabrication processes, similar to the vertical assembly method above, include the high-temperature, VLS nanostructure synthesis method that may raise the overall thermal budget of the device manufacturing, as well as the limitation to the type of high-temperature substrate materials that could be introduced to the VLS growth chamber. The research overview presented in the following section will describe the advantages of the proposed 2D nanostructure array in detail.

1.3 Research Overview

1.3.1 2D Individually-Addressable Nanostructure Array

The work presented in this dissertation introduces a versatile, two-dimensional (2D) nanostructure array fabrication process and architecture that directly integrates one-dimensional nanoscale building blocks into the device platform without the need for time-consuming assembly procedures. A schematic of the proposed 2D nanostructure array is presented in Figure 1-10, illustrating vertical 1D nanostructures integrated between top and bottom electrodes.

For semiconducting, metal-oxide 1D nanostructures such as n-type, zinc oxide (ZnO) nanowires, the metal-semiconductor (MS) junction formed between the bottom and top electrode to the nanowire could be either ohmic or rectifying. In an ohmic MS junction, electrons flow freely from the metal to the semiconductor under forward-biasing conditions ($V_{\text{applied}} > 0$), giving rise to a large current even for small biases. If the applied bias were reversed ($V_{\text{applied}} < 0$) and exceeds a few tenths of a volt, electrons similarly flow freely from the semiconductor to the metal, resulting in a large reverse current. In a rectifying MS junction under forward-biasing, on the other hand, electrons could similarly flow freely from the semiconductor to the metal and give rise to an exponentially-increasing current (shown in the right shaded region of Figure 1-11) [2]. Reversing the biasing condition, however, blocks the flow of electrons from the semiconductor to the metal. While some electrons will flow from the metal to the semiconductor, the reverse current is relatively small and saturates in the characteristic behavior shown on the left hatched region of Figure 1-11.

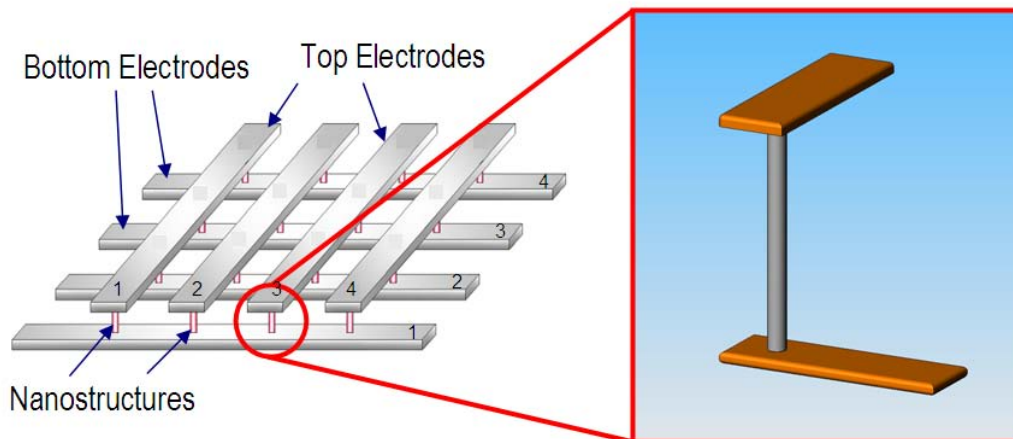


Figure 1-10. Schematic of the two-dimensional, individually-addressable nanostructure array, illustrating vertical nanostructures between top and bottom electrodes.

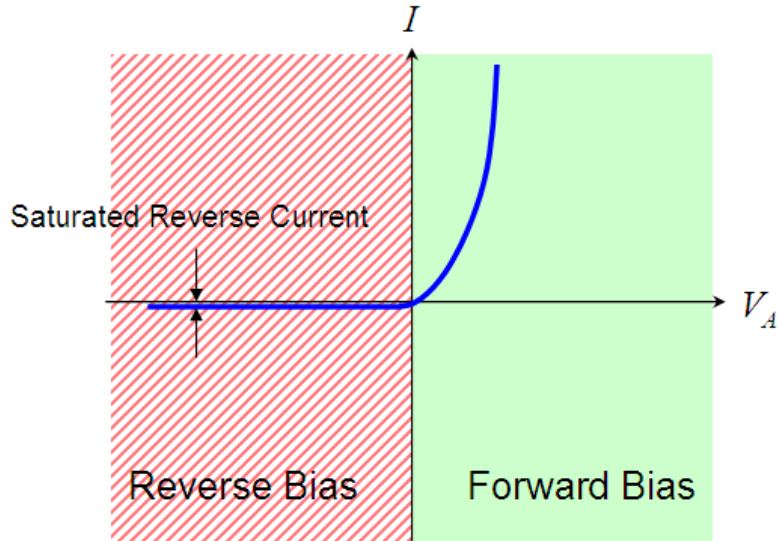


Figure 1-11. General form of the I-V characteristics of a rectifying Schottky contact.

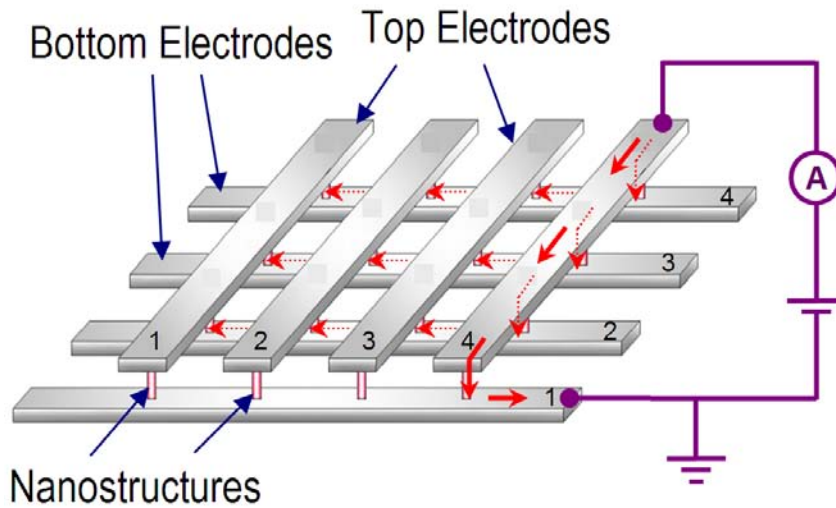


Figure 1-12. Schematic of the individual-addressability and the multiple current pathways (dotted red arrows) through the 2D nanostructure array.

The interfaces from the bottom electrode to the semiconducting ZnO nanowire and to the top electrode form a back-to-back metal-semiconductor-metal (MSM) junction that could be designed to allow current to flow only in one direction. When the top electrode-to-ZnO nanowire MS junctions are rectifying and the nanowire-to-bottom electrode junctions are ohmic, all the MSM elements in the 2D nanowire array form junctions that allow current to flow (in this configuration) only from the top electrode to the bottom electrode through the nanowires under a forward-biasing condition. The nanowire element at the intersection of top electrode #4 and bottom electrode #1, for example, could be addressed by connecting top electrode #4 with bottom electrode #1 in an electrical circuit configured according Figure 1-12. Although current

on the top electrode may follow multiple pathways through other nanowires down to the #4, #3, and #2 bottom electrodes, the rectifying nature of the top electrode-to-nanowire junctions inhibits current flow from the nanowires back to the top electrodes, thereby allowing current to flow only through the nanowire at the node that is to be addressed. It will be possible, therefore, to individually-address each nanowire in the 2D array. If a negative voltage were imposed upon the top electrode #1 instead, electrons or current would not flow through the circuit freely and would exhibit the same saturating, rectifying current characteristics of a Schottky diode.

1.3.2 Advantages of 2D Individually-Addressable Nanostructure Array

The proposed 2D individually-addressable nanostructure detailed above is realized with standard semiconductor and microelectromechanical systems (MEMS) processes, as well as the vapor-liquid-solid (VLS) catalyst-assisted 1D nanostructure synthesis process. Using standard lithographic pattern transfer techniques, the precise location for the subsequent, vertical growth of 1D nanostructures could be predetermined across an entire wafer, circumventing the need for time-consuming post-growth assembly processes. After the synthesis of these vertical 1D nanostructures, the only step required to complete the device fabrication is to deposit top metal electrodes to make electrical contacts to the nanostructures across the entire wafer. Combining assembly and the growth of the nanostructured building blocks into one step also enables the very-large-scale integration (VLSI) of 1D nanostructures into high-density functional systems of devices, a main requirement for the economic manufacture of inexpensive components for consumer products.

The vertical orientation of the 1D nanostructures in the proposed 2D array extends the device geometry into the third dimension, beyond traditional planar device architectures, and creates the possibility for ultrahigh-density system designs. Using state-of-the-art, double patterning photolithography techniques currently available in the semiconductor industry to produce $32 \times 32 \text{ nm}^2$ unit cells, the density of vertical nanostructured transistors based on carbon nanotubes (CNTs), for example, could reach tera-levels with approximately 1×10^{11} device elements per square centimeter. These device elements configured in the 2D individually-addressable array could lead to ultrahigh-resolution image sensors and ultrahigh-density nanoelectronic memory devices.

The individual-addressability of each of the 1D nanostructures within the 2D array could also bring additional functionality and complexity to existing complementary metal-oxide-semiconductor (CMOS) circuitry and devices. By selectively forming electrode-nanostructure-electrode Schottky diodes as well as p-n junctions at predetermined locations within the 2D nanostructure array, a number of different devices could be fabricated onto the same underlying CMOS circuitry to make it a truly multi-functional system. Clusters of nanowire photodetectors, single-molecule biological/chemical sensors, and light-sensitive photo-switches, for example, could be co-located with vertically-emitting nanowire lasers, light-emitting diodes (LEDs), and field-effect transistors (FETs), all operating independently or as parts of a highly-integrated system.

The overall fabrication process of the 2D nanostructure array could also be compatible with current integrated-circuit/CMOS manufacturing technology (for low-temperature nanostructure synthesis processes), allowing for its integration into existing semiconductor infrastructures without much risk or expenses. Although the catalyst-assisted, high-temperature

vapor-liquid-solid (VLS) growth technique is utilized in the present work to synthesize 1D nanostructures, various low-temperature synthesis methods could be adopted to form nanostructured devices and systems on completed CMOS circuitry on the same silicon wafer, without contributing to the overall thermal budget of the IC manufacturing process. One such low-temperature synthesis technique is the thermal decomposition of zinc nitrate hydrate in an aqueous solution of methenamine or diethylenetriamine at 90°C to form vertical ZnO nanowires across a four-inch silicon wafer [22]. Because there are no metal catalyst particles (gold is commonly used as the catalyst for VLS nanowire growth) in this thermal decomposition process, there are also no contamination issues with the current IC manufacturing processes.

1.3.3 Potential Applications

The direct, vertical integration of 1D nanostructures into a two-dimensional array could find potential applications in the field of nano-photonics, specifically in the areas of nano-resolution information displays, photo-lithography, and photo-detectors. Extending the device geometry in the vertical direction enables the fabrication of nanometer-scaled unit cells that could reach as high as 1×10^{11} device elements per square centimeter by using state-of-the-art double patterning photolithography techniques. P-N junctions between the crystalline nanowires and the patterned bottom semiconductor could be incorporated into the 2D array platform to form individually-addressable vertical light-emitting-diodes (LEDs) as the image pixels of a nano-resolution information display system. If zinc-oxide nanowires were used as the light-emitting elements in the 2D array, the band-edge emission wavelength would be centered in the ultra-violet region at 375 nm. The UV emission from this 2D array could be used as the light source for nano-resolution photo-lithography in which the individually-controllable pixel elements form the pattern that is to be transferred to the photoresist. This “maskless” lithography system could eliminate the need for expensive photomasks used in conventional IC manufacturing processes.

Instead of operating it in the light-emission mode with forward biasing, the 2D nanostructure array could be reverse-biased and operated in the light-absorption mode to function as a light sensor. The nano-resolution capability of the 2D array could provide spatial resolutions well beyond the diffraction limit of approximately 200 nm for conventional optical microscopy methods. Coupled with a near-field scanning microscope, the 2D nanowire-based photodetector array could provide an areal image of nanoscaled objects such as the DNA double-helix without the need to scan across the specimen. The high-resolution image would, instead, be generated in a single scan as the individual nanowire light sensors in the 2D array capture the features of the entire specimen. The focus of the current research will be to fabricate and demonstrate the feasibility of a two-dimensional photodetector array based on individually-addressable, vertically-integrated ZnO nanowires.

1.4 Dissertation Outline

In this dissertation, the issue of assembly and integration of one-dimensional nanoscale building blocks into functional devices is resolved by a proposed two-dimensional, individually-addressable device architecture that directly integrates vertically-oriented 1D nanostructures into the array platform. Chapter 2 focuses on process development for the fabrication of the 2D nanostructure array. A proof-of-concept CNT array has been fabricated to demonstrate the feasibility of the 2D architecture. An optimized 15x12 array has also been fabricated successfully and the electrical resistance values of the CNT connections between the top and bottom electrodes correlate consistently with those derived from a single carbon nanotube.

In chapter 3, individual-addressability of the 2D array has been enabled by replacing the metallic CNT structures with semiconducting zinc-oxide (ZnO) nanowires and creating rectifying, Schottky diodes at the 2D array nodes. The VLS synthesis of ZnO nanostructures on silicon substrates and metal electrodes was investigated, and a completed 2x5 array featuring asymmetric bottom platinum-nZnO Schottky junctions and top nZnO-titanium/gold ohmic contacts was tested for its photodetection and individual-addressability characteristics.

Chapter 4 concludes the various topics in this dissertation and summarizes the experimental results. Future research directions are also presented to improve the performance of the 2D ZnO nanowire photodetector and to enhance the functionality of the device for potential applications in various fields.

CHAPTER 2 – PROCESS DEVELOPMENT FOR 2D ARRAYS

2.1 2D Nanostructure Array Fabrication

2.1.1 Overall Fabrication Process

The two-dimensional array platform presented in this dissertation utilizes the systematic, rational self-assembly and integration of one-dimensional nanostructures into functional devices and nanosystems. A schematic of the nanostructure array was first presented in Section 1.2.1 and is repeated in Figure 2-1, showing vertically-oriented 1D nanostructures situated between top and bottom metal electrodes. The overall fabrication process to realize this device architecture is presented in Figure 2-2, with the individual steps utilizing conventional top-down

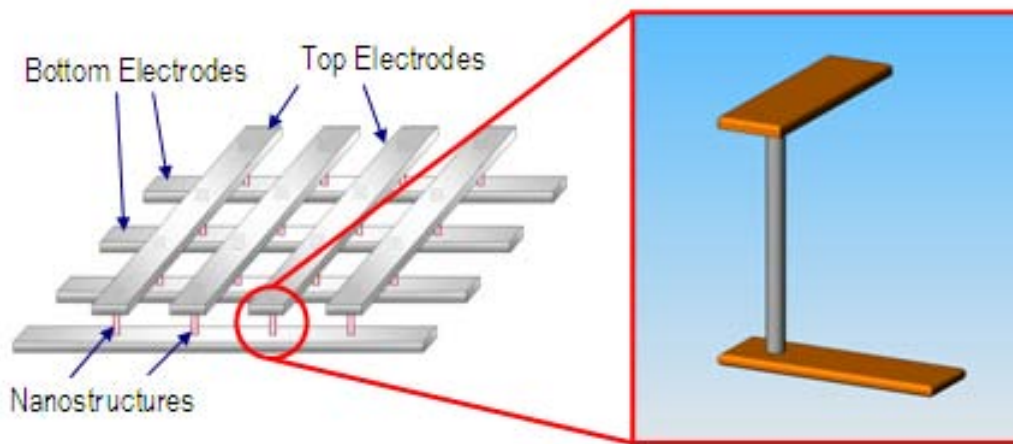


Figure 2-1. Schematic of the two-dimensional, individually-addressable array platform.

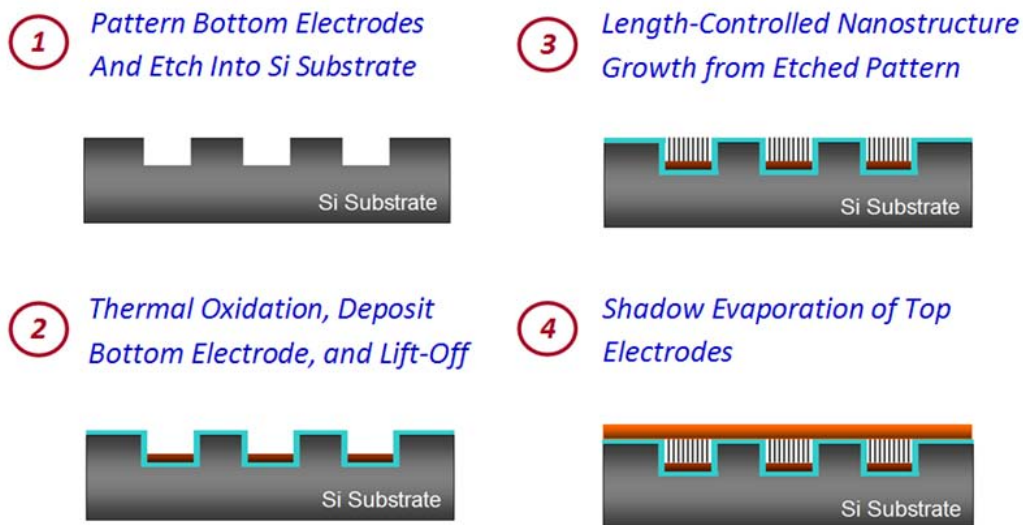


Figure 2-2. Overall fabrication process flow for the 2D nanostructure array.

IC/MEMS surface micromachining techniques as well as the bottom-up VLS nanostructure synthesis method.

In order to form the pattern for the bottom electrodes of the 2D nanostructure array, a photolithography step is necessary. A 500 μm -thick silicon wafer (*p*-type, $\langle 100 \rangle$ orientation, 5-10 $\Omega\text{-cm}$ resistivity) is first pre-cleaned with acetone and isopropyl-alcohol and baked in a furnace at 125°C for ten minutes to remove any moisture. In order to enhance the adhesion of the photoresist to the silicon substrate surface, hexamethyl-disilizane (HMDS) is spun onto the dehydrated silicon wafer in a CEE 100 spinner (Brewer Science, Inc.) at 4500 rpm for 30 seconds, with a ramp rate of 4500 revolutions/second. A positive S1813 photoresist (Rohm & Haas Electronic Materials) is immediately spun onto the HMDS-coated silicon wafer at 4500 rpm for 30 seconds, with a ramp rate of 4500 revolutions per second, to achieve a film thickness of approximately 1 μm . After soft-baking the wafer on a hotplate at 90°C for two minutes, the photoresist is exposed with a UV light source (wavelength of 365 nm, I-line) on a MA-6 Karl-Suss contact aligner (150 mJ/cm^2 exposure dose) with a chrome photomask containing a pattern of the bottom electrodes. The exposed photoresist is then developed with a solution of the Microposit LDD-26W developer (Rohm & Haas Electronic Materials) for two minutes and finally hard-baked on a hotplate at 115°C for two minutes.

After the photolithography step is completed, the photoresist pattern is transferred into the silicon wafer by an advanced silicon etch process in a STS inductively-coupled plasma (ICP) etching tool. This etching process utilizes alternating cycles of etching and polymer sidewall passivation to achieve high-aspect-ratio trenches into the silicon substrate. These trenches (shown in process Step 1 of Figure 2-2) provide the structural support for the top electrodes and, at the same time, define the pattern of the bottom electrodes of the 2D nanostructure array. The process parameters of the STS etcher listed in Table 2-1 yield a silicon etch rate of approximately 2 μm per minute. After forming trenches of a desired depth in the silicon wafer, the patterned substrate is soaked in an acetone bath to remove the photoresist, rinsed in isopropyl alcohol, and dried with nitrogen. In order to remove any residual organics, the wafer is subsequently cleaned in a Piranha solution (3:1 mixture of $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$) at 120°C for ten minutes, rinsed with deionized water, and dried with nitrogen.

<i>PARAMETER</i>	<i>PASSIVATION STEP</i>	<i>ETCHING STEP</i>
C₄F₈ Flow	85 SCCM	0 SCCM
SF₆ Flow	0 SCCM	130 SCCM
O₂ Flow	0 SCCM	13 SCCM
Platen RF Power	0 Watts	12 Watts
Coil RF Power	600 Watts	600 Watts
Cycle Time	7 sec	9 sec
Over Run	0.5 sec	0.5 sec

Table 2-1. STS plasma etching parameters for defining trenches in the silicon substrate.

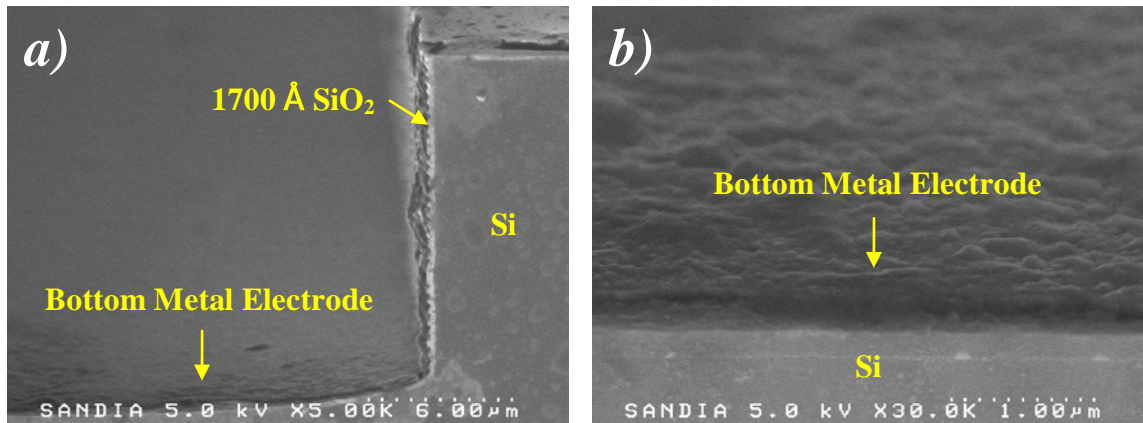


Figure 2-3. SEM images showing the metal electrode at the bottom of an etched trench that is 15 μm deep: a) cross-sectional view and b) close-up view of the metal deposit.

Serving as electrical isolation between the bottom electrodes, a silicon dioxide layer of approximately 1500 Angstroms is formed conformally across the entire silicon wafer by oxidizing the silicon wafer in Tystar atmospheric oxidation furnace at 750°C with deionized water steam and oxygen for two hours (Step 2 in Figure 2-2). Another photolithography step is carried out to align the original chrome photomask pattern (from Step 1 in Figure 2-2) to the etched features. In order to completely fill the etched trenches and cover the features evenly, a thick-film photoresist (AZ 9260, AZ Electronic Materials) is spun onto the wafer in a CEE spinner at 950 rpm for 13 seconds, with a ramp rate of 500 revolutions per second. The final film thickness achieved by this spin speed is approximately $26 \mu\text{m}$. After soft-baking the photoresist on a hotplate at 95°C for ten minutes, the chrome photomask containing the same bottom electrode pattern as the previous photolithography step is aligned on the MA-6 Karl-Suss aligner to the etched pattern and exposed with a dose of $2100 \text{ mJ}/\text{cm}^2$. The exposed photoresist is then developed with a solution of the AZ 400K 1:4 developer (AZ Electronic Materials) for nine minutes.

Bottom electrodes and 1D nanostructure growth catalyst are sequentially deposited into the open etched trenches by a straight-on electron-beam evaporation of the metals (SR-6 CHA E-Beam Evaporator, CHA Industries) while the deposited metals outside of the pattern region are removed together with the remaining photoresist in an acetone bath under ultra-sonic agitation in a lift-off process. The resulting features (after Step 2 in Figure 2-2) are shown in the cross-sectional view of the scanning electron microscope (SEM) image shown in Figure 2-3. One-dimensional nanostructures are grown in a length-controlled, timed VLS synthesis process to the height of the etched trenches. Finally, a metal shadow mask with openings for the top electrodes is used to selectively deposit the top electrodes directly over the nanostructures to complete the device fabrication.

2.1.2 Vapor-Liquid-Solid (VLS) Synthesis of 1D Nanostructures

The vapor-liquid-solid mechanism for the synthesis of one-dimensional nanostructures was first proposed in 1964 for the growth of single-crystal silicon whiskers from a silicon substrate (Figure 2-4) [23]. This VLS growth process, illustrated in Figure 2-5, begins with a

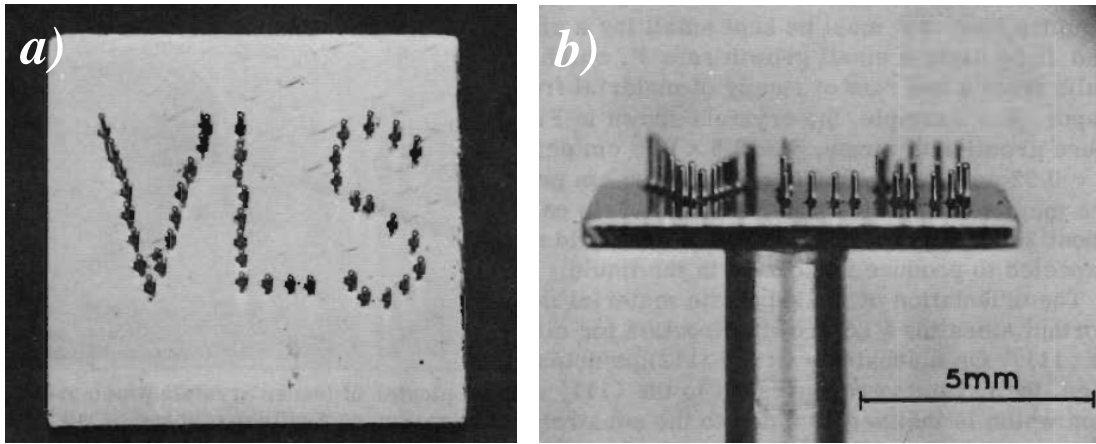


Figure 2-4. Optical images depicting an array of silicon whiskers grown on a silicon substrate from gold particles: a) top view and b) side view [23].

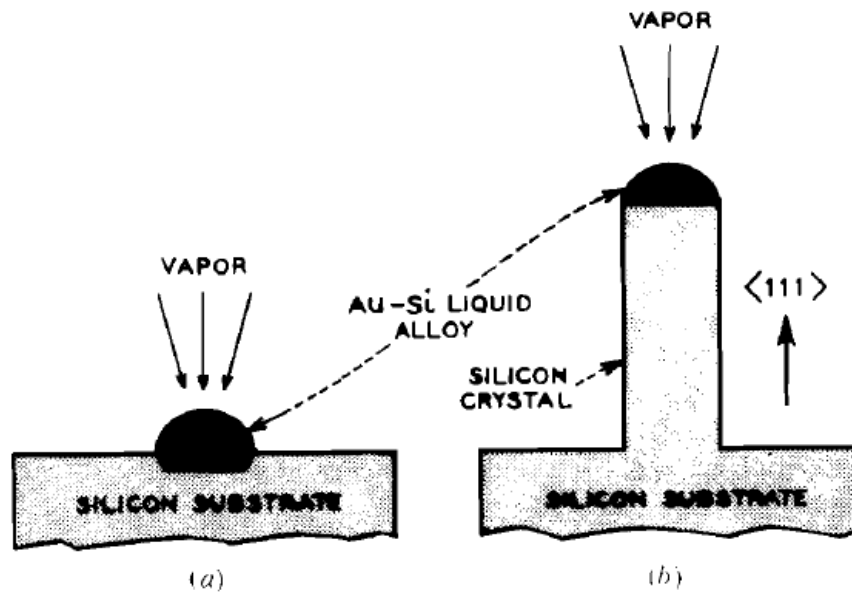


Figure 2-5. Illustrations of the VLS growth process for single-crystal Si whiskers: a) formation of eutectic liquid alloy on Si and b) growth of silicon whisker in $\langle 111 \rangle$ direction from substrate [23].

metal catalyst particle (gold) forming an eutectic alloy with the silicon surface at the specific metal-silicon eutectic temperature (363°C for the gold-silicon system). The formation of this alloy island (Figure 2-5a) follows the Volmer-Weber mode for thin film growth, and must be stable enough to allow the VLS growth mechanism to proceed. The minimum critical radius (r_{min}) of this liquid island is given by the equation:

$$r_{min} = \frac{2\gamma_{LV}V_L}{RT \ln \sigma} \quad (2-1)$$

where γ_{LV} is the liquid-vapor interfacial free energy per unit area, V_L is the volume of the liquid island, R is the gas constant, and T is the temperature. σ is the supersaturation of the vapor and is given by the equation:

$$\sigma = \frac{(P_{vap} - P_o)}{P_o} \quad (2-2)$$

where P_{vap} is the vapor pressure of the liquid alloy and P_o is the equilibrium vapor pressure of the metal at temperature T . The critical radius of the liquid droplet is approximately 100 nm for most metals in a supersaturated environment of $\sigma = 1.02$ [23].

The change in chemical potential or free energy (ΔG) of the liquid eutectic alloy is described by the following equation:

$$\Delta\mu = -k_B T \ln\left(\frac{P_{ss}}{P_{vap}}\right) \quad (2-3)$$

where k_B is the Boltzmann constant, T is the temperature of the system, and P_{ss} is the supersaturation pressure of the system. The system pressure during the VLS growth process is usually maintained at a point that is higher than the vapor pressure of the liquid alloy (P_{vap}) to achieve the supersaturation condition in the liquid alloy and the subsequent precipitation of the reactant vapors since a ratio of P_{ss} / P_{vap} greater than one will lead to condensation. Because the surface of this liquid alloy has a high accommodation coefficient and absorbs the incoming reactant vapors (Si from SiCl_4 precursors), as shown in Figure 2-5a, the liquid alloy becomes supersaturated with silicon atoms and eventually results in the formation of silicon whiskers at the $\langle 111 \rangle$ planes of the substrate (Figure 2-5b). The growth rate (J , in atoms/cm²-second) of these silicon whiskers is given by the equation:

$$J = \alpha \sigma P_o (2\pi m k_B T)^{-1/2} \quad (2-4)$$

where α is the sticking coefficient of impinging atoms that are chemisorbed by the liquid alloy.

The VLS growth mechanism was first demonstrated in 1998 to be able to synthesize one-dimensional silicon nanostructures for applications in the field of nanoelectronics [24]. Since then, it has become the main synthesis method to grow 1D nanostructures and is also the method used in this present research to synthesize carbon nanotubes and zinc-oxide nanowires during the direct vertical integration process to form a functional two-dimensional nanostructure array.

2.2 Proof-of-Concept 2D Array with Carbon Nanotubes (CNTs)

In order to demonstrate the feasibility of integrating vertical, free-standing, one-dimensional nanostructures into a two-dimensional array, a proof-of-concept device was fabricated using carbon nanotubes (CNTs). The ability to synthesize dense, highly-aligned vertical clusters of carbon nanotubes via the vapor-liquid-solid (VLS) mechanism has been proven by many experimentalists, including our research group [25-28]. A carbon nanotube

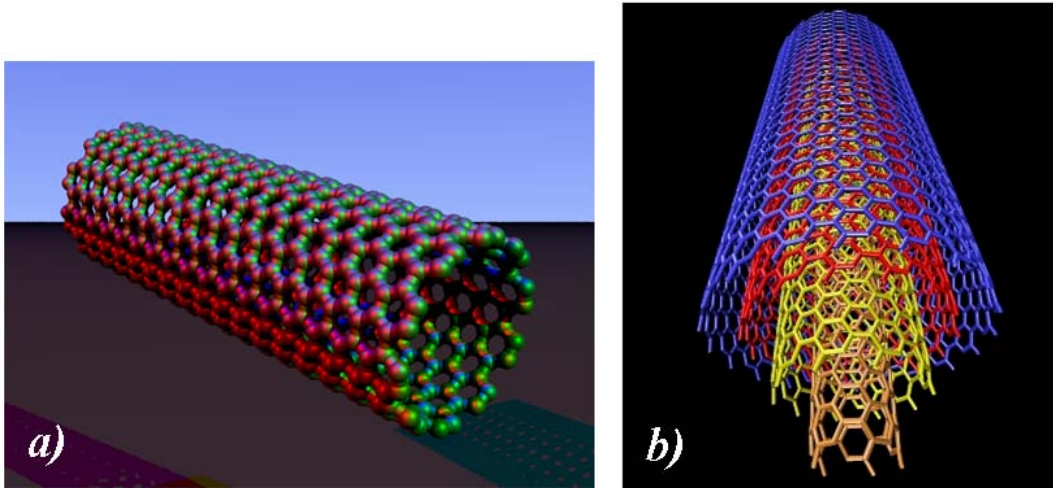


Figure 2-6. Illustrations showing the structure of *a)* single-walled [30] and *b)* multi-walled carbon nanotube [31].

(illustrated in Figure 2-6a) is structured as a rolled-up sheet of graphene (a one-atom thick layer of graphite with a hexagonal lattice of carbon atoms) that could have a length-to-diameter ratio as large as approximately 28,000,000:1 and have multiple concentric tubes inside one another to form a multi-walled nanotube (Figure 2-6b) [29]. Carbon nanotubes have a broad range of electronic, thermal, and mechanical properties unique to their structure and size that change according to the diameter, length, and chirality or twist. These one-dimensional nanostructures have a broad range of applications that include high-strength materials, single-electron switching transistors, drug-delivery vessels, super-capacitors, and oxygen sensors among many others. The ability of the proposed 2D nanostructure array architecture to accommodate carbon nanotubes will demonstrate the flexibility of the platform to vertically integrate a wide variety of one-dimensional nanostructures.

2.2.1 Device Fabrication

To simplify the fabrication process, the proof-of-concept device was created directly on top of a silicon wafer that has been coated with 1000 angstroms of thermal silicon dioxide (Figure 2-7). Using the S1813 photoresist recipe detailed in Section 2.1.1, photolithography was used to define the bottom electrode and catalyst pattern directly on top of the thermal oxide. Five nanometers of iron were used as the carbon nanotube growth catalyst, which was e-beam evaporated onto a metal stack consisting of a 10 nanometer-thick aluminum layer atop of a 60 nanometer-thick molybdenum layer. The underlying molybdenum layer serves as the current-carrying metal while the aluminum layer promotes the growth of dense CNT bundles in the presence of an iron catalyst layer [28].

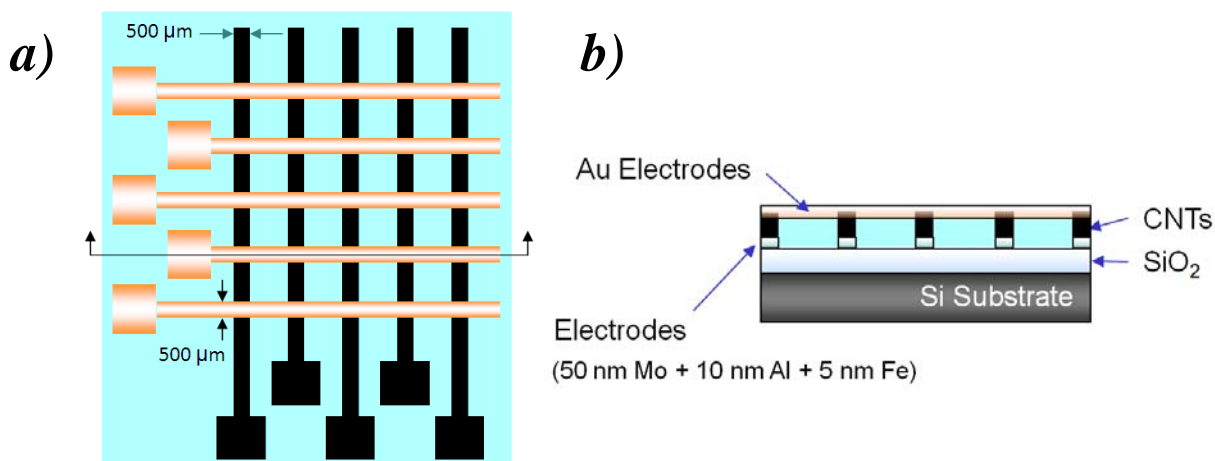


Figure 2-7. Schematic illustration of the proof-of-concept 2D array with carbon nanotubes: a) top view and b) cross-sectional view of the device.

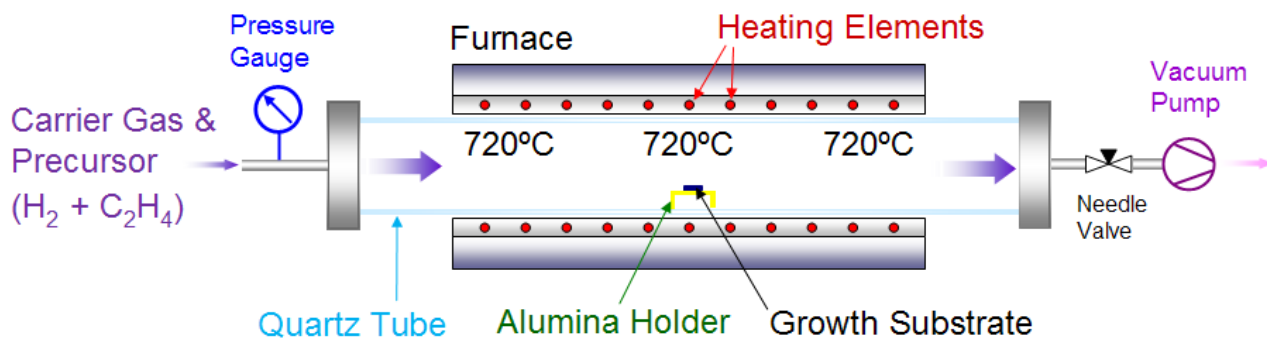


Figure 2-8. Experimental setup for the VLS synthesis of carbon nanotubes in a tube furnace.

After metal lift-off to form the final bottom electrode pattern, the growth chip was placed into a quartz tube (47 mm outer diameter, 6 feet in length) inside a three-zone, horizontal tube furnace (Lindberg/Blue M). This experimental setup is shown in Figure 2-8. In order to avoid the oxidation of carbon in the presence of oxygen, the quartz tube was evacuated with a rotary vacuum pump (Welch Vacuum Technology, Model 8907) to a base pressure of approximately 4 millibar (3 Torr) for five minutes. The tube pressure was then increased to atmospheric pressure (760 Torr) by flowing argon gas into the reaction chamber at 100 standard cubic centimeters per minute (SCCM) for 2 minutes. Once atmospheric pressure was reached, hydrogen (H_2) gas was introduced at a flow rate of 26 SCCM while the furnace heated up to the growth temperature of $720^\circ C$. When the temperature reached $720^\circ C$, the H_2 flow rate was increased to 477 SCCM to preclude the formation of amorphous carbon, while ethylene (C_2H_4) precursor was added into the growth chamber at a flow rate of 119 SCCM.

The pyrolysis of ethylene in the quartz tube is described by the following reaction equation [32]:



The C_2H_2 gaseous products are then adsorbed by the iron liquid catalyst particles and further decompose to form carbon according to the following reaction equation [33]:



This VLS synthesis of carbon nanotubes (illustrated in Figure 2-9) is allowed to occur in the reaction chamber for ten minutes, after which the flow of gases is turned off and the furnace is allowed to cool to room temperature.

The scanning electron microscope (SEM) images presented in Figure 2-10 depict the resulting carbon nanotube bundles after the growth process that are vertically-aligned and conform to the pattern of the metal electrodes. In order to form a continuous top electrode metal layer over the top of these 25 μm -tall CNT bundles, a support structure is required. A liquid

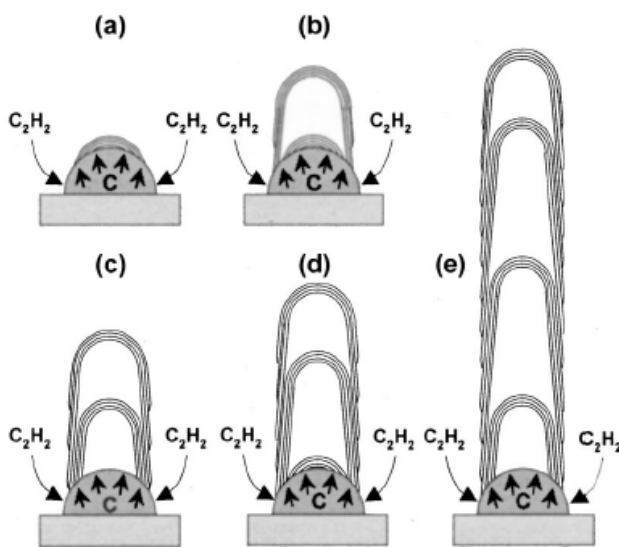


Figure 2-9. VLS growth mechanism of carbon nanotubes from the pyrolysis of C_2H_4 to C_2H_2 [33].

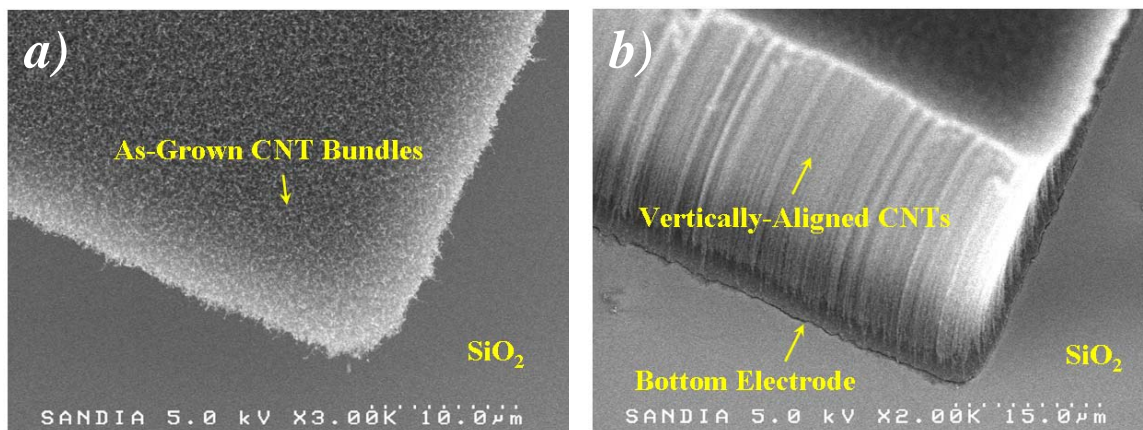


Figure 2-10. SEM images showing vertically-aligned carbon nanotube bundles conforming to the electrode pattern: *a)* top view and *b)* 30° tilted view of the as-grown CNT bundles.

<i>STEP #</i>	<i>PROCESS</i>
1	Pipette PMMA onto substrate and let it sit for 5 min
2	Ramp spin speed from 0 to 500 rpm over 50 sec
3	Ramp spin speed from 500-5000 rpm over 75 sec
4	Stop spinner
5	Bake substrate in furnace (in air) from 0 to 150°C over 30 min
6	Hold furnace temperature for 5 min, then allow to cool naturally

Table 2-2. Spin and curing recipe for the deposition of PMMA onto the CNT bundles to form the support structure for the top electrodes.

<i>PARAMETER</i>	<i>SETTING</i>
O₂ Flow	50 SCCM
Chamber Pressure	5 mTorr
Substrate Temperature	25°C
RF Power	30 Watts
ICP Power	300 Watts
Cycle Time	60 sec

Table 2-3. PMMA etching parameters in the PlasmaLab Series 100 RIE/ICP plasma etcher.

solution of 950K molecular-weight polymethyl-methacrylate (PMMA) in 5% anisole (MicroChem Corp.) was spun onto the CNT bundles to form the support layer for the top electrodes in a CEE spinner according to the recipe detailed in Table 2-2.

After completely covering the entire substrate surface and the CNT bundles, the PMMA was etched in a plasma reactive-ion etcher (PlasmaLab Series 100, Oxford Instruments) with the recipe parameters listed in Table 2-3 to expose the tops of the carbon nanotubes for electrical connection to the top metal electrode. The etch time is constantly adjusted experimentally to assure that the PMMA on top of the CNT bundles are removed for the subsequent top electrode metal deposition.

A 1 mm-thick stainless steel stencil with 1 mm-wide line openings was taped directly over exposed CNT bundles on the etched substrate, both of which were affixed to a carrier wafer (representative image shown in Figure 2-11). This metal stencil functions as the shadow mask to define the top electrode patterns when the entire unit is placed in an e-beam evaporator to deposit 200 nm of gold. The resulting 2D carbon nanotube array is shown in Figure 2-12, with 10 top gold electrodes (500 μm wide) over 10 bottom black CNT-coated electrodes (500 μm wide) forming a 10x10 array with 100 nodes.

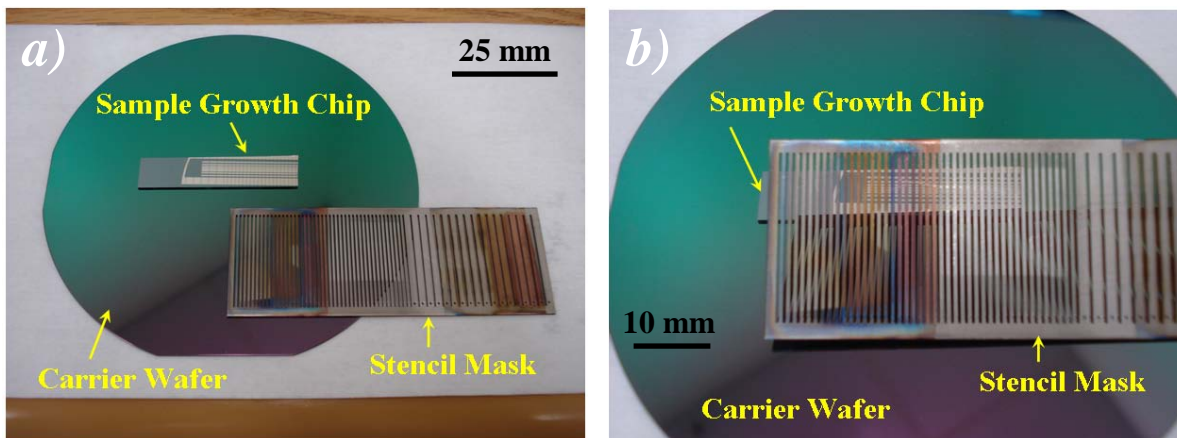


Figure 2-11. Optical images of the a) stainless steel stencil mask and b) how it covers a sample growth chip.

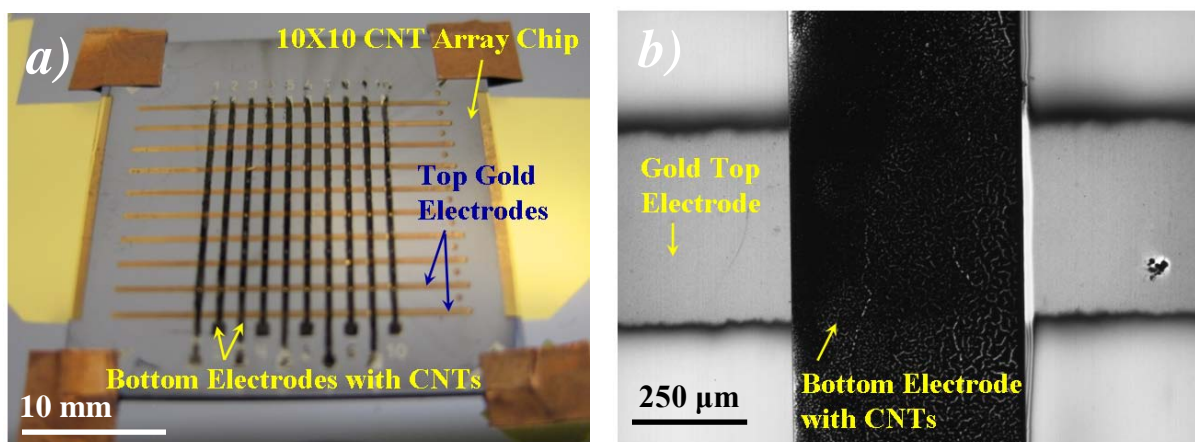


Figure 2-12. Optical images of a) the complete 10x10 array based on carbon nanotubes and b) a 10X magnified view under a microscope.

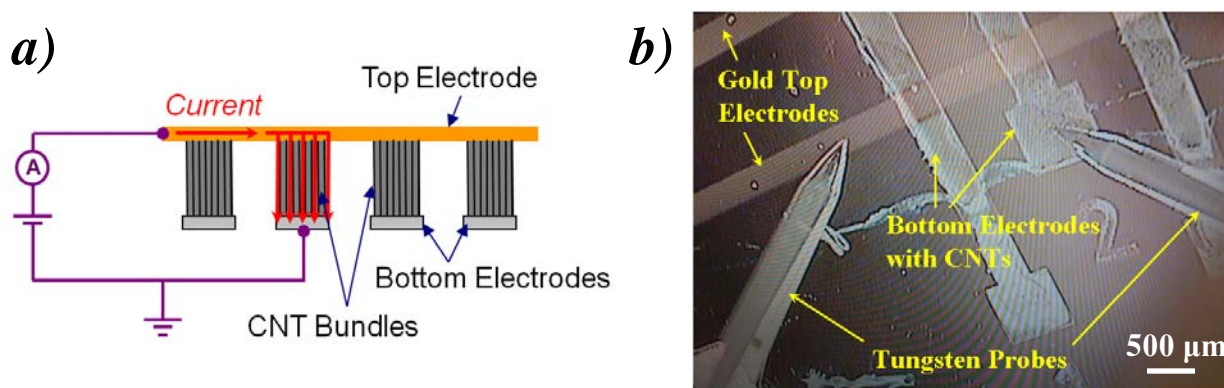


Figure 2-13. a) Schematic illustration and b) an optical image of probing the top and bottom electrodes of the CNT array to measure the current-voltage characteristics of the connections through the CNT bundles.

2.2.2 Device Characterization and Analysis

The electrical transport properties of the 10x10 carbon nanotube array were measured on a probe station with tungsten probe needles contacting the top and bottom electrodes away from the intersecting node (Figure 2-13). The current-voltage (I-V) characteristics of the top electrode to bottom electrode connection through the carbon nanotube bundles were measured by a Semiconductor Parameter Analyzer (Hewlett Packard, Model 4145B). It is noted that this 10x10 network based on CNTs will cause internal shorting as there are no “switches” on the individual CNT nodes. Therefore, individual top electrode rows of the array were isolated from the rest of the network (cut by a diamond saw) in order to measure the electrical characteristics.

Typical I-V curves of near-linear characteristics of the metallic multi-walled carbon nanotubes (MWCNTs) are presented in the plot of Figure 2-14a, showing possible successful electrical connections of the top electrode to the bottom electrodes through the CNT bundles. The electrical resistance of these connections was calculated to be several hundred ohms. The slight non-linearity in some of the curves shown in Figure 2-14a and the large variation in calculated resistance values could be attributed to the contact resistance between the tungsten probe tip and the bottom electrode (~100-200 ohms). During current-voltage measurements, the electrical contact between the tip and bottom electrode noticeably improved when the probe was pressed harder into the electrode, possibly penetrating the top insulating metal layers and contacting more conductive layers underneath. This resulted in electrical transport characteristics with lower calculated resistance values.

The I-V characteristics of the electrodes (measuring 500 μm in width and 1 inch in length) across the entire device substrate without the CNT bundles were measured on a separate sample that was not subjected to the CNT growth process (Figure 2-14b). The electrical resistance values of the top electrode, bottom electrode, and the direct top-to-bottom electrode contact without the CNT bundles were calculated to be 7, 50, and 12 ohms, respectively. Because these metal electrical resistance values are a magnitude smaller than those of the CNT-connected nodes, the top electrodes must be connected to the bottom electrodes at each node through the CNT bundles.

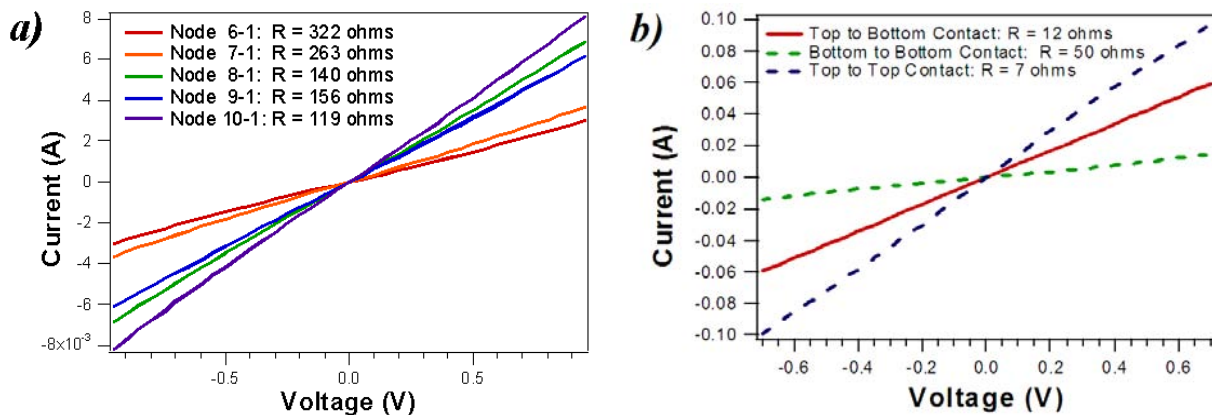


Figure 2-14. Current-Voltage characteristics of a) successful connections of the top electrode to bottom electrodes through the CNT bundles and b) the electrodes without the CNT bundles.

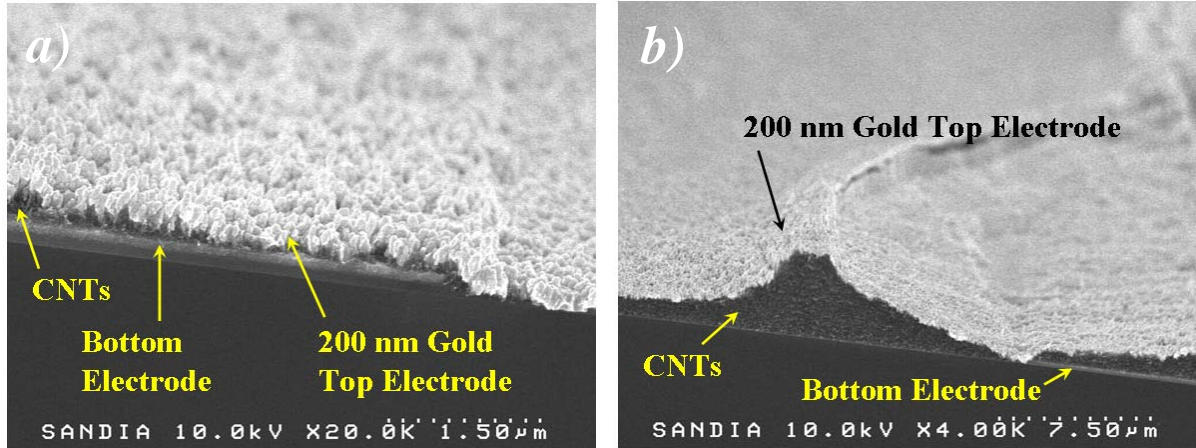


Figure 2-16. Cross-sectional SEM images of the 200 nm gold top electrode covering the CNT bundles on top of the bottom electrode, illustrating that most of the CNTs were etched away in the O₂ plasma.

Further characterization of the 10x10 CNT array was performed by cleaving the sample at the nodal area so that the cross-sectional view of the device could be examined under a scanning electron microscope. Figure 2-16 presents the scanning electron microscopy images of the nodal area of the CNT array, showing the 200 nm-thick gold top electrode layer over the CNT bundles and bottom electrode. It is apparent that most of the CNTs have been etched away since the ~30 µm as-grown CNT bundles (Figure 2-10b) have become shorter at the nodal junction. It has been showed that multi-walled carbon nanotubes could be readily etched away in an oxygen plasma environment (90 watts, 30 mTorr chamber pressure) using an Applied Materials reactive-ion etcher (RIE) in approximately 90 seconds [34]. The etching of vertical CNT bundles at the nodal junctions is, therefore, not an unusual result.

In order to avoid oxygen plasma etching to planarize the supporting structure around the CNT bundles and expose the CNT contacts, another spin-on material could be used. A dielectric spin-on-glass solution (SOG-512B, Honeywell Electronic Materials) was chosen for its ability to fill narrow spaces and form a planar surface, as well as the ability to remove it in an RIE machine by a standard silicon dioxide etch process using CF₄ and CHF₃ gases. The SOG-512B was spun onto the CNT bundles to form the support layer for the top electrodes in a CEE spinner at a spin-speed of 200 rpm for 3 seconds (200 revolutions per second ramp rate), followed by 1500 rpm for 18 seconds (200 revolutions per second ramp rate) in the same spin program. The SOG-coated sample was then cured on hotplates at 90°C, 150°C, and 250°C in succession for 60 seconds each, which yielded a dielectric film thickness of approximately 1.1 µm thick. The SOG solution, however, proved to be too viscous and caused the tall CNT bundles to clump together and topple over, as illustrated by the SEM images in Figure 2-17.

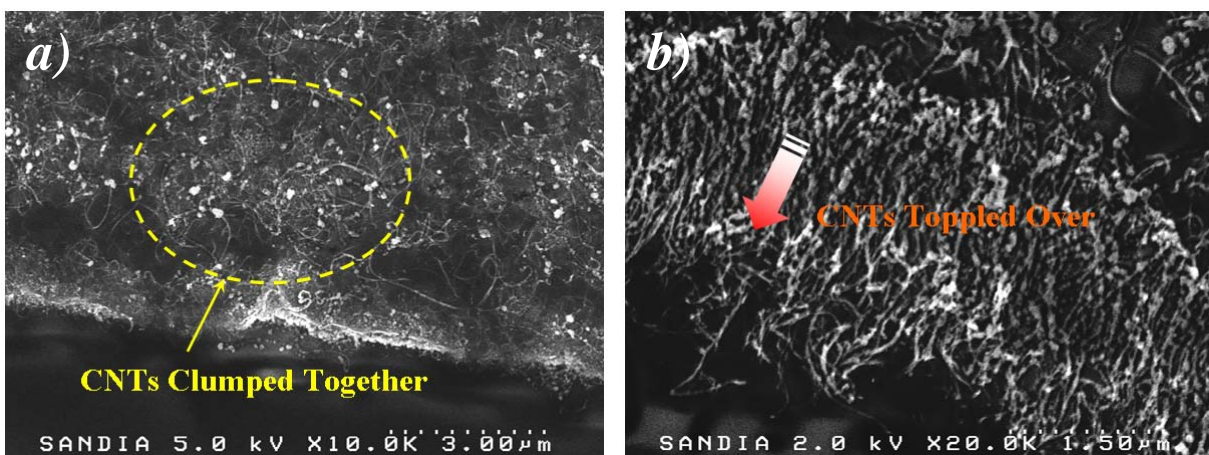


Figure 2-17. SEM images of the CNT bundles after coating with spin-on glass, showing the *a)* clumping and *b)* toppling over of individual nanotubes.

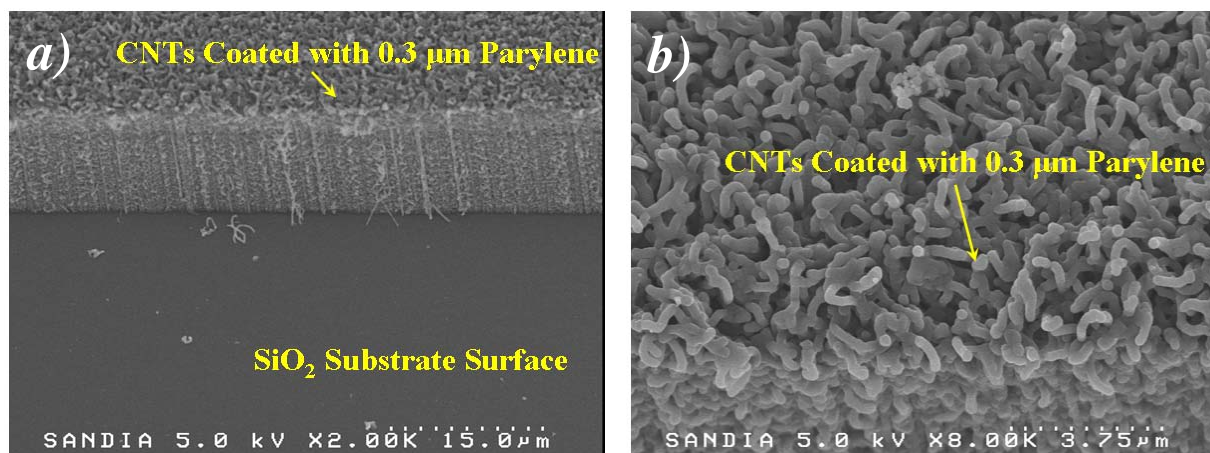


Figure 2-18. SEM images of CNTs coated with 0.3 µm Parylene C: *a)* CNT bundles on SiO₂ substrate surface and *b)* close-up view of conformal Parylene coating on individual CNTs.

As a solution to the problems associated with the viscosity of the liquid spin-on glass solution, a vapor-phase deposition of a conformal polymer such as Parylene C (poly-paraxylylene) was carried out to create the support structure for the top metal electrodes. The Parylene was sublimated inside a Parylene Deposition System 2010 (Specialty Coating Systems) at 175°C in a vacuum environment of approximately 25 milli-Torr, which yielded an average deposition rate of approximately 2 µm per hour. The SEM images presented in Figure 2-18 illustrate the resulting Parylene deposit of approximately 0.3 µm thick from a 10-minute sublimation of 2 grams of source material. The sublimated Parylene C vapors deposited conformally over the carbon nanotube bundle as well as the substrate surface at a similar rate. The SEM images in Figure 2-19 show the resulting 1 µm-thick Parylene film that was deposited over the CNTs bundle after a 30 minute sublimation of 5 grams of source material. The conformal Parylene coating over each individual carbon nanotube was so thick that it filled the spaces between each nanotube and formed a large mass of Parylene-coated bundle. The Parylene film that was deposited on the SiO₂ substrate surface, however, did not form a planar

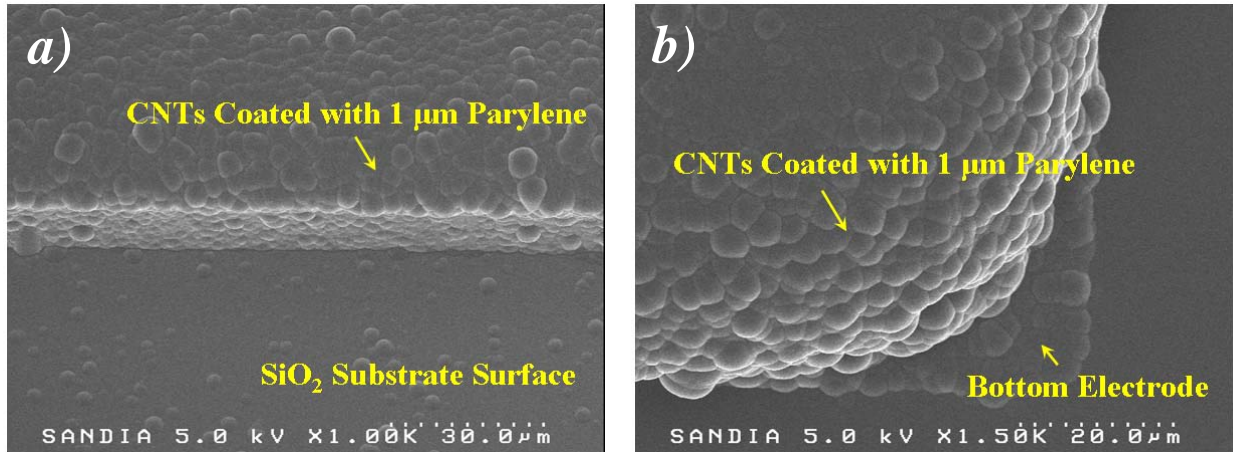


Figure 2-19. SEM images of CNTs coated with 1 μm Parylene C: *a)* CNT bundle forms a large continuous clump of Parylene and *b)* close-up view of the Parylene clump.

surface with the top of the CNT clump. In order to form a structural support layer that is as tall as the carbon nanotubes, a Parylene deposition of a thickness comparable to the nanotube length is required. This would also result in the formation of a very large clump of Parylene deposit around the carbon nanotubes themselves and require the subsequent planarization step using an oxygen plasma reactive-ion etch, which would again etch away the CNT bundles themselves in the process.

2.3 Optimized Carbon Nanotube 2D Array

2.3.1 Device Fabrication

Circumventing the problems associated with filling the CNT to form the support structure for the top electrodes, the fabrication process for the nanostructure array platform that was detailed in Figure 2-2 was adopted. After etching 15 μm-deep trenches into a silicon substrate, thermally-oxidizing the etched surfaces, and depositing the bottom electrode metal stack (Step 2 of Figure 2-2, repeated in Figure 2-20a for quick referencing), the nanostructure array platform (Figure 2-20b) is ready for the length-controlled growth process of vertically-oriented carbon nanotubes.

Following the same VLS growth parameters detailed in Section 2.2, precise control over the length of the CNT bundles was achieved by timing the exact duration of the exposure of the growth substrates to the reactant precursor gases at the prescribed growth temperature of 720°C. The flow of the reactant gases was turned off after the exposure time was reached and the sample remained in the heated furnace for exactly 60 seconds before it was removed. The SEM images presented in Figure 2-21 illustrate the formation of a planar, unorganized field of carbon nanotubes after a one-minute exposure to the reactant gases, with the CNTs extending approximately 2 μm from the base of the trench. Figure 2-22 presents the SEM images of the CNT bundles after the substrate was exposed to the reactant gases for 2.5 minutes. The CNTs are vertically-aligned (due to the van der Waals interactions between the carbon nanotubes that

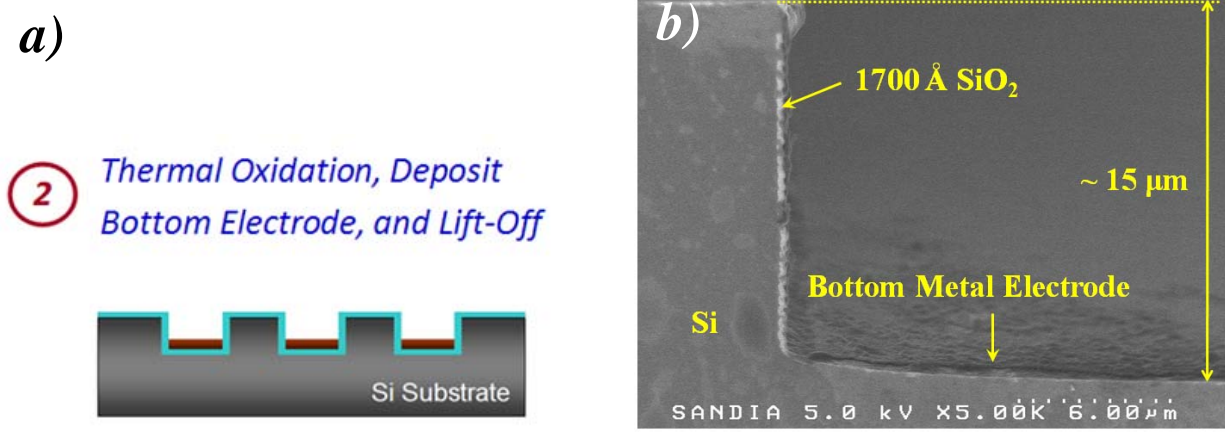


Figure 2-20. a) Nanostructure array platform after depositing bottom electrode metal into the thermally-oxidized trenches and b) cross-sectional SEM image of an etched trench.

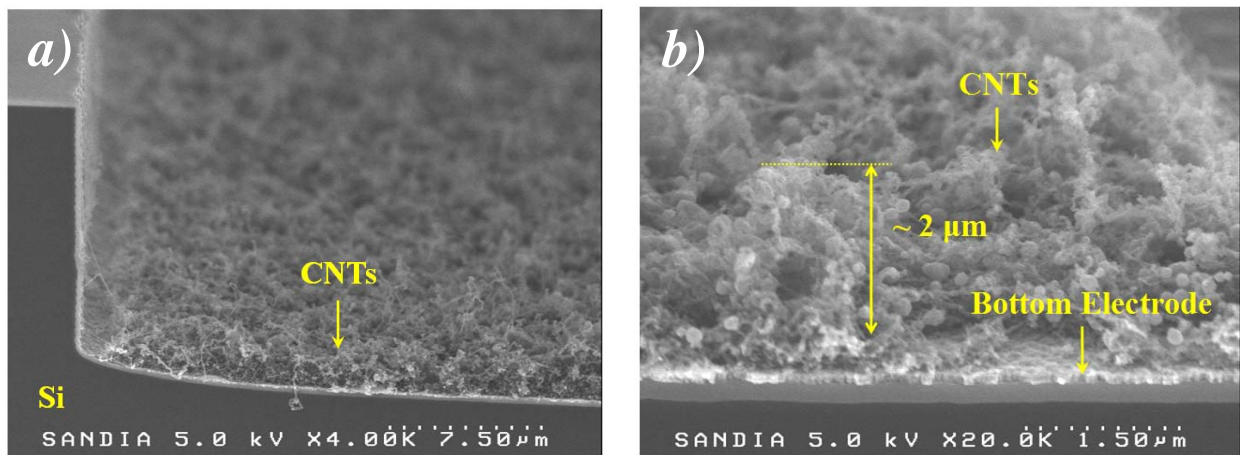


Figure 2-21. SEM images of CNTs after a 1-minute exposure to reactant gases: a) planar, unorganized field of CNTs and b) CNTs extending approximately 2 μm from the trench bottom.

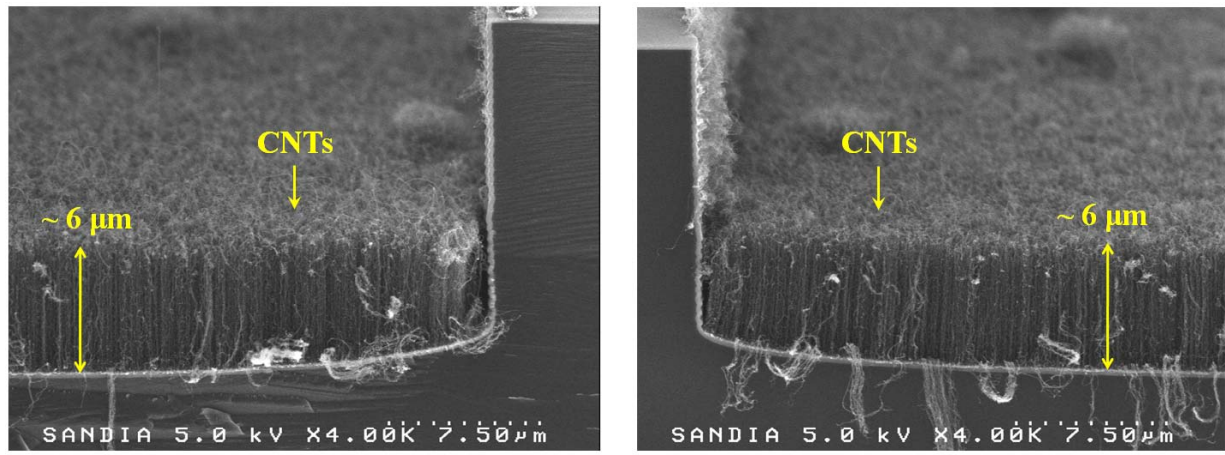


Figure 2-22. SEM images of CNTs after a 2.5-minute exposure to reactant gases.

cause them to organize and grow in the vertical, out-of-plane direction [35]) and extend approximately 6 μm from the bottom of the trench. Figure 2-23 presents the SEM images of the resulting CNT bundles after exposing the growth substrates to the reactant gases for various durations of time. A linear relationship between the length of the CNT bundles and the substrate exposure time to the reactant gases at 720°C could be inferred from the CNT growth rate graph presented in Figure 2-24.

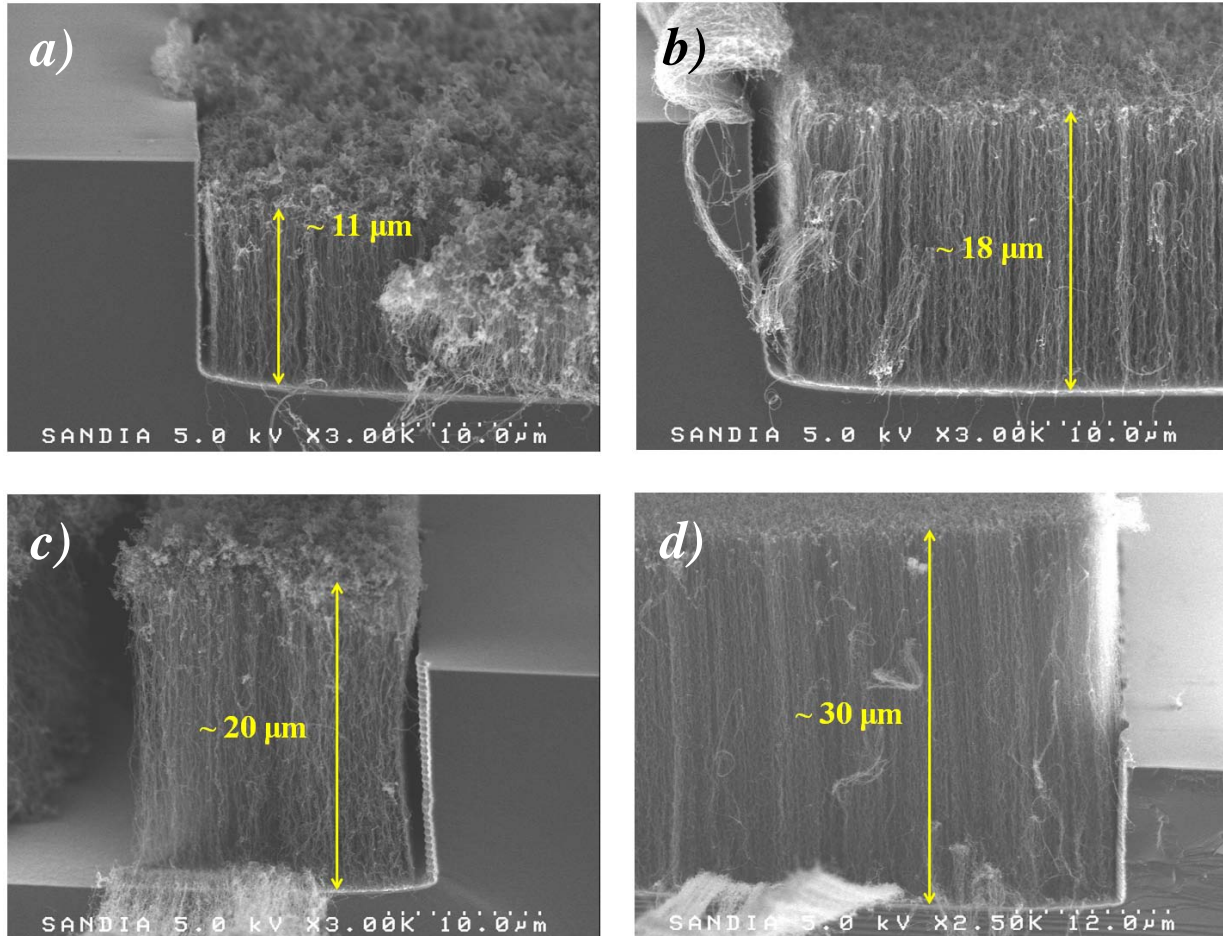


Figure 2-23. SEM images of CNT bundles after exposure to the reactant gases for a) 5 minutes, b) 6 minutes, c) 7 minutes, d) 10 minutes.

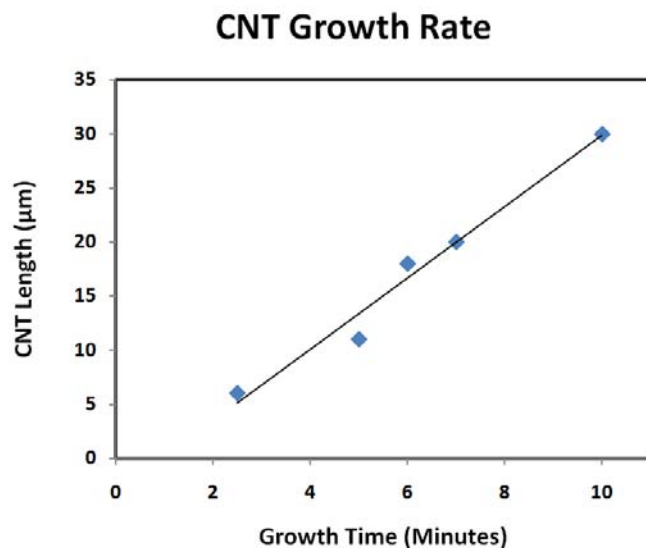


Figure 2-24. Linear relationship between the CNT length and exposure time to the reactant gases at 720°C.

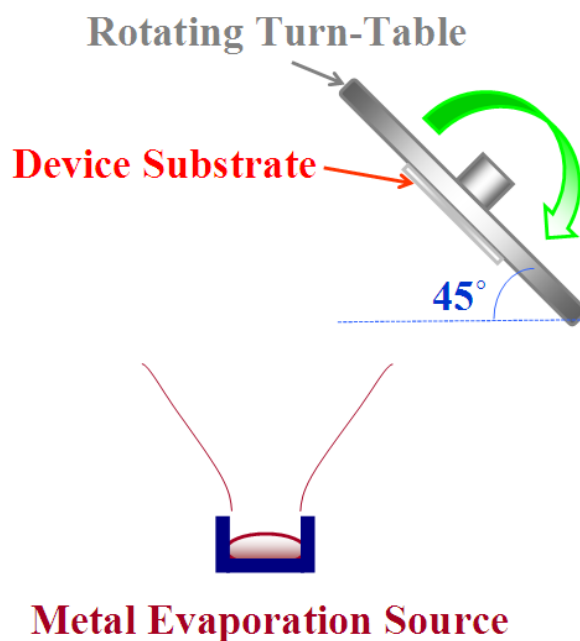


Figure 2-25. Schematic of a rotating turn-table tilted at 45° relative to the evaporation source to ensure that the metal is deposited conformally over the CNT structures.

In order to form a continuous layer of metal across the top of the silicon trench and the top of the CNT bundles, the height of the CNTs must be on the same level as the top of the trench. A growth time of six minutes, according to the length-controlled growth experiments, yielded the best planar CNT bundles with respect to the top of the etched trenches and was used as the baseline process for fabricating the CNT array devices. After the aligned CNTs were

synthesized to fill the etched trenches to a planar level, the stainless steel stencil mask (1 mm in thickness) with 1 mm-wide openings was again taped over the growth substrate and affixed to a carrier wafer for the deposition of top metal electrodes. One concern is that the direct metal evaporation process may cause significant metal penetration into the CNT array and short the device. Therefore, a continuously-rotating turn-table tilted at 45° relative to the e-beam evaporation source (schematic shown in Figure 2-25) is utilized to ensure that the metal is deposited conformally over the CNTs.

The SEM images presented in Figure 2-26 illustrate that a top-electrode metal deposition consisting of 50 nm of titanium (adhesion layer) and 300 nm of copper only coats the individual CNT structures and does not form a continuous metal film. When the top copper layer was

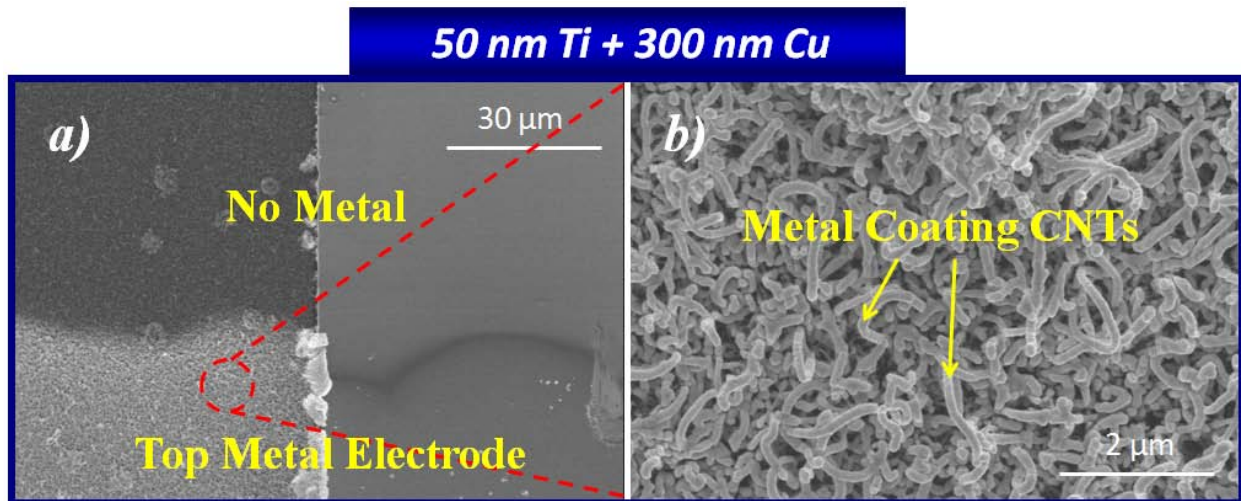


Figure 2-26. SEM images illustrating a) Ti/Cu top metal deposition of 350 nm thick and b) the metal only coats the CNT fibers and does not form a continuous film across the top.

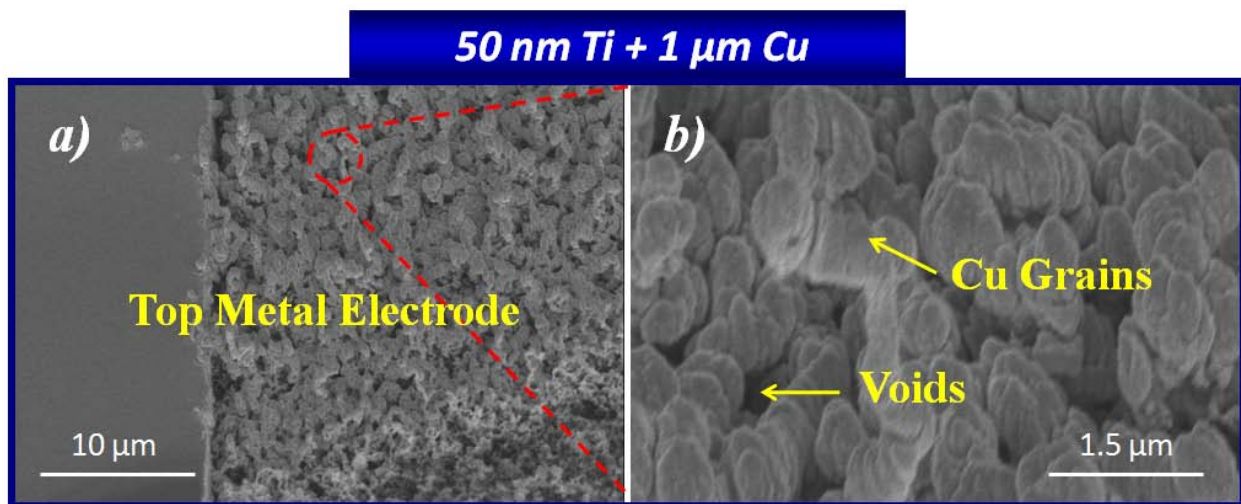


Figure 2-27. SEM images illustrating that increasing the copper metal to 1 μm results in the formation of metal grains at the ends of the CNTs, but still does not form a continuous film.

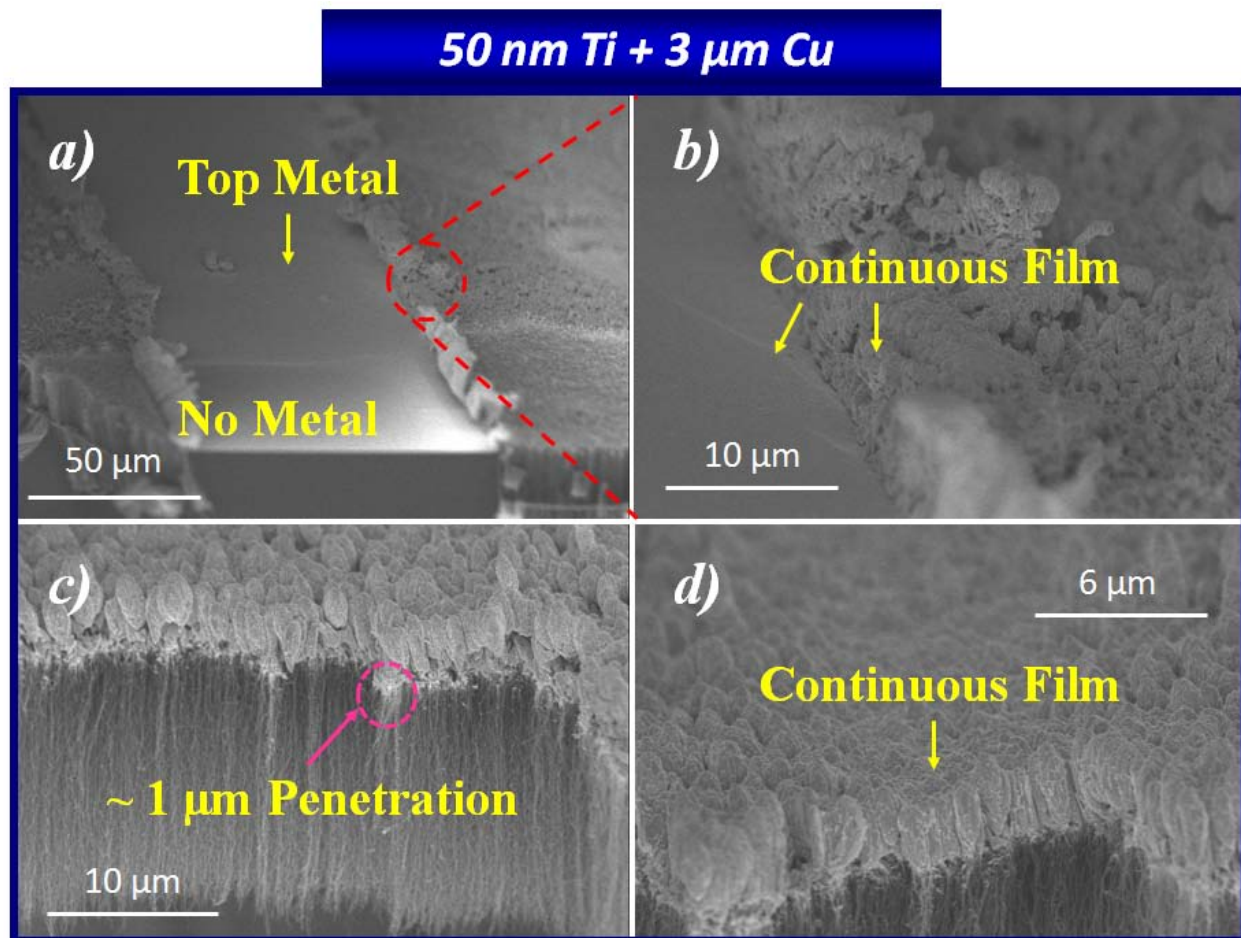


Figure 2-28. SEM images illustrating that *a), b)* increasing the copper metal to 3 μm results in the formation of a continuous top electrode film, and *c), d)* the Ti/Cu metal only penetrates approximately 1 μm down from the top of the CNT structures.

increased to 1 μm , copper grains started to form on top of the CNT structures but were still not sufficient to form continuous top electrodes across the CNT structures (Figure 2-27). As the metal evaporation deposits copper to a thickness of 3 μm , the voids between the metal grains at the ends of the CNT structures become completely filled and a continuous top electrode film is formed over the CNTs (Figure 2-28a and 2-28b). The cross-sectional views of the CNT bundle shown in Figure 2-28c and 2-28d illustrates that the evaporated Ti/Cu metals only penetrate approximately 1 μm down into the porous CNT structures and do not form direct contacts to the bottom to create shorts between the top and bottom electrodes.

The resulting 2D carbon nanotube array is shown in Figure 2-29a, with 15 top copper electrodes (500 μm wide, pictured in red) over 12 bottom black CNT-coated electrodes (400 μm wide, pictured in purple) forming a 15x12 array with 180 nodes (pictured in yellow). Each node measures approximately 500 μm x 400 μm . Because multi-walled carbon nanotubes (MWCNTs) with diameters measuring ~ 30 nm are metallic, all of the top electrodes are electrically connected to the bottom electrodes through the CNT nodes and the electrical current could have multi-paths (bi-directional paths through the CNT “interconnects” as shown by the red arrows in Figure 2-30) throughout the entire 15x12 array. Although the 2D carbon nanotube

array was fabricated as a proof-of-concept device, the electrical behavior of the top-to-bottom electrode connections through the CNT bundles could still be characterized by electrically isolating each top electrode. This was accomplished by sacrificing every other top electrode by removing it completely with a fine-tip diamond scribe (Figure 2-31).

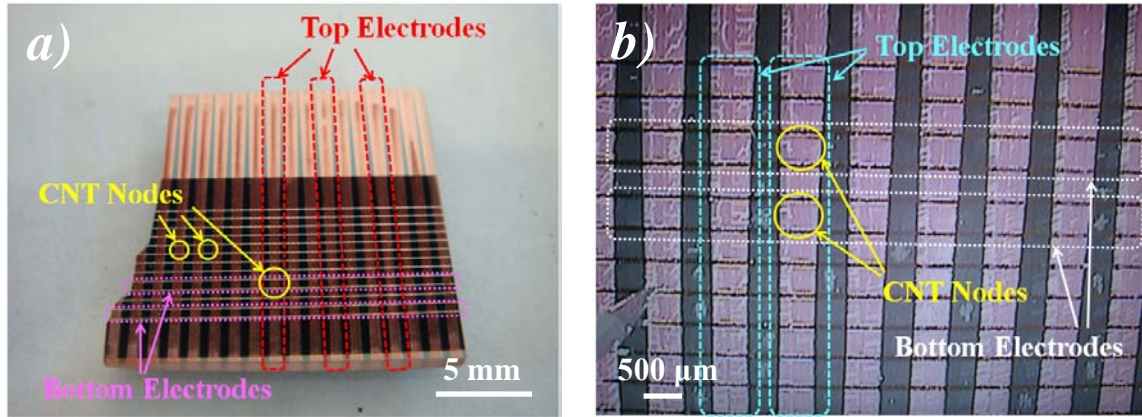


Figure 2-29. Optical images of *a)* the completed 15x12 CNT array and *b)* a close-up view of the array.

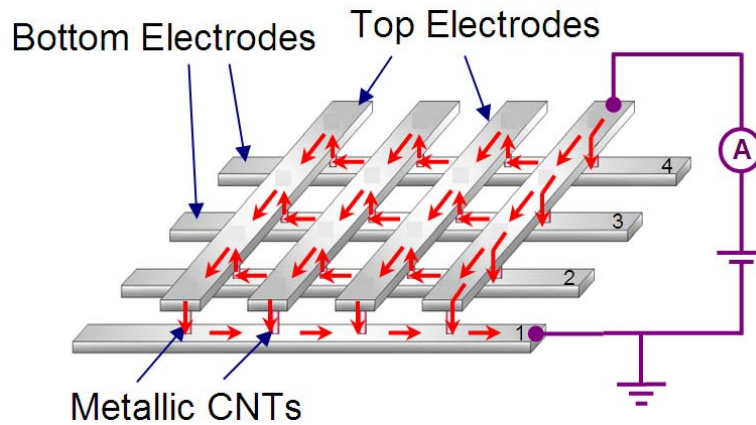


Figure 2-30. Multiple pathways for the current to travel throughout the array due to the metallic electrical characteristic of the MWCNT nodes.

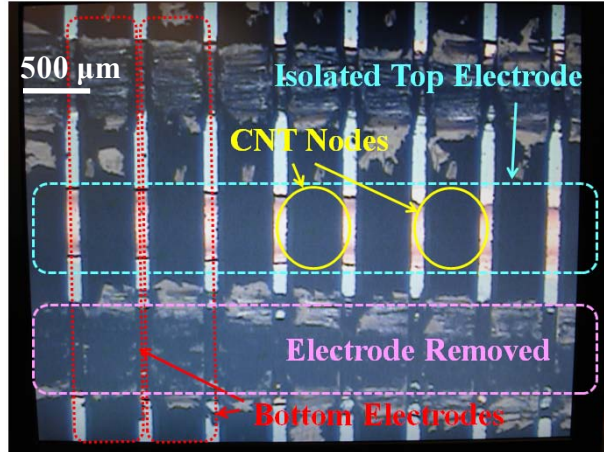


Figure 2-31. Optical images of the CNT array after the top electrodes were electrically isolated by scratching off the neighboring electrodes.

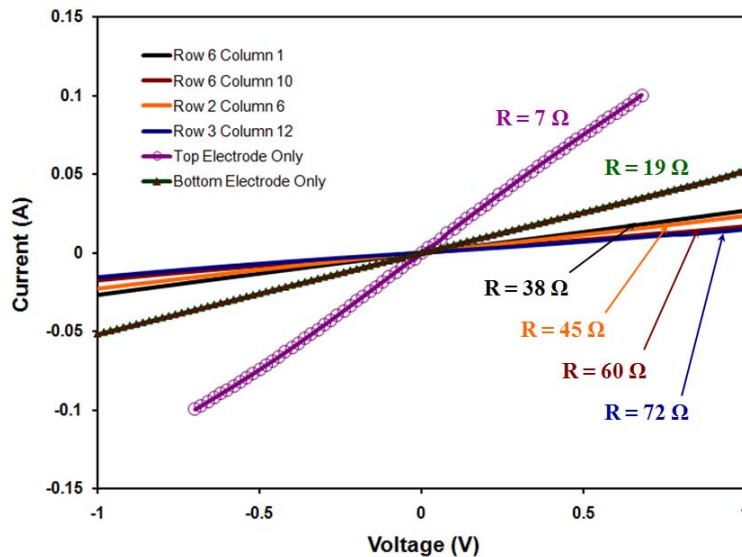


Figure 2-32. Typical I-V characteristics of the CNT device, showing expected linear behavior of the metallic MWCNTs.

2.3.2 Device Characterization and Analysis

The current-voltage characteristics of the MWCNT bundles (typical curves shown in Figure 2-32) at the electrically-isolated 84 nodes of the array exhibit the expected linear behavior for metallic carbon nanotubes. The bottom electrodes (measuring 400 μm in width and 15 mm in length) have an average resistance value of 19 Ω as calculated from the I-V data ($R=V/I$) while that of the top electrodes (measuring 500 μm in width and 15 mm in length) is 7 Ω. The average resistance values across the CNT structures that connect the top electrode to the bottom electrode of the electrically-isolated nodes of the device are presented in the histogram in Figure 2-33. As evident in the histogram, there is a large number of resistance values centered about ~50 Ω and a

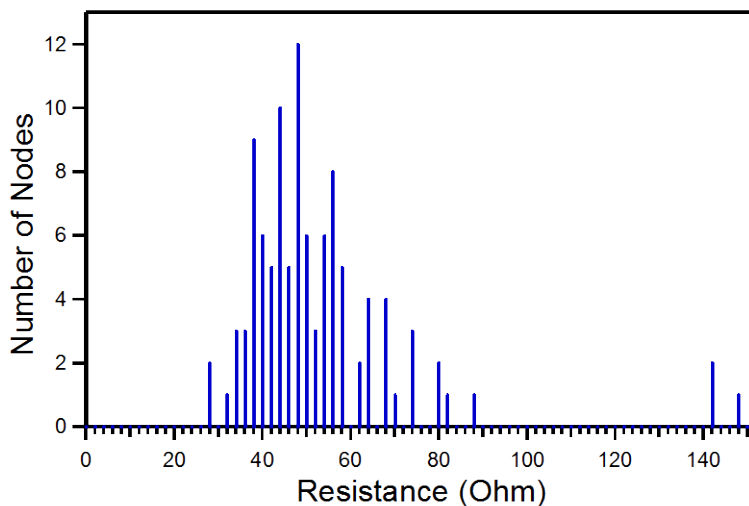


Figure 2-33. Histogram of calculated resistance values from the 84 electrically-isolated nodes in the 15x12 CNT array.

few anomalous resistance values higher than 100 Ω , while the average resistance value of the 84 nodes is approximately 54 Ω . The uncharacteristic data points could be attributed to the fact that the Mo/Al bottom electrode metal stack has become insulating due to the possible formation of a thin aluminum-carbide film during the CNT synthesis process. During the I-V measurements for the CNT array, it was noticed that, when the probe tips were pressed hard into the bottom electrode, the electrical connection between the two interrogating probe tips and the CNT device electrodes improved and yielded a lower calculated resistance value. The probe tips most-likely penetrated through the insulating aluminum-carbide film and made contacts to the highly-conductive molybdenum metal material. The resistance values in the histogram that are higher than 100 Ω were, therefore, due to the poor electrical contact between the probe tip and the bottom electrodes.

To facilitate the verification that the electrical measurements and the calculated resistance values of the CNT nodes in the 15x12 array are reasonable, the electrical behavior of a single carbon nanotube was characterized inside a Hitachi S-4500 Field-Emission Scanning Electron Microscope (FE-SEM). Using two MM₃A-3M micromanipulators with tungsten nano-tips (Kleindiek Nanotechnik GmbH) mounted inside the SEM specimen chamber, CNT strands were toppled-over from the cleaved edge of a growth substrate by dragging the nano-probe across the top of the CNT bundle (Figure 2-34a). When one single strand became separated from the rest of the toppled CNTs, it was attached to the nano-probe tip through a Joule-heating/welding process by focusing the SEM electron beam on the CNT-probe interface [36]. After a stable, permanent attachment is achieved, the nano-probe was moved away from cleaved edge of the substrate, breaking the CNT strand from the substrate in the process (Figure 2-34b). A second nano-probe was then brought into contact with the dangling end of the CNT strand and a permanent connection was made with the same Joule-heating/welding process (Figure 2-35).

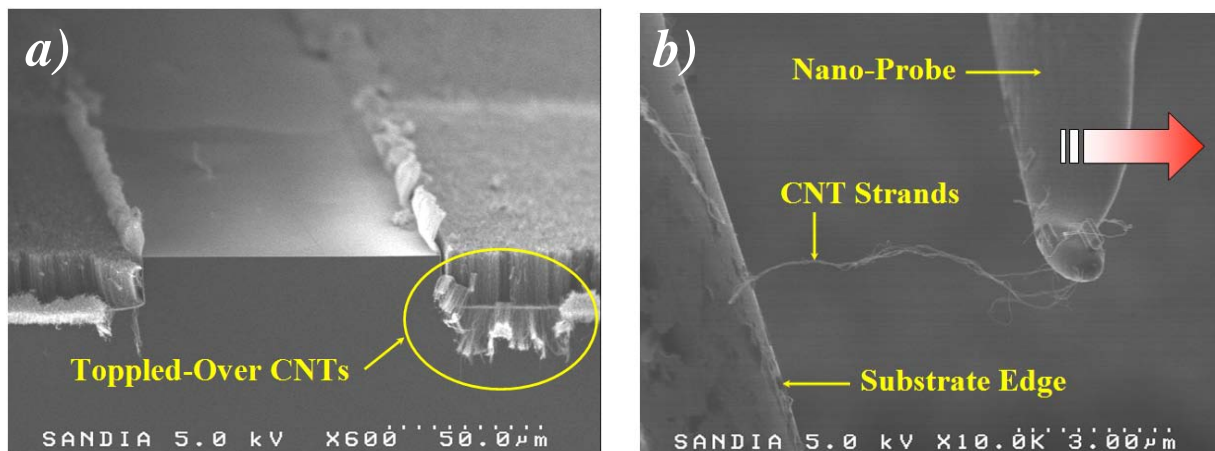


Figure 2-34. SEM images of *a)* the toppled-over the CNT bundles and *b)* the nano-probe breaking several CNT strands from the substrate.

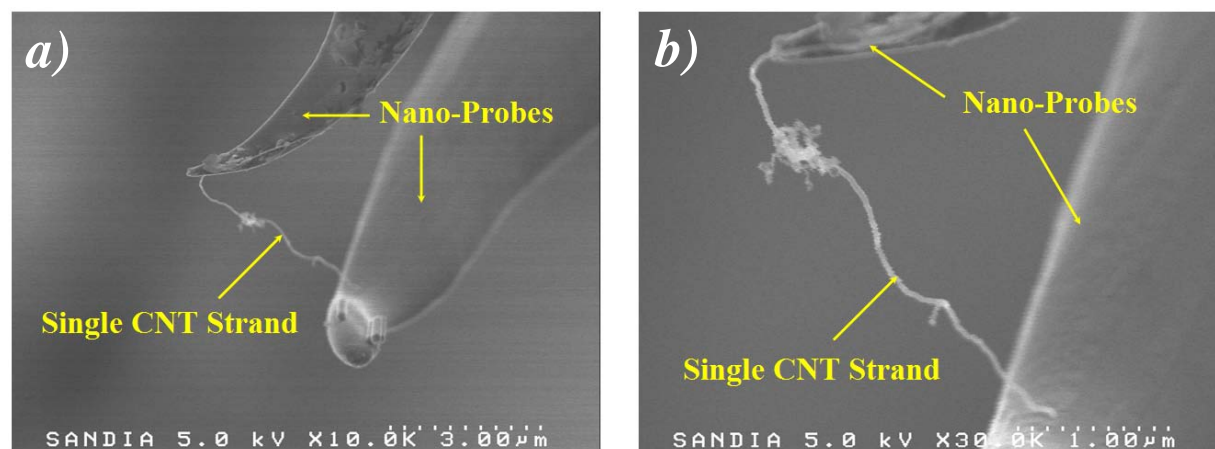


Figure 2-35. SEM images of *a)* a single CNT strand attached to two nano-probe tips and *b)* the close-up view.

The electrical behavior of the single carbon nanotube was characterized by current-voltage measurements (Keithley Instruments Inc., Model 237 High Voltage Source Measuring Unit) within the SEM specimen chamber under high-vacuum. For the 1 μm -long multi-walled carbon nanotube shown in Figure 2-36a, the I-V characteristic shown in the graph of Figure 2-36b exhibits a near-linear behavior that is typical of metallic carbon nanotubes. The resistance of this specific nanotube is calculated to be approximately 79 M Ω . The corresponding resistivity of the 1 μm -long carbon nanotube with a diameter of approximately 30 nm is calculated to be 0.056 $\Omega\text{-m}$ according to:

$$R = \frac{\rho L}{A} \quad \text{or} \quad \rho = \frac{RA}{L} \quad (2-7)$$

where R is the resistance (Ω), ρ is the resistivity ($\Omega\text{-m}$), L is the nanotube length (m), and A is the

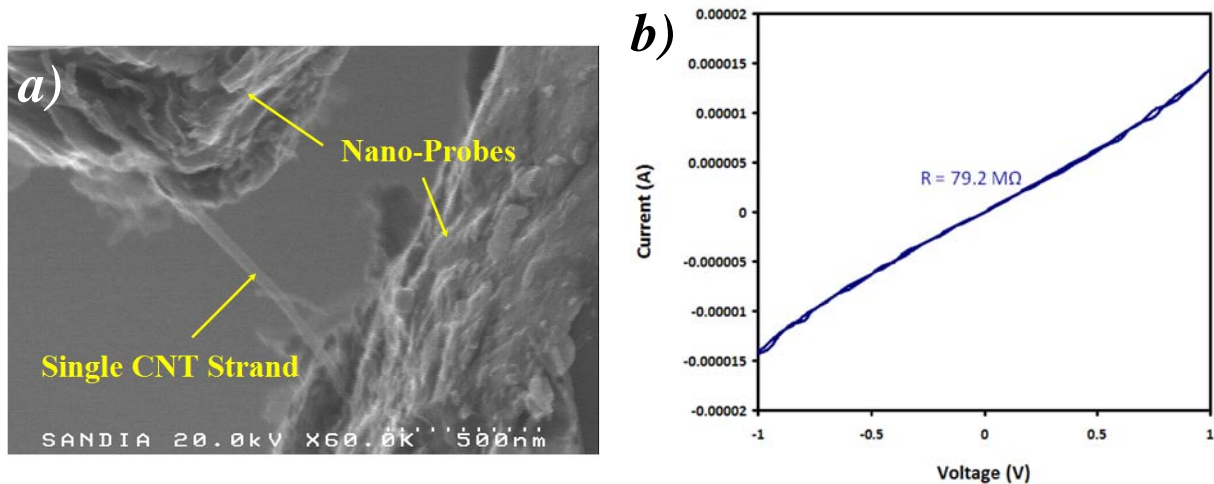


Figure 2-36. a) SEM image of a single 1 μm -long CNT across two nano-probes, b) I-V characteristic of the 1 μm -long nanotube.

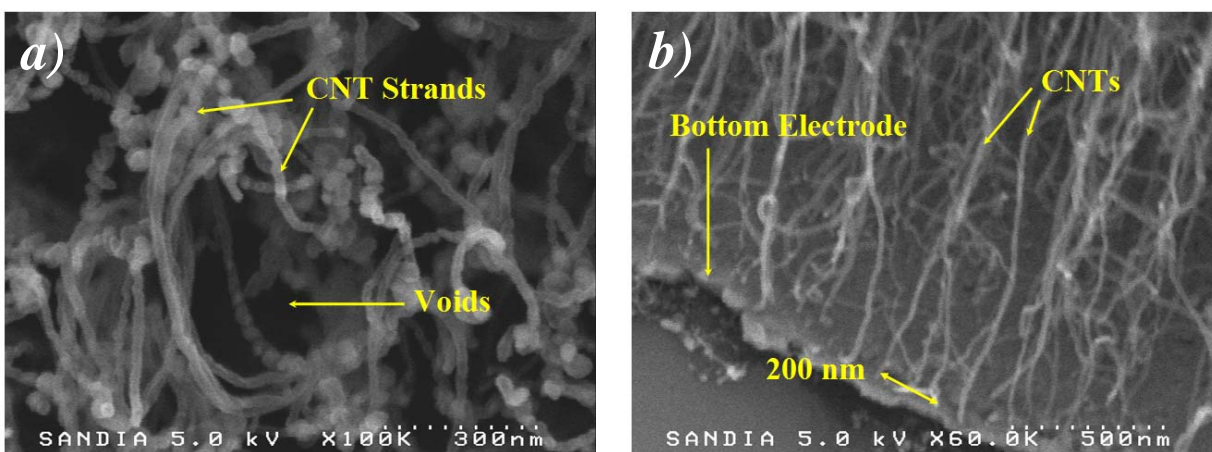


Figure 2-37. a) Top-down SEM image of the as-grown CNT bundles showing a low density, b) cross-sectional SEM image illustrating that there is a 200 nm separation between each nanotube.

cross-sectional area of the nanotube (m^2). Using the same equations above, the resistance value of a single carbon nanotube that measures 17 μm long (the length of the CNTs in the fabricated 15x12 array) is calculated to be approximately 1.4 G Ω . Since each nodal area in the CNT array is 500 μm x 400 μm , the total number of individual carbon nanotubes that could potentially be closely-packed into the nodal area is approximately 2.2×10^8 nanotubes. The density of the CNT bundles, however, is not very high as illustrated by the top-down SEM image of Figure 2-37a. The cross-sectional SEM image presented in Figure 2-37b illustrates that there is an average separation of approximately 200 nm to 300 nm between each carbon nanotube on the bottom electrode from which it grew. This would lead to an approximation that the CNTs occupy the 500 μm x 400 μm nodal area with a density range of 15% to 10%, respectively, leading to $33 \times 10^6 \sim 22 \times 10^6$ carbon nanotubes connecting the top electrode to the bottom electrode at each node.

The overall resistance value of each node in the CNT array is calculated to be approximately 41~61.4 Ω according to Equation 2-8 (for the 15% density estimate).

(2-8)

$$\begin{aligned}\frac{1}{R_{Tot}} &= \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \dots \\ &\cong 33 \times 10^6 \times \left(\frac{1}{1.35 \times 10^9 \Omega} \right) \\ &\cong 0.0244 \Omega^{-1}\end{aligned}$$

$$R_{Tot} \cong 41 \Omega$$

This result correlates very well with the measured resistance values from the 84 electrically-isolated CNT nodes shown in the histogram of Figure 2-33, signifying that there are indeed successful electrical connections between the top and bottom electrodes through the CNT bundles sandwiched in between.

2.4 Summary

This chapter detailed the numerous process-development experiments and results that have led to the successful demonstration of a two-dimensional nanostructure array based on carbon nanotubes. After overcoming all the problems associated with the fabrication process of the proof-of-concept CNT device, a complete 15x12 carbon nanotube array was realized and fully characterized in terms of the electrical properties of the CNT nodes that connected the top and bottom electrodes.

The concept of individual-addressability was not demonstrated with the CNT arrayed device due to the metallic nature of the multi-walled carbon nanotubes, which allowed the electrical current to flow freely across many multiple nodes throughout the array. The overall architecture of the proposed 2D nanostructure array, nevertheless, was demonstrated by the optimized 15x12 CNT-based device as well as the successful electrical connections that correlated well to the nodal electrical resistance estimates.

All of the lessons learned from the process development experiments for the CNT device will be carried over to the fabrication and characterization of a functional, individually-addressable 2D nanostructure array based on zinc-oxide nanowires. Details of the zinc-oxide nanowire array will be presented in the following chapter of this dissertation.

CHAPTER 3 – 2D ZINC-OXIDE NANOWIRE ARRAY

3.1 Introduction

The two-dimensional nanostructure array based on multi-walled carbon nanotubes presented in the previous chapter demonstrated the feasibility of integrating vertical, one-dimensional nanostructures into a functional device. Because of the metallic behavior of the carbon nanotubes, the individual-addressability feature of the device was not demonstrated. The solution presented in this chapter is to replace the metallic CNT structures with semiconducting zinc-oxide (ZnO) nanowires and create rectifying, Schottky diodes at the 2D array nodes. The rectifying nature of the nodes would allow the electrical current to travel in one direction only, thereby eliminating the multi-path problem associated with the CNT device.

Zinc-oxide is a direct, wide band gap semiconductor ($E_g = 3.37$ eV) with attractive materials properties such as piezoelectricity, biocompatibility, high electron mobility, large exciton binding energy (~60 meV), as well as its stability under high-energy radiation. One-dimensional ZnO nanowires have, therefore, found widespread applications in nano-devices such as energy generators [37], chemical-biological sensors [38], field-effect transistors [39], light-emitting diodes [40], optically-pumped lasers [41], and UV photodetectors with high internal gain [42].

The nanostructure device architecture presented in this dissertation integrates these ZnO nanowires into a 2D ultra-violet (UV) photodetector array that is capable of discrete pattern discrimination. The high crystallinity, large surface-to-volume ratio, and the reduced dimensionality of the 1D ZnO nanowire active areas in the UV photodetector could contribute to a substantial increase in the photoconductive gain [42], illustrating the potential application of the individually-addressable array as a highly-sensitive UV image sensor.

3.2 ZnO Nanowire Array Design

The individual-addressability of the nodes in the 2D nanostructure array is realized by forming rectifying, Schottky electrical contacts between the bottom electrodes and the vertical zinc-oxide nanowires, as well as ohmic electrical contacts between the top electrodes and the nanowires (Figure 3-1). This design concept was first introduced in the research overview section of this dissertation (Section 1.3) and will be thoroughly explained in this section.

A Schottky contact could be formed at the junction between a metal and a semiconductor (MS junction) to produce a potential barrier that conducts electric current in one direction while blocking current in the opposite direction. This rectifying property was designed into the 2D zinc-oxide nanowire device by choosing a metal electrode material whose work function (the minimum energy needed to move an electron from its Fermi level into vacuum) is considerably larger than that of intrinsically n-type ZnO nanowires in order to form a sufficient rectifying potential barrier, Φ_B . This barrier is the surface potential energy barrier encountered by electrons in the metal at the Fermi energy level (E_f) while traveling to the semiconductor.

Platinum is a suitable material to form this rectifying MS junction because the work function for polycrystalline platinum is 6.1 eV [43] while that of ZnO nanowires is 5.2 eV [44]. The energy band diagrams for these two materials and the resulting MS junction are presented in

Figure 3-2. The potential barrier (Φ_B) that results from the formation of this Pt-nZnO Schottky junction is calculated to be approximately 1.6 eV according to the following equation:

$$\Phi_B = \Phi_{metal} - \chi_{semiconductor} \quad (3.1)$$

where Φ_{metal} equals 6.1 eV, $\chi_{semiconductor}$ is the electron affinity of ZnO and equals 4.5 eV. The voltage drop across this Schottky junction under equilibrium conditions is the built-in voltage (V_{bi}) shown in Figure 3-2b. This built-in voltage is often referred to as the turn-on voltage of the

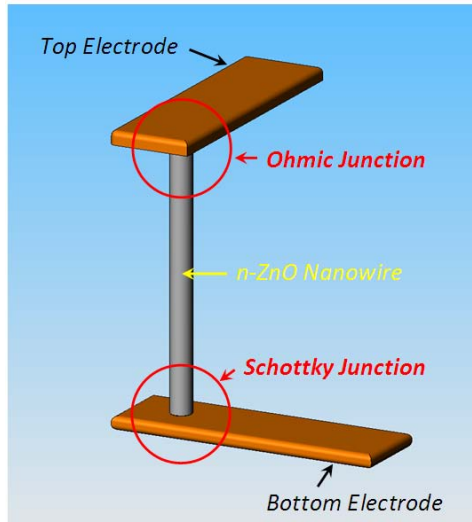


Figure 3-1. Schematic illustration of the ohmic junction between the top electrode and ZnO nanowire as well as the Schottky junction between the ZnO nanowire and bottom electrode.

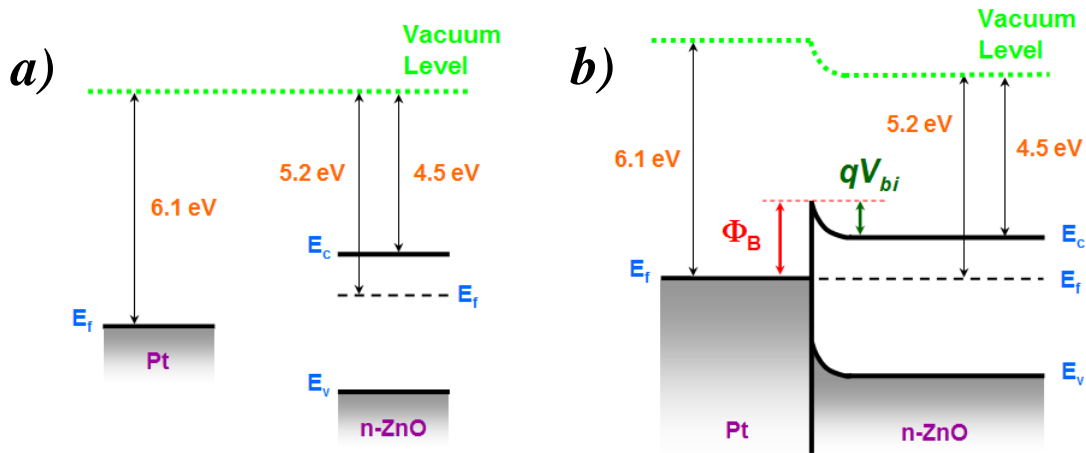


Figure 3-2. Energy band diagrams for a) platinum and n-type ZnO and b) the Schottky MS junction and the potential barrier (Φ_B) formed between the two materials under equilibrium conditions.

device and is the potential barrier that must be overcome under forward-biasing conditions to produce a forward current. For the Pt-ZnO Schottky junction pictured in Figure 3-2b, the built-in voltage is the difference between the platinum and ZnO work functions and is approximately equal to 0.9 V.

At the opposite end of the ZnO nanowire, an ohmic contact is formed when the other metal electrode material has a work function that is smaller than that of ZnO. Aluminum is a suitable material for this ohmic MS junction since its work function is 4.2 eV [37]. The energy band diagrams for aluminum and ZnO and the resulting ohmic MS junction are presented in Figure 3-3. When the 2D array is completed and successful electrical connections are achieved between the n-type ZnO nanowires and the ohmic top electrodes as well as the rectifying bottom electrodes, back-to-back metal-semiconductor-metal (MSM) junctions are created (Figure 3-4a). Because the ohmic junctions between the aluminum electrodes and the n-type ZnO nanowires

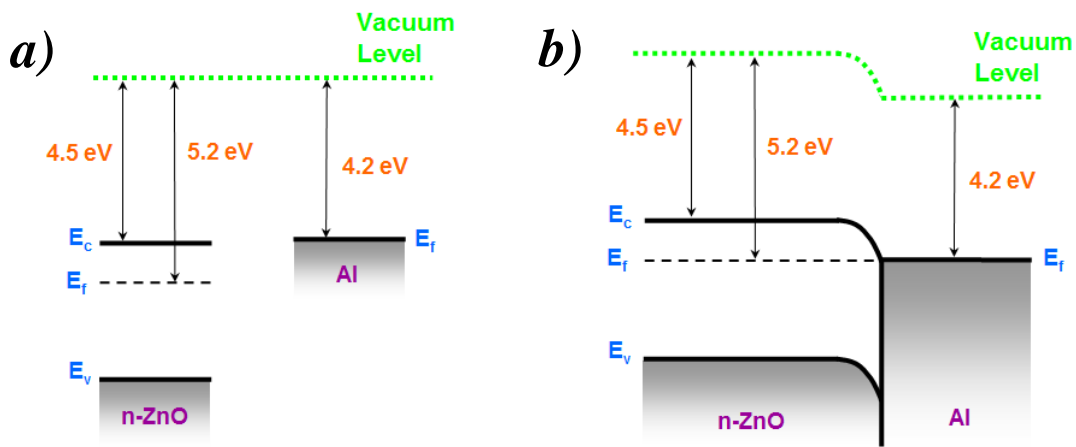


Figure 3-3. Energy band diagrams for a) n-type ZnO and aluminum and b) the ohmic MS junction between the two materials under equilibrium conditions.

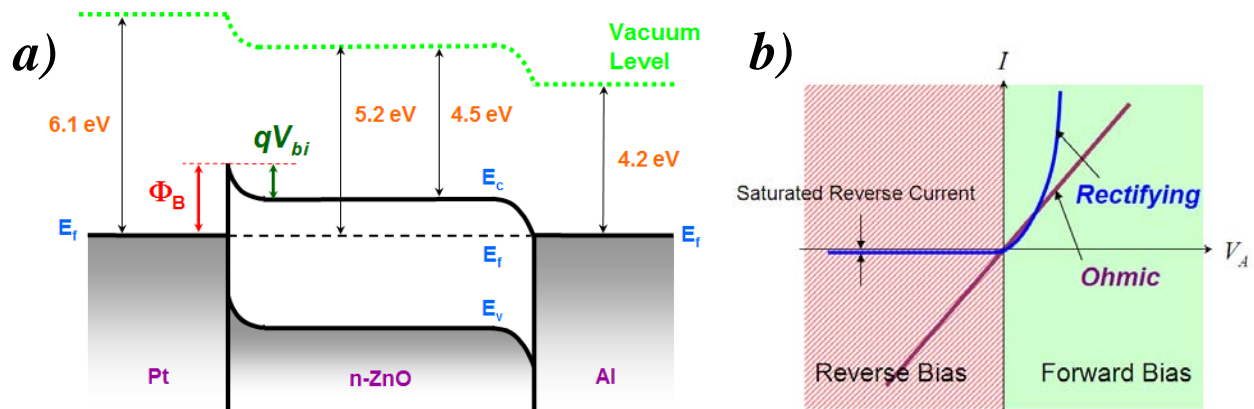


Figure 3-4. a) Energy band diagram under equilibrium conditions for the back-to-back MSM junctions formed when n-type ZnO nanowires are connected to platinum and aluminum electrodes at opposite ends; b) general form of the I-V characteristics of the MS junction.

give rise to linear current-voltage relationships in both forward and reverse-biasing conditions (Figure 3-4b), electric current could flow freely from the metal to the semiconductor, and vice-versa. The rectifying junctions between the platinum electrodes and the ZnO nanowires, on the other hand, require careful examination.

When the rectifying junctions in the 2D ZnO nanowire array are forward-biased ($V_A > 0$), the energy band diagram of the n-ZnO semiconductor moves in the upward direction relative to that of platinum, reducing the barrier seen by electrons in the semiconductor and permitting a net flow of electrons from the semiconductor to the metal (Figure 3-5a). A rapidly-rising forward current is created (Figure 3-4b) when the applied bias is increased because an exponentially-increasing number of electrons from the ZnO semiconductor are able to overcome the surface barrier. If a reverse bias were applied ($V_A < 0$), on the other hand, the energy band diagram of the n-ZnO semiconductor moves in the downward direction relative to that of platinum and increases the surface barrier between the semiconductor and the metal (Figure 3-5b). This blocks the flow of electrons from the ZnO semiconductor to the platinum metal. Some electrons from the metal will still be able to overcome the potential barrier (Φ_B) to reach the semiconductor, contributing to the small, saturating reverse-bias current shown Figure 3-4b.

The flow of electric current and the associated pathways through the 2D ZnO nanowire array could be analyzed according to the schematic illustration in Figure 3-6. When the electric current flows into the 2D array from the bottom platinum electrode, the Schottky MS junction between the platinum electrode and the n-type ZnO nanowire is under forward-biasing conditions and a large current flows from the metal to the ZnO semiconductor, corresponding to the situation depicted in Figure 3-5a. As the current travels up the nanowire, it encounters the ohmic junction between the n-type ZnO nanowire and the aluminum electrode and freely flows to the top electrode. The current then comes to another ohmic aluminum-ZnO junction at a different node and flows freely across it to the ZnO nanowire. The Schottky junction between

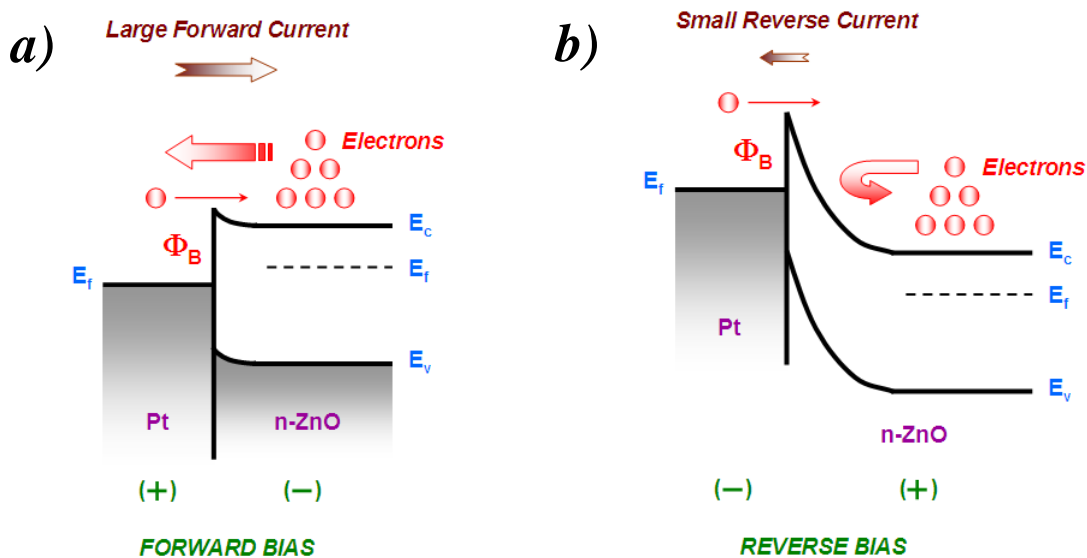


Figure 3-5. Energy band diagrams of the rectifying Schottky junction between Pt and n-ZnO under a) forward-biasing conditions and b) reverse-biasing conditions.

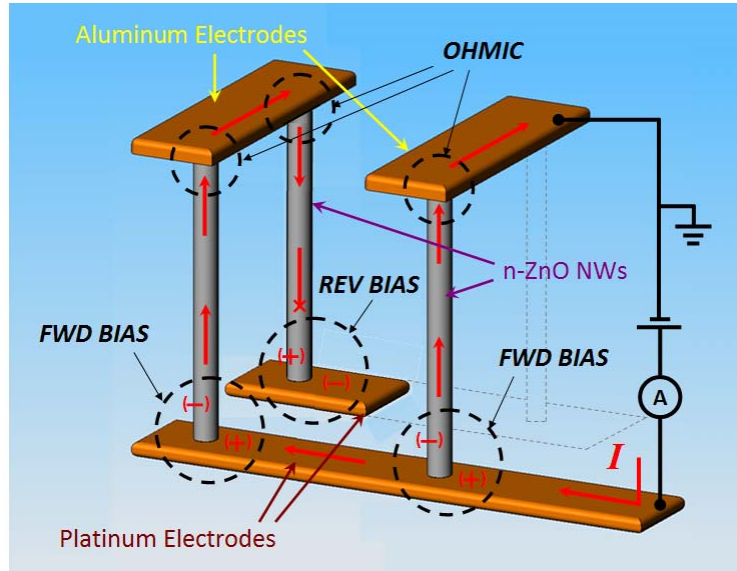


Figure 3-6. Schematic illustration showing that the electric current (red arrows) flows from the bottom platinum electrode through the forward-biased Pt-ZnO Schottky junction, the ZnO-Al-ZnO ohmic junctions, and finally being blocked by the reverse-biased ZnO-Pt Schottky junction.

the ZnO nanowire and the platinum bottom electrode that the electric current encounters, lastly, is under a reverse-biased condition and blocks current flow from the semiconductor to the bottom electrode, corresponding to the situation depicted in Figure 3-5b.

If the external electric current source were applied to the top aluminum electrode instead of the bottom platinum electrode, the current from the top electrode would pass freely through the ohmic junction at the Al-ZnO interface and down to the n-type ZnO nanowire. As soon as the current encounters the Schottky junction between the ZnO nanowire and the bottom platinum electrode, the current flow from the semiconductor to the bottom electrode is blocked due to the reverse-biasing condition as illustrated by Figure 3-5b.

Since the multi-path flow of electric current throughout the 2D array is curbed by the directional, rectifying Schottky junctions between the platinum electrodes and the n-type ZnO nanowires, individually-addressability could be realized by the two-dimensional architecture proposed and presented in this dissertation. Details of the fabrication processes used to realize the 2D ZnO nanowire array are presented in the following section.

3.3 ZnO Nanowire Array Fabrication

3.3.1 Overall Fabrication Process

The device architecture of the 2D ZnO nanowire array is identical to that of the CNT array detailed in chapter two, with the only difference being the lack of the trenches etched into the silicon substrate from which the one-dimensional nanostructures grow. Because the areal density of the as-grown ZnO nanowire on the growth substrate (Figure 3-7a) is typically much lower than that of the CNT bundles (Figure 3-7b), it would be difficult to deposit a continuous

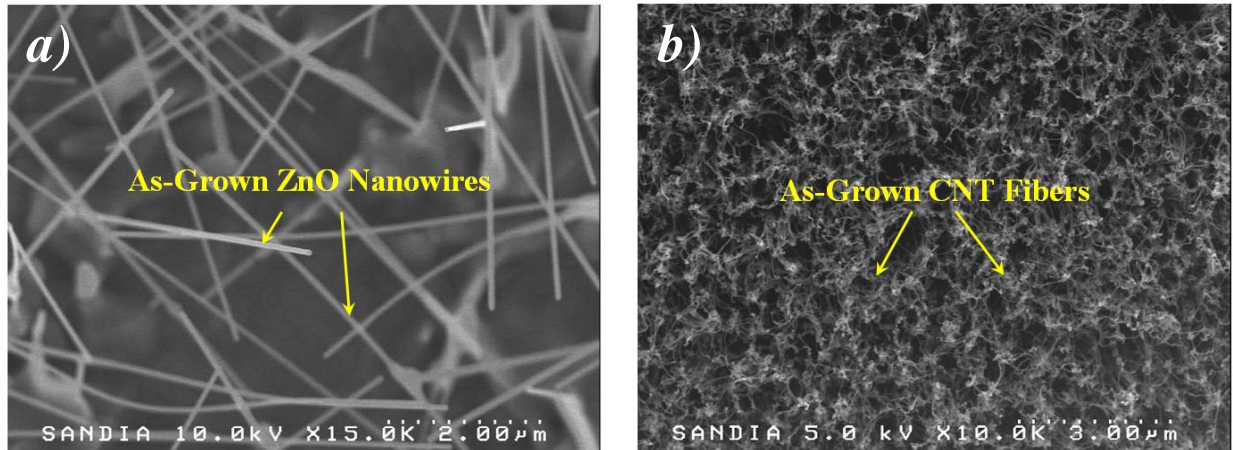


Figure 3-7. SEM images showing a) the low areal density of the as-grown ZnO nanowires versus b) the much denser as-grown CNT structures.

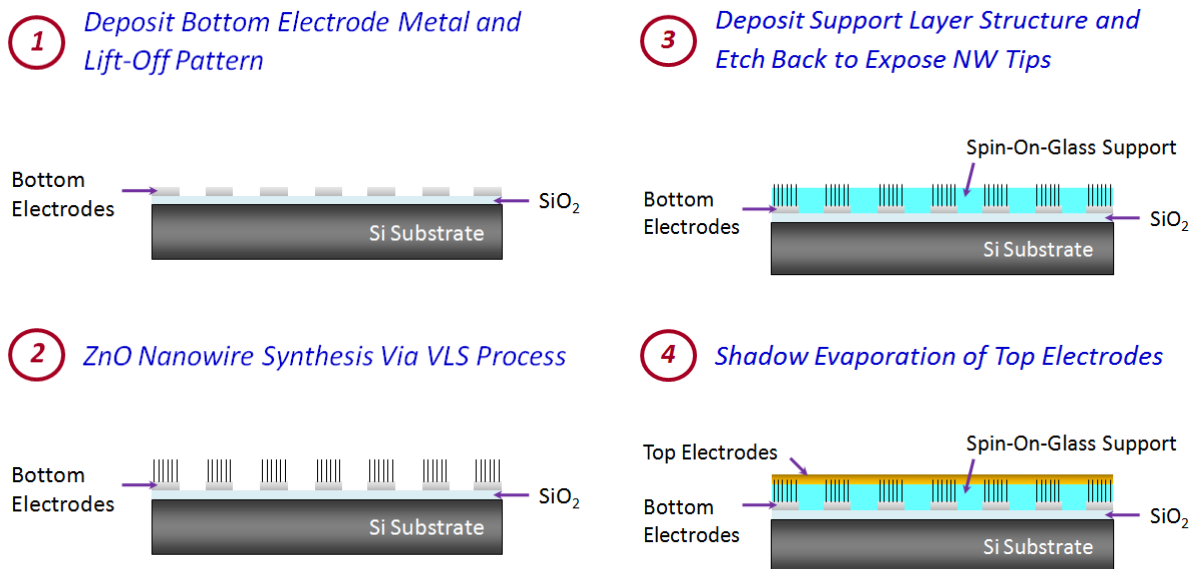


Figure 3-8. Fabrication process flow for the 2D ZnO nanowire array.

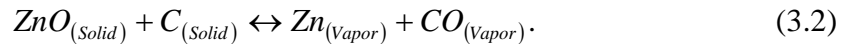
metal film to span the tips of the ZnO nanowires as the top electrodes of the 2D array. As a consequence, the trenches that were etched into the silicon substrate for the CNT array are no longer necessary for the ZnO device. Instead of synthesizing the 1D nanostructures from metal electrodes at the bottom of etched trenches to a height that is level to the top of the trenches, the ZnO nanowires are synthesized from bottom electrodes directly on top of a 1000 Å-thick SiO₂-coated silicon substrate. The fabrication process of the ZnO nanowire array is similar to the proof-of-concept CNT device detailed in Section 2.2 and is presented in Figure 3-8.

Using the Shipley S1813 photoresist recipe detailed in Section 2.1.1, a photolithography step defined the bottom electrode pattern directly on top of the silicon dioxide surface. The width and pitch of the bottom electrodes are approximately 150 μm and 450 μm, respectively. Five nanometers of gold was used as the ZnO nanowire growth catalyst, which was e-beam

evaporated onto a sputtered, bottom-electrode metal film (either aluminum or platinum) measuring 450 nm thick. This RF sputter deposition process was carried out under a chamber pressure of 2.5 mTorr and a RF forward power of 300 watts (PVD Vacuum System CMS-18, Kurt J. Lesker Company). The experimental deposition rates for aluminum and platinum are approximately 33 and 82 Å per minute, respectively. After a metal lift-off process in acetone to form the final bottom electrode pattern (Step 1 of Figure 3-8), the growth substrate was placed into a quartz tube inside the horizontal tube furnace for the synthesis of ZnO nanowires via the vapor-liquid-solid (VLS) crystal growth process (Step 2 of Figure 3-8).

In the ZnO nanowire growth process, an alumina boat (measuring 30 mm in length, 8 mm in width, and 11 mm in depth) was packed with a 1:1 mixture (by weight) of ground ZnO (Puratronic, 99.999% metals basis, Alfa Aesar) and graphite powders (crystalline, 300 mesh, 99%, Alfa Aesar) and placed in the center of the tube furnace. The growth substrates were placed downstream of the source powder on a separate, inverted alumina holder that raised the growth substrate surface to the level of the packed powder (Figure 3-9). The quartz tube was then evacuated to a base pressure of 3 Torr for five minutes and brought back to atmospheric pressure by flowing argon gas into the reaction chamber at 100 SCCM. Once atmospheric pressure was reached, the argon gas flow was decreased to 50 SCCM and oxygen gas was introduced into the chamber at a flow rate of 1 SCCM to promote the oxidation of zinc. The furnace was then heated at a rate of 60 degrees per minute to a temperature of 950°C at the gas-inlet zone while the middle and outlet zones of the furnace were heated to 860°C.

The carbon-assisted thermal (carbothermal) evaporation of the mixture of zinc-oxide and graphite powder is dominated by the following equation [45]:



There are also two possible reactions that involve oxygen in the carbothermal evaporation process:

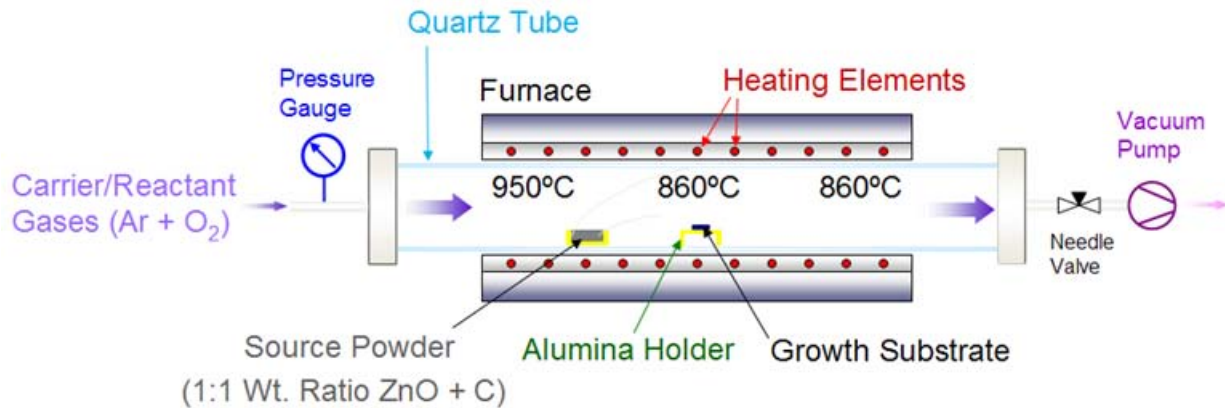
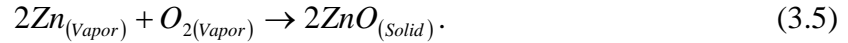


Figure 3-9. Experimental setup for the VLS synthesis of ZnO nanowires in a tube furnace.

The zinc and oxygen vapors are then adsorbed by the gold liquid catalyst particles and further decompose to form zinc-oxide according to the following reaction:



The VLS synthesis of ZnO nanowires is allowed to occur in the reaction chamber for 30 minutes, after which the furnace is allowed to cool to room temperature under constant flow of the gases.

3.3.2 Growth of ZnO Nanowires on Silicon Substrates

The kinetics of the reactions during the carbothermal evaporation and the subsequent re-oxidation of Zn vapors to form ZnO nanowires are highly complex and involve many interdependent variables. Because “low-dimensional” nanostructures such as nanowires are not their thermal equilibrium shapes [46], slight variations in the deposition chamber temperature, pressure, and carrier gas flow rate affect the supersaturation levels in the liquid catalyst particles and greatly alter the morphology of the resulting nanostructures. The supersaturation level within the reaction chamber has been correlated to produce different types of nanostructures on silicon substrates according to the plot presented in Figure 3-10 [47]. These published results are consistent with the experimental results presented by the SEM images shown in Figure 3-11.

Four identical <100> silicon growth substrates measuring 3x3 mm² (coated with 5 nm of e-beam evaporated gold) were placed one, five, ten, and fifteen centimeters downstream from the ZnO+C source powder inside a quartz reaction tube measuring 47 mm in outer diameter (low gas flow rate of 25 SCCM). After heating the furnace to the prescribed temperatures of 950°C at the inlet zone and 860°C at the center and outlet zones for 30 minutes and allowing it to cool to

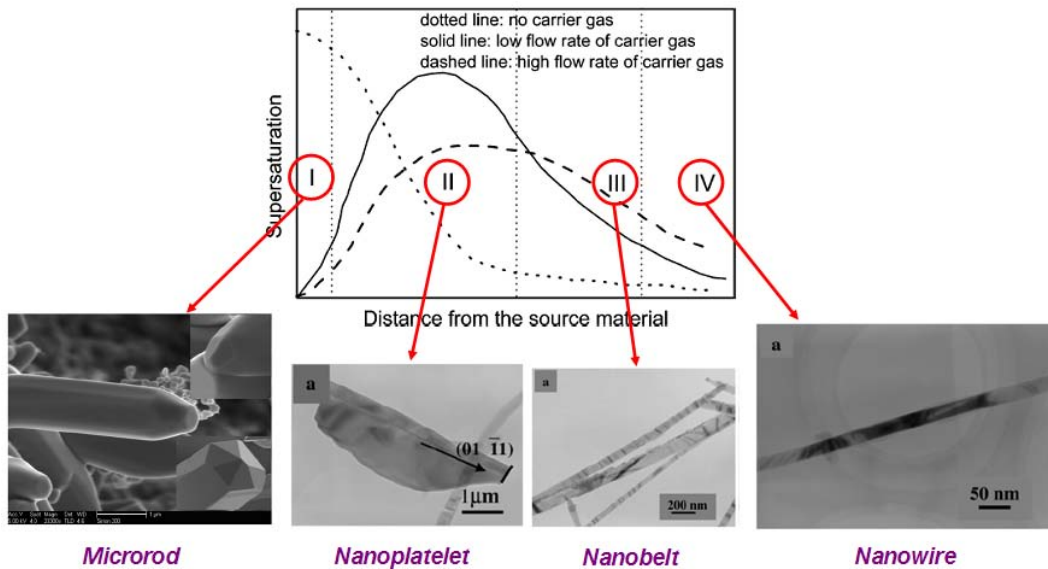


Figure 3-10. Qualitative supersaturation profile of the ZnO vapor in the reaction chamber under low gas flow rate, and the resulting nanostructures that form in each region on plain silicon substrates [47].

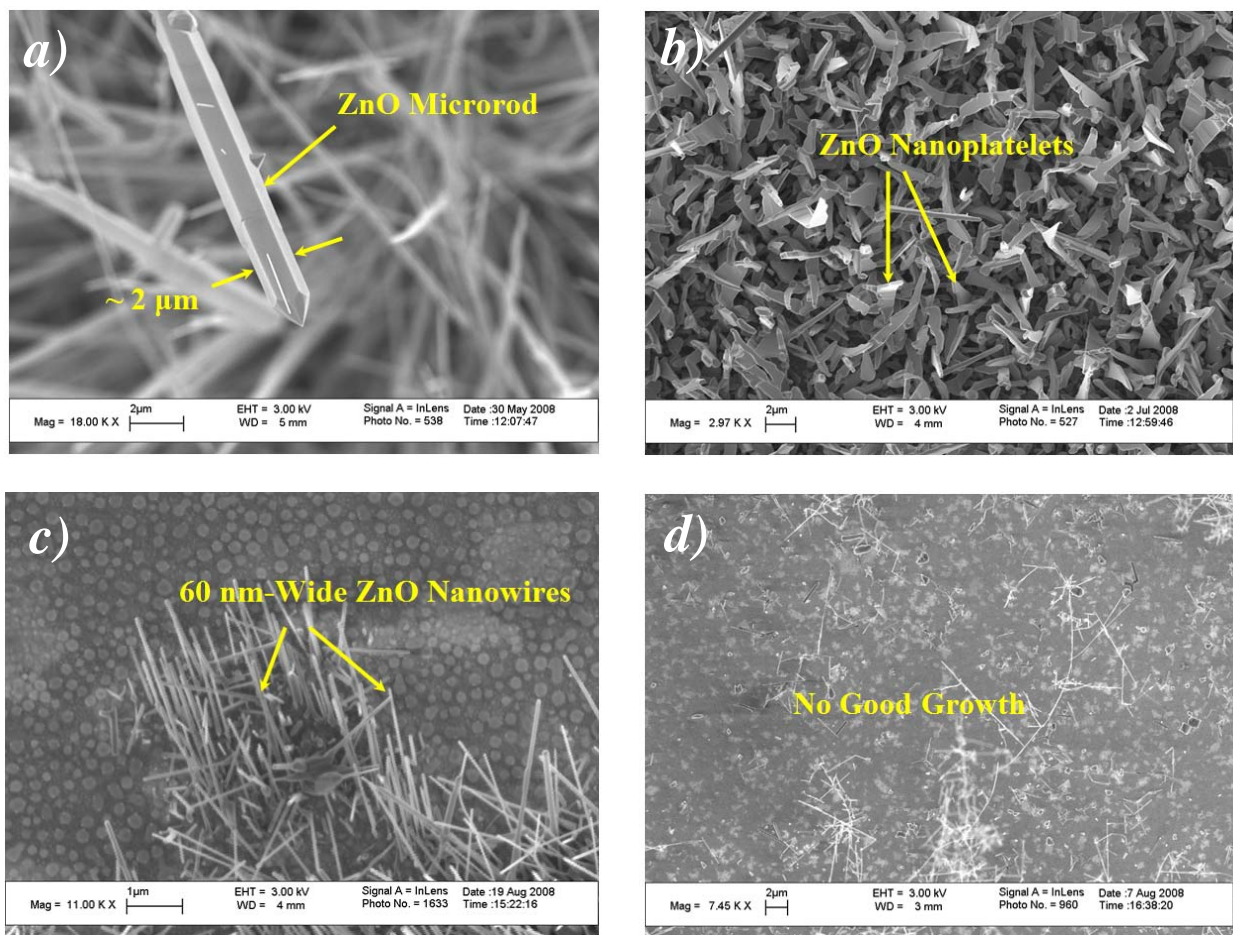


Figure 3-11. SEM images of ZnO nanostructures synthesized in regions of varying supersaturation levels that correspond to those of Figure 3-10: *a)* Region I – ZnO microrod measuring several micrometers in diameter, *b)* Region II – ZnO nanoplatelets, *c)* Region IV – ZnO nanowires measuring 60 nm in diameter, and *d)* no significant nanostructure growth.

room temperature, the resulting ZnO nanostructures synthesized on the substrate that was one centimeter away from the source powder were indeed large microrods that measured several micrometers in diameter (Figure 3-11a). Because the supersaturation level is low at this distance away from the source powder, the ZnO nanostructures grow under conditions close to thermal equilibrium to form rods with well-defined facets that reflect the crystallographic symmetry of hexagonal ZnO [47].

ZnO nanoplatelets were found on the substrate that was five centimeters away (Figure 3-11b). The supersaturation level in this region is the highest, resulting in growth conditions far from thermal equilibrium. The diffusion and incorporation of adsorbed ZnO vapor molecules at high surface-energy side faces of the nanostructure during this growth process result in the formation of nanosheets and nanoplatelets. The nanostructures that were synthesized on the substrate that was 10 centimeters away were ZnO nanowires measuring 60 nm in diameter (Figure 3-11c). In this region, the supersaturation level is low and the adsorbed molecules form quasi-one dimensional morphologies in the form of nanowires. Finally, at a separation distance

of fifteen centimeters between the source powder and the growth substrate where the supersaturation level is very low, there is no significant nanostructure growth (Figure 3-11d).

The local temperature at the furnace zone where the deposition growth substrate is located also determines the morphology of the synthesized ZnO nanostructures. Because a sufficiently-high temperature is required to generate Zn vapors during the carbothermal reduction of ZnO, the ZnO+C source powder mixture was always placed in the furnace at the 950°C zone during the following experiments. The deposition chamber pressure (maintained at 23 Torr throughout the growth process) and the source powder-growth substrate separation distance (10 centimeters) were also not changed in the temperature-dependence experiments. When the local temperature was set to 900°C at the middle of the furnace where the growth substrate was located, the synthesized ZnO nanostructures had the morphology of nanobelts and nanoplatelets (Figure 3-12a). The higher temperature in this growth process and the associated non-equilibrium growth kinetics may have contributed to the formation of these nanobelts and nanoplatelets in a situation similar to the one depicted in Figure 3-11b. Decreasing the growth substrate temperature to 860°C resulted in the formation of ZnO nanowires only (Figure 3-12b) since the adsorbed Zn/O atoms no longer have enough thermal diffusion energy at this lower

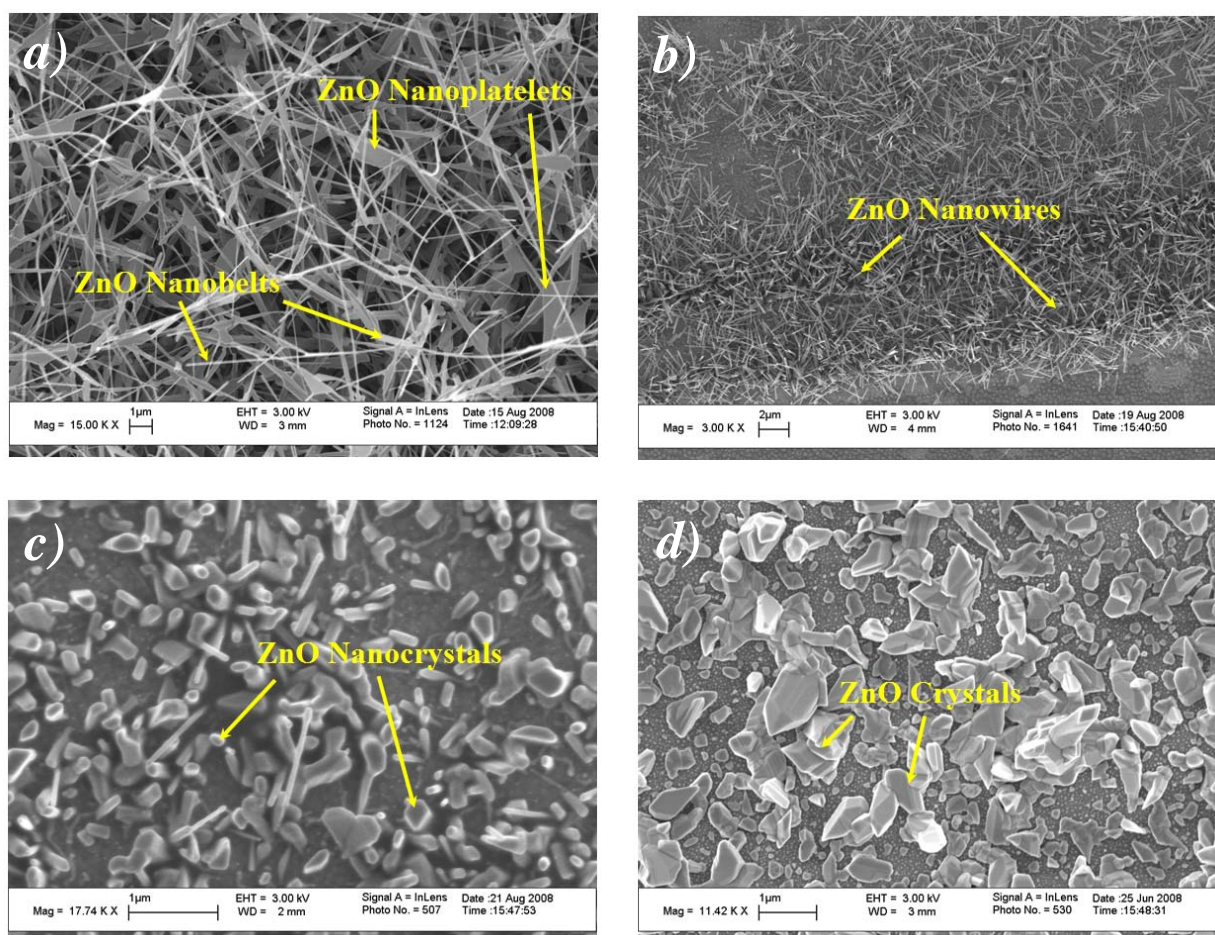


Figure 3-12. SEM images of ZnO nanostructures synthesized at a local zone temperature of a) 900°C, b) 860°C, c) 800°C, and d) 600°C.

temperature to form nanobelts. Decreasing the temperature further to 800°C resulted in the formation of ZnO nanocrystals (Figure 3-12c). At a very low temperature of 600°C, large ZnO crystals were deposited on the growth substrate (Figure 3-12d).

The pressure within the deposition chamber is another synthesis parameter that could greatly affect the growth results. During one ZnO nanowire synthesis experiment, a 3x3 mm² silicon growth chip (coated with 5 nm of gold) was placed directly on top of the ZnO+C source powder and heated to 860°C under a constant argon gas flow of 50 SCCM at atmospheric pressures (760 Torr). After heating the chamber for 30 minutes, the entire setup was allowed to cool to room temperature. The resulting nanostructures that formed on the substrate were very short ZnO nanowires measuring 500 nm in length that originated from the holes where the gold catalyst was located (Figure 3-13a).

In a subsequent growth experiment, all of the parameters remained identical, except for the deposition chamber pressure. After the growth substrate was loaded into the quartz tube and sealed, the chamber was evacuated by a rotary pump to a base pressure of 3 Torr and allowed to heat up to 860°C under the same argon gas flow at 50 SCCM. After holding the temperature at 860°C for 30 minutes, the furnace was again allowed to cool to room temperature. The nanostructures that were synthesized on the substrate in this experiment were very long ZnO nanowires measuring several hundred micrometers that covered the entire growth surface (Figure 3-13b). The low hydrostatic pressure (P_{hyd}) conditions during this experiment resulted in a large ZnO+C solid source evaporation flux (ϕ) according to the following equation:

$$\phi = \frac{\alpha_e (P_{vap} - P_{hyd}) N_a}{(2\pi MRT)^{1/2}} \quad (3.6)$$

where P_{vap} is the equilibrium pressure of the ZnO vapor, N_a is the Avogadro number, M is the molar weight, R is the universal gas constant, T is the chamber temperature, and α_e is the

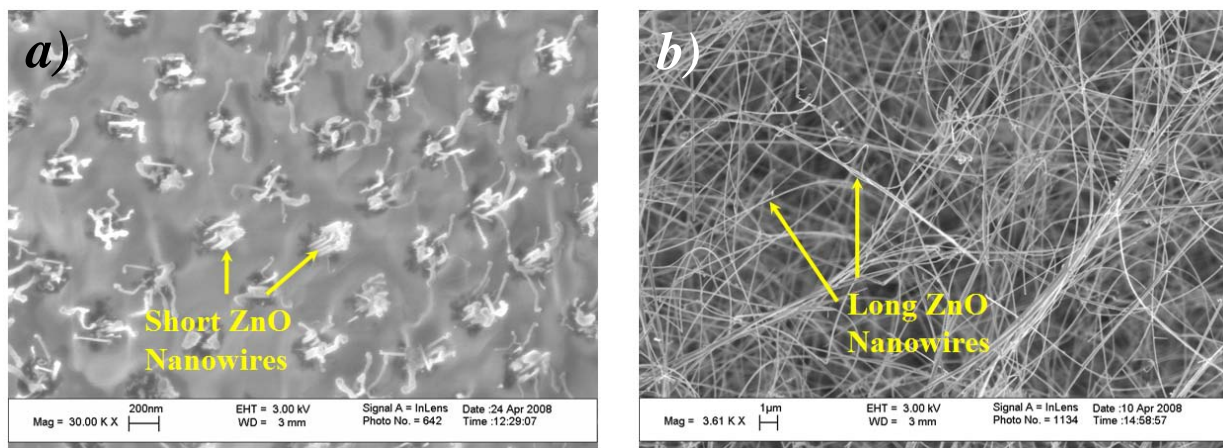


Figure 3-13. SEM images of ZnO nanostructures synthesized at a temperature of 860°C under a chamber pressure of a) 760 Torr and b) 3 Torr.

evaporation coefficient defined as:

$$\alpha_e = \frac{\phi_{ideal}}{\phi_{actual}}. \quad (3.7)$$

This large evaporation flux led to the high reaction and growth rate that resulted in the formation of very long ZnO nanowires shown in Figure 3-13b.

3.3.3 Growth of ZnO Nanowires on Aluminum Electrodes

The selective, patterned synthesis of ZnO nanowires directly on top of metal electrodes is an essential step towards the realization of the two-dimensional array platform based on asymmetric Schottky and ohmic metal-semiconductor contacts. Vertically-aligned ZnO nanowires have been successfully grown directly on top of aluminum and platinum metal electrodes via the vapor-solid-liquid (VLS) synthesis process [48]. Of the two metal materials, aluminum yielded results most suitable for the 2D nanowire array platform because ZnO nanowires were shown to grow only from the electrode areas where the gold catalyst material was present (Figure 3-14a). Patterned growth of ZnO nanowires on platinum metal electrodes was also demonstrated. The growth pattern, however, was not limited only to the areas where the gold catalyst was present, but across the entire metal electrodes (Figure 3-14b). Because the Schottky MS junction in the 2D array could be formed either on the bottom or top metal electrode, aluminum was chosen as the bottom electrode material due to its ability to yield a selective, patterned growth of ZnO nanowires. This would lead to ohmic MS junctions at the bottom electrodes. The Schottky junctions could then be formed at the top MS junctions by using a high work function metal such as platinum as the top electrode material.

Bottom electrodes (measuring 150 μm in width, 5mm in length, and 450 μm in pitch) were formed by sputtering a 450 nm-thick aluminum film into a Shipley S1813 photoresist pattern on a thermally-oxidized (1000 \AA) silicon substrate in a RF sputter deposition process (RF forward power of 300 watts, chamber pressure of 2.5 mTorr). A stainless-steel stencil mask was mounted perpendicular to the metal-deposited photoresist pattern to selectively deposit 5 nm of

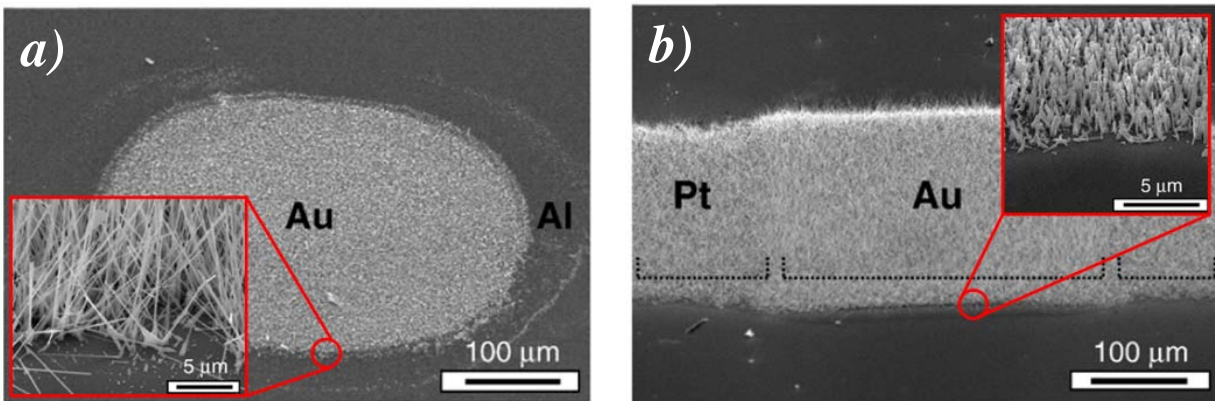


Figure 3-14. Patterned growth of ZnO nanowires from a) aluminum and b) platinum electrodes [48].

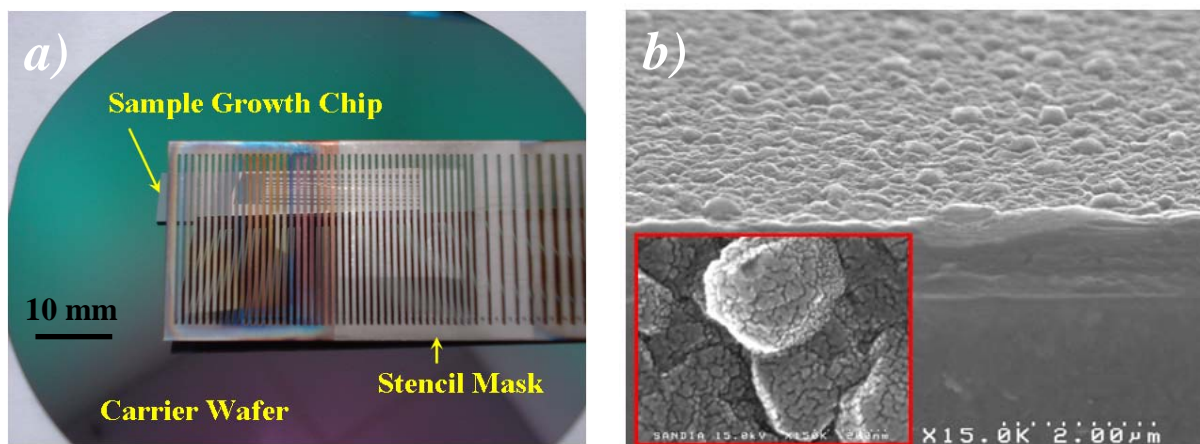


Figure 3-15. a) Stainless steel stencil mask mounted perpendicular to the bottom electrode pattern for the shadow evaporation of the gold catalyst film, b) SEM image of the bottom aluminum electrode with the inset showing the gold catalyst layer over the aluminum film.

gold as the catalyst layer via e-beam evaporation (Figure 3-15a). The stencil mask opening, pitch, and thickness are approximately 1 mm, 2 mm, and 1 mm, respectively. After the metal deposition steps, the photoresist and metal films were removed in a lift-off process to reveal the final bottom electrode structures (Figure 3-15b). The growth chip was then placed into a quartz tube inside the three-zone, horizontal tube furnace (Figure 3-9) for the VLS synthesis of ZnO nanowires.

In order to increase the amount of zinc vapor within the deposition chamber, two alumina boats packed with the ZnO+C source powder mixture were used instead of one boat. A smaller outer-diameter quartz tube measuring 25 mm was used inside the furnace instead of the 47 mm one used in previous experiments. All three zones of the furnace were set to 925°C instead of setting the deposition temperature at 860°C. The argon and oxygen gas flow rates were also changed to 30 SCCM and 1-1.5 SCCM, respectively. Finally, the position of the growth substrate was relocated. Instead of placing it 10 cm away from the source powder boats, the inverted alumina deposition chip holder was placed against the trailing edge of the powder boats while the actual growth substrate was located 1 cm downstream from the leading edge of the inverted holder (Figure 3-16). The smaller diameter quartz tube decreases the reaction chamber volume directly above the source powder and the deposition substrate, resulting in more reactant vapors on the growth substrate and a higher supersaturation level overall. The proximity of the alumina deposition holder to the source powder also increases the supersaturation level on the growth substrate at the gas flow conditions listed above. These changes all contributed to the highly-reproducible ZnO nanowire growth results presented below.

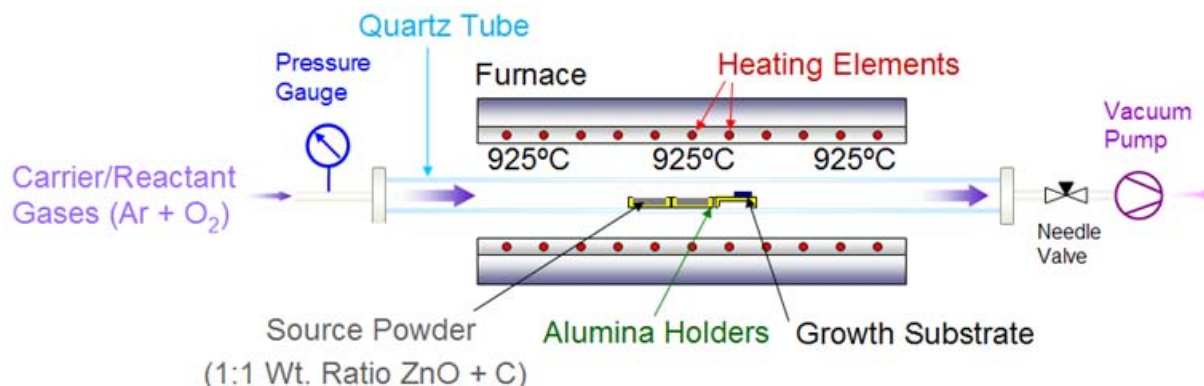


Figure 3-16. Experimental setup for the VLS synthesis of ZnO nanowires on metal electrodes.

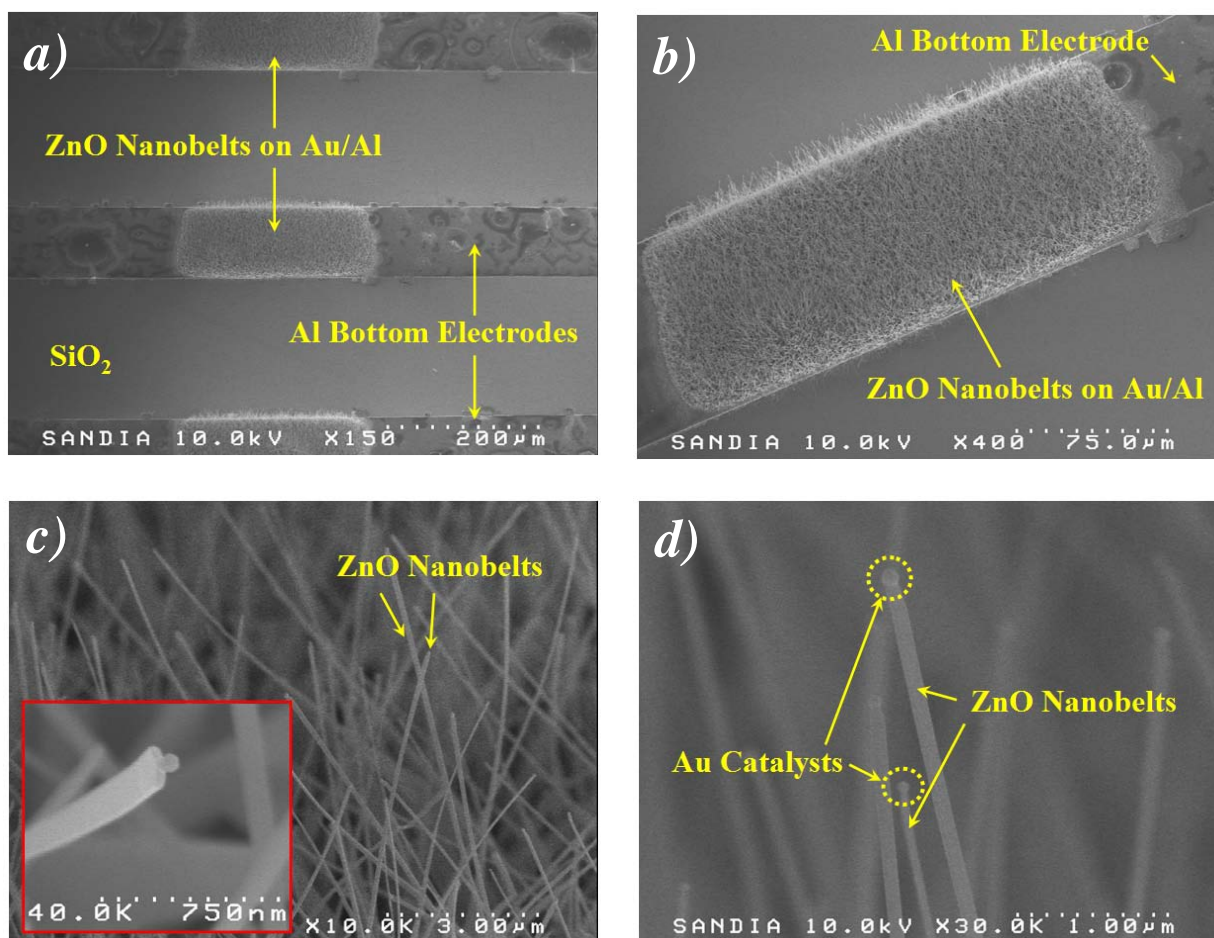


Figure 3-17. SEM images showing the *a)* patterned, selective growth of ZnO nanobelts on aluminum electrodes where the gold catalyst was deposited, *b)* magnified top-down view of the ZnO nanobelt growth, *c)* tilted views of the nanobelts showing the rectangular cross-sectional profile (inset), and *d)* gold catalyst particles at the tips of the nanobelts.

The SEM images presented in Figure 3-17a,b show the growth of ZnO nanostructures selectively on aluminum electrodes where the gold catalyst film was deposited after 15 minutes at 925°C with Ar and O₂ flow rates of 30 and 1.5 SCCM, respectively. The close-up view presented by the SEM image of Figure 3-17c reveals that the synthesized ZnO nanostructures were 15 μm-long nanobelts with rectangular cross-sectional profiles (inset of Figure 3-17c) that measures approximately 100-200 nm in width and 60 nm in thickness. The gold catalyst particles at the end of the ZnO nanobelts (Figure 3-17d) verify that the growth mechanism for these nanostructures indeed follows the vapor-solid-liquid (VLS) process. An Auger surface analysis of these small catalyst tips (Figure 3-18a) confirmed that the main constituents within the particles are zinc (15.2 atomic %), oxygen (20.2 atomic %), and gold (18.4 atomic %). Another Auger surface scan was performed away from the gold catalysts on the ZnO nanobelt body itself (Figure 3-18b) and confirms that the main elements that make up this structure are zinc (24.8 atomic %) and oxygen (26.9 atomic %). The presence of carbon and chlorine from these Auger scans indicates that there are surface contaminations on the sample from the environment.

The quality and integrity of the ZnO nanobelts were characterized optically by measuring their photoluminescence (PL) spectra. The as-synthesized ZnO nanobelts were excited by a continuous-wave helium-cadmium laser (Omnichrome, Series 56) with a wavelength of 325 nm, a measured output power of 5 mW, and an interrogating spot size of approximately 40 μm in diameter. The PL spectrum was then collected by a microscope coupling a multimode fiber to an Ocean Optics Spectrometer (USB-2000). Figure 3-19a presents the PL spectrum of the ZnO nanobelts, illustrating the large band-edge peak centered about 385 nm and the low green defect peak at 550 nm that is attributed to the oxygen vacancy point-defects typically located at the surface of n-type ZnO nanostructures [49]. Optical images of the photoluminescence from the nanobelts under ambient white-light illumination (Figure 3-19b) and under dark conditions (Figure 3-19c) show the violet color associated with the tail of the main band-edge PL peak centered at 385 nm.

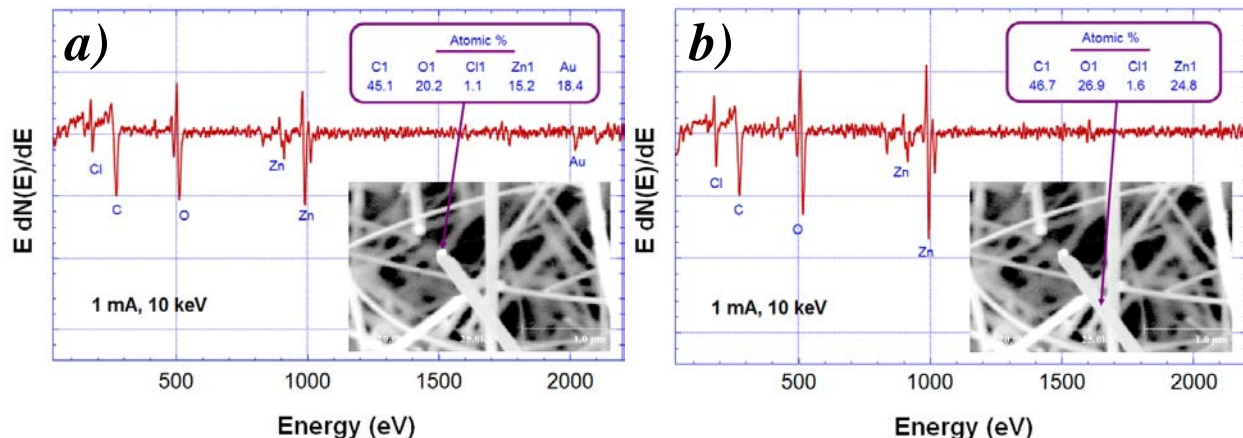


Figure 3-18. Auger surface analysis of the *a)* round catalyst particles at the tips of the ZnO nanobelts and *b)* the main body structure of the nanobelt away from the catalyst particle.

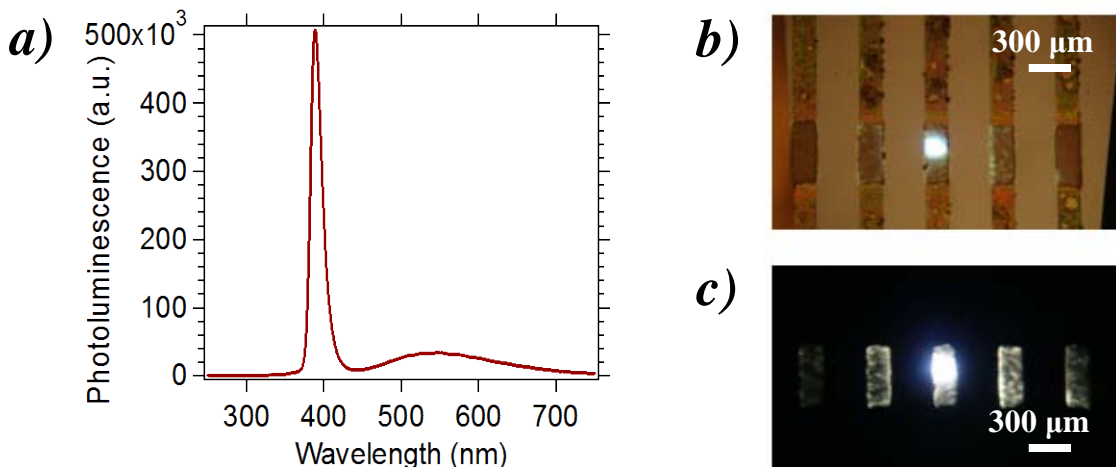


Figure 3-19. a) Photoluminescence spectrum of the as-synthesized ZnO nanobelts. True color optical images of photoluminescence under b) white-light illumination and c) without white-light illumination.

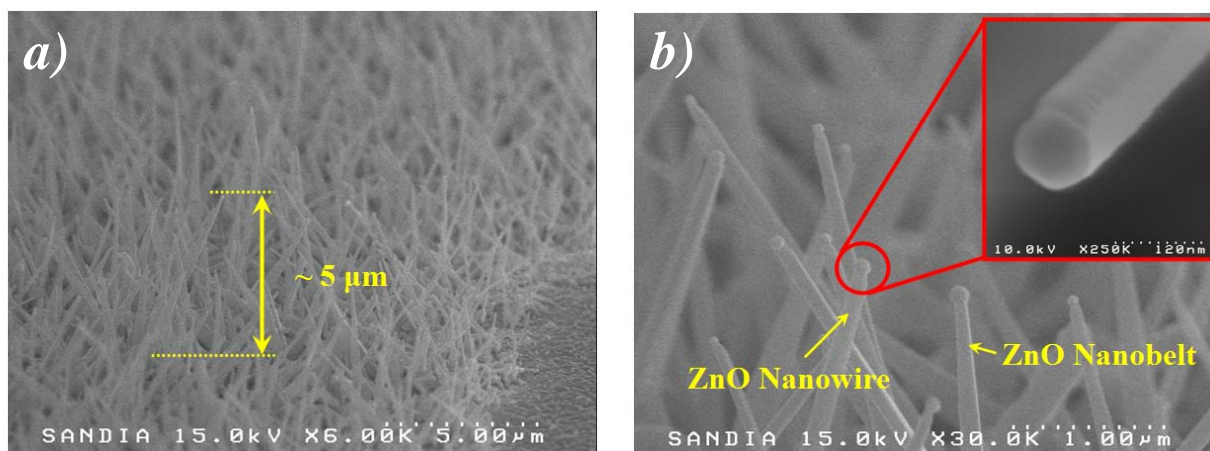


Figure 3-20. SEM images showing the a) patterned, selective growth of ZnO nanobelts on aluminum electrodes where the gold catalyst was deposited, b) magnified

In order to form support structures for the metal top electrodes, a dielectric material such as spin-on-glass SOG-512B must be introduced to fill the voids between the ZnO nanobelts. The 17 μm -long ZnO nanobelts synthesized under the conditions listed above were, however, too long to be planarized by the SOG solution since depositing a layer thicker than 10 μm would introduce severe cracks in the film. The growth conditions, therefore, were altered to yield shorter ZnO nanostructures. By decreasing the oxygen flow rate from 1.5 to 1 SCCM and the growth time from 15 minutes to 12.5 minutes, the synthesized ZnO nanostructure length decreased to approximately 5 μm (Figure 3-20a). In addition to the nanobelts, ZnO nanowires with hexagonal cross-sectional profiles measuring 100 nm in diameter (inset of Figure 3-20b) also appeared on the gold-coated aluminum electrodes alongside the nanobelts (Figure 3-20b).

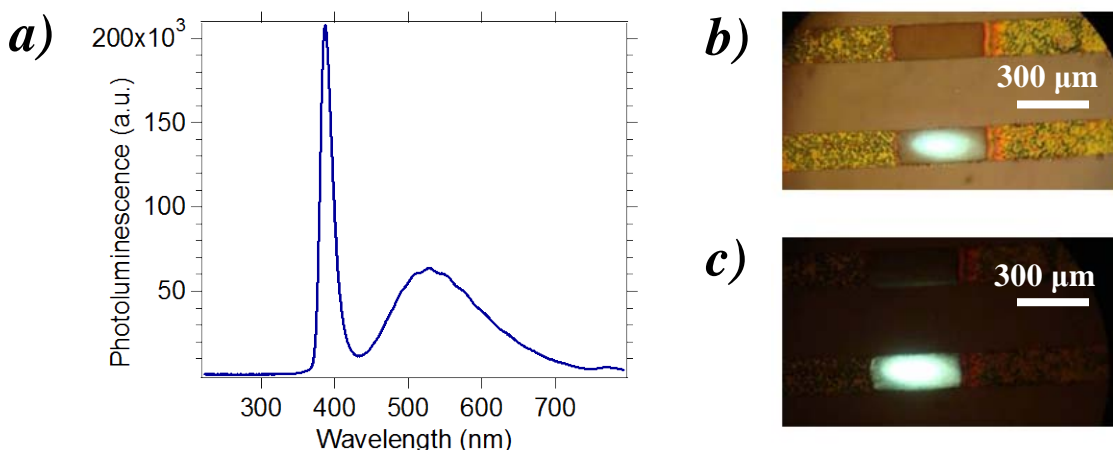


Figure 3-21. a) Photoluminescence spectrum of the as-synthesized ZnO nanowires and nanobelts. True color optical images of photoluminescence under b) white-light illumination and c) without white-light illumination.

The formation of nanowires most likely resulted from the decreased oxygen concentration in the reaction chamber, leading to a slightly lower supersaturation level that could produce both ZnO nanowires and nanobelts.

The photoluminescence spectrum for these 5 μm -long ZnO nanowires and nanobelts is presented in Figure 3-21a, showing a larger defect peak at 530 nm (relative to the main band-edge peak at 385 nm) as compared to that of Figure 3-19a. This could be attributed to the presence of ZnO nanowires and the increased surface area of the hexagonal cross-sectional profile. These six crystal planes (inset of Figure 3-20b) are not as smooth as the four planes on the ZnO nanobelts (inset of Figure 3-17c) and most likely have more surface defects associated with oxygen vacancies that contribute to the green defect peak at 490-560 nm. Optical images of the photoluminescence from the ZnO nanowires and nanobelts under ambient white-light illumination (Figure 3-21b) and under dark conditions (Figure 3-21c) show the mixture of the violet tail of the main band-edge peak at 385 nm and the green color associated with the defect peak centered about 530 nm.

After the selective, patterned growth of ZnO nanowires and nanobelts on aluminum electrodes, a liquid solution of SOG-512B was drop-casted into the ZnO growth area and spun at a spin-speed of 800 rpm for 30 seconds (80 revolutions per second ramp rate). This spin process was repeated two consecutive times to achieve a film that was thick enough to planarize the ZnO growth area. Prior to the SOG deposition steps, a strip of Kapton tape was used to cover approximately 1 mm of the bottom electrodes near one edge of the growth substrate in order to protect that area from the SOG coating and allow probes to make electrical contacts to the bottom electrodes during final device testing. This Kapton tape was removed after the spinning steps and the SOG-coated sample was then cured on hotplates at 90°C, 150°C, and 250°C in succession for 60 seconds each, resulting in a dielectric film thickness of approximately 4 μm that allowed the tips of the 5 μm -long ZnO nanostructures to be exposed (Figure 3-22a). After removing the thin SOG deposit from the tips of the ZnO nanostructures in a 75 second oxygen RIE plasma etch at a RF power of 30 watts, chamber pressure of 5 mTorr, O₂ flowrate of 25 SCCM (Figure 3-22b), 50 nm of palladium was e-beam evaporated through the stainless steel

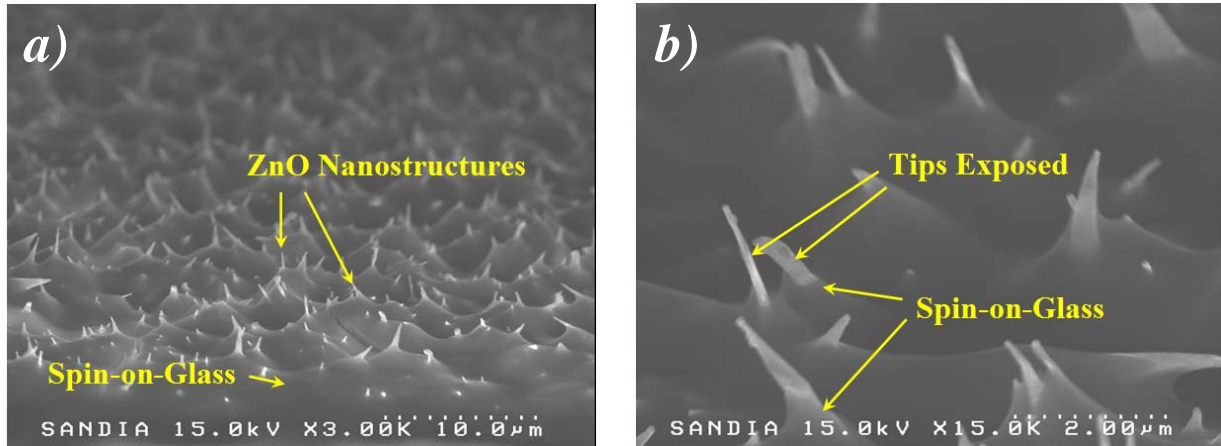


Figure 3-22. SEM images showing *a)* the 5 µm-tall ZnO nanostructures embedded in a 4 µm-thick SOG layer and *b)* the tips of ZnO nanostructures exposed after a 75-second oxygen plasma etch.

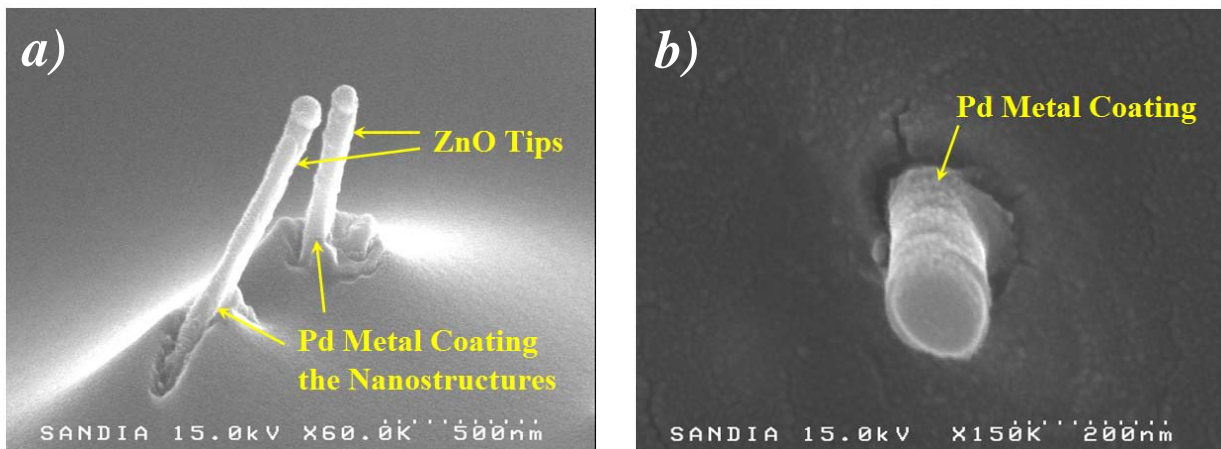


Figure 3-23. SEM images showing *a)* tilted view of the Pd top electrode contacts to the tips of ZnO nanostructures and *b)* top-down view of the 50 nm Pd metal coating on the ZnO tips.

stencil mask (mounted perpendicular to the bottom electrodes and aligned with the nanostructure growth area under an optical microscope) to form the top electrode contacts to the exposed nanostructure tips and complete the device (Figure 3-23). Palladium has a large metal work function (5.6 eV) that is comparable to platinum (6.1 eV) and capable forming Schottky MS contacts to the n-type ZnO nanostructures. Palladium was chosen to replace platinum because of its better metal adhesion characteristics.

Two completed 2D ZnO nanostructure arrays are shown in Figure 3-24. The device shown in Figure 3-24a has three top palladium electrodes that measure approximately 500 µm wide (pictured in red) and five bottom electrodes that measure approximately 150 µm wide (pictured in purple), forming a 3x5 array with 15 nodes that connect the top electrodes to the bottom electrodes via the ZnO nanostructures (pictured in yellow). The 5x10 device shown in Figure 3-24b has five top electrodes (other two electrodes cut off from the field of view) and 10 bottom electrodes that form 50 ZnO nanostructure nodes.

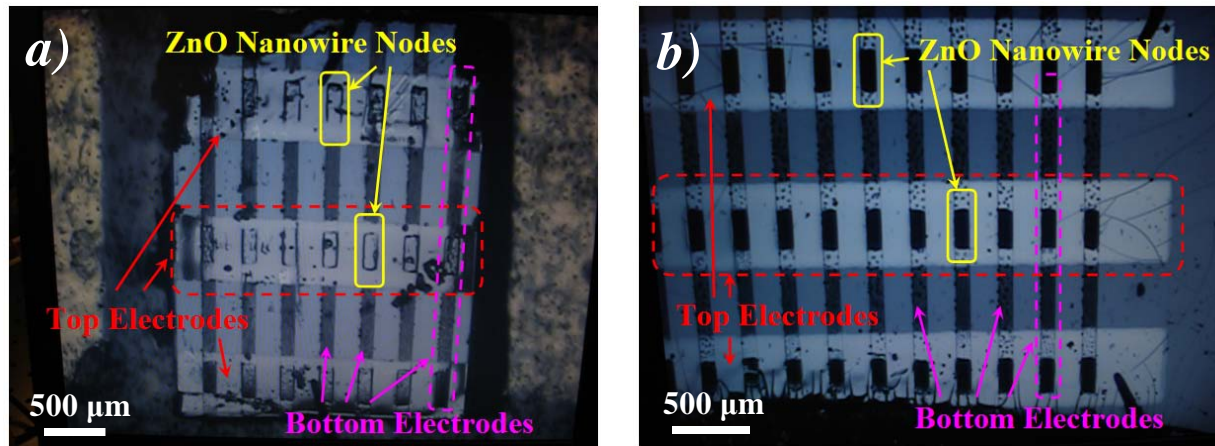


Figure 3-24. Optical images of a) 3x5 2D array based on ZnO nanostructures and b) 5x10 device.

The current-voltage characteristics of the two completed 2D array based on ZnO nanowires and nanobelts grown from aluminum bottom electrodes were measured under a probe station. However, it was discovered that the bottom aluminum electrodes were completely oxidized during the ZnO nanostructure synthesis process. Because the VLS synthesis process was carried out at a temperature of 950°C that is well beyond the melting point of aluminum (660°C), the aluminum electrodes oxidized in the reaction chamber where oxygen was intentionally introduced to promote the oxidization of zinc vapors to form ZnO nanostructures and were no longer conductive to provide I-V characteristics of the fabricated 2D arrays. The metal material for the bottom electrodes, therefore, needed to be changed to a metal that would not oxidize in an oxygen environment under high temperatures.

3.3.4 Growth of ZnO Nanowires on Platinum Electrodes

Platinum is a logical alternative bottom electrode material to aluminum due to its very high melting temperature (1768°C) and the fact that it is possible to synthesize ZnO nanowires directly on top of platinum metal electrodes (Figure 3-14b). The design of the 2D ZnO nanowire array architecture would simply change to include the Schottky MS junctions at the bottom platinum electrodes and ohmic MS junctions at the top aluminum electrodes. Although the growth of ZnO nanostructures would no longer be selectively confined to areas where the gold catalyst is located along the metal electrode, the 2D array device would still be functional if the entire bottom electrode were covered with ZnO nanowires. The top electrodes would make electrical connections to the nanowires within the nodal area while the nanostructures away from the nodes remain free-standing and unattached electrically.

The growth substrate was similarly prepared by sputtering 450 nm of platinum directly into a photoresist bottom electrode pattern on top of a silicon wafer that was coated with 1000 Å of thermal oxide. A gold catalyst film measuring 5 nm in thickness was also selectively deposited onto the platinum electrodes with the stainless steel stencil mask. After lift-off, the growth substrate was placed 2.5 cm away from the source powder boats and heated to 950°C for 30 minutes. The argon and oxygen gas flow rates were increased to 50 and 2.5 SCCM, respectively, during the growth process. The SEM images presented in Figure 3-25a,b show the growth of ZnO nanowires across the entire platinum electrode. The nanowires that grew on top

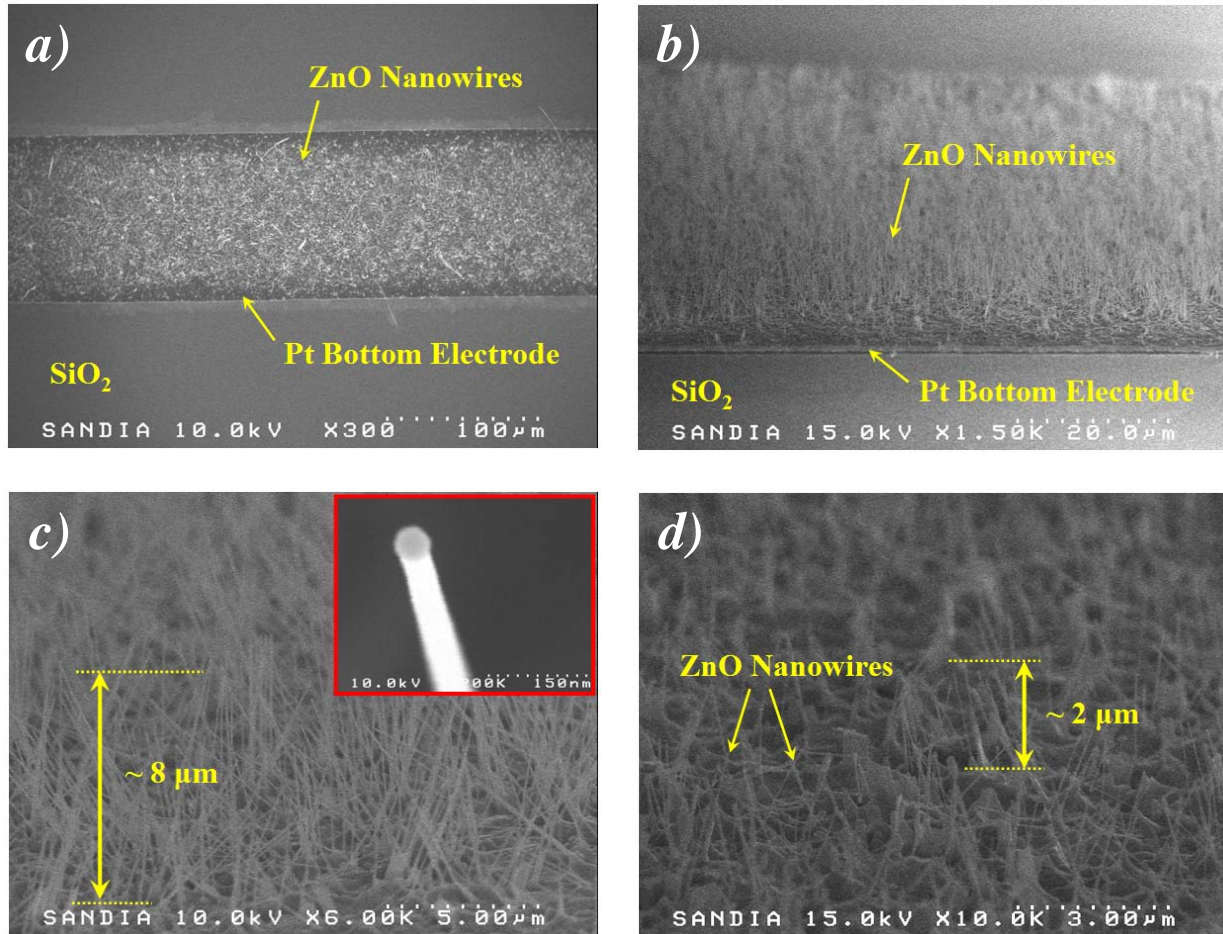


Figure 3-25. SEM images showing the *a)* patterned growth of ZnO nanowires on a platinum electrode, *b)* magnified tilted view of the ZnO nanowire growth, *c)* 8 μm-long nanowires densely packed with hexagonal cross-sectional profile (inset) grown on top of the gold catalyst film, and *d)* sparsely packed 2 μm-long nanowires grown on platinum electrode without the gold catalyst.

of the platinum electrode where the gold catalyst layer was present were densely packed and measured approximately 8 μm in length and 60 nm in diameter (Figure 3-25c) while those that grew from areas where there was no gold were sparsely packed and measured approximately 2 μm in length (Figure 3-25d).

After the patterned growth of ZnO nanowires on platinum electrodes, the 512B spin-on-glass solution was drop-casted into the ZnO growth area following the same process as the one used for the aluminum bottom electrode device. However, care was taken to introduce the SOG solution away from the nanowire growth areas and allow capillary forces to wick the solution in so that the thin nanowires were not toppled over. The SEM image presented in Figure 3-26a show the 8 μm-long ZnO nanowires embedded in the SOG film while the image in Figure 3-26b show the removal of the thin SOG deposit from the tips of the nanowires after a five-minute oxygen plasma etch (RF power of 30 watts, chamber pressure of 5 mTorr, and O₂ flowrate of 25 SCCM). The stainless steel stencil mask was again mounted perpendicular to the bottom electrodes and aligned with the gold catalyst areas under an optical microscope. 100 nm of titanium and 100 nm of gold were then e-beam evaporated onto the SOG-coated growth substrate

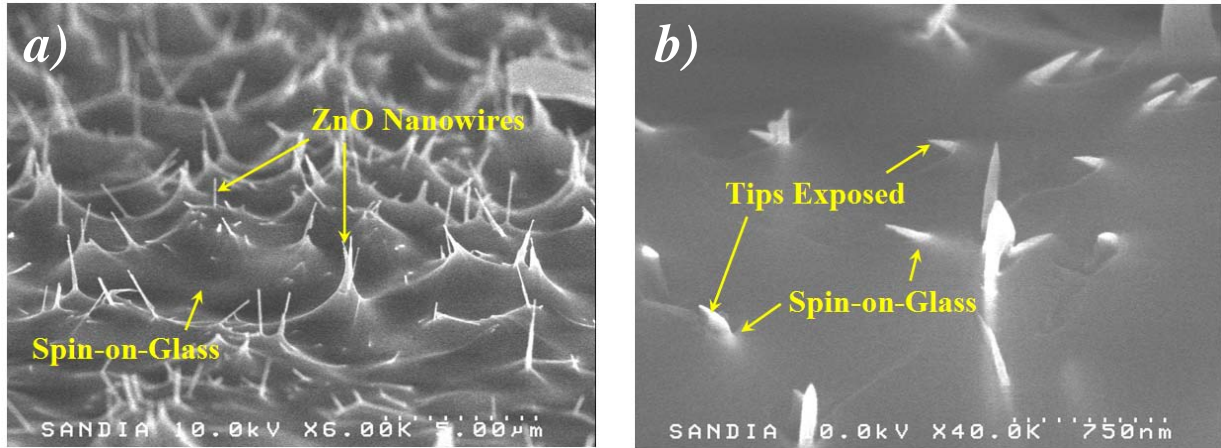


Figure 3-26. SEM images showing *a)* the 8 μm -tall ZnO nanowires embedded in a 4 μm -thick SOG layer and *b)* the tips of ZnO nanostructures exposed after a 5-minute oxygen plasma etch.

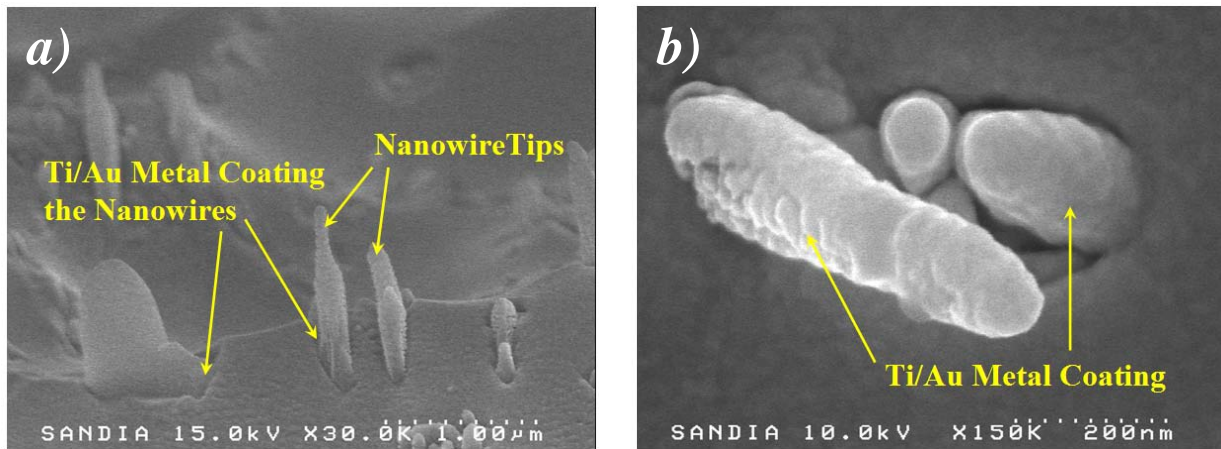


Figure 3-27. SEM images showing *a)* tilted view of the Ti/Au top electrode contacts to the tips of ZnO nanostructures and *b)* top-down view of the Ti/Au metal coating on the ZnO tips.

to form the top contacts to the exposed nanowire tips and complete the device fabrication (Figure 3-27). Titanium was chosen as the ohmic top electrode material because of its good metal adhesion characteristics while the gold capping layer serves to prevent oxidation of the titanium contacts. Titanium has a metal work function (4.3 eV) that is comparable to aluminum (4.2 eV) and is widely used as the metal of choice to form ohmic contacts to n-type ZnO nanowires [50].

The completed 2D ZnO nanowire array is shown in the optical images presented in Figure 3-28. The two top titanium/gold electrodes are approximately 500 μm wide (pictured in red) while the five bottom electrodes are approximately 150 μm wide (pictured in purple), forming a 2x5 array with 10 nodes (pictured in yellow) that could be interrogated by probing the appropriate top and bottom electrodes. Because individual-addressability of the nodes in the 2D array is realized by the Schottky electrical contacts between the bottom electrodes and the vertical zinc-oxide nanowires, as well as the ohmic contacts between the top electrodes and the nanowires, the completed ZnO nanowire array serves as the prime platform for a highly-sensitive UV image sensor. Before optical and electrical characterizations of the 2D ZnO nanowire array

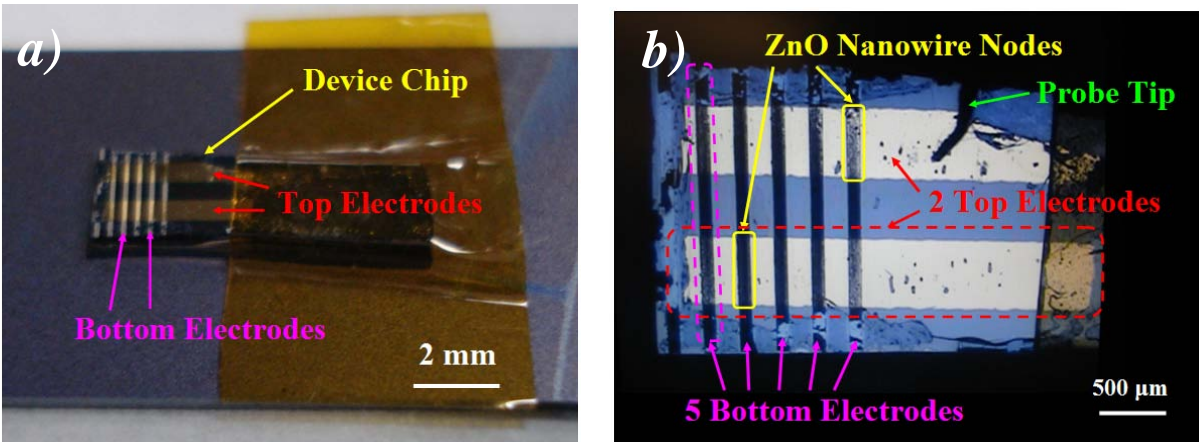


Figure 3-28. Optical images of the completed 2x5 ZnO nanowire array: *a)* direct view and *b)* view through an optical microscope.

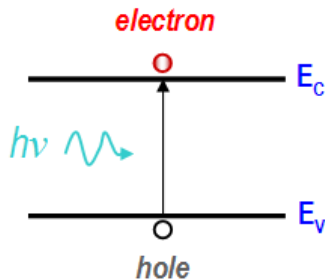


Figure 3-29. Schematic illustration of an electron-hole pair generated in a semiconductor material by the absorption of a photon.

are presented, the fundamental principles of photodetection are introduced in the following section.

3.4 Fundamentals of Photodetection

3.4.1 Operating Principles of a Photodetector

The fundamental processes of photodetection include the absorption of electromagnetic radiation by a semiconductor material, the creation of electron-hole pairs within the semiconductor, and the subsequent separation and collection of these photogenerated charge carriers for detection. Incident radiation with a photon energy ($h\nu$) greater than the bandgap of a semiconducting material could be absorbed to excite an electron from the valence band of the material to its conduction band (Figure 3-29). The resulting electron-hole pair is then separated by an electric field and collected by metal electrodes on opposite sides of the semiconducting material.

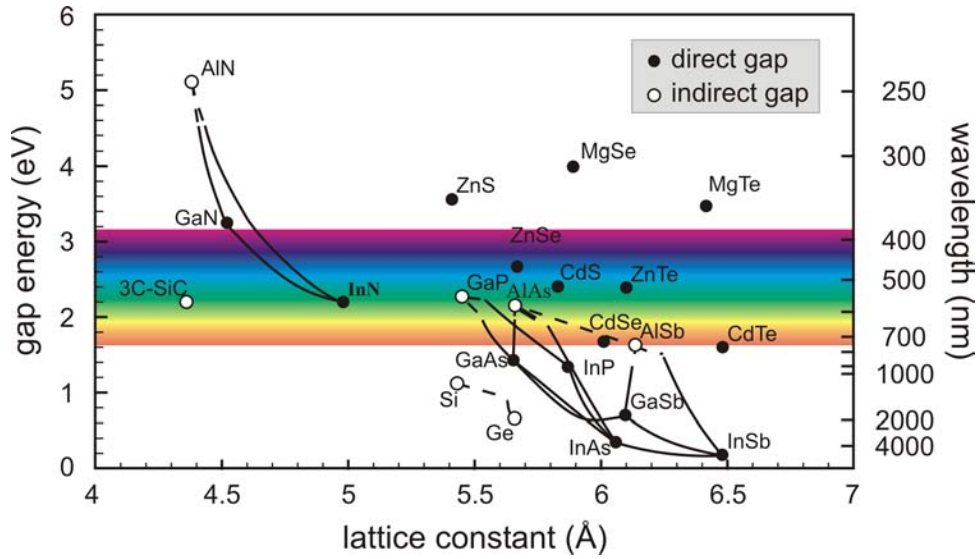


Figure 3-30. Illustration showing the bandgap energy of different semiconducting materials and the corresponding wavelength of light [52].

The material selection for the photodetector is based on the desired detection spectral range for the specific application. The minimum photon energy (E_{ph}) that could be detected by the semiconductor is equal to the bandgap energy (E_g) of the material as given by the following equation [51]:

$$E_{ph} = \frac{hc}{\lambda} > E_g \quad (3-8)$$

where h is Planck's constant, c is the speed of light, and λ is the wavelength of the photon. Rearranging the equation gives the maximum detectable wavelength (in micrometers) for a semiconductor with bandgap, E_g (in electron-Volts), according to:

$$\lambda_{\max} (\mu m) = \frac{1.24}{E_g (eV)} \quad (3-9)$$

The illustration presented in Figure 3-30 depicts the bandgap energy of different semiconducting materials and the corresponding wavelength of light that could be detected [52].

The absorption coefficient of the material used in the photodetector affects the efficiency at which the semiconductor absorbs the incident radiation. The graph in Figure 3-31a shows various semiconducting materials and their corresponding absorption coefficients (α) as a function of wavelength [53]. The sharp drop-off in the absorption curves for direct-bandgap semiconductors such as CdS, GaAs, and GaInAsP indicates that these materials have large absorption coefficients and absorb the incident radiation at specific wavelengths very efficiently. The shallow-sloping absorption curves for indirect-bandgap semiconductors such as Si and Ge, on the other hand, indicate that these materials absorb light less efficiently. The distinction

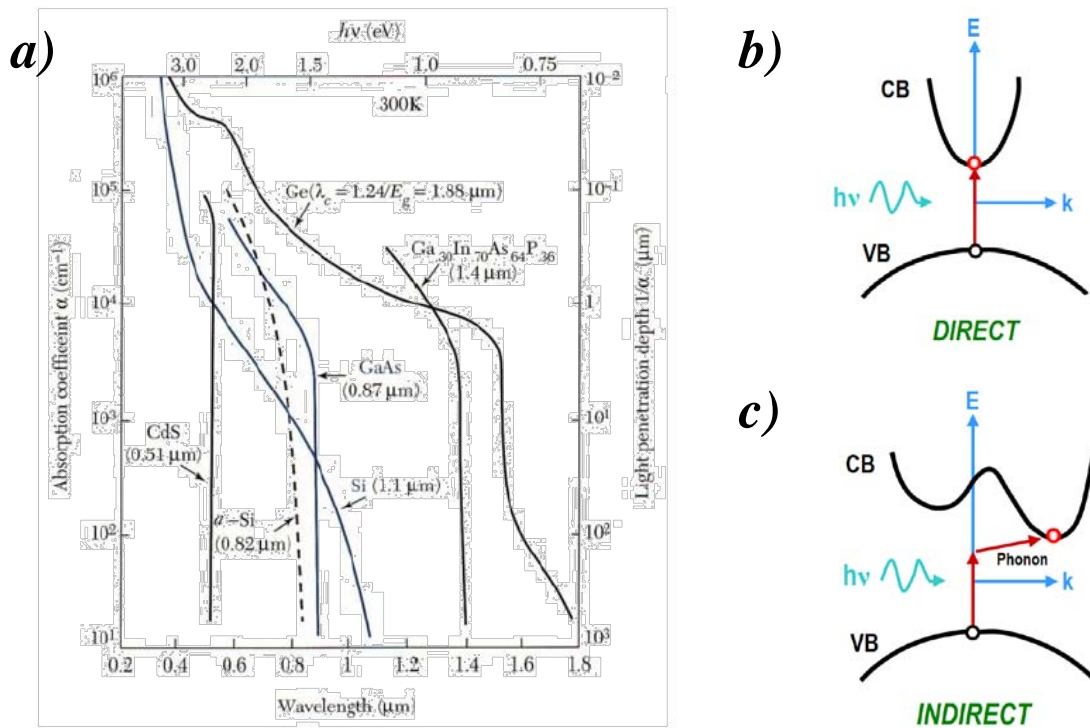


Figure 3-31. a) Absorption coefficients of various semiconductor materials as a function of wavelength [53]. Schematic illustration showing the distinction between b) direct and c) indirect-bandgap semiconductor materials in light absorption.

between the absorption efficiency of direct and indirect-bandgap semiconducting materials is illustrated by the schematics in Figures 3-31b and 3-31c, respectively. In a direct-bandgap semiconductor, the conduction band minimum coincides in energy-momentum (E - k) space with the valence band maximum at the center of the Brillouin zone. Photons could therefore excite electrons across the minimum bandgap without a change in momentum. This is an efficient process involving only two particles and leads to the sharp absorption coefficient (α) for energies greater than E_g . The conduction band minimum of an indirect-bandgap semiconductor, on the other hand, is not aligned with the valence band maximum in E - k space. A photon and a phonon are required to satisfy the energy and momentum changes necessary to excite an electron across the minimum bandgap. Because the likelihood of this three-particle process is lower, the absorption of light in an indirect-bandgap semiconductor is less efficient than an direct-bandgap material, leading to the small increase in α near its minimum bandgap energy.

After the semiconducting material in the photodetector absorbs the incident radiation and electron-hole pairs are created, the photogenerated charge carriers must be separated and collected in order to be detected. These charges are separated by the presence of an electric field induced by either an external bias or a space charge region resulting in a built-in potential in the material. The built-in potential in semiconductor diode junctions is typically found in PN , PIN , metal-semiconductor (MS), metal-semiconductor-metal (MSM), and Avalanche photodetectors. The photodetection capability of the 2D ZnO nanowire array, as presented earlier in this chapter, results from the Schottky MS junctions between the platinum bottom electrodes and the n-type ZnO nanowires.

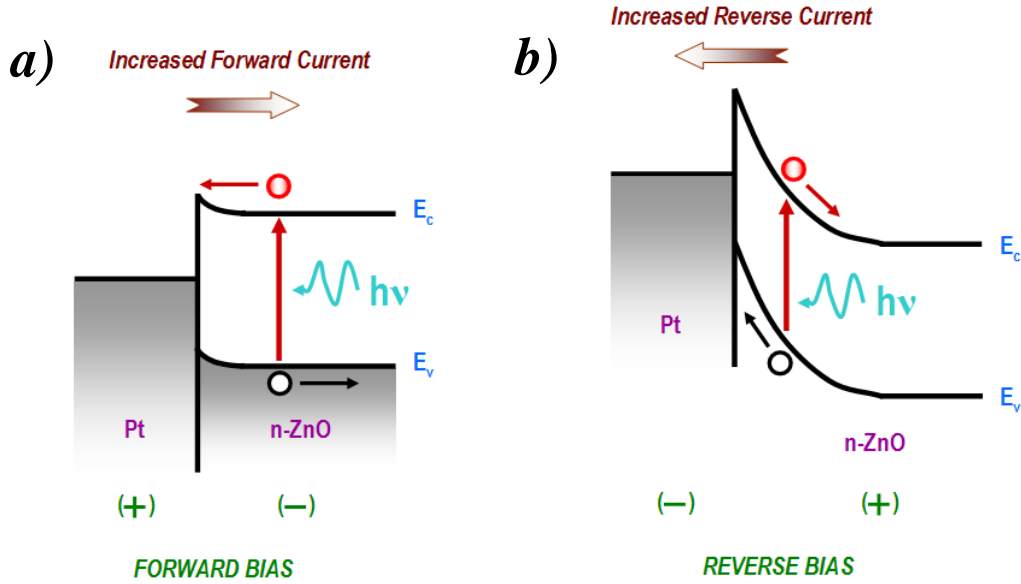


Figure 3-32. Schematic illustrations of the effect of photogenerated current in a MS diode under a) forward-biasing conditions and b) reverse-biasing conditions.

In the Schottky diode, electron-hole pairs generated by the incident radiation will lead to an increase in the forward current as well as the reverse current. When the Schottky MS junction is forward biased, the photogenerated carriers add to the number of available electrons that diffuse across the lowered surface potential (Figure 3-32a). Under reverse-biasing conditions, carriers generated in the space charge region of the n-type ZnO semiconductor experience the built-in potential and contribute to increase the reverse drift current (Figure 3-32b). The current-voltage characteristic of the metal-semiconductor Schottky diode under dark conditions is described by the following equations [53]:

$$I_{dark} = I_o \left(e^{\frac{qV_a}{k_B T}} - 1 \right) \quad (3-10)$$

where I_o is reverse saturation current, V_a is applied voltage, k_B is Boltzmann's constant, and T is temperature. The saturation current is given as:

$$I_o = \frac{4\pi q k_B^2 m_n^*}{h^3} A T^2 e^{-\phi_B/kT} \quad (3-11)$$

where m_n^* is effective mass of the electron, A is cross-sectional area, and Φ_B is the potential barrier height. When incident radiation strikes the Schottky MS diode, the photogenerated electron-hole pairs increase the overall current by an amount I_{ph} according to Equation 3-12.

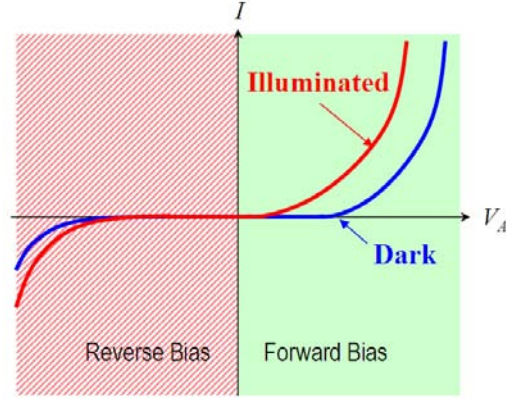


Figure 3-33. General form of the I-V characteristics of an Schottky MS diode under dark and illuminated conditions.

$$I' = I_o \left(e^{qV/k_B T} - 1 \right) + I_{ph} \quad (3-12)$$

The internal quantum efficiency of the material (η_{int}), defined as the probability of generating an electron-hole pair from an absorbed photon that could be separated by the electric field induced by the depletion region, is given by the following equation:

$$\eta_{int} = 1 - \frac{e^{-\alpha\omega}}{1 + \alpha L_p} \quad (3-13)$$

where α is the absorption coefficient, ω is the depletion width, and L_p is the hole diffusion length. Because the number of photogenerated electron-hole pairs that could surmount the potential barrier height (Φ_B) increases exponentially with increasing applied bias, the photocurrent (I_{ph}) is dependent on the photogenerated carrier concentrations (Δn and Δp) and the bias voltage (V_b) and could be approximated as [54]:

$$I_{ph} = q\phi_{photon}\eta_{int} \approx qA \left(\frac{\mu_n \Delta n}{L_n} + \frac{\mu_p \Delta p}{L_p} \right) V_b \quad (3-14)$$

where ϕ_{photon} is the incident photon flux, A is the cross-sectional area, μ is the carrier mobility, and L_n is the electron diffusion length. This photogenerated current contributes to the overall forward and reverse current of the Schottky diode under both forward and reverse-biasing conditions as illustrated by the current-voltage plot in Figure 3-33.

3.4.2 Performance Parameters of a Photodetector

The key parameters that describe the performance of a photodetector include responsivity, signal-to-noise ratio, noise-equivalent power, spectral response, and time response.

Responsivity (R) is defined as the photocurrent that could be extracted from the photodetector, relative to the input optical power, according to the following equation [53]:

$$R = \frac{I_{ph}}{P_{opt}} \quad (3-15)$$

This parameter represents the efficiency of the device in converting incident photons to a detectable electrical signal. The magnitude of this responsivity depends on the material quality and device design. High-quality, defect-free materials minimize the absorption of photons by deep level traps and increase the responsivity of a photodetector. The device could also be designed and engineered to promote the efficient collection of photogenerated charge carriers before they recombine.

Signal-to-noise ratio (SNR) is defined as the ratio of the signal current (I_{ph}) to noise current (I_n). Noise equivalent power (NEP) is the performance parameter that describes the limitations of the photodetector and is defined as the output power of the device at which SNR becomes 1, occurring when the photocurrent (I_{ph}) is equal to the noise current (I_n). This parameter represents the minimum amount of incident light power needed for photodetection.

The spectral response of a photodetector is the detectable spectrum range of the device, with a maximum wavelength value calculated from Equation 3-9. For direct and indirect-bandgap semiconductors, the detectable spectral range include all wavelengths below the maximum wavelength. The NEP and responsivity of indirect-bandgap materials, however, will be lower for wavelength ranges where the bandgap transitions are indirect.

Finally, the time response (τ) of a photodetector represents the time it takes for the photocurrent to fall from 90% to 10% of its maximum value. This performance parameter defines the fastest optical pulses that could be detected by the device.

3.5 ZnO Nanowire Array Characterization Results and Analysis

The completed 2x5 ZnO nanowire array was characterized both optically and electrically for its quality and integrity. The photoluminescence spectra, photoresponse, and current-voltage measurements of the device were collected on a micromanipulator probe station set up according to Figure 3-34. The probe station is mounted to an optical table inside an enclosure with a small opening on its right wall as the entrance for the HeCd UV laser. The laser could be blocked by an external shutter that is controlled remotely. The laser beam is reflected into the microscope by a series of mirrors and focused onto the sample through a 36X objective. Electrical connection to the device substrate is achieved with low-profile, bent probe tips extending into the small clearance space below the objective lens. The photoresponse of the 2D ZnO nanowire array was characterized by collecting current-voltage sweeps with and without the HeCd laser excitation.

3.5.1 Optical and Electrical Characterization

The optical quality of the 8 μm -long ZnO nanowires in the fabricated 2x5 array was analyzed through its photoluminescence spectra. A typical PL spectrum, shown in Figure 3-35a,

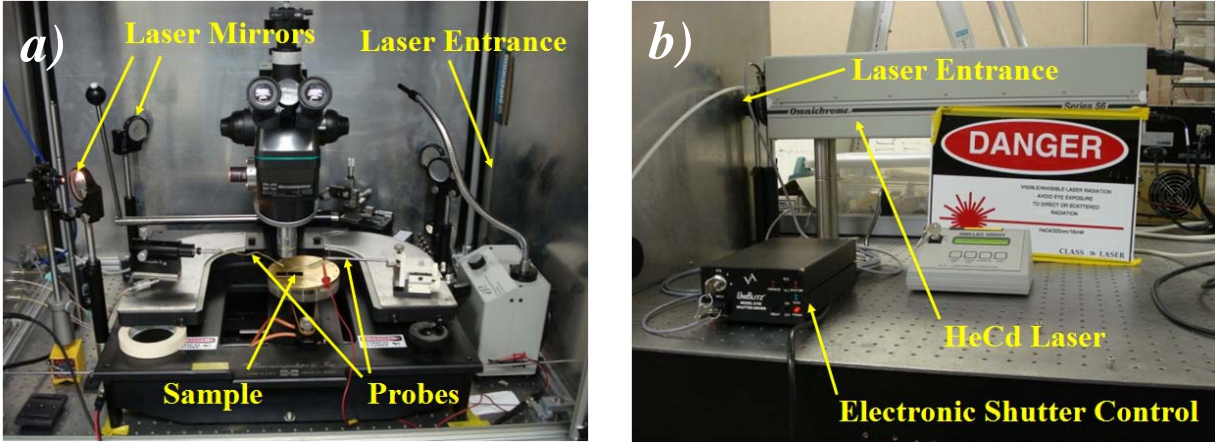


Figure 3-34. Optical images of the experimental setup for device characterization. *a)* Probe station mounted on an optical table inside an enclosure and *b)* a HeCd laser used as the photoexcitation source.

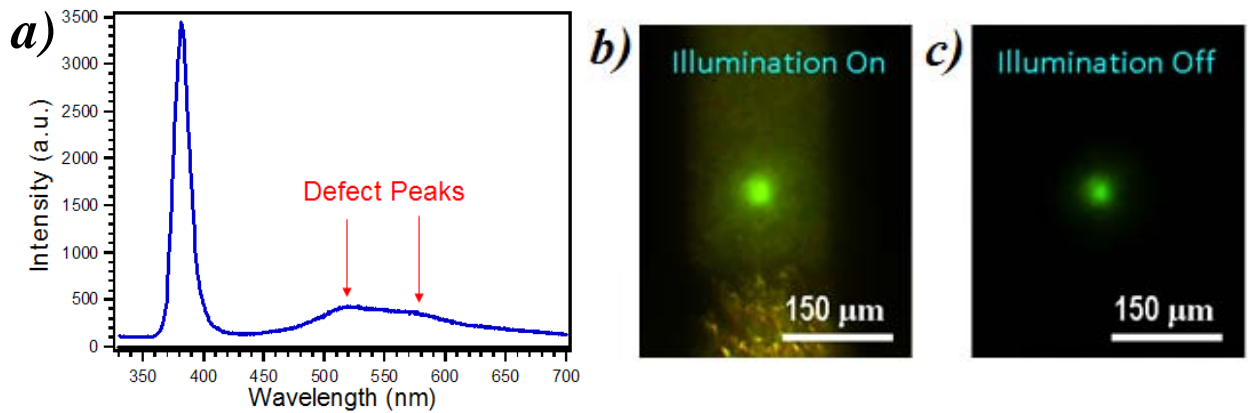


Figure 3-35. *a)* Photoluminescence spectrum of ZnO nanowires synthesized on platinum electrodes. True-color optical images of photoluminescence under *b)* white-light illumination and *c)* without white-light illumination.

contains a large narrow band-edge peak centered about 385 nm and two small defect peaks at 520 nm and 580 nm. The large narrow peak is attributed to inter-band transitions while the green defect peak at 520 nm is attributed to oxygen vacancy point defects at the nanowire surfaces. The yellow defect peak at 580 nm is attributed to oxygen interstitials typically found away from the surface [55]. The large intensity of the band-edge peak with respect to the defect peaks indicates a high quality material where band-to-band transitions dominate. Since the ZnO nanowire synthesis was carried out at a high temperature, the nanowire quality is expected to be high. Optical images of the photoluminescence from the ZnO nanowires under ambient white-light illumination (Figure 3-35b) and under dark conditions (Figure 3-35c) reveal the dominant yellow-green color associated with the defect peaks at 520 nm and 580 nm.

After Ti/Au metal layers were deposited over the ZnO nanowires as the top electrodes, the nanowires were evaluated again for their photoluminescence characteristics to ensure that the

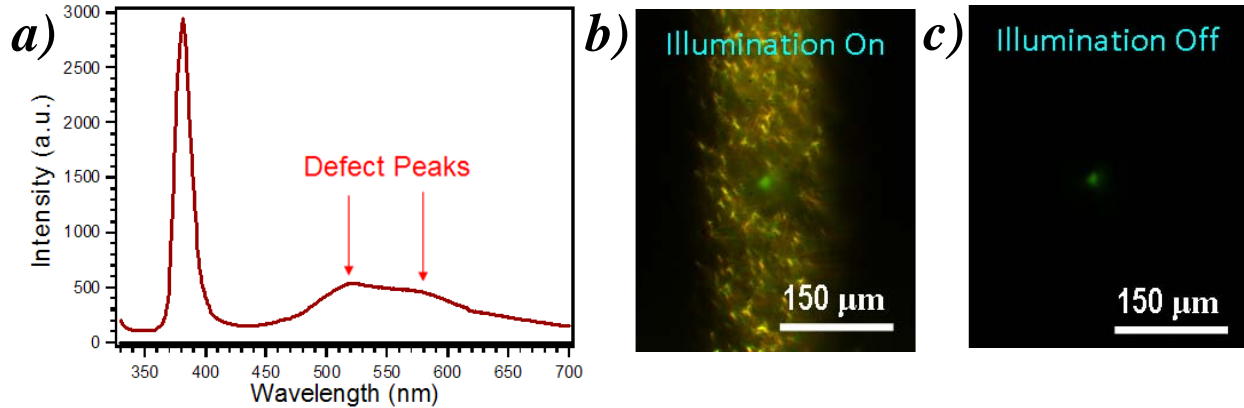


Figure 3-36. *a)* Photoluminescence spectrum of ZnO nanowires after top electrode metal deposition. True-color optical images of photoluminescence with *b)* white light illumination and *c)* without white light illumination.

design architecture still allowed for the laser interrogation of the individual nodes through the top electrodes. As shown by the PL spectrum in Figure 3-36a, the quality of the ZnO nanowires did not degrade after top metal electrode formation. Furthermore, laser excitation and photoluminescence detection were still possible through the top contacts. However, the photoluminescence intensity was lower, but still bright enough to be easily captured by the photographs presented in Figures 3-36b and 3-36c. It is speculated that, although the deposited top electrode metal thickness is relatively thick at 200 nm, optical transparency is still possible due to the irregular surface comprised of nanowire tips. The conformal coating of the metal over this irregular surface most likely led to some thin spots where optical excitation and collection were possible.

The current-voltage (I-V) characteristics of each of the ten nodes in the 2D ZnO nanowire array were measured to analyze the electrical integrity of the top and bottom electrode contacts to the nanowires. As illustrated in Figure 3-37a, four of the ten nodes in the 2D array exhibited rectifying, Schottky current-voltage behavior. The asymmetric Schottky-ohmic contacts that were designed into the array architecture were, therefore, formed correctly for those four nodes. The other six nodes in the 2D array exhibited shorting behavior with resistance values on the order of $\sim 100 \Omega$. A poor SOG filling around the nanowires in these nodes most likely contributed to the formation of pinholes since the SOG solution was drop-casted away from the ZnO nanowires and allowed to wick in from the right side of the device chip (Figure 3-37a). Deposition of the top electrode Ti/Au films then filled these pinholes and created an electrical short between the top and bottom electrodes. The typical I-V curve of a rectifying node (shown in Figure 3-37b) illustrates that the turn-on voltage for the 2D array is approximately 1 V. This value is in good agreement with the theoretical built-in potential (0.9 V) that was calculated in Section 3.2.

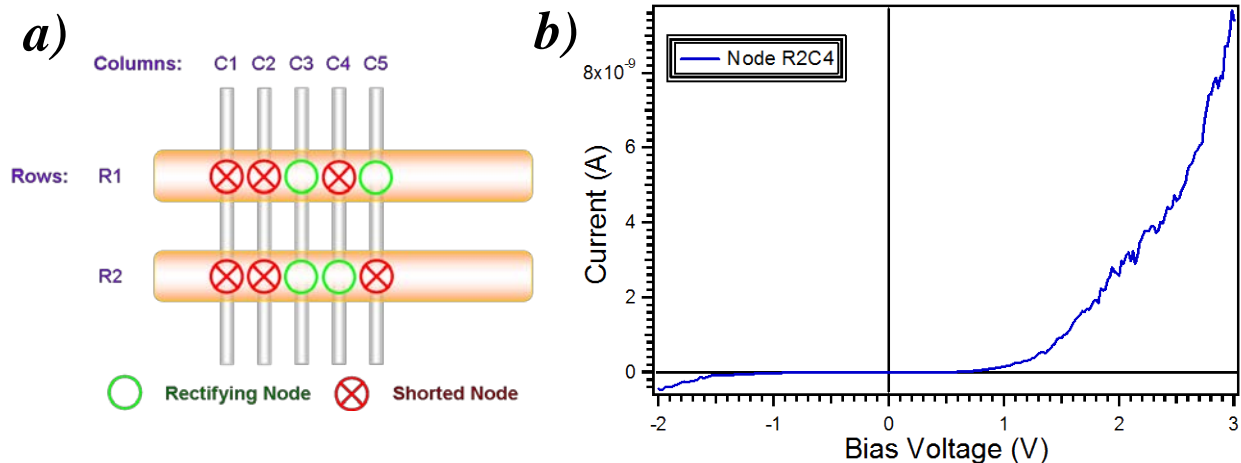


Figure 3-37. a) Schematic illustration showing rectifying nodes and shorted nodes in the completed device. b) Typical current-voltage behavior of a rectifying node.

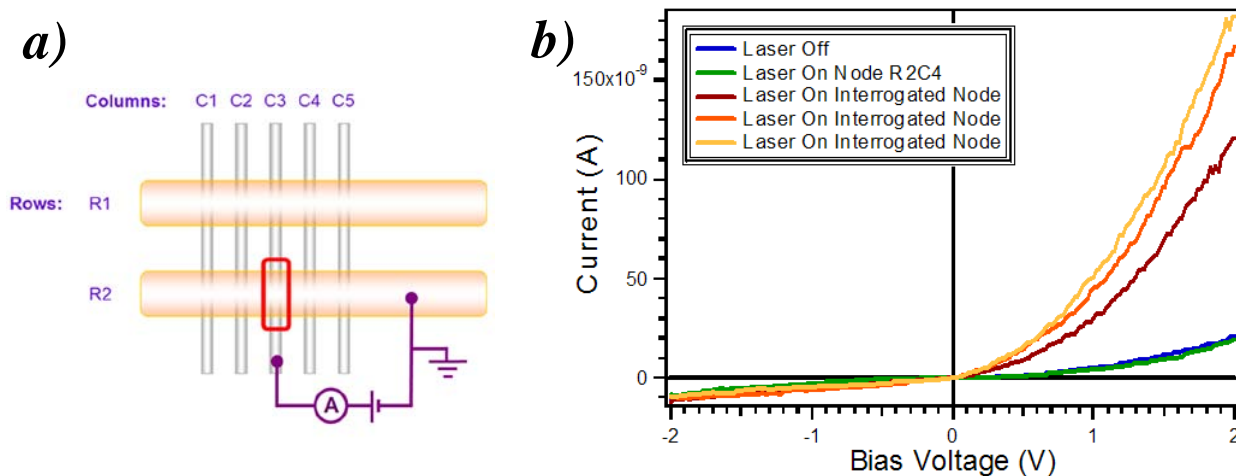


Figure 3-38. a) Schematic illustration showing the interrogated Node R2C3 and b) current-voltage behaviors indicating photodetection and individual-addressability.

The four rectifying, Schottky nodes in the 2D ZnO nanowire array were then tested for their photodetection characteristics. At Node R2C3 (Figure 3-38a), a current-voltage measurement was first taken under dark conditions with the probe station enclosure sealed and all external light sources turned off (blue curve in Figure 3-38b). After the dark measurement was complete, the UV laser source was focused on the node and the current-voltage measurement was taken again. This measurement was repeated several times and the results are plotted as the brown, orange, and gold curves in Figure 3-38b. As illustrated in the graph, the photocurrent generated in the node was repeatable over several cycles of turning the laser on and off. The laser spot was subsequently focused on a separate node (Node R2C4) and the current-voltage measurement was taken again for Node R2C3. The resulting I-V characteristic (green curve in Figure 3-38b) was nearly identical to the dark-current curve, confirming that the

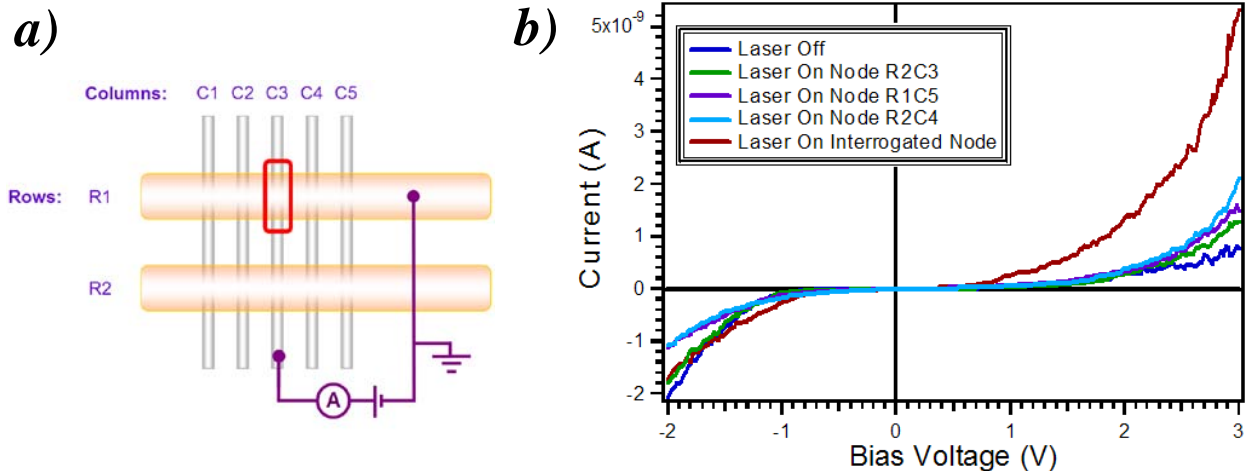


Figure 3-39. a) Schematic illustration showing interrogated *Node RIC3* and b) current-voltage behaviors indicating photodetection and individual-addressability.

electrical circuit was indeed formed through the correct node. This result also verifies the individual-addressability of the 2D nanowire array since the photogenerated current from the laser-excited nanowires in *Node R2C4* had no effect on the current-voltage behavior of the interrogated *Node R2C3*.

The results presented in Figure 3-39 for *Node RIC3* are analogous to the previous measurements. For this analysis, the laser spot was moved to various different node locations. Each laser spot location yielded similar current-voltage behaviors similar to the dark curve. This reaffirms that the photoexcitation of other nodes does not add photocurrent to the interrogated node. Even the close proximity (a separation of 300 μm) of the photo-excited node (*Node R2C3*) to the interrogated *RIC3* node had little effect on the measured current-voltage characteristics.

The electrical characterization of *Node R2C4* yields similar results to the other rectifying nodes (Figure 3-40). Various neighboring nodes were again excited by the HeCd laser, and no photocurrent contribution was apparent in the current-voltage behavior of the interrogated node. The strong rectifying behavior of this particular node is illustrated by the very small saturation current in the reverse-bias region of the I-V curve (Figure 3-40b).

Finally, the results from *Node RIC5* are shown in Figure 3-41. Although this fourth node exhibited a slightly different behavior than the previous three nodes, its current-voltage behavior could still be characterized as rectifying. The conductivity was higher in this particular node and the current-voltage curves were not very smooth. This node may also have pinholes with discontinuous metal pathways between the top and bottom electrodes that push the node to the verge of shorting.

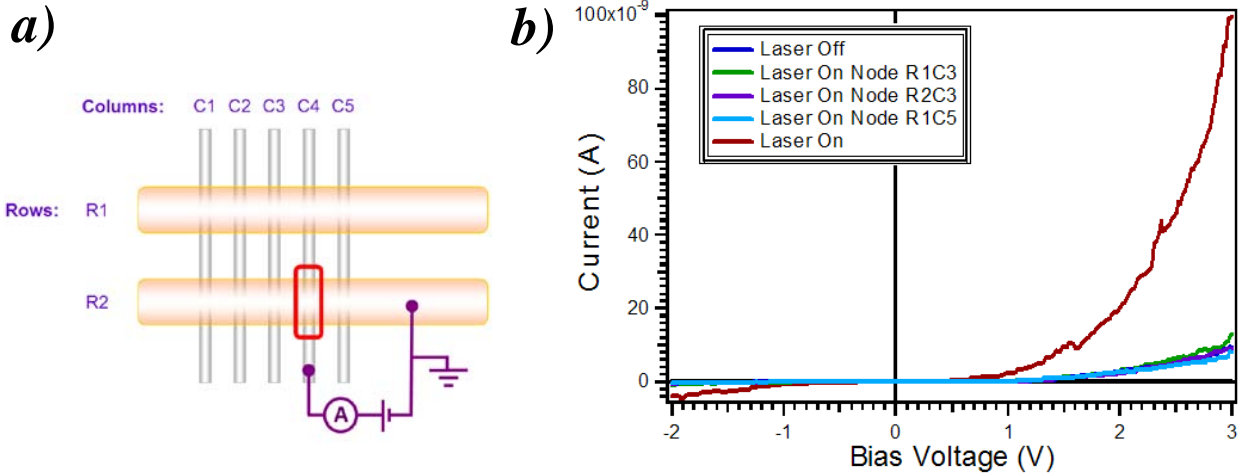


Figure 3-40. a) Schematic illustration showing interrogated *Node R2C4* and b) current-voltage behaviors indicating photodetection and individual-addressability.

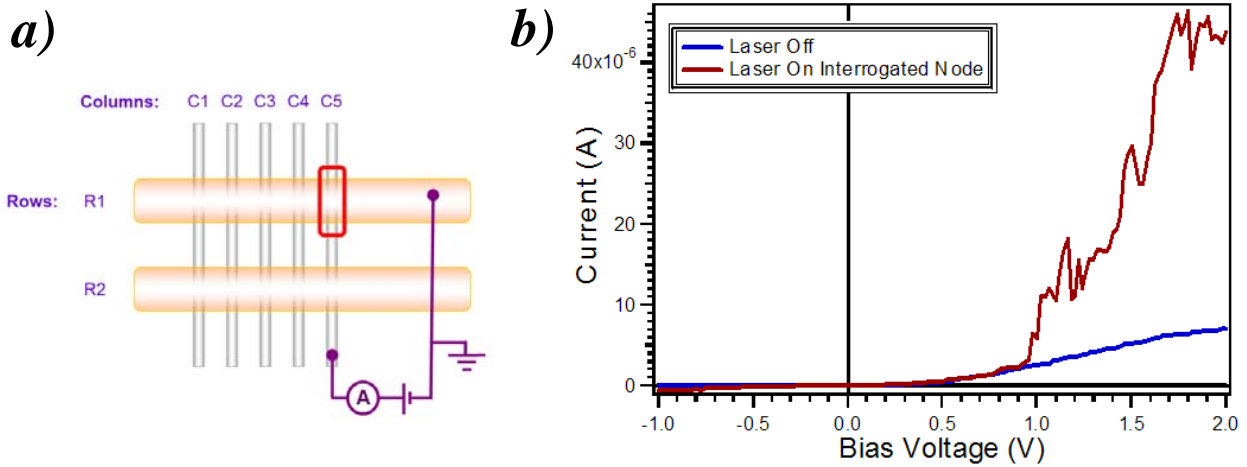


Figure 3-41. a) Schematic illustration showing interrogated *Node R1C5* and b) current-voltage behaviors indicating photodetection.

The 2D ZnO nanowire array was analyzed for its time response characteristics with a constant applied bias of 1 volt imposed across *Node R2C3*. While continuously recording the current across the interrogated node, the UV laser beam was controlled by an electronic shutter to illuminate the sample for five seconds, immediately followed by five seconds of off-time. The time response this node (shown in Figure 3-42b) is characterized by a photocurrent rise and decay time constants of $\tau_{\text{rise}} = 0.7$ seconds and $\tau_{\text{decay}} = 1.5$ seconds, respectively. The photocurrent decay in the photodetector follows the relationship [56]:

$$I(t) = I_o \exp\left(\frac{-t}{\tau_{\text{decay}}}\right) \quad (3-16)$$

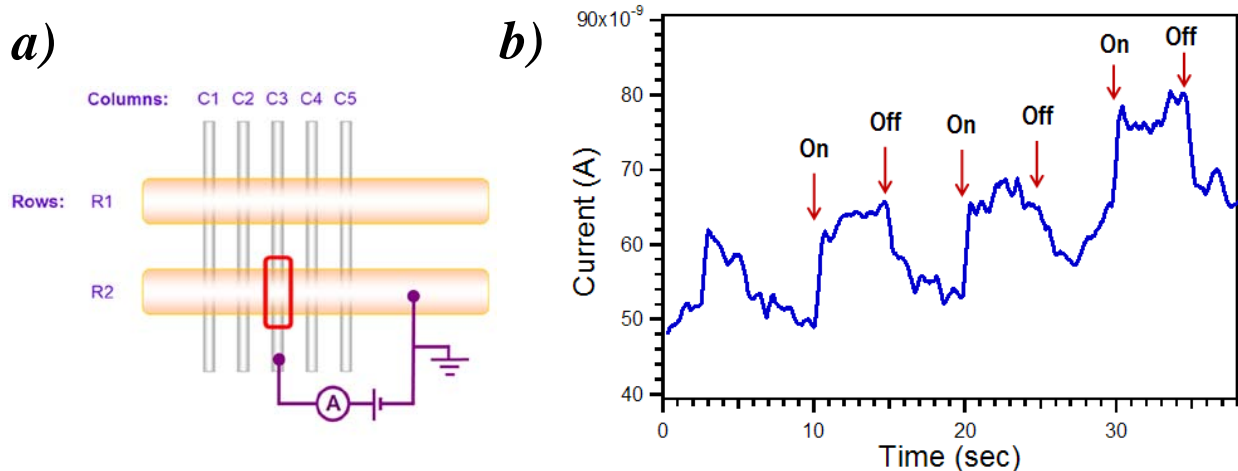


Figure 3-42. a) Schematic illustration showing interrogated Node R2C3 and b) plot showing the time response behavior of the photodetector.

where I_0 is the photocurrent before terminating the UV illumination. The photocurrent rise time constant is dominated by the charge carrier transit time while the slower decay time constant is dominated by the recombination of photogenerated electrons and holes.

An estimate of the responsivity of the photodetector is calculated by assuming that 1% of the 5 mW laser output power is transmitted through the 200 nm-thick metal top electrodes. From the time response data, the photocurrent is calculated to be approximately 14 nA by subtracting the dark current (~48 nA) from the measured UV illuminated current (~62 nA). These results yield a relatively low responsivity value of 3×10^{-4} A/W, as compared to the 1.31×10^{-1} A/W responsivity value (at 325 nm) of a commercially-available UV photodetector (Hamamatsu, Model 818-UV) [57]. Future iterations of the device could increase its responsivity by minimizing the thickness of the top electrode to allow more incident light to be transmitted to the ZnO nanowires. The internal efficiency of the device could also be increased by improving the crystal quality of the synthesized ZnO nanowires.

From the time response data, the total photocurrent of the ZnO nanowire node in response to the UV laser and the dark current are approximately 62 nA and 48 nA, respectively. Therefore, the signal-to-noise ratio of the 2D ZnO nanowire array at an operating voltage of 1 V and a laser input power of 50 μ W is calculated to be approximately 1.3. This ratio again is low and could be optimized by future iterations of the device. The spectral response of this device is inherent to the ZnO material itself ($E_g = 3.37$ eV), so wavelengths shorter than 367 nm are detectable. The flexibility of 2D array architecture allows the customization of the nanowire material so that the photodetector could measure other wavelengths of light in the electromagnetic spectrum.

Although the performance parameters for the fabricated 2x5 ZnO nanowire array were under par, the objective of this research was not to fabricate a high performance photodetector. Instead, the goal was to fabricate a 2D individually-addressable nanostructure array platform, which was successfully achieved. To the best of the author's knowledge, this marks the first successful demonstration of vertically integrating ZnO nanowires into an individually-addressable 2D array. The platform marks the first step towards many potential, high-impact

applications, such as high-resolution maskless lithography, nanoscaled-resolution image sensors, and integrated nanosystems of light-emitting diodes, lasers, and photodetectors.

3.6 Summary

This chapter detailed the successful fabrication of a 2D individually-addressable zinc-oxide nanowire-based photodetector. The carbon nanotubes of the previous chapter were replaced by ZnO, a semiconducting material, in order to resolve the problem of individual node addressability. The use of ZnO enabled a design platform consisting of Schottky electrical contacts between the platinum bottom electrodes and the n-type ZnO nanowires, as well as ohmic electrical contacts from the nanowires to the Ti/Au top electrodes. The rectifying nature of the Schottky contacts allowed the electric current to flow only in one direction through each node. This restriction surmounted the problems associated with the multiple electrical pathways throughout the 2D array.

Several fabrication architectures were pursued and a successful protocol was finally established. The final device was created using platinum as the material for creating Schottky MS contacts and titanium as the material for creating ohmic contacts. Platinum, as the bottom electrode material, enabled the patterned growth of the ZnO nanowires through the VLS process. A vertical growth orientation, Schottky MS junction formations, and structural and electrical integrity after the high temperature synthesis process were all achieved by using the platinum material. The optical quality of the ZnO nanowires grown on platinum electrodes was high as indicated by the large dominating band-edge peak at 385 nm in the photoluminescence spectra.

The completed device was a 2x5 ZnO nanowire array that exhibited rectifying current-voltage behaviors in four of the ten nodes. The remaining six nodes were shorted due to pinholes in the SOG layer that led to metal interconnections between the top and bottom electrodes. Photodetection characterizations were performed on the four working nodes using an integrated probe station and UV laser setup. The beam of a 325 nm HeCd laser, focused to a spot size of 40 μm in diameter, was able to excite the ZnO nanowires within a single node. When the interrogated node was excited with the laser, increased current in both forward and reverse-biased voltages was clearly observed. Furthermore, when the laser spot was moved to illuminate other neighboring nodes while electrically interrogating the original node, there was no observed photocurrent contribution to the interrogated node. This demonstrates the individual-addressability of the 2D ZnO nanowire array and its ability for discrete pattern recognition as a pixilated UV photodetector.

CHAPTER 4 – CONCLUSIONS

4.3 Dissertation Summary

The research presented in this dissertation addresses the issue of assembly and integration of one-dimensional nanoscale building blocks into functional devices and nanosystems. A two-dimensional, individually-addressable device architecture has been proposed by directly integrating vertically-oriented 1D nanostructures into the array platform. This 2D architecture has been realized with standard semiconductor and microelectromechanical systems (MEMS) processes, as well as the VLS catalyst-assisted 1D nanostructure synthesis method. The vertical orientation of the 1D nanostructures in the 2D array extends the device geometry beyond traditional planar device architectures into the third dimension, creating the possibility for ultrahigh-density design applications in nanoelectronic memory, information displays, nanolithography, and photodetectors.

In order to demonstrate the feasibility of integrating vertical, free-standing, one-dimensional nanostructures into a 2D array, a proof-of-concept 2D array has been fabricated using multi-walled carbon nanotubes. Although many issues were encountered throughout the fabrication processes of the first CNT array, the obstacles were surmounted and an optimized 15x12 array was successfully fabricated. The current-voltage characteristics of each electrically-isolated node in the CNT array exhibited the expected linear behavior for metallic carbon nanotubes. The average calculated resistance value across the CNT forest structures with an area of $500 \times 400 \mu\text{m}^2$ that connect the top electrodes to the bottom electrodes was approximately 54 Ω .

A single, 1 μm -long carbon nanotube with a diameter of 30 nm was attached to two nanoprobe tips inside a scanning electron microscope and its current-voltage characteristics were measured. The resistance and resistivity of this carbon nanotube were calculated to be 79.2 M Ω and 0.056 $\Omega\cdot\text{m}$, respectively. A carbon nanotube measuring 17 μm in length and 30 nm in diameter was interpolated to have a resistance value of 1.4 G Ω . After analyzing the density of the as-synthesized CNT bundles and estimating that there are approximately $22 \times 10^6 \sim 33 \times 10^6$ carbon nanotubes connecting the top electrode to the bottom electrode at each $500 \mu\text{m} \times 400 \mu\text{m}$ node, the overall resistance value of the CNT nodes in the 2D array was calculated to be approximately 41~61.4 Ω . This result correlates well with the measured average resistance value of 54 Ω from the 84 electrically-isolated nodes in the 15x12 array, signifying that there are successful electrical connections between the top and bottom electrodes through the CNT bundles in between.

Because the metallic carbon nanotube nodes in the device served as electrical interconnects between the top and bottom electrodes, individual-addressability of the 2D array was not demonstrated in the CNT device. The solution presented in the dissertation was to replace the metallic CNT structures with semiconducting zinc-oxide (ZnO) nanowires and create rectifying, Schottky diodes at the 2D array nodes. The rectifying nature of the nodes would allow the electric current to travel in one direction only, thereby eliminating the multi-path problem associated with the CNT device.

A completed 2x5 ZnO nanowire array features platinum bottom electrodes forming Schottky metal-semiconductor junctions with the n-type ZnO nanowires and titanium/gold top electrodes forming ohmic junctions with the nanowires. Current-voltage measurements across each node in the 2D array revealed that four of the ten nodes exhibited rectifying, Schottky

electrical behavior. The other six nodes exhibited electrical shorting behavior with resistance values on the order of $\sim 100 \Omega$.

The rectifying nodes were tested for their photodetection and individual-addressability characteristics. After recording the I-V characteristics of a node under dark conditions, the forward and reverse current through the node increased noticeably once a UV laser was directed onto the node, confirming that photogenerated current is detectable from the ZnO nanowire array. The laser beam was subsequently moved to a neighboring node $300 \mu\text{m}$ away and the current-voltage characteristics of the original node were measured again. The photogenerated current in the neighboring nodes did not contribute to the current measured in the interrogated node, which was similar to that of dark conditions.

The transient photocurrent response of the ZnO nanowire array was analyzed by applying a constant bias of 1 volt across a rectifying node. The measured time response was characterized by a photocurrent rise time constant of $\tau_{\text{rise}} = 0.7$ seconds that is limited by the transport of photogenerated charge carriers. A slower photocurrent decay time constant that is dominated by the recombination of photogenerated electrons and holes was calculated to be $\tau_{\text{decay}} = 1.5$ seconds. The responsivity of the 2D array was estimated to be 3×10^{-4} A/W, a relatively low value compared to 1.31×10^{-1} A/W for a commercially-available UV photodetector. This low responsivity is likely attributed to two major reasons. First, the relatively thick top metal deposition used in the current work could block a significant amount of UV light. Second, only a small fraction of the nanowires in each of the $150 \times 500 \mu\text{m}^2$ node are illuminated by the UV laser to contribute to the sensing results. The signal-to-noise ratio of the device is approximately 1.3 at an operating voltage of 1 V and with a laser input power of $50 \mu\text{W}$. Although the performance of the fabricated 2×5 array is far from ideal, several optimization measures could improve the device in future iterations and are presented in the following section.

4.4 Future Directions

An evident problem associated with the fabricated ZnO nanowire array is the yield in the number of rectifying Schottky nodes. Of the ten possible nodes in the 2×5 array, four nodes exhibited rectifying electrical characteristics while the other six nodes exhibited shorting behaviors. A poor SOG filling around the nanowires in these nodes contributed to the formation of pinholes that allowed direct electrical connections between the top and bottom electrodes during the top metal evaporation process. This problem could be solved by drop-casting the SOG solution from all directions onto the device substrate (instead of introducing it from one side only) so that a uniform filling around the nanowires could be achieved. The SOG solution could then be left on the substrate to settle for a few minutes before spinning it to the final film thickness. These crucial steps would ensure a more conformal, defect-free dielectric separation between the top and bottom electrodes and increase the number successful rectifying metal-semiconductor connections in the 2D array.

The responsivity of the 2D ZnO nanowire photodetector could be optimized by improving the crystalline quality of the synthesized nanowires. From the photoluminescence spectra of the ZnO nanowires, there are two relatively small defect peaks centered at 520 nm and 580 nm. The deep level traps associated with these peaks absorb some of the incident photons and serve as recombination sites for the photogenerated carriers which decrease the photocurrent/responsivity of the photodetector. These defects could be reduced by adopting

other nanowire synthesis techniques, such as metal-organic chemical vapor deposition (MOCVD) using diethyl-zinc and oxygen as the growth precursors. The ZnO nanowires synthesized from this process have been shown to have very high crystalline quality (Figure 4-1a) and no defect peaks in its PL spectra (Figure 4-1b), as compared to ZnO nanowires grown via the VLS process by the thermal evaporation of ZnO powder [58]. The MOCVD synthesis of ZnO nanowires (carried out at 605°C) is a lower temperature process compared to the VLS growth process at 925°C used in this research, and could lower the overall thermal budget of the device manufacturing process. The ZnO nanowire surface defects associated with oxygen vacancies could also be passivated by a SiO₂/Si₃N₄ bilayer coating directly after the synthesis process to reduce the scattering and trapping of charge carriers by the surface states [59].

Other engineering solutions to improve the performance of the 2D ZnO nanowire photodetector include decreasing the top electrode metal thickness to allow more incident light to be transmitted to the ZnO nanowires, as well as decreasing the nanowire length to promote the efficient collection of the photogenerated charge carriers before recombination. Because only a small fraction of nanowires in each of the 150 μm x 500 μm node in the 2D array were photo-excited by the 40 μm-wide UV laser beam, the signal-to-noise-ratio (SNR) of the device could be improved by increasing the laser spot size to encompass the entire nodal area or by decreasing the dimensions of the nodes. Nano-imprint or laser interference lithography could be utilized to decrease the width of the bottom and top electrodes to several hundred nanometers (Figure 4-2). This would lead to a 2D array with submicron-sized nodes with a high SNR performance. Because the nano-imprint and laser interference patterning techniques are capable of producing periodic structures across the entire 4” substrate in a single exposure, the manufacture of ultra high-resolution photonic devices using the 2D nanowire device platform would be economical and practical [60, 61].

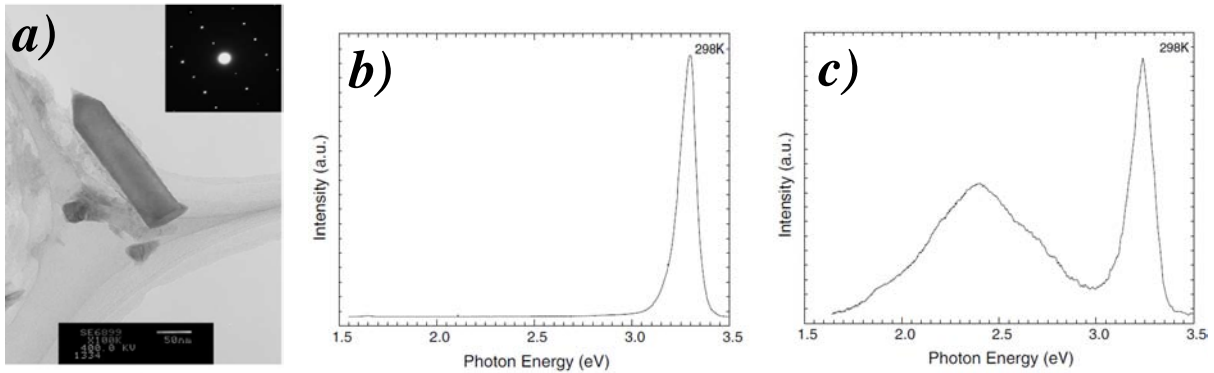


Figure 4-1. *a)* TEM image and selected-area electron diffraction pattern (inset) of ZnO nanowires synthesized by MOCVD, and PL spectra of ZnO nanowires *b)* synthesized via MOCVD, showing no defect peaks *c)* synthesized via the VLS process by thermal evaporation of ZnO powder, showing a large defect peak [58].

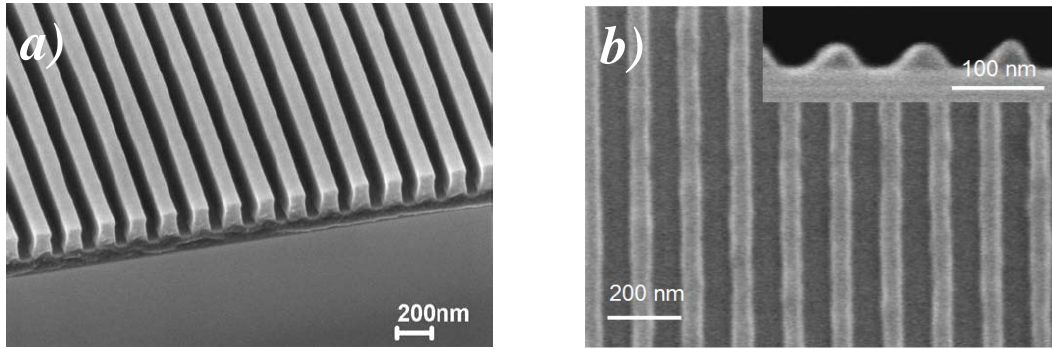


Figure 4-2. SEM images of *a)* nano-imprinted resist pattern of 100 nm-wide lines in 200 nm pitch [60] and *b)* resist patterns of 36 nm-wide lines in 96 nm pitch from 157 nm interference lithography [61].

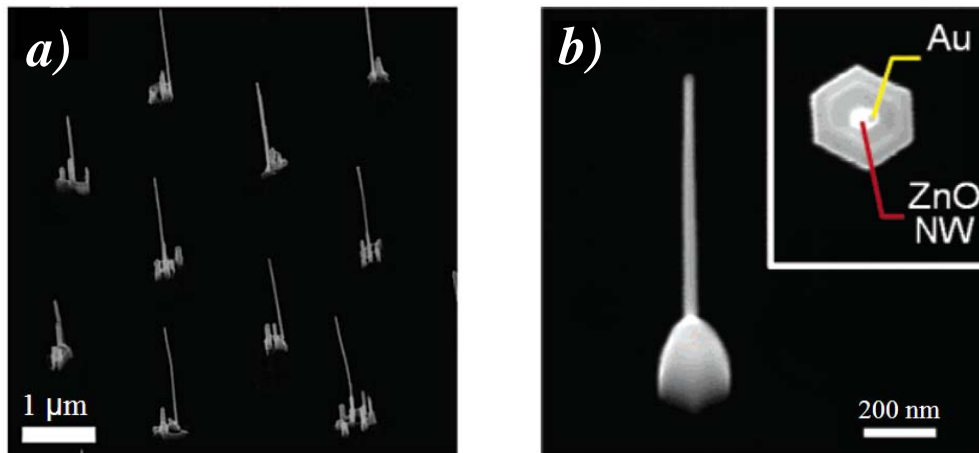


Figure 4-3. SEM images of *a)* an array of individual ZnO nanowires growing from each catalyst spot, *b)* a vertical ZnO nanowire projecting from a dome-like ZnO buffer layer (inset shows the hexagonal shape of the dome) [62].

It is also possible to synthesize a single ZnO nanowire, via the VLS process by the thermal evaporation of ZnO powder (Figure 4-3), from a gold catalyst particle measuring 200 nm in diameter and 2 nm in thickness (patterned by electron-beam lithography) to form the active elements in the 2D array, which could lead to a photodetector with resolution capability in the tera-level range [62]. The growth of single ZnO nanowires from prescribed locations, however, has not been demonstrated by the VLS nanowire synthesis process used in the research presented in this dissertation. The ZnO nanowire growth conditions and procedure, therefore, would still need to be optimized in the future to produce high-quality nanostructures with resolute optical and electrical characteristics, size and dimensionality uniformity, and dopant distribution. These material properties could dictate the functionality of the nanostructures and nanosystems.

Reproducible nanostructural interfaces between metal-semiconductor and semiconductor-semiconductor still need to be explored by the careful engineering and examination of the chemistry and physics occurring at the interface, as well as their influence on device performance and operation. Different metal materials could be investigated to determine the one

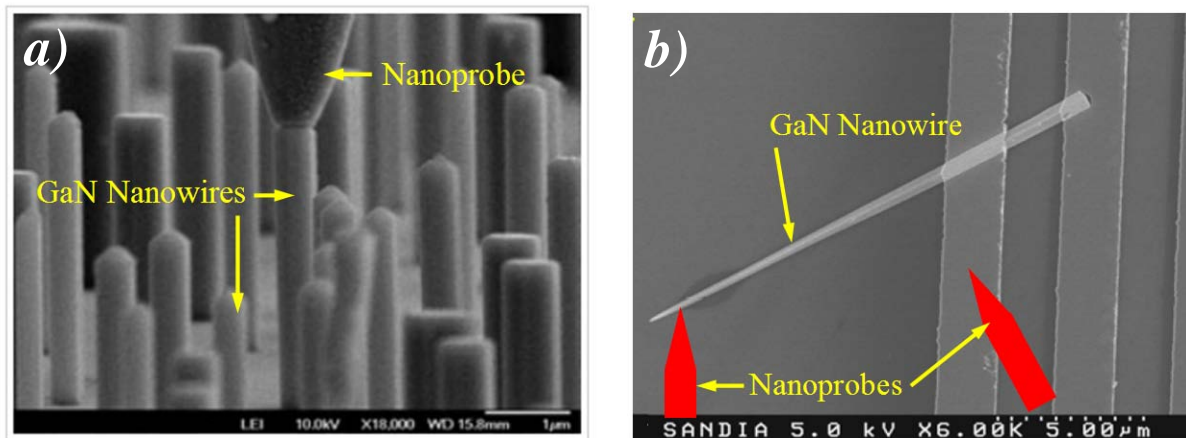


Figure 4-4. SEM images of a) a nanoprobe in contact with a GaN nanowire to characterize the bottom electrode/nanowire contact and b) nanoprobes contacting a nanowire tip and top electrode to characterize the top electrode/nanowire contact [63].

that yields the least resistive ohmic contact between the top electrode and the n-type ZnO nanowires. The bottom electrode metal could also be changed to a material that produces a near-ideal rectifying, Schottky contact with the ZnO nanowire with a small turn-on voltage. These contact formation characterization studies would entail synthesizing the ZnO nanowires on different bottom electrode materials and measuring the resulting electrical transport characteristics of the MS junction with one Kleindiek nanoprobe contacting the bottom electrode and the other contacting the tip of the nanowire (Figure 4-4a) [63]. Top electrode contact formation studies would be carried out by depositing the nanowire on an insulating substrate, evaporating a metal onto one end of the nanowire to make a planar side contact, and contacting the nanoprobes to the tip of the nanowire and the metal electrode (Figure 4-4b).

Additional functionality could be designed into the 2D nanostructure array if the Schottky junctions in the device were changed to *pn* junctions. This could be accomplished by replacing the metal bottom electrode by a highly-doped, p-type silicon device layer on top of the buried oxide layer in a silicon-on-insulator (SOI) substrate. This p-Si/n-ZnO heterojunction (Figure 4-5a) has been successfully fabricated with ZnO nanorods to form a light-emitting diode (Figure 4-5b) whose electroluminescence spectrum shows a narrow ultraviolet peak at 387 nm and a broad green band at 535 nm (Figure 4-5c). Because the crystal lattice mismatch between silicon and ZnO is approximately 40%, there are many interfacial defect states at the p-Si/n-ZnO heterojunction acting as recombination sites that decrease the device efficiency [64]. Another p-type material such as Mg-doped gallium-nitride (GaN) thin film could be used to form the *pn* junction with n-ZnO nanorods since the lattice mismatch between the two materials is approximately 1.9% in the a-plane [65]. The schematic diagram of such a p-GaN/n-ZnO light-emitting diode is shown in Figure 4-6a while an optical image of the blue light emission and its electroluminescence spectrum are shown in Figures 4-6b and 4-6c, respectively [66]. The light-emitting diodes could then be co-located with photodetecting nodes on the same 2D array and function as optical circuit elements in a highly complex nanosystem.

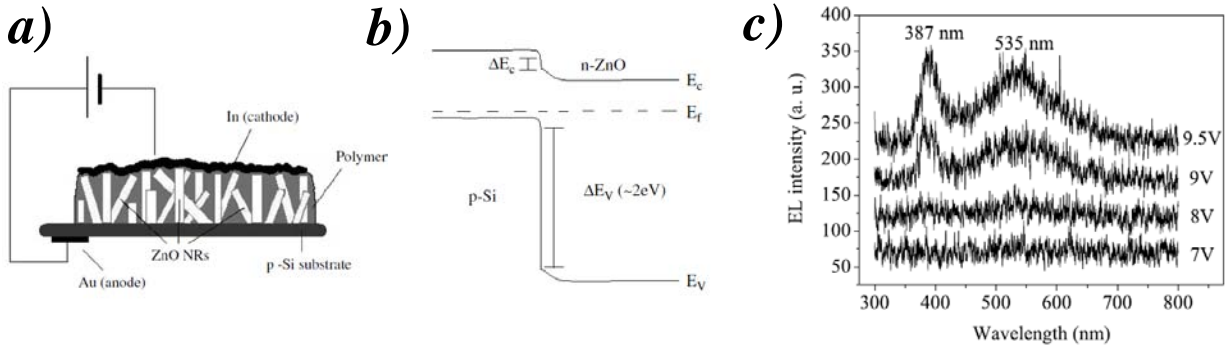


Figure 4-5. Light-emitting diode fabricated with the n-ZnO nanorods/p-Si heterojunction. *a)* Schematic diagram of the device, *b)* expected energy band diagram of n-ZnO/p-Si heterojunction, *c)* electroluminescence spectra of the light emitting diode [64].

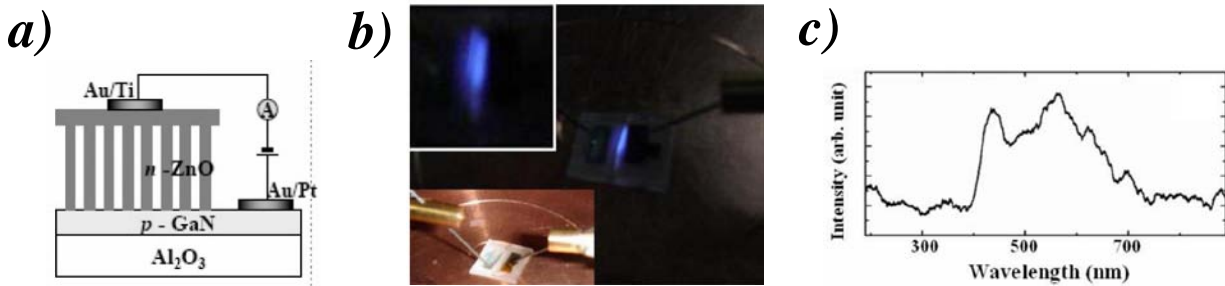


Figure 4-6. Light-emitting diode fabricated with the n-ZnO nanorods/p-GaN heterojunction. *a)* Schematic diagram of the device, *b)* optical image of the blue light emission, *c)* electroluminescence spectrum of the light emitting diode [66].

Another device functionality such as piezo-electric nanogenerators based on ZnO nanowires could be incorporated into the 2D array possibly to power the light-emitting diodes in the nanosystem. The coupling of piezo-electric and semiconducting properties of zinc-oxide has been demonstrated to create a strain field and charge separation due to the bending of ZnO nanowires, while the rectifying characteristics of the Schottky barrier between a metal AFM tip and the nanowire lead to electric current generation (Figure 4-7) [37]. The output power density of the nanogenerator has been estimated to be as high as $10 \text{ pW}/\mu\text{m}^2$ for a nanowire density of $20/\mu\text{m}^2$ on the device substrate. If the nanowire array size were $10 \mu\text{m} \times 10 \mu\text{m}$, the amount of power generated could sustain a single-nanostructure device [37].

The goal of the research presented in this dissertation was to address the issue of assembly and integration of one-dimensional nanostructures into functional devices and nanosystems. Utilizing a two-dimensional nanostructure array architecture and the direct, vertical integration of 1D ZnO nanowires into the device platform, UV photodetection and individual-addressability have been demonstrated by the fabricated 2×5 ZnO nanowire array. The successful demonstration of the proposed 2D nanostructure array architecture marks the first step towards the future realization of potential high-impact applications in various fields.

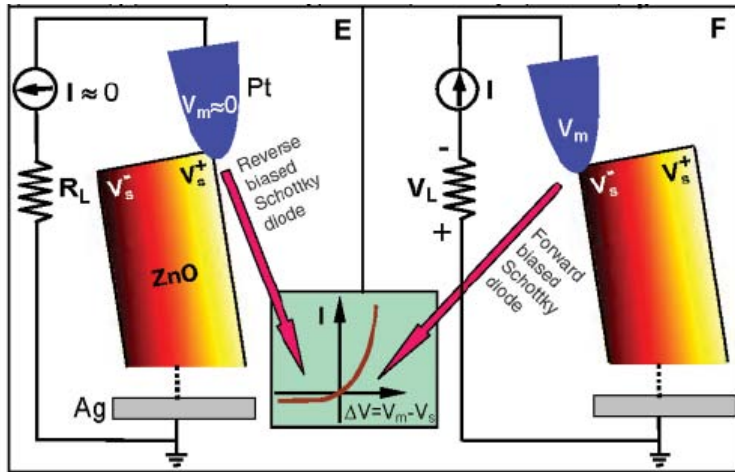


Figure 4-7. Piezo-electric nanogenerators based on ZnO nanowires and an AFM tip [37].

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