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Dynamic and Power Performance of Multiple State Electrostatically Formed Nanowire Transistors

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Abstract—Electrostatically formed nanowire (EFN)-based transistors have recently been proposed as a single device with multiplexer functionality. In these transistors, the conduction path between source and one of the drains is determined by the bias applied to the two junction-side gates. By applying a nonsymmetric bias on the side gates, the lateral position of the EFN is controlled. We present a detailed analysis of the different states of the multiple state electrostatically formed nanowire transistor device, the transient time between them and the power exerted during each transition. The dependence of transition time between states and leakage currents in cutoff states on different geometry parameters is also presented.

Index Terms—FETs, logic devices, nanowires, transient.

I. INTRODUCTION

MULTIPLE state electrostatically formed nanowire transistors (MSETs) have been recently suggested as multiple state multiplexer such as transistors [1]. These transistors are based on the G-4 FET where two junction-side gates determine the width of the source–drain conduction channel and with it the threshold of the top and back gates [2]–[5]. When a negative bias is applied to the side junction gates, the region around them becomes depleted from charge carriers confining the conduction path between the source and the drain to a thin channel, the electrostatically formed nanowire (EFN). When the bias on the side gates is asymmetric, the depletion region around one gate is larger than the other and the conduction path lateral position is controlled [6]–[8]. By splitting the drain in to several isolated drains, the MSETs exploit this lateral movement in order to form a multiple state, single transistor multiplexer. For example, in the case of two drains MSET, a well-defined conduction path between a single drain and the source can be formed by depleting the region between the other drain and gate close to it. In a similar manner, if the regions adjacent to both drains are depleted, there is

Fig. 1. Test circuit with a resistor and a two drains MSET. The biases applied to the gates create a conduction channel between the source and second drain contacts. The arrows mark the direction of positive current flowing through each of the terminals according to standard convention.

no conduction at all between the drains and the source. When both gates are not biased there is conduction between both drains and the state is undefined.

Fig. 1 shows an illustration of a two drains MSET, where the two drains, d_1 and d_2 , are connected to a specific voltages, V_{d1} and V_{d2} . In this example, the source is connected to a pull down resistor. Hence, the voltage divider between conduction channel and the pull down resistor R_C defines the output voltage. Previous work has shown that for some drain voltages and geometries, the output voltage of such a circuit can be very close to the drain voltages yielding the multiplexer functionality. However, the device switching frequency and power consumption were not addressed. In this paper, we analyze the dynamic performance and power consumption of a two drains MSET. It is shown that the switching frequency of a circuit similar to the one in **Fig. 1** can reach 10 GHz. The static and transient power consumptions are simulated as a function of key device parameters. A clear tradeoff between switching speed and power consumption implies that the optimal MSET structure will be determined by the application.

II. PERFORMANCE CHARACTERISTICS

The transition times between the different states and power consumption during operation are two main figures of merit

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of transistors operation. In principle, the MSET relies on the formation of depletion regions of p-n junctions in a similar manner to the junction FETs (JFETs).

The transition time is the time required for the circuit in order to change its output and reach steady state. In a circuit as in Fig. 1, the output voltage is the source voltage. In this case, outputs V_i and V_j with a voltage difference $\Delta V = |V_j - V_i|$ correspond to states i and j , respectively. We denote by t_0 the starting time for the transition and by t_r the time when the voltage of the source reaches 90% of ΔV . We also denote by t_s the time by which the source voltage reaches a range of 5% difference from the final voltage V_j . The transition rise time T_r is defined by $T_r = t_r - t_0$ and the transition settling time T_s is defined by $T_s = t_s - t_0$.

In modern transistors, with low threshold voltages and thin gate oxides, leakage can account for as much as a third of total active power [9]. The static power is dominated by the subthreshold leakage current which is the current flow when a transistor is in an OFF state.

We define the static power P_s to be the power dissipated within the device in steady state

$$P_s = \sum IV = I_{d1}V_{d1} + I_{d2}V_{d2} + I_{g1}V_{g1} + I_{g2}V_{g2} + I_sV_s. \quad (1)$$

This parameter is important for logic design, because it provides an estimate for the power dissipated by the device.

The transient power is the power dissipated by the device while switching from one state to another. The transition consists of charging and discharging of the junctions and diffusion capacitance of the device as well as passing current through the EFN. The power consumed during this operation is given by

$$P_d = \frac{1}{T_s} \int_{t_0}^{t_s} I(t)V(t)dt \quad (2)$$

where the integral is calculated across the transition and T_s is the total transition time.

III. SIMULATION SETUP

The following simulations were all performed using *Sentaurus* TCAD. The simulated MSET is a two gates, two drains MSET as shown in Fig. 12. The specific geometry is given in Appendix A. All the simulations in this paper are 2-D in the sense that gradients along the thickness of the device are not considered. The thickness of the silicon-on-insulator is 1 μm .

The simulated circuit consists of a single MSET as above with a pull down resistor to the ground. The drains are connected to ideal voltage sources $V_{d,1}$ and $V_{d,2}$. The gates are also connected to ideal voltage sources which determine the EFN position and the conduction state. An illustration of the simulated circuit is shown in Fig. 1.

We define four conduction states for the MSET; in state 0, there is no bias on the side gates and both drains are passing current. Since we are interested in CMOS like operation where only leakage current flows in steady state, we consider this state to be invalid. In state 1, there is bias on gate 2 such that

TABLE I
CIRCUIT STATES

State	$V_{g,1}$	$V_{g,2}$	V_{out}
0	0	0	-
1	0	V_b	V_1
2	V_b	0	V_2
3	V_b	V_b	0

there in conduction only through drain 1. In state 2, gate 1 is biased such that there is conduction only through drain 2. In state 3, there both gates are biased such that both drains are isolated and $V_s = 0V$. The different states are summarized in Table I. The bias applied to the gates in order to reach the different states is denoted by V_b .

We would like to determine the resistance R_C for a proper device operation. This resistance has a great effect on the transition time, because it acts as a pull down for the source contact. A low R_C value will cause a significant drop in the source voltage while switching between states 1 and 2. As a result, low R_C values restrict the maximum switching frequencies. On the other hand, high resistivity causes a longer transition time to state 3 as the current to the ground is low. Furthermore, A low R_C value reduces significantly the transition time to state 3. However, since the voltage on the source contact for states 1 and 2 is a voltage division between the appropriate drain voltage and the ground, a low R_C value will reduce the output voltage. In order to balance between these conflicting demands for the magnitude of R_C , we chose it to have a value of around the resistance of the channel. A resistor with such resistance causes the voltage on the source contact to reach half the magnitude of the drains voltages and also pulls down the source voltage in about the same time as a transition between states 1 and 2.

The choice of R_C as the resistance of the channel is also problematic. Static simulation of the MSET device reveals a strong dependence between the voltages of the drains and the channel resistance, this dependence is explored in Appendix B along with the device geometry parameters. The calculations show that for a fixed R_C and different drain voltages, the source contact may reach half the magnitude of one of the drains, but not necessarily the other. That is because the conduction channel between the each of the drains and the source has a different resistance.

In order to have a unified and simple test circuit, the voltage $V_{d,1}$ is set to 0 V and $V_{d,2}$ to 0.25 V. This choice enables setting $R_C = 12.5 \text{ K}\Omega$, which is the channel resistance corresponding to a drain voltage $V_{d,2}$, and thus have the source voltage at half the drain voltages at states 1 and 2. The biases to the gates were chosen 0 or -2 V to allow conductance from just one drain. These values were used in all the following simulations unless stated otherwise.

IV. TRANSIENT RESPONSE

Fig. 2 shows the snapshots of the current density in the transition from state 1, conduction from drain 1, to state 2, conduction from drain 2. Fig. 3 shows the source voltage as

Fig. 2. Electron current density snapshots at the transition from state 1 to state 2. The snapshots are of a zoomed-in view on the active region of the device. After 5.1 ps, the channel is positioned next to drain 2.

Fig. 3. Source voltage and drain currents during transition from state 1 to state 2.

a function of time for the same transition as well as current through the two drains. At state 2, the channel conducts only from drain 2 and the source voltage is exactly half of V_{d2} . The currents through the two drains have opposite signs throughout this transition; the region next to drain 2 is depleted of electrons, causing them to pass into the drain 2 contact. After the initial burst of electrons at about 1 ps, the current decreases rapidly until at about 4 ps it changes sign and becomes positive (the channel reaches its final position at 5 ps as shown in Fig. 2). This positive current is the steady-state source to drain current of state 2. On the other hand, the region next to drain 1 has a large electron population in its initial state which is removed (a positive current) when the channel is replaced until reaching its steady-state leakage current.

The currents have a peak value shortly after the rapid change of the gates bias which is caused by the rapid movement of the depletion regions. The currents drop to their steady state quickly while the source is charged through the new channel. As the EFN shifts from drain 1, the source voltage drops below the two drain voltages. This very fast voltage drop is caused by electron flow through the source contact; these electrons also originate from the fast shift of the depletion regions and the charge and discharge of junction capacitance.

As can be seen in Fig. 2 the lateral movement of the EFN reaches its final position next to drain 2 after 5 ps. After the channel reached the appropriate position, the source must be charged by injecting electrons toward the drains in order for it to reach its steady-state voltage.

TABLE II
RISE AND SETTLING TIMES FOR STATE TRANSITIONS

Transition	Rise time	Settling time
1 to 2	13.7ps	16.6ps
2 to 1	11.4ps	13.7ps
2 to 3	0.12ps	44ps
3 to 2	0.14ps	25.4ps

Fig. 4. Source voltage response to several state transitions.

The transient response was calculated for the transitions between all the states is listed in Table I. The rise and settling times for the different transitions are given in Table II and Fig. 4. The transitions between states 1 and 2 are significantly faster than transitions to or from state 3. In the first case, the channel moves from the first drain to the second or vice versa while most of the depletion regions are unchanged. Transitions to or from state 3 consist of the formation or removal of the entire channel and this process requires relatively large variations of the depletion regions. On the other hand, the rise time related to state 3 is significantly faster because of the overshoots seen in Fig. 4. In a transition between states 1 and 2, the depletion regions charging currents through the source contact are of opposite directions and, thus, cancel out. For transitions involving state 3; however, the currents are unidirectional and so cause a voltage drop on the source.

The results show that the transition from state 2 to state 3 is significantly slower than the reverse transition. This phenomenon is caused by the overshoot of the source voltage. For the transition from state 3 to state 2, the channel is formed after around 5 ps and the source voltage is brought down from about 0.7 V through both the source and drain 2 contacts. For the 2 to 3 transition, after about 5 ps, the channel is removed and the source voltage is about -0.6 V. This voltage is charged to 0 through the source contact only and thus this process is slower.

The transition time between the different states is strongly affected by the geometry of the device. Fig. 5 shows the effect of the device length L on the settling time of the transition from state 2 to state 3. The length of the oxide buffer is $L/3$. The length of the device has a nearly linear effect on

Fig. 5. Transition settling time between states 2 and 3 for different device lengths. The length of the oxide buffer is $L/3$.

Fig. 7. Static power consumption in state 3 versus the length of the MSET. The length of the oxide buffer is $L/3$.

Fig. 6. Transition settling time between states 2 and 3 as a function of the device bulk doping concentration.

Fig. 8. Static power in state 3 versus the bulk doping of the MSET.

the settling time. As expected, increasing the device length increases the free-carrier charge in the channel and, therefore, gives rise to a slower turn OFF speed [10].

Fig. 6 shows the transition settling time between states 2 and 3 as a function of the device bulk doping concentration, N . The doping of the bulk has a more complex effect on the transition time as it changes both the resistance of the channel, its area and the amount of charge carriers that have to change their position during the transition. The resistance of the channel decreases with the increase of the doping, reducing the charging time of the source contact. On the other hand, increasing the doping concentration also increases the capacitance of the depletion regions, and so the channel itself takes longer to form or change position. The settling time monotonic decrease with the bulk doping concentration indicates that the reduction in the channel resistance and the increase in its cross section area have the most significant effect.

V. STATIC POWER

The static power consumption of the device is an important figure of merit of state 3. In this state, the channel should be

closed and the device should ideally function as a resistor with an infinite resistance. In practice, the resistance is not infinite and there is a leakage current which causes power dissipation. This power consumption can be estimated using (1). In order to examine the effects of the geometry parameters, the static power consumption was calculated for the MSET device only.

The static power is strongly affected by the geometry of the device. The effect of the bulk doping N and the length of the device L on the static power in state 3 are shown in Figs. 7 and 8, respectively.

As shown in Fig. 7, the length of the device has an exponential effect on the static power exerted by the device. Fig. 9 shows the current density distribution at state 3 for $L = 0.9 \mu m$ (left) and $L = 0.55 \mu m$ (right). The leakage current between the source and drain 2 is more significant than the leakage between the two drains and is higher for shorter devices. The oxide buffer has two roles in the device geometry; the first is to separate the two drains and prevent current flow between them, the other is to cause a channel cutoff for biases that would otherwise give rise to a conductive channel from source to drain. As L decreases, the buffer provides inferior separation; the drain-to-drain and source-to-drain currents increase by orders of magnitude. The ratio between

Fig. 9. Current density distribution at state 3 for L_D $0.9 \mu\text{m}$ (left) and L_D $0.55 \mu\text{m}$ (right).

Fig. 10. Current density distribution at state 3 for N_D $1.33 \times 10^{17} \text{cm}^{-3}$ (right) and N_D $9 \times 10^{16} \text{cm}^{-3}$ (left).

the voltages used in the device and the properties of the buffer has a very significant impact on the cutoff currents and power. Further study on this phenomenon is required in order to minimize the static power consumption in this state.

The bulk doping of the device has an exponential effect on the static power exerted by the device. The main contributor to the static power is the current through drain 2. The current through the drain 2 contact changes from about 10^{-17}A at a bulk doping concentration of $9 \times 10^{16} \text{cm}^{-3}$ to about 10^{-10}A at a doping concentration of $1.3 \times 10^{17} \text{cm}^{-3}$ while the drain voltage is kept constant. As the bulk doping decreases, the depletion regions within the bulk increase. At about $9 \times 10^{16} \text{cm}^{-3}$, the bulk becomes completely depleted and further decrease of the doping does not have any effect. Fig. 10 shows the currents distribution at state 3 for $N = 1.33 \times 10^{17} \text{cm}^{-3}$ (right) and $N = 9 \times 10^{16} \text{cm}^{-3}$ (left). As can be seen in Fig. 10, the increase in N widens the conduction channel and gives rise to higher leakage between the two drains. The higher bulk doping concentration also increases tunneling current between the gates and the source. This leakage is negligible comparing with the other currents and can be removed by smoothing the corners in the gates doping profiles.

VI. TRANSIENT POWER CONSUMPTION

The transient power of the device was calculated for all the transitions according to (2) for the same voltages and geometry as described in Section III and Fig. 12, the results are presented in Table III. The circuit was set up to the starting state before each transition. Negative values in Table III are a result of

TABLE III
TRANSIENT POWER FOR STATE TRANSITIONS

Transition	Transient power
1 to 2	$32 \mu\text{W}$
2 to 1	$40 \mu\text{W}$
1 to 3	$44.4 \mu\text{W}$
3 to 1	$-9 \mu\text{W}$
2 to 3	$31 \mu\text{W}$
3 to 2	$-63 \mu\text{W}$

Fig. 11. Transient power consumption of the device terminals at the transition from state 1 to state 2.

discharge of capacitance charged during the set up phase. The dynamic power consumption of each contact for the transition between state 1 and state 2 can be seen in Fig. 11. The total power dissipation curve has two parts. In the first part, the dissipated power is negative and is mostly due to hole current flow through Gate 2 as the gate capacitance is charged when the voltage applied to it changes from -2 to 0V . The second part of the power dissipation curve is positive and is mostly affected by the holes going through Gate 1 while the voltage applied to it changes from 0 to -2V . The first part is faster because the voltage on Gate 2 quickly reaches about 0V and negative power drops to 0 . On the second part, the voltage on Gate 1 stays at -2V and so the power drops with the holes current. The different timing between the gates is not clear at first glance. A closer look shows that this timing is skewed by the different voltages of the two multiplying symmetric currents.

VII. DISCUSSION

In this paper, 2-D simulations were conducted in order to demonstrate the MSET transient performance and power dissipation. The 2-D simulation represents an ideal silicon-on-insulator (SOI) device. This implies that the doping profiles and oxide separators are perfectly vertical and effects such as substrate capacitance and space charge induced by trapped charges at the top and bottom surfaces are not considered. Since the device discussed in this paper inherits its basic operation from JFETs principles, the effects induced by these features would be quite similar. Including these effects requires

a full 3-D, transient simulations which are extremely computationally intensive and are left for future work. The input signals to the gates follow an exponential transient with a time constant that is significantly faster than the device transients, effectively yielding a step function. Such inputs, although unphysical, highlight the mechanisms that govern the device transients. Once the device is targeted to a specific application, its performance with respect to this specific input should be studied.

The MSET device provides interesting opportunities for digital and analog circuits. It can be used as a multistate transistor and also as a multiplexer. For the first usage, the MSET can be configured to act as a transistor with more than two states. An MSET with d drains has $d + 1$ valid states: one state for each drain that is connected to a unique voltage and one extra state for cutoff. In each of the drain states, the source contact is connected through a conduction channel to the appropriate drain and thus having a voltage level that is proportional to the drain appropriate voltage. By choosing a high enough pull down resistor, the source and drain voltages can be practically identical [1]. In the cutoff state, none of the drains are connected to the source so it can be driven by a complementary circuit. For the second usage, the MSET can be used as a multiplexer of signals. A traditional multiplexer requires more than a few transistors to implement. On the other hand, one MSET device can act as a multiplexer of d signals, where d is the number of drains. The conduction channel can be manipulated to connect each of the drains to source, thus multiplexing between them. The MSET can also function as an analog multiplexer to some extent.

The two drains MSET exhibits interesting temporal properties. For the geometry and voltages used, the switching frequency can reach around 20 GHz for the usage of all states and about 70 GHz for a multiplexer like operation (using only states 1 and 2). Optimization of the geometry of the device may allow considerable faster switching. Furthermore, it was shown that the geometry of the device has a strong effect on the timing of the device and so, further work is required in order to achieve an optimized design. Although the length of the device was shown to have a linear impact on the settling time of the longest transition, it has a direct reverse impact on the static power exerted by the device, and so there is a timing-power tradeoff that should be addressed according to the choice of application.

The dimensions used in this paper were of the magnitude of $1\ \mu\text{m}$. However, the current state-of-the-art fabrication node is of the magnitude of 10 nm. In order for the MSET technology to compete with such technology, it should shrink drastically. In theory, this would also allow for an improvement in timing and power dissipation over the current characteristics. This shrinkage proves difficult because moving the conduction channel is much more challenging as the dimensions become smaller. Nevertheless, recent advances in SOI-based, multiple terminal transistors may allow fabrication of nanoscale MSET devices [11]. In order to have a moving channel, the relation between the gates doping and the bulk doping should be such that on the one hand, small biases to a gate will have a noticeable effect on the depletion region of the bulk while

a 0 bias should diminish the depletion region as much as possible. We could not find doping concentrations that would produce a working device for $0.1\ \mu\text{m}$, so a significant change in geometry is needed.

One of the first requirements from the MSET as a logic device is concatenation [12]. This requirement dictates that the output of one device can drive the input of the next device. This is mandatory in order to produce sophisticated circuits that have some operational purpose.

The two drains MSET device that was initially suggested used an n-channel with gate voltages of 0 and $-2\ \text{V}$ while the drain voltages were of 0.5 and 0.75 V. These voltages are problematic in three aspects.

- 1) The gates and drain voltages are of an opposite sign. The gate voltages must be negative in order to create a depletion region and to move the channel while the drain voltages must be positive to prevent current from flowing between the gates and the drains (in the case of 0 bias on the gates). As a result, the source voltages are always nonnegative so it cannot drive a gate of the next level but only another drain.
- 2) The drain and gate voltages are of different magnitudes. The magnitude of the gate voltage required to move the channel as required is about twice the magnitude of the drains.
- 3) The source voltage is determined by different drain voltages. However, since the source should be later connected to a gate, the drains voltages must also be valid gate voltages.

In order to use the MSET as a logic device, these three issues must be addressed. The first issue can be resolved using alternating n-and p-type logic. This way, an n-type channel MSET uses positive drains and negative gate voltages, while the p-type channel uses negative drains and positive gate voltages. The logical circuit can then be constructed with the source of an n-channel MSET connected to one of the p-channel MSET's gates.

The second and third issues are more challenging. The difference in magnitude might be resolved using a different geometry; the geometry used in this paper can be changed in terms of widths, lengths, doping, and materials in order to achieve a geometry that uses voltages of similar magnitude but different signs for the gate and drains. The difference between the magnitudes of the drains is problematic because it is the enabler of the multilevel design. In order to have an MSET circuit that can support more than two levels of logic (not binary), more than one bias voltage value to the gate should be able to create a valid conduction channel. However, the width and position of the conduction channel depends greatly on the bias of the gates and so, a very specific geometry should be designed for the challenge.

In order to address the second issue without the third one, one gate and the opposite drain were grounded and the other gate voltage was set to $-V_d$. This voltage arrangement implicates a binary operation of the device, as the voltages allowed in the circuit (n-type and p-type alike) are 0 and $\pm V_d$ while the valid source voltages are only 0 and $V_d(-V_d)$ for n-type (p-type) device.

Several simulations were performed with the range of voltages between 0.5 and 3 V, while the parameters of L , L_B , W_B , and N_{d0} from Table IV were changed, the devices was of the form shown in Fig. 12. No geometry in which the voltages could be applied as described earlier could be achieved. The difficulty consists of two problems.

- 1) A low voltage could not manipulate the position of the channel enough to achieve a good differentiation between the different states.
- 2) At high voltages, there is a strong field between the drains. This field in turn causes a current between the two drains over the oxide.

VIII. CONCLUSION

This paper presented the MSET device and explored the timing and power specifications of a specific device geometry, along with the influence of different geometry parameters on them. The MSET was tested as a digital component that might be integrated with the CMOS technology.

The simulation results shows that the $0.48 \mu\text{m}^2$ device could reach a switching frequency in the order of magnitude of tens of gigahertz. The settling time of each transition consists of two parts. The first is the movement of the channel itself and the second is the charge or discharge of the source contact. The results show that the second part is responsible for the majority of the transition time between states, while the movement of the channel takes up about 20% of the total time.

The geometry parameters have a significant influence on the performance of the device; an increase to the length of the device gave rise to inferior switching time with a reduction of the static power. An increase to the doping of the bulk of the device improved timing performance at the expense of higher power excretion.

The MSET device was suggested as the logical equivalent of a multiplexer. The analysis showed that using the MSET device as a logical device is problematic for the unique voltages it requires and the difficulty of concatenation.

An interesting takeoff of the MSET device is to use the concept of nanowire creation in a FinFET. Although the dimensions does not fit the physics of the MSET device, replacing the doped gates with a metal and oxide could integrate the benefits of a nanoscale device with multiplexer-like operation of the MSET. This device would work using depletion rather than inversion principles and thus would still need both the positive and negative biases to operate.

APPENDIX A

The device bulk is n-type doped with a concentration of 10^{17} cm^{-3} , the gates are p-type doped with a concentration of 10^{19} cm^{-3} , and the source and drains are n-type doped with a concentration of 10^{19} cm^{-3} . Also shown in Fig. 12 are the main geometry parameters. All the device parameters along with their simulation values are listed in Table IV. According to standard conventions, positive current describes injection of holes from the contact into the device or injection of electrons from the device into the contact. Hence, in standard operation, the source current is negative and the drains current positive

Fig. 12. Schematic of the MSET device used in the *Sentaurus* simulations. The widths and lengths used for the simulations are listed in Table IV.

TABLE IV
TWO GATES, TWO DRAINS MSET SIMULATION PARAMETERS

Parameter	Symbol	Size
SOI width	W	600[nm]
SOI length	L	800[nm]
SOI thickness	T	1000[nm]
Drains length	L_D	40[nm]
Drains width	W_D	100[nm]
Source width	W_S	400[nm]
Source length	L_S	50[nm]
Gates first length	L_{G1}	325[nm]
Gates second length	L_{G2}	200[nm]
Gates first width	W_{G1}	100[nm]
Gates second width	W_{G2}	9[nm]
Oxide buffer length	L_B	270[nm]
Oxide buffer width	W_B	160[nm]
Bulk doping	$N_{d,0}$	$10^{17} [\text{cm}^{-3}]$, Arsenic
Drains doping	$N_{d,D}$	$10^{19} [\text{cm}^{-3}]$, Arsenic
Source doping	$N_{d,S}$	$10^{19} [\text{cm}^{-3}]$, Arsenic
Gates doping	$N_{a,G}$	$10^{19} [\text{cm}^{-3}]$, Boron

such that the power dissipation is proportional to the potential difference between the source and the drains.

APPENDIX B

The effect of the drain voltage on the channel resistance can be seen in Fig. 13. The trend is almost linear and is caused by the current limitation of the channel. The current working conditions are comparable to the linear domain of the JFET device.

In order to check the effect of different geometry parameters on the timing and power characteristics of the MSET device, the same circuit as in Fig. 1 was used. As discussed in Section III, the resistance of the channel depends heavily on the geometry of the device and the voltages used. For example, if the effect of the length L of the device is to be studied, the resistance R_C should be adjusted for

Fig. 13. Source to drain 2 channel resistance as a function of drain 2 voltage. Drain 1 voltage is 0 V and gate biases were -2 and 0 V.

Fig. 14. Source to drain 2 channel resistance versus the length of the device. The length of the oxide buffer is $L/3$.

Fig. 15. Source to drain 2 channel resistance as a function of the bulk doping concentration.

each L value so that the voltage on the source contact for state 2 will be half the voltage of drain 2.

The dependence of the channel resistance on the length of the device can be seen in Fig. 14. All the length parameters of the geometry of the device change proportionally with L

in order to keep the original ratios of the device. The channel resistance has a linear dependence on the length of the device, this phenomenon is expected as the length of the channel is directly influenced by L and was shown to have a linear effect on the resistance [13].

The dependence of the channel resistance on the doping of the bulk of the device can be seen in Fig. 15. The doping has a more complex effect on the resistance than the length [10] because it changes the mobility in the channel, its width and the built in potentials between the bulk and the gates.

REFERENCES

- [1] G. Segev, I. Amit, A. Godkin, A. Henning, and Y. Rosenwaks, "Multiple state electrostatically formed nanowire transistors," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 651–653, Jul. 2015.
- [2] K. Akarvardar, S. Cristoloveanu, M. Bawedin, P. Gentil, B. J. Blalock, and D. Flandre, "Thin film fully-depleted SOI four-gate transistors," *Solid-State Electron.*, vol. 51, no. 2, pp. 278–284, 2007.
- [3] K. Akarvardar, S. Cristoloveanu, P. Gentil, R. D. Schrimpf, and B. J. Blalock, "Depletion-all-around operation of the SOI four-gate transistor," *IEEE Trans. Electron Devices*, vol. 54, no. 2, pp. 323–331, Feb. 2007.
- [4] S. Cristoloveanu *et al.*, "The four-gate transistor," in *Proc. Solid-State Device Res. Conf.*, 2002, pp. 323–326.
- [5] K. Akarvardar, S. Cristoloveanu, and P. Gentil, "Analytical modeling of the two-dimensional potential distribution and threshold voltage of the SOI four-gate transistor," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2569–2577, Oct. 2006.
- [6] A. Henning, N. Swaminathan, A. Godkin, G. Shalev, I. Amit, and Y. Rosenwaks, "Tunable diameter electrostatically formed nanowire for high sensitivity gas sensing," *Nano Res.*, vol. 8, no. 7, pp. 2206–2215, 2015.
- [7] G. Shalev, G. Landman, I. Amit, Y. Rosenwaks, and I. Levy, "Specific and label-free femtomolar biomarker detection with an electrostatically formed nanowire biosensor," *NPG Asia Mater.*, vol. 5, no. 3, p. e41, 2013.
- [8] L. I. Glazman and I. A. Larkin, "Lateral position control of an electron channel in a split-gate device," *Semicond. Sci. Technol.*, vol. 6, no. 1, pp. 32–35, 1999.
- [9] N. H. E. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*. Reading, MA, USA: Addison Wesley, 2011.
- [10] J. Yuan and J. Liou, *Semiconductor Device Physics and Simulation* (Microdevices Series). New York, NY, USA: Springer, 1998.
- [11] H. E. Dirani *et al.*, "A sharp-switching gateless device (Z3-FET) in advanced FDSOI technology," in *Proc. Joint Int. EUROSIO Workshop Int. Conf. Ultimate Integr. Silicon (EUROSIO-ULIS)*, Jan. 2016, pp. 131–134.
- [12] D. E. Nikonov and I. A. Young, "Overview of beyond-CMOS devices and a uniform methodology for their benchmarking," *Proc. IEEE*, vol. 101, no. 12, pp. 2498–2533, Dec. 2013.
- [13] S. Sze and K. Ng, *Physics Of Semiconductor Devices*, 3rd ed. New York, NY, USA: Wiley, 2006.