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Low-EVM Adaptive Millimeter-Wave Transmit and Receive Systems

A dissertation submitted in partial satisfaction of the requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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2013
The dissertation of Arpit Kumar Gupta is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

Chair

University of California, San Diego

2013
DEDICATION

To my parents - Mrs. Gayatri Devi Gupta and Mr. Ashok Kumar Gupta.
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The dissertation author was the primary author of these materials, and co-authors have approved the use of the material for this dissertation.

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**PUBLICATIONS**


Beamforming is a necessary feature of high-capacity communication links operating at millimeter-wave (mm-wave) bands. Due to the advancement of CMOS-SiGe processes, mm-wave phased arrays can be manufactured at low cost with compact sizes. Transmit arrays are capable of improving the low-output power of silicon PAs through beam directivity. However, reaching (relatively) high efficiency while maintaining high-linearity for QAM waveforms poses a design trade-off. Receive systems suffer from low signal levels and potentially high-power jammers from neighboring links that are not spatially rejected. High linearity is essential for attaining the most efficient communication for both transmit and receive systems. High directivity of the system suggests the need for adaptive beam-scanning meth-
ods that do not require skilled labor to determine the location of the transmitter and receiver.

The first portion of the dissertation discusses the performance of two phased-array architectures (LO and RF scanning) in presence of jammers. Analytical equations are derived which incorporate the antenna array geometry, array circuit architecture, and channel non-linearity.

Secondly, a low-EVM (error-vector-magnitude) direct-conversion I/Q modulator is presented at $Q$-band in 120 nm SiGe process. The effect of various circuit errors on modulation quality is analyzed. In particular, a new analysis and closed-form equations are presented for the impact of I/Q path compression, power-amplifier AM-AM and AM-PM non-linearity on the system EVM. The second version of implemented $Q$-band I/Q upconverter incorporates two 12-bit DACs and active mixers and is demonstrated to pre-distort a 16-QAM through an off-chip power amplifier.

Finally, a novel adaptive beam-steering I/Q receiver array is proposed and demonstrated in 45 nm CMOS SOI process. The proposed architecture allows auto-steering in the direction of the incident signal and supports modulated RF signal for high-data rate communication. The technique uses combined dynamics of coupled-oscillator arrays (COA) and coupled-phased locked loops (CPLL). This is the first demonstration of self-steering mechanism in a monolithic platform.
Chapter 1

Introduction: Reliable & High-speed Millimeter-wave Wireless Communication

Millimeter-wave communication systems offer wide-bandwidth and therefore allow high-data rate communication. Fig. 1.1 pictorially illustrates some of the applications of mmWave systems. Q-band (33 - 50 GHz) circuits are being explored for satellite-communication and defence applications. 60-GHz unlicensed band has been commercialized and is used for home and personal area networks [1]. Automotive radars employ phased-array systems at E-(70/80 GHz) and W-bands(75 - 110 GHz). High capacity E-band point-to-point links enable back haul applications.

Increased path loss and inability to generate high transmit powers at mm-wave frequencies pose significant challenges for implementation of transceivers. Beam-forming provides a practical solution to alleviate most of these issues. Due to small wavelength at high-frequencies, compact and low cost multi-antenna modules can be fabricated. Recent advancement in Si/SiGe integrated circuit processes have presented with new opportunities to implement low cost phased-array transmitters and receivers.

In phased-array systems, transmit power is increased by free-air combining using multiple antennas and power amplifiers. Spectrally efficient quadrature
amplitude modulation (QAM) schemes offer high-data rate in bandwidth-limited channels. To achieve high power efficiency, the power amplifiers are operated close to their compression point which degrades the modulation quality. This results in high transmission errors and low reliability. For receivers, it is important to spatially reject the high power jammers from neighboring links to avoid signal corruption.

1.1 Linearity Comparison of Phased-Array Receiver Architectures

Beamforming for communication and sensing systems requires an appropriate choice of antenna array as well as receiver architecture that provide high dynamic range [2]. Integration considerations have resulted in several variations of the array architectures including RF phase shifting, LO phase shifting and digital beamforming [3, 4]. Previous analysis for transmit arrays described spatial
filtering of coherent intermodulation terms generated by highly nonlinear power amplifiers [5]. In Chapter 2, uniform N-element linear arrays are analyzed to demonstrate the generation of intermodulation distortion (IMD). As an extension to the previous analysis done in [6, 7] for linear and MVDR (Minimum Variance Distortionless Response) arrays, the proposed linearity analysis can be generalized for more sophisticated array configurations that are not necessarily uniformly spaced with an appropriate array factor. The choice of receiver architecture impacts IMD generation. SFDR improvement for a digital-beamforming architecture has been analyzed in [6–8]. Although digital beamforming eliminates the need of RF front end, it requires A/D converters with very high dynamic range (90 dB). Therefore, digital beamforming is practical at only very low carrier frequencies (10 MHz in [6]) and cannot be used at millimeter-wave frequencies.

1.2 Low-EVM I/Q Upconverter for Broadside Transmit Array

Linear transmitters are critical to achieving high-capacity communication links. With the advancement of the fabrication processes through lithographic scaling, transmitter systems that include digital signal processing, analog baseband circuitry, and RF front-ends can be implemented in lowcost Si/SiGe processes at millimeter-wave (mm-wave) bands. High-capacity communication for satellite links suggests using spectrally efficient M-ary quadrature amplitude modulation (QAM). Isolating the impact of various circuit non-idealities on EVM is necessary to satisfy the low error vector magnitude (EVM) demands for M-QAM modulation. Existing literature on transmit system analysis does not decompose sources of non-linearity in a transmitter between the baseband, upconverter, and RF contributions. Typically, the impact of PA amplitude (AM-AM) compression and phase compression (AM-PM) on the EVM is treated but not distinguished from other sources of circuit compression [9, 10]. In particular, the separate contribution of the I/Q path compression and PA compression has not been previously analyzed.

Chapter 3 presents theoretical derivations and discussions of the EVM con-
tributions due to I/Q path non-linearity and PA AM-AM and AM-PM compression for various M-QAM schemes. Other well-known sources of errors like I/Q gain and phase imbalances, LO leakage, LO phase noise and symbol rate are also included in the subsequent analysis to discuss the relative impact and how these errors are related to the compression effects. Process variations and modeling limitations at high frequency result in systematic errors which significantly degrade the EVM. Digital calibration is a preferred method to compensate for these errors instead of incurring high area and power penalties to reduce the mismatches [11]. As higher M-ary QAM is considered, the overall contribution to EVM of these non-linearity effects and circuit mismatches is discussed. Additionally, digital correction through pre-distortion can compensate the transmitter linearity without significant sacrifice to overall efficiency. Mm-wave power amplifiers (PA) are not particularly high-power or efficient relative to amplifiers at RF-bands. Consequently, a mm-wave PA operating at peak efficiency degrades the EVM through gain compression. Digital pre-distortion (DPD) is primarily used for compensating the PA compression. Pre-distortion has been demonstrated for GaAs/GaN PAs [12, 13] and in CMOS process at RF bands [14]. Previously implemented I/Q modulators rely on external sources for baseband signal generation and have not shown the capability to perform digital correction and pre-distortion [14–19]. The implemented I/Q modulator, in this dissertation, contains high-resolution and high-speed D/A converters to perform digital calibration and pre-distortion in a monolithic platform.

1.3 Adaptive Beam-steering I/Q Receiver Array

Self-steering arrays have been suggested as a low-power and low-cost alternative to phased-array transmitters and receivers [20]. Adaptive beam-steering is desirable feature for highly-directive point-to-point links and retro-directive arrays. Due to the very narrow beam-widths in point-to-point links, a manual and precise antenna alignment becomes necessary to maximize signal-to-noise ratio. Adaptive beam-alignment eliminates the cost and time associated with the skilled antenna alignment. Retrodirective receivers automatically point their beam in the direc-
tion of incident RF signal. Using a phase conjugation schemes, a signal can be transmitted back in the direction of the interrogator establishing full duplex communication. Such systems are particularly attractive for mobile communication systems like satellite networks, aircraft navigation, collision avoidance sensors and RFID [21]. Previously, self-steering arrays have been demonstrated using discrete components [20, 22, 23]. This work demonstrates the first monolithic self-steering I/Q receiver array.

An open-loop configuration with external phase shifters is used for auto-steering in [20]. Such systems require careful calibration and are vulnerable to mismatches and temperature variations. Retrodirectivity is achieved using mutually exclusive modulation schemes for the received and transmitted signal in [23]. [22] uses digital-signal processing (DSP) to extract the array geometry phase. In this work, a new compact and low power architecture is proposed that does not require DSP and could be used with any modulation scheme. The proposed architecture achieves self-steering with the combined operation of coupled-oscillator array (COA) and coupled-phased locked loop (CPLL). Coupled-oscillators have been shown to be a practical alternative at mmWave phased-array transmitters [24]. In the past, coupled-oscillator arrays have been used to demonstrate beam-steering using edge-detuning [25, 26] and single control voltage [27]. To eliminate the need of control signal and to achieve self-phasing, coupled-phased locked loops are used to automatically detune an array of coupled oscillators. Although the fabricated receiver array operates at X-band (8 - 12 GHz), it could be appended with a mmWave front-end to extend the operating frequency.

1.4 Dissertation Organization

Background material, previous work and new contributions have been mentioned in Chapter 1. Importance of linear and adaptive phased-array Tx/Rx modules has been outlined.

Chapter 2 illustrates the new analysis for characterizing the array factor of IMD products generated by incident RF and jammer signals. The array factor
for a linear antenna array is reviewed. This array factor analysis is extended to calculate and compare the array factor for third-order IMD (IM3) products. The spatial orientation of RF and jammer (JM) signals generates in-band interference in the receiver array. Finally, The theoretical SFDR of the two architectures is compared.

Chapter 3 presents a comprehensive analysis of the circuit non-idealities and mismatch contributions to the EVM. The EVM is calculated from the derived equations for various cases. The EVM dependance on the M-ary QAM modulation formats is also discussed. Next, the first version design of Q-band I/Q upconverter is presented. The first version focuses on the low-power implementation with on-chip 8-bit digital-to-analog D/A converters (DACs). For the implementation of second version, the EVM analysis is used to derive the key system specifications, which is followed by the discussion of the implemented modulator architecture and the design of various building blocks. Measurement set-up details and results are included. Digital calibration of the systematic errors is performed and the achieved EVM for different M-ary QAM schemes is presented. Finally, EVM enhancement with the aid of digital pre-distortion of the input signal is demonstrated in while an external power amplifier is operated close to compression point.

Various concepts used to arrive at the final adaptive beam-steering receiver array architecture are presented in chapter 4. The effect of key design parameters on stability of the system is also presented. Analysis is followed by the design of a prototype 4-element I/Q receiver array. Schematics and simulation results of various building blocks are mentioned. Measurement set-up and test printed-circuit board are illustrated. The array response with 4-element and 3- elements is plotted to demonstrate the self-steering capability. Oscillator tuning range, array locking bandwidth, wideband spectra and phase noise are also shown. The array is also measured with different M-QAM modulated signals and exhibits stable operation with low error-vector magnitude.
Chapter 2

Spur Free Dynamic Range Prediction for Phased-Array Receivers

2.1 Linear Antenna Array & Array Factor

The antenna array factor is a useful method for predicting the spatial pattern of the antenna array independent of the details of the element pattern [28]. In practical scenarios, the element pattern may introduce mutual coupling that limits the scan range of the array [29]. For a sufficiently large number of elements, the directivity, beamwidth and sidelobe levels are determined by the array factor. Since omni-directional antenna elements allow the greatest steering range, an omni-directional element pattern is assumed in this work without loss of generality. The effect of the element pattern is resolved by multiplying the array factor by element factor and is subsequently considered.

A uniform linear array factor is described in Fig. 2.1. The array factor (AF) in the azimuth angle $\psi$ for a linear one-dimensional array with $N$ elements is
Figure 2.1: Linear array in azimuth plane \((N = 8)\).

\[
AF(\psi) = \sum_{n=0}^{N-1} e^{jnkd(sin\psi - sin\psi_{RF})},
\]

\((2.1)\)

where \(k = \frac{2\pi}{\lambda}\), \(d\) is the spacing between elements, and \(\psi_{RF}\) is the desired beam direction. To adjust the maximum array gain in the direction of \(\psi_{RF}\), the phase in \(n^{th}\) RF signal path is tuned to

\[
\phi_n = nkd\sin\psi_{RF},
\]

\((2.2)\)

where \(n\) ranges from 0 to \(N-1\). The linear array factor is plotted in Fig. 2.2 with \(d = \frac{\lambda}{2}\) to minimize the sidelobe level. Linear arrays conventionally offer high sidelobe suppression (13.3 dB for \(d = \frac{\lambda}{2}\)) but sidelobe levels tend to increase when the beam is steered away from broadside. As the array is scanned towards ±40°, the beamwidth widens from just over 10° to more than 17° for an eight element array. The sidelobes are maintained at 13 dB below the carrier.

Non-uniform arrays further reduce the sidelobes [30]. This work does not further consider non-uniform array weighting or the element factor since the impact of each can be incorporated into the array factor from well-known references [28]. The following analysis relates a given array factor to the array linearity.
Figure 2.2: Normalized linear array factor for $N = 8$ and $d = 0.5\lambda$ in the azimuth plane.
2.2 Single-channel Receiver Linearity in Presence of Jammers

Wideband receivers are prone to intermodulation distortion due to the presence of strong interferers that mix with the desired RF signal. Each receiver chain generally consists of a low-noise amplifier (LNA) and mixer. In this analysis, these circuit elements are modeled as weakly nonlinear blocks, i.e. third-order nonlinearities. The weakly nonlinear receiver channel is illustrated in Fig. 2.3 where the RF and jammer (JM) tones at frequencies $f_{RF}$ and $f_{JM}$ generate two in-band intermodulation (IM) products at $f_1 = 2f_{RF} - f_{JM}$ and $f_2 = 2f_{JM} - f_{RF}$ due to the third order nonlinearity.

The general case of a nonlinearity in a single narrowband receive channel requires a Volterra series to represent the circuit response [8]. The voltage at the output of each receiver chain before the signals are combined is

$$V_n = G_1(f_a) \circ V_{RF} + G_2(f_a, f_b) \circ V_{RF}^2 + G_3(f_a, f_b, f_c) \circ V_{RF}^3,$$

(2.3)

where $G_k(\cdot)$ is the $k^{th}$-order Volterra kernel. For a memoryless (wideband) nonlinearity, the nonlinear coefficients become frequency independent and eqn. (2.3) simplifies to

$$V_n = \sum_{i=1}^{3} G_i V_{RF} (\sin \Phi_{RF} + \sin \Phi_{JM})^i \approx G_1 V_{RF} (\sin \Phi_{RF} + \sin \Phi_{JM}) +$$

$$\frac{3}{4} G_3 V_{RF}^3 (\sin (2\Phi_{RF} - \Phi_{JM}) + \sin (2\Phi_{JM} - \Phi_{RF})),

(2.4)$$

where the absolute phases are $\Phi_{RF} = \omega_{RF}t + \phi_{RF,n}$ and $\Phi_{JM} = \omega_{JM}t + \phi_{JM,n}$. The expression considers only the frequency components resulting from the nonlinear
behavior that fall near the RF signal. Harmonics are assumed to be filtered and second-order intermodulation is ignored from further analysis. The relative phase of the RF and JM signals, $\phi_{RF,n}$ and $\phi_{JM,n}$ at each receiver element are found from eqn. (2.2). Assuming homodyne down-conversion or direct conversion (i.e. $f_{LO} = f_{RF}$), the relative phases of the two third-order intermodulation products located at $f_1$ and $f_2$ are

$$\phi_{1,n} = 2\phi_{RF,n} - \phi_{JM,n} - \phi_{LO,n} \text{, and}$$

$$\phi_{2,n} = 2\phi_{JM,n} - \phi_{RF,n} - \phi_{LO,n}. \tag{2.5a} \tag{2.5b}$$

These phase expressions are valid only if JM and RF frequency are close to each other. Including the phase of the RF and JM tones allows investigation of IM generation in receiver arrays.

Third-order intermodulation distortion products (IM3) are calculated from the last term in eqn. (2.4), e.g. $IM3 = \frac{3}{4}G_3V_{RF}^3$. Conventionally, $IM3$ is defined for two tones with equal RF amplitude. The actual IM3 voltage is found by considering that the jammer signal has a power $\Delta$ dB relative to the RF signal, e.g. $\Delta = P_{JM} - P_{RF}$ in dBm. If $f_2$ is the jammer, the value (in dB) of the IM3 products is

$$IM3_1 = IM3 + \Delta \tag{2.6a}$$

$$IM3_2 = IM3 + 2\Delta \tag{2.6b}$$

Fig. 2.4 shows the power of the desired RF tone and the IM tones with respect to the input power of RF and jammer signals in dBm. Third-order intercept (TOI) point or input-referred intercept point third (IIP3) of the receiver is the measure of the receiver linearity and is defined as the input power ($P_{RF} = P_{JM}$) for which the power of the RF and IM tones are equal at the receiver output. For the weakly non-linear receiver model of Fig. 2.3, TOI can be expressed as $TOI_G = \sqrt{\frac{4G_1}{3G_3}}$. A high TOI value for the receiver indicates good receiver selectivity. Receiver sensitivity depends on the noise figure. The minimum detectable
signal power at the input is $MDS_m = FkTB$ where $F$ and $B$ are the receiver noise figure and signal bandwidth. $k$ is the boltzman constant and $T$ is the temperature in °K. The spur-free dynamic range of a receiver is defined as the range of input powers for which the signal is detectable and free of spurs. SFDR in dB can be graphically written from Fig. 2.4 as

$$SFDR(dB) = \frac{2}{3}(TOI - MDS_m).$$  \hspace{1cm} (2.7)

This conventional analysis of linearity considers only the linearity of an individual receive channel. While we might predict the array to eliminate jammers coincident at nulls of the array factor, this would incorrectly suggest that intermodulation distortion is also eliminated. The following sections discuss how the choice of the receiver architecture influences the generation of intermodulation distortion.

2.3 Linearity in mmWave Phased-Array Receiver Architectures

This section analyzes and compares the SFDR of the two different receiver architectures illustrated in Fig. 2.5 which have been proposed for millimeter-wave systems.

First, LO-scanned arrays combine energy from each of $N$ receiver channels at the IF frequency. This approach simplifies monolithic integration of the circuitry since no phase shifter is required in the RF path. Instead, multiple oscillator phases are generated and distributed to each receiver [31, 32]. A mixer is needed at each channel and the LO phase controls the IF phase of each channel. Earlier work on coupled oscillator arrays also suggested an LO-scanning approach for receiver arrays [25,33]. Continuous phase distributions can be generated across the array through manipulation of nonlinear dynamics in the coupled oscillator system [34]. Second, RF-scanned arrays are adapted from conventional array systems and combine energy from each of the $N$ receiver channels at the RF band. Therefore, only a single mixer is required but $N$ RF phase shifters are introduced. This
approach has been implemented at microwave and millimeter-wave frequencies in silicon monolithic processes through the development of wideband 360 degree phase shifters [4, 35]. Prior work has not comprehensively analyzed the impact of antenna array and receiver architecture on the fundamental limits of spur free dynamic range (SFDR).

2.3.1 LO-scanned Arrays

For an LO-scanned array, the weakly nonlinear coefficients $G_k$ in eqn. (2.4) consist of the cascade of the LNA and mixer as shown in Fig. 2.3. The LNA is represented by a block $H$ that is weakly nonlinear, e.g. $V_{x,n} = H_1 V_{RF} + H_2 V_{RF}^2 + H_3 V_{RF}^3$ while the frequency translation from RF to IF in the mixer is also assumed to exhibit a weakly nonlinear response $V_{IF} = M_1 V_y + M_2 V_y^2 + M_3 V_y^3$ where $V_{IF} = \sum V_{y,n}$ for the LO-scanned receiver.

In Fig. 2.6, this array architecture is decomposed into two circuit paths; the first is the fundamental path represented by $G_1 = H_1 M_1$ and the second is the intermodulation distortion path described by $G_3 = H_1^3 M_3 + 2H_1 H_2 M_2 + H_3 M_1$. An intermodulation array factor $AF_{IM3}$ accounts for the phase relationship between the $IM3$ products analogous to the array factor.

The array factor for intermodulation terms in the LO phased arrays are calculated based on the relative phase of the RF and JM signal. For a linear array, the phase of the RF and JM signal at each element is $\phi_{RF,n} = nkd \sin \psi_{RF}$ and $\phi_{JM,n} = nkd \sin \psi_{JM}$. Summing the terms from eqn. (2.5a) and (2.5b), the array factor for the $IM3$ terms is

$$AF_{IM3,1}(\psi_{RF}, \psi_{JM}) = \sum_{n=1}^{N} e^{j(2\phi_{RF,n} - \phi_{JM,n} - \phi_{LO,n})}$$  \hspace{1cm} (2.8a)

and

$$AF_{IM3,2}(\psi_{RF}, \psi_{JM}) = \sum_{n=1}^{N} e^{j(2\phi_{JM,n} - \phi_{RF,n} - \phi_{LO,n})}.$$  \hspace{1cm} (2.8b)

When the signals are coincident (i.e. $\psi_{RF} = \psi_{JM}$), $|AF_{IM3,1}| = |AF_{IM3,2}| = |AF|$. In other words, the array factor for the RF signal is the same as the array factor for the IM3 products and the array is incapable of distinguishing these
signals and provides no $IM^3$ rejection. However, if the RF and JM frequencies are different, then $\phi_{RF,n} \neq \phi_{JM,n}$ even if both signals are coincident since propagation constant $k$ is different and the two array factors should be evaluated.

The proposed intermodulation array factor accounts for spatial variation of the IM3 products generated by the jammer and the RF signal. Each of the IM3 ($m = 1, 2$) products for the LO-scanned array is

$$IM^3_m(\psi_{RF}, \psi_{JM}) = \frac{3}{4} AF_{IM^3,m} G^3_{RF},$$

where the amplitude of the $IM^3$ tones depends on the strength of the third-order nonlinearity of the receive chain and the IM3 array factor described in eqn. (2.8a)-(2.8b).

The input-referred third-order intercept ($TOI$) is a measure of the linearity of a generalized receiver [36, 37]. In this treatment, both quantities refer to an input referred voltage. For LO-scanned arrays, the $TOI$ is expressed as the RF voltage that causes the $IM^3$ to reach the same amplitude as the RF signal, i.e. $|G^1_{RF}| = |IM^3_m(\psi_{RF}, \psi_{JM})|$.  

$$TOI(\psi_{RF}, \psi_{JM}) = \sqrt{\frac{4G^1_{RF}AF(\psi_{RF})}{3G^3_{max}(AF_{IM^3,m}(\psi_{RF}, \psi_{JM}))}}.$$  

The $TOI$ expression accounts for the azimuthal arrangement of the RF and JM signals. The second equality makes an important relationship between the $TOI$ of the array and the $TOI$ of an individual receiver channel. The denominator of eqn. (2.10) of the square root chooses the maximum array factor between the two intermodulation products ($m = 1, 2$). For a coincident jammer, the $TOI$ of the LO-scanned array reduces to $TOI_G$. When the array eliminates both the IM3 terms ($AF_{IM^3,m} = 0$), the $TOI$ of the array becomes infinite even while the individual receive chain has a finite $TOI$. Therefore, the array offers more linearity than is predicted from the finite linearity of each channel.

The $TOI$ for the linear array normalized to the channel $TOI$ is plotted in Fig. 2.7 as a function of the azimuth jammer angle. The array factor $AF$
is constant since the plot assumes that the incident angle of the RF signal is \( \psi_{RF} = 0 \). The intermodulation array factor \( AF_{IM3} \) depends on the incident angle of the jammer since the \( IM3 \) products generated at each antenna element are down-converted with different phases. Peaks in the \( TOI \) plot indicate where the intermodulation array factor effectively nulls the \( IM3 \) terms while minima indicate points where no or little \( IM3 \) rejection occurs. Notably, the minimum \( TOI \) is more than 6 dB higher than that of the individual receive channel from azimuth angles between 15° and 65°.

While the array might eliminate the jammer, it might not eliminate the \( IM3 \) products. From Fig. 2.2, the linear broadside scanned array factor has nulls at ±90° and one would expect that when the jammer is incident from ±90° the array rejects the jammer after beam-forming as shown in Fig. 2.6. However, both the JM and RF signals are present in the circuits until the output of the mixer and consequently, \( IM3 \) tones are generated before beam-forming. From eqn. (2.8a), (2.8b) and (2.10), the \( IM3 \) tones at \( 2f_{RF} - f_{JM} - f_{LO} \) add out-of-phase after beam-forming while the \( IM3 \) tones at \( 2f_{JM} - f_{RF} - f_{LO} \) add in-phase. Therefore, jammers incident from an angle of ±90° cause the \( TOI \) to become unity for LO-scanned arrays relative to the channel \( TOI \) as shown in Fig. 2.7.

Note that an omni-directional element pattern has been assumed in previous analysis. The analysis can be generalized to take into account the element factor, \( E(\psi) \). For instance, eqn. (2.9) can be modified as

\[
IM3_1(\psi_{RF}, \psi_{JM}) = \frac{3}{4} E(\psi_{RF})^2 E(\psi_{JM}) AF_{IM3,1} G_3 V_{RF}^3 \\
IM3_2(\psi_{RF}, \psi_{JM}) = \frac{3}{4} E(\psi_{RF}) E(\psi_{JM})^2 AF_{IM3,2} G_3 V_{RF}^3
\]

(2.11a)

(2.11b)

where \( E(\psi_{RF}) \) and \( E(\psi_{JM}) \) are the element factors for RF and jammer signal respectively. If the element pattern does not have any gain at ±90°, the jammer will be eliminated completely through the element pattern. In that case, the \( TOI \) will be infinite at ±90° jammer incident angles.

The sensitivity of the \( TOI \) improvement to the RF steering angle is shown in Fig. 2.8. Here, the minimum \( TOI \) shifts with the RF beam angle. Additionally,
a TOI shadow occurs at an angle 60° offset from the main lobe. In this shadow, the array is particularly sensitive to IM3 generation due to incident jammers.

2.3.2 RF-scanned Arrays

In the case of the RF-scanned array, a phase shifter is included before the RF power combiner and introduces additional nonlinearity. Now, the weakly nonlinear combination of the LNA and phase shifter is represented by coefficients $H_k$ while the mixer is still represented by $M_k$. Finally, the beam is formed after the mixer when the IF signals are combined, i.e. $V_y = \sum V_{x,n}$. Since the RF signals are combined, the generation of IM3 products is distinguished from the diagram shown in Fig. 2.6 for the LO-scanned array. The beam is formed in the RF direction and while the fundamental path gain is identical to that for the LO array, e.g. $H_1M_1AF$, IM3 terms are generated through two paths shown in Fig. 2.9. Based on this figure, the IM3 terms are expressed in eqn. (2.12a) and (2.12b). The element factor could be accounted for using a similar approach as in previous section.

Since the RF-scanned array places some of the overall receiver nonlinearity after the power combining element, the overall linearity of the cascade is $\text{TOI}_G^{-2} = \text{TOI}_H^{-2} + N^2H_1^2 \cdot \text{TOI}_M^{-2}$, and the TOI is calculated as shown in eqn. (2.13a) and (2.13b). Rewriting the overall linearity in terms of the mixer linearity shows that

$$\frac{N_H}{\sqrt{R^2 - 1}} = \frac{\text{TOI}_M}{\text{TOI}_H}$$

where $R$ is the ratio of LNA (and phase shifter) TOI to the total TOI, e.g. $R = \frac{\text{TOI}_H}{\text{TOI}_G}$. Each of these equations expresses the TOI in terms of the ratio of $R$. Since the LNA TOI must be higher than the overall receiver TOI, this ratio is always greater than one.

When $R = 1$, the mixer is perfectly linear and the LNA introduces all of the nonlinearity in the receive chain. Under this condition, eqn. (2.13a) and (2.13b) reduce to the results derived for the LO-scanned array since the LO-scanned array placed all of the nonlinear elements before the IF combining element. When $R \to \infty$, the LNA is ideal and the mixer contributes all of the nonlinearity in the receive chain.

The ratio $R$ allows comparison for both architectural approaches when con-
strained to a fixed overall receiver linearity $TOI_G$. In this case, the linearity is weighted between the LNA and the mixer. The choice of $R = N$ results in a relationship between the mixer and LNA linearity where the output referred intercept point of the LNA and phase shifter is equal to the input referred intercept point of the mixer.

The $TOI$ improvement for a linear RF-scanned array is shown in Fig. 2.10. The $TOI$ improvement is compared for $R = 1$ and $R = 8$. The $R = 1$ condition implies that the mixer is perfectly linear and all the non-linearity is introduced before power-combining. Therefore, for $R = 1$, the RF-scanned receiver array degenerates to the LO-scanned array architecture previously described. From eqns (2.13a) and (2.13b), the $TOI$ expression normalized to the channel $TOI$ reduces to eqn. (2.10). The latter condition for the RF-scanned array ($R = 8$) shows a few interesting features. First, the $TOI$ improvement for the RF-scanned array is always better than the LO-scanned array for a given overall receiver chain linearity $TOI_G$. Second, the $TOI$ of the RF-scanned array removes the shadow region at $\pm 90^\circ$ present for the LO-scanned array. The $TOI$ does not significantly vary between the two choices of $R$ for angles under $\pm 45^\circ$.

The sensitivity of the $TOI$ with RF steering angle for the RF-scanned array is shown in Fig. 2.11. As the beam is steered to $40^\circ$, the $TOI$ of the RF-scanned array becomes slightly more sensitive at around $-75^\circ$ jammer angle.

The ratio $R$ describes the relative linearity of circuit components before and after beam-forming. High values of $R$ imply that the non-linearity is introduced after beam-forming. From eqns (2.13a) and (2.13b), the $TOI$ expressions normalized to the channel $TOI$ simplify to $\frac{N}{\sqrt{AF(\psi_{JM})AF(\psi_{RF})}}$ and $\frac{N}{AF(\psi_{JM})}$ for large $R$ and indicate that the $TOI$ is improved with the number of elements.

The variation of the $TOI$ with respect to $R$ at various incident jammer angles is shown in Fig. 2.12 when the array is steered to broadside. Starting at $\pm 45^\circ$, the $TOI$ improves modestly until reaching a plateau around $R$ of 1.4. At $\pm 60^\circ$, the $TOI$ is unchanged with the choice of $R$. At this particular angle, both array architectures offer the same $TOI$ for $N = 8$. At $\pm 75^\circ$, the $TOI$ generally improves till just over an $R$ of 4. Note that the $TOI$ improves at 20 dB per decade.
At $\pm 90^\circ$ jammer angle, the TOI improves indefinitely since after beam-forming the jammer is rejected and mixer non-linearity does not significantly impact the TOI. One important trend is evident. As the immunity to jammers is required over a larger range of angles, the required value of $R$ for a given number of elements increases. In other words, more TOI improvement is realized at $\pm 75^\circ$ as opposed to $\pm 45^\circ$ with a larger choice of $R$. Therefore, the distinction between the RF- and LO-scanned receiver arrays is greater as the specification of the range of incident jammer angles increases.

These TOI curves estimate the intermodulation power resulting from a given RF and jammer signal. Since the RF and JM signals are not typically the same amplitude, the actual power of the IM3 tones is determined from eqn. (2.6a) and (2.6b). In terms of the TOI, the input-referred power of IM3 tones in dBm is

\[
P_{IM3,1} = 2P_{RF} + P_{JM} - 2 \cdot TOI(\psi_{RF}, \psi_{JM})
\]  

\[
P_{IM3,2} = 2P_{JM} + P_{RF} - 2 \cdot TOI(\psi_{RF}, \psi_{JM})
\]

The spatial dependence of the TOI now accounts for the relative relationship between the RF and JM signals.

### 2.4 SFDR of LO- and RF-scanned Arrays

An example set of receiver parameters based on circuit implementations is shown in Table 2.1. While the SFDR of an array is limited to the SFDR for a single channel, the LO-scanned and RF-scanned arrays have different SFDR limits since the single channel of the RF-scanned array introduces an additional phase shifter. For the LO-scanned receive channel consisting of an LNA and mixer, the RF receiver has an SFDR of 107.3 dBc $\cdot$ Hz$^{2/3}$. For the RF-scanned receiver channel which includes the phase shifter, the SFDR is reduced to 102.1 dBc $\cdot$ Hz$^{2/3}$. In this example, the reduced SFDR is the result of the linearity degradation introduced by the phase shifter. Absolute comparison of the circuit architectures based on SFDR is approximate because of the range of circuit implementation trade-offs between
gain, noise figure, linearity and power consumption. This example suggests that implementation differences are handled through a relative SFDR comparison for either the RF-scanned and LO-scanned arrays by normalizing against the SFDR for the receive channel.

From eqn. (2.7), receiver SFDR depends not only on linearity (TOI) but also on noise factor. Standard noise factor analysis for cascaded systems is used to calculate noise factor for LO and RF scanned arrays [36]. The noise factor for a homodyne LO-scanned phased array is

\[ F_{LO,ARRAY} = F_{LNA} + \frac{F_M - 1}{G_{LNA}}, \]  \hspace{1cm} (2.15)

where \( F_{LNA} \) and \( G_{LNA} \) are the noise factor and gain of the LNA and \( F_M \) and \( G_M \) are the noise factor and gain of the mixer. Using values from Table 2.1, the SFDR of the linear, LO-scanned array is plotted as a function of the jammer angle in Fig. 2.13.

Two major points are evident when comparing the SFDR as a function of jammer angle with a small and large number of elements. As predicted earlier, the SFDR of the LO-scanned phased array is sensitive to jammers at ±90°. At these two angles, the SFDR is not enhanced by the number of elements. Second, the peak SFDR improvement occurs at ±40° and provides an additional \( \frac{2}{3} \cdot 10 \log_{10} N \)

Table 2.1: Receiver Component Budget

<table>
<thead>
<tr>
<th>Component</th>
<th>Gain [dB]</th>
<th>Noise Figure [dB]</th>
<th>TOI [dBm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>10</td>
<td>7</td>
<td>0</td>
</tr>
<tr>
<td>Phase Shifter</td>
<td>0</td>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td>Mixer</td>
<td>0</td>
<td>17</td>
<td>10</td>
</tr>
<tr>
<td>Receive Chain (without phase shifter)</td>
<td>10</td>
<td>10</td>
<td>-3</td>
</tr>
<tr>
<td>Receive Chain (with phase shifter)</td>
<td>10</td>
<td>10.3</td>
<td>-10.5</td>
</tr>
</tbody>
</table>
of SFDR improvement at these angles. In other words, the 2-element array SFDR improves by at most 2 dB while the 64-element array SFDR improves by at most 12 dB.

The noise factor for an RF-phase shift array is the same as LO-scanned array. Since the noise power at the output of a lossless power combiner is the same as the noise power at each of its inputs (uncorrelated), the noise factor contribution due to the mixer is not divided by the array gain $N$ [38]. The input referred noise power of the mixer will appear at each of the $N$ input ports of the power combiner, resulting in the same noise figure as expressed in eqn. (2.15). Using the values from Table 2.1, the SFDR of the linear, RF-scanned array is plotted as a function of the jammer angle in Fig. 2.14. Again the minimum SFDR occurs when the jammer is coincident with the RF signal. However, the RF-scanned array offers a significant advantage when compared to the LO-scanned array at other angles. In particular, the SFDR reaches a maximum at $\psi_{RF} = \pm 90^\circ$. Whereas the SFDR for the LO-scanned array in Fig. 2.13 generally begins to degrade for angles greater than $50^\circ$, the SFDR is shown here to remain above 12 dBC · Hz$^{2/3}$.

### 2.5 Conclusions

This chapter presents a general analysis of linearity in phased array receiver architectures based on spatial variation of intermodulation distortion products that considers the antenna array factor, array receiver architecture and receive channel linearity. Differences in intermodulation generation are compared for the two different receiver architectures. While the LO-scanned phased array offers no rejection to jammers incident along the linear array axis, the RF-scanned phased array offers theoretically superior SFDR across a broader range of jammer angles.

### Acknowledgements

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This work was supported by Dr. Brian Meadows and John Cothern of SPAWAR-Pacific. This dissertation author was the primary author of this material.
Figure 2.4: Power of the RF and IM tones at receiver output in presence of jammer.
Figure 2.5: Two phased array architectures based on RF-scanning and LO-scanning.

Figure 2.6: Weakly nonlinear model for intermodulation generation in an LO-scanned array approach. Note that intermodulation terms are introduced before IF power combining.
Figure 2.7: TOI normalized to $TOI_G$ for a linear omni-element array as a function of jammer angle ($N = 8$, $d = 0.5\lambda$ and $\psi_{RF} = 0^\circ$).
Figure 2.8: LO-scanned $TOI$ improvement normalized to $TOI_G$ in linear omni-element array ($N = 8$, $d = 0.5\lambda$).
Figure 2.9: Weakly nonlinear model for intermodulation generation in RF-scanned arrays. Here a nonlinear block is introduced after RF power combining.

\[ IM3_1(\psi_{RF}, \psi_{JM}) = \frac{3}{4} V_{RF}^3 [H_3 M_1 AF_{IM3,1}(\psi_{RF}, \psi_{JM}) + H_1^3 AF(\psi_{RF})^2 AF(\psi_{JM}) M_3] \]  

(2.12a)

\[ IM3_2(\psi_{RF}, \psi_{JM}) = \frac{3}{4} V_{RF}^3 [H_3 M_1 AF_{IM3,2}(\psi_{RF}, \psi_{JM}) + H_1^3 AF(\psi_{RF}) AF(\psi_{JM}) M_3] \]  

(2.12b)
\[
TOI_1^{-2}(\psi_{RF}, \psi_{JM}) = TOI_G^{-2} \frac{1}{N^2} \frac{AF(\psi_{RF}) AF(\psi_{JM})}{AF(\psi_{RF})} + TOI_H^{-2} \left( \frac{AF_{IM3,1}(\psi_{RF}, \psi_{JM})}{AF(\psi_{RF})} - \frac{1}{N^2} AF(\psi_{RF}) AF(\psi_{JM}) \right) + \frac{1}{N^2 R^2} AF(\psi_{JM}) AF(\psi_{RF})
\] 

\[ (2.13a) \]

\[
TOI_2^{-2}(\psi_{RF}, \psi_{JM}) = TOI_G^{-2} \frac{1}{N^2} AF(\psi_{JM})^2 + TOI_H^{-2} \left( \frac{AF_{IM3,1}(\psi_{RF}, \psi_{JM})}{AF(\psi_{RF})} - \frac{1}{N^2} AF(\psi_{JM})^2 \right) + \frac{1}{N^2 AF(\psi_{JM})^2}
\] 

\[ (2.13b) \]

**Figure 2.10:** TOI improvement in linear omni-element array for different ratios of \( TOI_H \) to \( TOI_G \) \( (N = 8, d = 0.5\lambda \text{ and } \psi_{RF} = 0^\circ) \).
**Figure 2.11**: RF-scanned $TOI$ improvement normalized to $TOI_G$ in linear omni-element array ($R = 8$, $N = 8$, $d = 0.5\lambda$).
Figure 2.12: TOI improvement with respect to ratio $R$ for a linear omni-element RF-scanned array steered to broadside.
Figure 2.13: SFDR normalized to the receive chain SFDR for a linear, LO-scanned ($R = 1.0$) phased array ($\text{NF}_{LNA} = 7 \text{ dB}, G_{LNA} = 10 \text{ dB}, \text{NF}_{MIX} = 17 \text{ dB}$).
Figure 2.14: SFDR normalized to the receive chain SFDR for a linear, RF-scanned ($R = 8$) phased array ($NF_{LNA} = 7$ dB, $G_{LNA} = 10$ dB, $NF_{MIX} = 17$ dB).
Chapter 3

Highly Accurate (Low-EVM) Millimeter-wave Direct-conversion I/Q Upconverters

3.1 System Overview

The goal of this work is to demonstrate an efficient and highly linear direct-conversion I/Q transmitter at Q-band (45GHz). Fig. 3.1 shows the complete system block diagram. Digitally pre-distorted I/Q data is fed to the I/Q upconverter IC. The on-chip digital-to-analog converters convert the digital signal into analog which is then filtered using a reconstruction filter and upconverted to 45 GHz carrier frequency. The modulated RF signal at Q-band is distributed to power amplifier grid which is connected to a broad-side antenna array for beam-forming. The scope of this work is to demonstrate a nearly error-less I/Q upconverter chip in Si/SiGe process using on-chip baseband and mmWave circuits.
3.2 Error Vector Magnitude (EVM) and Bit Error Rate (BER)

Error vector magnitude (EVM) is the key metric for the transmit systems employing $M$-QAM. A low EVM is desired to achieve reliable transmission. For any modulated signal constellation, EVM defined as the normalized error between the transmitted symbol and the reference or ideal symbol. EVM is related to bit error rate and is plotted for 64-QAM in Fig. 3.2. Generally, BER equal to 1e-6 is considered acceptable in wireless communication which is equivalent to 4.4% EVM. However, a significant portion of this error comes from channel noise and limited receiver sensitivity. Therefore, the EVM contribution due to transmitter must be minimized. Consequently a low $EVM = 2.5\%$ is targeted for this work.

3.3 First Generation Design - A 9 mW Q-band I/Q Upconverter

This work investigates the low-power implementation of an I/Q modulator at $Q$-band with on-chip 8-bit digital-to-analog D/A converters (DACs). The integration of both mixed-signal data converters and millimeter-wave I/Q modualtors results in a low EVM. The proposed modulator is measured up to the symbol rates of 10 MS/s (40 Mbps @ 16-QAM) with $M$-ary QAM modulation and could achieve data rates as high as 240 Mb/s at 39 GHz. The proposed circuit architecture is presented in section 3.3.1 and discusses the specification and design of the baseband and RF circuit blocks. Section 4.3 presents measurement results of

![Figure 3.1: System block diagram and scope of this work.](image_url)
the baseband circuit linearity including static and dynamic D/A converter perfor-
mance. Small-signal and large-signal measurements verify the matching of the 
modulator and linearity of the upconverter to predict the EVM performance and 
compare this to prior work. QPSK and QAM modulation results are demonstrated
to show extremely low EVM with power consumption under 10 mW.

3.3.1 Circuit Architecture

Fig. 3.3 illustrates the block diagram and chip microphotograph of the pro-
posed direct conversion I/Q modulator with two 8-bit digital-to-analog converters 
(DAC). Two 240 Mb/s serial interfaces are provided to reduce the pad frame. This 
data is de-multiplexed to a parallel bus with a shift register and divided version 
of the input clock. The DAC sampling rate is 60 MSamples/s to support symbol 
rates that exceed 10 MSymbols/s with oversampling. Oversampling improves the 
ability to reject spurious tones generated by the DAC due to the clock.
For high spur-free dynamic range (SFDR), the DAC static performance is characterized by differential non-linearity (DNL) and integral non-linearity (INL) \[^{[39]}\]. A partially-segmented, current-steering DAC was implemented as shown in Fig. 3.4. Six binary-weighted current sources are controlled using the six least significant bits (LSB) while the two most significant bits (MSB) are decoded to control three linear current sources. The static performance of a current-steering DAC depends on how well the current sources are matched \[^{[39]}\]. For INL \( \leq 0.5 \) LSB, a 99.7% yield across 8-bits of resolution requires a standard deviation in the LSB current mismatch of under 1% \[^{[40]}\].

A cascode PMOS current source increases the output impedance. For a given current and area, the PMOS device requires higher source-gate voltage and is less sensitive to device \( V_t \) mismatch. For an LSB current of 1 µA, a PMOS current source with \( W = 3 \mu m \) and \( L = 3 \mu m \) yields around 1% standard deviation for current mismatch when operating at an effective overdrive voltage of 115 mV under typical process-voltage-temperature (PVT) conditions. To maintain the high output resistance, all current sources, cascodes and switches are scaled according...
Figure 3.4: Partially segmented DAC architecture and digital interface.

to the desired current handling. The DAC full scale current is 255 µA. The DAC operates at a sampling rate of 60 MHz to oversample the transmitted symbols and alleviates filtering requirements of the clock harmonics from the baseband signal. A single pole $RC$ filter with a cut-off frequency of 30 MHz filters the DAC output. A differential load resistance of 2 $k\Omega$ provides a 510 mV differential output voltage swing at the DAC full-scale current while limiting the baseband load capacitance to 2.6 pF.

Each DAC has a signal buffer designed to drive a low impedance of the I/Q double-balanced passive mixers as shown in Fig. 3.4. A PMOS differential pair allows low common mode voltage at the DAC. A differential resistive load of 400 $\Omega$ eliminates the need of a common-mode feedback circuit. The voltage swing presented to the mixer is about 500 mVpp differential which is equivalent to -2 dBm IF input power. The buffer consumes 4mA current from a 1V supply.

A passive double balanced ring mixer is implemented to directly convert the IF signal to 45 GHz [41]. The passive mixer offers high linearity while consuming zero dc power at the expense of conversion loss. In the transmitter, high power (-2 dBm) is supplied to the mixer. The double-balanced mixer suppresses the LO-to-RF leakage and even-order LO and IF harmonics. The mixer achieves a
conversion loss of 8.17 dB and input-referred P1dB of 9 dBm for an LO power of 6 dBm. The DSB noise figure is under 6.6 dB. The differential RF output of the mixer is converted to a single-ended output by a passive balun and an on-chip combiner to produce a complex RF signal.

A hybrid coupler at 45 GHz was used to generate I and Q phases of the LO. Electromagnetic (EM) simulations indicate a gain-mismatch of less than 0.8 dB and quadrature phase error of less than 2.5° between 42 and 49 GHz. The I/Q LO signals are converted to differential signals with on-chip passive baluns. The primary has one turn on a thick (4 µm) metal layer. The secondary has two turns to provide the proper impedance transformation. EM simulations indicate about 0.1 dB magnitude error and 1° phase error. The Wilkinson combiner provides isolation between I and Q ports but adds an additional loss of 0.5 dB at 45 GHz. To enable the low power operation, the entire system is designed to operate at 1 V supply.

3.3.2 Measurements

The I/Q modulator chip is fabricated in a 0.12 µm SiGe BiCMOS process and occupies an area of 1.5mm².

The DAC output signals are provided to pads for external testing. An Agilent 1134A high-impedance probe is used to probe the DAC output differentially with the Agilent DSO 80604B real-time oscilloscope. The serial interface to the DAC is provided using the Agilent 81134A pulse generator and is controlled with a PC to supply data patterns. For static measurements, a slow (t_step = 1 µs) digital ramp signal is applied to DAC. For dynamic measurements, the data patterns corresponding to single tone and two tone tests are generated using MATLAB and loaded into the pulse generator.

Each DAC occupies an area of 0.025mm² and consumes just 0.55mW from the 1 V supply. The measured DNL error is within one LSB. Therefore, the DAC is considered monotonic. The best fit INL is 0.6 LSB over the eight bit resolution. Moreover, INL profile suggests a second order non-linearity.

The DAC SFDR is tested under a two tone test to demonstrate the IM3
characteristics in Fig. 3.5. Both tones have an amplitude of -6 dBFS and are located at 800 kHz and 1 MHz. While the IM3 tones are under -55 dBFS, second order intermodulation products tend to dominate due to the second order non-linearity present in the DAC INL profile. Finally, the DAC SFDR begins to roll-off at around 1 MHz and is -44 dBFS at 10 MHz.

On-chip measurement of the return loss is performed with the Agilent E8361A 67GHz network analyzer. SOLT calibration is done on a CS-5 substrate to move the reference plane to probe tips. RF return loss is better than 10 dB between 39 GHz and 44 GHz and LO return loss is better than 10 dB beyond 40 GHz.

The total transmitted output power is measured with the Agilent E4419B power meter and N8487A power sensor. The through-port of Agilent 87301C coupler is connected to power sensor while the coupled port (-10 dB) is connected to the Agilent E4448A spectrum analyzer to view the output RF spectrum. The

**Figure 3.5:** DAC two tone spectrum at $f_{\text{sig}1} = 800k\text{Hz}$, $f_{\text{sig}2} = 1\text{MHz}$ and $f_{\text{sample}} = 60\text{MHz}$.
E8257D PSG signal generator is used to generate LO power as high as 10 dBm. The cable loss is 7.4 dB, through-port of the coupler attenuates by 1.3 dB and coupled-port has an additional attenuation of 1.8 dB. Also, the RF GSG probe has 1 dB attenuation. These losses are de-embedded from the large-signal results.

To measure the total output power, the I/Q modulator was driven with 1 MHz full-scale sine wave at both I and Q inputs. The maximum transmit power is achieved at a 39 GHz center frequency. For an LO power of 6 dBm, the total output RF power is -9.3 dBm or -12.3 dBm per fundamental tone as shown in Fig. 3.6. For an IF power of -2 dBm at the input of mixer and a loss of 0.5 dB from combiner, the output power of -9.3 dBm translates to a mixer conversion loss of about 6.9 dB. The third-order distortion tones are at -38 dB with respect to fundamental tones. From Fig. 3.6, the LO leakage at the RF port is -31 dBm and results in 37 dB of LO-to-RF isolation.

![Image](image.png)  
**Figure 3.6**: RF output spectrum ($f_{\text{center}} = 39\,\text{GHz}$, $f_{\text{baseband}} = 1\,\text{MHz}$).

The spectrum analyzer measures modulation characteristics to a maximum symbol rate of 10 MS/s with a residual error-vector-magnitude (EVM) of 1.7%. However, the implemented I/Q modulator supports symbol rates in excess of 60
MS/s (or 240 Mbps for 16-QAM) using on-chip DACs. The measured constellation and eye diagrams for QPSK and 16QAM are 2.45% and 3.95% at 1 MS/s when de-embedded from the residual EVM. As shown in Fig. 3.7, the EVM for QPSK and 16QAM starts to become the same beyond the symbol rate of 3 MS/s due to instrument limitation. Therefore, EVM measurements only until 3 MS/s are considered reliable. At 3 MS/s, the transmitter achieves an EVM of 3.6% for QPSK and 5.2% for 16QAM.

![Figure 3.7: EVM vs. symbol rate.](image)

This I/Q modulator is compared against other millimeter-wave I/Q modulators in Table 3.1. The table indicates that the I/Q modulator achieves excellent EVM and linearity performance while consuming a fraction of the power consumption from a low-supply voltage. Previously published work has not incorporated the baseband circuitry on-chip. Also, a reflection-type architecture is used in [15] which will result in side-lobes in the modulated signal, thus degrading ACPR (Adjacent channel power ratio). The proposed modulator demonstrates the first integration of baseband circuitry and mmWave components on-chip at
Q-band. Various transmitter errors like I/Q imbalances, LO leakage and side-lobe suppression can be digitally corrected with the use of on-chip DACs.

Table 3.1: Low Power I/Q Modulator Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>This Work</th>
<th>[15]</th>
<th>[18]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.12µm SiGe BiCMOS</td>
<td>0.13µm RF CMOS</td>
<td>SiGe</td>
</tr>
<tr>
<td>Frequency</td>
<td>39 GHz - 44 GHz</td>
<td>20 - 40 GHz</td>
<td>77 GHz</td>
</tr>
<tr>
<td>On-chip DACs</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>EVM</td>
<td>2.45% @ 2 Mbps (QPSK)</td>
<td>3% @ 54Mb/s</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>5.2% @ 12 Mbps (16-QAM)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1 V</td>
<td>–</td>
<td>5.5 V</td>
</tr>
<tr>
<td>Transmit Power</td>
<td>-9.5 dBm</td>
<td>-5 dBm</td>
<td>-11 dBm</td>
</tr>
<tr>
<td>LO-to-RF Isolation</td>
<td>37 dB</td>
<td>40 dB</td>
<td>23 dB</td>
</tr>
<tr>
<td>Required LO Power</td>
<td>6 dBm</td>
<td>10 dBm</td>
<td>7 dBm</td>
</tr>
<tr>
<td>Third-order Distortion</td>
<td>-38 dBc</td>
<td>-30 dBc</td>
<td>–</td>
</tr>
<tr>
<td>Total Power Consumption</td>
<td>9.1 mW</td>
<td>–</td>
<td>495 mW</td>
</tr>
</tbody>
</table>

3.4 Linearity Considerations for Low-EVM

This section presents a comprehensive analysis of the circuit non-idealities and mismatch contributions to the EVM. The EVM is calculated from the derived equations for various cases. The EVM dependance on the $M$-ary QAM modulation formats is also discussed.

various circuit non-idealities, such as amplitude non-linearity, in-band noise, LO or carrier phase noise, IQ gain and phase imbalances and LO leakage, degrade
the EVM. While prior work has discussed some of these individual contributions to EVM, this analysis seeks to describe the impact of nonlinearity before and after the upconversion and how these sources of nonlinearity interact to impact EVM.

As shown in Fig. 3.8, the direct conversion I/Q modulator is decomposed into a series of dominant sources of non-ideality and mismatch that impact EVM. The I/Q signal path is represented as a third-order polynomial given by $a_1v + a_3v^3$ where $a_1$ and $a_3$ are the first-order (linear) and third-order coefficients respectively and $v$ is the input I or Q voltage. Parameters $\alpha$ and $\theta$ denote the I/Q gain and phase mismatches in Fig. 3.8. Since LO leakage or carrier feed-through appears as the DC offset in the envelope after down-conversion, it is modeled as an additive d.c. voltage in I/Q path. The multiplicative term $e^{j\psi_{\text{rms}}}$ represents the LO phase noise. Finally, $b_1$, $b_3$ denote the PA AM-AM non-linearity and $\Phi(|v|)$ denotes the PA AM-PM non-linearity. A thorough analysis and discussion on how each of these issues affect the EVM is presented in the following sections.

![Figure 3.8: Transmit system model with various circuit errors.](image-url)

### 3.4.1 EVM Definition

The block diagram of a direct conversion I/Q modulator is shown in Fig. 3.8. Baseband I and Q signals, $v_I(kT)$ and $v_Q(kT)$, are generally independent inputs corresponding to a particular input symbol of a complex constellation generated at discrete time intervals of symbol rate $T$. While the constellation can be arbitrarily constructed with $M$ symbols assigned arbitrary probabilities, this work
assumes that a rectangular $M$-QAM constellation is sampled and each I and Q signal takes one of $2^{\frac{1}{2}} \log_2 M$ values with equal probability. For 64-QAM, $v_I(kT)$ and $v_Q(kT)$ independently take one of eight different values, e.g. -7,-5,-3,-1,1,3,5,7.

The ideal RF envelope should be a linear scaling $G$ of the transmitted envelope;

$$v_{\text{ref}}(kT) = G \cdot (v_I(kT) + jv_Q(kT)).$$ (3.1)

When non-linearity and mismatch is present in the signal path, the transmitted envelope is distorted relative to the ideal reference constellation. The EVM is deduced from an ideal receiver based on the best estimate of the constellation from an apriori knowledge of the constellation characteristics. At this receiver, the reference envelope, $v_{\text{ref}}(kT)$, is calculated to normalize the power of the transmitted envelope $v_{\text{env}}(kT)$, i.e. $E[|v_{\text{ref}}(kT)|^2] = E[|v_{\text{env}}(kT)|^2]$, where $E[]$ is the expectation operator. Therefore, the EVM is defined as

$$EVM = \sqrt{\frac{E[|v_{\text{env}}(kT) - v_{\text{ref}}(kT)|^2]}{E[|v_{\text{ref}}(kT)|^2]}}.$$ (3.2)

In subsequent discussions, the impact of each source of non-linearity and error is used to calculate the impact on EVM. For brevity, the discrete-time notation for the envelope and reference are removed.

### 3.4.2 Linearity of the I/Q Signal Path

Assuming I/Q baseband circuit blocks are differential, a weakly nonlinear model includes only third-order non-linearity. Since the I and Q signal paths are identical, the envelope of the RF carrier is expressed as

$$v_{\text{env}} = a_1(v_I + jv_Q) + a_3(v_I^3 + jv_Q^3),$$ (3.3)

where $a_1$ and $a_3$ represent the linear and third-order non-linearity of the I/Q channel gain. Therefore, the scaling factor for the reference constellation is determined from the nonlinear coefficients;

$$G = \sqrt{a_1^2 + 2a_1a_3g_1 + a_3^2g_2}$$

where $g_x = \frac{E[|v_I^{x+2}|]}{E[|v_I^2|]}$. (3.4)
The gain scaling factor $G$ is equal to $a_1$ when no nonlinearity is present in the signal path ($a_3 = 0$). Note that since the nonlinearity is often compressive, $a_3 < 0$ and the scaling factor is less than one. The scaling factor not only depends on features of the signal path but also the construction of the constellation. The factors $g_1$ and $g_2$ estimate the deviation in power between symbol values. In eqn. (3.4), the I signal is used to deduce $g_x$ but the Q signal could also be applied. Since the statistics of the symbols transmitted on both channels are identical, the result for $g_1$ and $g_2$ based on the Q signal is the same.

From eqn. (3.1) and (3.2), the EVM due to non-linear compression of the I/Q signal path is

$$EVM_{IQ} = \frac{1}{G} \sqrt{(a_1 - G)^2 + 2 (a_1 - G) g_1 a_3 + g_2 a_3^2}. \quad (3.5)$$

Several features of this expression are relevant. Again when no nonlinearity is present in either signal path, the EVM is zero as expected. Alternatively, when the power of every symbol in the constellation is the same, for example QPSK, $g_1$ and $g_2$ are identically one and $EVM_{IQ} = 0$. Therefore, I/Q channel non-linearity will not degrade the EVM of QPSK since each path only sees two symbol levels and any amount of compression will not change the relative spacing between the symbols in constellation. If compression in I and Q channels is not identical, this manifests as an I/Q gain and phase imbalance in the constellation for QPSK resulting in EVM degradation.

### 3.4.3 Power Amplifier AM-AM Compression

PA AM-AM compression is conventionally the dominant form of nonlinearity in the transmitter. This compression is distinct from the compression calculated in the Section 3.4.2. While I/Q channel non-linearity compresses the I and Q signals independently, PA AM-AM compresses the magnitude of the vector sum of the I and Q signals. The difference is distinguished in Fig. 3.9 where a fixed amount of nonlinearity is described in each example constellation. At the PA input, the magnitude and phase of each symbol is $M = a_1 \sqrt{v_I^2 + v_Q^2}$ and $\phi = \tan^{-1} \left( \frac{v_Q}{v_I} \right)$. For PA compression, the RF and reference envelopes are expressed as
\[ v_{PA} = (b_1 M + b_3 M^3) \exp(j(\phi + \Phi)) \] (3.6)

\[ v_{ref} = H \cdot M \exp(j\phi) \] (3.7)

where \( b_1 \) and \( b_3 \) are the power series coefficients describing PA gain compression and \( \Phi \) is the factor for AM-PM compression that will be discussed in the following section. The scaling factor \( H \) is similar to the factor introduced for I/Q compression \( (G) \) to match the reference constellation to the transmitted envelope power. This factor is calculated in the same manner:

![Diagram](image)

**Figure 3.9**: 64-QAM constellation under IQ channel and PA non-linearity for the same \( P_{out} \) and \( P_{1dB} \).

\[ H = \sqrt{b_1^2 + 2b_1b_3h_1 + b_3^2h_2} \]

where \( h_x = \frac{E[M^{2x+2}]}{E[M^2]} \).

(3.8)

The EVM resulting from AM-AM compression is similar to eqn. (3.5):

\[ EVM_{AM-AM} = \frac{1}{H} \sqrt{(b_1 - H)^2 + 2(b_1 - H)b_3h_1 + b_3^2h_2}. \] (3.9)

To compare the effect of nonlinearity in the transmitter in the I/Q circuit blocks and in the PA, the EVM is plotted in Fig. 3.10 in terms of the margin between the average power of the signal and the 1-dB compression point of the circuit.
The 1-dB compression based on the weakly non-linear model of the circuit is given by
\[ V_{1dB} = \sqrt{0.11 \frac{404}{3a^3}}. \]
At a given margin between the 1-dB compression and average signal power, the EVM is higher for the I/Q nonlinearity than for AM-AM compression. Typically, the I/Q blocks are operated away from compression to avoid any contribution of the I/Q compression to EVM. However, PAs operated close to their compression point operate at higher overall system power efficiency. Therefore, in practice, the linearity margins are not necessarily the same for PA and I/Q path.

Figure 3.10: EVM degradation due to IQ and PA AM-AM non-linearity for the same \( P_{out} \) and \( P_{1dB} \).

### 3.4.4 Power Amplifier AM-PM Conversion

The PA exhibits a phase shift depending upon the input amplitude which distorts the constellation. To evaluate the impact of this type of non-linearity on EVM, a phase relationship similar to the one mentioned in [42] is assumed;
\[ \Phi = c_2 M^2 - c_4 M^4 \quad (3.10) \]

where \( c_2 \) and \( c_4 \) are the power series coefficients of the AM-PM conversion. Based on this behavior, the EVM is

\[ EVM_{AM-PM} = \sqrt{c_2^2 h_2 + c_4^2 h_4 - 2c_2 c_4 h_3}, \quad (3.11) \]

where the factor \( h_x \) is determined in eqn. (3.8).

In Fig. 3.11, EVM due to AM-PM non-linearity is plotted for \( c_2 = 0.1 \) and \( c_4 = 0.075 \). The corresponding impact on a 64-QAM constellation is shown in the inset where the symbols with higher magnitudes are rotated more than the inner symbols. To characterize the AM-PM response, the maximum phase deviation \( \Phi_{max} \) over the output power range is considered. When the I and Q paths are normalized to unity, the maximum phase shift is calculated from eqn. (3.10). For example, \( \Phi_{max} = 0.1 (\sqrt{2})^2 - 0.075 (\sqrt{2})^4 = -5.7^\circ \). Different values of \( c_2 \) and \( c_4 \) could result in a different maximum phase deviation. The EVM degradation corresponding to the maximum phase deviation of the signal path is plotted in Fig. 3.11.

### 3.4.5 Correlation between AM-AM and AM-PM Compression in I/Q Upconverter and PA

Since transmission of symbols at peak power levels implies that high signal levels are seen in both the I/Q channels as well as in the PA, it is reasonable to assume that correlation exists between the AM-AM behavior in the I/Q signal path and the AM-AM and AM-PM behavior in the PA. To account for this correlation, we introduce the factors \( \gamma_{IQ,AM-AM} \) and \( \gamma_{IQ,AM-PM} \):

\[ \gamma_{IQ,AM-AM} = \frac{EVM_{IQ+AM-AM}^2 - EVM_{IQ-AM}^2}{EVM_{IQ}EVM_{AM-AM}}, \quad (3.12a) \]

\[ \gamma_{IQ,AM-PM} = \frac{EVM_{IQ+AM-PM}^2 - EVM_{IQ-AM-PM}^2}{EVM_{IQ}EVM_{AM-PM}}. \quad (3.12b) \]
The exact value of this factor depends on signal characteristics as well as the signal path nonlinearity and succinct algebraic expressions are difficult to derive. Here, estimation of this factor is reached from numerical techniques. The EVM is estimated when both types of non-linearity are present and when one or the other is present exclusively. The difference indicates a correlation between the two factors that is used to proportionally represent the weight of the I/Q and PA nonlinearity.

Contours in Fig. 3.12 show $\gamma_{IQ,AM-AM}$ and $\gamma_{IQ,AM-PM}$ based on the linearity margins in the I/Q and PA signal paths and phase compression in the PA. While $\gamma_{IQ,AM-AM}$ and $\gamma_{IQ,AM-PM}$ do not depend on specific implementation of the I/Q path, they do depend on the linearity margins. The factor $\gamma_{IQ,AM-AM}$ is positive when both the I/Q and PA are compressive in behavior suggesting that these sources of linearity compound to make the overall EVM worse. On the other hand, $\gamma_{IQ,AM-PM}$ is negative since the I/Q compression mitigates the impact of
AM-PM non-linearity on the overall EVM.

3.4.6 I/Q Imbalance

For small gain and phase imbalances, the linear component of the envelope described in eqn. (3.3) is

\[ v_{out} = a_1 (1 + \frac{\alpha}{2}) e^{j\theta/2}v_I + ja_1 (1 - \frac{\alpha}{2}) e^{-j\theta/2}v_Q, \]

where \( \alpha \) is the gain error and \( \theta \) is the phase imbalance. The EVM due to the I/Q imbalance is

\[ EVM_{\Delta IQ} = \sqrt{\left( \frac{\alpha}{2} \right)^2 + \left( \frac{\theta}{2} \right)^2}. \]

For the remainder of this treatment, we will assume that I/Q imbalance is small and independent of the I/Q nonlinearity. The EVM contribution due to the I/Q imbalance and the I/Q compression is treated as two separate independent sources of error. For large mismatch and high-compression, this might not be completely accurate but is a reasonable assumption for low EVMs.

3.4.7 LO Phase Noise

If the LO signal has an \( \text{rms} \) phase noise of \( \psi_{\text{rms}} \) radians, the EVM contribution is approximately [9]

\[ EVM_{LO} = \psi_{\text{rms}}. \]

If the \( \text{rms} \) phase noise is \( 1^\circ \), the EVM will be 1.74%.

3.4.8 LO Leakage

For direct conversion modulators, DC offsets present in the I and Q channels cause the LO signal to leak to the RF output and contribute LO power to the RF output for direct upconversion transmitters. From [9], the EVM degradation due to LO leakage is
Figure 3.12: Contour plots for the EVM co-dependence between non-linearity in the I/Q and PA signal paths for 64-QAM.
\[ EVM_{\text{Leak}} = \sqrt{\frac{P_{\text{LO, leak}}}{P_{\text{avg}}}}. \] (3.16)

If the carrier power is 20 dB below the average signal power, the EVM will be 10%. LO leakage is particularly significant for direct conversion receivers since the LO contributes to a d.c. offset in the received constellation.

**Figure 3.13:** Effect of I/Q gain and phase imbalance, LO leakage, and LO phase noise on 64-QAM constellation.

### 3.4.9 Overall EVM

The EVM contributions due to each of the discussed sources of circuit non-ideality are now tallied. The overall EVM is
\[
EVM_{\text{net}}^2 = EVM_{IQ}^2 + EVM_{AM-AM}^2 + EVM_{AM-PM}^2 \\
+ EVM_{\Delta IQ}^2 + EVM_{LO}^2 + EVM_{\text{Leak}}^2 \\
+ \gamma_{IQ,AM-AM} EVM_{IQ} EVM_{AM-AM} \\
+ \gamma_{IQ,AM-PM} EVM_{IQ} EVM_{AM-PM}.
\]

(3.17)

This net EVM incorporates several assumptions that should be investigated for a particular implementation. All sources of EVM are discussed as independent statistical processes, which allows I/Q imbalances, LO leakage and LO phase noise to be summed as squares and added to the non-linear effects. The EVM contributions due to PA AM-AM and PA AM-PM are independent in this case since our model of these nonlinearities assumed that the AM-AM compression resulted from odd-order polynomial terms while the AM-PM compression resulted from even-order polynomial terms. However, I/Q imbalances and LO leakage do in fact exhibit very weak correlation to non-linearities. For instance, for \( P_{1dB,PA} - P_{out} < 10dB \) and phase imbalance \( \theta < 5^o \), the magnitude of \( \gamma \)-factor is under 0.2. For simplicity, we ignore these other sources of EVM correlation.

3.4.10 Selection of Constellation for a Given Nonlinearity

Increasing the number of symbols in the constellation improves the spectral efficiency of the channel, however, the EVM increases to a point that communication is no longer reliable. The various sources of EVM described in previous sections dictate the best choice of QAM modulation.

EVM degradation caused by I/Q gain and phase imbalances, LO leakage and LO phase noise is the same for any QAM modulation scheme since these issues do not depend on the order of the constellation. However, non-linearity in the transmitter, e.g. I/Q channel, PA AM-AM and PA AM-PM depend on the modulation scheme. Based on the previous analysis, the EVM is plotted for \( M \)-ary QAM at the same average output power in Fig. 3.14 when \( P_{1dB,PA} - P_{out} = 6dB \) for I/Q and PA AM-AM non-linearity and \( c_2 = 0.05; c_4 = 0.0375 \) for PA AM-PM non-linearity which gives \( \Phi_{max}(M_{max} = \sqrt{2}) = 2.87^o \) at 64-QAM from eqn. (3.10).

From Fig. 3.14, we observe that the sensitivity of the transmitter to I/Q
channel non-linearity, PA AM-AM and PA AM-PM non-linearity increases as \( M \) increases. For QPSK (4-QAM), the EVM contribution of I/Q and PA AM-AM non-linearity is zero. Any identical compression in I/Q path or compression after I/Q combining only scales the constellation for QPSK. There is a slight decrease in EVM due to PA AM-PM at 16-QAM. This is due to the reduced \( \Phi_{\max} \) for 16-QAM at the same average output power. However, as mentioned in Section 3.4.4, different phase characteristics could result in different behavior. For 16-QAM and higher schemes, IQ and PA AM-AM non-linearity do not degrade the EVM significantly. Note that the \( P_{1dB} - P_{out} \) will be less than 6 dB for the combined system. Combined EVM saturates at 2.9% for the conditions described in this section.

\[
\text{Figure 3.14: Comparison of EVM for different modulation schemes under different types of non-linearities.}
\]
3.5 Second Generation Design - Modulator Architecture and Design

The implemented millimeter-wave IQ modulator is intended to support low EVM for high-order constellations (64-QAM). Since the digital pre-distortion (DPD) is mainly used to compensate for the PA non-linearity, the I/Q modulator part of the transmitter should be designed for very low EVM. An “error-less” modulator has a very low bit-error rate ($1 \times 10^{-15}$) and suggests that the EVM must be under 2.5% [43].

An EVM budget is constructed to suggest acceptable contributions due to various errors in the I/Q signal paths in Table 3.2. The analysis and modeling presented in Section 3.4 is used to determine the contribution of each modulator circuit block. For this work, modulator output $P_{1dB}$ is targeted to be 0 dBm. From Table 3.2, this translates to -6 dBm of typical $P_{out}$ for the modulator. Therefore, each of the I and Q channels should have $P_{1dB} = -3$ dBm and $P_{out} = -9$ dBm.

Table 3.2: EVM budget

<table>
<thead>
<tr>
<th>Error Source</th>
<th>EVM Contribution (%)</th>
<th>Constraint/Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>IQ Channel</td>
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<td></td>
</tr>
<tr>
<td>Non-linearity</td>
<td>1.5</td>
<td>$P_{1dB} - P_{out} = 6dB$ (Fig. 3.10)</td>
</tr>
<tr>
<td>IQ Gain Error</td>
<td>2% (0.2 dB) gain error (Eqn. (3.14))</td>
<td></td>
</tr>
<tr>
<td>IQ Phase Imbalance</td>
<td>1.1 deg phase imbalance (Eqn. (3.14))</td>
<td></td>
</tr>
<tr>
<td>LO Leakage</td>
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<td>-40 dBc LO leakage (Eqn. (3.16))</td>
</tr>
<tr>
<td>LO Phase Noise</td>
<td>0.6 deg rms LO phase noise (Eqn. (3.15))</td>
<td></td>
</tr>
<tr>
<td>Net EVM</td>
<td>2.5</td>
<td></td>
</tr>
</tbody>
</table>
For the I/Q channel, the overall 1-dB compression point is composed of a composite linearity for the baseband circuit, e.g. the DAC and filter, and the mixer and is derived with a standard analysis for cascaded systems [36]. The voltage compression of each channel is calculated as

\[ V^{-2}_{1dB,I} = G^{-2}_{mix}V^{-2}_{1dB, BB} + V^{-2}_{1dB,mix} \] (3.18)

where \( G_{mix} \) is the mixer conversion gain in V/V. Preliminary simulations reveal that an equal allocation of d.c. current between the baseband and mixer circuits is a good compromise between linearity and signal swing. Therefore, from a net power budget of 100 mW (or 50 mW per I/Q path), 25 mW is assigned to the mixer. The mixer exhibits \( G_{mix} = 0.316 \) V/V (−10dB) and \( V_{1dB,mix} = 280mV \) \( (P_{1dB,mix} = -1dBm) \) for 25 mW of assigned power budget. From eqn. (3.18), the \( V_{1dB,BB} \) should be approximately 1.12V and \( V_{out,BB} \) should be 0.355V to get -9 dBm output power after upconversion.

The third-order harmonic distortion (\( HD3 \)) is the ratio of the 3rd harmonic tone and the fundamental tone. For a third-order non-linearity\( V_{1dB,BB} \) and \( HD3, BB \) are directly related.

\[ HD_{3, BB} = \frac{1}{4} \left| \frac{a_{3, BB}}{a_{1, BB}} \right| V^2_{out, peak}. \] (3.19)

In other words, \( HD_{3, BB}[dBc] \) can be expressed in terms of \( V_{1dB,BB} \) and \( V_{out,BB} \) as

\[ HD_{3, BB}[dBc] = -28.7 + V_{out, BB}[dB] - V_{1dB, BB}[dB]. \] (3.20)

From eqn. (3.20), the \( HD3, BB \) should be -39 dBc for the desired baseband linearity for \( V_{1dB,BB} \sim 1.12V \) and \( V_{out,BB} \sim 0.355V \).

### 3.5.1 Modulator Circuit Design

The I/Q modulator block diagram is shown in Fig. 3.15. A high-resolution current-steering D/A converter (DAC) is implemented in each of the baseband channels. DAC resolution (bits) decides the DAC SNR and is given by \( SNR (dB) = 6N + 1.76 \), where \( N \) is the DAC resolution in bits. EVM is related to SNR as
\[ EVM_{SNR}(\%) = \frac{1}{10^{SNR(dB)/20}} \times 100 \]  

(3.21)

Although a 7-bit DAC is enough to achieve less than 1% EVM, a 12-bit DAC is implemented to enable precise digital correction of systematic circuit errors like I/Q gain and phase imbalance, canceling LO leakage by introducing d.c. offsets in the transmitter and digital pre-distortion (DPD) to compensate PA compression.

**Figure 3.15:** Block diagram of the implemented IQ modulator.

To handle DPD, the I/Q channel must support a larger bandwidth than the desired signal bandwidth. For example, the DAC sample rate is typically more than a factor of three larger to compensate the compression related to the third-order nonlinearity. However, the higher DAC sample rate offers the advantage of pushing signal aliases appearing at clock harmonics to higher frequency.

The DAC is followed by a third-order active filter to reduce the signal aliases and spurious harmonic content. For a signal BW of 20 MHz, the filter cut-off frequency is chosen to be 60 MHz to enable digital pre-distortion. The use of a high DAC sampling rate equal to 200 MHz along with the filter limits the signal aliases to below -40 dBc, which is well under our ACPR specification (-35 dBc). The filter output is fed to an active double-balanced Gilbert cell mixer. A hybrid coupler along with the passive RF baluns is used to provide the differential
I and Q LO signals to the mixers. Mixer outputs are summed in current domain and converted to a single-ended output using another RF balun.

**D/A Converter**

The DAC circuit diagram is shown in Fig. 3.16. A standard current-steering architecture is adopted to implement the DAC due to its advantage of high-speed operation [39]. Partial segmentation (6 bits) is used to relax the matching requirements on the current sources and to reduce the data-dependent glitches [39, 44]. The DAC current cell is designed to reduce the mismatch and thereby achieve a high SFDR (spur free dynamic range). SFDR is defined as the ratio of the amplitude of the fundamental tone to the amplitude of the highest undesired spur. Since third-order distortion is usually dominant, SFDR becomes equal to the inverse of HD3. DAC SFDR affects the harmonic content of the baseband signal and therefore, the P1dB of the I/Q path. For 12-bit resolution, the standard deviation of the current mismatch for an INL < 0.5 LSB is 0.5% for 70% yield [45]. Monte Carlo simulations for the thin- and thick-oxide PMOS devices available in the 120-nm SiGe BiCMOS process are performed at the same unit current. Thin-oxide devices are used to implement the current cell due to their low area for the same mismatch performance and headroom. A current-cell layout configuration which minimizes linear and second-order process variations in two dimensions is chosen to mitigate the impact of process variations on current source matching [44].

Simulations show that the SFDR due to harmonic distortion of the DAC remains better than 55 dBc up to 20 MHz of the signal bandwidth. As expected, the DAC SFDR rolls-off with higher signal frequency [46]. A high DAC sampling rate of 200 MHz is used to oversample the input. Oversampling enables predistortion and better filtering of the signal copies at dac clock harmonics. Typical DAC full-scale current is 2 mA from 2.5 V supply and can be scaled to 10 mA to increase output power. With a 200 Ω differential load resistance, the full-scale DAC output voltage ranges from 400 mVpp to 2 Vpp with little impact on harmonic distortion. At the low-end of the full-scale current range, the DAC power consumption is 5.5 mW including the digital circuits.
Figure 3.16: A 12-bit partially-segmented D/A converter.

Filter Design

High-order filtering is necessary to eliminate sample clock harmonics and signal aliases. On-chip passive filters provide high linearity and no power consumption but occupy very large area considering the desired signal bandwidth. Therefore, an active gm-C filter is implemented with a third-order roll off (-60 dB/decade) and cut-off frequency at three times the signal bandwidth (60 MHz). Gm cells used with feedback to implement gyrators (or inductor) can be used to implement higher order filters [47]. In section 3.5, at $V_{out,pp} = 0.71V$ (1 dBm baseband power) about -40 dBc of HD3 is enough to achieve target EVM. To avoid significant degradation in the HD3, the filter is designed for less than -50 dBc distortion.
A design methodology similar to [48] is used. Fig. 3.17 shows the schematic of the implemented filter and equivalent passive model. An input gm-cell amplifies and converts the DAC output voltage to current. Output voltage of the filter is supplied to active mixer. The circuit diagram of the individual gm-cell is presented in Fig. 3.18. All the gm-cells used in the filter are identical with the exception of the input gm-cell. PMOS input pair with resistive degeneration is used to boost the linearity. A common-mode feedback circuit sets the desired output dc voltage. High linearity requirement for the filter entails a high power consumption. The filter consumes 38.5 mW power from 2.5V supply.

![Diagram of the filter and equivalent model](image)

**Figure 3.17**: Third-order active gm-C filter.

**Mixer and RF Components**

A double-balanced gilbert cell mixer is used to upconvert the baseband signal to 40-45 GHz (Fig. 3.19). Input pair is implemented using HBTs with resistive degeneration to increase the mixer linearity. HBTs have higher transconductance (gm) than MOS devices for the same bias current. Therefore, to achieve
the same linearity performance, HBT emitter degeneration is more effective than MOS source degeneration at a given power consumption. LO is applied to thin-oxide NMOS switches. Simulations show that NMOS switches when compared to HBT switches require more LO power but provide better linearity. Mixer core consumes 14 mA current from 1.8V (25.2 mW dc power) with simulated $P_{1dB}$ of -1 dBm and conversion loss equal to 10 dB.

Hybrid coupler available in the process model kit is used to generate IQ phases of the LO. Hybrid coupler exhibits low gain and phase imbalances for wide
bandwidth as shown in Fig. 3.20.

![Graph showing simulated magnitude and phase errors between I and Q outputs of the hybrid coupler.]

**Figure 3.20**: Simulated magnitude and phase errors between I and Q outputs of the hybrid coupler.

Single-ended I and Q outputs of the hybrid coupler are converted to differential signals using an RF balun. Careful EM simulations are performed using SONNET EM solver [49] to design RF baluns. Outputs of I and Q mixers are summed in current domain and another output RF balun is connected to get a single-ended modulated RF signal at $Q$-band.

### 3.5.2 Measurements

The I/Q modulator is fabricated in a 120 nm SiGe BiCMOS process. The CMOS devices are used primarily in the baseband signal path and the HBTs are used for the I/Q upconverter. The total chip area is $5mm^2$ and is dominated by the DAC area and I/Q 90 degree hybrid coupler. The chip pad frame supports 400 Mbps digital I/O, d.c. bias voltages and currents and the $Q$-band carrier. The
mixed-signal nature of the circuit requires a hybrid approach to measure the chip. All digital signals and bias voltages are wire-bonded to a standard FR-4 PCB. Since the FR-4 substrate becomes excessively lossy for signals above 10 GHz, the Q-band LO and modulated RF signals are probed using GSG RF probes.

Fig. 3.21 shows the four-layer PCB board and chip-on-board assembly. Controlled-impedance microstrip lines carry the high-speed digital signals. Digital lines are routed to one side of the PCB while the bias voltages are supplied from the opposite side for the ease of connections. Low-profile surface mount components are used to ease the use of RF probes. The chip is epoxied to the PCB and a via-field to the bottom ground plane acts as a heat sink.

While the design power budget was constrained to 100 mW, the power consumption is 138 mW for the implemented I/Q modulator. This is due to an additional gm-cell to interface between the DAC and the filter. Also, the baseband circuits require higher supply voltage (2.5V) compared to mixer (1.8V) to allow for headroom.
Figure 3.21: Chip-on-board assembly of the fabricated modulator chip.
Baseband Measurements

The baseband signal measurements are discussed in this section. The baseband filter frequency response is shown in Fig. 3.22. A reduction in the measured cut-off frequency relative to simulation is observed and results from additional parasitic loading of PCB traces on the filter outputs. The filter roll-off matches the anticipated 3rd-order response.

Baseband signal quality is measured from SFDR (spur-free dynamic range) defined as the ratio of the fundamental signal power to the power of the highest spur. A high-bandwidth Agilent DSO80604B oscilloscope is used with an high-input impedance active probe to monitor the baseband signals. The SFDR is plotted as a function of output voltage in Fig. 3.23. The output voltage swing is varied by scaling the DAC full-scale current. As mentioned in section 3.5.1, DAC SFDR reduces with output frequency.

From our simulation, the DAC SFDR is better than 55 dB up to 20 MHz and the distortion is mainly dominated by the filter. Our measurements indicate that the DAC SFDR showed degraded frequency dependence, thereby reducing SFDR at 20 MHz by 10 dB. The possible reasons for this are the additional capacitances seen by the current sources after layout and the timing skew at the input of current steering switches caused by the layout effects [46]. The filter distortion varies with the voltage swing due to the finite linearity of gm-cells resulting in lower SFDR at higher output voltage. At low frequency, SFDR is limited by the linearity of the filter. At high frequency, SFDR is limited by the DAC. Measurements reveal that the SFDR is better than specification by 5 dB up to target bandwidth of 20 MHz.
Figure 3.22: Filter frequency response.
RF Measurement Set-up and Results

The RF measurement set-up is presented in Fig. 4.13. A Xilinx ML605 evaluation kit with VIRTEX-6 FPGA is used along with a PC to supply various data patterns. Raised-cosine pulse shaping filtering is applied to the digital data using Matlab which greatly reduces the sidelobes and improves the adjacent channel power ratio. Since this is done in digital domain, it does not degrade the linearity of the I/Q path. An Agilent 81134A dual-channel pulse generator supplies synchronized clocks to the FPGA board and the prototype modulator. A high-speed, low pin count FMC connector is used to connect the ML605 data output to the DUT. The Agilent E8257D signal generator provides the LO carrier signal at 40 - 45 GHz with as much as 14 dBm output power. However, the 2.4 mm coax and GSG probe have a total of 6-dB loss at Q-band and limit the maximum available LO power to 8 dBm. An Agilent E4419B power meter along with the N8487A power sensor is used to measure the total RF output power. To view the

![Figure 3.23: SFDR Vs output voltage.](image)
spectrum, a 10-dB Krytar coupler is connected to Agilent E4448A spectrum analyzer. The coupler adds 1-dB loss at Q-band. All external losses are de-embedded from the measurement.

Figure 3.24: RF and modulation measurement set-up.

Figure 3.25: LO and RF port matching.
Fig. 3.25 shows the measured LO and RF port matching characteristics. LO port reflection co-efficient is below -7.5 dB beyond 40 GHz and RF port is well-matched to below -8 dB beyond 37 GHz.

The uncalibrated modulator measurements show high LO leakage (-20 dBc) and low side-band suppression (-15 dBc), which prevents demonstration of high-order modulation formats since sideband suppression reflects high I/Q gain and phase imbalances. Sideband suppression \( SB \) is represented in terms of I/Q magnitude and phase errors as [9]:

\[
SB = 10 \log_{10} \left( \frac{\alpha^2}{4} + \frac{\theta^2}{4} \right)
\]

(3.22)

where \( \alpha \) is the absolute magnitude error and \( \theta \) is the phase imbalance. From Table 3.2, \( \alpha \) and \( \theta \) are specified to be under 2\% and 1 degree to satisfy the EVM and, therefore, the required sideband suppression is 37.5 dB. Lower sideband suppression results from device mismatches, process variations and mistuning of RF baluns, however, these systematic errors are static and can be corrected. A digital correction is performed to compensate for the LO leakage and I/Q imbalances. For instance, the LO leakage is compensated by introducing a d.c. offset between the I and Q path. The I/Q gain and phase imbalances are expressed as [50]:

\[
\begin{bmatrix}
I_{\text{out}} \\
Q_{\text{out}}
\end{bmatrix} = M_{IQ} \begin{bmatrix}
I_{\text{in}} \\
Q_{\text{in}}
\end{bmatrix}
\]

(3.23)

where

\[
M_{IQ} = \begin{bmatrix}
(1 + \frac{\alpha}{2}) \cos(\frac{\theta}{2}) & (1 - \frac{\alpha}{2}) \sin(\frac{\theta}{2}) \\
(1 + \frac{\alpha}{2}) \sin(\frac{\theta}{2}) & (1 - \frac{\alpha}{2}) \cos(\frac{\theta}{2})
\end{bmatrix}
\]

(3.24)

To correct for the errors, the raw I/Q symbols are multiplied by \( M_{IQ}^{-1} \) using digital techniques.

Fig. 3.26 shows the output RF spectrum at a 42 GHz RF and 10 MHz IF frequency when the LO power is 8 dBm and DAC full scale current is 2 mA. Measurements are done at 42 GHz instead of higher frequency due to higher output power at 42 GHz. This is because of slightly degraded RF port matching at higher frequencies and increased losses from on-chip passive components. At this
condition, the output RF power from the modulator is -8 dBm. The I and Q channels are supplied with identical sinusoidal patterns. The LO leakage is below 39 dB. Similarly, sideband suppression is below 39 dBC after digital correction as shown in Fig. 3.27 which indicates that the I/Q imbalance is sufficient to achieve a 1% EVM contribution from Table 3.2.

![Figure 3.26: Measured output RF spectrum at $f_{LO} = 42\, GHz$ and $f_{IF} = 10\, MHz$ before and after LO leakage calibration.](image)

Output $P_{1dB}$ and $P_{IP3}$ are measured by scaling the DAC full scale current. The measured output $P_{1dB}$ is 1 dBm, which is 1 dB lower than the simulation. The $P_{IP3}$ is measured with two tone test. The IF signal with two -6 dBFS tones at $f_{IF1} = 8\, MHz$, $f_{IF2} = 10\, MHz$ is supplied at both I and Q inputs. The power of the desired tones and the IM3 tones is measured and plotted in Fig. 3.28 and demonstrates a measured $P_{IP3}$ of 11 dBm.
(a) Lower sideband suppression.

(b) Upper sideband suppression.

**Figure 3.27**: Measured RF output spectrum with sideband (image) suppressed.
(a) RF output power Vs. DAC full scale current.

(b) Output third-order intercept point.

Figure 3.28: Measured output $P_{1dB}$ and third-order intercept point.
IQ Modulation and EVM Results

As presented in Section 3.5.2, the $P_{1dB}$, I/Q gain and phase imbalances and LO leakage must meet the specification in Table 3.2 to achieve a 2.5% EVM. The LO signal is generated with the Agilent E8257D and has an integrated phase jitter of $0.1^\circ$ rms when integrated from 1 KHz to 1 MHz offset which does not incur a significant impact on EVM.

Fig. 3.29 plots the measured EVM for various modulation schemes with respect to symbol rate for a DAC full scale current of 2 mA corresponding to an output power of -8 dBm. At all rates supported through the signal modulator, the EVM is specified at under 2.5%. Probe contact resistance was found to introduce an uncertainty of around 0.5% EVM and contributes to some of the irregular behavior of measured data points in Fig. 3.29. Predicted EVM is lower than the specified since the LO phase noise is no longer a significant contributor to EVM. Also, EVM is almost independent of symbol rate. EVM measurements could only be done upto symbol rates of 10 MS/s due to the IF bandwidth limitation of Agilent E4448A spectrum analyzer’s digital modulation utility. Nonetheless, the modulator can theoretically achieve the symbol rates in excess of 40 MS/s (240 Mbps with 64-QAM) without significant degradation of EVM beyond 2.5%.
Figure 3.29: Measured EVM vs symbol rate at $P_{out} = -8\, dBm$, and $P_{dB} = 1\, dBm$.

Measured output constellation and eye diagram for various QAM modulation formats are presented in Fig. 3.30 at 8 MS/s symbol rate and -8 dBm RF output power. Eye diagrams for QPSK, 16-QAM and 64-QAM have two, four and eight distinct voltage levels and almost identical I and Q eye opening.

Spectrum of the modulated RF signal with 8 MS/s symbol rate is shown in Fig. 3.31. Raised-cosine filtering with unity roll-off factor is applied to the baseband data to minimize the out of band sidelobes. The ACPR is about -35 dBc and is equal to SNR in this case which implies that ACPR is not limited by the IQ channel non-linearities. Output power is -8 dBm.
(a) QPSK, EVM = 2.2%
(b) 16-QAM, EVM = 2.3%
(c) 64-QAM, EVM = 2.1%

**Figure 3.30:** Measured output constellations and eye diagrams at 8 MS/s symbol rate.

**Figure 3.31:** Modulated RF spectrum at 8 MS/s symbol rate.
Digital Predistortion

To reach high-power levels needed for satellite communication, substantial external power amplification is required. The linearity of the I/Q modulator can be used to introduce digital pre-distortion for external power amplifier compression. In this section, the EVM results presented in the prior section are extended to demonstrate the digital-predistortion with a Spacek Labs 20 dBm power amplifier (SG4510-30-15V) when operated close to its 1dB compression point.

Fig. 3.32 illustrates the output constellation prior to predistortion using a 16-QAM constellation at a 18 dBm output power. Notably, the highest power points in the constellation show maximum deviation from the ideal positions due to a dominant AM-AM compression. The measured EVM is 8.2%.

Estimation of the power compression at the high power points is used to create a compensation scheme for the digital predistortion. The input of the PA is digitally pre-multiplied with the compensation factor

\[
C = \left( 1 - \frac{b_3}{b_1} M(kT)^2 \right).
\]

From eqn. (3.6), the compensated PA output becomes:

\[
v_{PA,comp}(kT) = (b_1 C M(kT) + b_3 C^3 M(kT)^3) e^{j\phi(kT)}
\]

\[
\simeq b_1 M(kT) e^{j\phi(kT)}
\]  

(3.25)

After memoryless digital pre-distortion is applied, the outlier symbols are pushed back towards their ideal locations the EVM improves from 8.2% to 4.9%. Closer inspection of the constellation after pre-distortion reveals that there is some spread in the high power constellation symbols and suggests a possible memory effect in the power amplifier. PA memory effects occur when the output depends on previous inputs. For a random input envelope, a spread in the output voltage is observed which tends to become worse with high output power. Memory effects are often caused by bias circuits, self-heating and trapping effects in transistors [51–53]. This suggests the need for real-time closed loop correction to eliminate the memory effect.

Digital pre-distortion is also performed at 64-QAM under the same conditions as 16-QAM (DAC current, symbol rate and center frequency). The EVM improved from 5.7% to 4.2% for 64-QAM. Note that EVM is lower for 64-QAM..
than 16-QAM since, for the same DAC current, peak power is the same but average power is lower for 64-QAM. This implies that linearity margin ($P_{1dB} - P_{out}$) is higher, hence lower EVM from Fig. 3.10.

**Figure 3.32**: Measured constellations at the output of external power amplifier (16-QAM, 8 MS/s).
Comparison to Prior Work

The implemented millimeter-wave I/Q modulator performance is compared with prior work in I/Q modulators in Table 3.3. The I/Q modulator achieves the lowest EVM at similar data rates to prior demonstrations and initially supports digital pre-distortion for power amplifiers. The lowest LO leakage and highest image suppression at millimeter-wave carrier frequencies is shown.

3.6 Conclusions

A high-linearity I/Q signal modulator is implemented in a 0.12 $\mu$m SiGe process. A new analysis of the impact of signal compression considers how the combination of baseband and RF compression contributes to EVM degradation. The breakdown of EVM suggests a linearity specification for the implemented circuit. The measured I/Q modulator achieves an EVM of less than 2.5% at a 48 Mbps bit rate while performing 64-QAM at 42 GHz. Digital pre-distortion capability is demonstrated by driving an external power amplifier into compression at 18 dBm and the EVM is reduced from 8.2% to 4.9%.

Acknowledgements

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Table 3.3: Second I/Q Modulator - Performance summary and comparison

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<th>[15]</th>
<th>[17]</th>
<th>[18]</th>
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† EVM degradation due to LO leakage not included
Chapter 4

Self-steering I/Q Receiver Array

This chapter describes the proposed technique, circuit concepts and prototype demonstration of a 4-element self-steering I/Q receiver array. The receiver circuit presented in this work is demonstrated with four elements but can be scaled to larger arrays. It operates for an RF input at X-band (8 - 12 GHz) and could be used in conjunction with a millimeter-wave front-end as shown in Fig. 4.1. Section 4.1 illustrates the various concepts used to arrive at the final architecture. The effect of key design parameters on stability of the system is also presented. The design of the prototype 4-element I/Q receiver array is presented in section 4.2. Schematics and simulation results of various building blocks are mentioned. Finally, section 4.3 shows the measurement set-up and results. The array response with 4-element and 3-elements is plotted to demonstrate the self-steering capability. Oscillator array locking bandwidth and wideband spectra are also shown. The array is also measured with different $M$-QAM modulated signals and exhibits stable operation with low error-vector magnitude.
**Figure 4.1**: Self-steering beamformer circuitry for receiver arrays. The receiver forms a beam in the direction of the interrogating signal.

### 4.1 Proposed Concept and Architecture

#### 4.1.1 Receiver Beam-scanning using Coupled-oscillators

The phase dynamics of an oscillator in the presence of an injection signal close to its natural frequency of oscillation can be written as [54,55]

\[ \frac{d\theta}{dt} = \omega_o + \frac{\epsilon \omega_o}{2Q} \sin(\theta_{inj} - \theta) \]  

(4.1)

where \( \omega_o \) and \( Q \) are the natural frequency and quality factor of the oscillator. \( \theta_{inj}, \theta \) are the instantaneous phases of the injection signal and oscillator. \( \epsilon \) is the coupling or injection strength and depends on the coupling network, injected signal power and oscillator swing. The oscillator locks to the injected signal frequency within a certain bandwidth called locking bandwidth, \( \Delta\omega_{lock} \) which is given by \( \Delta\omega_{lock} = \frac{\epsilon \omega_o}{2Q} \). Due to the frequency detuning of the oscillator, there exists a phase difference between the oscillator and injected signal found using 4.1

\[ \Delta\theta = \sin^{-1}\left(\frac{\omega_{inj} - \omega_o}{\Delta\omega_{lock}}\right). \]  

(4.2)

The maximum stable phase difference, \( \Delta\theta \) is equal to \( \pm 90^\circ \) when \( \omega_{inj} = \omega_o \pm \Delta\omega_{lock} \). 

---

\( \Delta\phi = \pi \sin \psi \)
Figure 4.2: Beam-steering using COA and CPLL. (a) By edge-detuning of coupled-oscillators. (b) Auto-steering using both COA and CPLL. (c) Modification of (b) to enable I/Q down-conversion.

The above mentioned property of injection-locked oscillators has been exploited for beam-forming and steering in discrete phased-array transmitters. Liao et. al. [56] showed that a constant phase difference is generated across an array of coupled-oscillators by detuning the outermost oscillators given the same natural frequency of inner oscillators. A limited beam-steering range of \(-15^\circ\) to \(+12.5^\circ\) was measured by manually detuning the outer oscillators with antenna spacing \(d = 0.86\lambda\). An extended steering range of \(-30^\circ\) to \(+40^\circ\) was achieved in a later demonstration using \(d = 0.29\lambda\) [57]. Alexanian et. al. proposed that the steering range of the array can be further increased by using frequency multipliers [26].

Based on above principles, beam-scanning for receivers can be implemented as shown in Fig. 4.2(a). The phase difference between the RF inputs (RF progressive phase shift) for a steering angle of \(\psi_{RF}\) is given by

\[
\Delta \phi = kdsin\psi_{RF} \tag{4.3}
\]

where \(k\) is the phase constant given by \(k = \frac{2\pi}{\lambda}\) and \(d\) is the antenna spacing. For half-wavelength antenna spacing \(\Delta \phi = \pi sin\psi_{RF}\). For coherent combining of down-converted IF signals, coupled-oscillators must be manually detuned within their locking range such that \(M\Delta \theta = \Delta \phi\). The theoretically achievable \(\Delta \phi\) is plotted in Fig. 4.3 for different frequency multipliers. Frequency doublers (\(M = 2\)) are sufficient to achieve \(\Delta \phi = \pm 180^\circ\) covering entire hemisphere with \(\psi_{RF} = \pm 90^\circ\).

Implementing larger arrays using coupled-oscillators would require at least
two control parameters [56, 58, 59]. Moreover, the natural frequencies of the inner oscillators must be identical which is hard to achieve due to circuit mismatches and process variations.

4.1.2 Self-steering using Coupled-phased-locked-loops

Coupled-phased lock loops (CPLL) have been used instead of coupled-oscillator arrays (COA) for beam-steering in past to overcome the small locking bandwidth, phase noise, non-identical unit cells and amplitude fluctuations of COAs [60,61]. However, offset voltages were required in [60] and edge-detuning was required in [61] to steer the beam. Yan et. al. proposed a solution based on both COAs and CPLLs where a limited steering range of $-6.5^\circ$ to $+16^\circ$ was achieved using single control parameter for beam-steering [27]. The goal of this work is to demonstrate larger steering range in a monolithic platform with automatic steering where no control parameter is required.
In this work, both the COA and CPLLs are used to implement self-steering receiver. Fig. 4.2(b) shows an adaptive beam-steering receiver. To lock the coupled-oscillators at a known frequency, an external signal is injected at half the RF frequency. Coupled-phased lock loop detunes the second oscillator such that at the steady-state down-converted IF signals $IF_1$ and $IF_2$ are phase aligned. $\pi/2$ phase shift is required in one of the IF paths since the mixer-type phase detector locks the CPLL at $\pi/2$ input phase difference. The architecture of Fig. 4.2(b) can be modified to Fig. 4.2(c) to insert the $\pi/2$ phase difference in LO path instead of IF path. This enables the I/Q down-conversion. Now the CPLL is driven by the quadrature and in-phase down-converted IF signals of neighboring receive elements.

The architecture of Fig. 4.2(c) is modular and can be extended to larger arrays. Fig. 4.4 shows the implemented 4-element adaptive beam-steering I/Q receiver. In the presence of both COA and CPLLs, the phase dynamics of oscillators can be written as a set of non-linear differential equations shown in eqn.
(4.4) [27,56]. For (4.4), \( i = 2, 3, \omega_o \) and \( Q \) are the oscillator free-running frequency and quality factor, \( K_{vco} \) is the oscillator tuning coefficient, \( K_{pd} \) is the phase detector gain, and \( f(t) \) is the impulse response of the loop filter (integrator). \( f(t) = \frac{2m}{C} u(t) \) for the gm-C integrator used as loop-filter for this work where \( u(t) \) is the unit step function. All oscillators are assumed to have the same amplitude and quality factor. Under steady-state locked conditions

\[
\frac{d\theta_1}{dt} = \frac{d\theta_{i=2,3}}{dt} = \frac{d\theta_4}{dt} = \frac{d\theta_{inj}}{dt} = \omega_{inj} - \frac{\Delta\phi}{2}
\]

(4.5)

where \( \Delta\theta \) and \( \Delta\phi \) are the phase differences between neighbor oscillators and input RF signals. A stable phase difference of \( \pm 90^\circ \) between oscillators results in \( \pm 180^\circ \) RF phase shift, hence enabling auto-steering angle of \( \psi_{RF} = \pm 90^\circ \) covering the entire visible region.

### 4.1.3 Stability Analysis

An approach similar to [27] is adopted for stability analysis of the system. The phase equations from (4.4) are linearized around their steady state solution given by (4.5). For small perturbation around the steady-state oscillator phases, the stability matrix for the 4-element receiver is shown in eqn. (4.6).

\[
S = \begin{bmatrix}
-K_0 & K_1 & 0 & 0 & 0 & 0 \\
K_0 & -2K_1 & 1 & K_2 & 0 & 0 \\
0 & M_1 & 0 & 0 & 0 & 0 \\
0 & K_1 & 0 & -2K_2 & 1 & K_3 \\
0 & -M_1 & 0 & M_2 & 0 & 0 \\
0 & 0 & 0 & K_2 & 0 & -2K_3 \\
0 & 0 & 0 & -M_2 & 0 & M_3 \\
\end{bmatrix}
\]

(4.6)

Here \( K_i = C_1 \cos \Delta\theta_i \) and \( M_i = C_2 \sin(2\Delta\theta_i - \Delta\phi_i + 90^\circ) \) while \( C_1 = \frac{c\omega_o}{2Q} \) and \( C_2 = -4K_{vco}K_{pd} \frac{\omega_o}{C} \). \( \Delta\theta_i = \theta_{i-1} - \theta_i \) is the steady-state phase difference between neighbor oscillators while \( \Delta\phi_i = \phi_{i-1} - \phi_i \) is the phase difference between RF inputs. For linear antenna array, \( \Delta\phi_1 = \Delta\phi_2 = \Delta\phi_3 = \Delta\phi \) where \( \Delta\phi \) is
given by eqn. (4.3). For stable operation, the eigenvalues of stability matrix must have negative real parts [62]. It can be shown that only the condition that $\Delta \theta_1 = \Delta \theta_2 = \Delta \theta_3 = \Delta \phi/2$ meets the stability criteria. However, the stable RF progressive phase difference depends on the value of design parameters $C_1$ and $C_2$. As mentioned in section (4.2), for this design $\epsilon = 0.1 - 0.5$, $\omega_o = 5GHz$, $Q = 13$, $K_{vco} = 1.6GHz/V$, $Kpd = 1$, $g_m = 65\mu A/V$ and $C = 5nF$.

Stability Dependence on Coupling Strength, $\epsilon$

Fig. (4.5(a)) plots the stable range of RF progressive phase difference, $\Delta \phi$ with respect to coupling parameter, $\epsilon$ for 2-, 3- and, 4-element array. Increasing $\epsilon$ increases the oscillator locking bandwidth allowing more detuning of oscillators, hence higher stable phase range. If there is no coupling present i.e. $\epsilon = 0$, the array is unstable and stable range of $\Delta \phi = 0$. This conclusion can also arrived at by observing that CPLL transfer function has two poles at dc (integrator and oscillator) and is inherently unstable. Therefore, a certain amount of coupling is required to make the system stable. Also from Fig. (4.5(a)), at a given value of coupling strength, stability degrades with larger arrays [58].
Stability Dependence on Loop-filter Capacitor

For the fixed values of $K_{vco}$, $K_{pd}$ and $g_m$, the CPLL loop bandwidth is inversely proportional to the size of loop filter capacitor. The higher the capacitor size, the smaller the PLL loop bandwidth and $C_2$ in eqn. (4.6). Fig. (4.5(b)) shows the stable RF progressive phase shift with respect to integrator capacitor size at
fixed coupling strength for 2-, 3- and 4-element array. A higher size capacitor yields better stability and therefore larger stable phase range. Also, increasing the size of array results in lower stable phase range, a trend similar to Fig. (4.5(a)).

4.2 Integrated Circuit Implementation

Different circuits blocks of the proposed system are designed in 45 nm SOI CMOS process. A power and area constrained approach is adopted for the design with the total power budget of 150 mW for 4-element receiver array. Minimal use of inductors allows area saving. Block level designs and simulated results are presented in the following sections.

4.2.1 Oscillator Path & Coupling Network

A cross-coupled LC oscillator is designed as shown in Fig. 4.6. PMOS cascode current source is used to improve supply rejection. Typically, Metal-on-metal capacitors are used to achieve high quality factor with discrete tuning steps. However, the analog nature of the loop dynamics requires the use of analog varactors. Therefore, MOS capacitors are used as varactors to tune the oscillator. With improved metalization the MOS capacitor exhibits the quality factor equal to 20. A differential spiral inductor with lowest metal shield is designed and simulated using Sonnet EM Solver [49]. Grounded metal shield reduces the substrate coupling and eddy-current losses. To improve the quality factor, the inductor turns are composed of parallel connection of top three metals available in the process. Any further parallel metalization does not improve the quality factor due to reduced lower metal thickness. The simulated 1nH inductor has a quality factor equal to 13 at 5 GHz center design frequency. A relatively large aspect ratio of cross-coupled pair improves swing at the given power consumption. The simulated tuning range for the stand-alone oscillator is 4.3 GHz to 5.5 GHz. The simulated differential voltage swing is 1.2V with typical 4.5 mW power. An array of four oscillators is coupled through resistive network. An NMOS in triode-region alongwith poly resistors is used to allow the changes in coupling strength.
The oscillator is followed by the frequency doubler shown in Fig. 4.7. The doubling pair is biased in class C to maximize the second harmonic for a given transistor size [63]. Cascode device reduces the effect of miller capacitance and improves input to output isolation. An LC resonant load with 10 GHz resonant frequency is used to filter the higher harmonics at the output of doubler. However, narrow-band nature of LC load causes swing variation with the oscillator tuning. A parallel 200 ohm resistor is used to reduce the quality factor of the LC load to broaden the bandwidth and thereby minimizing the swing variation. The simulated doubler loss is 8 dB with typical 1.0V input swing at 5 GHz input frequency. The power consumption is 4.5 mW.
Figure 4.7: Oscillator path schematic.
Figure 4.8: RF front-end.

An active balun amplifies the 10 GHz doubler output while converting it to differential signal. No matching inductors are used to save the area. The first stage of active balun is resistively loaded NMOS differential pair. A push-pull type second stage is added to overcome the loss of poly-phase filter. The active
Figure 4.9: CPLL blocks.

balun amplifies the signal by 9 dB while consuming 7.5 mW power. A single-stage poly-phase filter is used to generate in-phase and quadrature LO signals. This type of poly-phase filter provides 90° phase difference between the I/Q outputs for all frequencies [64]. However, the magnitude is equal only at single design frequency. Magnitude response can be broadened using multiple stages at the cost of higher loss. This would require further amplification of LO signal increasing power consumption. Inductor-based quadrature all pass filter overcomes some of these limitation but occupies large area due to the use of inductors [65]. Therefore, a single-stage poly-phase filter is used to minimize power consumption and area. The loss is 6 dB due to the capacitive loading provided by the down-converting mixers. The entire LO path consumes 16.5 mW power from 1.5V supply while providing 0.5V peak-to-peak swing at the I and Q outputs.

4.2.2 RF Front-end

The RF front-end is designed at X-band (8 - 12 GHz). An active balun shown in Fig. 4.8 converts the single-ended input RF signal to differential while
amplifying it by 10 dB. Inductive degeneration along with the series inductor provides a 50 ohm match at the input. Addition of gate-source capacitances $C_{1,2}$ reduces the required inductor sizes. A capacitor $C_M$ is connected between the drain of $M_1$ and gate of $M_2$. Addition of this capacitor results in significant reduction of the phase error. However, due to the leakage of signal current through capacitor $C_M$, the magnitude error increases. $C_M = 30fF$ provides a good compromise for this design. A relatively low operating frequency coupled with the low device capacitances in this process allows the resistive load instead of L-match which results in more area-efficient design. The balun has a simulated gain equal to 10 dB, 5 dB noise figure and -9 dBm input-referred 1-dB compression point ($P_{1dB}$). The magnitude and phase errors are within 1 dB and 1 degree across the band of interest (8 - 12 GHz). The power consumption is 4.5 mW.

Two double-balanced Gilbert-cell mixers down-convert the X-band RF signal to an IF frequency of 100 MHz. Gilbert-cell mixers exhibit low loss. Also, due to the high input impedance, the mixer can be directly driven by the active balun output. Low IF frequency is used to reduce the effect of parasitics and routing losses. RC loading at the output helps filtering the up-converted signal at $f_{rf} + f_{lo}$. Mixer has a simulated gain of 1 dB with typical 0.5V LO swing and input $P_{1dB}$ is equal to -2 dBm with 3 mW power consumption.
4.2.3 CPLL Blocks

Fig. 4.9 shows the different building blocks of the coupled-phased locked loop. A low-power double-balanced Gilbert cell mixer provides multiplier-type phase detection. Also, the analog phase detector supports the modulated input signals. The output of such a phase detector is proportional to the cosine of input phase difference. Therefore, at the steady-state the loop locks at 90° phase difference. The gain of the phase-detector is varied by the variable resistance implemented using PMOS in triode region. Phase detector gain is variable from 1V to 8V with 0.3 mW power. Gm-C integrator acts as the loop filter. NMOS differential pair with PMOS current source load is used as the gm-cell. A continuous-time common-mode feedback circuit sets the output common-mode voltage at the integrator output. Off-chip 10 nF capacitors are used to improve the stability of the system. Typical $g_m$ of the gm-cell is 65 $\mu$A/V with 10 $\mu$A tail bias current. An op-amp with resistive feedback acts as the voltage summer and converts the differential integrator output to single-ended. The single-ended op-amp output is
used to detune the individual oscillators. Two-stage RC compensated topology is used for the op-amp with 30 MHz unity-gain bandwidth. The op-amp bandwidth is much higher than the PLL loop bandwidth (~ 500 KHz) to avoid another pole in the loop. Level-shifters (not shown in Fig. 4.9) are used to adjust the dc voltage levels at the interface of integrator and voltage summer. The net power consumption of the loop blocks is 0.9 mW.

4.2.4 IF Combiners and Buffers

As mentioned in section 4.1, at steady-state locked condition, the in-phase and quadrature IF signals are phase aligned and are combined to maximize receiver SNR. Fig. 4.10 shows the IF combiner. IF combiner is implemented using four NMOS differential pairs with shared load and tail current source. A higher 2V supply is used to allow for large swing as a result of combining. The dc power consumption is 4 mW with 3 dB voltage gain and -5 dBm input $P1dB$ per IF input.

Fig. 4.11 shows the schematic of the output buffer used to convert the combined differential IF signal to single-ended while providing a 50Ω output impedance. Transistor $M_1$ is driven by the non-inverted signal and acts as the source follower while transistor $M_2$ is driven by the inverted signal and acts as common-source
amplifier. Source follower $M_1$ ensures good linearity and 50Ω output impedance. Common-source device is resistively degenerated to boost its linearity. The buffer attenuates the combined IF signal by 10 dB while providing a 50Ω output resistance. The input referred $P1dB$ is 10 dBm with 3.8 mW net power consumption.

4.3 Experimental Results

4.3.1 Measurement Scheme and Set-up

Fig. 4.12 shows the microphotograph of fabricated 4-element self-steering I/Q receiver array. The chip area is 3.45 mm² (2.3 mm X 1.5 mm) including the pad frame. As mentioned in section 4.2, for area saving, only four inductors are used per receive path. Individual Rx path occupies 0.36 mm² area including inductors. An isolation wall extending from substrate to the top ground metal is used to reduce
undesired sources of coupling between elements. Chip pad frame includes four RF GSG pads for the X-band RF inputs at the north side and all the DC biases at the east side. To provide a low-inductive and resistive supply path, the $VDD$ pads are arranged on both east and west side. West side also incorporates differential GSSG pads for $5GHz$ injection signal. Combined I/Q IF outputs are available at the south end along with various integrator outputs to connect off-chip loop-filter capacitors. Output of the first oscillator in the on-chip COA is also buffered to the south end for measurements of COA locking bandwidth, oscillator tuning range, wideband spectrum and phase noise. Multiple ground pads in all four directions enable low-net bond-wire inductance to printed-circuit-board ground.

A two conductor layer PCB with Rogers 4003 substrate is designed and fabricated for the chip-on-board assembly. Additional thick standard FR4 substrate with dummy conductor layers is added to provide mechanical stability as shown in the PCB cross-section in Fig. 4.12. Thin 8 mils Rogers 4003 substrate allows low-inductive transitions close to the chip-bonding location. The CMOS chip is glued to the PCB ground using conductive epoxy. Via field below the chip acts as the heat sink. All the signals and biases are wire-bonded with standard 1 mil gold bondwires. RF inputs, LO injection signal, oscillator output and IF signals are routed using grounded coplanar waveguide (GCPW) t-lines shown in inset. A quarter-wave shorted stub at $10GHz$ provides electro-static discharge path at the RF inputs while acting as an open for RF signal. Low-profile surface mount (SMT) capacitors are used for decoupling and loop-filtering while bidirectional diodes protect dc lines from an ESD event. The PCB measures $3\text{ inch} \times 3\text{ inch}$.

Fig. 4.13 shows the set-up used to measure the array response. Agilent E8257D signal generator along with 4-way power splitter is used to generate four RF inputs for the 4-element receiver chip. Mechanical phase shifters are inserted in RF paths to create different progressive phase differences $\Delta\phi$ between RF signals to emulate a beam incident from different steering angles $\psi$. Agilent N5181A signal generator with 180 deg hybrid coupler injects a differential $-3dBm$ LO signal into the COA. Output I/Q signals are plotted in Agilent digital sampling scope. Also, the phase noise, wideband spectrum, tuning range and locking bandwidth are
measured by monitoring the first oscillator output with Agilent E4448A spectrum analyzer.

### 4.3.2 S-parameter Measurements

For s-parameter measurements, Agilent network analyzer along with the E-cal kit is used to calibrate and bring the reference plane to the input of test PCB. Fig. 4.14 shows the measured RF port matching and isolation at X-band. RF ports are numbered according to Fig. 4.12. Reflection co-efficients at all the four RF ports is below -8 dB. Multiple resonance points in reflection coefficient plot are seen due to the long GCPW lines present on the PCB having a characteristic impedance slightly different than 50 ohms. A more accurate geometry of the GCPW lines on PCB could eliminate this effect. Measured RF isolation is more than 25 dB between neighbor RF inputs. Isolation improves for farther located ports as expected.
4.3.3 Oscillator Spectrum & Array Locking Bandwidth

Oscillator array tuning range is measured by varying the dc tuning voltage of the array and adjusting the injection frequency accordingly. The measured tuning range is from 3.68 GHz to 4.72 GHz. To measure the locking bandwidth of the COA, the tuning voltage and injected signal power are kept constant while
the injected frequency is varied. Fig. 4.15 shows the measured locking range of the array and normalized oscillator power for -3 dBm injected signal power and coupling strength $\epsilon \cong 0.5$. The array exhibits $\pm 90\, MHz$ locking bandwidth at 4 GHz center frequency. However, the oscillator power varies across the locking range. Fig. 4.17 shows the measured oscillator phase noise across the array locking range. As expected, the phase noise increases with higher injection frequency. The wideband spectra shown in Fig. 4.16 is spur-free at both low and high end of the lock range.

![Figure 4.15: Measured array locking range and normalized oscillator power for $P_{inj} = -3\, dBm$.](image)

**Figure 4.15**: Measured array locking range and normalized oscillator power for $P_{inj} = -3\, dBm$. 
Figure 4.16: Measured oscillator wideband spectrum across the lock range.
4.3.4 Self-steering Array Response

Ideal and simulated 4-element array factor for a broadside RF signal are shown in Fig. 4.18(a) in absence of any adaptation. This indicates that in absence of the self-steering mechanism (CPLL in this work), the down-converted IF output power depends on the RF incident angle $\psi$ or RF progressive phase $\Delta \phi$. The ideal desired response of the array is to maintain the same output power irrespective of the incident angle. Measured I/Q outputs with CPLL loop enabled are superimposed in Fig. 4.18(a) to show that array self-steers to the direction of the incident beam. This leads to 18 dB power improvement at array factor nulls due to self-steering. The measured stable progressive phase shift, $\Delta \phi$ is $\pm 100^\circ$ which corresponds to $\psi = \pm 35^\circ$.

To measure the response with 3-elements, fourth Rx path is electrically disconnected using laser cut. A much larger stable progressive phase, $\Delta \phi$ equal to $\pm 170^\circ$ (or incident angle $\psi = \pm 70^\circ$) is measured with three elements as shown in

![Phase Noise vs Frequency Offset](image)

**Figure 4.17**: Measured oscillator phase noise across the array locking range.
Fig. 4.18(b). This confirms the theoretical observation made in section 4.1.3 that the system stability improves with fewer Rx elements.

Figure 4.18: Measured self-steering response of the I/Q receiver array with $f_{\text{inj}} = 4GHz$, $P_{\text{inj}} = -3dBm$ and $f_{rf} = 8.1GHz$. 
4.3.5 Modulation Results

Modulated RF signal is generated by upconverting a modulated IF signal using Agilent N5182A vector signal generator and external mixer. The down-converted output IF signals are combined using a wilkinson power combiner and fed as input to the spectrum analyzer. Digital demodulation utility of spectrum analyzer plots the signal constellation & eye diagrams and displays the EVM. Array is measured to be stable with modulated RF input across the full stable phase range measured in section 4.3.4. The EVM is plotted for different modulation schemes and $\Delta \phi$ in Fig. 4.20(a) at 10 MS/s symbol rate and $P_{rf} = -16 \text{ dBm}$ per input. The injected signal frequency and power are 4 GHz and -3 dBm. The input RF carrier is 8.1 GHz giving the output IF frequency as 100 MHz. The measured EVM is roughly constant over different modulation schemes and $\Delta \phi$. The 4-element array achieves less than 4% EVM at 60 Mbps data rate (10 MS/s symbol rate) at 64-QAM.

EVM is also measured with respect to RF input power as shown in Fig. 4.20(b) at 10 MS/s. At low power, the low receiver SNR degrades the EVM while at high power the EVM increases due to compression. EVM degradation is much higher for 16- and 64-QAM in compression regime while QPSK is roughly unaffected [66]. EVM could only be measured upto 10 MS/s symbol rate due to IF BW limitation of digital demodulation utility. The frequency response measurements of the chip show more than 240 MHz 3-dB IF bandwidth. This allows data rates in excess of 1 Gbps with 64-QAM modulation.
Figure 4.19: Measured constellations and eye diagrams for QPSK, 16-QAM and 64-QAM at $P_{RF} = -16$ dBm/channel and $\Delta \phi = \pm 73^\circ$. 
(a) At different RF progressive phase shift, $\Delta \phi$ with $P_{rf} = -16\,dBm$ per element.

(b) With respect to RF input power at $\Delta \phi = -73^\circ$.

**Figure 4.20:** Measured error-vector magnitude for 4-element I/Q receiver array at $f_{rf} = 8.1\,GHz$ and $f_{inj} = 4\,GHz$.

### 4.4 Conclusions

A new technique to perform self-steering for receiver arrays is proposed which uses the combined dynamics of coupled-oscillator array and coupled-phased...
locked loops. A 4-element self-steering I/Q receiver array is demonstrated in 45 nm CMOS SOI process indicating the practicality of implementation of such systems in widely used CMOS processes. The array achieves a stable auto-steering range of ±35° with 4-elements and ±70° with 3-elements. The demonstrated architecture supports RF signals modulated with spectrally-efficient M-QAM schemes for high data rate communication. The measured EVM is less than 4% at 60 Mbps with 64-QAM at $Pr_f = -16dBm$ per element. EVM remains under 6% for 30 dB input dynamic range with 64-QAM and 40 dB dynamic range with QPSK.

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Chapter 5

Conclusions

This dissertation presents the analysis, design and prototype results in the area of millimeter-wave integrated circuits for wireless communication. Firstly, an analytical approach to predict the spur-free dynamic range (SFDR) of two mmWave phased-array receiver architectures is presented. Derived equations and techniques enable the linearity comparison of LO and RF scanned arrays for any given antenna geometry and receive path linearity. Based on the analysis, it is concluded that RF-scanning architecture offers better SFDR for wider jammer incident angles.

Secondly, a new analysis is presented that enables the estimate of linearity requirements in I/Q modulators employing M-QAM schemes like 16- and 64-QAM for high data rate. The analysis separates the I/Q path compression and PA AM-AM and PA AM-PM non-linearities. Closed-form equations are derived to calculate the linearity requirements of the I/Q path and power amplifier to achieve a certain low value of EVM. Using this analysis, a low-EVM Q-band (40-45GHz) direct conversion modulator is designed and fabricated in 120 nm SiGe BiCMOS process. To the best of author’s knowledge, the measured prototype achieves the state-of-the-art performance in terms of error-vector-magnitude (EVM), LO rejection and image suppression. This work also demonstrates the digital pre-distortion of an off-chip power amplifier using on-chip digital-to-analog converters.

Finally, a technique to perform self-steering in the phased-array receivers is proposed. The approach uses the combined dynamics of coupled-oscillator array
and coupled phase-locked loops to self-align the receiver beam in the direction of the incoming rf signal. This type of systems are particularly useful for high directivity point-to-point links and full-duplex retro-directive arrays. A 4-element I/Q receiver array based on this technique is fabricated in 45 nm CMOS SOI. The array achieves a measured stable steering range of +/-35 degrees with 4-elements and +/-70 degrees with 3-elements. Additionally, the self-steering array IC supports modulated RF signals and exhibits less than 4 % EVM at 60 Mbps. To the best of author’s knowledge, this work is the first demonstration of self-steering I/Q receiver array in a monolithic circuit.
Bibliography


