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Thermally Stable Metal/GaAs Contacts

J. Ding
(Ph.D. Thesis)

June 1989

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Thermally Stable Metal/GaAs Contacts

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Ph.D. Dissertation

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June 1989

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THERMALLY STABLE METAL/GaAs CONTACTS

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Ph.D. Thesis

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ABSTRACT

Further improvement of electrical properties and thermal stability of reactively sputtered refractory metal nitride contacts on GaAs and In-based ohmic contacts to GaAs require a systematic study of the relationships between structural and electrical characteristics at the interface.

In this study, the interface morphologies and structures of Nb/GaAs, NbN/GaAs, TiN/GaAs, WN/GaAs and In/GaAs contacts have been investigated before and after annealing at temperatures up to 950 °C by transmission electron microscopy and diffraction, energy dispersive spectrometry of x-rays, x-ray diffractometry and cross-sectional high resolution transmission electron microscopy. The results from these techniques were combined to provide detailed descriptions of the structural evolution of the interface region in refractory metal nitride/GaAs and In/GaAs heterojunctions. Structural details were related to the corresponding electrical characteristics.

For the refractory metal nitride contacts on GaAs, no significant interface reactions occurred even after annealing at temperatures up to 950 °C. However, phase transformation in the thin NbN films and some interdiffusion at the NbN/GaAs interface were found at 850 °C. Outdiffusion of As or Ga and As from the GaAs substrate occurred at 500 °C for the TiN/GaAs contacts and at 900 °C for the WN/GaAs contacts. This outdiffusion resulted in pocket-like protrusions formed beneath the original interface. Improvement of the electrical characteristics of these contacts during annealing was attibuted to changes of the electronic structure at the interface resulting from the removal of sputtering dam-

age and to the loss of As or Ga and As at the interface. In comparison to the nitrides, Nb reacts with GaAs at the interface forming a rough interface at 700 °C.

For the In/GaAs contacts, the results show the existence of a miscibility gap in the InAs-GaAs pseudobinary system with a critical temperature between 575 °C and 650 °C. This suggests that an annealing temperature above 650 °C should be used to form a graded $In_{1-x}Ga_xAs$ layer at the interface for a thermally stable and low resistance ohmic contact.

1. INTRODUCTION

Metallization systems are fundamental components of all semiconductor devices and integrated circuits. They provide the electrical link between the active region of the semiconductor and the external circuit. In the case of an integrated circuit, they also interconnect the circuit elements with great precision providing the necessary conducting paths. The primary consideration in the choice of a metallization system is to ensure that the contact has the desired electrical properties. There are two distinct types of contacts required for solid state devices. They are ohmic (low resistance) and Schottky (rectifying) contacts. The importance of these contacts to semiconductor technology stimulates intensive study with emphasis on morphology, reliability, improvement of electrical characteristics, and understanding of the underlying physics.

Interest in developing high-speed low power field effect transistor devices based on GaAs has been increasing in recent years due to the high electron mobility in GaAs, and the low-power dissipation compared to Si devices with comparable speed. There is only limited information on the reactions between metal films and GaAs, and on the electrical properties of reacted contacts. In addition, ternary phase diagrams and thermodynamic data for most of these systems are not known. Therefore, it is difficult to predict what products will form when metals and GaAs react. This is especially complicated since these reactions can lead to formation of ternary as well as binary compounds. Much attention has recently been attracted to the thermal stability of metal-GaAs contacts, the most crucial problem associated with the fabrication of devices such as metal-semiconductor field-effect transistors. High-temperature interfacial reactions generally involve the interdiffusion of the semiconductor elements into the metal overlayer and/or of the metal elements into the substrate, resulting in the formation of interfacial phases. To develop thermally stable contact systems, fundamental understanding both of the interface reaction mechanisms and the effect of the native oxide on the reaction is essen-

tial.

The purpose of this research is to study some specific metal-semiconductor contacts, and to provide detailed interface morphology and microstructure information for GaAs and several metal thin films. The correlation between the structure properties and the electrical characteristics of the contacts are also investigated. The study is concentrated on systems chosen for their thermal stability to understand the reaction mechanisms and the effect of the native oxide on the interface reaction. High-temperature stability is a main focus in this research.

1.1. Why Thermally Stable Contacts

Metal-semiconductor interfaces have been a subject of study for important technological reasons. Metal-GaAs electrical contacts have been in increasing demand in solid state electronic devices such as Schottky-barrier impact ionization avalanche transit time (IMPATT), and metal-semiconductor field effect transistors (MESFET). In these devices, electrical properties such as barrier height and contact resistance of the junctions are generally sensitive to the microstructure and chemical composition near the interface.

Recently, the GaAs field effect transistor (FET) has been considered as a basic element for high speed logic circuits. Various types of GaAs FET's and process techniques have been proposed; among these, the self-aligned gate technique is one of the simplest and most feasible approaches to fabricating GaAs large-scale integrated circuits.[1–3] This approach is especially important for enhancement mode MESFET's where source parasitic resistance can significantly degrade transconductance. Using this technology, the parasitic-source series resistance of the FET can be significantly reduced through (self-alignment) placement of the source-drain regions and/or contacts on as close a proximity as possible to the gate region so as to improve switching-speed performance. Also, the self-aligned MESFET is superior in packing desity because it does not require accurate alignment.

Figure 1 shows the major steps in self-aligned GaAs MESFET fabrication.[4] First, the Schottky gate contact is formed on n-GaAs substrate. Next, source and drain regions of an FET are formed by ion implantation using a gate material as an implantation mask which eases constraints on the subsequent source-drain metallization alignment. Then, the ion implanted GaAs wafer, together with the gate material undergoes annealing at high temperature ($\geq$ 800 °C) to activate dopants and to form self-aligned n^+ region. Fabrication is completed by ohmic metallization. The gate material must retain its Schottky contact characteristics with the substrate during high-temperature processing. Since the self-aligned process requires post-implant anneals in excess of 800 °C, the development of a high-temperature compatible Schottky barrier gate metal system is a key technological barrier to be overcome.

The use of ohmic contact metals which can withstand a high annealing temperature reduces and simplifies the process steps for the device fabrication, e.g. simultaneous annealing for contact formation and activation of implanted dopants. Furthermore, application of thermally stable ohmic contacts to MESFET devices reduces deterioration of edge profiles, and the spacing between the gate and ohmic contacts can be significantly reduced, leading to improvement of the device performance.

Concerns for high-temperature stability, reliability and reproducibility have motivated investigations of many alternative Schottky and ohmic contact schemes. For this reason, there has been a significant amount of research devoted to finding materials which maintain stability when in contact with GaAs after exposure to elevated temperature. Increasing attention has recently been directed toward the refractory metals, their silicides and nitrides as gate contacts to GaAs because of their high-temperature stabilities.[1,5–15] For ohmic contacts, there has been a lot of effort to achieve a uniformly stable interface, in particular, In-based ohmic contacts.[16–25]

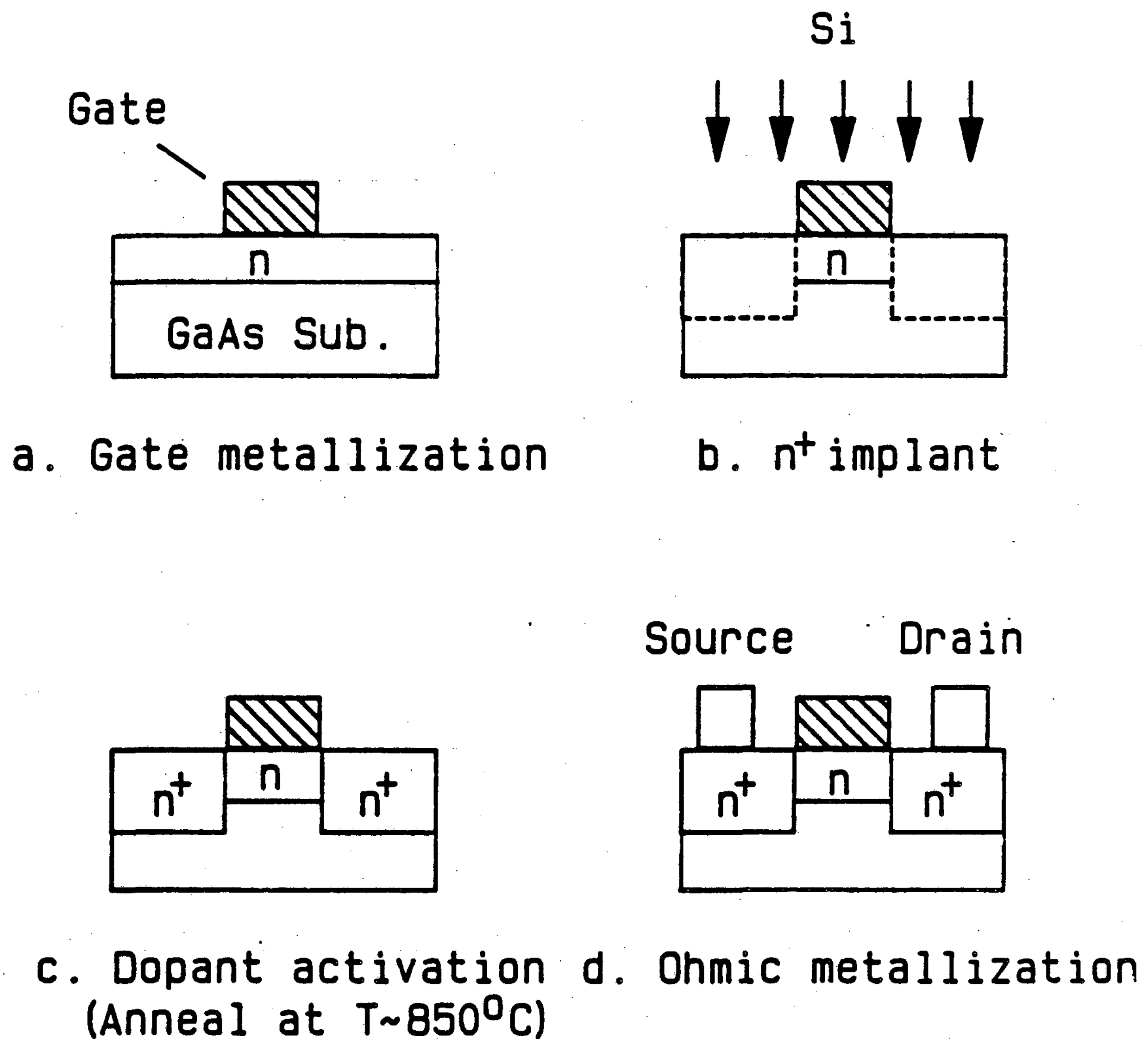

Fig. 1. Major steps of the self-aligned MESFET fabrication process. (From Ref. 4)

1.2. Electrical Background

1.2.1. Schottky Barrier Contact

A rectifying metal-semiconductor contact is known as a Schottky barrier after W. Schottky, who first proposed his now classic model for barrier formation.[26] Schottky and Mott[27] subsequently explained the mechanism of barrier formation and also proposed models for calculating the barrier height and the shape of the barrier. An extensive account of earlier work on metal-semiconductor contacts is reviewed by Henisch.[28]

According to Schottky-Mott theory of the ideal metal-semiconductor contact, when a metal is brought into intimate contact with a semiconductor, the potential barrier acoss the interface is formed by a separation of charges at the metal-semiconductor interface such that a high-resistance region devoid of mobile carriers is created in the semiconductor. It was also suggested that this rectifying nature of the contact depends on the work functions Φ_M and Φ_S of the metal and semiconductor, respectively. The barrier height of the contact Φ_B is equal to the difference between the metallic work function Φ_M and the electron affinity X_S of the semiconductor:

$$\Phi_B = \Phi_M - X_S \tag{1}$$

This is illustrated in Fig. 2 which shows the metal/n-type and p-type semiconductor energy band diagrams before and after the establishment of thermal equilibrium.

Experimental evidence has not, however, borne out the relationshop of Eq. (1). In most practical metal-semiconductor contacts, the ideal situation shown in Fig. 1 is never reached because an abrupt uniform interface free from defects and contamination cannot be realized. For example, the native oxide forms on the semiconductor surface during processing; solid state reaction between metal and semiconductor and interface interdiffusion occur during the contact fabrication, etc.. Metal-semiconductor barriers have been found to exhibit weak or no dependence at all on the metallic work function. The insensitivity of barrier height to the metal work function Φ_M was first explained by

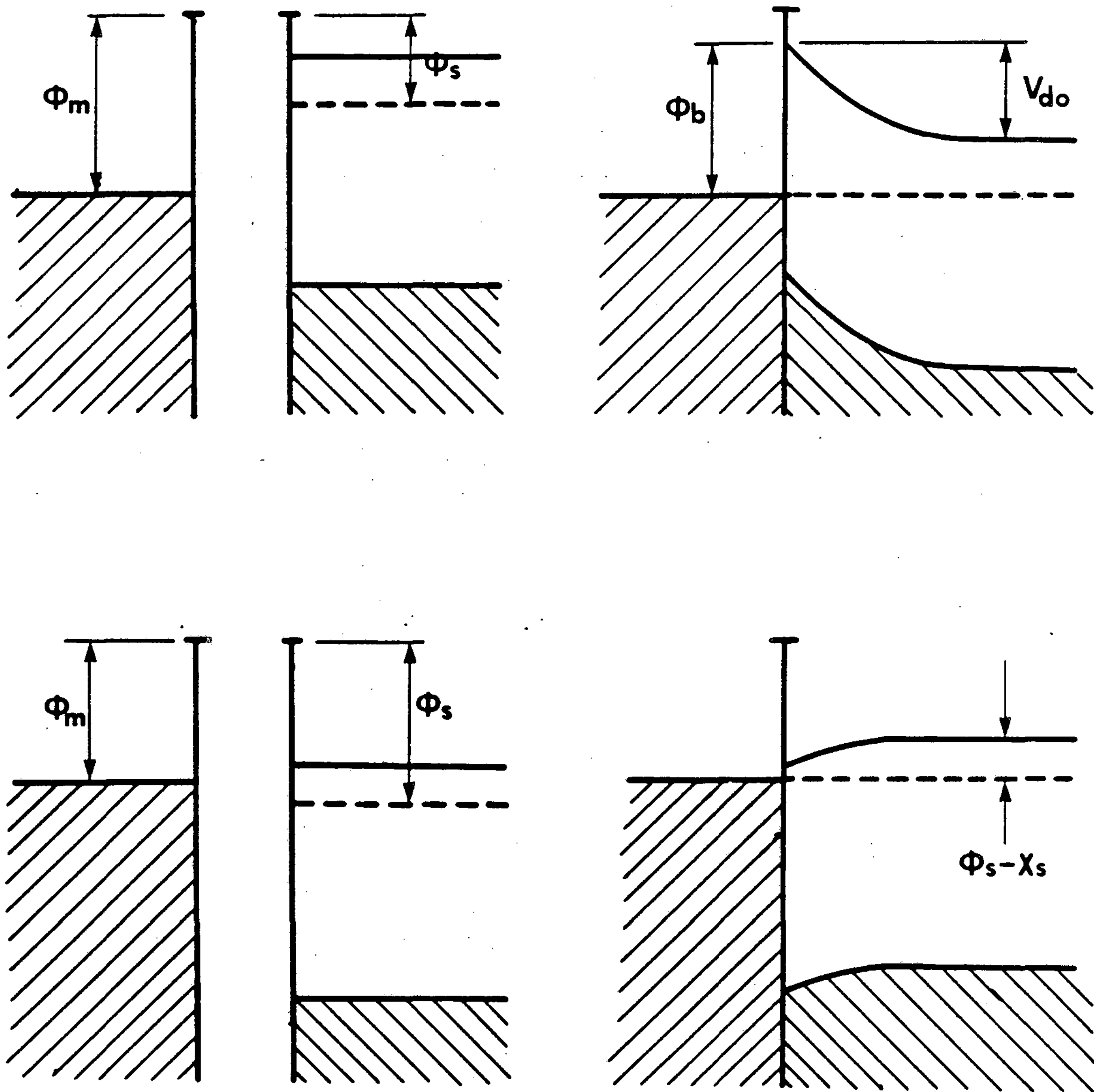

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Fig. 2. The ideal metal and n-type semiconductor band diagram for $\Phi_m > \Phi_s$ (a) before contact, (b) after contact, and for $\Phi_s > \Phi_m$ (c) before contact, (d) after contact, where Φ_m and Φ_s are the work functions of metal and semiconductors, respectively. X_s is the electron affinity of semiconductor. Φ_b and V_{do} are the barrier height and diffusion potential of electrons (carriers), respectively .

Bardeen,[29] who suggested that the discrepancy may be due to the effect of surface states; that in thermal equilibrium there exists a barrier even at the free surface of a semiconductor. If the surface state density is high, this barrier can be pinned to its free surface value after subsequent contact to a metal. Equation (2) represents the limiting form of the Bardeen theory for a high density of surface states such that Φ_B is independent of the metallic work function Φ_M:

$$\Phi_B = E_g - \Phi_o \tag{2}$$

where E_g is the energy gap of the semiconductor, and Φ_o is the neutral level which characterizes the continuous distribution of surface states present at the semiconductor surface. More recent models ascribe the formation of Schottky barriers to "metal-induced gap states",[30] or to defects like anion clusters[31] or point defects[32] near the interface. These models will be introduced briefly in section 1.3.

The conduction properties of metal-semiconductor contacts are determined by the actual transport mechanism. Electrons can be transported across a metal-semiconductor junction in various ways. The dominant mechanism of current flow depends primarily on temperature, barrier height, dopant concentration and its profile, the effective masses of the charged carrier and the dielectric constant. Besides, several other factors such as the presence of interfacial layers or the stoichiometry of the semiconducor surface influence the transport mechanism. At room temperature, and for a relatively light to moderate doping level ($N_{D,A} < 10^{18}\ cm^{-3}$), the dominant mechanism for current transport across a metal-semiconductor interface is thermionic emission[33] of carriers over the top of the barrier. In the case of a very heavily doped (degenerate) semiconductor, it is possible for electrons with energies lower than the top of the barrier to penetrate the barrier by quantum-mechanical tunneling. This may modify the thermionic process in one of the two ways: (1) electrons with energies close to the Fermi-energy in the semiconductor tunnel through the barrier, known as "field" emission;[34,35] (2) "thermionic-field" emission[36] in which electrons are excited to higher energies by increasing the temperature, from which

they "see" a thinner and lower barrier.

An abrupt metallurgical transition between a metal and a nondegenerate semiconductor forms a rectifying Schottky barrier junction with thermionic emission as the dominant conduction mechanism. According to the thermionic emission theory, if V is the applied voltage across the Schottky diode, the current, I, across the barrier is given by:

$$I = SA^{**}T^2\exp(\frac{-\Phi_B^{I-V}}{kT})\ [\ \exp(\frac{qV}{nkT}) - 1\ ] \tag{3}$$

where S is the area of the diode, A^{**} is the effective Richardson constant (8.16 $Acm^{-2}K^{-2}$ for n-type, 74.4 $Acm^{-2}K^{-2}$ for p-type). T is the measurement temperature in degrees Kelvin, q is the electronic charge, k is the Boltzmann constant, and n is an "ideality" factor which is close to unity if thermionic emission is the dominant transport mechanism.

1.2.2. Ohmic Contact

An ohmic contact on a semiconductor should allow electrical current to flow into or out of the semiconductor. "Ohmic" contacts between a metal and a semiconductor are defined as those which exhibit linear current-voltage (I-V) characteristics. The most important feature of such contacts is that the voltage drop across them should be negligible compared with the voltage drop across the device, so that the contacts do not effect the I-V characteristics. In principle, such a contact can be formed by using a metal with a work function less than the work function of the n-type semiconductor or greater than that of the p-type semiconductor. However, there are very few metal-semiconductor combinations which satisfy these conditions due to Fermi-level pinning near the middle of the energy band gap. Therefore, the vast majority of ohmic contacts involve a thin layer of very heavily doped semiconductor immediately adjacent to the metal, so that the depletion region is thin enough to allow the carriers to tunnel through it easily even though the barrier height Φ_B remains essentially the same.

For example, by increasing the doping concentration of a rectifying Schottky barrier junction with thermionic emission as the dominant conduction mechanism, the barrier

width decreases with the square root of the doping concentration and thermionic-field emission starts to dominate. Finally, at very high doping level, the barrier width becomes so narrow that field-emission tunneling is dominant. The contact starts to behave like an ohmic contact when the contact resistance reaches a sufficiently small value. Consequently, the study of ohmic contact formation according to Schottky's theory is reduced to the study of conditions under which the "impedance" of the Schottky barrier is low.

The graded band-gap contact to n-type GaAs was proposed by Woodall et al.[16] and the reported electrical data suggested that this contact is a good condidate for a number of heterojunction devices. The important aspect of such contacts is that they are ohmic by virtue of the formation of a graded $In_{1-x}Ga_xAs$ heterojunction rather than by the creation of the usual n^{++}-doped interface region.

The method for forming graded heterojunction ohmic contacts to GaAs utilizes the fact that for InAs surfaces, Fermi-level pinning occurs at or in the conduction band.[37,38] InAs, with its small band gap (0.36 eV) and Fermi-level pinning at or in the conduction band, can easily form an ohmic contact with most deposited metal films. Figure 3a shows the "conventional" metal-GaAs contact with $\Phi_B = 0.8$ eV. In order to make an "ohmic" contact, it is necessary to form an n^+ layer between metal and n-doped semiconductor. Figure 3b shows the analogous situation for the metal/n-InAs contact. In this case, the Fermi-level is pinned in the conduction band. Thus, there is no barrier Φ_B to electron flow and the contact is ohmic. This indicates that tunneling is not required, and low-resistance contacts can be formed for a wide region of n-type doping levels without the need for n^{++} formation. From this result, one might conclude that an ohmic contact for GaAs can be formed by using the structure M/n-InAs/n-GaAs. This is shown in Fig. 3c. Note that the Fermi-level E_F is pinned at the same position as for the metal/GaAs case, which results in a positive barrier Φ_B between n-InAs and n-GaAs. This band structure will form a rectifying or tunneling ohmic contact, depending on the doping level. This

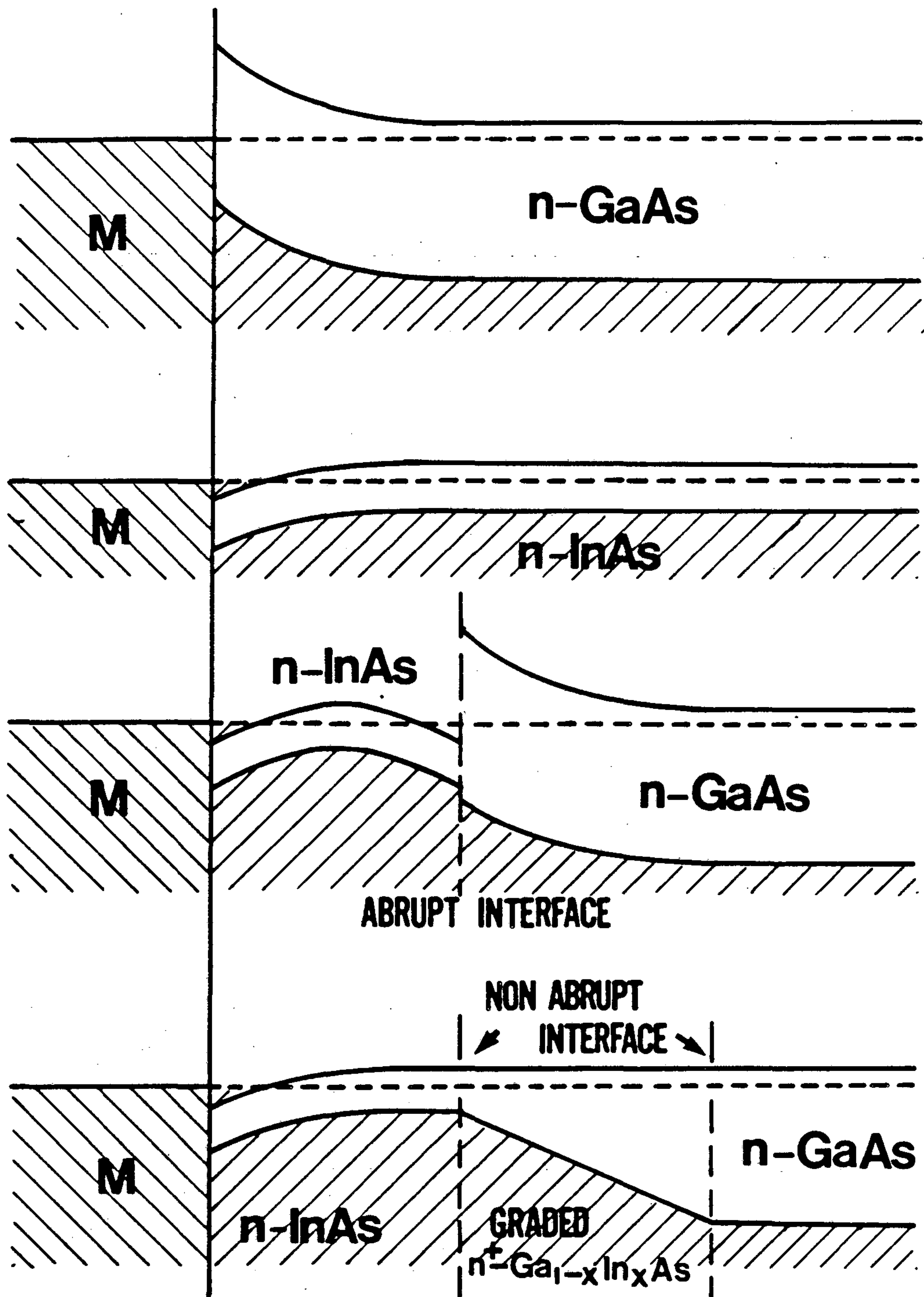

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Fig. 3. Band bending diagram for various semiconductor interfaces: (a) metal on n-GaAs; (b) metal on n-InAs; (c) metal on n-InAs/n-GaAs; (d) metal on n^+-InAs/graded n^+-$In_{1-x}Ga_xAs$/n-GaAs. (From Ref. 16)

may be due in part to the large lattice mismatch (7%) between GaAs (lattice parameter $a_o = 0.565$ nm) and InAs ($a_o = 0.606$ nm). This large lattice constant discontinuity results in a large density of misfit dislocations at the interface which, in turn, pin the Fermi-level in both GaAs and InAs.[39] Other reasons for rectifying behavior may be a large conduction band discontinuity across the interface, and a "dirty" GaAs surface condition prior to thin film growth. To overcome these problems, a non-abrupt interface is formed by grading the interface region $In_{1-x}Ga_xAs$ in composition from $x = 0$ at the InAs interface to $x = 1$ at the GaAs interface. The solution to this problem is shown in Fig. 3d. Due to the fact that there are no abrupt discontinuities in the conduction band, and that Φ_B is ≤ 0 for the M/n-InAs contact, this structure is expected to form non-alloyed low resistance contacts. Misfit dislocations, if present, are distributed and result in a reduced barrier action. J. M. Woodall et al.[16] have fabricated this structure by using Molecular Beam Epitaxy (MBE) to grow a graded band gap layer of $In_{1-x}Ga_xAs$. A low contact resistance, $< 10^{-6}\ \Omega\ cm^2$, has been obtained for a Ag/n-$In_{1-x}Ga_xAs$/n-GaAs MESFET structure.

1.3. Models for Fermi Level Pinning

There has been considerable interest over the past two decades in the mechanisms of Schottky barrier formation at Metal/III-V compound semiconductor interfaces because of the insensitivity of the barrier height to the metallic work function. To account for this "pinning" behavior, researchers have proposed a variety of microscopic models, including gap states due to point defects generated by the release of energy as metal is deposited on the semiconductor serface,[32] metal-induced gap states with Fermi level Φ_F pinned by states intrinsic to the metal-semiconductor interface,[30] effective work functions of interface alloys involving As precipitates,[31] and chemically-formed dipole layers.[40] Most of these models can be traced back to the foundations laid by Bardeen[29] and Schottky[26] many years ago. First, Schottky proposed the work function difference model for the rectifying barrier formation in 1939. Then, Bardeen introduced "Fermi-level pinning" by

surface or interface states in 1947 since there was strong experimental evidence for weak or no dependence of barrier height on work function Φ_M. A broad review of more recent work on the models of Fermi-level pinning at the metal-semiconductor interface can be obtained from several publications.[40,41] Three of the recently proposed models have drawn much attention and will be discussed below.

1.3.1. Unified and Advanced Unified Defect Models

Recently, Spicer and co-workers have introduced a defect model to explain Fermi-level pinning at the metal-semiconductor interface.[32] In order to study the formation of Schottky barriers as well as interface chemistry, etc., on a microscopic level, x-ray photoemission spectroscopy was used to monitor the position of the Fermi-level on clean (vacuum cleaved) GaAs, InP, and GaSb surfaces while metal atoms are deposited under ultrahigh vacuum conditions. It has been found that even less than a monolayer of metal or non-metal can perturb the semiconductor so as to produce lattice defects at or near the semiconductor surface. These defects were considered to be responsible for the Fermi-level pinning in the energy gap of the semiconductors.

The Unified Defect Model (UDM) was derived from a wide range of experimental results.[32] Figure 4 shows the measured distribution of interface states and the corresponding models for GaAs, InP, and GaSb. In this model, acceptor-like states were assigned to anion vacancies and donor-like states were assigned to be produced by cation vacancies. For example, the Fermi-level of (110) GaAs is pinned by two defect states dependent on the type of the substrate, an acceptor level (0.75 eV) due to missing As for n-type and a donor level (0.5 eV) due to missing Ga for p-type.

More recently, Spicer and co-workers proposed an advanced unified defect model (AUDM)[42] which has clarified the defect associated with the levels of the UDM. This improved new model assigned the key point defect to be an As_{Ga} antisite defect which has a good coincidence with the UDM defects on the energy levels as shown in Fig. 5a. This

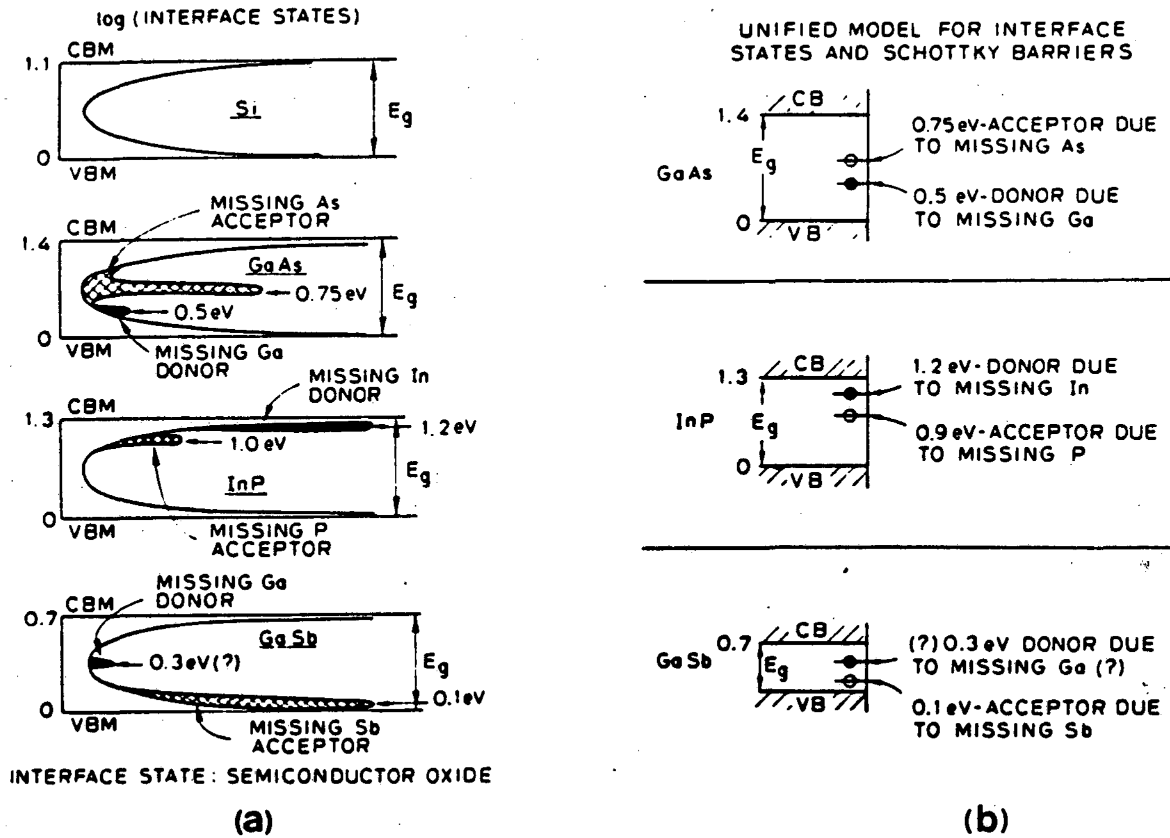
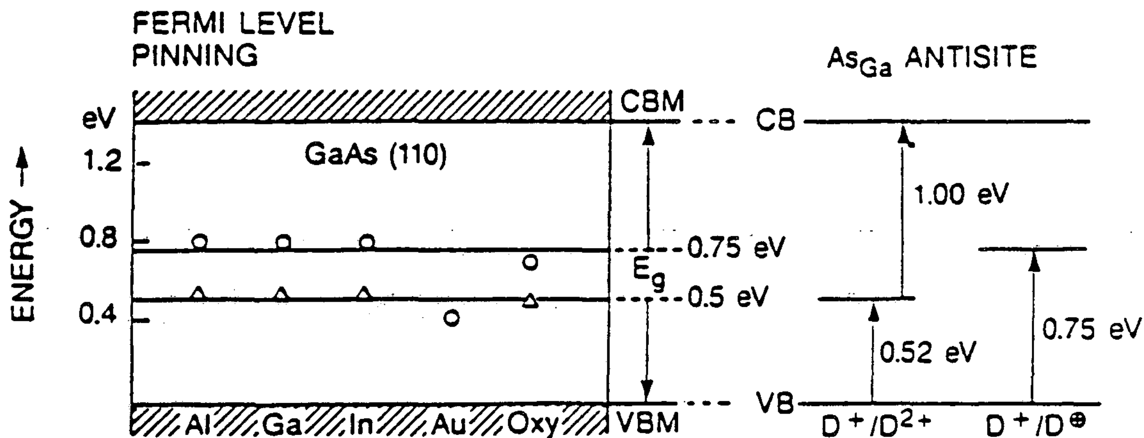
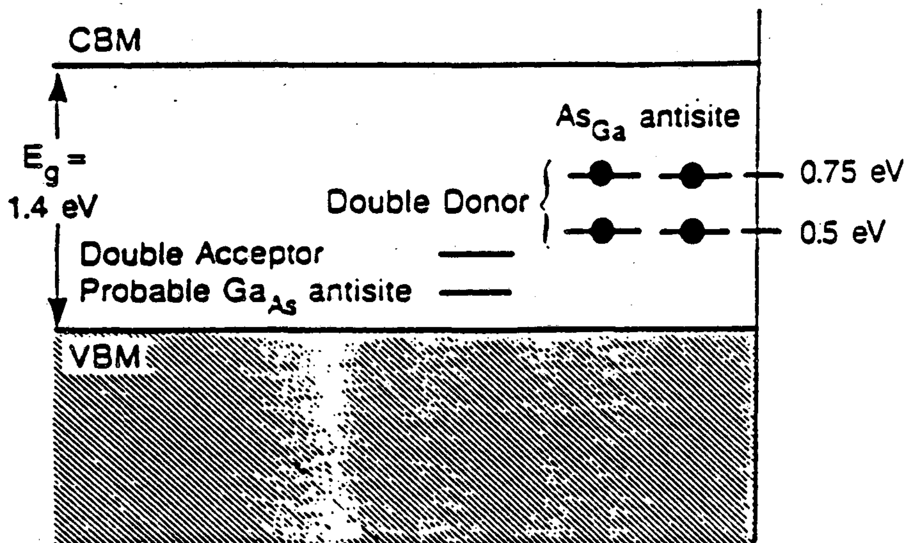


Fig. 4. The model of extrinsic states produced near or at the surface by perturbing the surface through addition of metals or oxygen to the surface of GaAs, InP, and GaP. (a) The defects against the continuum of interface states usually found at semiconductor-oxide interfaces. Si is included for comparison. (b) The position in energy donor or acceptor nature of the defect is shown as well as a suggestion as to the missing atom responsible for the defect. (From Ref. 32)



(a)



ADVANCED UNIFIED DEFECT MODEL

(b)

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Fig. 5. (a) The left energy level diagram for the pinning positions obtained on n- and p-GaAs with very low coverages (1 ML or less) of the indicated element measured at room temperature (E_g = 1.42 eV). The right diagram indicates the defect energy of the As_{Ga} antisite levels from the VBM measured at 8 K (E_g = 1.52 eV). (b) The energy level diagram for the Advanced Unified Defect Model (AUDM). The As_{Ga} antisite double donor with levels of 0.75 and 0.5 eV and the compensating acceptor with levels below 0.5 eV are shown. (From Ref. 42)

antisite defect is a double donor with levels of 0.75 and 0.52 eV above the valence band maximum (VBM), and the level 0.75 eV has been considered to provide EL-2 and semi-insulating GaAs.[43,44] In order to explain the Fermi-level pinning and semi-insulating GaAs based on the antisite defect As_{Ga} (or EL-2), Spicer et al. also suggested that the minority acceptor for compensating the upper donor of As_{Ga} is Ga_{As} antisite defect with energy levels of 0.078 and 0.200 eV above the VBM reported by Figielski.[45] The AUDM is shown in Fig. 5b.

The AUDM has permitted a variety of observations on GaAs surfaces and interfaces to be explained, and the Schottky barrier formation on GaAs can be understood on a microscopic or atomic level in terms of this model. For example, the UDM indicated that a pinning position difference for n-type and p-type is about 0.25 eV which is unable to explain the observation of the same pinning position for many metals no matter if the GaAs is n-type or p-type. Newman et al.[46] found that electronegative metals, such as Au, Ag, and Cu, pin the Fermi-level of n-type GaAs near the 0.5 eV level; electropositive metals such as Al, In, and Ga, on the other hand, pin the Fermi-level near the 0.75 eV level. Spicer et al. have assigned this phenomenon to "movement of electrons from the As_{Ga} sites to the metal for electronegative metals and in the opposite direction for electropositive metals".[42] The AUDM also successfully explains the changes of Schottky barrier height with solid state reaction and interfacial interdiffusion near the metal-GaAs interface due to annealing.

The AUDM has provided a framework for understanding barrier formation at metal-semiconductor interfaces on an atomic level, e. g., the Schottky barrier formation of the metal/GaAs contacts. This new model has been used successfully to explain[42]: the change in Fermi-level pinning behavior upon cooling to low temperatures based on the assumption that only As_{Ga} antisites are formed up to a coverge of about 0.1 monolayer; the Fermi-level pinning on As-rich surfaces and the Fermi-level motion with changing surface stoichiometry for MBE (100) surfaces;[47] the movement of the Fermi-level from

0.75 to 0.5 eV when the As excess changes at the interface in PES and I-V studies of LaB_6 on GaAs;[48,49] the changes of the Schottky barrier heights upon annealing for Au[50,51] and Al[52,53] on GaAs. To evaluate this model, much more work is needed to be done, e. g., to explain the behavior of other metal-semiconductor systems.

1.3.2. Metal Induced Gap State

The Bardeen model[29] assumes that there are surface states intrinsic to the semiconductor which pin the Fermi level at the surface at about one third of the band gap above VBM in covalent semiconductors. In 1965, Heine[54] questioned the Bardeen medel and suggested that in clean contacts the conduction electrons in the metal can tunnel into the forbidden gap of the semiconductor. The wave functions of these electrons will decay exponentially into the semiconductor (typical decay lengths 0.3 $\sim$ 1.0 nm), and these tail states are not localized but extend into the semiconductors. Thus these metal-induced gap states (MIGS) are responsible for the Fermi-level pinning. Louie et al.[55,56] have used semiempirical pseudopotential calculations to model the metal interfaces with several semiconductors, and have shown that the electronic structure was much as described by Heine.[54]

The model of MIGS has recently been revived and refined by Tersoff[30] who proposed a simple model consistent with the theoretical calculation results of Louie.[55,56] Tersoff suggested that the first few layers of the semiconductor contacted by metal must be locally metallic since there is a continuum of states in the band gap of the semiconductor and these states are within several layers from the semiconductor surface. It is argued that the Fermi-level then is pinned at the energy level which gives local charge neutrality. Two contributions were considered to be responsible for the Fermi-level pinning: a short range part related to surface dipoles may result from the electronegativity difference between the metal and the semiconductor or more subtle details of bonding; an additional dipole from the metallic screening by MIGS which tends to pin the Fermi-level so as to

maintain local charge neutrality. The penetration depth of MIGS, i. e., the properties of the semiconductor band structure determines primarily if the short range or metallic screening effect dominates. Tersoff[57] assumed that the Fermi-level at the interface is simply the intrinsic "local Fermi-level" of the "metallized" semiconductor near the interface.

The MIGS has explained, in a simply way, why the Schottky barrier formation of the II-VI compound semiconductors are more dependent on the metal work functions in terms of shorter decay length of electrons for more ionic, larger band gap substrates. The MIGS has been described as that it would be operative at a "perfect" metal-semiconductor interface free of defects or other imperfections.[42] Up to date, the MIGS model has failed to explain the experimental data[58] on the Fermi-level pinning for submonolayer metal coverage and the identical pinning position for intimate metal/semiconductor contact and metal/native oxide/semiconductor system. This model is also considered to lack the ability to explain the changes of the barrier height due to annealing with the metal-GaAs interfacial chemistry.[42] All these have put the MIGS into a questionable position.

1.3.3. Effective Work Function Model

Based on the concept of the original Schottky model, Freeouf and Woodall[31] proposed a new model, called the effective work function model (EWFM). In the Schottky model, the barrier height of an n-type semiconductor is equal to the difference between the metal work function Φ_M and the semiconductor electron affinity X_S under the assumption that the interface is abrupt and free of the surface states and induced interface states:

$$\Phi_{Bn} = \Phi_M - X_S \tag{4}$$

where Φ_{Bn} is the Schottky barrier height at the metal/n-type semiconductor interface. Therefore, the barrier height between a metal and a given n-type semiconductor should be determined by the metal work function, which has not been confirmed by many experimental results.

The EWFM model suggested that the barrier heights of metal-semiconductor interfaces can be determined by replacing the work function of the metal in the Schottky model with the effective work functions of the several phases formed at the interface. These phases were believed to result from either oxygen contamination or metal-semiconductor reaction during metallization. They argued that each phase at the interface has its own work function and the effective work function Φ_{eff} is the weighted average of the work functions for the different phases present. The modified formula is shown as:

$$\Phi_{Bn} = \Phi_{eff} - X_S \tag{5}$$

Freeouf and Woodall also believed that the anion is the primary contributor to the effective work function Φ_{eff} for the III-V semiconductors and the Fermi-level pinning is independent of the contact metal. For example, for metal-GaAs contacts, the Fermi level should be pinned by the presence of excess As at the metal/GaAs interface which may also form As precipitates, which dominate the interface behavior and thus dictate the effective work function. Since excess As is required at the interface to form anion clusters, this approach could be considered as coincident with the defect approach in which As_{Ga} antisites are assumed to be dominant.[42]

Freeouf and Woodall[31] have shown a reasonably good agreement between the predictions of the EWFM and the experimental data of the barrier heights from Au and several semiconductors. The problems with this model are: (1) the large uncertainty in the work functions for different overlayers, which results in difficulty in comparing the predictions with the experimental results; (2) the formation of metal-anion phases and the segregation of cations on the surfaces in many GaAs and InP systems. A more detailed discussion of this model can be found in Ref. 40.

1.4. Metallurgical Background

1.4.1. Thermally Stable Materials

As discussed in section 1, the development of very large scale integrated (VLSI) technology to submicron dimensions presents new challenges to the semiconductor industry, with special concerns for device reliability and stability. Since smaller contact size of the device requires a low resistivity contact metal and since the contact metallurgy has to withstand thermal cycles associated with a high temperature metallization process (~800 °C), many studies have been focused on understanding and developing suitable contact materials which can prevent or reduce the reaction between the contact metal and semiconductor to maintain contact performance after the thermal process. In recent years, researchers have paid much attention to refractory metal nitrides because of their high temperature and chemical stability. For example, a critical aspect of the self-aligned gate process in MESFET fabrication is the selection of a refractory material for use as the gate, the Schottky barrier, which must be stable during the post-implantation annealing (typically 800 °C).

As mentioned above, one of the most important requirements in developing devices such as MESFET's is the fabrication of thermally stable contacts to GaAs with uniform interfaces. In the case of Schottky barrier contacts, most single element metallizations react rapidly with GaAs at high temperatures. The result of this high-temperature chemical instability is usually a degradation in the electrical characteristics of the contacts, as has been observed for Nb,[5] Ti[6] and W[1,7,8] metal layers. In contrast, several refractory metal silicides (e.g., $MoSi_2$,[9] W_5Si_3,[11,12]), and nitrides (e.g., TiN,[12,13] NbN,[5,13] ZrN[13] and WN[13–15]) have been demonstrated to be superior to elemental metal layers as Schottky barrier contacts to GaAs. In terms of their high temperature stability, good electrical conductivity and low diffusivity,[59] the nitrides are more attractive alternatives for thermally stable thin film design in the fabrication of MESFET's. These refractory metal

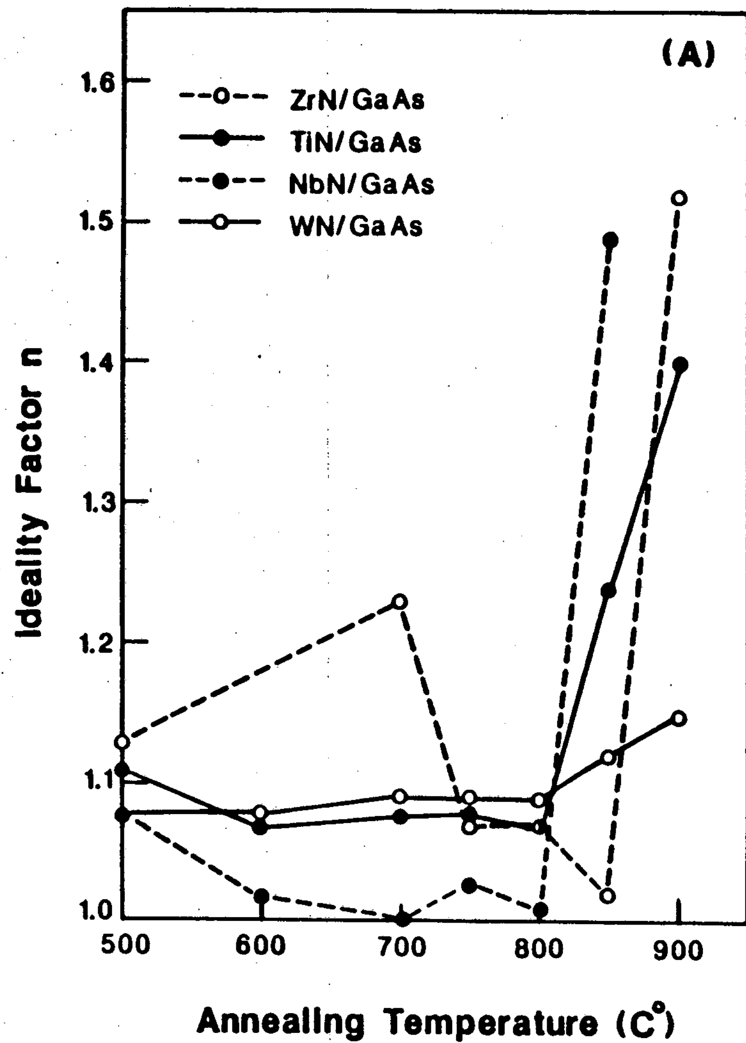
nitrides exhibit improved chemical stability and electrical characteristics,[13] such as enhanced Schottky barrier height and good ideality factor after a high temperature anneal as shown in Fig. 6. Hence, the electrical characteristics of these nitride contacts can remain relatively unchanged or even improved after annealing.

The AuNiGe system has been extensively used as an ohmic contact to n-type GaAs,[60–63] yielding reproducible contacts with low contact resistivity of $10^{-6}\Omega cm^2$. However, the spread of the contact resistance values is usually large, which is a result of the nonuniform microstructure at the interface.[64,65] Furthermore, the existence of the β-AuGa phase with a low melting point (375 °C) deteriorates the interface uniformity, causing an increase in contact resistance even after annealing at 400 °C. This has resulted in a contact edge slide which was measured to be 0.2-0.47 μm after contact alloying at 440 °C for 2 minutes in this system.[66] This effect of contact edge slide could limit the use of the AuNiGe contact in GaAs submicron devices. Contacts such as the graded $In_{1-x}Ga_xAs$ band-gap contact to n-type GaAs proposed by Woodall[16] in 1981 have many advantages compared to AuNiGe contacts, especially for those applications requiring small-area self-aligned devices. In particular, it is important to develop technologies which result in low resistance, thermally stable, uniform and shallow contacts that are compatible with refractory metallization. Recent development on In-based ohmic contacts such as MoGeInW[24] and NiInW[25,67] have shown excellent results with a uniform interface and low resistance remaining even after annealing at 850 °C.

During fabrication of the device, the chemical behaviour of the system can give rise to unexpected metallurgical changes at the interface. The existence of a native oxide layer on the substrate prior to deposition may also effect the morphology of the interface. For examples, see references 68 and 69.

1.4.2. Refractory metal nitrides

The alloying of transition metals with the elements H, B, C, O, N, and Si creates a



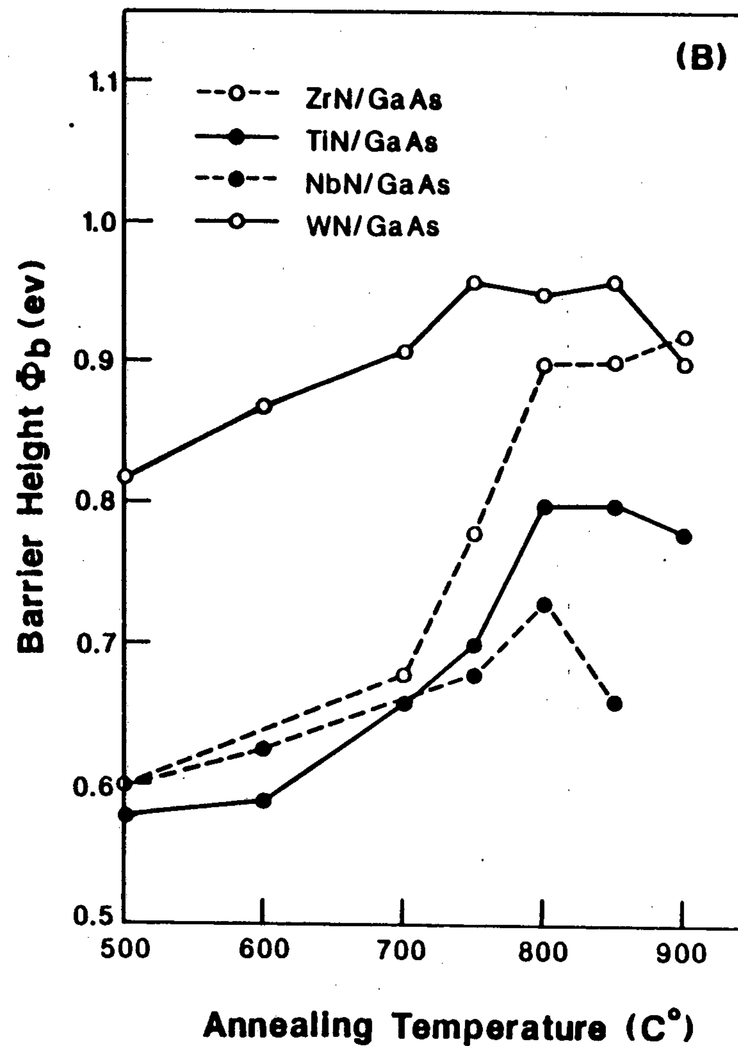


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Fig. 6. Ideality factors n and barrier Φ_b for ZrN, TiN, NbN and WN contacts on GaAs annealed at different temperatures. (From Ref. 13)

family of structures known as interstitial compounds.[70–73] These alloys are known as such because the smaller nonmetal atoms are located in the octahedral or tetrahedral sites of the metal lattice. The structure of interstitial systems can be described in geometrical terms as an array of metal atoms with the smaller nonmetal atoms located in the interstices; it is found that they are formed only if a radius ratio of nonmetal-to-metal atoms is less that about 0.59. The lattice of the interstitial compound is frequently found to be either cubic or hexagonal close packed with a co-ordination number 12 or cubic body centered with a co-ordination number 8. For radius ratios > 0.59, the crystal structure of the interstitial compounds is usually more complex. For compounds of the stoichiometry MX, where X is either carbon, nitrogen or oxygen, the structure is frequently the NaCl structure which is composed of an fcc metal lattice with the octahedral sites filled by the smaller interstitial atoms. Examples of these compounds are TiN, ZrN, VN, and ZrH. The stoichiometry of these structures can vary widely by the creation of vacancies on either the metal lattice sites or on the interstitial sites. The result of these variations in stoichiometry can lead to a wide range of properties for materials of nominally the same composition and structure.

The characteristics of interstitial compounds are summarized below. Interstitial compounds resemble metals in their opacity and characteristic lustre, they are good electrical conductors and, in common with alloy systems, they often show an indeterminacy of composition and a sequence of distinct phases. They differ from intermetallic systems, however, in that they are brittle and extremely refractory, and have a hardness often approaching that of diamond. They also have very high melting temperatures (2000 °C∼4000 °C). Due to those special properties, interstitial compounds are finding increased industrial application.[59,74–77]

The exceptional stability of the interstitial compounds with the sodium chloride structure is ascribed to the preference for octahedral co-ordination about the metal atom as well as about the nonmetal. This suggests that the metal orbitals involved are the

d^2sp^3 hybrids, and it is noteworthy that the interstitial structures are formed by just those metals in which such hybridization is commonly found. Therefore, this structure satisfies simultaneously the requirements of the bond configuration of both metal and nonmetal.[59,71]

Bonding in refractory metal nitrides has not been completely understood. There are numerous contradictory theories of bonding for these nitrides, and available experimental evidence is not sufficient to distinguish unambiguously between these theories. Nevertheless, certain features in these theories have been used to interprete physical properties of these nitrides.[59]

The refractory metal nitrides are metallic in their electrical, optical, and magnetic properties.[59,71] Most of these properties have been found to differ slightly from those of the parent refractory metal elements. These properties were considered to be attributed to defect structure, principally vacancies on both nonmetal and metal lattices sites. It is also believed that their bonding is resposible for the metallic characteristics of these nitrides, probably combining contributions from both localized metal-nitrogen bonds and delocalized metallic bonds. For examples, typical resistivity values are 117.5 $\mu\Omega$ cm for ZrN, 80 $\mu\Omega$ cm for TiN, and 120 $\mu\Omega$ cm for NbN.[13,74,75]

1.4.3. Miscibility Gap

A continuous solid solution can only be formed if all components in the system have the same structure. Generally, the free energy of mixing of the solid solution system, ΔG_m, is given as:

$$\Delta G_m = \Delta H_m - T\Delta S_m \tag{6}$$

where the ΔH_m is the enthalpy of the mixing, the ΔS_m is the entropy of the mixing, and T is temperature in Kelvin. In the case of the regular solution, the enthalpy of mixing, i. e., the heat of solution, can be positive or negative, depending on whether one type of atom is preferably surrounded by the same type or a different type, respectively.[78–82] If $\Delta H_m <$

0, the free energy of mixing ΔG_m decreases at all temperatures as a result of mixing, since $T\Delta S$ is always positive. All alloys formed in this case are stable as a single phase solid. If $\Delta H_m > 0$, i. e., the different type of atoms 'repel' each other, the shape of the free energy versus composition curve may change strongly with temperature. At high temperatures, the $T\Delta S_m$ term is dominant for all compositions so that it is possible that the free energy of mixing ΔG_m versus composition curve has a positive curvature as that for $\Delta H_m < 0$. As the temperature is lowered, however, the enthalpy of mixing ΔH_m will begin to dominate in the free energy expression in Equ. 6 and the free energy of mixing ΔG_m develops a negative curvature in the middle region. In this middle region, two phases of similar lattice structure, but different composition and lattice spacing, co-exist in equilibrium. This region is known as a miscibility gap.

When immiscibility occurs, construction of a series of double-tangent lines to the free energy curve is possible.[78–82] This trace of tangent points is called a binodal curve, or miscibility gap, in a phase diagram, which marks the boundary between metastable and stable regions on the free energy curve. The trace of inflection points for the free energy curve is called a spinodal curve, which marks the boundary between metastable and unstable regions in the free energy cruve. Fig. 7a and 7b show the construction of a phase diagram with a miscibility gap (binodal curve) and the spinodal curve from the free energy curves. On a set of tangent points (binodal points), which can be connected by a tie line, solid solution component chemical potentials are equal for the two conjugate compositions,[80–82] and hence solid-solid equilibrium is possible between them.

As discussed above, a homogeneous phase will become unstable when it falls inside the spinodal curve and will favorably decompose into two separate phases. This process is called spinodal decomposition.[83] The two compositions of the separate phases in equilibrium are the binodal points, whose tie line passes on the initial composition. In thermal annealing (cooling) of a solid solution, the spinodal point will give a criterion for immiscibility. In crystal growth processes in near-equilibrium condition, as in LPE and VPE,

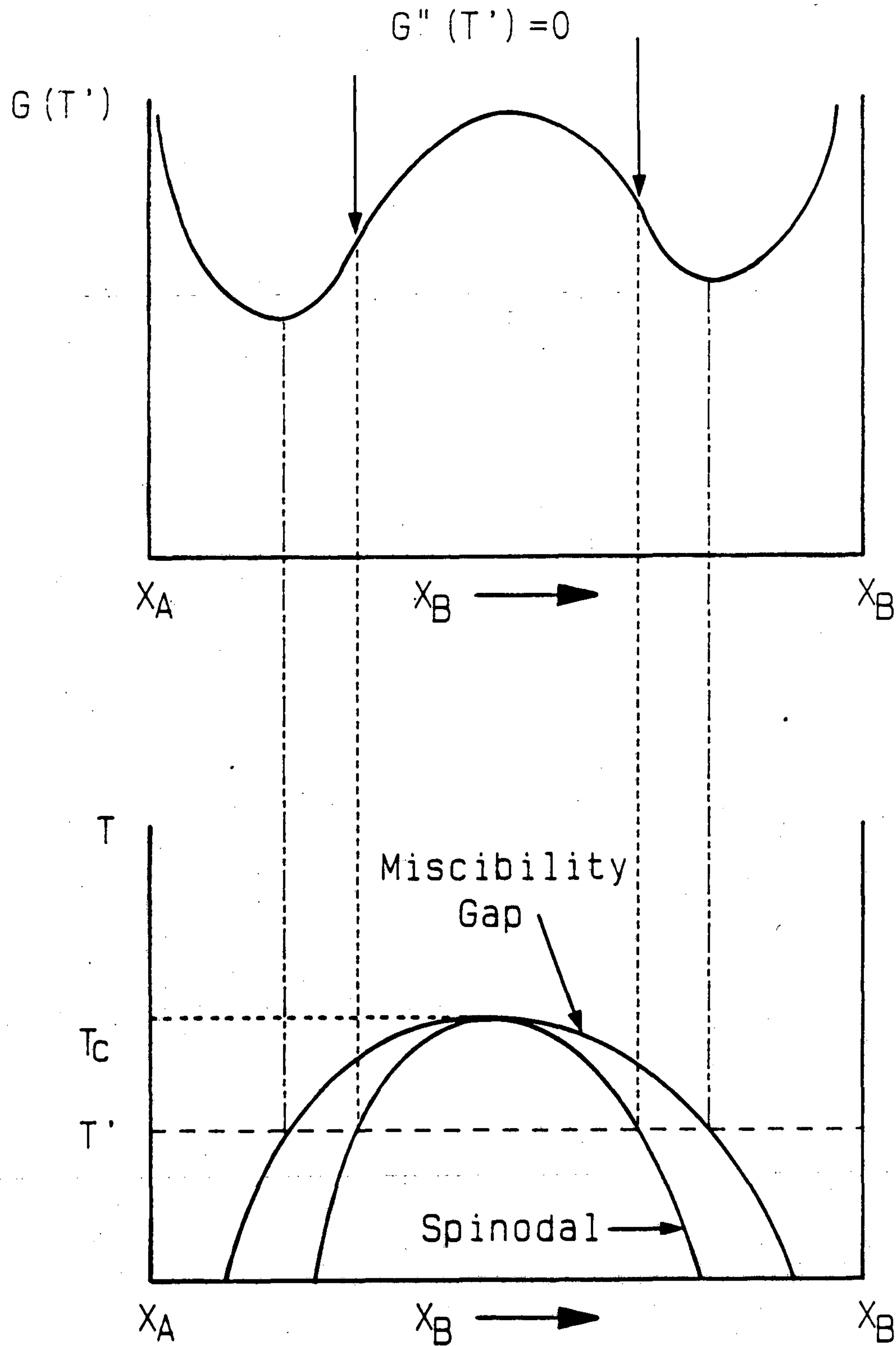

Fig. 7. Free energy v. composition curve and the corresponding phase diagram show the miscibility gap and spinodal.

immiscibility will manifest itself, being governed by binodal points.[84–87] A thermodynamic miscibility gap is defined as (metastable) + (unstable) regions bounded by binodal curves.[78–82] Thus, a full description for immiscibility in a solid solution must include both spinodal and binodal curves (with associated tie lines).

In earlier studies, various experimental[84–89] and theoretical[90–92] aspects of the phase relationships in the III-V compound semiconductor alloys were investigated. One of the principal concerns was the limit of miscibility in the solid phase, since this restricts the compositions that are important for basic research as well as for device technology. Calculations based on the thermodynamic properties of these III-V compound semiconductors have shown that an immiscibility gap occurs for some of the ternary and most of the quaternary alloy systems which are of practical interest.[90–92] Hence, some of these alloys, when below particular temperatures, should be unstable and so alloy clustering, i. e., local variations in chemical compositon, may then occur by the spinodal decomposition mechanism.[83] For example, for the GaInAsP system, calculations by de Cremoux et al.[90] predicted the existence of the miscibility gap of the InAs-GaAs psuedobinary system.

2. EXPERIMENTAL APPROACHES

The experiment approach for this study involves the fabrication and heat treatment of thin metal films on GaAs, characterization of the interface structure and morphology, and measurement of electrical characteristics.

In this research, transmission electron microscopy (TEM) has been used as the major tool to study the interface structure and morphology and reveal the orientation relationship between the thin film and substrate. Due to its superior spatial resolution, high-resolution electron microscopy (HREM) has been chosen for the identification of microphases and for the study of the details of the interface structure and morphology including the intervening oxide, misfit dislocations and other interfacial microdefects. Selected area diffraction (SAD) has been used also to identify the structure of the phases when possible. X-ray diffraction (XRD) has been performed to study the phase formation on a macroscopic scale. Energy dispersive x-ray spectrometry (EDS) which is one of the most widely used techniques for the chemical analysis of small areas has been used to determine the chemical compositions of the interfacial phases. Other analytical techniques such as x-ray photoelectron spectroscopy (XPS) is also applied to study the depth profiles, and chemical compositions of the metal-GaAs contact systems whenever necessary. The electrical characterization of these contacts are studied mostly by current-voltage (I-V) and capacitance-voltage (C-V) measurements.

2.1. Fabrications of Metal/GaAs Contacts

2.1.1. In/GaAs

In this investigation, liquid encapsulated Czochralski (LEC) semi-insulating GaAs wafers were used as substrates. In order to obtain suitable TEM specimens for the studies of surface and interface morphologies and orientation relationships between the GaAs substrate and the thin films, a very thin indium film is necessary. This requirement has

been satisfied by using the Molecular Beam Epitaxy (MBE) technique because of the possibility of accurate thickness control and oxide-free interface.

The samples were prepared by the following processes. After the substrates were degreased by boiling in chloroform, acetone and methanol twice for five minutes each time, respectively, they were etched with concentrated HCl for two minutes. Before swabbing the surface with H_2SO_4, the substrates were cleaned again in methanol by boiling twice for five minutes each time. Finally, the substrates were rinsed in deionized water and blown dry with nitrogen gas. These wafers were loaded into the MBE chamber. The temperature was increased up to 600 °C in approximately 10 minutes under ultra high vacuum conditions. The native oxide on the surface of the substrate was desorbed at 600 °C without an arsenic flux impinging on its surface. The (RHEED) pattern showed an arsenic stabilized surface after the oxide desorption. Following the oxide removal, the substrate was allowed to cool to 25 °C (approximately 30 min.). Indium was then deposited onto the rotating substrate (8 RPM) for 10 minutes with a deposition rate of 5.7 nm/min. under a vacuum of 3.2 x 10^{-9} Torr.

2.1.2. Nb/GaAs, NbN/GaAs and TiN/GaAs

The n-type (100) GaAs wafers with Si doping concentration of 1.5 x 10^{17} cm^{-3} were used as substrates. First, the substrates were degreased by boiling in trichlorethylene (TCE), acetone, and methanol for 10 minutes each time, respectively. These wafers were then eched with H_2SO_4:H_2O_2:H_2O (5:1:1) at 65 °C for 4 minutes to remove the first 4 μm layer where polishing damage and undesirable impurities are usually located. To ensure removal of the native oxide on the substrates, a dilute HCl (1:1) dip was performed right before the samples were loaded into the sputtering chamber.

Thin films were deposited onto the GaAs substrate by two different types of sputtering systems: radio frequency (rf)-diode sputtering for TiN and dc-magnetron sputtering for Nb and NbN. For both sputtering systems, the sputtering power, N_2/Ar flow ratio,

deposition time, and substrate temperature were controlled to obtain the best film composition and to improve adhesion to the substrate.

The sputtering system was pumped down to a residual gas pressure of 2~3 x 10^{-7} Torr. To minimize the amount of oxygen incorporated into the sputtered metal nitride films, the target was cleaned by presputtering in pure Ar for 50 minutes followed by a 10-min presputtering with the N_2-Ar gas mixture to form a nitride surface layer on the target.

The Nb thin film about 55 nm thick was deposited on GaAs by dc magnetron sputtering in an Ar ambient. The Ar pressure was chosen to be 14 mTorr to minimize stress in the film.[93] The deposition rate was about 12 nm/s with a power density of 7.7 W/cm^2.

For NbN deposition, the N_2/Ar flow ratio was 30% with a background pressure controlled at 6.5 mTorr. The power density was 9.6 W/cm^2. About 55 nm NbN film was deposited on GaAs with a deposition rate of approximately 8 nm/s.

For TiN, about 40 nm film was deposited on GaAs at a rate of ~8 nm/min. The flow ratio of N_2/Ar was 20% and rf-power density was 2.5/cm^2 under a total ambient pressure of 8 mTorr.

2.1.3. WN/GaAs

Si doped (5 x 10^{17} cm^{-3}) GaAs wafers in (100) orientation were used as substrates. These wafers were first degreased in organic solvents and then etched in 1:1 HCl:H_2O solution to remove the native oxide on the substrate surface. Finally, the substrates were rinsed in deionized water and blown dry with nitrogen gas. Prior to loading into sputtering chamber, the wafers were dipped in an 1:1 NH_4OH:H_2O solution for 1 minute to remove mechanical damage on the GaAs surface. A base pressure was 2.5 x 10^{-7} Torr and sputtering power density was 2 KW.

2.2. Annealing

2.2.1. In/GaAs

In order to investigate the miscibility gap in the pseudo-binary InAs-GaAs system, the samples were divided into four groups and annealed for 10 minutes at 350 °C, 500 °C, 575 °C and 650 °C respectively in an atmosphere of flowing forming gas (95% Argon, 5% Hydrogen).

2.2.2. Refractory Metal Nitride/GaAs Contacts

For Schottky barrier contacts, rapid thermal annealing (RTA) was used for ion implantation because the improved dopant activation, higher mobility of carriers, and sharper doping profiles can be achieved with this technique. Before annealing, all samples were capped with sputtered silicon nitride SiN_x on both the front and back sides as encapsulating layers to suppress the escape of the volatile As atoms from the substrate through the thin film. Subsequent rapid thermal annealing was carried out in the temperature range of 500~900 °C in a flowing Ar ambient using a halogen lamp system (AG Associate 210 Rapid Thermal Annealing). After RTA, the silicon nitride at the back side of the samples was removed by reactive ion etching (RIE) in a CF_4:O_2 plasma (CF_4:O_2 flow ratio ~10:1, rf-power ~150 W). Back-side ohmic contacts were formed by evaporation of Au-Ge followed by a 1-min sintering step at 450 °C in forming gas. The front side SiN_x cap layer was removed afterwards by RIE in CF_4/O_2 plasma at a much lower power to prevent attacking on both GaAs substrate and metal nitride films.

2.3. TEM Specimen Preparation

Pieces of the processed specimens (2 x 5 mm) were cleaved from the samples along the <110> cleavage directions of the GaAs wafer. After cleaning with acetone, two pieces of the specimens were glued face to face with epoxy (Devcon "two ton" epoxy works

well). This was done to attain better mechanical strength and facilitate handling, and also for the protection of the processed serfaces. This GaAs specimen assembly was allowed to stand for 30 minutes in an oven at the temperature of 70 °C for a complete drying of the adhesive. It was then placed onto the specimen mount of a GATAN Model 623 Disc Grinder with wax which allows the specimen to be thinned in the <110> GaAs directions. In order to avoid unwanted reaction between the thin film and GaAs substrate when the specimen was put into the molten wax on the mount, the specimen mount was taken off the hot plate, then cooled until the wax was viscous (~80 °C) before the specimen was placed on the mount.

The assembly was placed into the polisher using 1200, 2400 and 4000 mesh emery paper down to 1.5 mm, respectively. The final polishing was accomplished with 0.05 μm gamma alumina powder on a micropolish cloth with a rotating wheel. This polishing procedure was repeated on the other side of the specimen until a final thickness of between 20 and 50 μm was achieved. In order to facilitate uniform thinning, care was taken to ensure that the specimen was in good contact with the metal stage along its entire length. The same processes were repeated to remove these specimens.

Finally, the specimens were glued to a copper grid (3 mm diameter) for support and ease of handling. Subsequent thinning was performed in an ion milling machine with a liquid nitrogen cold stage. The thinning conditions were set at 14 ° specimen tilt, 5 KeV accelerating voltage and 0.5 mA argon ion (Ar^+) beam current for two guns. Since the crystal bonding of refractory metal nitrides is much stronger than GaAs, a low ion milling angle (~11 °) was used to obtain more uniform thickness at the interface region. In order to limit the effects of ion beam heating, the specimen stage was cooled in liquid nitrogen for 30 minutes prior to milling.

2.4. Electron Microscopy Investigations

The electron microscopy studies of the interfacial structure and morphology, and the orientation relationship between the thin films and GaAs substrate were carried out using cross-sectional specimens. Conventional TEM studies of the interface structures and orientation relationships were performed in Philips EM 301 and EM 400. Energy dispersive x-ray spectra were acquired with a Kevex model 7000 spectrometer on a Phlips EM 400 electron microscope. A JEOL 200CX transmission electron microscope equipped with an ultra-high resolution pole piece was employed for the cross-sectional work to obtain more detailed information of the interfaces, such as the identification of microphases and the study of the details of the interface structure including the intervening oxide, misfit dislocations and other interfacial microdefects.

2.5. Qantitative Microanalysis

Due to the overlap of diffraction spots from GaAs and Ga-rich $In_{1-x}Ga_xAs$, the estimation of composition by the electron diffraction technique was not straightforward for $x \sim 1$. Instead, the compositions of these Ga-rich precipitates were estimated by applying the energy dispersive spectrometry technique to cross-sectional samples. The EDS spectra were quantitatively analyzed by determining the proportionality factors $K_{X/Y}$ which relate the height ratios H_X/H_Y of the x-ray peaks (proportional to the total counts or intensities) to the concentration ratios [X]/[Y] of the elements X, Y. The relationship between the concentration ratio and the peak height ratio is expressed as:

$$[X]/[Y] = K_{X/Y} \frac{H_X}{H_Y} \quad (7)$$

where the proportionality factor $K_{Ga/As}$ relates the heights of the Ga and As $K\alpha$ peaks in spectra taken from the adjacent GaAs substrate. The value of x in the $In_{1-x}Ga_xAs$ is then given by the ratio [X]/[Y] determined from spectra taken from the $In_{1-x}Ga_xAs$ precipitate.

2.6. X-Ray Diffractometry

X-ray diffractometry was performed on a Siemens D500 x-ray diffractometer using CuKα radiation and a graphite monochromator. Step-scan mode (every 0.1° (2θ) per second) was used for the measurements through a Bragg angle 2θ, ranging from 20 to 90°. Composition and structure of the as-deposited thin film and phases formed after annealing were estimated by matching the diffraction peaks in the x-ray spectrum with those of x-ray powder diffraction data files.[94]

X-ray diffractometry was used to confirm the TEM results of the phase identification for the as-deposited thin film and the phases formed at the interface after annealing at various temperatures. This technique offers a very convenient, nondestructive and quick means to accurately compare x-ray spectra for different samples and for the same sample before and after annealing. A Seeman-Bohlin glancing angle x-ray diffractometer was also used due to its great sensitivity for very thin films.

2.7. Electrical Characteristics

The electrical properties of refractory metals and their nitride contacts on GaAs were characterized by both current-voltage and capacitance-voltage measurements. All the measurements were performed using a HP 4140B automatic current meter and HP 4192A automatic impedance analyzer.

The I-V characteristics of the Schottky contacts were analyzed in terms of the thermionic emission model of current transport[95]:

$$I = I_S \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \tag{8}$$

where I_S is defined as the saturation current density, V is the applied voltage, T is the temperature, q is the electronic charge, k is the Boltzmann constant, and n is an "ideality" factor which is close to unity if thermionic emission is the dominant transport mechanism. The equation 8 can be written as:

$$I = I_S \exp(\frac{qV}{nkT}) \tag{9}$$

for $V > 3kT/q$. The thermionic-emission barrier height Φ_B^{I-V} is related to I_S by:

$$I_S = SA^{**}T^2 \exp(\frac{-\Phi_B^{I-V}}{kT}) \tag{10}$$

where S is the area of the diode, A^{**} is the effective Richardson constant (8.16 $Acm^{-2}K^{-2}$ for n-type, 74.4 $Acm^{-2}K^{-2}$ for p-type). For a given Schottky contact, a value of I_S can be obtained by extrapolating the lnI vs V curve to zero voltage. At the forward bias regime, the Schottky barrier height Φ_B^{I-V} and ideality factor n can be determined from:

$$\Phi_B^{I-V} = kT\ln(\frac{SA^{**}T^2}{I_S}) \tag{11}$$

$$n = \frac{q}{kT}\frac{\partial V}{\partial \ln I} \tag{12}$$

where n corresponds to the slope of the lnI vs V curve.

The C-V characteristics of Schottky contacts were analyzed by plotting as $1/C^2$ vs V according to the conventional C vs V equation for the one-sided abrupt junction model:

$$1/C^2 = 2(\epsilon q N_D)^{-1}(V_d - V - \frac{kT}{q}) \tag{13}$$

where the intercept V_i on the voltage axis is related to the built-in V_d by $V_i = V_d$ - kT/q; N_d can be determined from the slope of $1/C^2$ vs V plot. The Schottky barrier height obtained by the C-V measurement is :

$$\Phi_B^{C-V} = V_i + \Phi_n + \frac{kT}{q} \tag{14}$$

where $\Phi_n = (E_C - E_F)$ is the energy difference between the Fermi-level and the bottom of the conduction band. A detailed description of the C-V measurement technique can be found in Ref. 96.

3. RESULTS AND DISCUSSIONS I:
Refractory Metals and Their Nitrides-GaAs Contacts

Refractory metal nitrides such as NbN, TiN, WN and ZrN are of considerable theoretical and practical interest due to their unique combination of properties including extreme hardness, high melting temperatures, low electrical resistivity, and wide range of superconducting properties.[59,70,72] These properties have been considered to be associated with a complex interatomic bonding comprised of covalent, metallic, and ionic contributions.[59] The present interest in these nitrides stems from thermodynamical and electrical properties which open up potential applications in the microelectronics industry.[97–99] Recent studies showed that these nitrides are among the most promising diffusion barrier materials in both silicon and III-V compound device technology in multilevel metallization schemes.[74,76,77,100,101] Other applications include use as the gate electrode in MOS transistors and as thermally stable Schottky contacts in MESFET's.[12,13,102]

As gate materials, refractory transition metals or their silicides have been preferentially used in the past.[1,5,6,9–11] Recently, refractory metal nitrides such as WN, ZrN, TiN and NbN have been investigated as contact materials to GaAs to achieve more thermally stable and higher Schottky barrier contacts.[13] In order to further improve the electrical properties of these contacts, a knowledge of the interfacial phenomena occuring during the formation of Schottky barrier contacts is of significant important. A fundamental understanding of the effect of the high annealing temperature on the interface morphologies and structures is necessary. In this work, a study of the interfacial phenomena occurring during thermal treatment has been undertaken in order to further determine high-temperature stabilities of the interfaces for refractory metals and their nitrides in contact with GaAs. NbN, TiN and WN contacts to n-GaAs were investigated. Nb/GaAs system was also studied for comparison with the NbN/GaAs contacts.

3.1. Nb/GaAs Contacts

3.1.1. Interface Structure and Morphology

Nb thin films were deposited on Si-doped (100) GaAs by dc magnetron sputtering, followed by rapid thermal annealing at 600 °C and 700 °C for Nb/GaAs samples as mentioned in Chapter 2. The annealing temperatures for this system were chosen to correlate the measured electrical characteristics with the structural properties at the interface.

For the as-deposited Nb thin films on GaAs substrates, a polycrystalline microstructure of the Nb thin film was revealed by plan-view transmission electron microscopy. As shown in Fig. 8, Nb grains in the thin film had an average size of ~30 nm. From the electron diffraction pattern shown in Fig. 8, the thin as-deposited film had a bcc structure with a lattice parameter $a_o = 0.331$ nm. The rings in the diffraction pattern were indexed to be 110, 200 and 211 reflections etc..

The interface morphology of as-deposited sample has been studied by transmission electron microscopy of cross-sectional samples. The TEM image in Fig. 9c shows that the interface was flat with a thin intervening oxide layer between the as-deposited Nb film and the GaAs substrate. This intervening native oxide can be seen as a thin white line at the interface. The thickness of this intervening layer was estimated to be about ~1 nm from the high resolution TEM image shown in Fig. 9c. The electron diffraction from the interface region of the cross-sectional sample in Fig. 9b reveals a preferred orientation relationship between the as-deposited Nb and the substrate: $(\bar{1}10)_{Nb}//(001)_{GaAs}$ and $[111]_{Nb}//[110]_{GaAs}$. This orientation relationship indicates that the Nb grains grow with a prefered orientation during the deposition. The presence of this preferred orientation relationship also suggests that the oxide layer did not cover the substrate surface completely and uniformly due to the instability of the Ga and As oxides on the surface of the GaAs substrate.[103] This orientation relationship will be discussed in a later section.

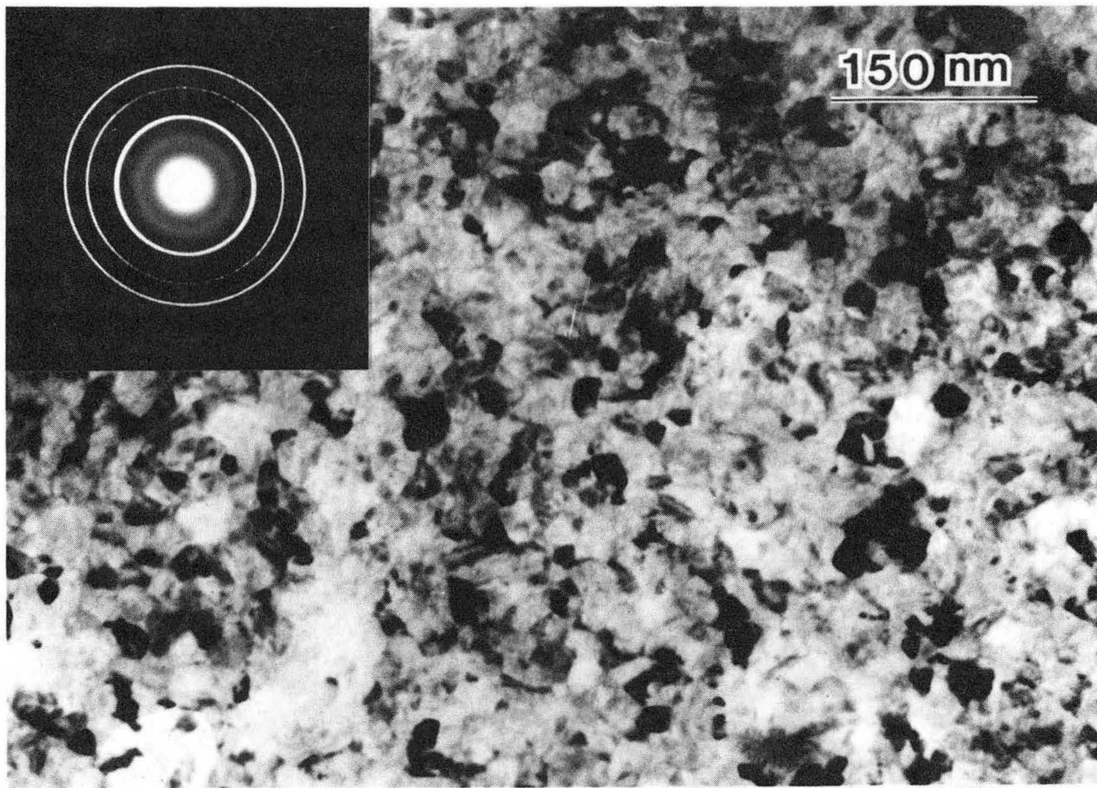

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Fig. 8. Plan-view TEM image and corresponding electron diffraction pattern of the as-deposited Nb/GaAs sample.

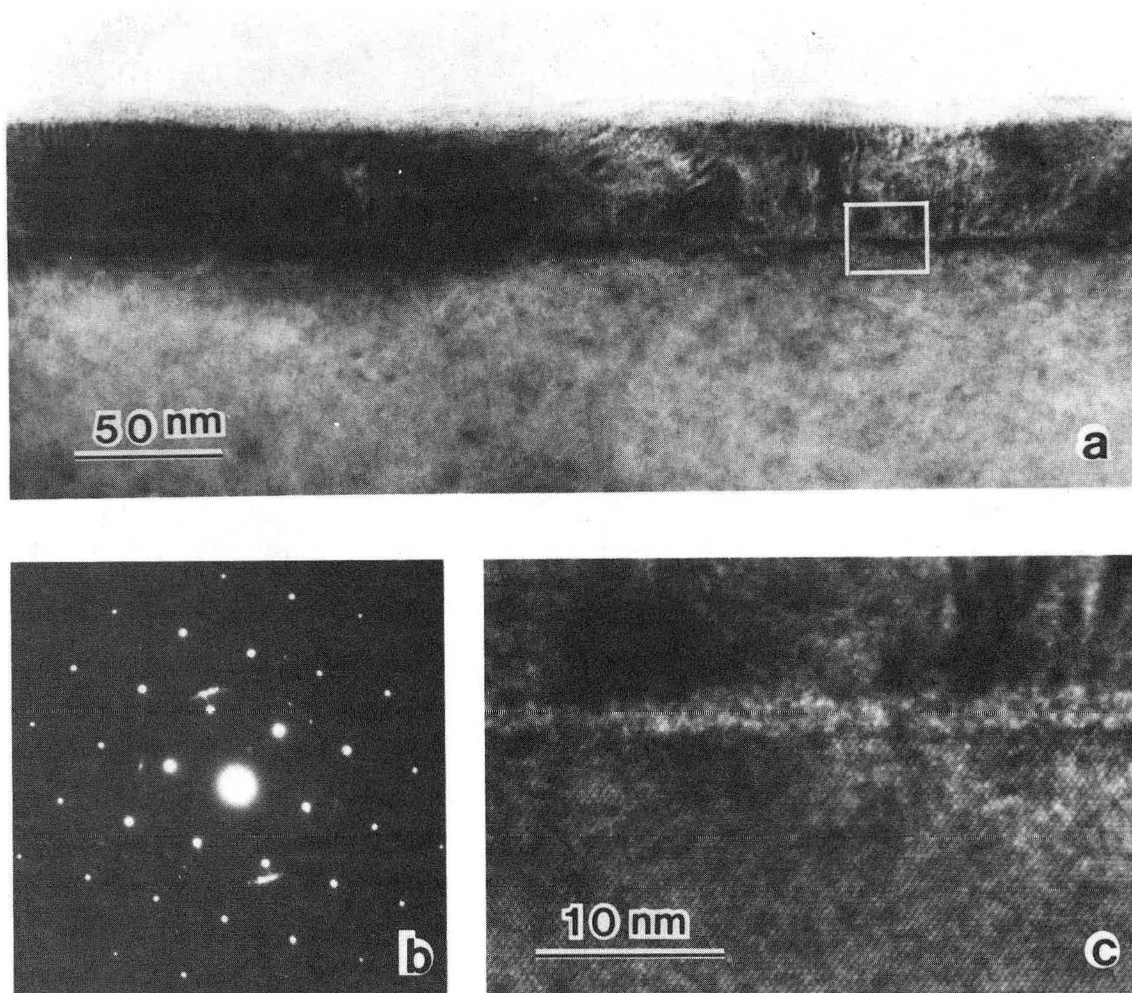

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Fig. 9. (a) Cross-sectional micrograph of the as-deposited Nb/GaAs interface. (b) Diffraction pattern from the same area showing the preferred orientation relationship between the Nb film and the GaAs substrate. (c) High-magnification image of the region boxed in (a).

The interface morphology of Nb/GaAs samples after annealing at 600 °C is shown in the XTEM image of Fig. 10a. As can be seen, the Nb/GaAs interface remains sharp after annealing at 600 °C but the intervening oxide has disappeared. The intervening oxide at the interface was dispersed or absorbed by the as-deposited Nb phase. Another reason for this sharper interface may be the removal of the sputtering damage caused during the sputtering deposition of the Nb thin film. From this TEM image, there is no evidence of significant Nb/GaAs reaction at the interface. The plan-view TEM image in Fig. 11a also did not show evidence of a Nb/GaAs reaction at the interface, nor any significant change in the grain size of the Nb.

However, the results from electron diffraction and x-ray data did give evidence of the formation of new phases for the 600 °C sample. Fig. 11b is the electron diffraction pattern from a plan-view sample. The diffraction rings in this pattern were indexed as shown in Table 1. As can be seen in Table 1, four possible phases were formed during 600 °C annealing: Nb_3Ga_2, Nb_3As, Nb_3Ga and Nb_4As_3. This suggests that interface interdiffusion has occurred during the annealing. As shown in Fig. 10a, it is clear that the interface is not flat and the interface at the areas marked by arrows has moved ~ 3 nm down into the substrate as the results of interface interdiffusion and incomplete coverage of native oxide.

Figure 12 shows the high resolution TEM image from the interface area marked by A in Fig. 10a. From this TEM lattice image, it can be seen that the area B and area C are on top of the regions where more GaAs from the substrate was consumed due to the interdiffusion through thin areas or pin-holes in the native oxide layer. Lattice spacings from the area B and area C were measured to be 0.35 nm and 0.256 nm, respectively. Based on this measurement and the electron diffraction data in Table 1, the phase in area B was considered to be Nb_3Ga_2. The measured lattice spacing (0.35 nm) corresponds to the lattice spacing between Nb_3Ga_2 (001) planes. The Nb_3Ga_2 phase has a tetragonal structure with lattice parameters $a_o = 0.692$ nm and $c_o = 0.35$ nm. The phase in area C

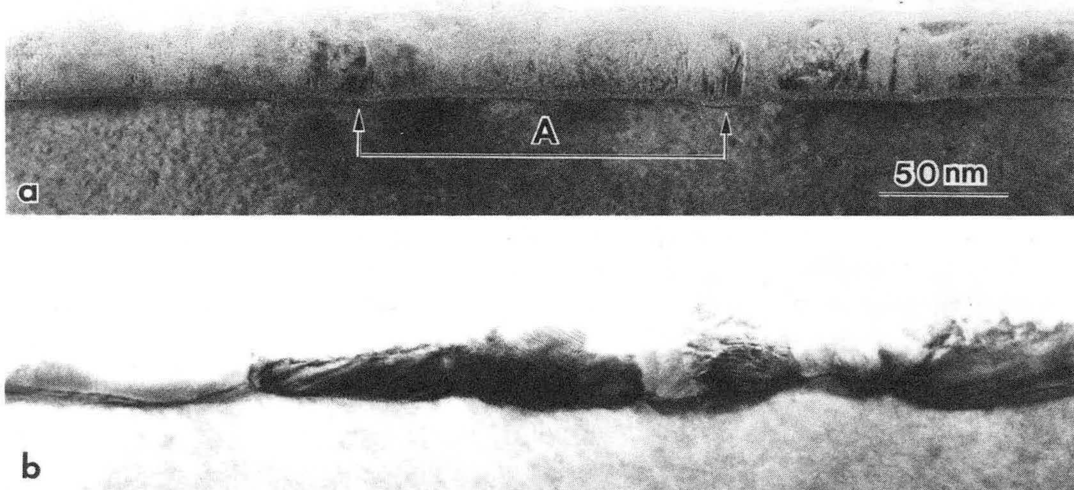

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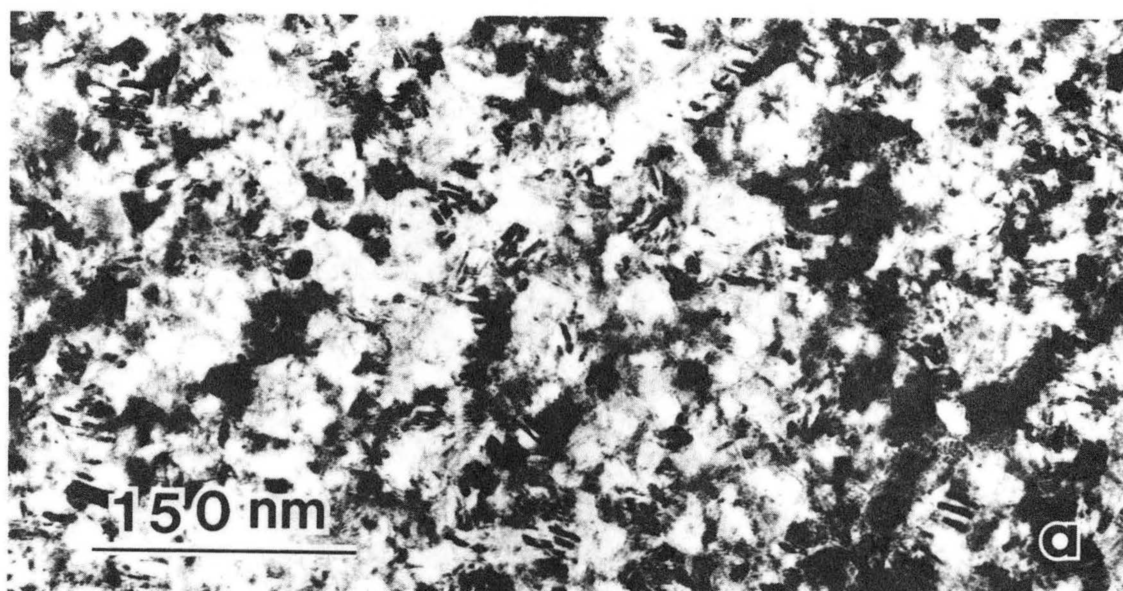
Fig. 10. Cross-sectional TEM images of the Nb/GaAs (a) annealed at 600°C, and (b) annealed at 700°C for 10 seconds.



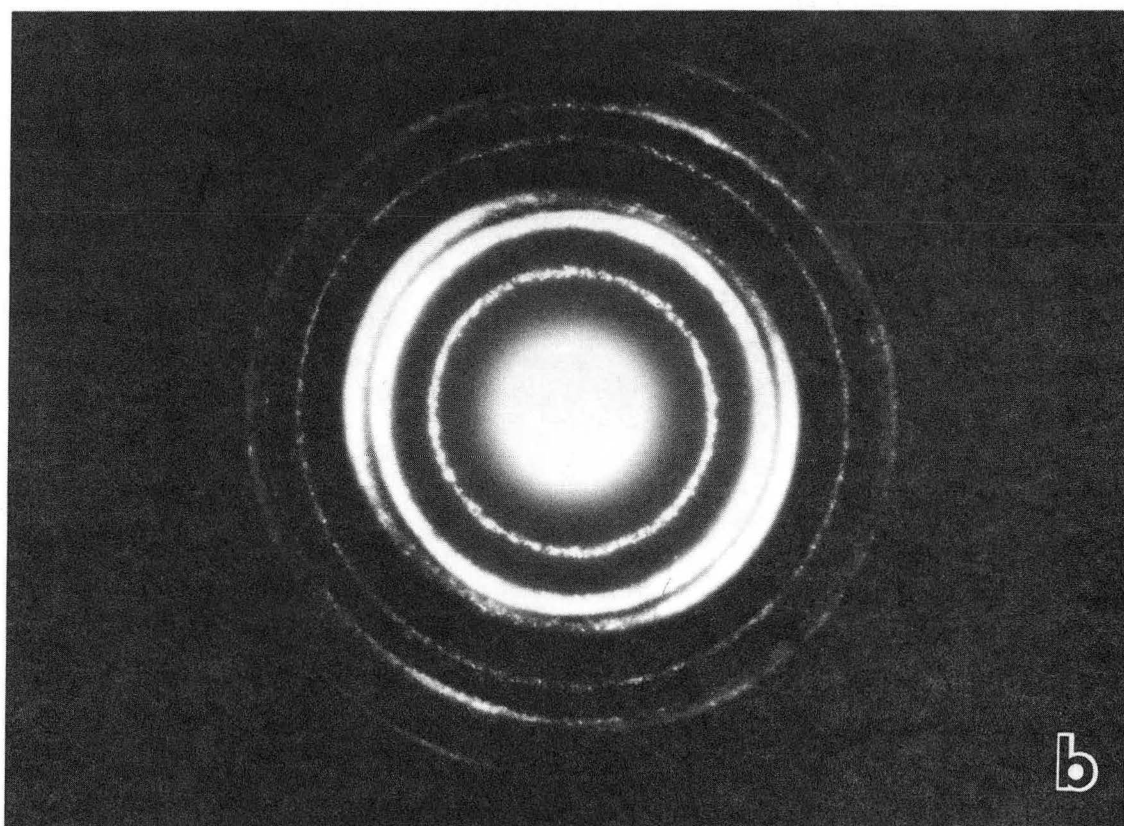


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Fig. 11. (a) Plan-view TEM image of the Nb/GaAs sample after annealing at 600°C for 10 seconds and (b) the corresponding electron diffraction pattern.

Table 1. Comparison of SAD data for annealed Nb/GaAs samples with powder diffraction data from the JCPDS file.

Nb/GaAs SAD data[a]	Powder diffraction data.[b]			
	Nb_3Ga_2	Nb_3As	Nb_3Ga	Nb_4As_3
0.343 nm	0.350 (001)	0.345 (201)		0.342 (110),(042)
0.240–0.260	0.244 (201),(220)		0.256 (200)	0.244 (134) 0.253 (115)
0.215–0.234	0.218 (310) 0.231 (100)		0.231 (210)	
0.175	0.175 (002)	0.177 (332)		0.176 (083),(200)
0.171		0.172 (600)		0.171 (084)
0.156	0.156 (202)	0.156 (223)		
0.149	0.148 (331)	0.148 (323)	0.148 (222)	
0.142	0.141 (421)	0.142 (143)	0.143 (320)	
0.136	0.137 (312)	0.136 (721)	0.138 (321)	
0.131			0.124 (400)	
0.123	0.122 (440)			

[a]The lattice spacings measured from the selected area diffraction (SAD) patterns.

[b]Powder Diffraction File (JCPDS International Center for Diffraction Data, Swarthmore, Penn., 1980).

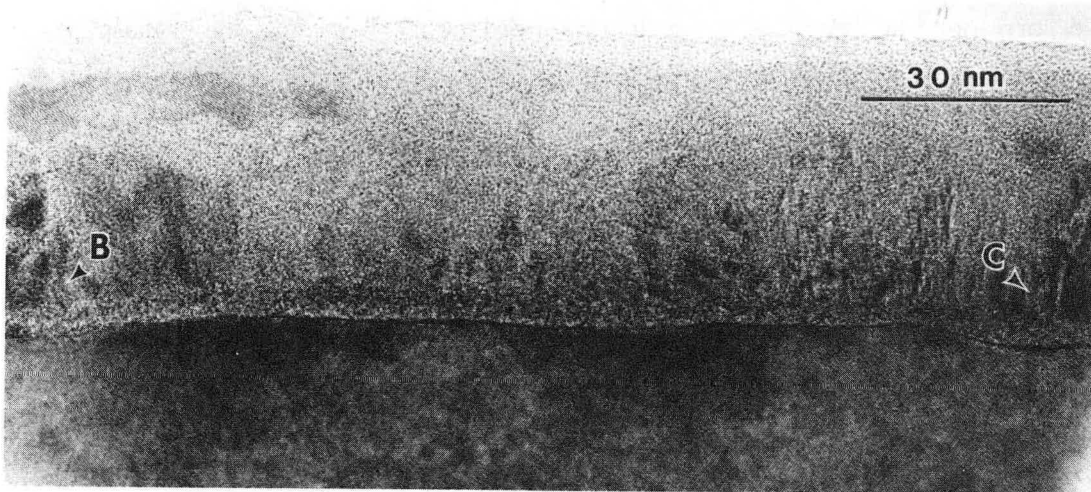

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Fig. 12. High-resolution TEM image from the interface area marked by A in Fig. 10a for the sample after annealing at 600°C for 10 seconds.

was identified as Nb_3Ga which has a cubic structure with a lattice parameter $a_o = 0.517$ nm. The lattice spacing measured in this case was 0.256 nm, which corresponds to the lattice spacing between Nb_3Ga (200) planes. It is not surprising that phase Nb_3Ga was formed right above the area where GaAs was consumed, and phase Nb_3Ga_2 was further above the interface since more GaAs from the substrate was consumed under the area C. No corresponding lattice spacings in this TEM image were found for phase Nb_3As and phase Nb_4As_3. However, since the lattice spacing 0.257 nm between Nb_3As (400) planes is so close to the measured value 0.256 nm, the phase in the area C could alternatively be Nb_3As.

Annealing at 700 °C resulted in a dramatic interface reaction with a laterally nonuniform morphology at the interface (Fig. 10b). Only binary phases were detected in the Nb/GaAs contact system after rapid thermal annealing at the temperatures above 700 °C. The results show two major phases, Nb_4As_3 and Nb_5Ga_3, with some evidence of NbAs and $NbGa_3$ formed during the annealing, yet there was still unreacted Nb, identified by electron diffraction analysis and confirmed by x-ray diffraction. As shown in Fig. 10b, the interface is nonuniform. This is probably due to the non-uniform native oxide layer on the substrate.

The interface morphology of the 700 °C sample studied by cross-sectional TEM shows that most regions in the film had mixed phases with microdefects in contact with the substrate while in other areas a layered structure of the film had been formed. Figure 13 is an example of this layered structure formed after RTA annealing for only 10 seconds. By measuring the lattice spacing of the phase contacting the substrate, this intermediate layer was identified to be NbAs which has a tetragonal structure with lattice parameters $a_o = 0.3452$ nm and $c_o = 1.1679$ nm. This intimate NbAs contact to GaAs is thermodynamically stable as will be shown in the Nb-Ga-As phase diagram (in Discussion). The phase on top of the NbAs has been identified as Nb_5Ga_3.

The electron diffraction pattern shown in Fig. 14 is the superimposed diffraction pat-

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Fig. 13. Cross-sectional TEM micrograph of the Nb/GaAs sample after annealing at 700°C for 10 seconds. Note that the layered structures were formed after annealing.

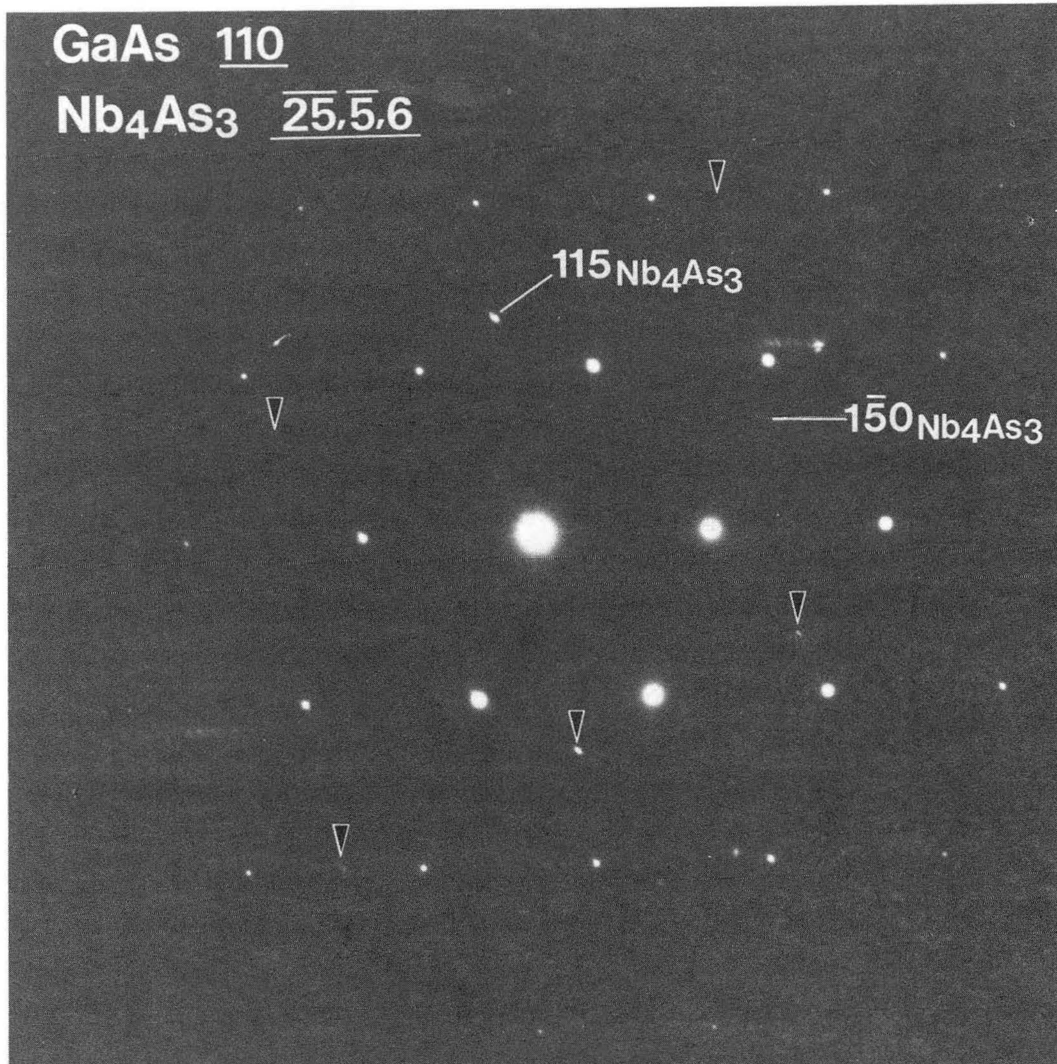

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Fig. 14. Electron diffraction pattern from the Nb/GaAs interface after annealing at 700°C. Note that the diffraction pattern from the Nb_4As_3 grain with a [$\overline{25}\,\overline{5}\,6$] zone axis is superimposed on the [110] GaAs diffraction pattern.

terns from the GaAs substrate and a Nb_4As_3 single crystal grain in the film. In this case, the diffraction pattern from the Nb_4As_3 grain has a $[\bar{2}\bar{5}\bar{5}6]$ zone axis parallel to the [110] zone axis of the GaAs substrate. Figure 15 gives another example which shows superimposed diffraction patterns from the GaAs substrate and a Nb_5Ga_3 single crystal grain. In both the electron diffraction patterns shown in Fig. 14 and Fig. 15, there are extra spots in addition to the diffraction patterns from the GaAs and the identified phases. These extra spots come from the grains which do not have a low index zone axis aligned with the [110] GaAs zone axis. The first major Nb-GaAs reaction product is the binary phase Nb_5Ga_3. The structure of this binary phase is body centered tetragonal with lattice parameters: a_o=1.028 nm, c_o=0.506 nm. Phase II, i. e., the second major phase, is also a binary phase Nb_4As_3. This Nb_4As_3 phase has a base orthorhombic structure with lattice parameters a_o=0.3516 nm, b_o=1.4661 nm and c_o=1.8830 nm.

Determination of the phase distribution was difficult due to the small size of the grains (about 20 nm) and high concentration of defects such as microtwins and stacking faults. The high resolution electron microscopy (HREM) image in Fig. 16 shows these microdefects in the reacted film near the interface. The phase on the left side was found to be Nb_4As_3 by measuring the lattice spacing. On the other side, stacking faults in the film are shown overlapping the substrate to form the morie fringes. The phase with the microdefects remains unknown.

3.1.2. Correlation Between Electrical Properties and Interface Morphology

The I-V characteristics[5] of the Nb/GaAs rectifying contacts were analyzed by a modified thermionic-emission theory as shown in Equ. 8 in Chapter 2. Figure 17 shows the forward and reverse I-V characteristics of the Nb/GaAs contacts before and after RTA at 600 °C and 700 °C for 10 seconds at each temperature. The Schottky barrier height Φ_b and ideality factor n are determined from the lnI-V plot by using Equ. 11 and Equ. 12, respectively. It is clear from the lnI-V plot that 600 °C annealing did not change

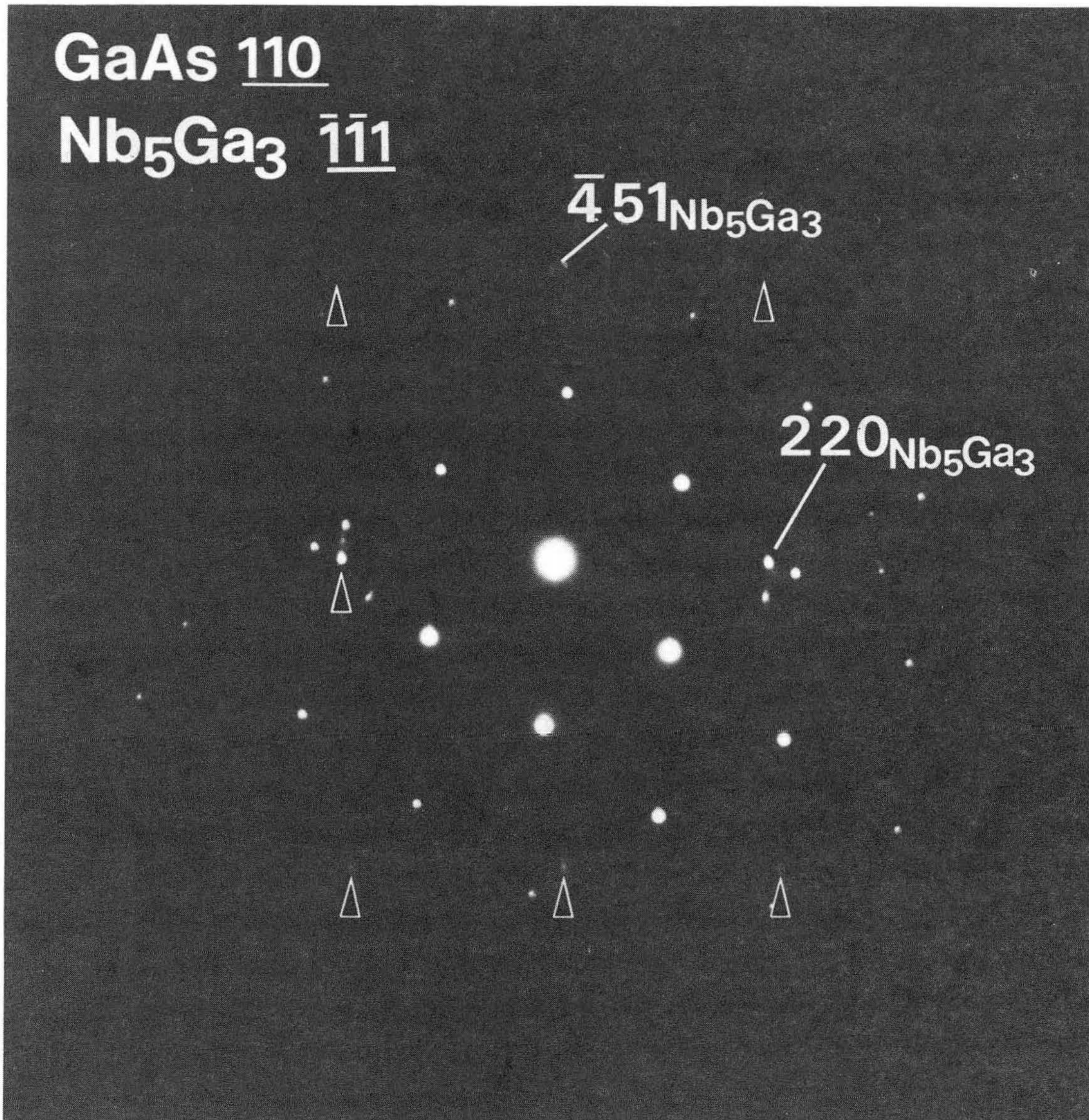

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Fig. 15. Diffraction pattern from the Nb/GaAs cross-sectional sample annealed at 700°C for 10 seconds, where the diffraction pattern of a Nb_5Ga_3 grain has a $[\bar{1}\bar{1}1]$ zone axis.

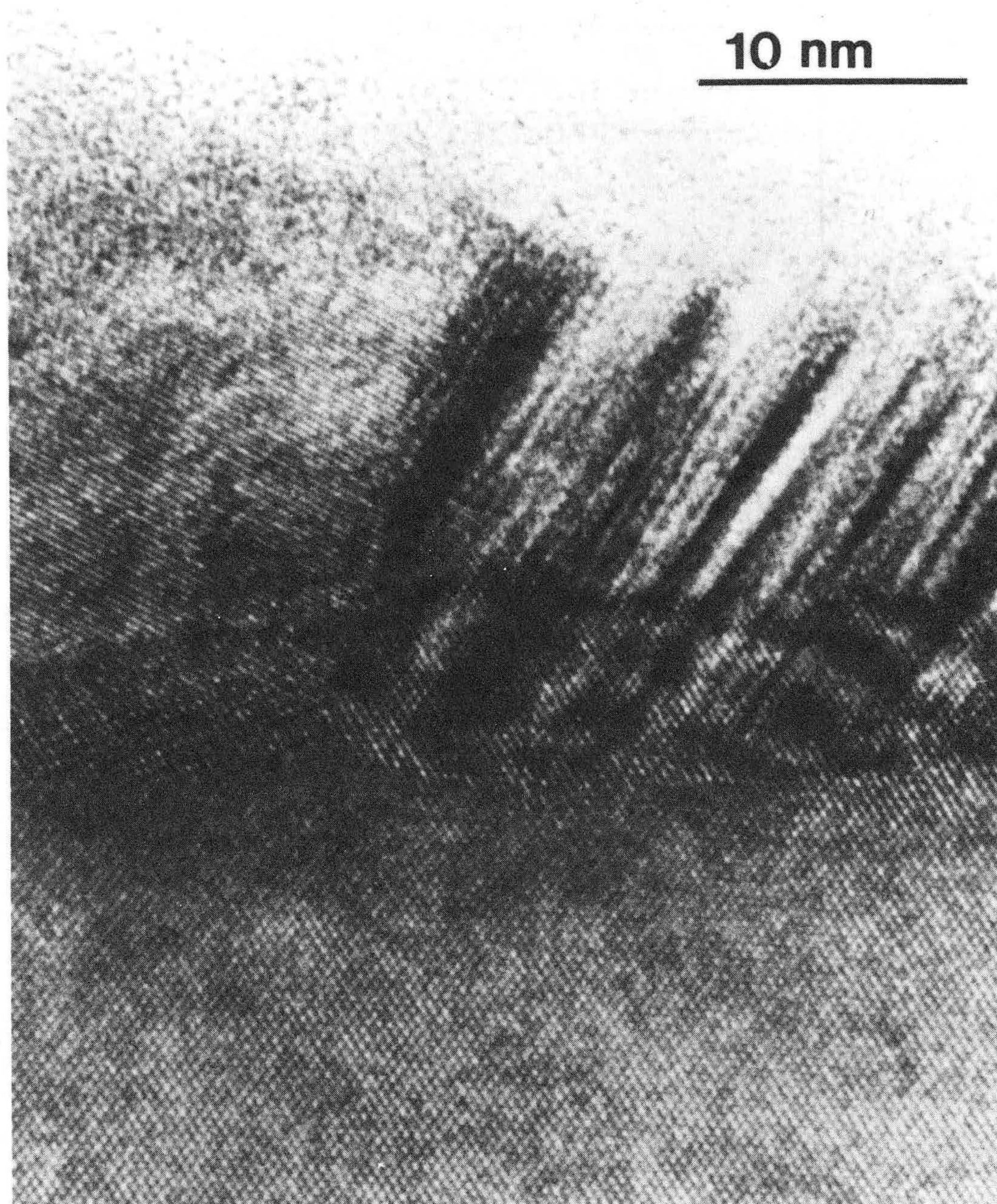

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Fig. 16. High-magnification cross-sectional micrograph from the Nb/GaAs sample annealed at 700°C for 10 seconds. Note the microdefects in the reacted film near the interface.

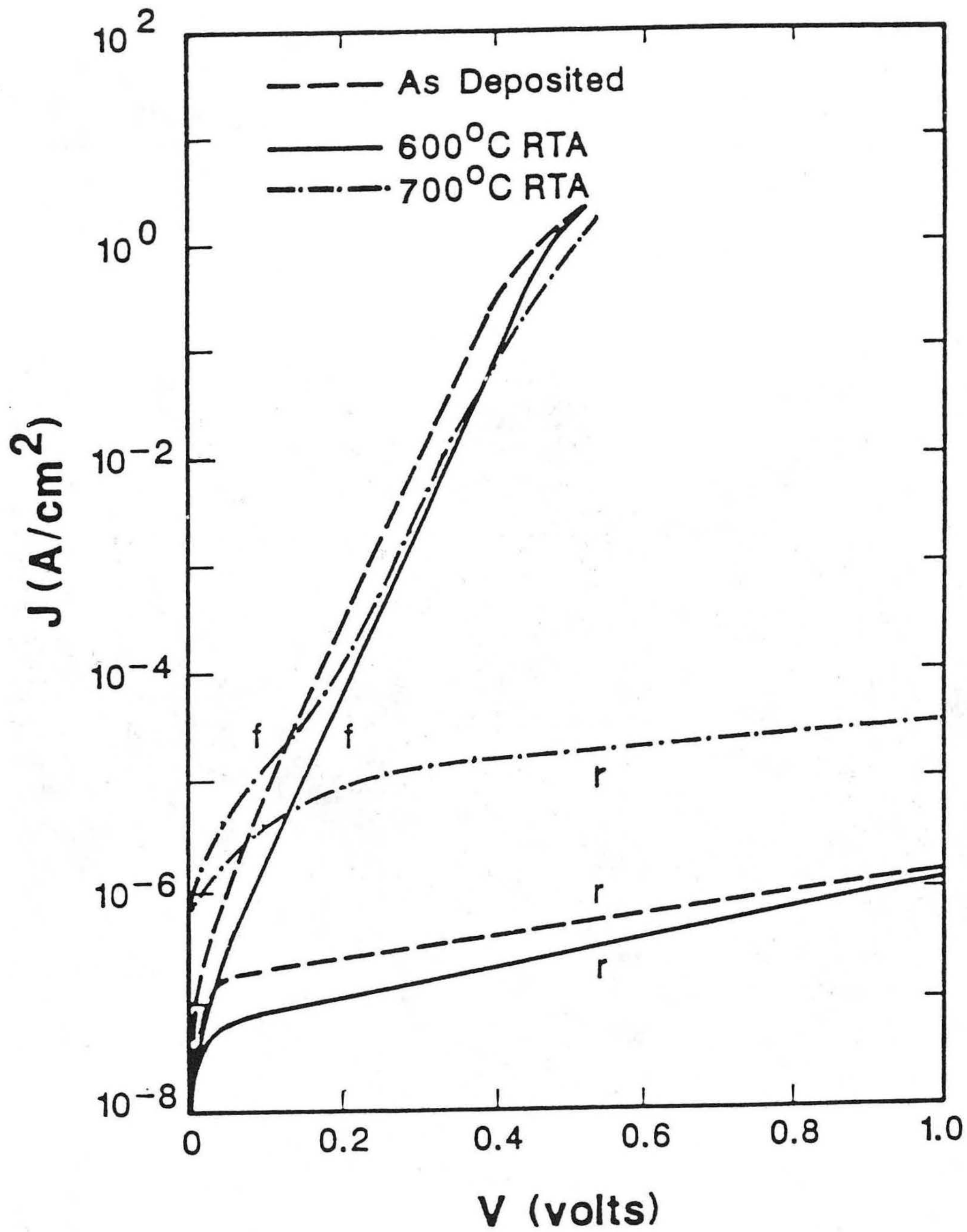


Fig. 17. I-V curves for the Nb/GaAs diodes before and after RTA at 600°C and 700°C for 10 seconds. (From Ref. 5)

the ideality factor much, but reduced reverse leakage current and increased the Schottky barrier height of the diode. The improvement of electrical characteristics of the diode after 600 °C RTA is in good agreement with what was expected from the interface morphology study. Since a sharp and uniform interface without intervening oxide layer was obtained after 600 °C RTA, the diode behaves like an ideal Schottky barrier. An I-V characteristic with an ideality factor of 1.03 and a Schottky barrier height of 0.78 eV was achieved.

After 700 °C RTA, the electrical properties were deteriorated as shown in the lnI-V plot (Fig. 17). As can be seen from the plot, the increase of reverse leakage current by more than an order of magnitude is accompanied by a significant increase of ideality factor (1.59) and a decrease of the Schottky barrier height (0.69 eV). This appears to have been due to an interface reaction resulting in phases with a high density of defects and nonuniform interface as shown in Fig. 10b. These microdefects across the thin film can cause a large reverse leakage current and decrease the Schottky barrier height and breakdown voltage. Due to the imperfections at the interface, an "excess" current different from the ideal thermionic-emission current was found at small forward bias ($V < 0.3$ V) shown in Fig. 17. Newman et al. have related this "excess" current to imperfections at the interface and at the periphery of the diode.[104]

3.1.3. Discussions

Effect of Native Oxide

During the fabrication of Schottky contacts in a typical device, there is generally a thin native oxide film present on the surface of the GaAs substrate after chemical cleaning. The question naturally arises as to interface chemistry during Schottky-barrier contact formation in the presence of this native oxide layer. Furthermore, the development of VLSI devices and fast devices such as MESFET's requires very small devices, with active regions as small as 5 to 20 nm. The constraints imposed by small demensions on

reliably fabricating such devices make it necessary to understand the microchemical processes occurring at the metal-contaminants-GaAs interfaces.

Based on previous experience,[103] a native oxide layer of 1~2 nm in thickness was expected on the chemically cleaned GaAs surface. This thin film contains mixed oxides of both Ga_2O_3 and As_2O_3 as well as free arsenic. Unlike SiO_2, Ga_2O_3 and As_2O_3 are poor electrical insulators, and also poor in their ability to provide protection of the semiconductor surface. They are also thermally unstable. Consequently, they cannot be used in GaAs technology as diffusion mask, gate oxide and passivation layers as is SiO_2 in Si technology.

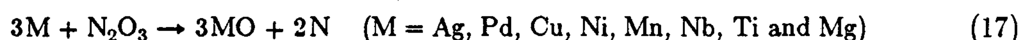
The presence of this interfacial layer of contamination was found to result in poor quality adhesion of thin film metallization to substrates since the adhesion strength of metallization deposited on these chemically prepared surfaces is weakened by the native oxides.[105–107] These native oxides could also cause a certain degree of degradation in the electrical characteristics, such as Schottky barrier height and ideality factor of the doides, upon annealing. The studies have shown that this native oxide layer is sufficient to locally disrupt metal/GaAs reactions and result in the development of a nonuniform interface during annealing. For example, the rough interface of the Nb/GaAs system after annealing at 700°C may result from the nonuniformity of the native oxide layer at the interface since this nonuniform oxide layer could result in faster diffusion and dissolution at the regions where pinholes or thin areas exist. The native oxide layer was also detrimental to the structural perfection of the phases formed on the GaAs substrate after annealing. In the case of the Nb/GaAs reaction, the microtwins and stacking faults in the film are formed to accomodate the nonuniform interface, so as to achieve a lower interfacial energy as shown in Fig. 16.

Kowalczyk et al.[108] examined chemical reactions between deposited metals and the native oxide on GaAs by using x-ray photoemission spectroscopy. It has been reported that the chemical reactivity for the formation of a metal oxide and the reduction of the

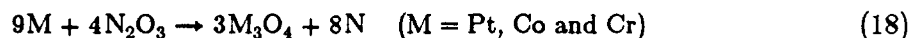
native oxides (Ga_2O_3 and As_2O_3) at room temperature can be simply and reliably predicted by the change of Gibbs free energy of formation ΔG_o.[109] The reactions between the native oxides, N_2O_3 (N = Ga or As), and reacting metal species, M, can be classified into four categories based on the formula of the metal oxides. These four categories are:

$$2M + N_2O_3 \rightarrow M_2O_3 + 2N \quad (M = \text{Au, In and Al}) \tag{15}$$

$$3M + 2N_2O_3 \rightarrow 3MO_2 + 4N \quad (M = \text{Mo, W and Zr}) \tag{16}$$



$$3M + N_2O_3 \rightarrow 3MO + 2N \quad (M = \text{Ag, Pd, Cu, Ni, Mn, Nb, Ti and Mg}) \tag{17}$$



$$9M + 4N_2O_3 \rightarrow 3M_3O_4 + 8N \quad (M = \text{Pt, Co and Cr}) \tag{18}$$

These reactions between the native oxides and the deposited metals could occur only if the change of Gibbs free energy is negative, i. e., $\Delta G_o < 0$. Table 2 lists the Gibbs free energies of formation of the native oxides (Ga_2O_3 and As_2O_3) and the most stable metal oxides.

In the case of the Nb/GaAs contact, the formation of Nb oxides at room temperature is thermodynamically favored since the heats of formation per oxygen atom for Nb oxides are higher than those of Ga or As oxides as shown in Table 2. Therefore, the as-deposited Nb would be expected to react with the native oxides Ga_2O_3 and As_2O_3 on the substrate to form Nb oxides at the Nb/GaAs interface. Yu et al.[110] reported that the newly formed oxides at the Nb/GaAs interface are the suboxides of Nb, i. e., Nb_2O or NbO_2, instead of Nb_2O_5. These Nb suboxides were reported to be good conductors.[111] Their formation produces a more intimate electrical contact to GaAs without an insulating layer present at the interface. This more intimate contact between the as-deposited Nb and the GaAs substrate ensures thermionic emission to be a dominant mechanism for carrier transport over the barrier. This probably explains the fact that excellent I-V characteristics with the ideality factor close to unity are observed without RTA and they change only very slightly after RTA at temperatures up to 600 °C.

Table 2. Summary of interfacial chemistry for several metals deposited on native oxide surfaces of GaAs.

Metal	Reaction with the native oxide ($Ga_2O_3 + As_2O_3$) predicted[a]	Oxide Products	ΔG (Kcal/mol)[b] Reacted with Ga_2O_3	ΔG (Kcal/mol)[b] Reacted with As_2O_3	ΔH (kcal/mol)[b] Heat of Formation of M_xO_y per oxygen	X (element)[c] Electronegativity (Pauling Scale)
Au	No	Au_2O_3	278.0	177.0	−0.72	2.54
Ag	No	AgO	249.0	148.0	−2.7	1.93
Pt	No	Pt_3O_4	—	—	−9.8	2.28
Pd	No	PdO	—	—	−20.0	2.20
As	—	As_2O_3	—	—	−50.3	2.8
Ni	No	NiO	83.5	−17.2	−51.7	1.91
In	No	In_2O_3	40.1	−60.0	−73.8	1.78
Ga	—	Ga_2O_3	—	—	−86.2	1.81
Cr	Yes	Cr_2O_3	−11.0	−112.0	−90.0	1.66
Nb	Yes	NbO	—	—	−97.0	1.60
Ti	Yes	Ti_2O_3	−107.0	−208.0	−122.0	1.54
Al	Yes	Al_2O_3	−138.0	−239.0	−133.3	1.61

[a]Prediction based on thermodynamic data presented in this table.

[b]The free energies used to calculate the ΔG's were obtained from Handbook of Chemistry and Physics, 64th ed., edited by R.C. Weast (CRC Press, Florida, 1983) and Lange's Handbook of Chemistry, edited by J.A. Dean (McGraw-Hill, New York, 1979).

[c]"Table of Periodic Properties of the Elements," Sargent-Welch Scientific Company, 1980.

Orientation Relationship

A different orientation relationship for the Nb/GaAs contact compared to the current study was reported by Eizenberg et al.[112] in 1986 as: $(100)_{Nb}//(100)_{GaAs}$ and $[001]_{Nb}//[011]_{GaAs}$. In their experiment, thin Nb layers (10~40 nm) were deposited on (100) GaAs substrates by electron beam evaporation in a MBE system under UHV conditions (~5 X 10^{-10} Torr), i. e., the Nb/GaAs interface is native oxide free. Therefore, it is not surprising that the orientation relationships of the two as-deposited Nb/GaAs systems are different because of the different surface preparation and deposition techniques in the two studies. In their case, a clean substrate prepared by MBE under UHV conditions ensured an epitaxial deposition of the Nb thin film. In the current case, a chemically cleaned and therefore air exposed substrate was used as shown in Fig. 9c where a native oxide layer (1~2 nm thick) appears at the as-deposited Nb/GaAs interface.

Many metal-GaAs systems such as Au/GaAs and Al/GaAs contacts[113] have also shown that the orientation relationship between the metal and the substrate is different for clean surfaces compared to oxide contaminated surfaces. One of the reasons for this difference has been attributed to the epitaxial formation of γ-Ga_2O_3 on GaAs substrates as soon as the substrates are exposed to air.[113-115] Therefore, the as-deposited metals have been considered to be epitaxially related to this native oxide layer.[113] In many cases, this thin γ-Ga_2O_3oxide layer (1~2 nm thick) which itself grows epitaxially on the GaAs substrate could conceivably help to grade the interfacial mismatch between the as-deposited film and the substrate.

The orientation relationship in this study can be attributed to the results of both the low interfacial energy resulting from the small lattice mismatch between the as-deposited thin film and the substrate and the growth kinetics. Assuming that the native oxide existing at the interface had an epitaxial relation with the substrate, the mismatches between the lattice planes of the thin film and the substrate can be calculated according to the equation $f=(d_f-d_s)/d_{avg}$, where d_f is the unstrained plane spacing of the thin film, d_s

is the corresponding plane spacing of the substrate and d_{avg} is the average of d_f and d_s. In the present case, the result of the calculation shows the mismatches at the Nb/GaAs interface to be 4.6% between $(111)_{Nb}$ and $(220)_{GaAs}$. This is the low value relative to other possible combinations of low index lattice spacings in this system. Note that a spread (~15 °) of the Nb 110 reflections in the diffraction pattern (Fig. 9b) indicates the arrangement of the interface structure which gives a low energy configuration for the system. On the other hand, it is well known that in the absence of any strong orienting effects of the substrate the growth textures of bcc metals are fiber textures with fiber axes {110} which is the most closely packed plane for bcc. Since Nb has a bcc structure, the growth textures of the bcc Nb on the GaAs substrate have texture axes <110> which might be one of the reasons for the present orientation relationship.

Nb/GaAs Reaction Mechanism

The stable and equilibrium configuration of the Nb/GaAs reaction products was reported by Schulz et al.[116] in 1988. The results of Schulz et al. showed a diffusion path determined after the bulk Nb/GaAs diffusion couples were annealed at 600 °C for seven days. The diffusion path is defined as a stable configuration which a series of phases may form and decompose before the final stable configuration is reached, i. e., the sequence of the phases formed in the couples.[116] This diffusion path can be used to rationalize the compound formation in the thin film contact system. Initial reaction products can be thermodynamically and kinetically unstable relative to the final stable configuration.

The Nb-Ga-As phase diagram has been studied theoretically by Schmid-Fetzer[117] and experimentally by Schulz et al.[116] Figure 18 shows the Nb-Ga-As ternary phase diagram of the experimental results of Schulz et al. which also suport the thermodynamic calculations by using Miedema's model reported by Schmid-Fetzer.[117] From the phase diagram, NbAs is been shown to have high relative stability. The final stable configuration for the Nb/GaAs reaction at temperatures above 600 °C for seven days has been found to be Nb/NbAs/$NbGa_3$/GaAs. As can be seen from the phase diagram, no

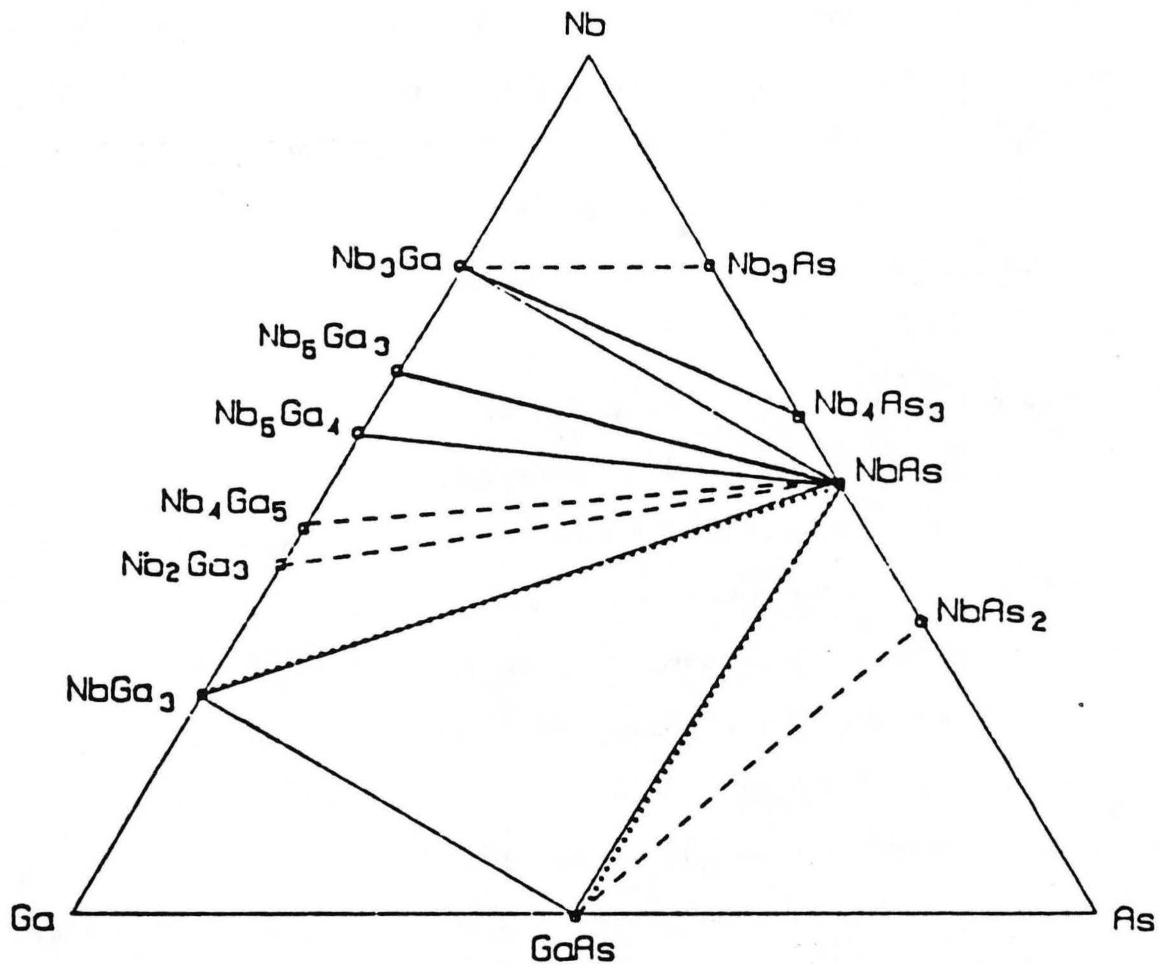


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Fig. 18. Nb-Ga-As phase diagram. Dashed lines indicate tie-lines not substantiated experimentally. Dotted lines indicate Nb/GaAs thin film diffusion path. (From Ref. 116)

ternary phases were expected. Therefore, at least two binary phases should be formed during annealing in order to consume equal amounts of Ga and As from the substrate. As discussed by Schulz et al.[116], Ga atoms are expected to diffuse rapidly into the metal thin film. This would leave excess As atoms at the interface which react with Nb to form Nb_4As_3 in contact with the GaAs substrate during the initial transition period. Some Nb_5Ga_3, Nb_5Ga_4 and $NbGa_3$ were also expected during this period. These are in good agreement with this study since only 10 seconds annealing time was used for RTA annealing so that the system can be considered in an initial transition stage of this Nb-GaAs reaction after the RTA annealing.

For 10 seconds annealing time, the interface morphology will be determined by the growth kinetics of the phases in the "diffusion couple". Therefore, the growth of Ga-Nb and Nb-As phases is controlled by the diffusion of Ga and Nb. Since the "diffusion couple" consisted of a thin film of Nb on GaAs, the overall compositon of the system could shift along the vertical line segment connecting Nb and GaAs into the three-phase region GaAs-$NbGa_3$-NbAs at point B. The initial and transient phase configurations would undoubtely be influenced by surface condition of the substrate and strain energy (lattice mismatch) which can create nucleation barriers, especially in the thin film case. The final stable configuration for the thin film couple would be GaAs/$NbGa_3$/NbAs if sufficient annealing time is given for the system to reach equilibrium. This implies that chemical stability, i. e., equilibrium thermodynamics, is the primary factor governing phase formation in these systems.

The thin film results for the M/GaAs systems are different from those measured in bulk samples.[116] The discrepancies can be due to nonequilibrium in the thin film case. Also the supply of the elemental metal in the bulk experiments is infinite within the time frame of the experiment while the supply of the elemental metal in the thin film experiment is not. Note also that the final phase morphology is not layered as was reported for the bulk diffusion couple.[116] The final morphology of the thin film system, is probably not

layered because of nonuniform growth/decomposition of the transient phases. The nonuniform growth of phases at the interface can result from the nonuniform oxide layer which would cause local regions of faster diffusion and dissolution.

3.2. Refractory Metal/GaAs Contacts

3.2.1. NbN/GaAs Contacts

Interface Morphology

The plan-view micrograph in Fig. 19a shows that the as-deposited niobium nitride is polycrystalline with an average grain size of about 6 nm. The as-deposited phase on the GaAs substrate was identified to be tetragonal Nb_4N_3 by both the electron diffraction and x-ray diffractometry techniques. The plan-view micrograph and electron diffraction pattern in Fig. 19b reveal that a new phase, hexagonal NbN with lattice parameters a=0.2986 nm and c=0.5548 nm, was formed in the deposited film during annealing at 800 °C and comprises a majority of the film since the intensity of the rings from this phase is higher than those from other phases.

The plan-view TEM image in Fig. 19b also shows the microstructure of this thin film; large elongated and randomly distributed grains were formed with small grains in between them during 800 °C annealing. The large grains have an average size of 70 nm while small grains have an average size of 9.2 nm. Note that the grain size of the new phase is about ten times larger than that of the as-deposited phase. These large elongated grains were identified to be NbN. Selected area diffraction pattern in Fig. 20 from one of these large elongated grains shows this NbN phase in $<\overline{3}11>$ zone-axis orientation. The faint rings in the diffraction pattern shown in Fig. 20 were found to be from Nb_4N_3. This indicates that not all the as-deposited phase had transformed to NbN; annealing at 800 °C for only 10 seconds may not be long enough to complete the phase transformation from Nb_4N_3 to NbN. Other rings can be assigned to pure Nb, indicating

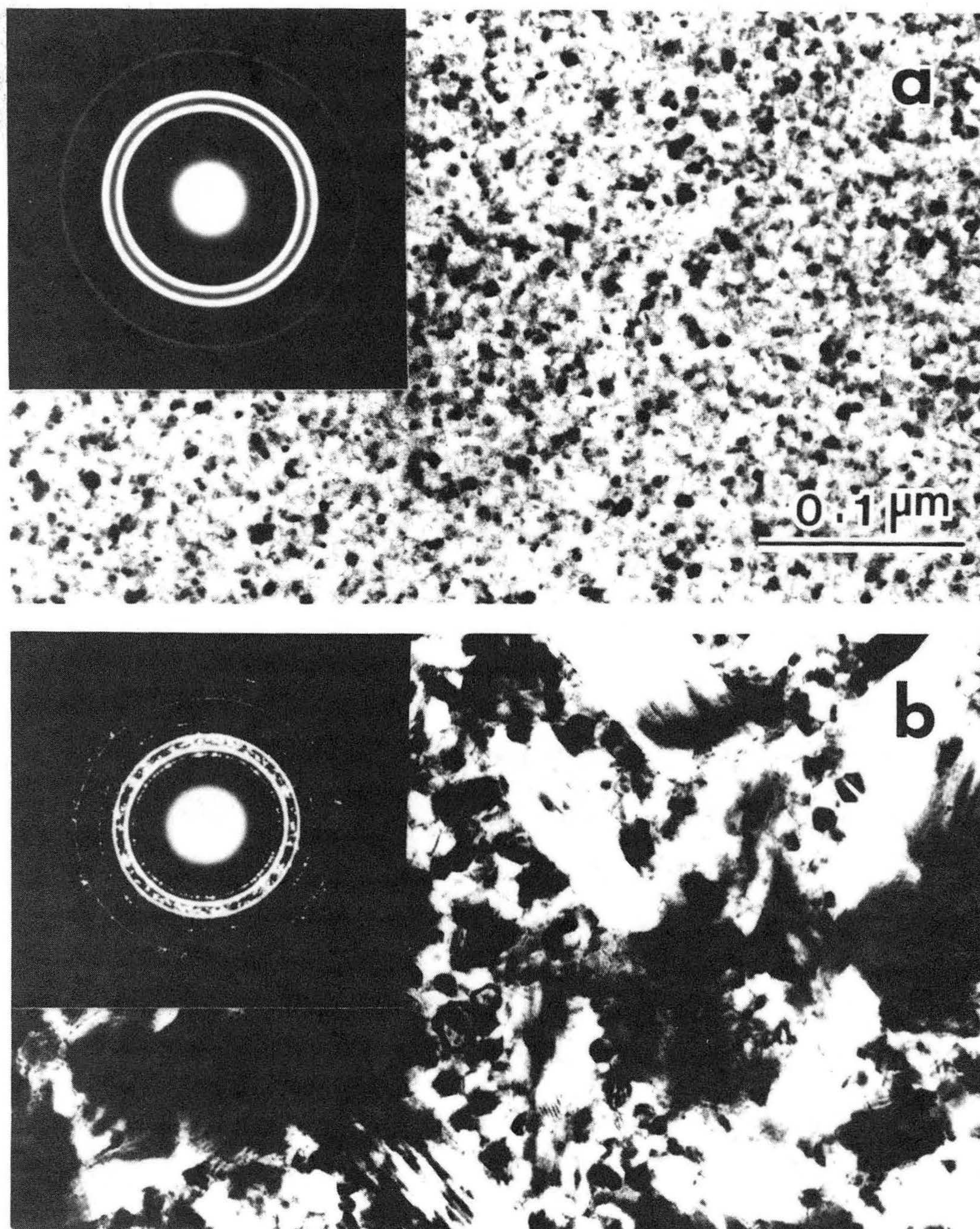

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Fig. 19. Plan-view TEM images and corresponding electron diffraction patterns of the NbN/GaAs (a) as-deposited sample and (b) the sample annealed at 800°C for 10 seconds.

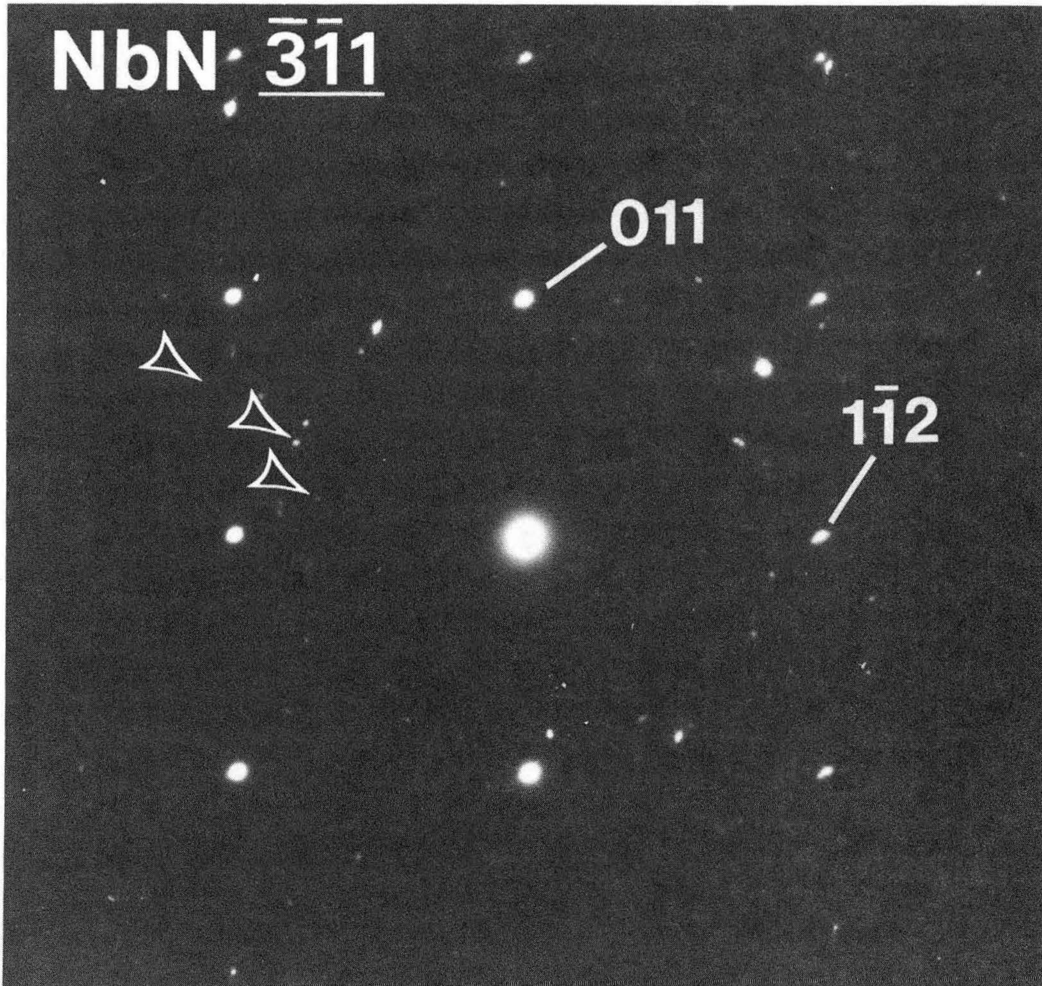

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Fig. 20. Electron diffraction pattern from a NbN grain with a [$\bar{3}\bar{1}1$] zone axis (the sample annealed at 800°C for 10 seconds).

that small Nb particles were also formed during the annealing, probably as a result of the reaction $Nb_4N_3 \rightarrow 3NbN + Nb$. Therefore, small grains between the large elongated NbN grains are believed to be untransformed Nb_4N_3 and Nb.

The interface morphologies of NbN/GaAs samples before and after annealing are shown in cross-sectonal TEM images in Fig. 21. For the as-deposited sample, the interface was flat and there was a thin native oxide layer at the interface. After annealing at 800 °C for 10 seconds by RTA, the interface became sharper and a thin intervening layer (about 1 nm) is visible at the interface as a white band [Fig. 21b]. It is suspected that this intervening layer may be a result of a reaction between free Nb and the native oxide to form Nb suboxides since the native intervening oxide present on the GaAs surface may likely be reduced by the Nb to form Nb suboxide.[110] No significant interdiffusion is observed between the NbN thin film and the GaAs substrate at this annealing temperature. An alternative explanation for the thin light band is that it represents the first appearance of a new interfacial phase due to interface interdiffusion.

For the sample annealed at 850 °C, the cross-sectional image in Fig. 21c indicates that the sample has a uniformly layered structure with a thin intervening layer formed between the thin film and the GaAs substrate. The thickness of this intervening layer was estimated to be about 2 nm. The noted difference in film thickness is due to an artifact of TEM sample preparation. The selected area diffraction technique was used to identify the new transformed phase in the thin film. The diffraction pattern shown in Fig. 22a was taken from the interface region, and shows the superimposed diffraction patterns from the <110> GaAs substrate and a single grain of the new transformed phase in the thin film. This diffraction pattern reveals that the newly transformed phase is Nb_3N, which has a $[\bar{6}19]$ zone axis. Other spots in this pattern also belong to Nb_3N, and they are not in a low index zone axis. Another example is shown in Fig. 22b, where a diffraction pattern from Nb_3N with a $[\bar{9}23]$ zone axis is superimposed on the GaAs <110> pattern. Nb_3N has a tetragonal structure with lattice parameters $a_o = 0.8742$ nm and b_o

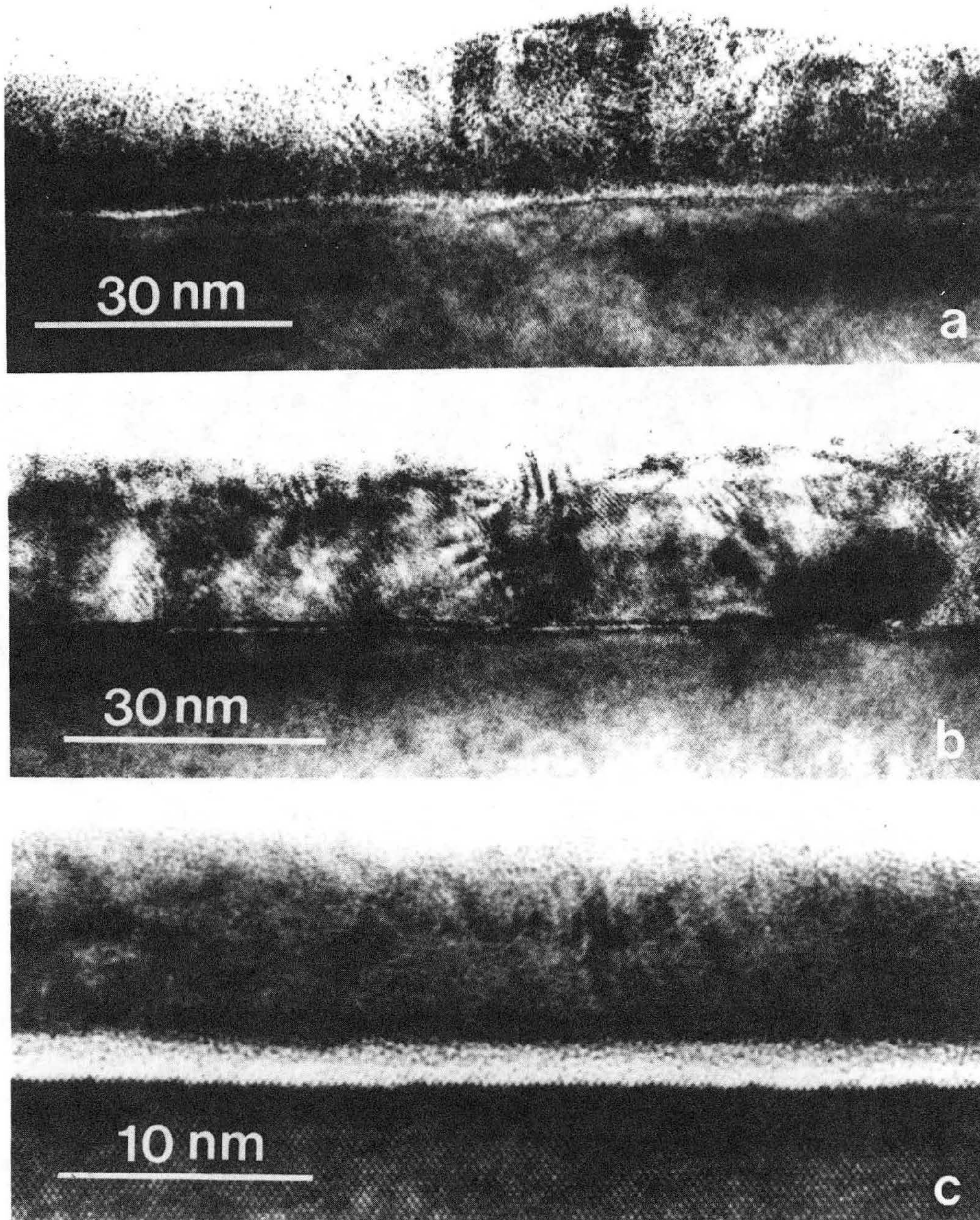

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Fig. 21. Cross-sectional TEM images of the NbN/GaAs (a) as-deposited sample, (b) annealed at 800°C, and (c) the sample annealed at 850°C for 10 seconds.

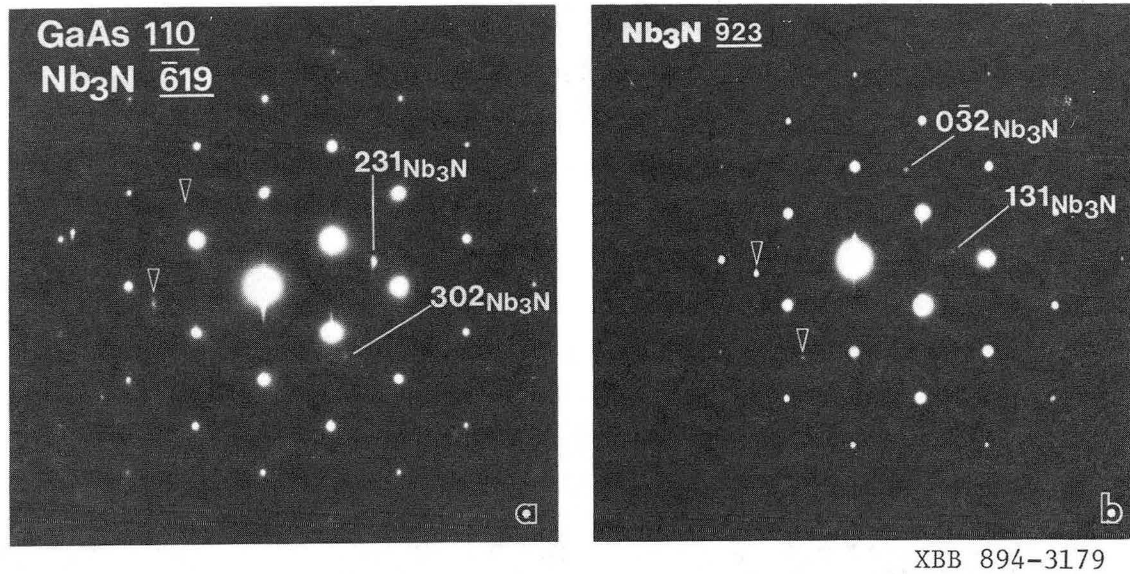

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Fig. 22. Electron diffraction patterns from the interface area of the NbN/GaAs samples annealed at 850°C for 10 seconds. (a) and (b) show that the diffraction patterns from two Nb_3N grains are superimposed on the [110] GaAs pattern.

$= 0.8592$ nm.

It can also be seen from these diffraction patterns that streaks are visible along the GaAs [100] direction and pass through 000 and other GaAs diffraction spots. As a result of the crystal shape effect, these streaks can be attributed to the thin intervening layer acting as a thin platelet parallel to the GaAs (100) plane. This effect is based on the basic theory of diffraction from thin crystals.[118] The reciprocal lattice points for a crystal in the form of a thin plate are elongated along the direction normal to the plate, to give reciprocal lattice spikes. The high resolution TEM image in Fig. 21c shows that the GaAs substrate extends into amorphous-like interfacial layer. This explains the existence of streaks on the GaAs diffraction spots as being a result of the thin "strain free" layer of GaAs with a difference in scattering amplitude.

It has been difficult to identify the interfacial phase, which appears as a white band, because it is still very thin (~2 nm) and covered by a thicker Nb_3N layer. The XPS technique was also used in an effort to identify this layer but it was unsuccessful. However, XPS data indicates a certain amount of nitrogen in the GaAs substrate close to the interface region. This suggests that diffusion of nitrogen atoms into the GaAs substrate occured during 850 °C annealing. These nitrogen atoms were considered to result from the phase transformation occurring during annealing ($Nb_4N_3 \rightarrow 4Nb_3N + 5N$). It is not surprising that nitrogen atoms were found in the GaAs substrate since the size of a nitrogen atom is smaller than the open GaAs <110> channel so that the activation energy for the diffusion of nitrogen atoms in GaAs should be small.

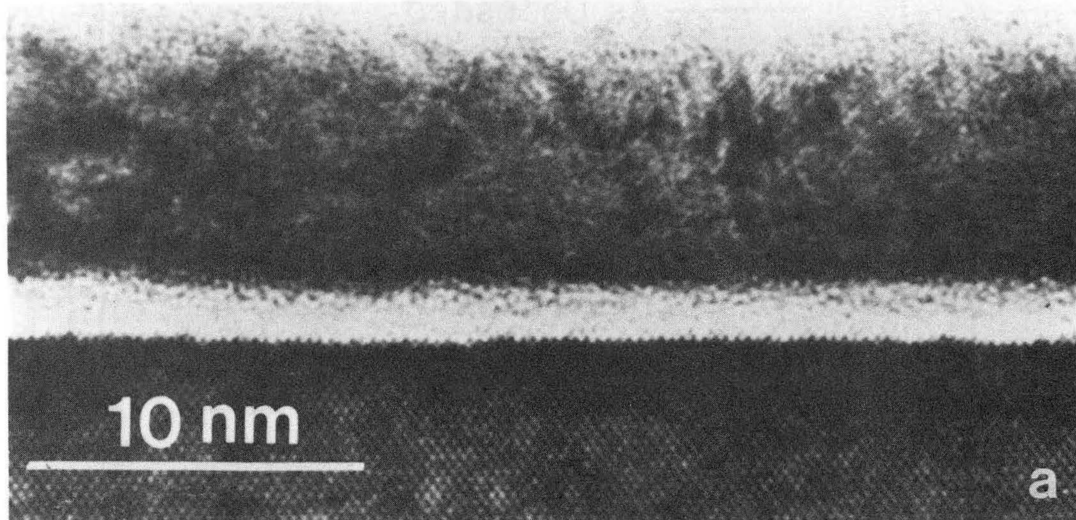
In a further effort to identify this interfacial phase, an optical diffraction study of the lattice image was also performed. Optical diffraction from a lattice image resembles electron diffraction and it can be obtained easily from small areas of the lattice image. For this purpose, the TEM lattice image shown in Fig. 21c was used to record optical diffraction patterns. Figure 23 shows optical diffractograms taken from ~10 nm diameter areas within the GaAs substrate (b), and the interface region (c) in the micrograph of Fig.

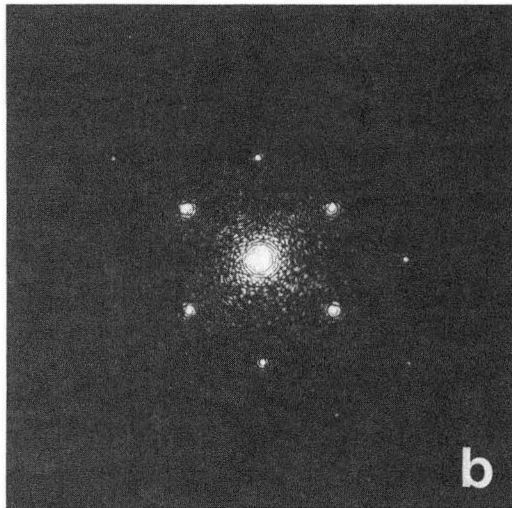
23a. The optical diffractogram in Fig. 23b shows a GaAs diffraction pattern with [110] zone axis as expected. The optical diffractogram in Fig. 23c was taken from the interface region which includes the GaAs substrate, intervening layer and the Nb_3N thin film. It shows the GaAs [110] diffraction pattern with streaks along the [100] direction and diffraction spots close to <111> GaAs reflections. The diffraction spots in this optical diffractogram were found to correspond to a d-spacing of 0.2504 nm and were indexed as [222] Nb_3N reflections. Note also that the diffraction spots are well aligned along one set of <111> planes (only a few degrees off). This information from the optical diffractogram is in excellent agreement with the measurements from the lattice image in Fig. 23a, where the lattice spacing in Nb_3N film measured to be 0.251 nm and the lattice planes are aligned along one set of the GaAs <111> directions. No information from the interfacial layer was found in this optical diffractogram except the appearence of the streaks on the GaAs spots. Even the exact composition of this intervening layer remains unknown. However, it is expected that Nb and/or nitrogen is present in this intervening phase due to interdiffusion at the NbN/GaAs interface.

Electrical Properties

The I-V characteristics[5] of the NbN/GaAs contacts before and after RTA to 800 °C and 850 °C are shown in Fig. 24. Compared to the Nb/GaAs contacts where the electrical characteristics degraded after annealing at temperatures above 600 °C, the I-V characteristics of the NbN/GaAs contacts improved upon RTA up to 800 °C with an enhancement of Schottky barrier height, a decrease of reverse leakage current density, and an ideality factor close to unity.

For the as-deposited sample, the intervening native oxide layer, with a thickness variation across the NbN/GaAs interface, apparently is one of the reasons for the poor I-V characteristics. Another possible reason for poor I-V characteristics is lattice damage of the GaAs surface caused by sputtering deposition of the NbN thin film. The combination of these effects could lead to the low Schottky barrier height (0.57 eV) and significant





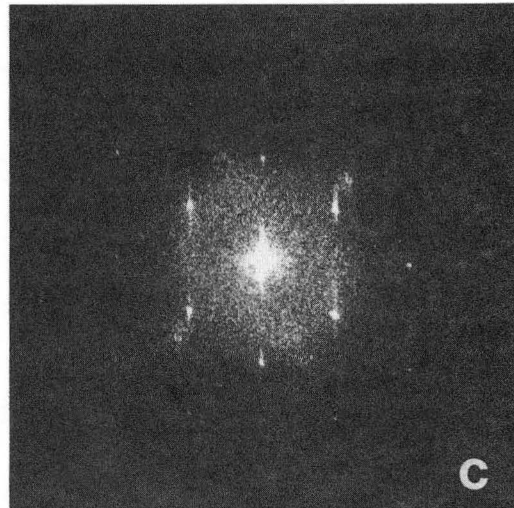


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Fig. 23. (a) High-resolution cross-sectional TEM image of the NbN/GaAs sample annealed at 850°C for 10 seconds, and the optical diffractograms from (b) the GaAs substrate and (c) the interface area of the TEM micrograph in (a).

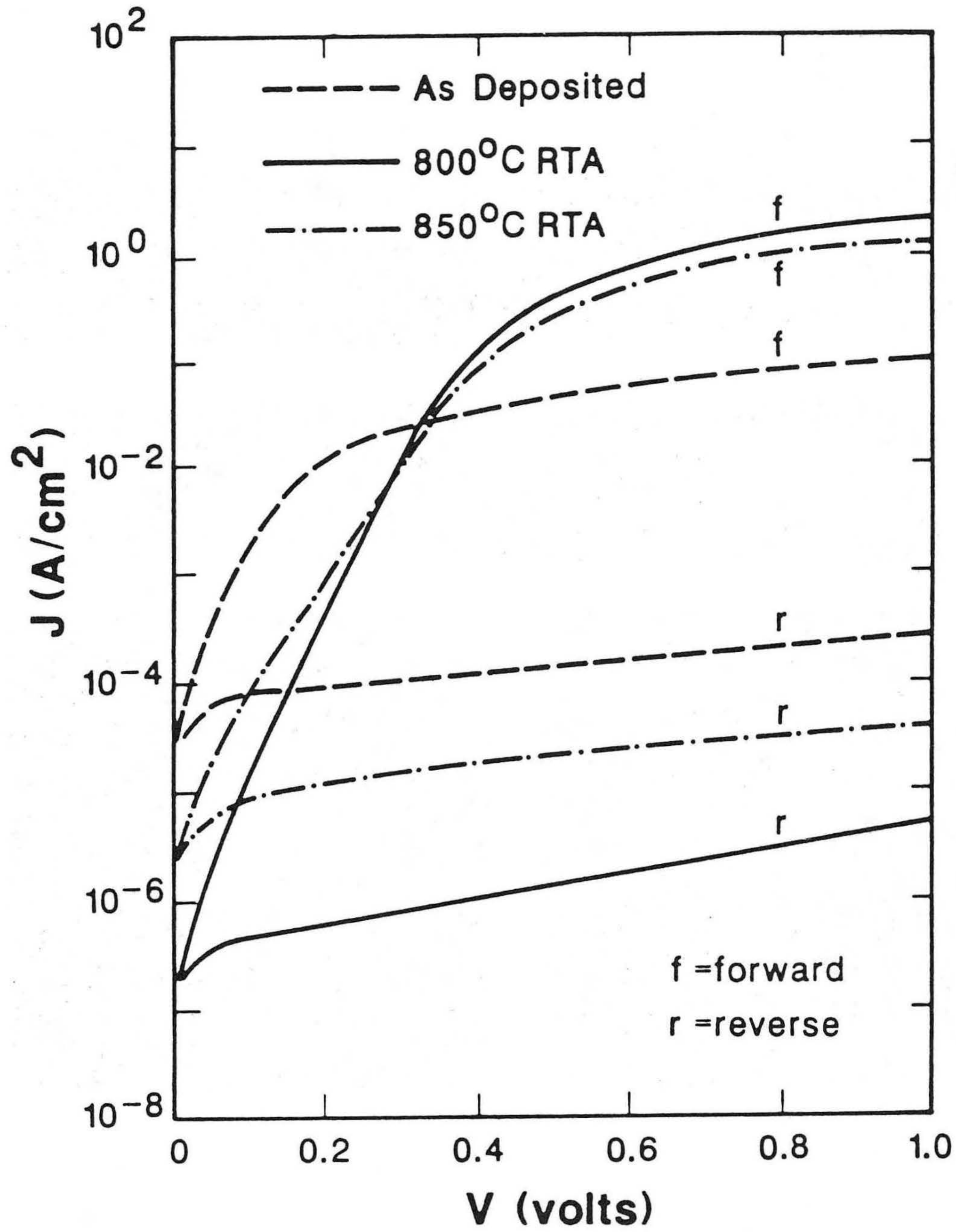

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Fig. 24. I-V curves for the NbN/GaAs diodes before and after RTA at 800°C and 850°C for 10 seconds. (From Ref. 5)

departure of ideality factor n from unity (1.74).

After annealing at 800 °C by RTA, the improvement of the NbN/GaAs electrical contact was probably the result of a sharper NbN/GaAs interface and thermally activated removal of any lattice damage caused by the NbN sputtering deposition. If the thin white band at the NbN/GaAs interface is a suboxide of Nb as discussed before, it may produce a more intimate electrical contact to the GaAs because the suboxides are good conductors.[111] Even if this intervening layer is not Nb suboxide instead of the first apparence of a new phase due to interface interdiffusion, it is still too thin (< 1 nm) for this layer to cause the degradation of the I-V characteristics. This is consistent with the measured improvement of the ideality from 1.74 to 1.06 and increase of barrier height from 0.57 to 0.73 eV. The decrease of the reverse leakage current by nearly two orders of magnitudes is accompanied by a significant increase in Schottky barrier height after annealing at 800 °C. The high temperature chemical stability of the NbN/GaAs interface up to 800 °C is advantageous for the fabrication of MESFET' devices.

Electrical degradation for the NbN/GaAs contacts occurred after annealing at 850 °C as shown in Fig. 24. This degradation shows a decrease of barrier height from 0.73 to 0.66 eV, a departure of ideality factor from unity (1.51), and an increase of reverse leakage current by more than one order of magnitude. It is suspected that the new intervening layer formed at the interface during 850 °C annealing can be the cause the deterioration of electrical characteristics of this contact. Because this intervening layer is relatively thick (~ 2 nm), thermionic emission cannot be the dominant carrier transport mechanism for the diode. This is suggested by its poor I-V characteristics with an ideality factor of 1.51.

3.2.2. TiN/GaAs Contacts

Titanium nitride, TiN, is a member of the fourth to sixth group transition metal mononitrides and monocarbides which crystallize with the B1 (NaCl) structure.[59] This

class of materials has a unique combination of properties including extreme hardness, high melting temperature (2000~4000 °C), low electrical resistivity. Therefore, TiN has been primarily used in hard wear resistant metallurgical coatings, and in decorative coatings. Previous studies showed that TiN is also among the most promising diffusion barrier materials and is being evaluated for use in both silicon and III-V compound device technology in multilevel metallization schemes involving aluminum as the second layer.[119–121] TiN has also been considered as a promising candidate for gate material because of its low resistivity (25 $\mu\Omega$ cm) and excellent interfacial thermal stability. Recent studies by Nicolet et al.[122,123] reported that reactively sputtered TiN films are a good Schottky barrier material on GaAs. Waldrop[12] studied the electrical and interface properties of TiN/GaAs contacts made by the reactive evaporation of TiN on a heated GaAs substrate. More recent reports by Zhang et al.[13,124] on TiN/GaAs Schottky contacts showed that improved electrical characteristics have been obtained after annealing at temperatures between 500 °C and 850 °C, e. g., enhancement of barrier height and breakdown voltage. In this study, the investigation of the interfacial structure and morphology of TiN/GaAs contacts before and after annealing has been performed using transmission electron microscopy to interpret electrical characteristics of the contacts.

Interface Structure and Morphology

TiN thin films (~40 nm) were formed on Si-doped (100) GaAs substrates ($N_D = 1.5\times10^{17} cm^{-3}$) by reactive sputtering deposition in an rf-sputtering system. Samples capped with sputtered SiN_x on both sides were annealed at 500 °C, 700 °C and 850 °C in a flowing Ar ambient using a halogen lamp rapid thermal annealing system for 10 seconds. Details of sample preparation and annealing procedure were described in Chapter 2.

The interface morphology of the as-deposited TiN/GaAs samples is shown in Fig. 25a. From this cross-sectional TEM image, the TiN thin film has been found to have a thickness of about 38 nm with a columnar microstructure. Average size of the TiN columnar grains was 12 nm. The columnar grains were divided into smaller subgrains

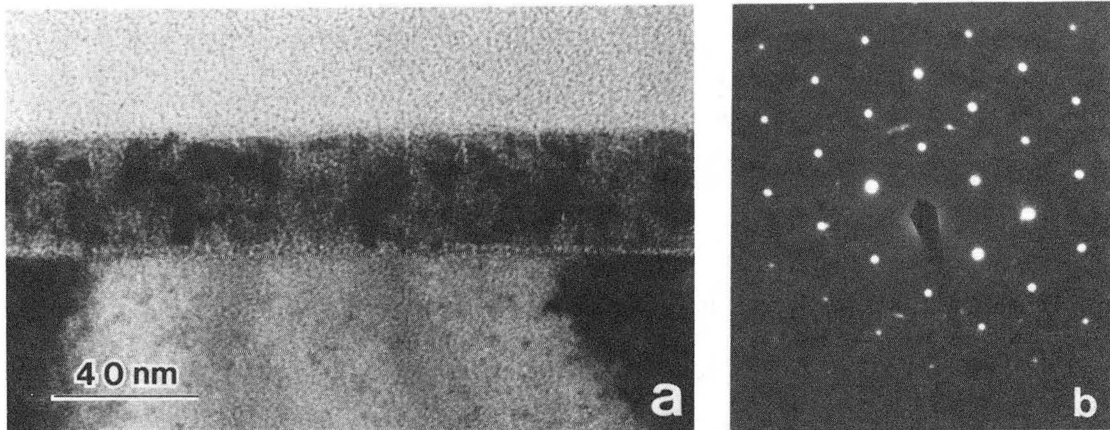

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Fig. 25. (a) Cross-sectional TEM micrograph and (b) corresponding electron diffraction pattern of the as-deposited TiN/GaAs sample.

separated by small angle grain boundaries. Optical diffraction patterns taken from such columns show a preferred orientation relationship between the TiN within one column and the GaAs substrate. The TEM image in Fig. 25a also shows that the interface of the as-deposited TiN/GaAs sample is abrupt with an intervening amorphous layer, probably native oxide between the as-deposited film and the substrate. Electron diffraction analysis revealed that the as-deposited TiN thin film had a NaCl structure with a lattice parameter a_o=0.424 nm. This can be seen in Fig. 25b where the ring pattern from the polycrystalline TiN thin film is superimposed on the GaAs diffraction pattern with a [110] zone axis.

After annealing at 500 °C for 10 seconds by RTA, the uniform interface morphology deteriorated and many pocket-like protrusions had formed beneath the interface. The size of pockets increased with increasing annealing temperature. Figure 26a shows the pockets formed at TiN/GaAs interface after annealing at 850 °C. Electron diffraction analysis revealed that the microstructure of the TiN thin film did not change even after annealing at 850 °C as shown in Fig. 26b. Nor did the grain size (~10 nm) of the TiN thin film change during annealing at 500 °C, 700 °C or 850 °C.

Detailed interface structure and morphology are shown in the high-resolution micrographs in Fig. 27. No sputtering-induced radiation damage at the as-deposited TiN/GaAs interface was seen in Fig. 27a as had been reported previously for NbN/GaAs contacts.[125] Damage from sputtering may have been annealed out during an earlier heat treatment (~450 °C) to sinter the Au-Ge contact to the back side of the substrate. Note that the intervening amorphous layer has a thickness of about 1.5 nm.

Pockets were found at the interface for the sample annealed at 500 °C as shown in Fig. 27b. The average depth of penetration of these pockets was about 4 nm with a maximum of 6 nm. The average edge-to-edge spacing between pockets was about 24 nm, giving a linear density of 40 per μm. Annealing at 700 °C increased the average pocket penetration depth to 5.3 nm, and decreased the average spacing between pockets to 23 nm.

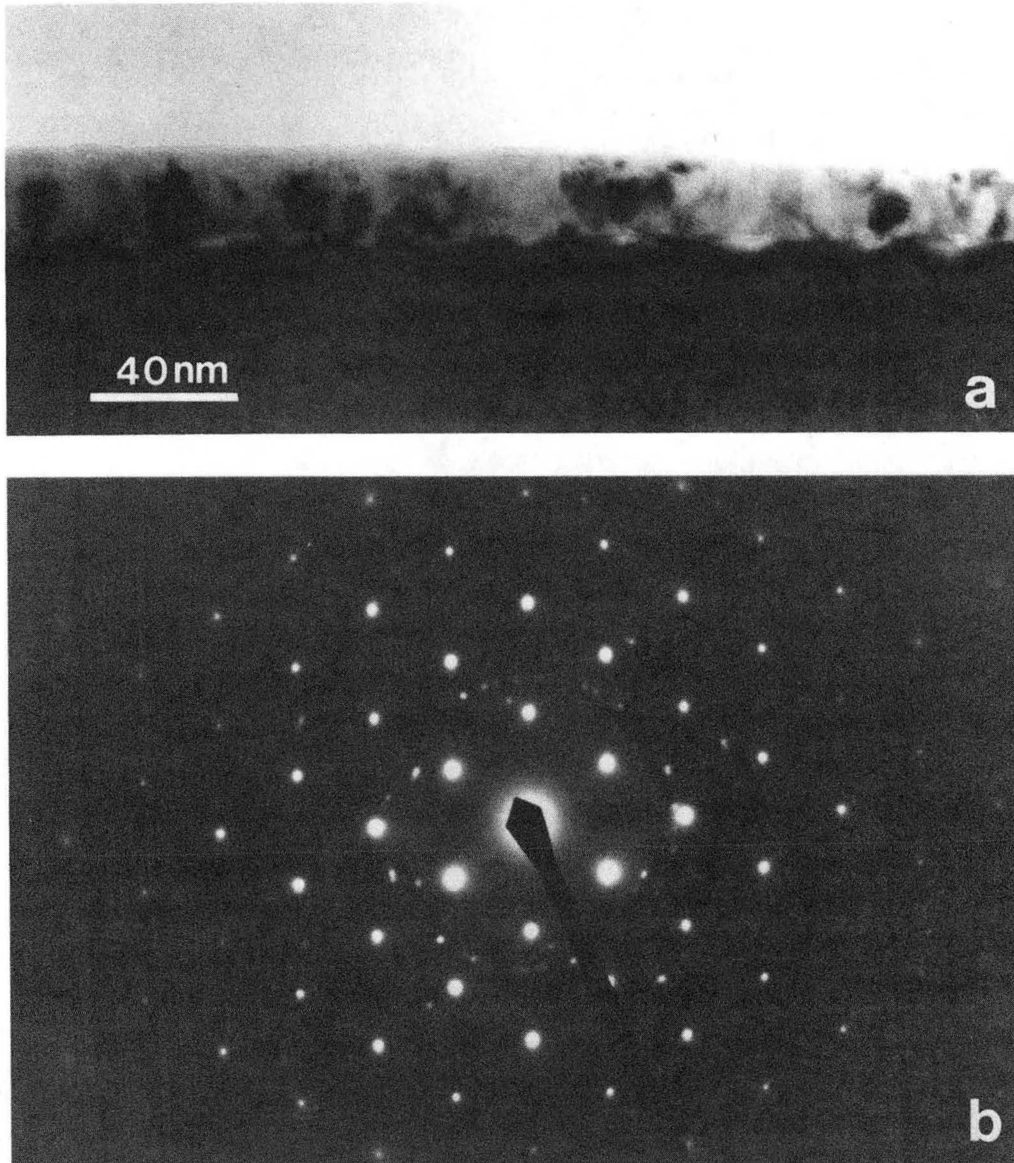

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Fig. 26. (a) Cross-sectional TEM image and (b) corresponding electron diffraction pattern of the TiN/GaAs sample annealed at 850°C.

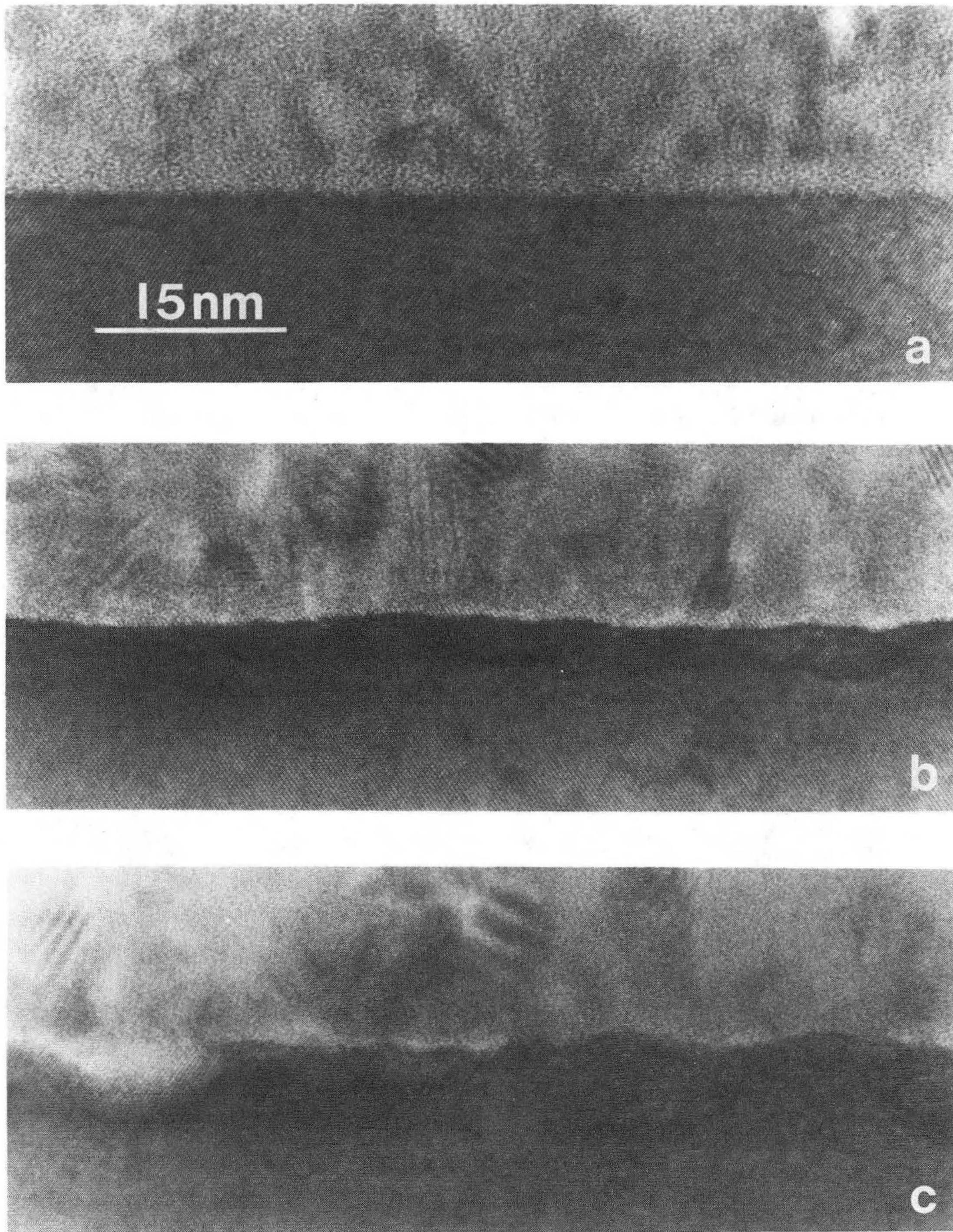

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Fig. 27. High-resolution cross-sectional TEM images of the TiN/GaAs (a) as-deposited sample, and (b) annealed at 500°C, and (c) sample annealed at 850°C.

The sample annealed at 850 °C shows that the dimension of the pockets had increased to an average depth of 6 nm; 27% of the pockets penetrated deeper than 7 nm. The maximum depth of the pockets found was 10 nm as shown in Fig. 27c on the right. The average spacing between neighboring pockets for the sample annealed at 850 °C decreased to 20 nm. For this annealing, more pockets were formed, and they penetrated more deeply than the 500 °C anneal.

High resolution images taken from the pockets show amorphous material in the thin areas of the sample or amorphous material overlapped with lattice fringes having the same lattice spacing as that of the GaAs {111} plane (0.326 nm). The maximum width of the pockets formed at the interface was about 20 nm. Since the thickness of the TEM sample at the TiN/GaAs interface region is on the order of a few tens of nanometers, it is probable that the lattice fringes are from GaAs substrate material overlapping the pockets.

Optical diffraction was performed for identification of the amorphous-like phase formed within the pockets under the interface. Figure 28 shows optical diffractograms from the GaAs substrate (b), the pocket-like protrusion (c), and the interface region (d) in the high resolution TEM image of Fig. 28a. The optical diffractogram (c) from the pocket marked by an arrow in Fig. 28a shows no evidence for any new phases. As can be seen in Fig. 28d, the [110] GaAs diffraction pattern overlaps on one set of <111> reflections of a TiN grain. This gives evidence of a preferred orientation relationship between the TiN within individual columns and the GaAs substrate.

The mechanism of the pocket formation is not clear. It is believed that no chemical reaction should occur at the TiN/GaAs interface even for the sample annealed at 850 °C since TiN has a high thermodynamic stability and low diffusivity. It can be expected that even though TiN thin films have been used widely as diffusion barriers in Si technology,[74,77] volatile arsenic atoms from the GaAs substrate may be able to escape through pinholes in the thin intervening layer at the interface, and diffuse out through the colum-

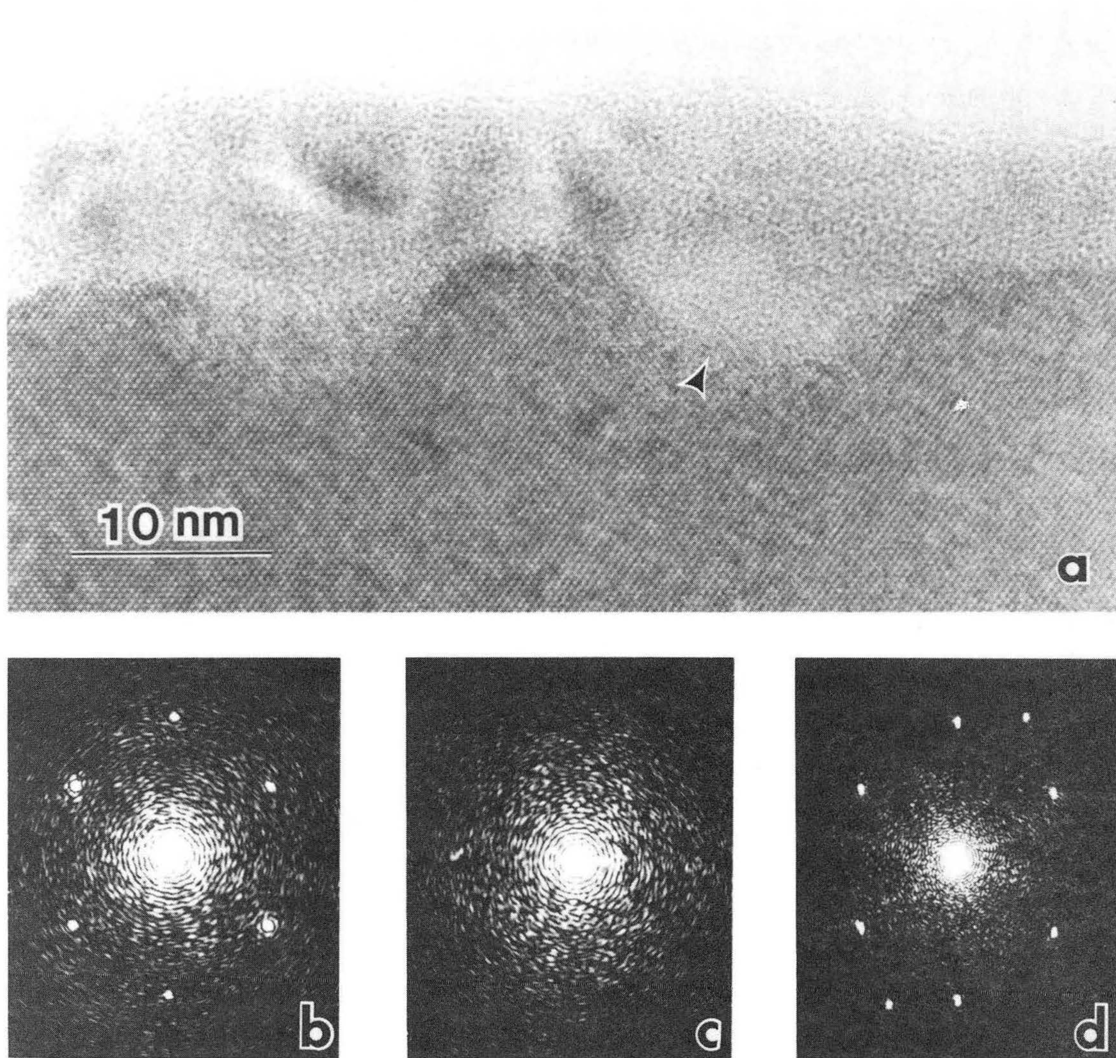

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Fig. 28. (a) High-resolution TEM image of the TiN/GaAs sample annealed at 850°C for 10 seconds, and the optical diffractograms from (b) the GaAs substrate, (c) the pocket-like protrusion (arrowed in (a)), and (d) the interface area in the micrograph in (a).

nar boundary structure of the thin film and the TiN grain boundaries during annealing at high temperatures. This extensive out-diffusion of arsenic atoms would leave excess gallium atoms at the interface near these pinholes, which might form GaN within the pocket. However, this phase was not detected by this study.

An alternative explanation for this pocket formation is that the fast diffusion paths provided by the columnar boundary structure of the thin film (relative to bulk lattice diffusion) may permit a certain degree of out-diffusion of both Ga and As atoms from the substrate which results in void formation below the interface.

It is believed that these columnar grain boundaries play a major role in the outdiffusion of both Ga and As atoms from the substrate if any since the diffusivity along these grain boundaries would be several orders of magnitude higher than the volume diffusivity in the low temperature range ($T < 0.5\ T_m$). Especially in the absence of porosity or other defects, these columnar grain boundaries would be the fastest diffusion paths and are probably the main mechanism of the atomic transport in the low-temperature region. This is a reasonable assumption since the annealing temperatures (500 °C~850 °C) used in this study were lower than half the TiN melting temperature (2930 °C).

Correlation to Electrical Characteristics

I-V and C-V characteristics of the diodes were measured on the as-deposited samples and the samples annealed at 500 °C, 700 °C and 850 °C. The same samples were used for the structural studies described above. The ideality factors for TiN/GaAs contacts were found to be below 1.1 after RTA annealing up to 850 °C, but departed dramatically from unity for higher annealing temperatures. Enhancement of the thermionic emission barrier height determined from I-V characteristics[13] was observed for the samples after annealing in the temperature range of 500 °C to 850 °C as shown in Fig. 29. Concomitantly, the diode capacitance decreased with increasing annealing temperature. To formulate a model consistent with the electrical properties[13] and with the interface structure,

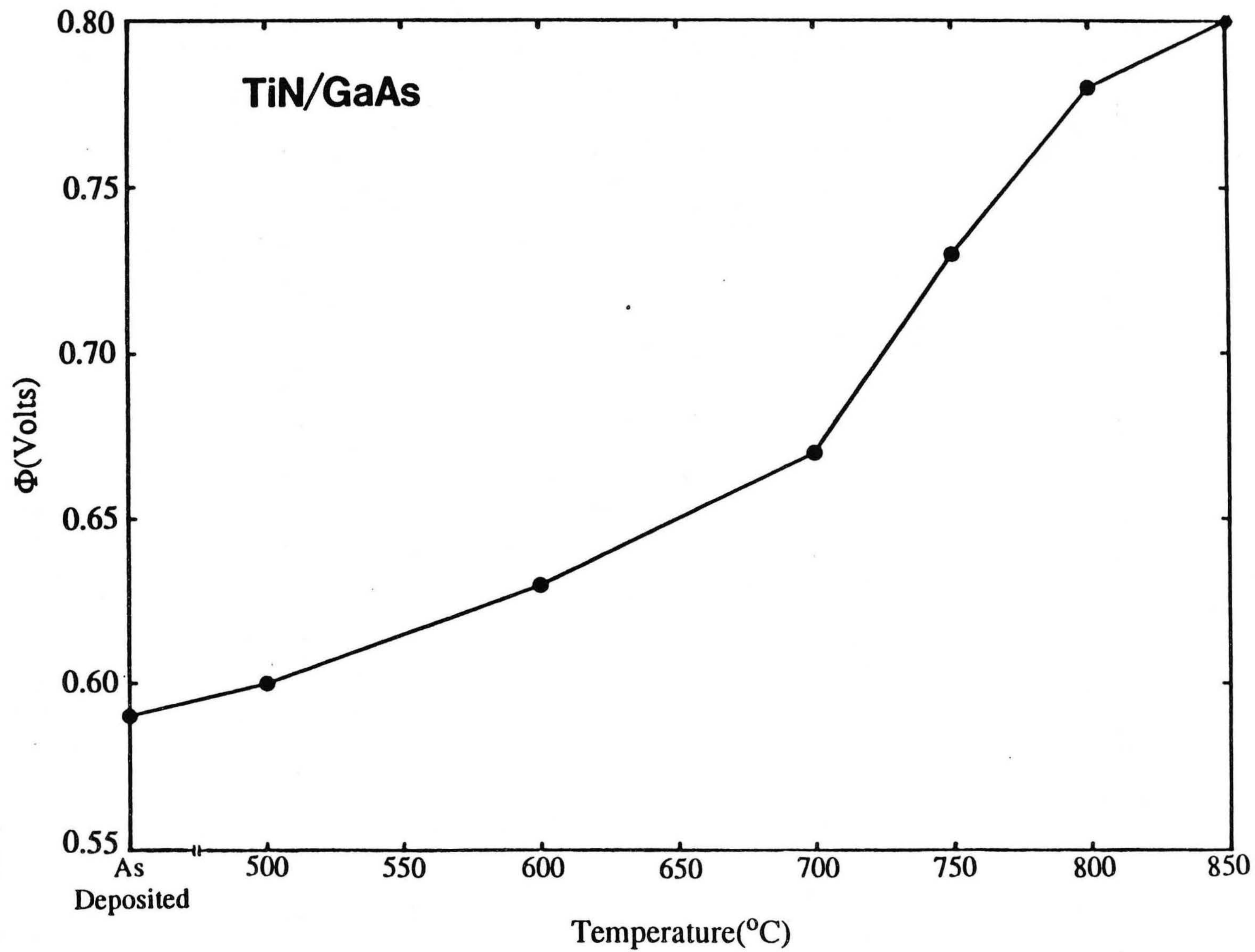

Fig. 29. Measured barrier height Φ for TiN/GaAs contacts annealed at different temperatures.

the pockets should be taken into account. As observed from TEM results, the fraction of surface area occupied by the pockets increased with increasing annealing temperature. The ratio of the surface area occupied by the pockets A_B to the area under which no pocket has formed A_S is defined as:

$$R = \frac{A_S}{A_B} \tag{19}$$

We observe that R decreases slightly with increasing annealing temperature with the order of magnitude for R equal to 10^{-1} for all annealing temperatures investigated.

In the following, possible explanations will be discussed for the increase of measured barrier height Φ from I-V with increasing annealing temperature from 500 °C to 850 °C, as shown in Fig. 29. The models start with the assumption that the pockets formed are accompanied by loss of As during annealing, as was directly confirmed by analytical TEM for similar pockets formed in annealed GaAs:Cr contacts.[126]

The first model assumes that pockets begin to form at 500 °C, and become p-type or create p-type regions at their circumference at higher annealing temperatures. Due to the close proximity of the extruded p-pocket regions, the lateral electric field of the p^+/n junctions will enhance the thermionic energy barrier in the surrounding n-GaAs. This metal/p^+-GaAs/n-GaAs structure has been called a Shannon contact, or a Camel diode.[127] A schematic energy diagram for such a metal/p^+-GaAs/n-GaAs structure is shown in Fig. 30 with two bias conditions: (1) with zero bias, and (2) with bias. This structure could provide an enhancement of barrier height, a high reverse breakdown voltage, and a suppression of reverse leakage current for the diode. The parallel Schottky diode model[128] was also considered, but would require R on the order of 10^{-4} to explain the 0.2 Volts difference in Φ from 500 °C to 850 °C. This is obviously in disagreement with the R values determined by TEM.

As shown in Fig. 31, the capacitance decreases with increasing annealing temperature from 500 °C to 850 °C. No variation in capacitance was observed over a frequency range of approximately 10kHz to 4MHz. The depletion depth x_d can be extracted from

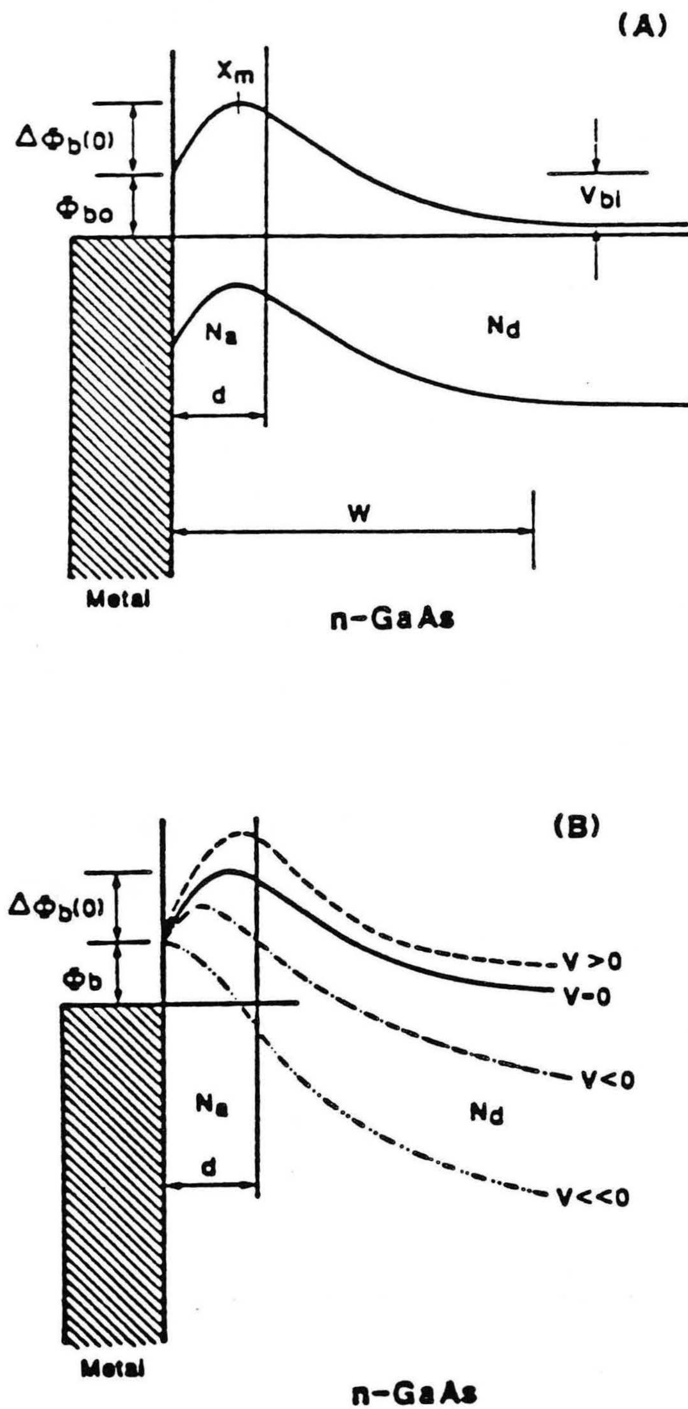

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Fig. 30. Schematic energy band diagram for a metal/p^+-GaAs/n-GaAs contact (a) without bias and (b) with bias. Three different bias conditions are shown in (b) forward bias $V > 0$, small reverse bias $V < 0$, and large reverse bias $V << 0$. With a large enough reverse bias, the barrier height enhancement $\Delta\Phi_b$ will disappear. (From Ref. 13)

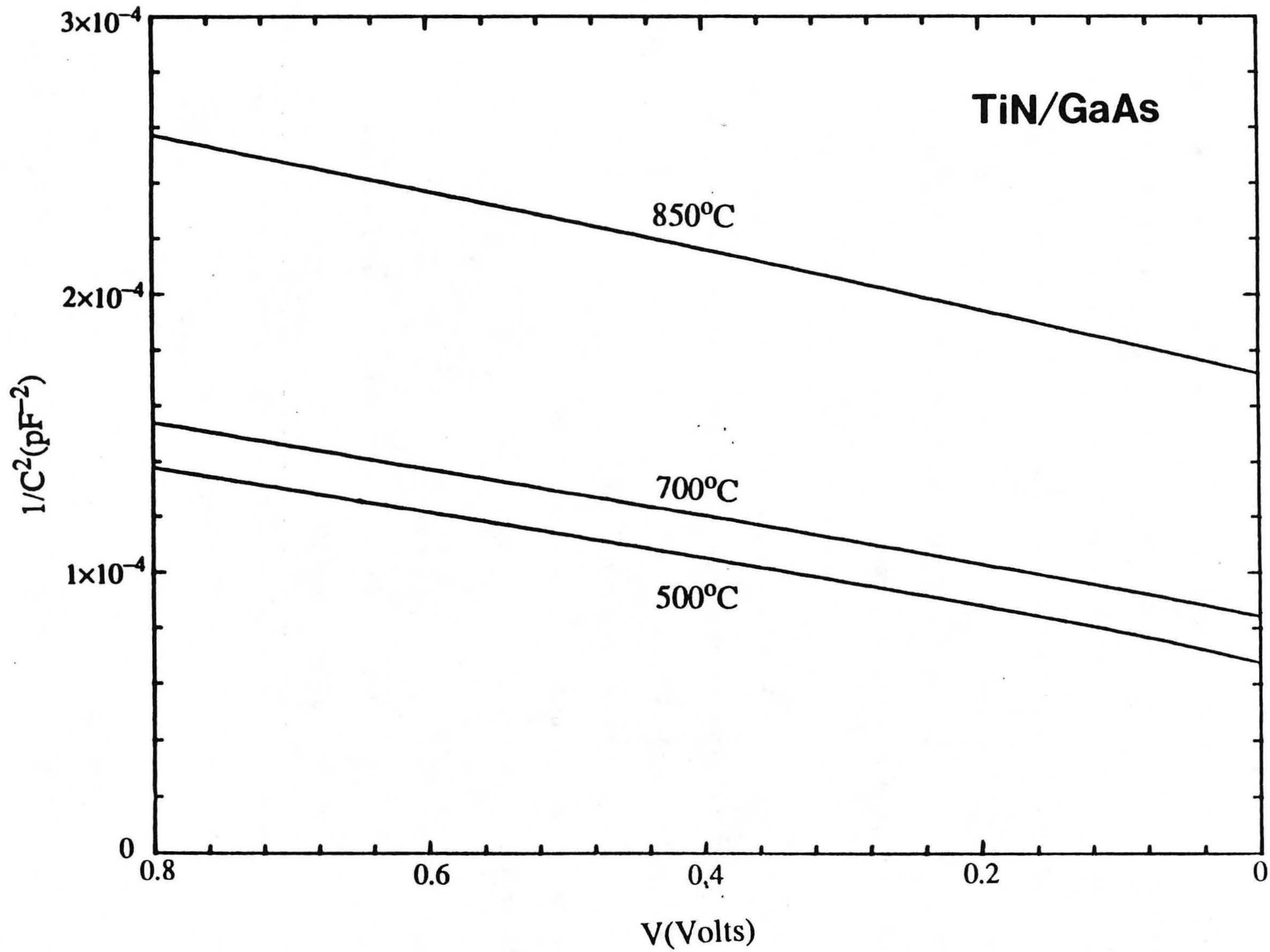


Fig. 31. C^{-2} vs V plots for TiN/GaAs contacts annealed at 500, 700, and 850°C.

the measured capacitance:

$$C = \frac{\epsilon(A_S + A_B)}{x_d} \tag{20}$$

where ϵ is the dielectric constant. From Eq. (20) the extracted x_d at 500 °C and at 850 °C are 84.2 nm and 134.1 nm, respectively. The background doping concentration determined from capacitance measurements was N_D is $1.5\times10^{17}cm^{-3}$. The barrier heights determined from the C^2–V intercepts were 0.53, 0.72, and 1.59eV for the as deposited, 500°C annealed, and 850°C annealed samples respectively. The band gap energy of GaAs is only 1.42eV. Therefore, the observed capacitance value at 850°C cannot be explained by the Schottky barrier model even when interface states are considered. However, the anomalously high built-in voltage is consistent with a sandwiched negative space charge layer.[13]

Noting that no other metallurgical phase was detected in the pocket regions, the measured increase in x_d due to the negative space charge layer can be explained by having the pocket regions be effectively p^+-GaAs. The volume of the pockets is of the order of $10^{-19}cm^3$. Therefore, it would take only one effectively p-type dopant per pocket region to obtain a p^+ doping concentration in excess of $10^{18}cm^{-3}$. The p-type concentration necessary to produce the observed x_d increase, δx_d, is given by:

$$N_A = \frac{\delta x_d N_D(R + 1)}{d} \tag{21}$$

where N_A is the p^+ concentration and d is the depth of the pocket. Taking the average value of pocket penetration depth from the sample annealed at 850 °C, d = 6 nm, and $R << 1$, we obtain $N_A = 1.2\times10^{18}$. This effective high doping concentration could be obtained, for example, by the loss of approximately one As and/or Ga atom in each pocket.

Other possibilities include a p-type nitrogen induced defect or defect complex introduced during sputter deposition of the refractory metal nitride film.[13] This could quantitatively explain the capacitance decrease after annealing at the temperature range of

500 °C to 850 °C. The postulation that, instead of the pocket regions, the GaAs regions surrounding the pockets or both become p-type with increasing annealing temperature converting the n-GaAs into p-type is also consistent with electrical data.

Alternatively, a loss of As in the near-interface region of GaAs could directly lead to an increase of barrier height on n-GaAs if the Fermi level is pinned by As-rich defects such as As_{Ga} antisite defects, as discussed elsewhere.[129]

3.2.3. WN/GaAs Contacts

Tungsten W, its silicide WSi_x and nitride WN_x have received attention from researchers for contacts to GaAs.[7,8,11–15] This is especially true for tungsten nitride WN_x since WN_x has lower resistivity than tungsten silicide, and can be formed easily by reactive sputtering from a pure W target in Ar/N_2 atmosphere. Yu et al.[130] recently reported a systematic study on the structural and electrical characteristics of WN_x/GaAs contacts under various annealing conditions, e. g., different nitrogen content in the films, annealed with or without a capping layer, and annealed in As overpressure and a flowing N_2 ambient.

For the present investigation, undoped and Si-doped ($N_D = 1.5\times10^{17}cm^{-3}$) GaAs wafers with (100) orientation were prepared for WN_x deposition by degreasing in organic solvants, etching in $HCl:H_2O$ solution, rinsing in de-ionized water and drying with nitrogen gas. Prior to loading into the deposition chamber, the wafers were dipped in a $NH_4OH:H_2O$ solution for 1 min. for removal of the native oxide from the GaAs surface. The WN_x films (~200 nm) then were deposited on the GaAs substrates by reactive dc sputtering. The total gas pressure was kept at 10 mTorr during the deposition. The relative partial pressure of nitrogen was used to control nitrogen content in the as-deposited WN_x films. The relative partial pressure of nitrogen was defined as $\gamma =$ $P(N_2/P(N_2 + Ar)$. In this work, the partial pressure of nitrogen was 20%.

The WN_x samples were annealed under different conditions. A set of samples were capped with an SiO_2 layer (~100 nm) by chemical vapor deposition. The samples were then furnace annealed (FA) at 700-850 °C for 30 min. under an As-overpressure or in flowing N_2. Some of the capped samples were annealed at 850, 900 and 950 °C for 10 seconds in a flowing Ar ambient in a halogen lamp rapid thermal annealing (RTA) system.

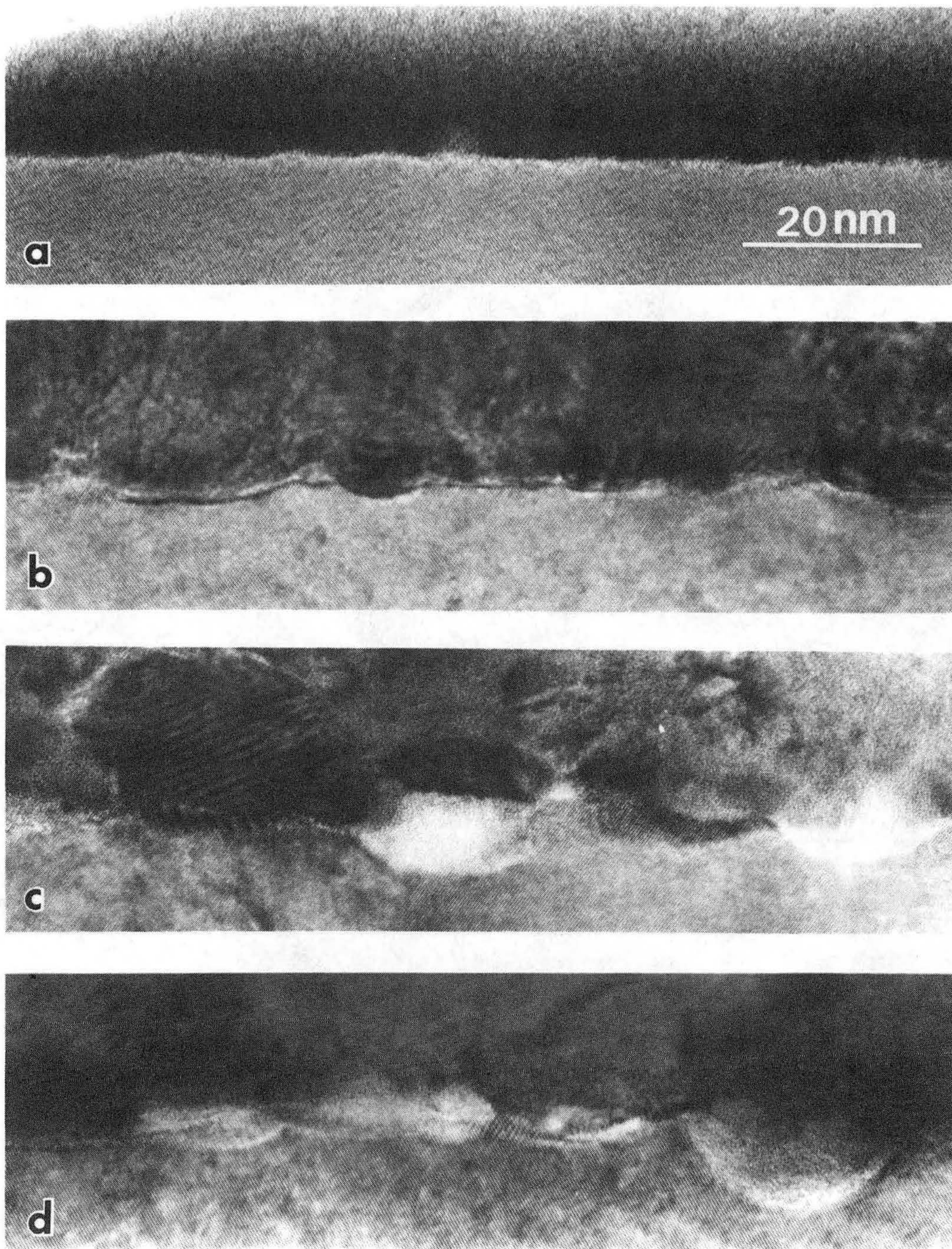
Interface Morphology

The interface morphology and structure of the WN_x/GaAs contacts were studied by TEM. Figure 32 shows the TEM images of cross-sectional samples before and after RTA at 850 °C, 900 °C and 950 °C. For the as-deposited sample, the interface between the as-deposited film and the substrate was relatively flat and no native oxide was observed. The structure of the as-deposited WN_x thin film with 20% N_2 was studied by the selected area diffraction technique. Figure 33 shows a diffraction ring pattern from the as-deposited thin film. This diffraction ring pattern has been indexed as the β-W phase.

The β-W phase is an A_3B compound with the A-15 crystal structure.[131] The A-15 structure has a cubic unit cell which is composed of four atomic layers parallel to the (100) planes with the 2 space B atoms in the bcc positions and the 6 space A atoms on the (001) basal planes. A previous study of β-W indicated that the β-W phase is probably formed by the metallic phase W_3W.[131] β-W has a cubic structure with a lattice parameter $a_o = 0.5050$ nm. The β-W film was also found to have a high resistivity (100~300 $\mu\Omega$ cm).

The electron diffraction pattern shown in Fig. 34a was taken from the interface region where an amorphous β-W ring pattern is superimposed on the [110] GaAs diffraction pattern. Since the amorphous film has a thickness of only ~15 nm, only the strongest 210 reflection from the β-W amorphous film is visible.

The interface morphology of the sample after RTA at 850 °C is shown in Fig. 32b.



XBB 881-660

Fig. 32. High-resolution cross-section TEM images of the WN/GaAs (a) as-deposited sample, and (b) annealed at 850°C, and (c) annealed at 900°C, and (d) sample annealed at 950°C.

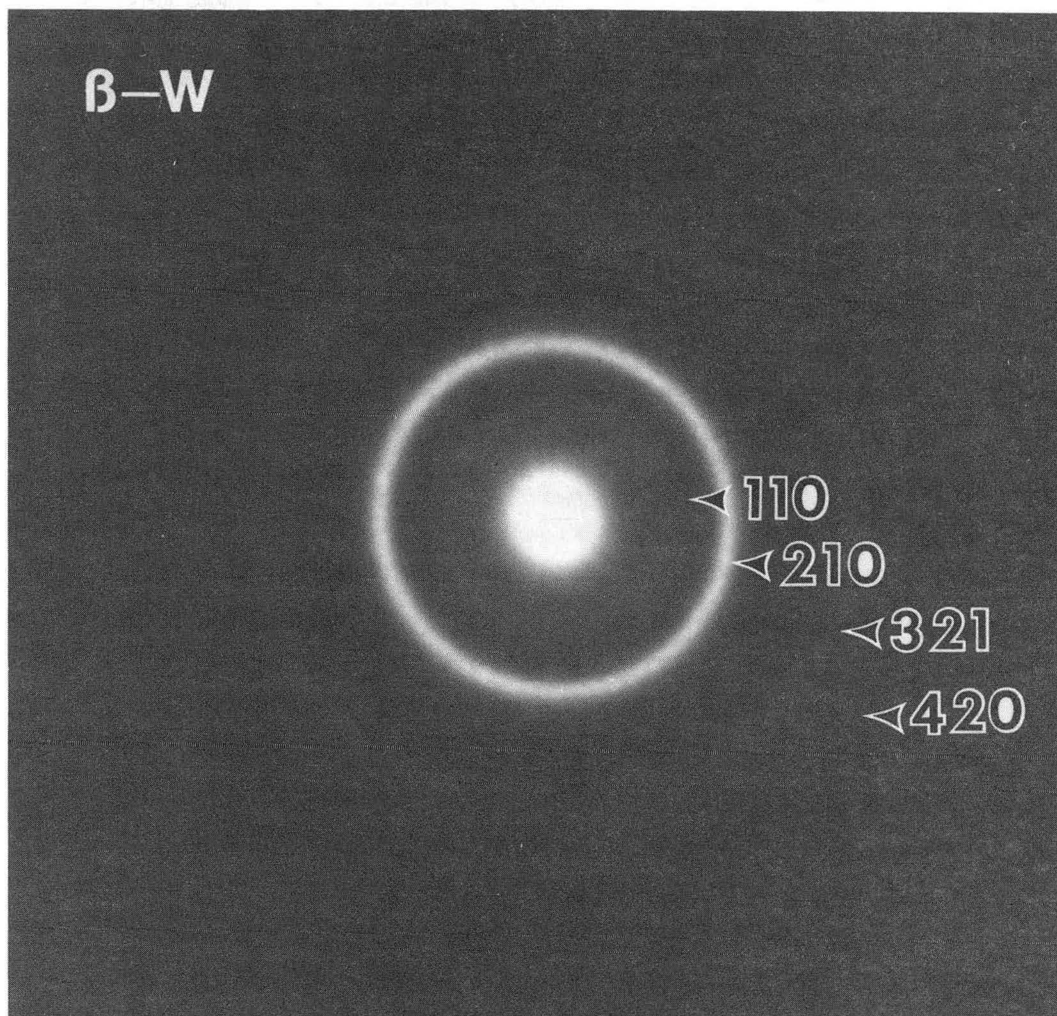


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Fig. 33. Electron diffraction pattern from the as-deposited WN thin film.

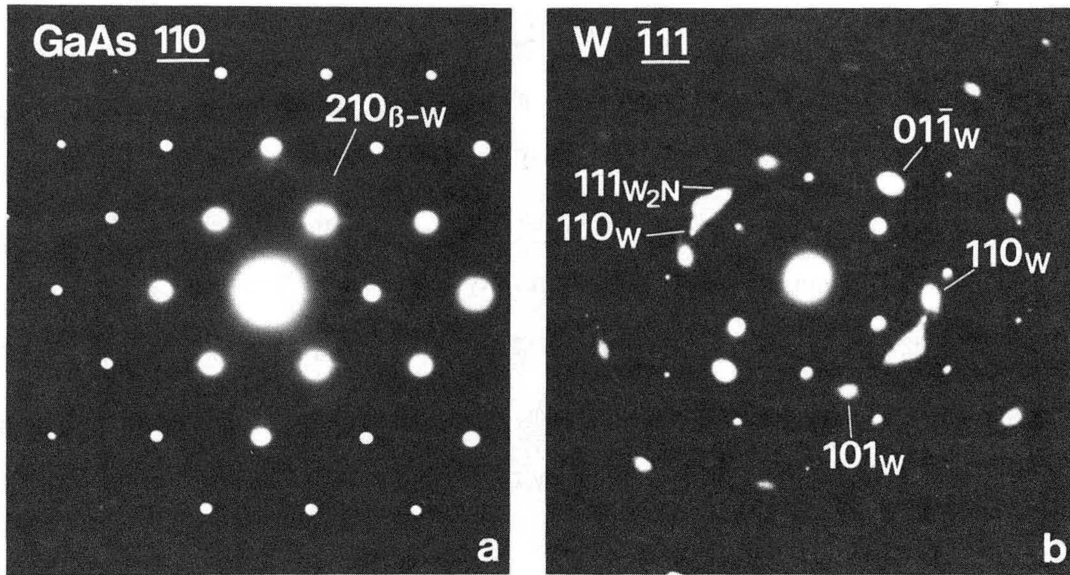

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Fig. 34. Electron diffraction patterns from the interface region of the WN/GaAs (a) as-deposited sample, and (b) sample annealed at 850°C.

The interface in this case was not flat, and there was evidence that interface interdiffusion occured during annealing. It is likely that some of the Ga and As atoms diffused into the WN_x film locally, and some As atoms may have diffused out along the grain boundaries in the film. RTA at 850 °C resulted in a crystallization of the as-deposited amorphous film. The crystallized grains in the film have been identified to be α-W and W_2N by XRD and electron diffraction techniques. As can be seen in Fig. 34b, a $[\bar{1}11]$ α-W diffraction pattern from one α-W single grain is superimposed on the [110] GaAs diffraction pattern. Note also that 110 α-W diffraction spots from another α-W grain shown on the left of the diffraction pattern are only a few degrees from the 111 diffraction spots of W_2N. This may indicate an epitaxial relationship between this α-W single grain and the W_2N grain since the lattice mismatch between the 110 α-W d-spacing (0.2238 nm) and the 111 W_2N d-spacing (0.2382 nm) is only 6.2%. Both α-W and W_2N have a cubic structure with lattice parameters 0.3165 nm and 0.4126 nm, respectively. From the x-ray and electron diffraction analysis, the majority phase in the film was α-W with a smaller amount of W_2N (20% of W_2N reported by Yu et al.[130]).

After RTA at 900 °C, the interface of the WN_x/GaAs contacts became very rough with pocket-like protrusions formed under the original interface of the WN_x/GaAs contact as shown in Fig. 32c. These pockets have an amorphous-like appearance as has been observed for TiN/GaAs contacts after annealing at temperatures above 800 °C.[132] The average width of the pockets is ~15 nm, and the average penetration depth of the pockets into the substrate is about 10 nm. It is expected that some W_2As_3 phase may be formed on the top of the pockets by outdiffusion of As atoms from the substrate. However, electron and x-ray diffraction results did not show any W_2As_3 patterns. This may be due to the very small amount of this phase present in the film.

RTA at 950 °C resulted in a very rough interface as shown in Fig. 32d. As shown in this figure, many more pocket-like protrusions were formed as compared with 900 °C RTA so that there is now no spacing left between them. This indicates that a significant

interface interdiffusion has occured during the 950 °C RTA. By measuring the lattice spacings from the phase at the top of these pockets in Fig. 32d, it was clear that the phase in intimate contact with GaAs was W_2N since only two phases, α-W and W_2N, were present in the thin film as indicated by electron and x-ray diffraction analysis. Figure 35 shows the electron diffraction pattern from the interface region of the sample after RTA at 950 °C. As can be seen in this figure, an α-W diffraction pattern with a [011] zone axis is superimposed on a [110] GaAs diffraction pattern, and also the (200) and (111) W_2N spots appear in this diffraction pattern. This indicates that the formation of α-W and W_2N is the result of the crystallization of the as-deposited amorphous materials after RTA in the temperature range of 850~950 °C. In comparison to the sample after 850 °C RTA, significant interface interdiffusion has occurred resulting in pocket formation beneath the original interface. It is likely that both Ga and As atoms diffused along the grain boundaries in the thin film to the surface since diffusion in grain boundaries is much faster than in the bulk in this temperature range. Significant outdiffusion of Ga and As atoms apparently requires an annealing temperatures above 850 °C because the first appearence of pockets beneath the original interface was after 900 °C RTA.

For the samples subjected to FA at 850 °C for 30 min. with and without SiO_2 caps, the interface morphology was almost identical with that after 850 °C RTA. This implies that annealing time at 850 °C is not an important variable compared to annealing temperature in determing the interface morphology. Figure 36a shows the interface morphology of the capped WN_x/GaAs sample after annealing at 850 °C for 30 min. From this bright field TEM image, the interface can be seen to be similar to that for the 850 °C RTA samples. In some regions the GaAs substrate was consumed by outdiffusion during annealing. The phase in intimate contact with the GaAs was again found to be W_2N by measuring the lattice spacings in Fig. 36a. This confirms the prediction by Yu et al..[130] Figure 36b shows the selected area diffraction pattern taken from the film only. The rings in this diffraction pattern were found to correspond to α-W and W_2N phases. From

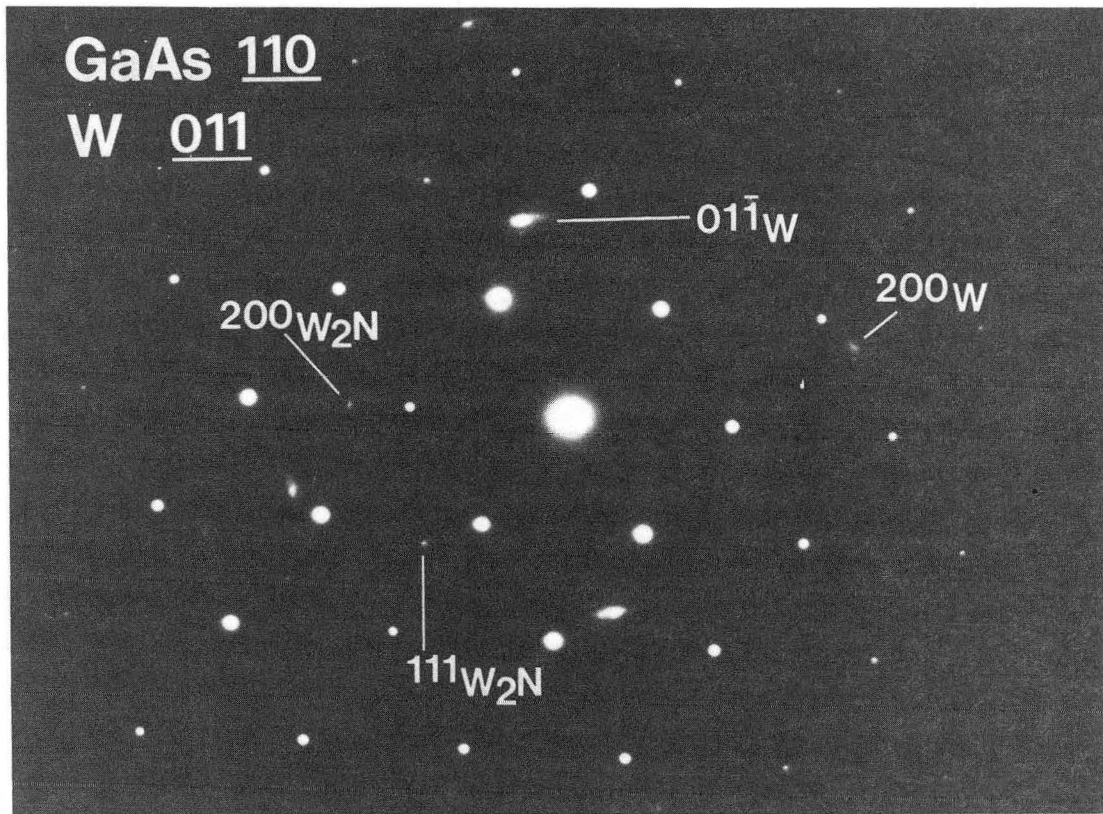

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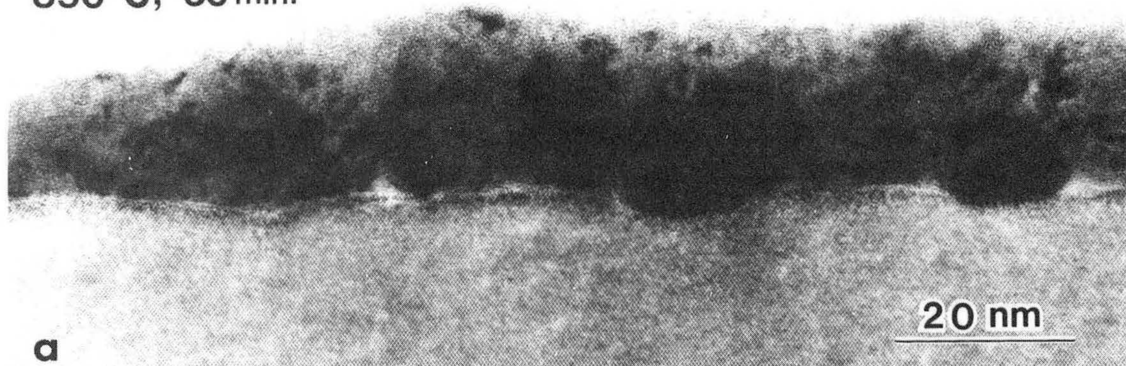
Fig. 35. Electron diffraction pattern from the WN/GaAs interface region after annealing at 950°C.



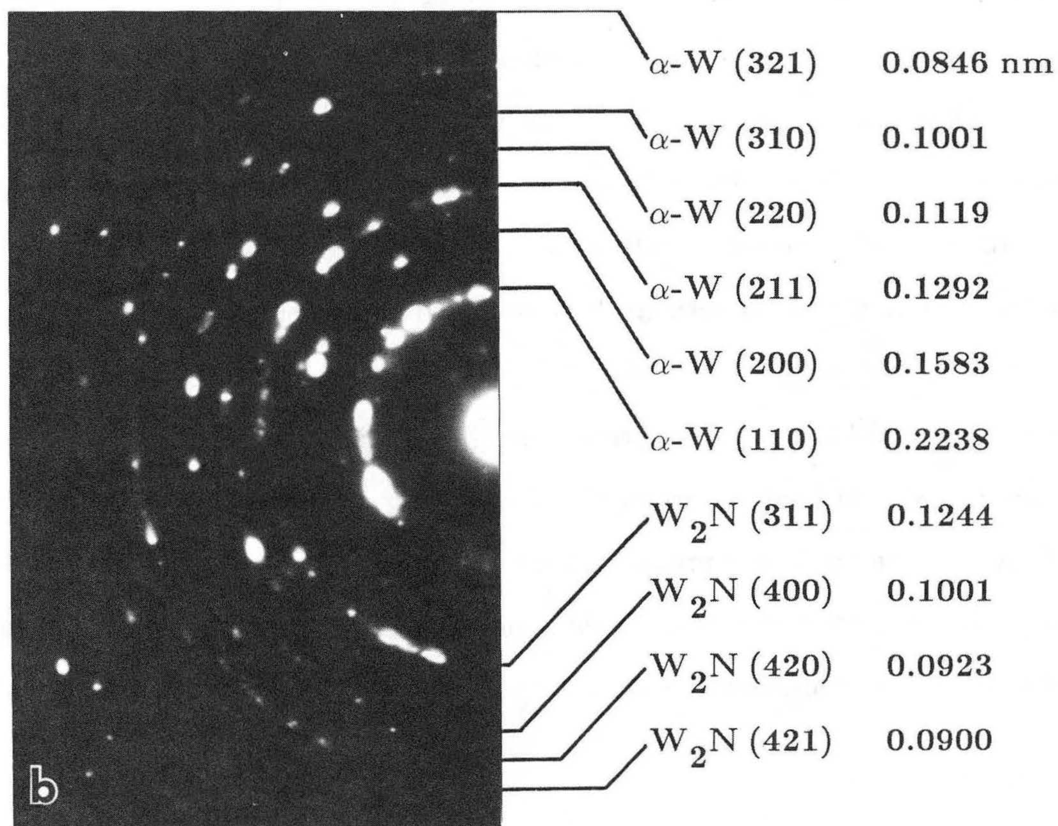


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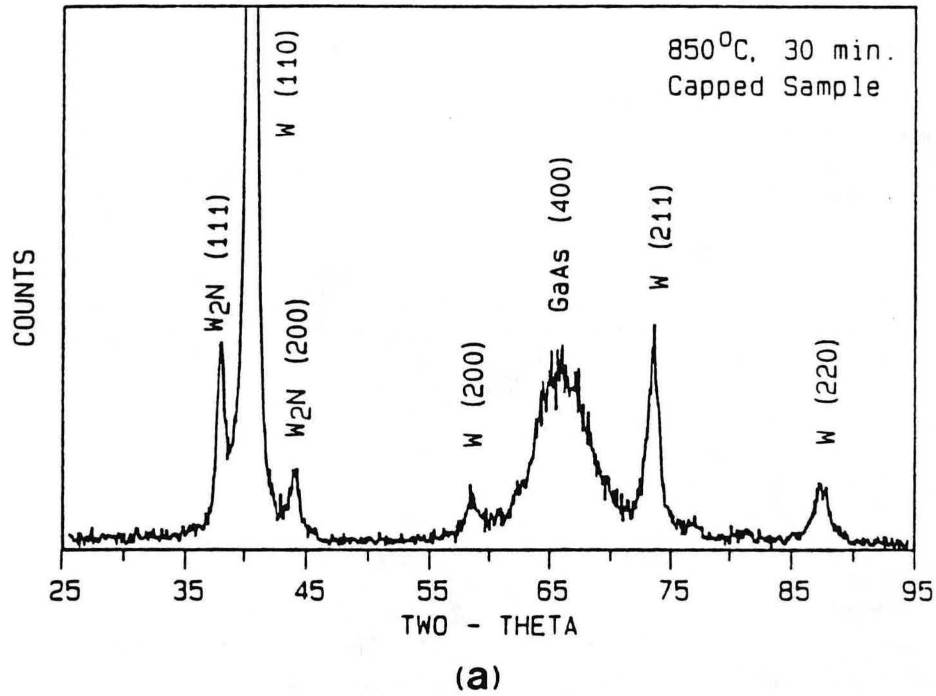
Fig. 36. (a) Cross-section TEM image of the capped WN_x/GaAs sample after FA at 850°C for 30 minutes, (b) Electron diffraction pattern from the thin film of the same sample.

the relative intensities of the diffraction rings, α-W was the major phase in the film.

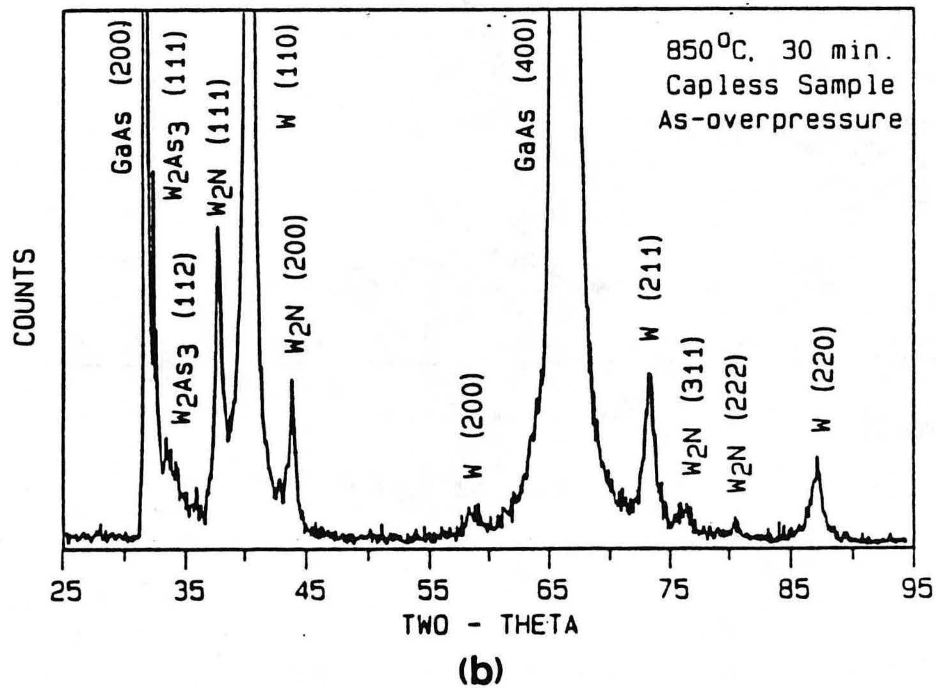
Results from the TEM cross-sectional samples did not show any difference in the interface morphology between the capless samples annealed in an As overpressure and the capped sample in a flowing N_2 ambient after furnace annealing at 850 °C for 30 min. XRD was also used to study the structure of WN_x/GaAs samples before and after annealing under different conditions, e. g., capped or capless, annealing in an As-overpressure or a flowing N_2 gas. Figure 37 shows the x-ray spectra from the capped (a) and capless (b) samples after annealing at 850 °C in a flowing N_2 gas and an As overpressure, respectively. The spectrum from the capped sample indicates that the thin film consists of a mixture of phases, α-W and W_2N. Note that the GaAs (200) diffraction peak did not appear, and also the GaAs (400) peak has a very low intensity due probably to misorientation of the GaAs substrate from a (100) plane, or the large thickness of the film formed on the GaAs substrate. Compared to the spectrum from the capped sample, the spectrum from the capless sample shows additional peaks corresponding to W_2As_3. Based on a previous Rutherford backscattering spectrometry (RBS) study,[130] it is believed that this W_2As_3 phase was formed on the surface of the thin film by the reaction of W on the surface of the film and an As overpressure during annealing. It is also interesting to note that the diffraction intensity of W_2N in the capless sample is higher than that of in the capped sample. This is also in good agreement with the previous RBS study.[130]

Electrical Properties

Figure 38 shows the electrical characteristics of the WN_x/GaAs contacts before and after annealing in different conditions in the temperature range of 700-850 °C for FA and 700-950 °C for RTA.[130] Yu et al. discussed the effects of nitrogen and annealing conditions on the thermal stability and barrier height of the WN_x/GaAs contacts.[130] The barrier height enhancement with annealing temperatures below 700 °C is attributed to the removal of sputtering damage and consumption of the native oxide at the interface. The reasons for the increase of the barrier height in the nitride contact systems after



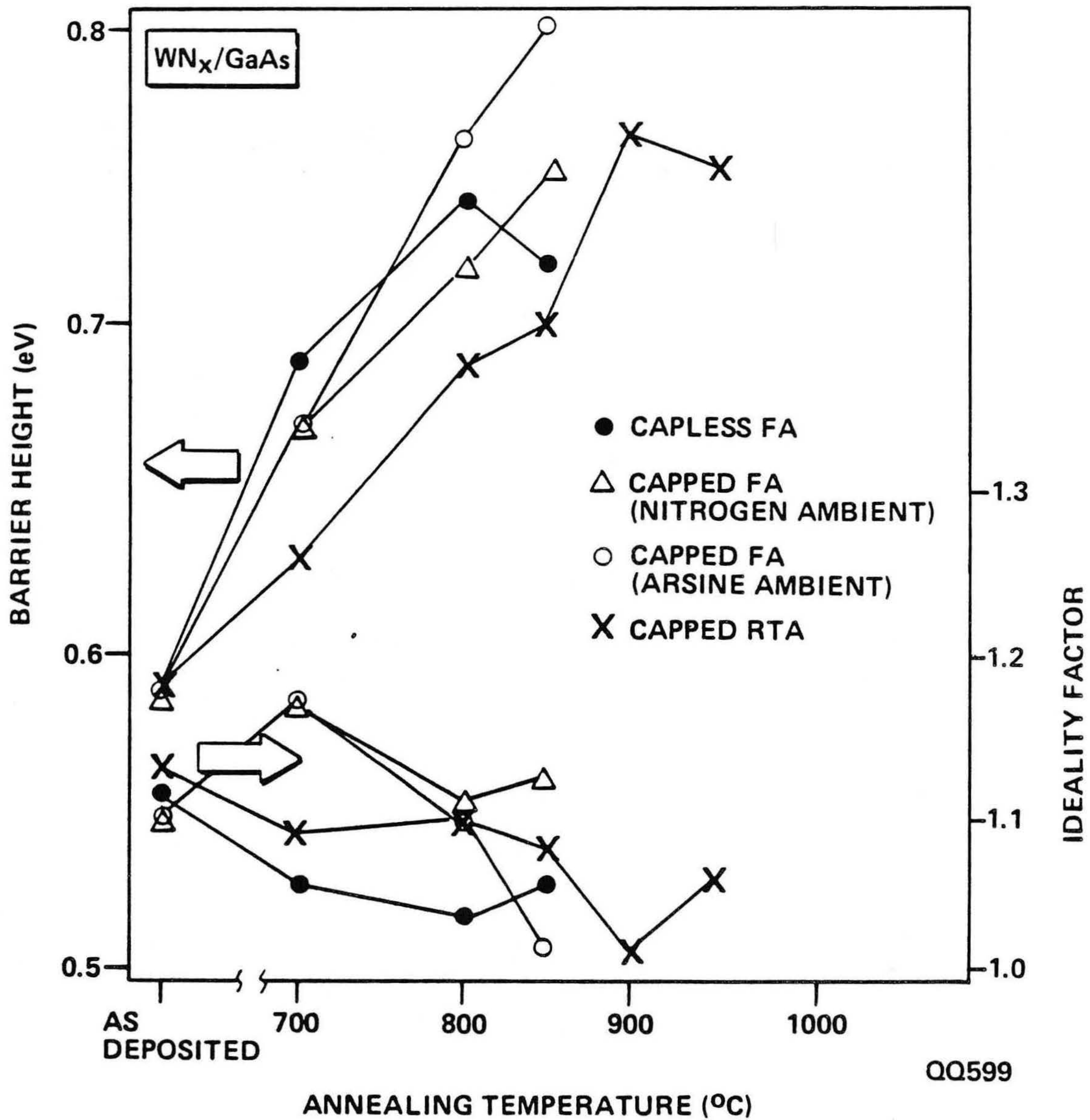
(a)



(b)

XBL 896-2293

Fig. 37. X-ray diffraction spectra of the samples after 850°C FA for 30 minutes (a) capped and (b) capless.



XBL 894-1586

Fig. 38. Plots of Φ_b and n as a function of annealing temperature under different annealing conditions for WN_x/GaAs diodes formed by $\gamma = 20\%$. (From Ref. 130)

annealing at temperatures above 700 °C have been a subject of speculation in the literature. The following explanations have been suggested: (1) the formation of a metal/p^+-GaAs/n-GaAs contact by incorporation of nitrogen into the substrate;[13] (2) the charge states of Ga vacancies formed near the interface;[130] (3) the effective electronegativity of the phase in intimate contact with GaAs.[130] The correct explanation is still not clear.

The results of this investigation show that most of the GaAs interface is in intimate contact with W_2N after annealing, and the interface is stable up to 850 °C. Yu et al.[130] reported that the amount of W_2N in the film is proportional to the relative partial pressure of nitrogen γ, and the film resistivity increases with increasing nitrogen concentration in the film. It was proposed that the intimate contact of W_2N phase and the GaAs substrate may be the reason of the increase in the barrier height of the contacts.[130] If this was true, a pure W_2N would be needed to form a high barrier contact which could be easily accomplished by increasing γ from 20% to above 40%. However, the resistivity of a pure W_2N film is very high ($\rho \simeq 220$ $\mu\Omega$ cm) as compared with that of a pure α-W which has a resistivity as low as $\rho \simeq 5.6$ $\mu\Omega$ cm,[130,133] a pure W_2N film as a contact metal would increase the RC time constant. Therefore, one might naturally consider using a pure W film as a contact metal on GaAs because of its high melting temperature (3417 °C) and low resistivity. Unfortunately, W/GaAs contacts have a relative high ideality factor (≥ 1.2) and low barrier height (0.65-0.7 eV) compared to the WN/GaAs contacts where $n \leq 1.1$ and $\Phi_b \simeq 0.8$ eV.

Since a mixture of α-W and W_2N phases can be obtained by controlling the relative partial pressure γ between 20% and 40% and since the W_2N phase forms in intimate contact with the GaAs substrate on annealing at temperatures above 800 °C, it is possible to choose a partial pressure γ which gives both high barrier height and low film resistivity. In this case, $\gamma = 20\%$ was found to give both desired electrical properties with $\rho \simeq 75$ $\mu\Omega$ cm and $\Phi_b \simeq 0.8$ eV after annealing at 850 °C for 30 minutes, where 20% of the W_2N phase formed in the film. It is still not clear why the W_2N phase was formed in intimate

contact with the GaAs substrate.

It is interesting to note that the pocket-like protrusions were formed above a critical temperature 900 °C RTA as also found for TiN/GaAs contacts where the first appearance of the pockets occurred after 500 °C RTA. The formation of pockets can be explained by outdiffusion of As or Ga and As. This loss of As or Ga and As can change the electronic structure, and create electrically active defects at or near the interface which might also result in barrier height enhancement. For example, it could create a p^+-GaAs thin layer surrounding the pockets,[132] or it might change the pinning position of the Fermi-level in the GaAs band gap by loss of As as discussed elsewhere.[129]

3.2.4. Discussion

As discussed previously, the advantages of the refractory metal nitride metallizations for MESFET fabrication include low resistivity, the ease with which the nitride can be formed by reactive sputtering deposition, and the thermal stability of the nitrides throughout device processing at temperatures up to 900 °C. Furthermore, the improved electrical characteristics of the refractory metal nitride/GaAs contacts after annealing at high temperatures ($\geq$800 °C) make it even more attractive for the gate contact formation, e. g., enhancement of contact barrier height, increase in reverse breakdown voltage, and decrease in contact capacitance. All these properties of the refractory nitrides make them very attractive candidates for thermally stable metal/GaAs contacts.

The thin nitride films were deposited on the GaAs substrate by using sputtering deposition. One of the advantages for using sputtering techniques instead of other deposition techniques is that sputtering can be used to clean the contamination such as the native oxide on the surface of the substrate prior to the thin film deposition. The sputter cleaning can be performed by simply reversing the bias, which is called "back sputtering". However, this procedure can cause a certain degree of lattice damage in the substrate.

Another advantage is that sputtering deposition can be performed at room temperature while evaporation techniques need high temperature processing which may result in a dissociation of the GaAs substrate. Especially for the refractory metals and their nitrides, deposition sources require very high temperatures for evaporation. Sputtering techniques solve this problem because the targets are bombarded at room temperature, and atoms ejected from the target deposit on the substrate.

The improvement of the electrical characteristics in the nitride/GaAs contacts after annealing in the temperature range 500-700 °C was believed to be the result of removal of the damage caused by sputtering deposition and *in situ* sputter cleaning prior to film deposition. Murakami et al.[134] studied GaAs substrate damage caused by the sputter cleaning by x-ray photoelectron spectroscopy. Their results showed that sputter cleaning could result in a damaged layer of GaAs containing 0.3-1.0 nm of gallium oxide at the GaAs surface. Poor I-V characteristics of the metal/GaAs contacts formed by sputtering deposition are the result of this kind of sputtering damage. Neverthless, this damage can be removed by annealing at temperatures of 500-700 °C as can been seen from the previously studied I-V and C-V characteristics for silicide/GaAs and nitride/GaAs contacts.[13,132]

Resistivity of the nitrides is the single most important criterion in considering them for the metallizations in the MESFETs devices and integrated circuits. This importance is a result of scaling down of device sizes, for example, submicron gate lengths in MESFETs. The gate lengths get narrower and sheet resistance contribution to the RC time constant increases. The effect of increased sheet resistance on device performence is a loss in device speed due to high RC time constant. Therefore, the relatively low resistivity of the refractory metal nitrides can lower the sheet resistance, i. e., lower RC time constant.

The contact capacitance of the diodes is another factor which can change the RC time constant. Since the contact capacitance of the refractory metal nitride/GaAs contacts decreases with annealing temperature above 700 °C, the RC time constant is

expected to decrease making high speed devices possible. The reason for this decrease of contact capacitance with annealing temperature will be discussed later.

Based on the experimental results, Zhang et al.[13] proposed that a thin p^+-GaAs layer formed between the nitride film and the GaAs substrate during annealing at temperatures above 700 °C as a result of diffusion and electrical activation of nitrogen and/or nitrogen-defect complexes introduced into the GaAs substrate during the initial stage of the sputtering deposition. The formation of this interfacial p^+-layer could result in a Shannon contact.[127] The Shannon contact model says that if both the p-type layer and n-type substrate are uniformly doped, a metal/p^+-GaAs/n-GaAs structure will enhance the barrier height which can be calculated by solving Poisson's equation with depletion approximation.[13,127,135]

There is evidence that the barrier height enhancement of the refractory metal nitride/GaAs contacts after annealing at temperatures above 700 °C is due to the formation of a Shannon contact. Zhang et al.[13] found that the breakdown characteristics of the contacts show a "sharp" turn-on feature instead of a "gradual" increase in reverse current with increasing reverse bias near the breakdown voltage. For a p-n junction, reverse voltage breakdown is caused by an avanlanche process within the depletion region, where electrons and holes are under very large electrical field. Once a critical electrical field is reached, electrons are pull out from the orbitals of atoms to produce a huge increase of electrons and holes as carriers. This avanlanche process will result in a "hard" turn at the breakdown. In the case of a Schottky contact, the contact barrier is relatively thin at the top half caused by doping. Applying reverse bias can cause the potential barrier to become thinner.[95,136] Therefore, electrons can tunnel through the narrow part of the barrier at lower reverse bias relative to a p-n junction. This results in breakdown characteristics having a "soft" turn-on feature for metal/GaAs contacts under the reverse bias. Tunneling is one of the most common causes of "soft" reverse characteristics.

The decrease in the contact capacitance is also evidence for the Shannon contact. As

shown in Equ. 20, the capacitance of the contact is inversely proportional to the width of the depletion region of the contact. The changes of the contact capacitance indicate variations of the width of the depletion region. In the case of the nitride/GaAs contacts, the decrease of the contact capacitance after annealing at temperatures above 700 °C represents a thicker depletion region as a result of a metal/p^+-GaAs/n-GaAs contact.

Considering the proposed model by Zhang et al.,[13] it is not surprising that nitrogen can easily diffuse into the substrate for two reasons. The first reason is that the size of nitrogen atoms (atomic or covalent radius) is only 0.075 nm but the GaAs [110] channel radius is 0.076 nm so that the activation energy for nitrogen diffusion in the GaAs substrate should be relatively low (the diffusion coeffecient of nitrogen in the GaAs is not available in the literature). The second reason is that for almost all refractory mononitrides, MN, the stoichiometry of the nitrides has range up to 20% nitrogen content with the same structure.[59,72] For example, TiN has a broad composition range from about $TiN_{0.6}$ to about $TiN_{1.0}$. Even at the stoichiometric composition, these nitrides have a large fraction of vacant sites on both the metal and the nometal sublattices.[59] This defect structures may permit nitrogen to diffuse out of the nitrides into the substrate.

Another possibility for the formation of an interfacial p^+-GaAs layer involves the pocket-like protrusions formed beneath the original interface. As discussed in an earlier section for the TiN/GaAs and WN/GaAs contacts, the pockets formed after annealing at high temperatures may be p-type by the loss of approximately one As and/or Ga atom in each pocket. By measuring the penetration depth of the pockets into the substrate and the spacing between the pockets, it has been shown that an effective p^+-GaAs layer may be formed between the nitride film and the n-GaAs if the pockets were p-type.

The advanced unified defect model proposed by Spicer at al.[42,136] for the Fermi-level pinning in GaAs has also been considered to explain the enhancement of the barrier height upon annealing at temperatures above 700 °C. As suggested by Spicer et al. in the AUDM,[136] a loss of As from the substrate upon annealing may change the Fermi-level

position in the band gap so to change the barrier height. The AUDM can be understood as follow: GaAs bulk crystals are usualy grown from the As-rich side of the phase diagram in order to obtain semi-insulating properties.[137] The undoped semi-insulating property of GaAs is the result of compensation by a native As_{Ga} antisite defect, i. e., an As atom on a Ga site in the GaAs lattice. The As_{Ga} antisite is a double donor, and it provides pinning levels at 0.75 and 0.5 eV above the valence band maximum.[43] The AUDM suggests that As-rich interfaces are expected to be pinned near the midgap level (0.75 eV), whereas less As-rich interfaces should exhibit pinning nearer the lower level.[42,136] In the current case, a loss of As through the grain boundaries in the thin films would result in a less As-rich interface so that the Fermi-level would be expected to be pinned near the lower level (0.5 eV). The change of pinning position from 0.75 to 0.5 eV above the valence band maximum would increase the barrier height for the nitride/GaAs contacts. However, the decrease of the contact capacitance with annealing temperatures above 700 °C has indicated that the enhancement of the barrier height was not due to the change of the Fermi-level pinning position in the band gap by a loss of As, at least it is not a dominant factor for the increase of the barrier height.

Refractory metal silicides have been successfully used as gate materials in MESFESs fabrications due to their low resistivity and relative high melting temperatures (900 °C∼220 °C).[9,11,12,138] As a comparasion to the refractory metal silicide metallizations, the refractory metal nitride/GaAs contacts have the advantage over the silicide contact to GaAs. One of the advantages of the refractory metal nitrides as gate metallizations over the refractory metal silicides is that at high temperatures, interface interdiffusion at the silicide/GaAs interface may change the electrical characteristics of the diodes since Si acts as a dopant in GaAs, while nitrogen is an electrically neutral atom in GaAs. Another advantage for the nitrides is that the barrier height of the contacts is higher than that of the silicide/GaAs contacts after annealing at temperatures about 800-850 °C; the difference of the barrier height in the two systems is as high as 0.2 eV.

Work is still necessary to further understand the mechanism of barrier height enhancement. For example, how might an interfacial p^+-layer be formed? By nitrogen and/or nitrogen complexes incorporated into the substrate during sputtering and annealing, or by losing As or Ga and As atoms during high temperature annealing?

4. RESULTS AND DISCUSSIONS II:
Miscibility Gap in the InAs-GaAs Pseudobinary System

Graded $In_{1-x}Ga_xAs$ layers on GaAs grown by molecular beam epitaxy have been shown to make low-resistance ohmic contacts to n-GaAs (Woodall et al. 1981).[16] Woodall et al. demonstrate that the composition grading is necessary to smooth out the conduction band discontinuity so that ohmic conduction can occur. Previous Auger electron spectroscopy studies by Lakhani[17,18] suggest that a graded $In_{1-x}Ga_xAs/GaAs$ heterojunction ($0<x<1$) can also be formed by heat treating thermally evaporated indium films on GaAs substrate at 350 °C. Recently, interface structures and morphologies of In on GaAs after annealing at 350 °C were investigated by Ding et al.[68] using transmission electron microscopy techniques. The result of this study demonstrated the abrupt nature of the interface between the GaAs substrate and the $In_{1-x}Ga_xAs$ islands. Contrary to the result of Lakhani[17,18], the $In_{1-x}Ga_xAs$ interfaces were not graded. Furthermore, only islands with $x<0.2$ or $x>0.8$ were observed. Ding et al.[68] proposed that the absence of precipitates with $0.2<x<0.8$ is direct evidence for a miscebility gap in the InAs-GaAs pseudo-binary system at 350 °C. This interpretation is consistent with the calculation of de Cremoux et al.[90] which suggest the existance of a miscibility gap with a critical temperature between 500 °C and 700 °C in the InAs-GaAs system. Other theoretical analyses with similar conclusions were reported by Stringfellow[91] and Onabe[92]. Quillec et al.[85] grew a series of InGaAsP thin films from the liquid phase on both (100) GaP and (100) InP substrates at relatively high temperatures (610 °C-700 °C). The experimental results from electron microprobe analyses indicated the existence of a miscibility gap in the $In_xGa_{1-x}As_yP_{1-y}$ system, supporting the previous theoretical results. The miscibility gap originates from an enthalpy of mixing (ΔHmix) which is greater than the absolute temperature multiplied by the entropy of mixing (TΔSmix) at temperature below some critical temperature, T_C. Atomistically, immiscibility in a system such as InAs-GaAs implies that In and Ga atoms repel so that a random distribution of Ga and In on the cation sites of the zincblende

structure is not energetically favorable.

4.1. Results

In this work, the previous study[68] of the In/GaAs reaction has been extended to include the temperature range 350 °C-650 °C.

The interface morphology of the In/GaAs sample after annealing at 350 °C for 10 minutes is depicted in Fig. 39. The two beam bright field TEM image is shown in Fig. 39a. A thin film of indium oxide can be seen to cover the reacted island. This precipitated phase has been identified structurally by electron diffraction analysis and compositionally by energy dispersive spectrometry. The EDS spectra from the island A and the substrate B (shown above the image) yield a composition of $In_{0.02}Ga_{0.98}As$ for the Ga-rich ternary phase with the zincblehde structure. The diffraction pattern from the interface region shown in Fig. 39b indicates that it is almost impossible to distinguish the diffraction spots of this ternary phase from those of the GaAs substrate because of the small concentration of indium in this epitaxial island. The high resolution lattice image in Fig. 39c reveals the detailed interface morphology. A misfit dislocation can be seen at the interface due to the mismatch (0.16%) between the Ga-rich ternary phase $In_{0.02}Ga_{0.98}As$ and the GaAs substrate. Another example of a precipitate from the same sample is shown in the cross-sectional high resolution micrograph in Fig. 40. The misfit dislocations and moire fringes appear at the interface, where they result from the two distinct lattice parameters of the epitaxial island and the GaAs substrate. This indicates that the interface is abrupt, i.e., no graded $In_{1-x}Ga_xAs$ layer exists at the interface. Since the ternary $In_{1-x}Ga_xAs$ phases exhibit a linear dependence of lattice spacing with composition,[139] i. e., they obey Vegard's law, the compositions of the precipitates studied can be determined by electron diffraction analysis, especially for In-rich $In_{1-x}Ga_xAs$ precipitates. Based on Vegard's law, the epitaxial island was identified from the diffraction analysis to be the In-rich ternary phase $In_{0.9}Ga_{0.1}As$. The EDS data also confirm that the island is In-

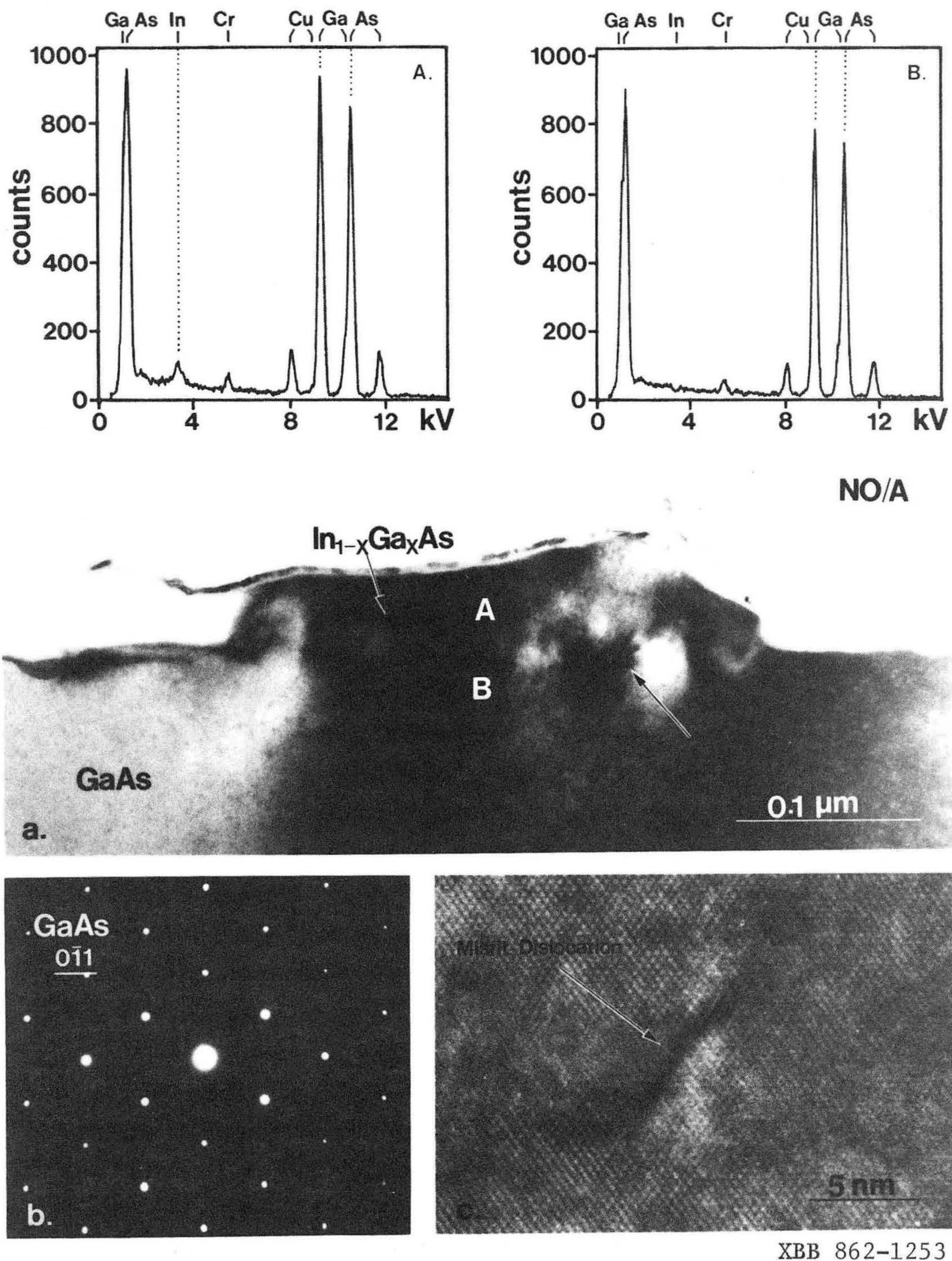


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Fig. 39. (a) Cross-sectional TEM image of the In/GaAs sample annealed at 350°C. The energy dispersive x-ray spectrum A indicates the patch A to have the composition of $In_{0.02}Ga_{0.98}As$. (b) Diffraction pattern taken from the interface area. (c) Lattice image of a misfit dislocation (arrowed in (a)) at the interface.

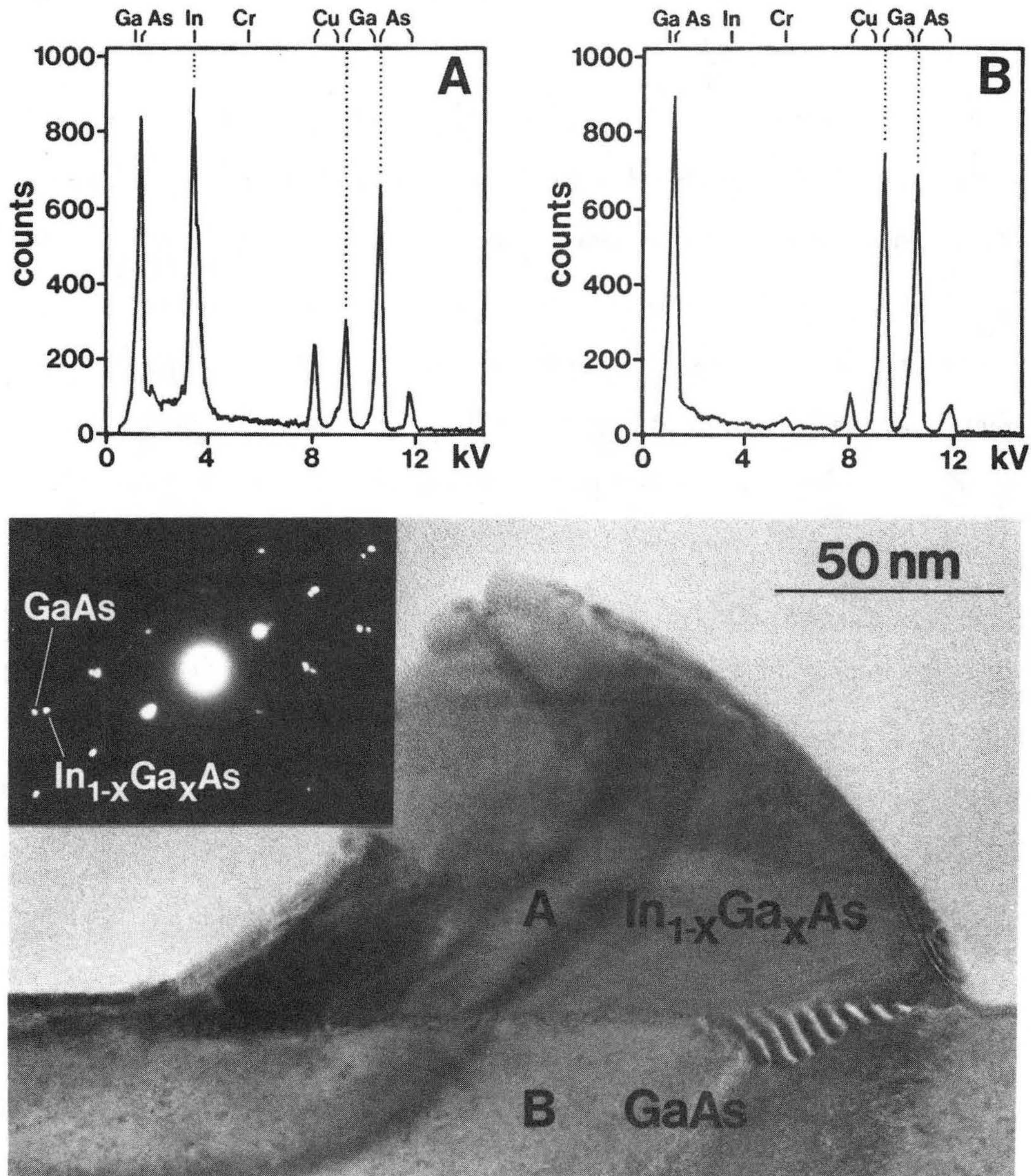

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Fig. 40. Cross-sectional TEM image of the In/GaAs sample annealed at 350°C. The misfit dislocations and the moire fringes indicate an abrupt interface. The patch A was estimated to be $In_{0.9}Ga_{0.1}As$ by diffraction analysis and energy dispersive x-ray spectrum.

rich $In_{1-x}Ga_xAs$. Precipitates with compositions ($0.2<x<0.8$) were not observed.

According to the theoretical calculations of de Cremoux et al.[90], a miscibility gap exists in the InAs-GaAs pseudo-binary system with a critical temperature between 500 °C and 700 °C. To investigate the effect of immiscibility on the In/GaAs reaction, a statistical study was performed by nnealing the In/GaAs samples at 350 °C, 500 °C, 575 °C and 650 °C. Several cross-sectional specimens from each sample were investigated by TEM and STEM. The distributions of precipitate compositions were determined by electron diffraction and EDS analyses. As can be seen in Fig. 41, three histograms from three different annealing temperatures reveal the extent of immiscibility in this system. It is also clear from the histograms that the critical temperature (i.e., the temperature above which InAs and GaAs are completely miscible) is between 500 °C and 650 °C. This miscibility gap in the InAs-GaAs pseudo-binary system was also revealed experimentally by x-ray diffractometry. The x-ray results from this system are shown in Fig. 42. Slow trace of the 400 peaks of the GaAs substrate and $In_{1-x}Ga_xAs$ ($0<x<1$) precipitates were obtained by employing CuKα radiation in an x-ray diffractometer. When compared with the spectrum from the as-deposited sample, the spectrum from the sample annealed at 350 °C shows an additional peak corresponding to In-rich $In_{1-x}Ga_xAs$ and a shoulder in the GaAs 400 peak corresponding to Ga-rich $In_{1-x}Ga_xAs$. This result is in agreement with EDS and electron diffraction data in Fig. 41. As the annealing temperature is increased, the In-rich $In_{1-x}Ga_xAs$ 400 peak shifts toward the direction of increasing Ga content (i.e., increasing x). The diffraction peak from the In-rich $In_{1-x}Ga_xAs$ ternary phase peak merges with the Ga-rich shoulder at 650 °C, suggesting that the critical temperature is close to 650 °C. Furthermore, It is apparent from the broad Ga-rich shoulder in the x-ray data that significant interdiffusion is taking place at 650 °C.

The experimental results described in this work provide direct evidence for the existence of a miscibility gap in the InAs-GaAs pseudo-binary system. It follows that the formation of graded $In_{1-x}Ga_xAs$ ($0 < x < 1$) layers by thermal reaction of In on GaAs is

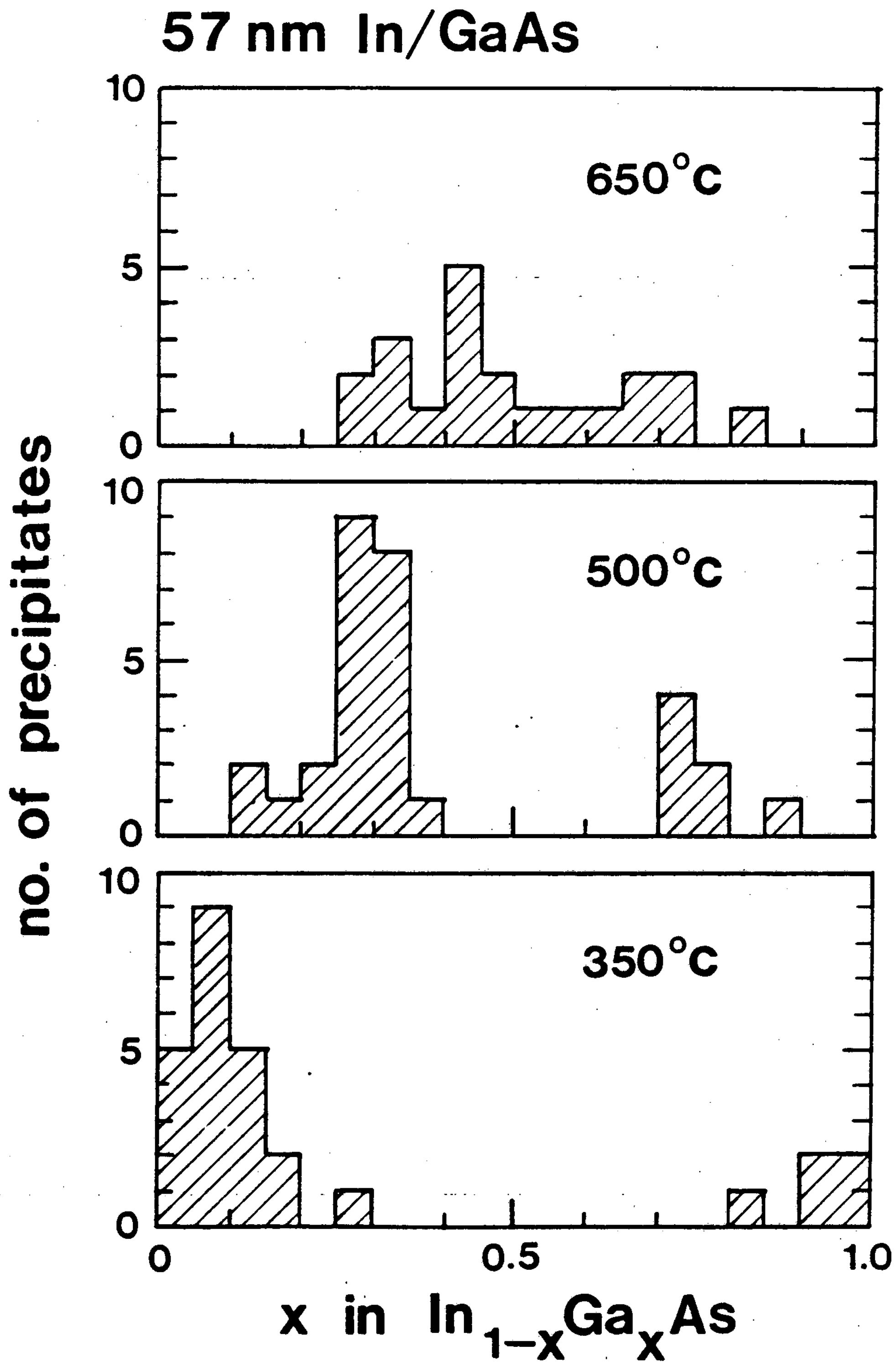

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Fig. 41. Histograms of the numbers of the $In_{1-x}Ga_xAs$ precipitates with respect to composition x from the three samples annealed at the different temperatures (350°C, 500°C and 650°C).

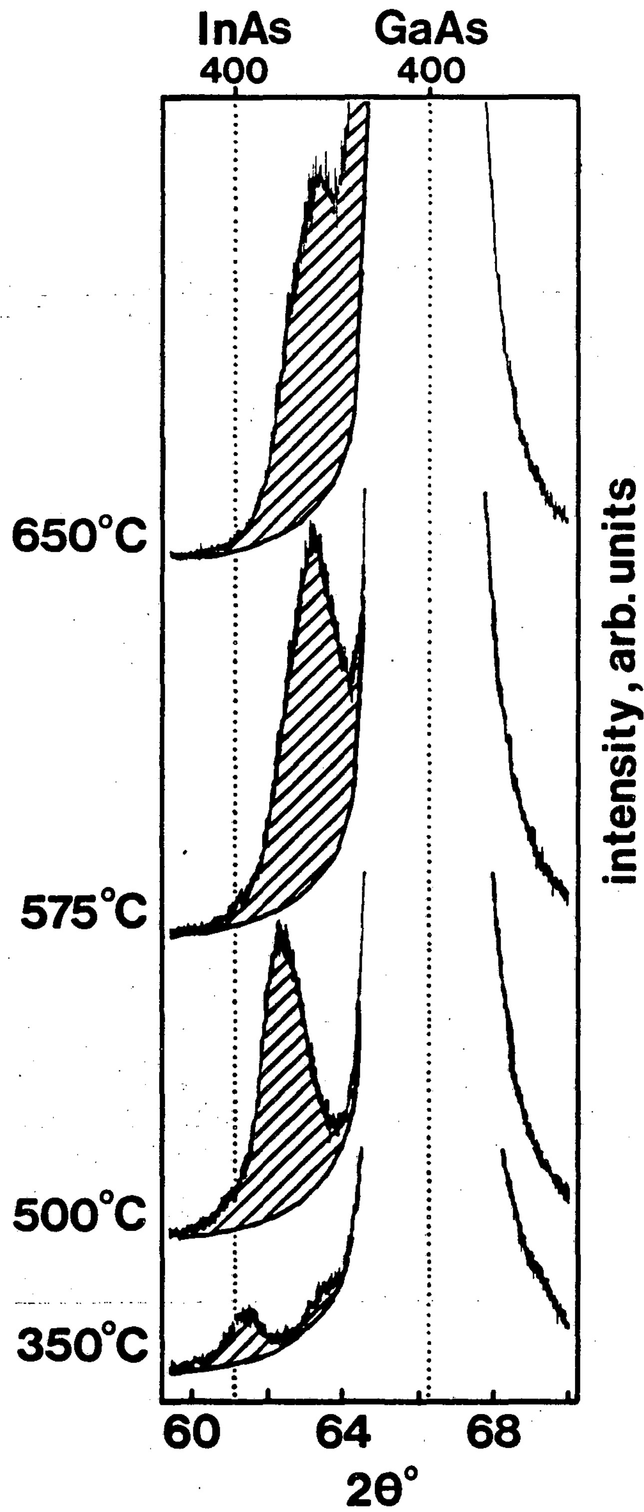

Fig. 42. Slow trace XRD patterns of the 400 reflections of as-deposited In on (100) GaAs and after annealing for 10 minutes at 350°C, 500°C, 575°C and 650°C, respectively (CuKα) radiation). Each trace is compared with the trace from the as-deposited sample (broken line).

not possible under furnace annealing conditions (slow heating and cooling) unless the annealing temperature is above the critical temperature, estimated in this study to be between 575 °C and 650 °C. If a graded layer is indeed necessary to form a low-resistance In-based ohmic contact to n-GaAs (i.e., to smooth out the InAs-GaAs conduction band discontinuity), the results suggest that fabrication of graded $In_{1-x}Ga_xAs/GaAs$ ohmic contacts by thermal reaction must involve annealing at temperatures above the critical temperature. Observation of ohmic conduction in In/GaAs samples annealed at temperatures significantly below T_C by Lakhani[17,18] can only be attributed to other mechanisms such as thermionic-field emission at small diameter protrutions in the $In_{1-x}Ga_xAs/GaAs$ interface.

4.2. Discussion

4.2.1. The In/GaAs Reaction Mechanism

The assumption is that the In-GaAs system rapidly approaches equilibrium after annealing. The observation that there is extensive reaction even at temperatures as low as 350 °C excludes solid state interdiffusion between In and Ga as the reaction mechanism for temperatures <650 °C. This is in agreement with a previous study[68] where the reactiion involving the dissolution of Ga and As into the molten In (melting T~156 °C) and the subsequent precipitation of $In_{1-x}Ga_xAs$ was discussed. In the reaction of the form

$$In\ (l) + GaAs \rightarrow In_xGa_{1-x}\ (l) + In_{1-x}Ga_xAs, \quad (22)$$

the presence of a liquid phase ensured that mixing was rapid and that the final states of the system, after annealing is close to equilibrium.

Such a reaction can be qualitatively understood by reference to a hypothetical isothermal section of the In-Ga-As phase diagram for $T<T_C$ as shown in Fig. 43. From this schematic diagram, it is apparent that when a limited amount of GaAs is involved in the reaction, as many as three phases, namely In-Ga(l), In-rich $In_{1-x}Ga_xAs$ and Ga-rich $In_{1-x}Ga_xAs$ can result. The mechanism of the In/GaAs reaction is proposed as that in the

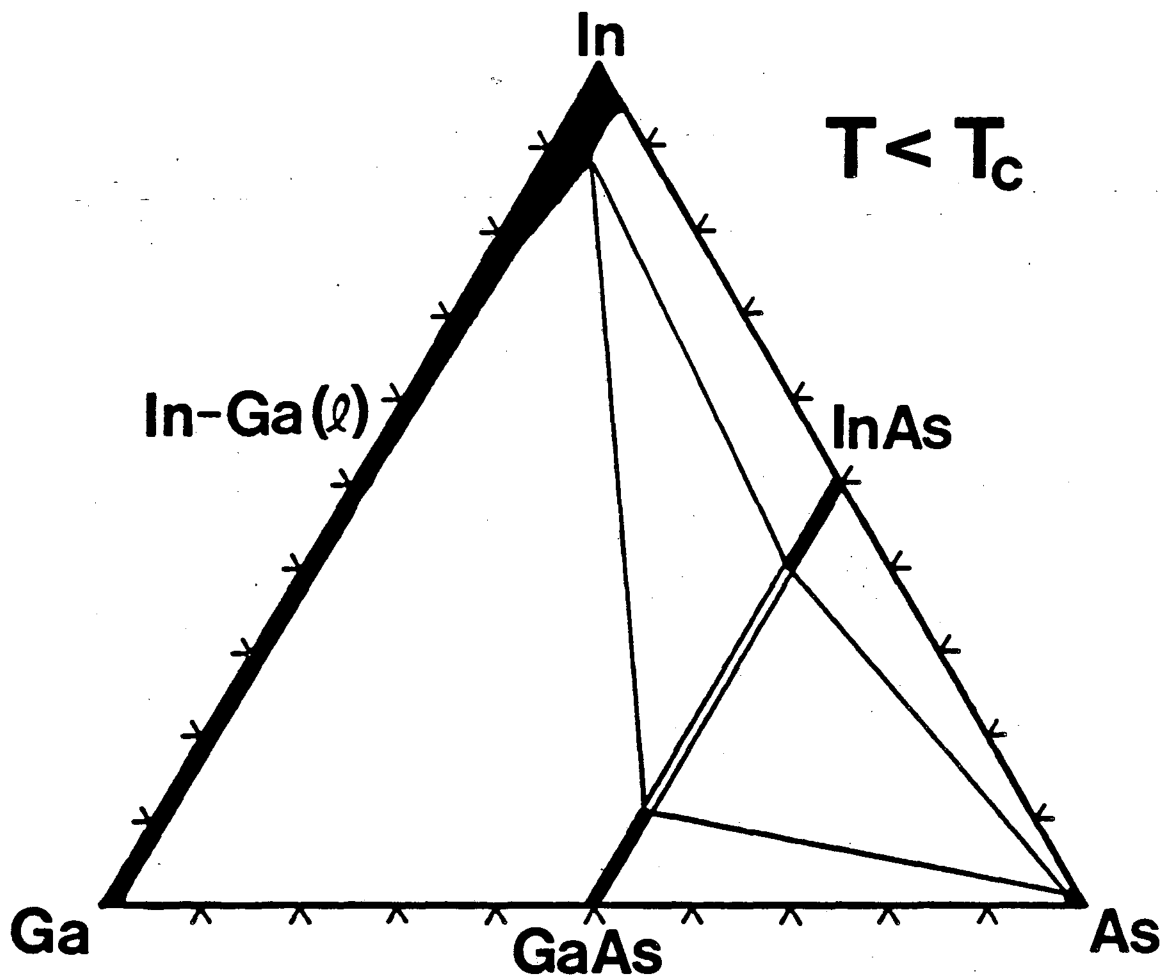

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Fig. 43. Schematic isothermal sections of In-Ga-As phase diagram at a temperature below T_C. Assuming no loss of arsenic during annealing, the average composition of the system remains on the vertical dashed line.

initial stages of the reaction, Ga and As are dissolved into the molten In so that the average composition of the system remaims on the vertical line connecting In and GaAs. As more Ga and As are incorporated into thhe molten material, i.e., as the molten In-Ga-As becomes supersaturated in Ga and As, the driving force for nucleation increases. Nucleation of $In_{1-x}Ga_xAs$ occurs at some time during the annealing treatment, most likely during cooling. The compositions of the phases formed depend on the degree of supersaturation at the time of nucleation. Misfit dislocations were observed only at the $In_{1-x}Ga_xAs$/GaAs interface and no diffraction spot streaking (indicative of compositional grading) was detected. These observations suggest that once a precipitate is nucleated, it continues to grow at the same composition. The strain energy or dislocation energy associated with spatial variations in composition will inhibit compositional grading.

4.2.2. Miscibility Gap in the InAs-GaAs System

The histograms shown in Fig. 41 determined by electron diffraction and EDS analyses provide the information of the phase boundary in the InAs-GaAs pseudo-binary system at two different temperatures. The histogram from the sample after annealing at 650 °C shows that there is no longer a miscibility gap at this temperature. The results of this study gives the first experimental data on the existance of the miscibility gap in the InAs-GaAs system, and shows that the critical temperature of this system is between 575 °C and 650 °C. Shortly after the completion of this study, Schultz[140] performed the investigations on the existance of the miscibility gap in the InAs-GaAs pseudo-binary system by using the In/GaAs, Ga/InAs diffusion couples annealed at various temperatures.

The figure 44 shows the results of the measurements of this study and Schultz's measurements along with the theoretical calculation of the miscibility gap in the InAs-GaAs pseudo-binary system (using the sub-regular model[140]). As can be seen in Fig. 43, the Schultz's measurements at 355 °C and 481 °C are consistent with the results of this study at 350 °C and 500 °C, respectively. The In-rich phase boundary measured by

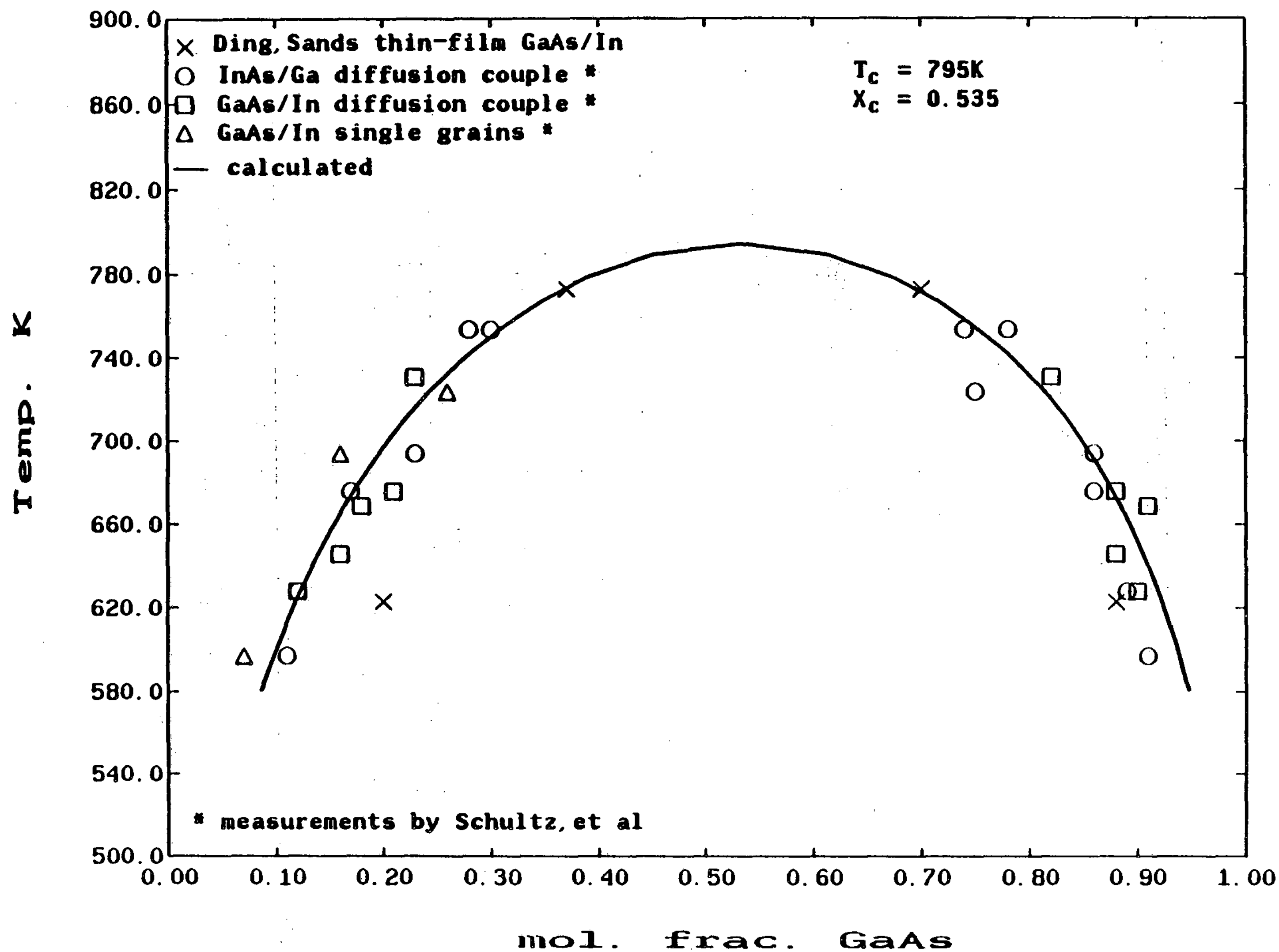

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Fig. 44. The calculated and experimental results on the miscibility gap of the InAs-GaAs pseudo-binary phase diagram are in agreement. (From Ref. 140)

Schultz from both the In/GaAs couple and the Ga/InAs couple at 355 °C (628K) also agree well with the value at 350 °C measured in this study. Since the thin In film can provide only a certain amount of indium for the In/GaAs reaction during annealing, the experimental conditions allow for a much greater degree of supersaturation as comparing with the In/GaAs and Ga/InAs diffusion couples. Therefore, the compositions of the In-rich $In_{1-x}Ga_xAs$ precipitates in the thin film case had much more scatter than those of the diffusion couples due to the precipitation of so much additional solid phase during cooling down to room temperature.

The experimental results described in this work provide direct evidence for the existence of a miscibility gap in the InAs-GaAs pseudo-binary system. It follows that the formation of graded $In_{1-x}Ga_xAs$ ($0 < x < 1$) layers by thermal reaction of In on GaAs is not possible under furnace annealing conditions (slow heating and cooling) unless the annealing temperature is above the critical temperature, estimated in this study to be between 575 °C and 650 °C. If a graded layer is indeed necessary to form a low-resistance In-based ohmic contact to n-GaAs (i.e., to smooth out the InAs-GaAs conduction band discontinuity), the results suggest that fabrication of graded $In_{1-x}Ga_xAs$/GaAs ohmic contacts by thermal reaction must involve annealing at temperatures above the critical temperature. Observation of ohmic conduction in In/GaAs samples annealed at temperatures significantly below T_C by Lakhani[17,18] can only be attributed to other mechanisms such as thermionic-field emission at small diameter protrutions in the $In_{1-x}Ga_xAs$/GaAs interface.

4.2.3. In-based Ohmic Contacts

The AuNiGe system has been used extensively as ohmic contacts to n-GaAs due to its reproducibility of low contact resistance of $\sim10^{-6}$ Ωcm^2 and the ease of the fabrication by using conventional evaporation systems. However, this system is thermally unstable because the β-AuGa phase has a low melting temperatue of 375 °C. Since the subsequent processing involves 400-500 °C annealing after contact formation, this will be a potential

problem for the fabrication of very large scale intergrated devices. For example, it will limit the fabrication of submicron devices by deteriorating the spatial resolution by the contact edge slide (up to 0.47 μm).[66] The formation of the protrusions into the GaAs substrate in this ohmic contact system is another problem for the submicron device fabrication, which could result in a nonuniformity of contact resistance in devices.

Thus, development of a new ohmic contact system with thermally stable and uniform interface is needed to form a desirable and reliable contact to n-GaAs. Woodall et al.[16] demonstrated that an epitaxial layer of n-$In_{1-x}Ga_xAs$ grown by MBE on n-GaAs which is graded in composition from 1.0 at the interface to 0.2 at the surface will produce a structure with a nearly zero Schottky barrier height for the metal-$In_{1-x}Ga_xAs$ interface and hence a low resistance ohmic contact (a low contact resistance of $5 \times 10^{-5} < R_c < 5 \times 10^{-6}$ Ωcm^2 for a Ag/n-$In_{1-x}Ga_xAs$/n-GaAs MESFET structure. In 1984, Lakhani[17,18] reported that an ohmic contact to n-GaAs with a contact resistance as low as 1.2×10^{-5} Ωcm^2 can be obtained by simply annealing thermally evaporated In film (600 nm thick) on GaAs at 350 °C. Lakhani[17,18] argued that the ohmic behavior can be attributed to the formation of graded $In_{1-x}Ga_xAs$ layer on GaAs, and the relative high contact resistance was a result of nonuniform reaction at the In/GaAs interface. A subsequent study of the structure and morphology of the In/GaAs samples before and after anneaing at 350 °C by Ding et al.[68,69] indicated that the nonuniform interface reaction of the In/GaAs samples is due to the intervening GaAs native oxide layer. The native GaAs oxide was found to effectively inhibit the In/GaAs reaction at 350 °C so that only local reaction between In and GaAs occurred through the pinholes and weak points in the oxide layer. Furtherfore, the $In_{1-x}Ga_xAs$/GaAs interfaces were observed to be structurally and compositionally abrupt to within ~3 nm. In this study, the plots of the number of the $In_{1-x}Ga_xAs$ precipitates vs. compositions for these different annealing temperatures (350, 500 and 650 °C) reveal experimentally the existence of an InAs-GaAs miscibility gap with a critical temperature of between 575 °C and 650 °C. The previous study on the effect of the interven-

ing oxide and the present investigation on the existence of the miscibility gap helped understanding the mechanism of the In/GaAs reaction and provided the detailed information for the development of In-based ohmic contact systems.

To form In-based ohmic contacts to n-GaAs with a low resistance, two major factors have to be taken into account, the intervening GaAs native oxide and the existence of the miscibility gap in the InAs-GaAs pseudobinary system. The GaAs native oxide layer can be removed by either heating the GaAs substrate under ultra-high vaccum conditions (10^{-11} Torr) at temperatures of ~600 °C to desorb the native oxide, or depositing a thin intervening metal layer which can penetrate the oxide layer to permit a uniform reaction at the In/GaAs interface. The influence of the miscibility gap on the In/GaAs reaction can be eliminated by annealing the contacts at the temperatures above the critical temperature T_c (between 575 °C and 650 °C in this study).

Recently, In-based ohmic contact systems have been extensively studied in attempts to form thermally stable contacts with low contact resistance. In these studies,[20,22,25,141] transition metals, Ni, Pd and Pt have been used as intervening layers between the In film and the GaAs substrate to eliminate the primary limitations, i. e., the low melting point In-Ga product phase (~16.5 °C) and the lateral nonuniformity of the reaction caused by the native GaAs oxide. A sysmetic study by Sands et al.[142,143] shows that Ni, Pd and Pt can penetrate the GaAs native oxide layer during reactions with GaAs to form the phases Ni_xGaAs, Pd_xGaAs and $PtAs_2$, respectively. Furthermore, these three transition metals react with In to form intermetallic compounds, e. g., Ni_3In, PdIn and Pd_3In_7 which have high melting temperatures. Since annealing temperatures required for the formation of these contacts (300-500 °C) and for the subsequent processing (500 °C) are significantly below the melting points of these intermetallic compounds (800-1300 °C), the contacts are thermally stable throughout the annealing cycle for the device fabrication.

The TEM and electrical study of an In/Pd metallization on n-GaAs by Allen et al.[22] suggests that the regrowth of $In_{1-x}Ga_xAs$ by the reaction of In (or $PdIn_3$) with Pd_xGaAs

may have occurred. It was proposed by Sands[144] that the formation of an interfacial $In_{1-x}Ga_xAs$ layer necessary for the ohmic contact characteristics is a result of the reaction-driven decomposition of the first transition metal-GaAs product phase. The mechanism of solid phase regrowth by reaction-driven decomposition of intermediate phases as a method to achieve laterally uniform epitaxial layers at low reaction temperatures ($< 500\,^\circ C$) has been discussed thoroughly by Sands et al..[144]

The In-based ohmic contacts recently developed by Murakami et al.[25,141] show that NiInW contact system forms thermally stable, low resistance ohmic contacts to n-GaAs. Ni was used to break the native GaAs oxide layer at the interface for the uniform reaction, and also to form an intermetallic compound with a high melting temperature which will provide additional thermal stability after contact formation. The top W layer was chosen primarily for its inertness as a cap layer, i. e., to provide a wide selection of materials for interconnection which should not react with the underlying contact metals. After annealing at 900 °C for 1 second, the contact resistance was found to be 3 x 10^{-6} Ωcm^2. The interface morphology and structure of the NiInW/GaAs samples before and after annealing were also studied. The results show that the contacts are thermally stable at 400-500 °C after annealing for ~100 hours. The thermal stability was believed to be due to the formation of the intermetallic compound $InNi_3$ which has a high melting temperature.[141] The formation of the $In_{1-x}Ga_xAs$ phase at the interface was considered to be responsible to the low contact resistance.

As a continuation of this study, a Pd/In/Pd/GaAs sandwich system was designed for a thermally stable ohmic contact with low contact resistance. Palladium was used to penetrate the native GaAs oxide for uniform interface reaction, and to form InPd intermetallic compound which has high melting temperature (1285 °C). The ratio of the amount of Pd and In deposited on the GaAs substrate was chosen to form a top layer of InPd intermetallic compound and interfacial $In_{1-x}Ga_xAs$ layer. The electrical measurements show that after a series annealings (250 °C for 10 minutes and 530 °C for 5

seconds), the contact resistance was found to be as low as 6 x 10^{-6} Ωcm^2. The preliminary results of the structure study by x-ray spectrometry indicate that InPd intermetallic compound is the only phase found after annealings. It is believed that only a very thin interfacial $In_{1-x}Ga_xAs$ layer was formed so that the contribution of the $In_{1-x}Ga_xAs$ phase on the intensity of the x-ray peaks is much smaller than those from the GaAs substrate and the InPd intermetallic compund formed after annealing. Detailed interface morphology and structure of the InPd/GaAs samples are needed to be studied by TEM in order to further understand the reaction mechanism and improve the interface uniformity and contact resistance.

As discussed above, the low contact resistance in the InNiW/GaAs and the PdIn/GaAs systems can be attributed to either the formation of graded $In_{1-x}Ga_xAs$ layer at the interface or two low barriers in series at the metal/$In_{1-x}Ga_xAs$ interface and the $In_{1-x}Ga_xAs$/GaAs interface. It has been reported that a $In_{1-x}Ga_xAs$ layer with a thickness of about 20 nm at the interface should be enough to form an ohmic contact with low contact resistance.[21]

It is apparent that In-based systems will play a role for the future development of thermally stable, low resistivity, and shallow ohmic contact tohe n-GaAs. However, as discussed by Sands,[145] there rae other factors preventing the application of indium for ohmic contacts in GaAs devices. For example, the as-deposited In thin film tends to form In islands instead of a uniform In thin layer, and also the In-Ga phase as a product of the In/GaAs reaction is liquid at room temperature which is not suitable for device application.

5. SUMMARY

This research was performed to investigate the interface morphology and structure of the metal/GaAs contacts before and after annealing at temperatures up to 950 °C for the purpose of further improving and developing thermally stable metallizations on GaAs. The principal conclusions of this investigation are summarized as followed:

1. Nb/GaAs Contacts

The interface morphology and structure of Nb/GaAs contacts have been studied before and after RTA at 600 °C and 700 °C for 10 seconds.

(a) A preferred orientation relationship between the as-deposited Nb and the GaAs substrate was revealed by electron diffraction analysis: $(\bar{1}11)_{Nb}//(001)_{GaAs}$ and $[111]_{Nb}//[110]_{GaAs}$. The presence of this preferred orientation relationship indicates that the oxide layer does not cover the substrate surface completely.

(b) The Nb/GaAs interface remains sharp after RTA at 600 °C for 10 seconds. However, new phases such as Nb_3Ga_2, Nb_3Ga, Nb_3As and Nb_4As_3 were formed in the thin film due to interface interdiffusion. The improved electrical properties of the diodes are attributed to this abrupt interface between the thin film and the GaAs substrate.

(c) Annealing at 700 °C resulted in a dramatic interface reaction between the Nb and the GaAs substrate with high concentration of structural defects such as microtwins and staking faults in the film. Two major phases, Nb_5Ga_3 and Nb_4As_3, were formed during annealing. Degradation of the electrical characteristics of the diodes was a result of the rough interface and high desity of the microdefects at the interface. the interface interdiffusion occured

2. NbN/GaAs Contacts

The NbN/GaAs contacts have been studied by transmission electron microscopy and

x-ray diffractometry. The results are shown as below:

(a) The as-deposited NbN thin film has been identified to have a composition of Nb_4N_3 by electron diffraction analysis. The Nb_4N_3 has a polycrystal structure with an average grain size of about 6 nm.

(b) Annealing at 800 °C for 10 seconds resulted in a phase transformation from Nb_4N_3 to NbN with some small Nb particles as a result of the reaction $Nb_4N_3 \rightarrow 3NbN + Nb$. The improved I-V characteristics of the diodes is considered to be attributed to the sharper interface between the NbN thin film and the substrate.

(c) A phase transformation from Nb_4N_3 to Nb_3N occurred during RTA at 850 °C. Interface interdiffusion resulted in a layered structure. The top layer was identified to be Nb_3N and the interfacial layer is still unknown because it is too thin (~2 nm) to be identified by TEM. This interfacial layer was considered to be responsible for the observed changes of the electrical characteristics since the thermionic emission may not be dominant carrier transport mechanism for the diodes.

3. TiN/GaAs Contacts

The interface morphology and stability of the TiN/GaAs contacts before and after annealing at 500 °C, 700 °C and 850 °C by RTA for 10 seconds have been investigated by transmission electron microscopy and electron diffraction analysis.

(a) The as-deposited TiN thin film has been found to have a columnar structure. The formation of the pocket-like protrusions was observed after annealing at temperature above 500 °C. After annealing at 700 °C and 850 °C, these pockets became larger with some newly formed pockets.

(b) Outdiffusion of As or Ga and As through the columnar grain boundaries in the thin film has been suggested as a possible mechanism for pocket formation. It has also been

proposed that a loss of As or Ga and As upon annealing and pocket formation near the interface might be the cause of the observed changes of electrical characteristics, e. g., the barrier height enhancement and the decrease in contact capacitance.

4. WN_x/GaAs Contacts

The interface morphology and stability of the WN_x/GaAs contacts before and after annealing at high temperatures ($> 700\,^\circ C$) under different conditions have been investigated by TEM and XRD analysis.

(a) The as-deposited WN_x film has been found to have a polycrystal β-W structure. Annealing at temperatures up to 850 °C did not change the interface morphology significantly under all annealing conditions, but polycrystalline β-W transformed to α-W and WN_x phases, with WN_x in intimate contact with the GaAs substrate.

(b) Pocket-like protrusions beneath the original interface were observed after RTA at temperatures above 900 °C. Outdiffusion of As or Ga and As along the grain boundaries is considered to be the most likely explanation for the formation of these pockets. These pockets may be partly responsible for the enhancement of barrier height after RTA at temperatures above 850 °C.

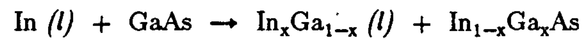
5. In/GaAs Contacts

The In/GaAs samples have been annealed at 350 °C, 500 °C, 575 °C and 650 °C for 10 minutes to investigate the existence of the miscibility gap in the InAs-GaAs pseudobinary system, and to understand the mechanism of the In/GaAs reaction.

(a) The experimental results from the analytical and high-resolution electron microscopies and x-ray diffraction provide direct evidence for the existence of a miscibility gap in the InAs-GaAs pseudobinary system with a critical temperature between 575 °C and 650 °C. The results are consistent with the theoretical calculation and other experimental data.

(b) A schematic isothermal section of the In-Ga-As phase diagram has been proposed to help understanding the mechanism of the In/GaAs reaction and developing the In-based ohmic contacts to n-GaAs.

(c) The basic reaction between the In and the GaAs substrate involves the melting of In (> 156 °C), dissolution of the GaAs substrate and finally, precipitation of epitaxial $In_{1-x}Ga_xAs$. The reaction may be written as:



$$In\ (l) + GaAs \rightarrow In_xGa_{1-x}\ (l) + In_{1-x}Ga_xAs$$

6. CONCLUSION AND FUTURE WORK

The interface morphologies and structures of the Nb/GaAs, NbN/GaAs, TiN/GaAs, WN_x/GaAs and In/GaAs contacts have been investigated before and after annealing at various temperatures up to 950 °C. The results from the refractory metal nitride contacts to GaAs indicate that no significant interface reactions occurred between the refractory metal nitrides and the GaAs substrate after annealing at temperatures up to 800 °C-950 °C. Two different types of the interfaces were observed after annealing at high temperatures, a layered structure for the NbN/GaAs and the formation of the pocket-like protrusions beneath the original interface for the TiN/GaAs and the WN_x/GaAs contacts. The interface structure and morphology of these contacts then were used to try to explain the observed changes of the electrical characteristics of the diodes. The results show that the refractory metal nitrides are very attractive canditates for thermally stable contacts to GaAs, i. e., for the gate metal in the MESFET fabrication. As a comparison to the nitrides, Nb and GaAs reacts at 700 °C and forms rough interface. Therefore, Nb cannot be used as a gate metal since the gate metal is required to withstand high temperature process (~800 °C) for the MESFET fabrication.

For the In/GaAs contacts, the results show the existence of a miscibility gap in the InAs-GaAs psedobinary system with a critical temperature between 575 °C and 650 °C. Therefore, it is suggested to anneal In-based ohmic contact structure at temperatures above the critical temperature in order to form a graded $In_{1-x}Ga_xAs$ layer to smooth out the InAs-GaAs conduction band discontinuity, i. e., low contact resistance.

These results naturally raise many new questions regarding a basic understanding of these metallizations on the GaAs substrate from the interface structural, electronic and thermodynamic points-of-view. Future work is clearly necessary.

A systematic study on the mechanism of the pocket-like protrusions beneath the original interface and the correlated electronic structure at the interface between the refrac-

tory metal nitride and the GaAs substrate would be of both fundamental and practical interest. It would also be interesting to study the stoichoimetry of the GaAs substrate near the interface in order to really understand the cause of the observed changes on the electrical characteristics. For In-based ohmic contacts, further study of the Pd/In/Pd/GaAs system by annealing the samples at temperatures above the critical temperature of the miscibility gap in the InAs-GaAs pseudobinary system would be of practical interest. It is also important to anneal the Pd/In/Pd/GaAs system at ~500 °C for ~50 hours to test its thermal stability and reliability.

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