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Selective Area Metal Organic Chemical Vapor Deposition Approaches for Novel Electronics and Photonic Integration

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in Electrical and Computer Engineering

by

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September 2021

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PUBLICATIONS

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ABSTRACT

Selective Area Metal Organic Chemical Vapor Deposition Approaches for Novel Electronics and Photonic Integration

by

Simone Tommaso Šuran Brunelli

With the advent of things like autonomous vehicles, augmented reality, high-capacity wireless networks, and high performance computing, the ways in which we sense, process and transfer information are evolving, and this is driving innovation in semiconductor electronics and photonics. At the forefront of this evolution III-V semiconductors like indium phosphide (InP) and gallium arsenide (GaAs) present themselves as high performance materials both in electronics (high mobility, heterojunctions) and photonic (direct bandgap, light emission) devices. Growth of these materials is possible via metal organic chemical vapor deposition (MOCVD), an ideal tool because highly scalable and industry standard for high volume production and throughput.

In this work we explore several MOCVD selective area growth (SAG) approaches for the growth of III-V based technologies.

First, we further develop a type of SAG called template assisted selective epitaxy (TASE) as a way to integrate horizontal heterojunctions (HJs) in a laterally grown structure while also allowing for planar gating. We show successful growth of horizontal HJs of InAs, GaAs and InGaAs, included in InP structures and characterized to show abrupt interfaces and crystalline material. The orientation of the templates and the substrate is chosen so that a flat vertical facet appears at the growth front allowing for the HJs to be horizontal, unlike typical planar epitaxy, enabling the design of novel electronic HJ devices like a low energy triple-HJ tunnel field effect transistor.

We then explore how III-V materials can be integrated onto CMOS compatible silicon substrates via SAG to create a low defect density pseudo substrate for the subsequent regrowth of active gain materials and the integration of photonic devices. This is attempted by leveraging aspect ratio trapping effects of TASE on Silicon or SOI (silicon on insulator) while scaling its size to a large enough area to accommodate photonic structures like micro disk lasers.

Finally, we demonstrate a different SAG approach where deep (>5 micron) recesses are etched into (001) silicon. The recesses are deep enough to allow application of mature defect engineering techniques (low temperature buffers, defect filtering layers and superlattices) and obtaining an antiphase boundary (APB)-free GaAs micro ridge, while remaining underneath surface, facilitating coupling with adjacent waveguide structures.

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1 Introduction

1.1 Metal organic chemical vapor deposition

Metal organic chemical vapor deposition (MOCVD), also often referred to as metal organic vapor phase epitaxy (MOVPE), as the name suggests, is an epitaxial deposition technique used for thin films, starting from organometallic precursors that are delivered in gas phase. It is a major player in the deposition of III-V semiconductors, i.e. compound semiconductors that are alloys of the group III and group V elements of the periodic table, like indium phosphide (InP), gallium arsenide (GaAs). The substrates used are wafers that can vary in sized depending on the system and the type of growth, typically ranging from 2" to 12" in diameter. Precursors used are metalorganics (MO) delivered directly in their vapor phase or via a saturated carrier gas such as hydrogen (H_2). The CVD implies that the deposition occurs due to the precursors reacting chemically at substrate's surface, typically activated by temperature, that ranges between 450-700°C for phosphides and arsenides and can reach 1200°C for nitrides. The pressures used in the process are considered medium vacuum, in the range between 50 -760 torr. Typical growth rates for thin films used in optoelectronics are 0.3-1 nm/s depending on the material but can be pushed higher at the expense of material quality.

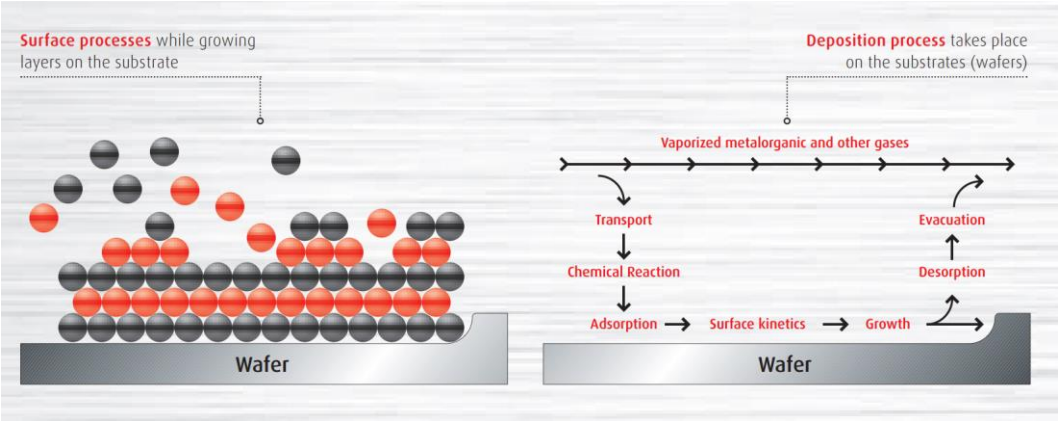

Figure 1. Schematic diagram of the key components of the epitaxial process via MOCVD. Source: Aixtron.

While other deposition systems had historically better thickness control of the layers grown, epitaxy via MOCVD has made a lot of progress and now competes. The higher growth rates, the relatively high growth pressures, and the gas phase nature of the technique, makes MOCVD a highly desirable method that is the key enabling technology for any future market with high growth potential.

1.2 Ex-situ characterization techniques

Material characterization is the first and most important tool to evaluate growth results, and it is a necessary part of the iterative process of optimization. Here I list some of the available characterization techniques available to the

MOCVD grower, focusing on the ones that I personally and extensively used throughout the work described in this dissertation.

1.2.1 Visual inspection and optical microscopy

Via the naked eye or aided by an optical microscope, visual inspection of the sample surface can immediately provide feedback, especially negative feedback. A milky, hazy appearing surface caused by light scattering, for example, suggests roughness, whereas a shiny reflective surface suggests smoothness. As another example, crosshatching visible to the naked eye may appear if a strained layer that has surpassed its critical thickness relaxes thereby producing defects. Large cracks can appear due to thermal stress. These may occur when a sample is subjected to thermal cycles or rapid heating or cooling ramps, especially if the sample consists of layers with mismatched thermal expansion coefficients that would generate strain.

1.2.2 Atomic force microscopy

Surface topology at the micro and nanoscale can reveal a great deal regarding the material quality and the nature of growth. Root mean square (RMS) roughness is a common figure of merit used to compare quality of growth from run to run. Absolute values of RMS are also considered when further processing and/or regrowth follow the initial epitaxy. Atomic force microscopy (AFM) is typically

used to measure average surface roughness. A 1x1 μm^2 area is typically sufficient to capture a representative area, but this will of course depend on the average size of topographic elements.

Epitaxial growth can proceed in different growth modes, where new epitaxial layers are formed in different ways. In its most basic categorization, three different growth modes are possible for vapor phase growth: Volmer-Weber mode has adatom-adatom interactions dominating leading to the formation of clusters or islands that eventually coalesce and planarize; Frank van der Merve mode favors precursor surface interactions leading to the formation of a wetting monolayer followed by ordered layer-by-layer growth; in Stanski-Krastanov mode, epitaxy is a combination of the previous two and begins with a wetting monolayer first, with a change in surface energy, then followed by island formations and 3D type growth. These different modes can be captured by a nanoscale topology characterization such as AFM.

Another important information from topology at the nanoscale is the presence of steps in the growth plane. A “step” occurs when the crystal plane of the sample is slightly misaligned with the sample’s macroscopic plane, and the step forms to compensate. Steps are generally formed kinetically and, at equilibrium, will be spaced regularly. Even spacing of steps, observable via AFM, suggests stable and controlled growth parameters allowing epitaxy to proceed per surface energy minima, maximizing smoothness.

While not strictly a post growth characterization, it is worth mentioning that presence of steps is not only important in the final epitaxial film but can also be in the starting substrate's surface. An example of this is during the growth of group III-V semiconductors on silicon. This will be explored in more detail later and briefly summarized here. A polar mismatch exists between the silicon substrate and the III-V film that leads to a disorder in the group III and group V atoms during growth, creating a type of defect know as an anti-phase boundary (APB). Thermal and chemical treatments exist that lead to the formation of atomic double steps in the silicon surface that prevent APB formation. AFM can be leveraged to reveal the presence or absence of APBs.

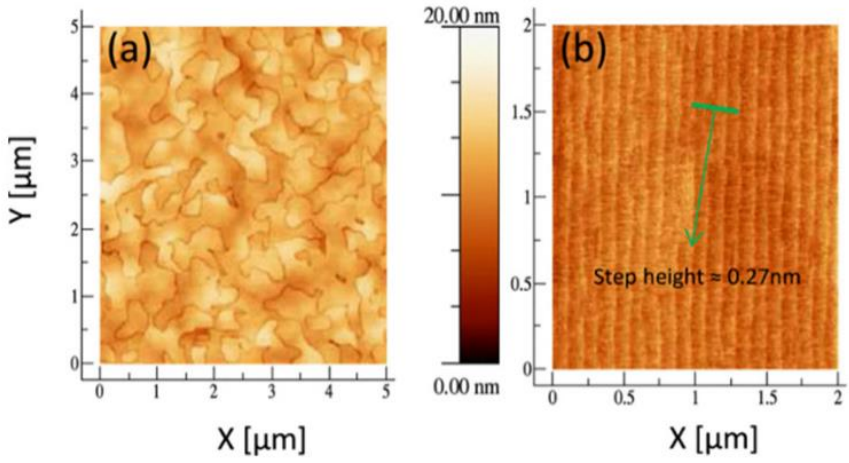

Figure 2. AFM images of 400 nm-thick GaAs grown on un-(001) Si with high density of randomly distributed APBs (left) compared to a double atomic step surface (right) obtained after growth optimization[1],

1.2.3 Photoluminescence spectroscopy

Photoluminescence (PL) is a key characteristic of III-V semiconductors. Photoexcitation of electrons from the valence band to the conduction band can be induced by incident light with sufficient energy. One pathway of relaxation of these exited electrons back into the valence band is light emission. The wavelength of this emission is characteristic of the material and can reveal several things. PL measurements are relatively simple and non-destructive, conducted in air, with an incident laser exciting the surface, optics collecting the output radiation, and a spectrometer to measure the wavelength and intensity of said emission.

The center of the emission peak will depend on the bandgap, caused by the main relaxation transition for that material. This is a simplification of course. Besides non-radiative relaxation phenomena like phonon emission, there are more than one radiative permitted transitions, but to first order, the III-V arsenide and phosphide semiconductors' direct bandgap typically yields a well-defined main peak that coincides with the direct bandgap spacing at the gamma point.

This makes PL a tool for quickly determining the composition of ternary compounds (bandgap being directly tied to composition), and combined with a measurement of strain, also quaternary materials. The presence of multiple clearly defined peaks could indicate a multimodal distribution of composition

(likely undesired), but, in the case of quantum dots, it is indication of the presence of an excited state due to quantum confinement.

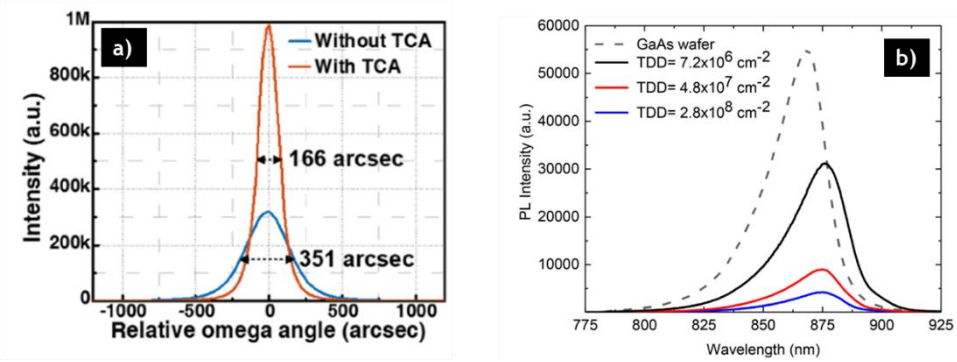

Figure 3. a) Overlayed PL spectra of two different GaAs on silicon growths showing a difference in FWHM [2]. b) Changes in PL due to the presence of defects [3].

The PL peak value can be used to compare samples, when all other measurement parameters are kept the same. In comparative measurements, it is best to use a reference sample as follows: prior to characterizing a new sample, adjust the laser output and photodetector collection time so that the emission value of a known reference sample is the same, then use the same parameters for the new sample. This is necessary to account for tool drift (be it degradation of the laser optical power output or wear on the optical fiber or other components on the collection side). Material quality can be inferred by emitted power. For example, the presence of threading dislocations or impurities in the lattice will act as non-radiative recombination sites, correlating emission intensity with defect density.

1.2.4 X-ray diffraction

X-ray diffraction (XRD) analysis is based on Bragg's law that correlates the angle of a diffracted X-ray beam with the lattice spacing of the analyzed crystal.

Rocking curve scans may assess the quality of the material by measuring the full-width at half-maximum (FWHM) of the primary peak.

Ayer's formulas [4] correlate defect density with the FWHM of the primary peak in a rocking curve scan. The most commonly used formula for dislocation density is:

$$D = K_{\alpha}/4.36\ b^2$$

measuring three rocking curves such as the (004), (115) and (117).

Peak broadening can occur for multiple reasons besides threading dislocation presence so generally speaking Ayer's law will always be an over estimation of defect density.

Measuring the fringe peak spacing with omega-2theta scans can be used to determine the thickness of a layer. Good practice is to avoid the 1-2 fringe peaks closest to the substrate peak or other layer peaks that will have their spacing affected.

1.2.5 Electron channeling contrast imaging

Electron channeling contrast imaging (ECCI) is a technique mainly used to identify and image defects at the surface of a sample. It is conducted in a

standard scanning electron microscopy (SEM) tool equipped with a backscatter electron (BSE) detector. A measurement is conducted by positioning a sample in such a way that patterns of scattered electrons known as Kikuchi lines (zoomed out with the sample out of focus so that the scanning beam is as perpendicular to the surface as possible). Then the beam is centered on a desired Kikuchi line/lines or intersections so that a channeling condition is obtained; this is achieved by rotating and tilting the sample, not by moving the stage. This is intuitive if we understand that the diffraction pattern occurs because of scattering of the electrons with the ordered crystal, not physical features. Once aligned in a channeling condition, the sample may be imaged. The channeling electrons "channel" through the crystal mostly unscattered, or more accurately, scattered deep enough in the material to not resurface, and hence undetected. When a defect is present, namely a dislocation or stacking fault, the strain surrounding it causes the crystal to create a deviation from this channeling condition that scatters electrons, detected by the BSE detector, and appearing as bright spots in the image. Each Kikuchi line represents a crystal direction, so the defects that can be imaged will be limited to the ones interfering with that specific crystal orientation (or orientations if the channeling condition is at an intersection of lines). This limitation, together with the fact that defects are manually counted by the user, makes ECCI a technique that inherently underestimates defect density, the opposite of using an XRD to estimate density through Ayer's law. While an Xray beam penetrates deep into the sample (range

of several micrometers), the scattered electrons that can be detected escape the sample only from the first few tens of nanometers only. This indicates that while an estimation based on Ayer's law [4] to a degree is influenced by the defect density in a thickness of material, ECCI only limits its measurement to actual defects that reach the surface;. in the case of III-V materials grown as virtual substrates, like the ones discussed in this thesis, those defects that reach the surface are relevant to device performance. A limitation of ECCI to consider could be the range of defect density in which measurements are useful or accurate. Since the technique is executed in an SEM tool, the size of the surface that can be imaged with a sufficient magnification is limited, therefore measuring relatively low defect density with ECCI may not be accurate.

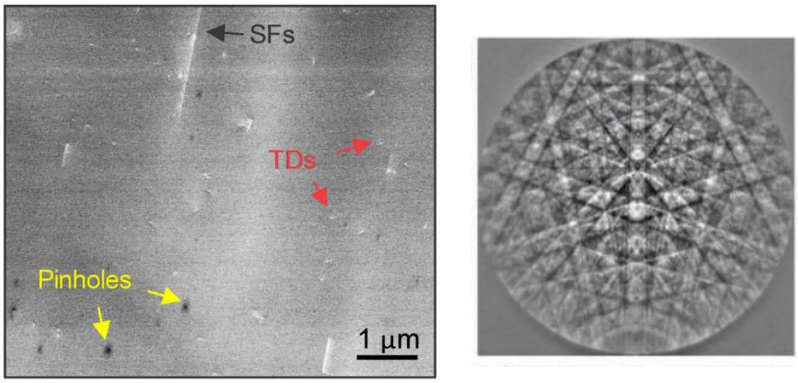

Figure 4. ECCI image of InP grown on silicon [5] showing the presence of surface defects (left). An electron diffraction pattern also known as Kikuchi lines as seen from the SEM [6] (right).

1.2.6 Secondary ion mass spectroscopy

Secondary ion mass spectroscopy (SIMS) is an elemental chemical analysis technique used to measure doping concentration in layer stacks. It is a destructive technique that uses accelerated ions to physically excavate a pit into the sample with an ion gun while detecting the sublimated atoms knocked from the surface (in their ionic form). Detection limits are as low as 10^{15} depending on the detected species, hence this technique is useful for doping concentration in doped layers (e.g., Si or Zn in n-InP and p-InP, respectively) as well as background contamination levels (e.g., H, C and O) albeit with less accuracy. Spatial resolution depends on the tool, but a lateral imprint of micrometers is typical for most tools, hence particular nanostructures are not suited for this technique. Depth resolution is also tool and parameter dependent but analyzing typical quantum well structures is possible and routine.

A typical SIMS stack consists of layers of a material, e.g., InP, doped at different levels (by using different precursor flows of a dopant during growth), separated by a marker, e.g., a few seconds (corresponding to a few monolayers) of arsenic precursor flow, that will be easily identifiable in the final measurement. In the case of dopants with a high diffusivity such as Zn in InP, averaging the concentration across the layer is typical. Fitting various value of doping levels versus dopant flows can then be used to design structures.

It is important to remember that counted ions in a SIMS measurement correspond to actual atomic concentration, while doping levels of actual interest are the concentration of active dopants that influence electronic properties like conductivity. A doped layer should be then also characterized with an additional technique, such as Hall Effect, to correlate physical atom concentration to active dopant level. This is not simply an offset/adjustment to doping level because in some cases the difference between the two measurements can be significant. For example, high flows of diethylzinc (a dopant precursor for Zn) can lead to the formation of clusters in InP, and high disilane (the dopant precursor for Si) flow can create aggregates. Both would result in a high concentration measured via SIMS despite a high portion of it not participating in electronic properties.

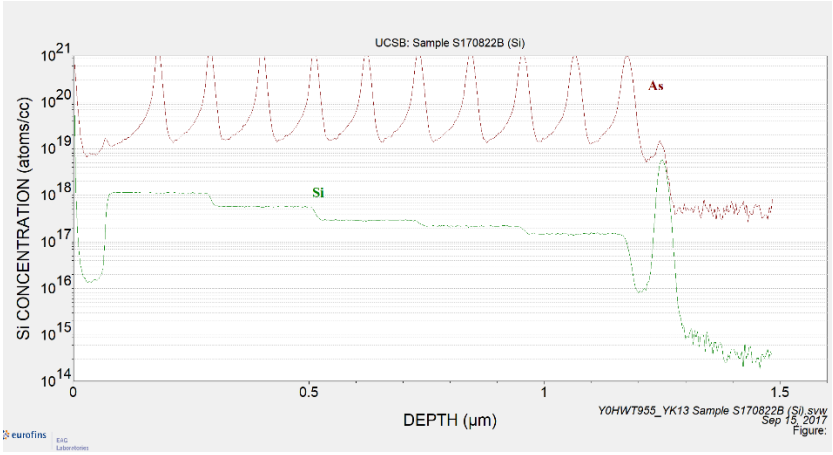

Figure 5. Example of a SIMS measurement showing different intentionally Si-doped layers of InP marked by As spikes. Also visible is a spike in the Si signal due to surface contamination at the growth interface.

1.3 Selective area growth

1.3.1 Principles

It is possible to use, instead of a bare wafer or sample, a surface that has been lithographically patterned with a mask that leaves part of the substrate surface exposed to the growth environment. MOCVD growth occurs when the gas phase precursors react between them on the surface. Save for undesired gas phase reactions like adduct formations, more common in III-N than phosphides and arsenides where they are virtually absent, it is the surface reactions that dominate growth, with the surface energy of the substrate directly contributing to the reaction and influencing the surface mobility of adsorbed molecules and atoms.

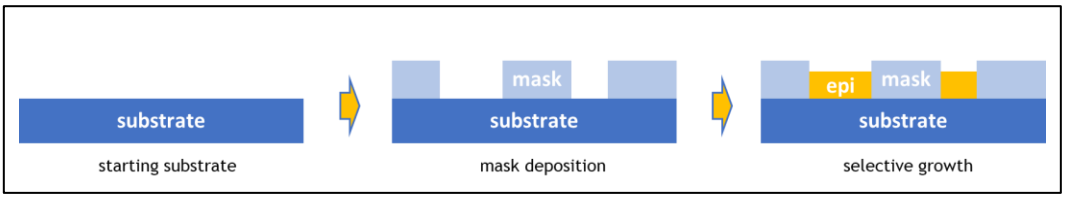

Figure 6. Basic steps for selective area growth process.

With an appropriate choice of mask and growth window then, the surface energies involved will make it so that growth reactions occur preferentially on the exposed area of the substrate. For a highly selective growth, if reaction does occur on the mask, either surface diffusion of adatoms and admolecules is sufficient to either migrate them to the unmasked area, or desorption back into

the gas phase occurs. Common masks used are deposited dielectric hard masks or thermal oxides, mainly because these must sustain the growth temperatures.

1.3.2 Loading effect

Precursors in MOCVD make up a small part of the total mass flow and are carried in the gas phase by a carrier gas. When in proximity to the substrate they will finally diffuse through the boundary layer with transport dominated by diffusion phenomena, driven by the partial pressure of the species.

Reactors are carefully designed to evenly distribute precursors across the entire substrate to achieve growth uniformity between, for example, the edge versus the center of a wafer. Different reactor designs account for this in different ways. In the case of a close coupled shower head design, efforts are put into the gas delivery system first, through the many inlets of the shower head itself, attempting to distribute gases as evenly as possible. The exhaust outlet resides beneath the susceptor so that gases are forced from the center to the edges, covering the surface. Finally, a rotating susceptor further homogenizes the distribution while affecting the boundary layer thickness.

In a horizontal reactor, precursors traveling across the sample are progressively consumed causing the partial pressure of said precursors to drop across the wafer. This would result in a gradient of growth rate across the sample. To compensate

for this the reactor ceiling is sloped, reducing the height gradually, in turn affecting the gas speed compensating for the reduced partial pressure.

Considering development efforts for reactor design, for planar growth, precursors are consumed evenly throughout the substrate surface. If a patterned substrate is used, precursors will be consumed locally at different rates, at higher rates at and near unmasked areas where epitaxial reactions cause a local decrement in partial pressure promoting diffusion from more concentrated volumes. The result is nonplanar isocore surfaces that follow the mask instead of being conformal to the substrate. In turn, uneven partial precursor pressure leads to uneven growth since growth rate is driven by group III availability at the growth interface.

Gibbons et al. [7] showcase this effect by performing selective area growth experiments using a simple dielectric silicon dioxide (SiO_2) mask consisting of stripes separated gaps. After growing InP at typical growth conditions and measuring the profile of the surface with a surface profiling tool (e.g., Dektak), it is clear that growth rate enhancement near the mask edges occurs. This is observed by identifying an “excess thickness” compared to the thickness in the “field,” i.e., far away from the masked area. The fill factor of the entire sample was small, so growth rate in the field far from the mask during the experiment was comparable to the typical growth rate of InP for planar growths.

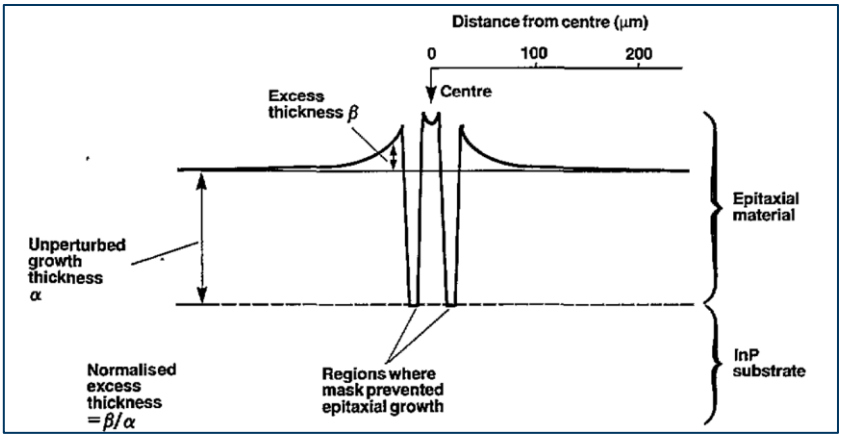

Figure 7. The profile of excess growth around the mask of a SAG sample showcasing loading effects in MOCVD. From [7].

A follow up experiment was performed where a deep trench was etched into the substrate near only one mask edge, in a zone that would be affected by loading effects, leaving the other side of the mask as before. After growth the "excess growth" profile was measured and analyzed. If surface diffusion dominated the loading effect, adsorbed species in the field would travel down and across the etched trench, lengthening the path of travel, and be captured in the trench. This would result in an asymmetry in the final growth profile between the sides of the mask. Asymmetry was not observed suggesting that the loading effect was dominated by gas phase diffusion.

Intuitively important elements that will influence the selective area growth results include parameters that affect this gas phase partial pressure profile. One such parameter is the size of the masked to unmasked area, generally referred to

as fill factor; the higher it is the more the loading effect and increase in growth rate. The range of the loading effect is limited to a certain distance from the mask edge after which the growth rate will be identical to that of an unpatterned substrate.

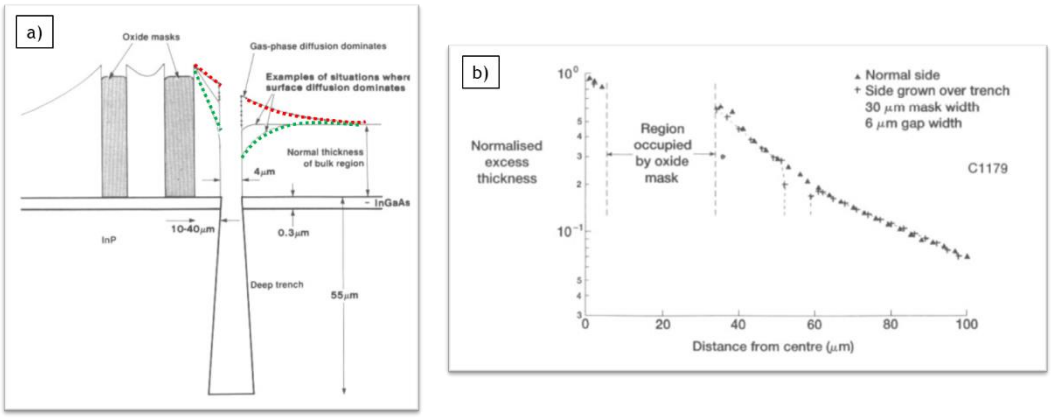

Figure 8. a) A model of expected profiles for surface (green line) and gas phase (red line) dominated diffusion in SAG. b) growth results demonstrating gas phase diffusion dominated effects. From [7].

Since selective area growth affects are determined by diffusion driven phenomena, and different precursors have different diffusion coefficients both in the gas phase for metalorganic precursors and on the surface as adsorbed species, it is unsurprising then that ternary and quaternary compounds sometimes demonstrate compositional variation. Experimentally, this is simply illustrated by measuring the photoluminescence change of a ternary compound like InGaAs when moving from a sampling location close to a mask to further away. An example is shown in Figure 9.

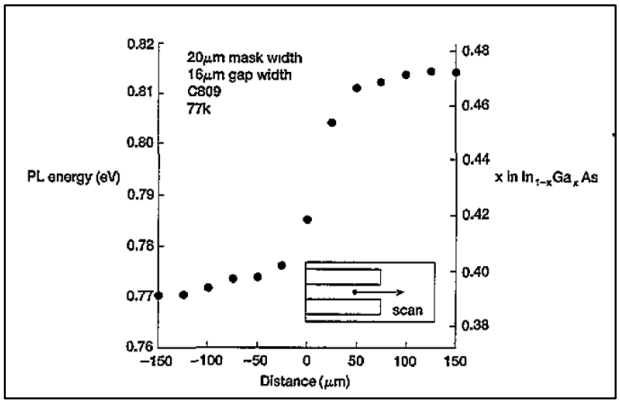

Figure 9. PL values of points near the mask edges (inset) of a SAG sample showing compositional variations due to loading effects.

1.4 III-V semiconductors on silicon substrates

1.4.1 Motivation for III-V integration on silicon

Silicon is the material of choice for electronic devices and has been for decades, penetrating in the lives of the general public with the advent of consumer grade electronic devices like computers and smartphones. Decades of development and technologic advancements in the CMOS industry led to the maturing of the silicon manufacturing infrastructure, capable of high quality and large-scale processing with high throughput. However, the electronic system performance is often limited by the input/output (I/O) and the power required to drive connections at today's high speeds.

Silicon photonics is historically more recent, but is advancing rapidly in recent times, not only demonstrating devices in the scientific literature but rising to large scale manufacturing outputting a number of active and passive devices, like modulators and photodetectors. Integration of multiple devices in photonic integrated circuits (PICs) enabled a wide range of applications from datacom and telecom sensors to light detection and ranging (LIDAR). In the datacom market, transceivers using silicon photonics are a multimillion unit market, needed to meet the increasing data rates demand. By benefiting from the advancements in electronics, silicon photonic devices are manufactured with compact sizes and excellent uniformity, with low costs and good scalability. The main limitation of the silicon photonics platform is the indirect bandgap of silicon itself, making it unsuitable for high performance active gain devices like lasers.

III-V semiconductors like InP and GaAs, thanks to their direct bandgap and high electron mobility, are the material of choice in optoelectronics and are the base for high performance devices. III-V electronic devices, for example, demonstrate higher speed operation and III-V photonic devices are highly efficient. Direct bandgap III-V materials also readily enable the realization of light emitting and laser devices, whereas indirect bandgap silicon does not. While dominating in the performance metric, III-V based devices suffer from relatively higher costs due to the more expensive substrates. Native InP and GaAs substrates are also commercially available in smaller sizes than silicon’s 300 mm wafers, limiting the economies of scale.

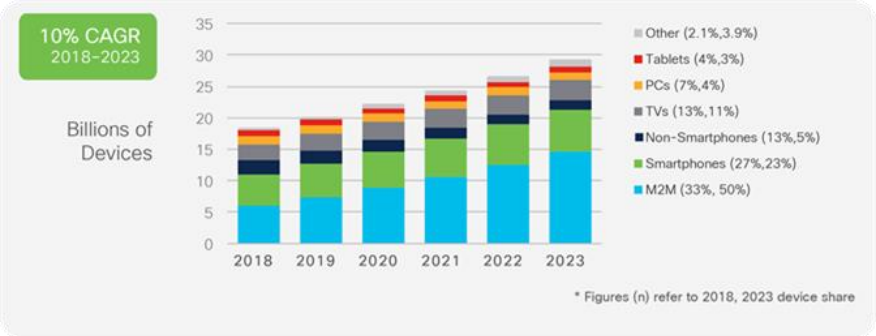

Figure 10. Projected increase in number of consumer devices. Source: Cisco.

The massive increase in demand for data and data processing by end users has exposed the limitations of tradition silicon semiconductor devices. Data centers, for example, now deploy more and more optical interconnects because copper cables consumer far too much power and cannot meet bandwidth requirements. Overall, the ways in which we sense, process and transfer information are rapidly changing and demand higher performing devices that can be manufactured in large volumes.

Bringing the two material systems, III-Vs and silicon, together and integrating them closely has been of historical interest. Integrating the III-V materials on silicon substrates would allow us to benefit from the intrinsic material properties of III-V materials and devices with the large-scale manufacturing capabilities of silicon, together with silicon based technologies. Si photonics could benefit from epitaxially grown III–V laser sources to realize fully integrated photonic integrated circuits. Integration of photonics with electronics would help with increasing the

speed and bandwidth of silicon photonics assemblies. And in general, high density of integration would both lower costs and help reduce power consumption.

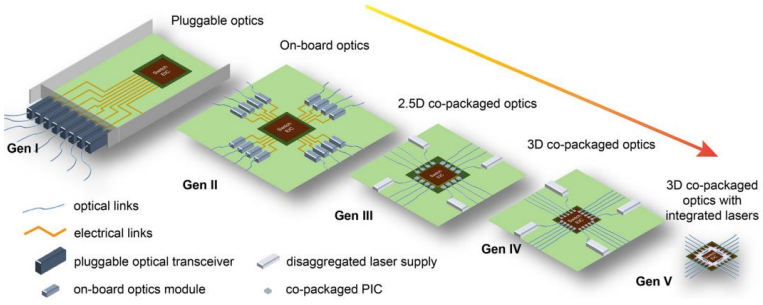

Figure 11. The evolution of integration approaches. From [8]

1.4.2 III-V on Si integration approaches

There are several techniques to integrate III-V materials and/or devices on a silicon substrate, all of them ultimately achieving the same goal but via significantly different pathways and with different challenges. These approaches can be grouped into three categories: co-packaging, hybrid/heterogeneous integration, and monolithic integration.

Co-packaging as the name suggests, only integrates at the packaging level, after III-V and Si chips have already been fabricated separately. For example, in Figure 12, silicon-photonic hybrid ring external cavity wavelength tunable lasers are realized with passive alignment of III-V gain elements to silicon passive waveguides, all on a common carrier.

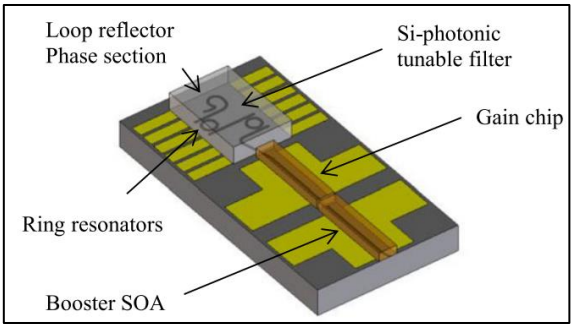

Figure 12.example of co/packaging integration. From [9].

This approach has the advantage of not adding complexity to or altering the fabrication of the chips themselves, since they are carried out separately. The chips then also can benefit from maximum native performance, not having suffered compromises. Disadvantages include the precise alignment required that could otherwise potentially diminish performance and yield. Cost of this process is also relatively high. Scalability in terms of throughput may be limited and the final product may be bulky, especially if intermediate optics elements are required for improving coupling efficiency or managing polarization or back reflection.

Hybrid/heterogeneous integration generally refers to the growth III-V devices on native substrates and then transfer of those materials to a silicon substrate. Flip-chip bonding integrates prefabricated III-V devices on silicon using solder bump or metal-to-metal bonding. Wafer bonding transfers bare III-V material to silicon and typically follows some co-fabrication. The III-V chips may be transferred with traditional pick and place tools or with micro transfer

printing, the latter of which transfers only a thin film.

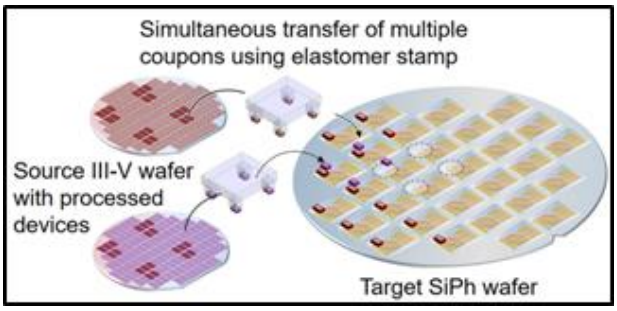

Figure 13. Chiplet transfer from III-V wafers to silicon wafers via micro transfer printing, as an example of heterogeneous integration. Source: Zhang et al., APL Photon. (2019)

Although these approaches vary in terms of maturity, they have been under development for a number of years, and all have realized high performance devices on silicon. These techniques also enable some degree of scalability. Disadvantages include required alignment accuracy (for flip chip bonding and micro transfer print), the sensitive bonding processes (especially for wafer bonding and micro transfer print), and the overall complexity and cost of the process and the equipment required. These techniques may also introduce some thermal management issues because of the bonding layers and the poor thermal conductivity of III-V materials.

Monolithic integration is the direct heteroepitaxy of III-V materials directly on silicon wafers. This refers to both unpatterned wafers and patterned wafers in the case of heteroepitaxy via SAG.

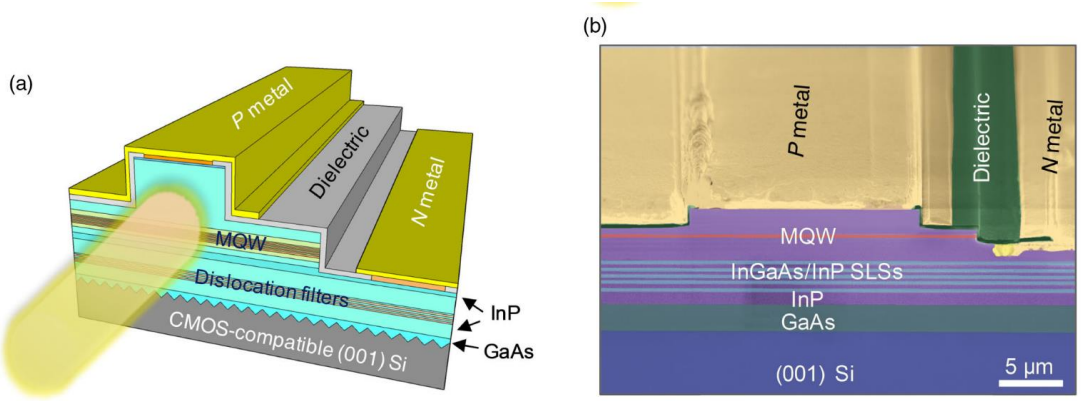

Figure 14. A laser diode directly grown on a CMOS compatible (001) silicon substrates via MOCVD [10]. a) diagram of the structure. b) SEM cryosection with false coloring.

This approach would provide the minimum overall cost, with devices fabricated directly on large silicon substrates and exploiting the very mature, high throughput infrastructure of silicon manufacturing. This approach may also allow for maximum integration density. The disadvantage of monolithic integration is inherent to heteroepitaxy that, due to the dissimilar nature of the materials, is subject to a large amount of material defects that can severely affect device performance, reliability, and lifetime. Despite this monolithic integration is considered the desired long-term goal of the industry to tackle the limits of current integrated electronic and photonic circuits.

1.4.3 Challenges of heteroepitaxy

To feasibly implement III-V materials on silicon, it is necessary to overcome some of the inherent challenges of direct heteroepitaxy. The main fundamental problems of III-V on silicon are the formation of material defects during growth, such as APBs, threading dislocations (TD), stacking faults (SF) and thermal cracking. These defects stem from differences in the material properties between III-Vs and silicon, including the difference in lattice spacing and coefficient of thermal expansion (CTE), as well as the polar nature of III-Vs.

	Si	**GaAs**	**InP**
Lattice mismatch (Å)	5.431	5.653	5.869
% mismatch with Si (%)	0	4.09	8.06
CTE mismatch (%)	0	119	76.9

Table 1. Material parameters for silicon and common III-Vs.

1.4.3.1 Threading dislocations

A lattice mismatch exists between all III-V materials and silicon. When a lattice mismatched material is pseudomorphically grown on a thick substrate, the lattice spacing will be initially accommodated via elastic strain, as illustrated in

Figure 15. The thicker the heteroepitaxial layer, though, the larger the strain accumulation. At a certain thickness this strain will be relieved, and this occurs via the formation of dislocations. The thickness when this happens is referred to as the critical thickness (h_c).

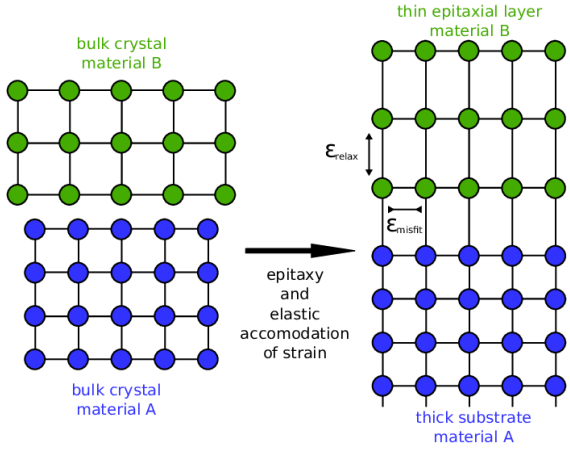

Figure 15. Lattice mismatched materials and elastic accommodation of strain.

A commonly used method to calculate the expected critical thickness is the one described by Matthew-Blakeslee[11], which define the h_c as:

$$h_c = \frac{b}{2\pi f}\frac{(1 - v\cos^2\alpha)}{(1+v)\cos\lambda}\left[\ln\frac{h_c}{b} + 1\right]$$

where b is the length of the Burgers vector for the dislocation, v is the Poisson ratio, α is the angle between the dislocation line and its Burgers vector, f is the lattice mismatch strain, and λ is the angle between the slip plane and the line in the film plane that is perpendicular to the intersection line of the slip plane and interface. Dislocations, by nature, cannot abruptly end inside a crystal lattice, so

they will extend inside the crystal up until the edge of the domain, or they will merge with other dislocations, if the Burgers vectors of each geometrically allow for this. Figure 16 shows an example cross section transmission electron microscopy (TEM) image of InP grown on GaAs grown on patterned CMOS-compatible (001) silicon. It is well known that the TDs introduce electronic states in the bandgap of III-V semiconductors, which act as non-radiative recombination centers. The dislocation density is also linked to degradation in device performance and lifetime.

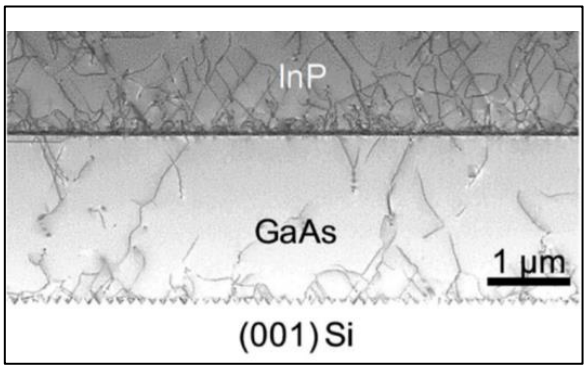

Figure 16. TEM cross section image of InP on GaAs on Si heteroepitaxy. Dark lines are threading dislocations generated at the heterointerfaces to relieve strain due to lattice mismatch between materials.

1.4.3.2 Anti-phase boundaries and domains

When attempting direct growth of III-Vs on (001) silicon, due to the polar III-V on non-polar silicon, and the presence of monoatomic steps on the surface[12][13], APBs are generated. Silicon is a diamond structure and mono-

elemental, while III-Vs are (typically) zinc-blende with the group III and the group V atoms residing on different sites of the FCC sublattices. During heteroepitaxy sometimes, the order is changed creating the planar defect APB as illustrated in Figure 17. The crystal domains separated by APBs are referred to as anti phase domains (APD).

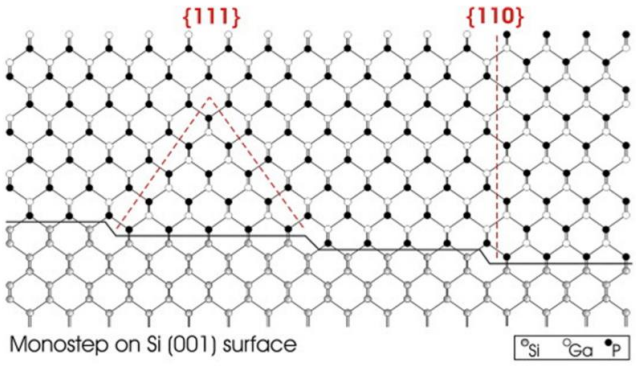

Figure 17. Illustration describing APB formation on monosteps of the Si substrate [14]

1.4.3.3 Thermal cracking

Heteroepitaxy of III-Vs always occurs at temperatures above ambient, meaning that the materials will experience temperature changes. Thermal expansion coefficients describe how much a material expands or contracts with temperature. Dissimilar CTEs can then cause thermal strain between the various layers, that upon cooling down from a 600°C growth temperature to room temperature (RT), for example, will contract at different rates and for different

extents. The accumulated thermal strain will sometimes relax by forming macroscopic cracks in the film[15] as illustrated in Figure 18.

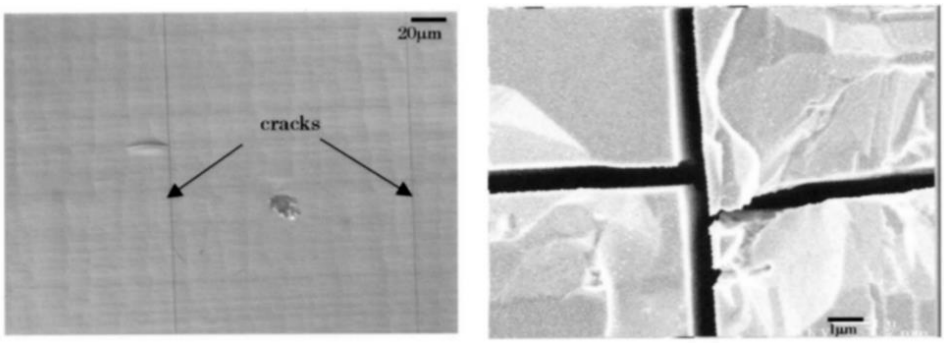

Figure 18. Cracks due to thermal stress induced during cooling for MOCVD growth of GaAs on silicon. From [16].

1.4.4 Planar heteroepitaxy of III-V on silicon

Monolithically integrating III-Vs on silicon substrates is desirable because it would enable the exploitation of the mature infrastructure of silicon to fabricate III-V devices. It would also enable the monolithic integration of silicon based and III-V based devices, since both "substrates" would be available on the same wafer, in proximity. Unfortunately, simply depositing III-Vs directly on silicon is not a viable option because the dissimilar inherent material properties would yield a defective product (see 1.4.3). It follows that most of the "III-V on Si" literature focuses on producing low defect III-V materials via several different techniques. Some of these, namely the most common and/or the ones used in the

chapters that follow, will be described here, with the intent of introducing the topic.

1.4.4.1 Buffer thickness

Threading dislocations have a chance to self-annihilate when they meet if their Burgers vector is the same but of opposite sign. It follows then that simply growing a thicker buffer may improve material quality, as illustrated in Figure 19. Low TDD values obtained this way are attractive for integrating III-V devices, but the costs and growth times associated with these results makes it less economical.

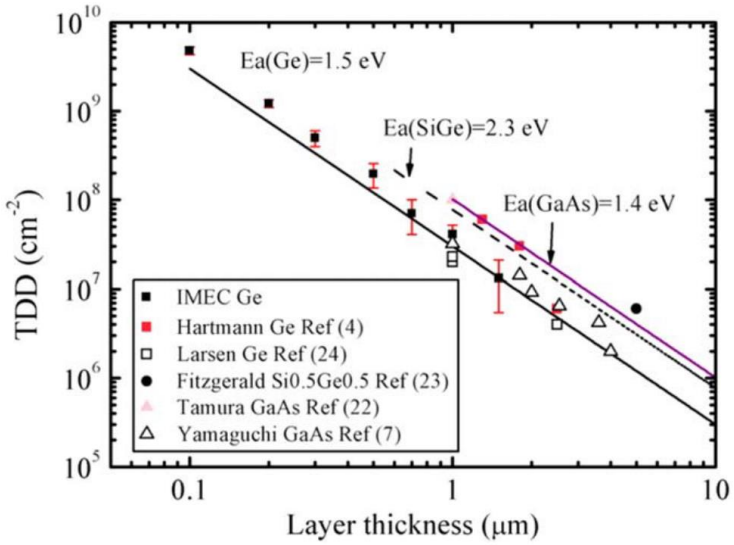

Figure 19. Threading dislocation density (TDD) as a function of the layer thickness of Ge, SiGe and GaAs deposited on Si substrates [17]

1.4.4.2 V-grooved silicon

As noted in the previous paragraph, APBs form in the III-V layers when growing on a silicon surface that presents monoatomic steps on the surface and the polar/non polar nature of the III-V/Si interface. This was true for (001) substrates; the use of highly miscut substrates does indeed prevent APB formation but does not necessarily yield smooth film surfaces. Unfortunately, miscut substrates are also not industry standard in CMOS fabrication facilities, so while of scientific interest, at the industrial level the use of miscut substrates is not ideal.

The same mechanism of growing on other planes other than {001} that does not induce APB formation is creating v-shaped grooves on the initial silicon wafer. This is typically achieved through patterning of the substrate with long strips of dielectric material, followed by anisotropic selective wet etching of the exposed silicon. The etch, commonly potassium hydroxide (KOH) or tri-methyl ammonium hydroxide (TMAH), being anisotropic, etches different crystal planes at different rates. The result is that the slower etch rate planes like the {111} are exposed. On (001) substrates this means that v-grooves are formed with exposed {111} facets. After the v-groves are formed the dielectric can be removed prior to III-V growth. So, while the starting wafer was patterned the growth itself can be considered planar because occurring on the entire surface. Examples of GaAs growth on v-grooved silicon are shown in Figure 20.

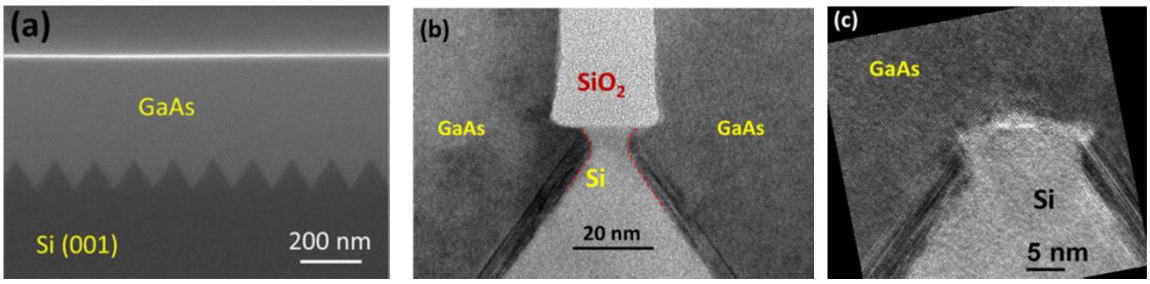

Figure 20. Cross section TEM images of GaAs grown on V-grooved silicon [18].

1.4.4.3 Low temperature seed layers

Prevention of APBs is important but also not sufficient for obtaining a high quality pseudosubstrate. The different lattice spacing between unstrained III-Vs and silicon will generate a high number of dislocations that are detrimental to devices. Growing on v-grooved silicon prevents APBs, TDDs in the order of 10^9 cm^{-2} are expected if no other measure is put in place. An initial low temperature seed layer to initiate growth was shown to homogeneously cover the silicon. TEM images of samples grown with low temperature buffers also show how there is a high dislocation density in proximity to the heterointerface, with a high number of TDs being confined in the buffer layer.

1.4.4.4 Thermal cycle annealing (TCA)

CTE mismatch between materials may generate defects and cracks if excessive. The same mechanisms behind the CTE mismatch could also be

exploited in our favor through what is known as thermal cycle annealing (TCA). This consists of ramping the temperature between a high and low value, typically holding those values for a few minutes each time, cycling one or more times. In this case the strain generated by the CTE mismatch is the driving force to encourage already existing dislocations to glide, statistically increasing the chances of them self-annihilating when meeting[3], [19]. A limitation of this approach is that it is the most effective in samples with a high number of dislocations. With low defect densities the chances of TDs encountering each other and annihilating are of course lower.

1.4.4.5 Intermediate lattice mismatch layers

When growing highly mismatched materials, e.g. InP to Si, it is very challenging to directly grow one on the other. It is useful instead to have an intermediate material with a lower lattice mismatch as transition. For example, GaAs has a 4% mismatch to silicon while InP is approximately 8%. Growing GaAs on v-grooved silicon, sometimes referred to as GoVS [2], is a common initial step before integrating InP on Si.

The same rationale applies to intermediate ternary layers with graded compositions. InGaAs with a 52% In composition is lattice matched to InP. One could be growing GaAs on silicon first, then slowly add In, up until $In_{52}Ga_{48}As$ before finally growing InP. The graded buffer will not be completely strain free of

course, but if the composition change is gradual enough the generation of misfit dislocations can be substantially reduced[2]. An example is shown in Figure 21.

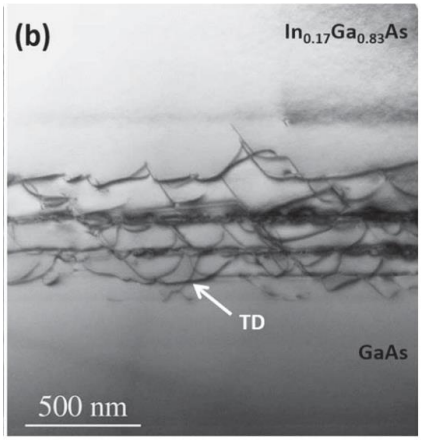

Figure 21. bright field TEM of an InGaAs graded buffer grown [20].

1.4.4.6 Defect filtering layers (DFLs) and strained layer superlattices (SLSs)

The purposeful use of additional strained layers grown within the buffer thickness to promote dislocation migration has proven effective with several different approaches. Ternary-binary SLSs DFLs have been widely used in GaAs/Si heteroepitaxy, including InGaAs/GaAs, InAlAs/GaAs, GaAsP/GaAs, and InGaAs/InP, In(Ga)AsP/InP, (In)GaP/InP for InP on silicon heteroepitaxy.

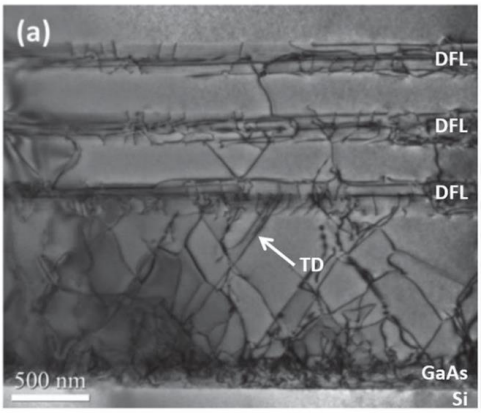

Figure 22. TEM image of GaAs deposited on a (001) Si substrate containing three DFLs of InGaAs/GaAs SLSs.[17]

The rationale behind these approaches is the same, to create a strain field, bending TDs into misfits migrating the dislocation horizontally towards the edge of the sample, plus promoting annihilation like with all dislocation movement. This occurs if the thickness of each SLS layer can accommodate strain due to the lattice mismatch, so has to be below the critical thickness that would otherwise generate new dislocations. At the same time is has to have enough lattice mismatch and thickness to generate enough strain to bend the existing TDs.

SLSs generally are included in multiple pairs of two lattice mismatched layers, creating a set. The set itself is often repeated throughout the epitaxial stack. The challenge then becomes balancing the defect reduction benefits with the additional cost hindrance of a thicker total buffer. Cross section analysis of samples with multiple DFLs, or alternatively growth interrupt experiments, can be used to evaluate the effectiveness of the approach as seen in Figure 23.

The SLSs commonly consist of multiple pairs of two lattice-mismatched layers alternately under compression and tension. If the thickness of each SLS layer is less than a certain critical thickness, which otherwise creates misfit dislocations, each SLS layer accommodates elastic strains caused by lattice mismatch. The strain field of SLSs can bend over and force the dislocations propagating upward to move laterally toward the edge of the sample, leading to the dislocation coalescence and annihilation. Noted that the SLSs should have enough lattice mismatch and thickness to generate strain required for bending dislocations.

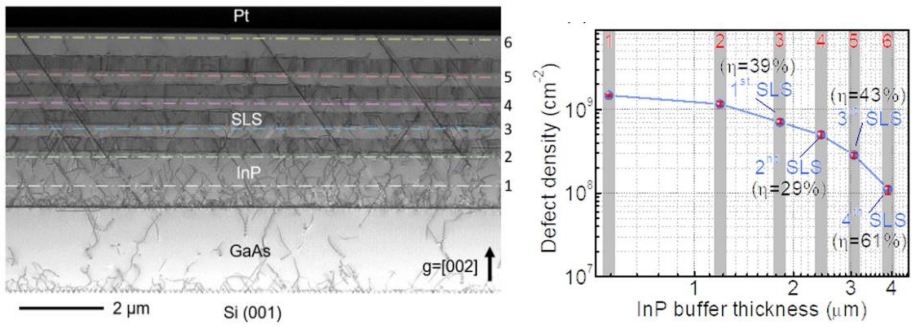

Figure 23. TEM cross section of multiple SLSs included within an InP buffer on a GoVs sample. The graph shows defect density reduction with the addition of multiple SLSs[21].

1.4.5 Selective area heteroepitaxy of III-V on Si

1.4.5.1 Aspect ratio trapping

Dislocations in all material systems have energetically preferred glide planes, so will "thread" at a preferred angle from where they are generated. Regardless of their direction though, all dislocations cannot end in the middle of a crystal domain but must reach the end of it. The concept of aspect ratio trapping (ART) exists in some types of selective area growth and it is based on creating an artificial boundary, typically a patterned dielectric mask, for dislocations to end into, instead of propagating into the epitaxial crystal. An example of this is in [20] where TDs are generated on the silicon surface but rise at an angle and end on the dielectric walls, so that the remaining epitaxial material is defect free.

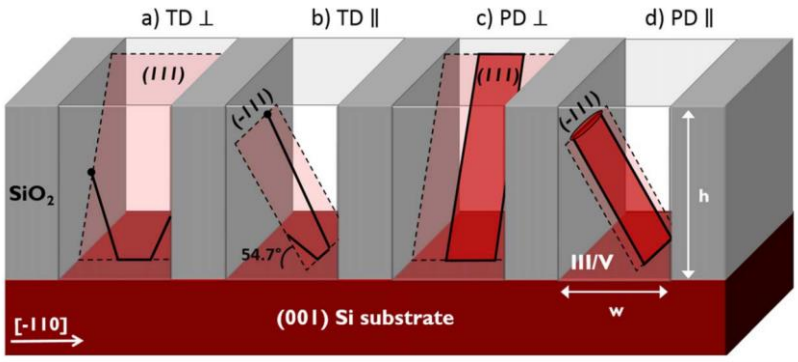

Figure 24. Diagram of aspect ratio trapping in narrow trenches. a,b and d show TDs being trapped by the dielectric mask while c) shows a TD that will surface.[20]

As the name suggests this is effective only for structures that have a high enough aspect ratio where the angle at which the TD rises makes it so that the TD will encounter a mask edge before making it to the surface. If the patterned dielectric, like in the example of Figure 24, consists of long stripes it is clear how it can only confine TDs rising in certain directions.

1.4.5.2 Defect trapping in v-groove mask

V-grooves have mostly been used as an APB elimination tool for planar heteroepitaxy with the dielectric mask being removed after the v-grooves are etched in the silicon. Some other SAG approaches use the same fundamentals but leave the dielectric stipes and aim to grow nanostructures directly inside the grooves. The benefit of this, beyond the APB reduction, is trapping of defects that occurs at the silicon undercut, right beneath the mask edge.

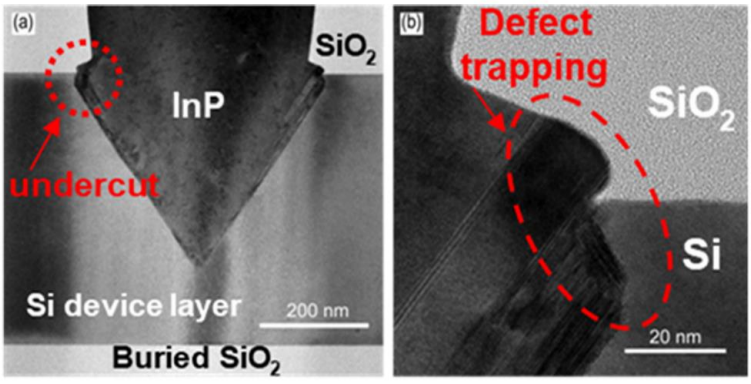

Figure 25. Cross-sectional HR-TEM images showing defect trapping by the Si undercuts for InP nanowires[22].

1.4.5.3 Epitaxial lateral overgrowth (ELOG)

Once dislocations are generated near the heterointerface due to the lattice mismatch they will develop towards the surface as threading dislocations, that, as stated previously, can only end at the edge of a crystal domain, not in the middle of one. ELOG[23] is a technique that relies on a dielectric mask patterned on top of a first heteroepitaxy. This mask will end most TDs and inhibit their propagation to the surface. Small openings in the mask will still allow a second growth to progress and "emerge" above the mask. Growth parameters can be tuned to promote later growth versus vertical, creating an overgrown layer that extends above the mask. The epitaxy directly above the mask opening will be populated by dislocations that will thread upwards, but the lateral growth will be defect free (see Figure 26).

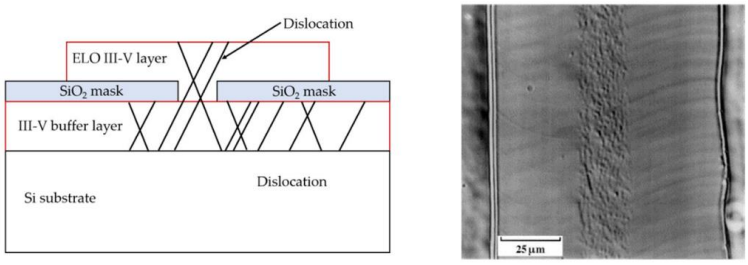

Figure 26. Diagram illustrating the defect confining mechanisms of ELOG (left) and an etch pit density micrograph of a layer grown via ELOG showing a high density of defects directly above the opening in the mask (right). [24]

1.4.5.4 Selective confined epitaxy

The dislocation trapping mechanisms so far described either rely on promoting self-annihilation or physically confining. The latter though was only shown in 2D geometries where at least one direction of growth was still left free, allowing a number of defects to continue their upwards developments and to finally surface. Selective confined epitaxy, as an approach, shifts this confinement of dislocations into a 3D geometry so that theoretically one could completely inhibit their propagation. Different works have been published with different names, and while they do differ in detail, they all share some fundamentals. These are illustrated in Figure 27 that shows the main steps in all confined epitaxy approaches. A 3D dielectric template is fabricated by removing a sacrificial layer leaving a cavity where the epitaxial growth will develop. The growth itself selectively initiates in a location deep inside the cavity that has an exposed area of the substrate material (referred to as a "seed"). Precursor gases will reach the seed entering the dielectric template through an opening in the top dielectric (referred to as "source hole") and travelling along the cavity.

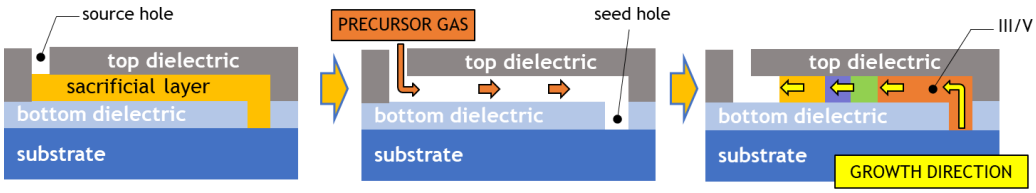

Figure 27. Diagram of the main steps in confined epitaxy within a dielectric template.

The first published work to our knowledge that describes this approach is seen in [25], [26] and referred to tunnel epitaxy, with the goal of creating an SOI platform with selective deposition of silicon via low pressure chemical vapor deposition (LPCVD). More recent work described very similar geometries but targeting InGaAs MOSFET (metal oxide semiconductor field effect transistor) devices selectively grown on a silicon substrate [27] with the goal of integrating III-V and silicon electronic devices, described as confined epitaxial lateral overgrowth (CELO). The main goal was to exploit the confined nature of the heteroepitaxy to confine the defect near the seed and then fabricate devices from the defect-free laterally grown material.

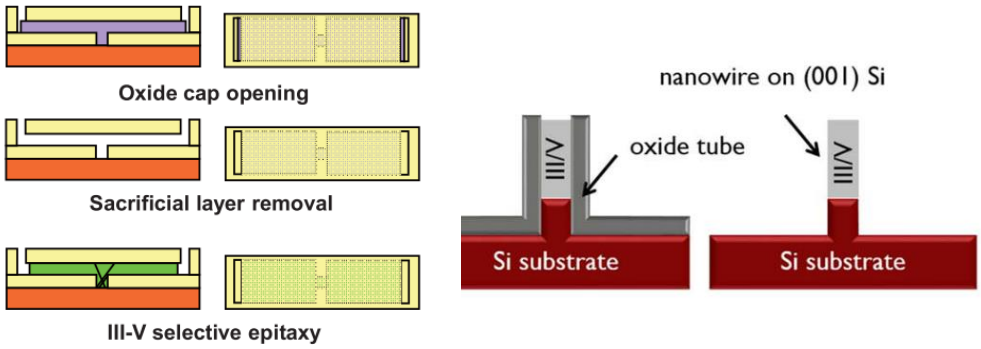

Figure 28. Diagram illustrating CELO [27] (left) and nanowires on Si via TASE [28] (right).

Template assisted selective epitaxy (TASE) was another named to initially describe the same approach as for the InGaAs MOSFET but later used to encompass other works which, despite having differing end goals, all shared having a dielectric template that forced the growth to proceed within it. III-V nanowires were demonstrated on silicon [29] directly grown inside the cavity of fabricated 3D vertical dielectric cylinders TASE was also used to laterally grow a larger pseudosubstrate used to then accommodate regrowth of additional material once the top oxide was removed[30]. Illustrations of CELO and TASE are shown in Figure 28.

2 Confined and selective epitaxial growth for a low energy triple heterojunction (3HJ) tunnel field effect transistor (TFET)

Epitaxial growth in confined 3D dielectric templates[25], [27], [28], referred to as Template Assisted Selective Epitaxy (TASE), has recently generated increased interest for multiple purposes such as integrating highly lattice mismatched materials[27], [28], [31], [32], as a virtual substrate approach for III-V on silicon integration[33]–[35], and as means to directly integrate novel nanowire devices[29], [36], [37]. TASE is a type of selective area growth that involves epitaxial growth of semiconductor materials within a confined structure that is formed with patterned dielectric materials[27]. Gas phase precursors enter the confined structure through a "source hole" and are exposed to an area of the semiconductor substrate, referred to as a "seed", where growth selectively initiates. The confined nature of the growth enables known defect trapping mechanisms characteristic of high aspect ratio structures, thereby enabling heteroepitaxy [38].

Early confined growth was investigated in [25], [39] for silicon on insulator (SOI) applications, but limited devices were fabricated and the technique was not widely adopted [25], [26], [39]. More recently, IBM Research demonstrated the integration of group III-V materials on silicon with TASE, sometimes also referred

to as confined epitaxial lateral overgrowth (CELO) [34][27]. Published results detailing TASE devices include MOSFETs [27], [28], [35], TFETs [35], [40], and gain material for lasers [41]. Limited studies regarding growth dynamics and template effects for TASE on Si have been published[42][36][43]. Additional work has leveraged TASE for defect trapping to grow GaN and has explored effects on a sub-micron scale using templates with cavity thickness less than 0.2μm[31], [32].

The TASE technique could also be leveraged for novel III-V nanoscale devices. TASE can rotate the direction of growth from vertical, typical of planar epitaxy, to being parallel with the substrate. Arbitrary orientation of the template allows subsequent growth to occur in a direction defined by the template, and to a predetermined final size and aspect ratio. It would be then possible to exploit the anisotropy of the energy bands in III-V semiconductors to design devices in such a way that electrons are confined in a specific crystal direction while transport would occur in another direction. If at the growth front inside a TASE template a flat, vertical facet could be realized, then heteroepitaxy would result in a horizontal heterojunction (HJ).

With transistors reaching their scaling limit, there is a need to move beyond traditional device designs[44]. Interesting novel devices have been proposed that base their theoretical superior electronic performances on: specific heterostructures, particular crystal orientations and the anisotropy of III-V energy bands [45]–[48], planar gating enabled by lateral growth, and buried oxides. Energy filters that reduce injection into the channel of electrons having energy

above the source Fermi energy have been proposed for nanowire FET devices[49]. Super lattice (SL) filters have also been proposed for planar and fin FETs with low subthreshold swings attractive for low power logic applications[48].

Horizontal HJs in TASE would enable these applications while benefiting efficiency as is shown in high efficiency heterojunction (HJ) based devices[45], [46], [50]–[52]. Additionally the lateral growth allows planar gating of the structures, resolving one of the issues of other structures that require complex gating, such as mesa and nanowire TFETs [53]–[56]. Direct integration of these horizontal heterojunctions via TASE is possible in a single step growth, with fast gas switching in the MOCVD allowing nanometer thin layers for quantum well structures to be grown directly in the confined channel.

This work first studies homoepitaxy on InP via TASE in micrometer templates, which has seen limited published work in the literature [57]. Fabrication on InP substrates experiences additional process constraints compared to that on-Si, with lower thermal and chemical stability. Here, two methods of fabricating horizontally oriented structures on InP substrates are explored. Particularly a new process that does not include an amorphous Si (a-Si) sacrificial layer is detailed, allowing to avoid etch damage due to the a-Si removal. Additional process constraints for TASE on III-Vs are also included. Growth via MOCVD of InP is executed on both types of templates, with good selectivity, and is characterized via SEM and TEM. Results reported show an increase in growth rate with

decreasing template length, increasing template width, decreasing pattern density.

In this work we demonstrate that TASE can be a novel and efficient way to grow various lateral horizontal heterojunctions, for several applications, and to serve as future "building blocks" for orientation-dependent and HJ-based devices. We begin by showing a successful growth of an InP/InAs HJ, which is an important material system for telecom wavelength room temperature lasers [58]. This is followed by a TASE overgrowth containing InP/GaAs and InP/InAs, important for HJ systems due to type-II band alignment between these materials showing interesting photoluminescence and quantum confinement properties[59]. Then we demonstrate the growth of an InGaAs/InP triple quantum well for energy filtering applications [48] as well as an InP/InAs/GaAs/InP triple-HJ structure, which is proposed for a high on-current TFET. We provide cross-sectional high-resolution TEM analysis to show the high quality of the material grown. Lastly, we show how the multiple HJs provide clues to changing growth rates inside a TASE template.

2.1 Materials and methods

2.1.1 Fabrication of confined epitaxy templates

Templates of varying sizes were fabricated on (100) and (110) InP 2" wafers by two general methods. These two methods share some initial fabrication steps, but

differ in the materials and deposition techniques used for the sacrificial layer and top dielectric. Both begin with a 5 nm thick alumina (Al_2O_3) etch stop layer followed by a 20 nm thick plasma enhanced chemical vapor deposition (PECVD) SiO_2 layer. Openings in the SiO_2 layer were then patterned by electron beam lithography (EBL) and inductively coupled plasma reactive ion etching (ICP-RIE) with $CHF_3/CF_4/O_2$ chemistry, exposing the small area of the InP, the seed, where growth will selectively initiate. Following this, a sacrificial layer was either deposited or spin coated and then patterned to define what will become the growth cavity. Finally, a top dielectric was either deposited or spin coated and patterned, exposing the sacrificial region to then be selectively removed. The process is summarized in Figure 29. Specific details of each fabrication technique and their effects on growth are discussed.

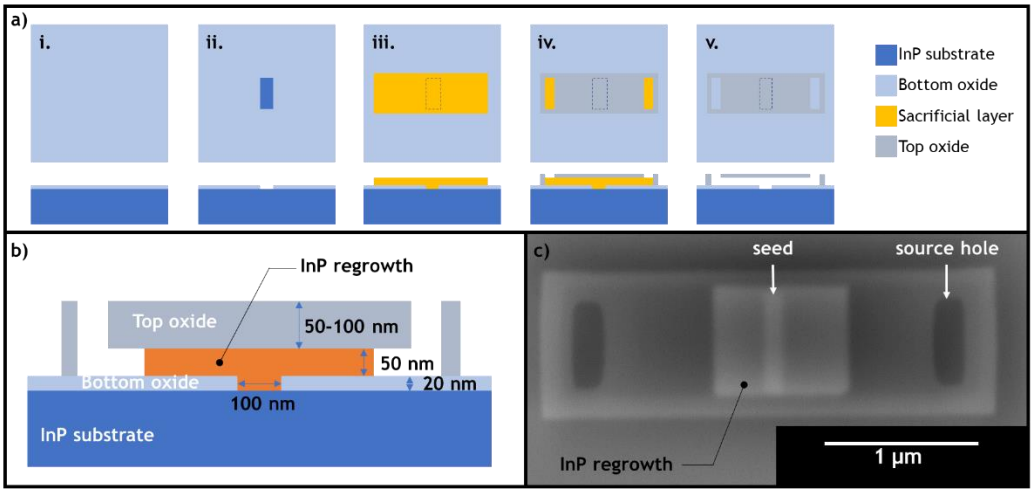

Figure 29. a) Illustration of general template fabrication b) Illustration of cross section of template after growth. c) Top-down SEM image of template after homoepitaxy of InP. The contrast allows to see the seed location, the confined lateral overgrowth, and the unfilled cavity.

All results presented in this chapter are derived from templates shaped as in Figure 29. Before settling on that specific geometry though several different template geometries were attempted. Simpler geometric shapes were preferred due to template edges increasing the potential for parasitic nucleation (see 2.2.1), but alternatives where number of seed holes and source holes varied were also tested. Admittedly, these structures were tested in early trials where many other factors could have affected the results, so no strong claim is made here as to which geometry works best. Choice of the final structure was mostly due to early results and for the need to down select to reduce the number of variables

and variations on the mask. Variations of the TASE templates are shown in Figure 30.

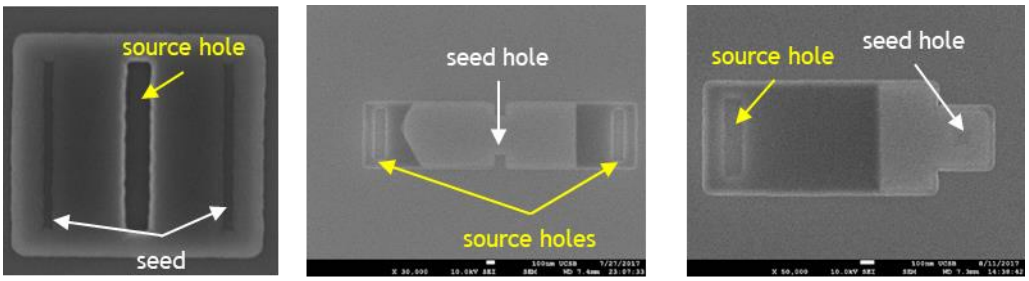

Figure 30. Variations of the TASE template in number of seed or source holes.

Even though a single template geometry was chosen there were still multiple variations of characteristic dimension that could influence results. The length of the template for example would change the distance that precursors would travel to reach the seed hole and the growth front. To test these effects, arrays of templates with changing characteristic dimensions (one at a time) were included on each die. Additionally, to characteristic sizes, orientation of the template on the substrate were also tested to explore possible effects on faceting. Details on this topic are shown in the results section (see 2.2).

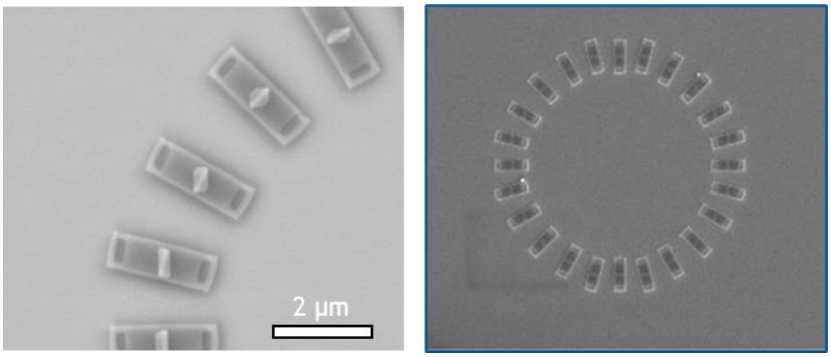

Figure 31. Orientation array of TASE templates, with 15° increments.

2.1.1.1 Dielectric mask (bottom oxide)

In this work, the fill factor (unmasked over masked area) is very low (less than 1%) compared to typical non-TASE SAG, thereby enhancing the risk of parasitics (i.e. nucleation on the dielectric mask). Because growth inside the cavity occurs more slowly than growth on the surface, any parasitic will grow much faster than the desired confined growth. This fast surface parasitic growth impairs characterization and further processing. Additionally, it locally consumes precursors, which changes the conditions inside nearby templates and renders control of the desired confined growth difficult. To minimize this, it is important to select dielectrics that provide the best growth selectivity and lowest sticking coefficient.

Thermal SiO_2, seen in previous TASE literature, is not possible on non-Si substrates and thus deposited oxides must be used. Deposited oxides, however, are not typically stoichiometric resulting in a wide range of sticking coefficients.

To choose among the available oxides, InP growth trials were performed on un-patterned substrates using typical SAG growth parameters, and then characterized by SEM to compare parasitic nucleation. PECVD SiO_x exhibited the lowest density of parasitic nucleation and was thus chosen for all future templates.

Oxide patterning must be considered to expose the seed areas. Silicon oxide is generally dry etched in fluorine chemistries and wet etched using hydrofluoric (HF) acid. However, for VLSI relevant scaling, wet etching causes pattern size to be at least equal to twice the bottom oxide depth, thus dramatically reducing lateral spatial resolution and packing density. Dry etching is thus preferred; however, etching through SiO_x in fluorine chemistry will eventually expose InP to fluorine plasma, which will form non-volatile InF_x that is difficult to remove and known to be detrimental to growth initiation. In fact, exposing InP to any ion-energy damages the surface impairing subsequent epitaxy. While process induced damage can be removed by etching InP, it was found that 1-5x digital etch cycles (15 min UV-ozone + 60s 1:10 HCl) was not enough to sufficiently recover the surface. An $HCl:H_3PO_4$ 1:4 etch was attempted as well but found to cause severe undercutting of the seed hole, which can then trap later process materials. Cooling the $HCl:H_3PO_4$ solution to 6°C reduces the etch rate; this was attempted and provided additional control but still resulted in a significant undercut.

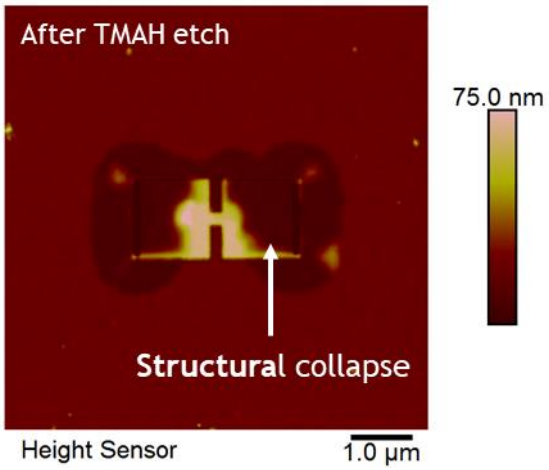

Figure 32. Structural collapse of a TASE template after the sacrificial layer removal possibly caused by undercutting of the bottom oxide .

To eliminate this, a 3-5 nm atomic layer deposition (ALD) Al_2O_3 layer was used as an etch stop to protect the critical growth interface from damage, and selectively removed with TMAH as the last step of the fabrication process.

2.1.1.2 Sacrificial layer

Choice of the sacrificial layer is critical because it must be selectively removable and, ideally, leave behind no residue or chemical modification of adjacent surfaces. Two materials were considered, each requiring a slightly modified fabrication process. Similar to Ref.[28], a-Si was investigated and, dissimilarly, the electron beam resist CSAR-62 was also investigated. We will refer to these as process A (a-Si sacrificial layer) and process R (photo-resist sacrificial layer).

For process A, prior to a-Si removal, an oxide densification anneal at greater than 700°C is useful to improve etch selectivity of a-Si/SiO_x in xenon difluoride (XeF_2). While achievable when using silicon substrates, annealing InP substrates at high enough temperatures would be impractical even with a phosphorus overpressure. Without an anneal, it was found that the XeF_2 modifies the oxide surface enough to cause severe parasitic nucleation during epitaxy. Recovering the surface damage, and thus selectivity, is although possible with an additional dilute HF dip that removes 2-5 nm of oxide prior to growth. This must be taken into account to avoid excessive thinning of the template sidewalls that could lead to mechanical failure.

For process R, CSAR, a common EBL resist, was selected as the sacrificial layer. Deposition of this resist is carried out via routine spin coating. The roughness was evaluated by AFM after development and found to have an RMS rougness of ~0.55 nm. The CSAR was finally removed in NMP-Rinse at 80°C for 2 hours, followed by a 3 min treatment in remote oxygen plasma at 350°C. This resist based sacrificial layer did not show adverse effects on growth selectivity during SAG trials.

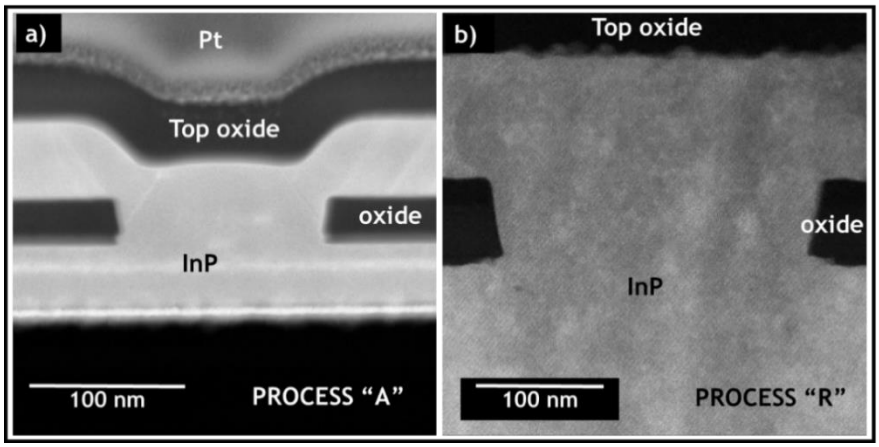

Figure 33. TEM cross section images of TASE cavities with homoepitaxy of InP fabricated by a) process A, where a dimple is present above the seed due to semi-conformal deposition of a-Si. b) process R, where no dimple is present due to planarization via spin coating. Additional roughness in top oxide likely due to intermixing of CSAR and HSQ.

2.1.1.3 Template structure (top oxide)

Using the same material, PECVD SiO_2,for both bottom and top dielectric is possible in process A, but for process R, because PECVD is often carried out at temperatures greater than 250°C, concerns about organic contamination of the deposition chamber led us to choose hydrogen-silsesquioxane (HSQ) instead. By eliminating dry etch steps, the process time was reduced, however at the expense of additional EBL time due to the large (~1000 μC/cm^2) exposure dose of HSQ. By using HSQ and an expose/develop process rather than an etch process to form openings in the top oxide, a true "bridge" is realizable over the sacrificial layer. Dry-etching openings in process A leave a sidewall and/or an additional "corner"

for the MOCVD precursors to traverse [42]. Spin coating the CSAR sacrificial layer in process R also leads to planarization of the surface, eliminating the depression that typically forms above the seed by the semi-conformal a-Si deposition of process A, as shown in Figure 33. Because sidewall deposition rate is often less than the normal deposition rate (in this case ~0.5x), this dimple behaves as a pinch point for gasses during the critical growth initiation and becomes more pronounced for thin cavities. One of the downsides of using HSQ over the spin coated CSAR is the resist intermixing that occurs at the interface. As observed in Figure 33, the ceiling of the template is significantly rougher in process R than in process A, higher than what is measured on the spin coated CSAR only (0.55nm RMS via AFM). We have not seen evidence of additional parasitic nucleation due to this roughness, but it is possible for it to induce additional crystal defects such as stacking faults during epitaxy, so additional material quality studies are desirable. To ensure that the HSQ itself properly planarizes, it is important that the HSQ is ~2x thicker than the underlying CSAR. This both limits the maximum cavity thickness and forces thick top oxides. Other than that, processes similar to manufacturer recommended processes for both resists are used.

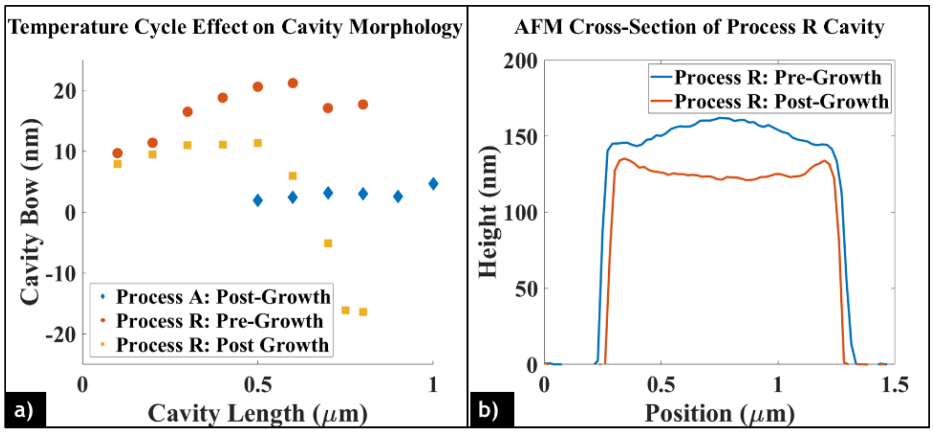

Figure 34. Cavity bowing in process A and R templates measured by AFM a) before and after growth as a function of body width and b) AFM cross-section perpendicular to growth direction at template center for 0.80 μm wide cavity before and after growth.

Completed templates were measured by AFM prior to and after growth to understand if a thermal cycle deforms the templates and "pinches" the cavity. Figure 34 shows the slight positive bowing of process R cavities prior to growth and negative bowing post-growth – dependent upon the box width. The grown film was also measured after removing the oxide and exhibits similar bowing to the cavity suggesting that the template bows early in growth, likely during the initial heat up of the MOCVD chamber. Cavities formed by process A do not exhibit a significant change in bowing during growth. Because curing HSQ at T>600°C induces compressive stress of -100 MPa[60] and the PECVD SiO_x has measured compressive stress of -250 MPa, the observed bowing in HSQ is unlikely due to stress. It has been reported that HSQ films shrink by more than 20% at 600°C[60]. Additionally, when the width is 1μm or larger, HSQ boxes often become

disconnected from the underlying oxide during develop and CSAR removal, suggesting poor adhesion or pronounced mid-range electron scattering effects common in both InP and HSQ processes. So thermal properties, in conjunction with poor adhesion, suggest that the downward bowing is likely due to expansion/contraction of HSQ cavities on the oxide surface during growth [32].

	Process A	Process R
Growth selectivity	Good (with DHF dip)	Good (with in-situ anneal)
Depression at seed	Present	Absent
Cavity thickness	Best for thick cavities Lower limit set by depression at seed	Best for thin cavities Upper limit set by resist processes
Cavity roughness	Low	High due to resist intermixing
Cavity width	High	Limited to <0.5um

Table 2. Summary of major benefits and limitations of the template fabrication processes.

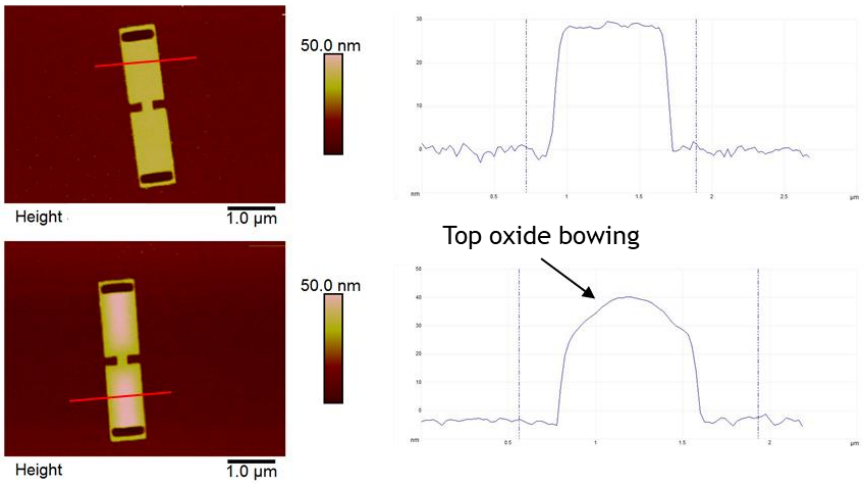

Figure 35. AFM scans of empty TASE templates showing bowing of the top oxide.

2.1.2 Sample preparation

Processed wafers were diced into 7x7 mm^2 samples, each containing four die and allowing for at least 1 mm of edge exclusion. Immediately before loading into the growth chamber, samples were dipped in 0.3% HF for 10 seconds and rinsed with DI water.

An in-situ anneal was conducted before growth and consisted of two steps: 350°C for 10 min in a hydrogen atmosphere, followed by 10 min at 660°C under both hydrogen and TBP to avoid group V desorption from the InP surface.

2.1.3 Epitaxy via MOCVD

MOCVD was carried out wtih a horizontal reactor using trimethylindium (TMIn), trimethylgallium (TMGa), tertiarybutylphosphine (TBP), tertiarybutylarsine (TBA), H_2 as carrier gas. Growth parameters used in the horizontal heterojunction trials for the different materials are summarized in Table 3.

Material	Temperature (°C)	Pressure (torr)	Group III (mol/min)	V/III ratio
InP	600	50	$2.7x10^{-6}$	570
InAs	600	50	$2.7\ x10^{-6}$	180
GaAs (Figure 57)	600	50	$1.9\ x10^{-5}$	25
GaAs (Figure 60)	600	50	$4.75\ x10^{-6}$	100
InGaAs	600	50	$5\ x10^{-6}$	95

Table 3. Summary of main growth parameters used in the horizontal HJ trials.

To achieve abrupt heterointerfaces in the heterojunction samples, when switching materials during growth, the growth rate was slowed down for a few seconds by reducing the molar flow of group III precursors in half, followed by a 1 s (approximate gas residence time in the reactor) purge in carrier gas only. All other parameters were kept unchanged throughout the growth. The 1 s purge was introduced to minimize instances of As/P intermixing typical of III-V

heteroepitaxy. An example of how a clearly identifiable intermixing shows up in a STEM image is show in Figure 36.

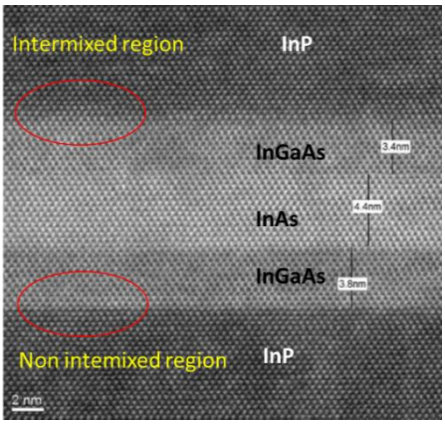

Figure 36. Example of As/P intermixing in a HAADF STEM image. A non-abrupt change in contrast suggests intermixing between the As and P based materials. The As -> P transition results blurred vs. the P -> As which is typical.

2.1.4 Growth characterization

2.1.4.1 SEM

SEM was used to determine the success and amount of growth in the template as well as an initial estimate of crystal quality. The top oxide, while present, is thin enough to allow electron penetration and enough contrast between grown material and an empty cavity.

2.1.4.2 TEM

Cross section TEM images were taken after thinning down a lamella from the center of the template, to include the "seed" and the initial growth interface (Figure 33). The samples were capped with sputtered iridium and platinum (Pt) prior to milling. The TEM lamella thickness was ~100nm. The samples were imaged at 200kV in bright-field (BF) TEM mode, high-resolution (HR) TEM mode.

2.2 Results and discussion

2.2.1 Selectivity and parasitic nucleation

Selective area epitaxy, by definition, aims at growing materials only in unmasked parts of the sample. We define parasitics as nucleation and growth that occurs on the dielectric mask or mask edge and is undesirable. Achieving good selectivity during growth is a prerequisite for successful TASE, and this was a major challenge. Growth on the dielectric is detrimental in more than one way. First, any deposition that occurs on the dielectric mask is wasted material that is not being incorporated on the target structures. Beyond this though, even when growth occurs as desired in the confined structures, material can still end up as parasitcs on the dielectric mask. Nucleation that occurs on the mask will not only keep growing during the run but will grow faster than the confined growth because will locally capture precursors, impacting the growth conditions in the

template. These large parasitics are sometimes micrometers in size, and particles this large impair any post growth processing including fabrication of contacts, lithographic patterning, and regrowth.

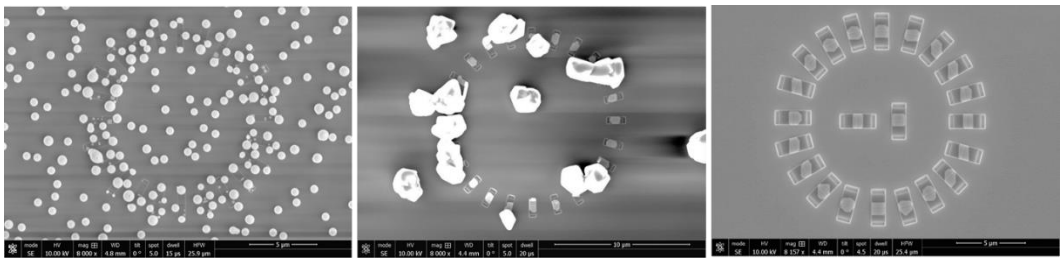

Figure 37. An orientation array from three different runs showing large number of parasitics covering both the field and the templates (left), parasitics appearing only on the template edge (center) and purely confined growth (right).

Minimizing the presence of parasitics was a main priority. We will discuss here below the causes of parasitics and the changes that were implemented to achieve good selective growth. Finally, for when parasitics were still present, we will discuss methods to remove them while preserving the confined growth.

2.2.1.1 Causes of parasitic nucleation

2.2.1.1.1 Fill factor

During MOCVD, III-V precursors reach the surface, thermally crack, and are adsorbed into the surface. In a dynamic process, these admolecules sometimes desorb and diffuse back into the growth atmosphere of diffuse on the surface. In

SAG, the probability of the admolecules to covalently bond with the unmasked parts of the substrate is higher than bonding with the dielectric mask. It is intuitive then that the more available unmasked areas are available for these molecules to diffuse to, the higher the chances of achieving good selective growth.

The ratio of unmasked to masked area. is referred to fill factor. By this definition then, for our TASE templates the fill factor is defined as:

$$FF \quad = \frac{A_{seed}}{A - A_{seed}}$$

This is the ratio of seed hole area to remaining sample area. The FF can be calculated slightly differently by recognizing that the precursor gasses first encounter the source hole and the partial pressure profile above the sample will track that and not the seed hole. The fill factor to consider is then the same ratio as above but with the area of the source hole replacing that of the seed hole, as follows:

$$FF = \frac{A_{source}}{A - A_{source}}$$

Regardless of which version we choose the result is largely the same, with TASE templates have an inherently very low FF (<1%) when compared to other SAG works.

Initial trials that started with using a standard planar InP recipe had extremely poor selectivity (i.e. none at all), with deposition randomly distributed all over the sample with no indication of selective growth. To the point of making it hard

to evaluate improvements due to a change in growth parameters (discussed later in this chapter) on the confined growth. To address this a sink area was added around templates to locally improve selectivity. This was simply a large exposed area of the InP substrate that encircled a template inside a smaller dielectric area (see Figure 38).

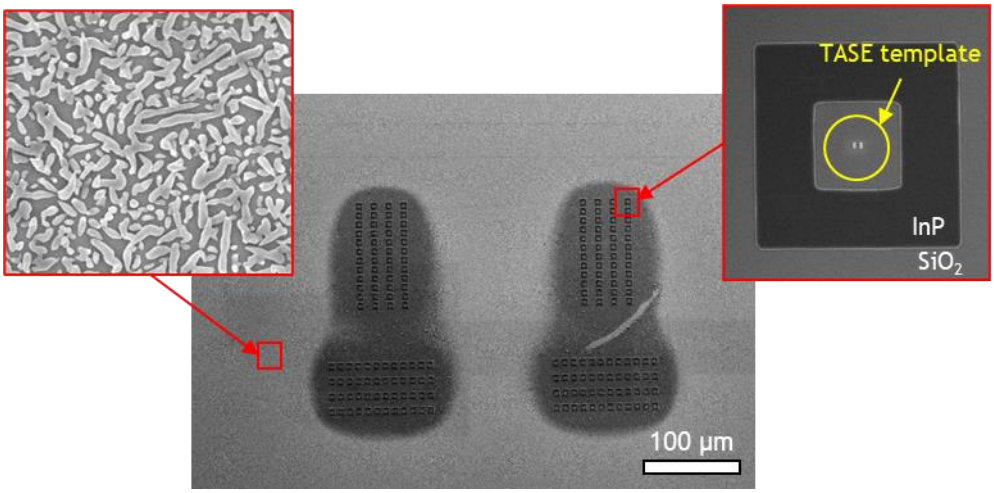

Figure 38. Local parasitic reduction induced by the presence of "sink" areas surrounding TASE templates.

The sink acts a local dramatic increase in FF improving the selectivity. This is further showcased by observing an array of sinks with increasing size correlating with progressive reduction of parasitics, as seen in Figure 39.

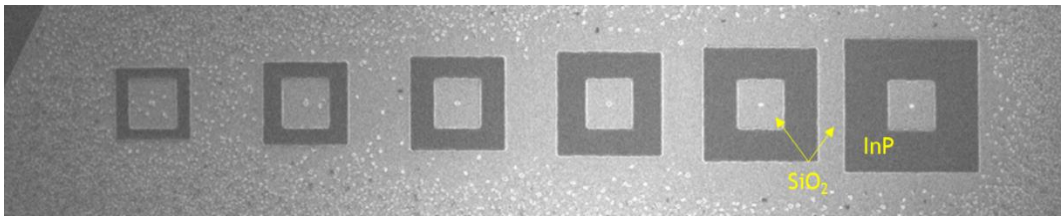

Figure 39. Exposed InP "sink" areas around the templates help with locally decreasing parasitics. The amount of parasitic scales with the size of the sink.

This was a temporary aid to selectivity, later removed in the final trials.

2.2.1.1.2 Choice of dielectric

Parasitic nucleation can occur in the field or on template edges, on the dielectric material, and this will depend on how likely the precursor is to chemically react with the surface. Available surface sites and the surface energy will then influence this, and so different materials and topographies will matter. It follows then that more dense and stoichiometric materials like thermal oxides will yield better selectivity versus other dielectrics.

For the experiments in this chapter deposited oxides were necessary because of the TASE template geometry, but there was still the question of which deposition method/tool would be best. A series of trials were made by simply running a standard InP MOCVD recipe on unpatterned samples with blanket oxides deposited. A visual inspection of the result determined that PECVD yielded better

results with the parasitic coverage being less homogeneous, failing to completely wet the surface, as seen in Figure 40.

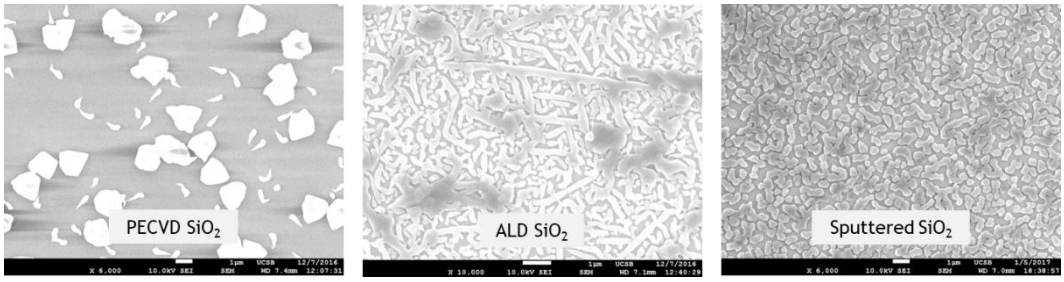

Figure 40. Comparison of parasitic nucleation of InP on samples of different dielectric materials after MOCVD growth of InP in typical planar conditions.

Later, when improvements were made on the selectivity thanks to changes in process parameters (see 2.2.1.1.4), parasitics would disappear from the field but still nucleate on the template edges. This again simply highlights how high energy sites, such as edges, can impact selective growth.

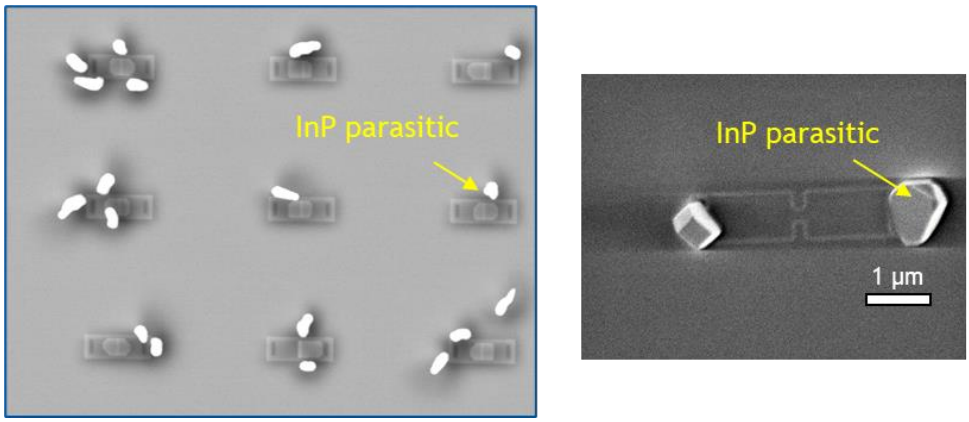

Figure 41. InP parasitics preferentially occurring at the template edge.

2.2.1.1.3 Pre-growth sample preparation and cleaning

The presence of particles due to lack of cleanliness also leads to parasitics, with residues from fabrication and other contaminants acting as favored sites for parasitic nucleation. In Figure 42 patterns of parasitic appear on the sample resembling what could be residues from wet processing, a poor cleaning step or a poor rinse. Properly cleaning the sample then becomes critical to achieve a good SAG result.

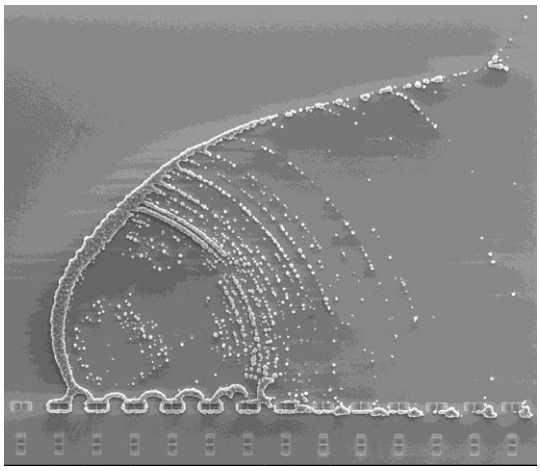

Figure 42. Parasitics of InP preferentially appearing on surface residues due to insufficiently clean wet processing, cleaning, or drying.

When using InP as a substrate some cleaning steps and chemicals, commonly used in silicon nanofabrication such as piranha solution, O_2 plasma and RCA cleans, are not available because they are not chemically compatible. Piranha solution directly etches InP and would have attacked the seed holes and the

backside of TASE template samples. Relying on the alumina etch stop layer and adding a backside mask possibly could have solved this but wasn't attempted. Plasma based tools like an O_2 plasma asher, while not directly etching the InP, damages the surface causing irregular growth, as seen in Figure 43.

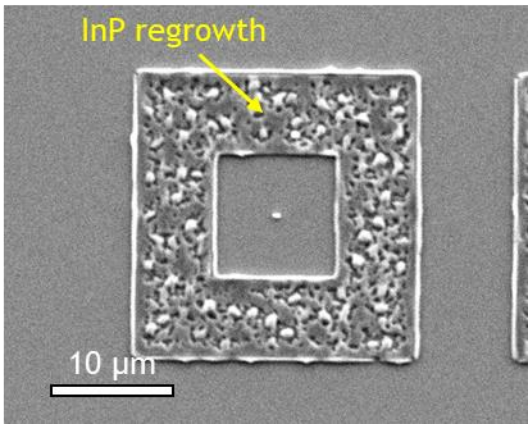

Figure 43. Irregular InP growth on InP substrate damaged by plasma.

Excellent selective growth was achieved relying on:

- Solvent (NMP rinse) cleaning in a spinner, with particles, PR residues and dicing dust being flung off the sample surface.
- Remote oxygen asher (Gasonics). Often as effective as plasma-based tools without the direct exposure to plasma.
- Dilute HF dip. General cleanup of all surfaces including the InP seed hole. The template itself is SiO_2 so this step had to be short (10 s) and the solution very dilute (0.5%) to avoid excessive etching.

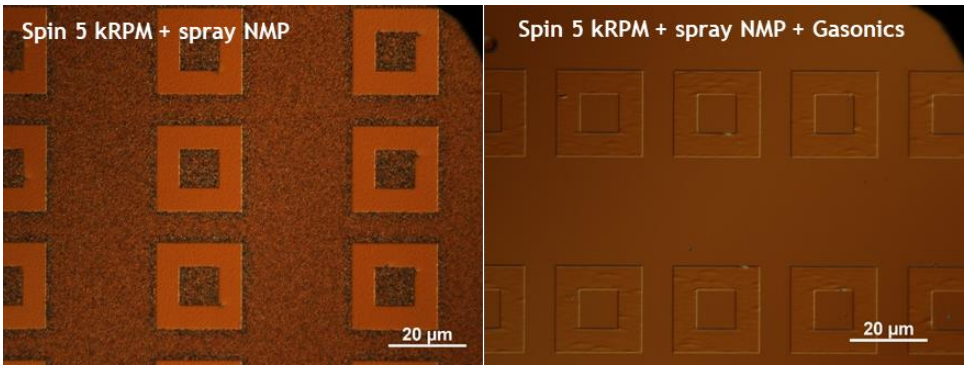

Figure 44. Optical microscopy images of samples after solvent clean at the end of fabrication without (left) and with (right) the addition of a remote oxygen ashing step, showing the change in particles surface

2.2.1.1.4 Growth parameters

Even with a very clean sample and optimized fabrication process, using some set of growth parameters can still lead to parasitics. Common growth parameters that yield excellent results in planar homoepitaxy were entirely unsuitable for very low fill factor selective area growth samples (or entirely dielectric samples like the left image in Figure 45). In general terms the following set of changes aided with selectivity:

- Lower growth pressure
- Higher temperature
- Higher V/III ratios
- Lower growth rate

All these changes are aimed at maximizing surface diffusion of precursors and facilitating desorption of adsorbed admolecules from the dielectric, to promote growth in the unmasked areas only.

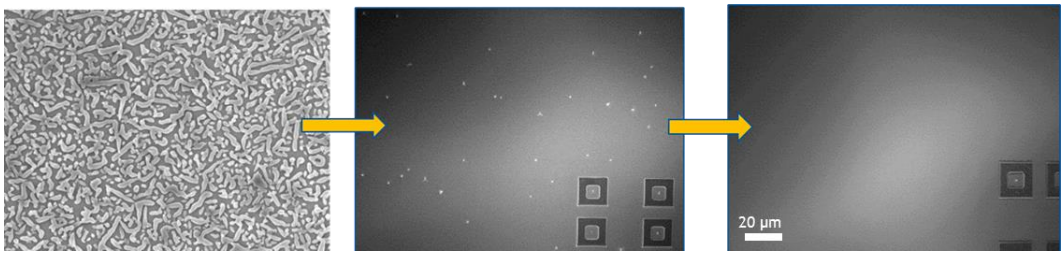

Figure 45. Representative SEM images of identical samples showing the improvement in selectivity with changing growth parameters.

In the case of process R templates, significantly less unwanted parasitic nucleation was observed at template edges if the in-situ anneal preceded growth. It is possible that the HSQ is not fully transformed into SiO_2 at pattern edges, presenting either hydroxyl or other residual organic groups that can act as nucleation sites and are removed or saturated during the anneal.

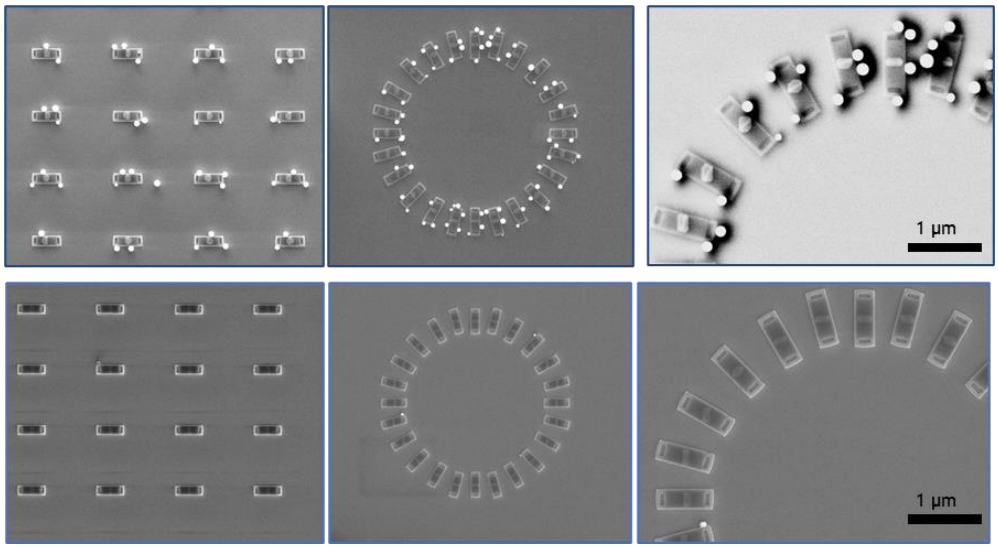

Figure 46. The addition of an in situ pre growth anneal at 650°C prevents the formation of parasitic nucleation on template edges.

2.2.1.2 Removing parasitics

Avoiding parasitics is also important because any further processing can be impaired by their presence. Deposition of PR for lithography of contacts for example is basically impossible with particles of several microns in size on the surface. And in the case of our TASE structures even the simplest measurements would be a challenge because of the need for metal contacts. To characterize a parameter such as doping level to develop recipes, in planar epitaxy the use of techniques like SIMS and Hall are routine. These are inadequate for the small confined growths in TASE.

While perfect selectivity was achieved for InP, arsine containing growths proved more challenging, and the need to remove the parasitics after growth

arose to facilitate lithography and metal contact deposition. A first solution was finishing the growth (see Figure 47) with a known layer that would act as a cap and a combination of dry and wet etches. The idea was to cap the confined growth inside the channel first, then an RIE dry etch, directional by nature, would remove the material above the top oxide while leaving the confined growth untouched. The dry etch could be used to entirely remove the parasitics or simply to partially remove the final layer, exposing the inner core. Finally, a selective wet etch would remove the rest of the parasitics.

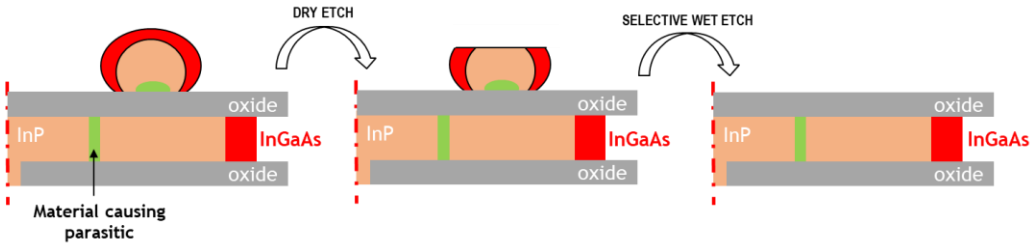

Figure 47. Diagram of the parasitic removal process using a combination of dry and selective wet etches.

Excellent results were achieved with a complete removal of the unwanted parasitics while leaving the TASE structures intact. This approach was further refined and prior to creating metal contacts and will be described in paragraph 2.2.4.

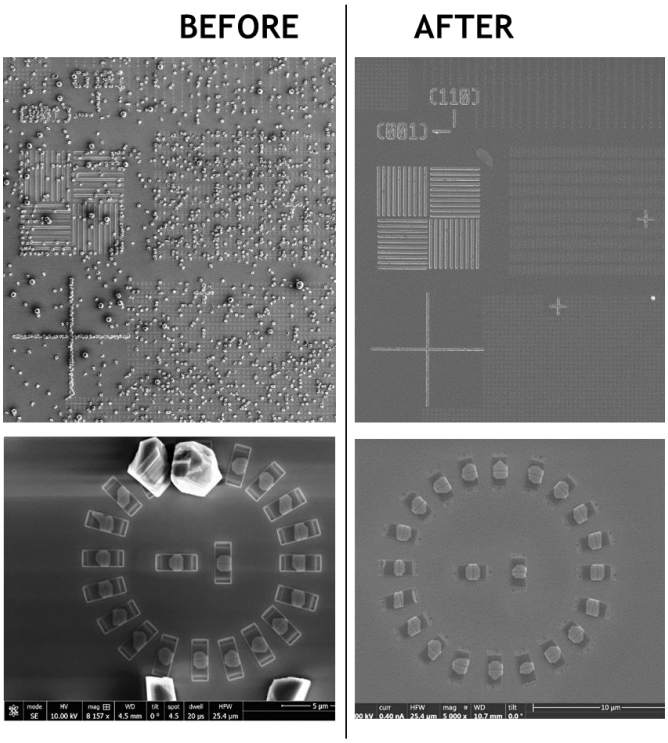

Figure 48. Before and after SEM images of the parasitic removal process.

2.2.2 InP homoepitaxy

A V/III ratio of 400 was chosen, which is high compared to typical MOCVD growth but is justified by some considerations. A morphological dependence of TASE growths on V/III ratio has been reported [42], [61]. Additionally effective V/III ratio has been inferred to be lower deeper within a template [42], [61]. As growth progresses, the template fills with grown material and the length of the remaining cavity is effectively shortened. As a result, the effective V/III ratio at the growth interface increases. A high V/III ratio is thus chosen to prevent local

growth conditions at the growth interface from changing significantly with the progression of growth.

After epitaxy, growth length was measured from the center of the seed to the growth front on either side and averaged. It is to be noted that while seeded growth occurs with 100% yield, not all templates are filled symmetrically. Possible residues from template fabrication at the growth seed have sometimes been observed to affect growth initiation and, consequently, final grown length.

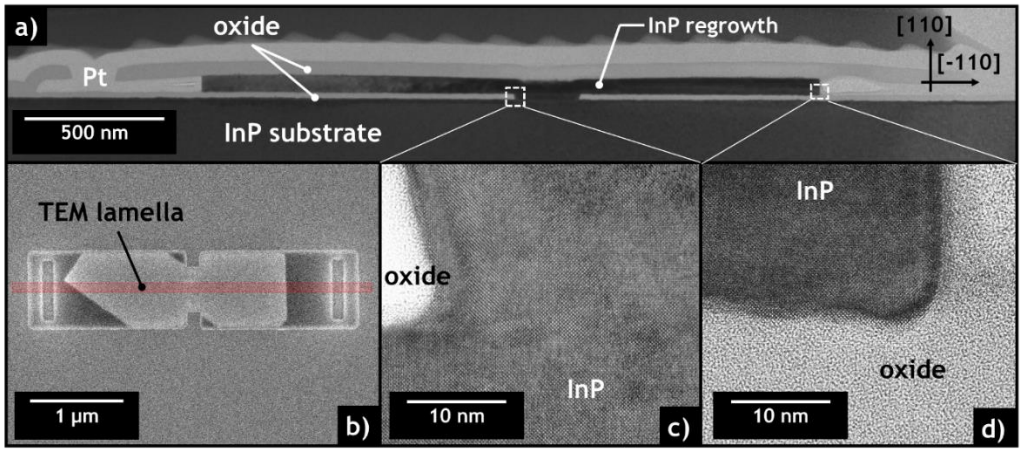

Figure 49. Early InP homoepitaxy via TASE with a process A template. a) Cross-sectional TEM. b) Top view SEM of the TASE structure showing where the TEM lamella is taken. Inconsistency between the left and right facet can be observed. c) HR-TEM at the initial growth front terminating on vertically oriented (-110) facet.

While the general geometry of the templates was the same, a parameterized array of characteristic dimensions was always included in all samples. Initially this was to determine the range of mechanically stable geometries and sizes, but then

also to allow for a study on the effects of template dimensions on confined growth outcomes. Multiple geometries and variations of templates included in every run with E-beam lithography allowing flexible designs and fast turnover.

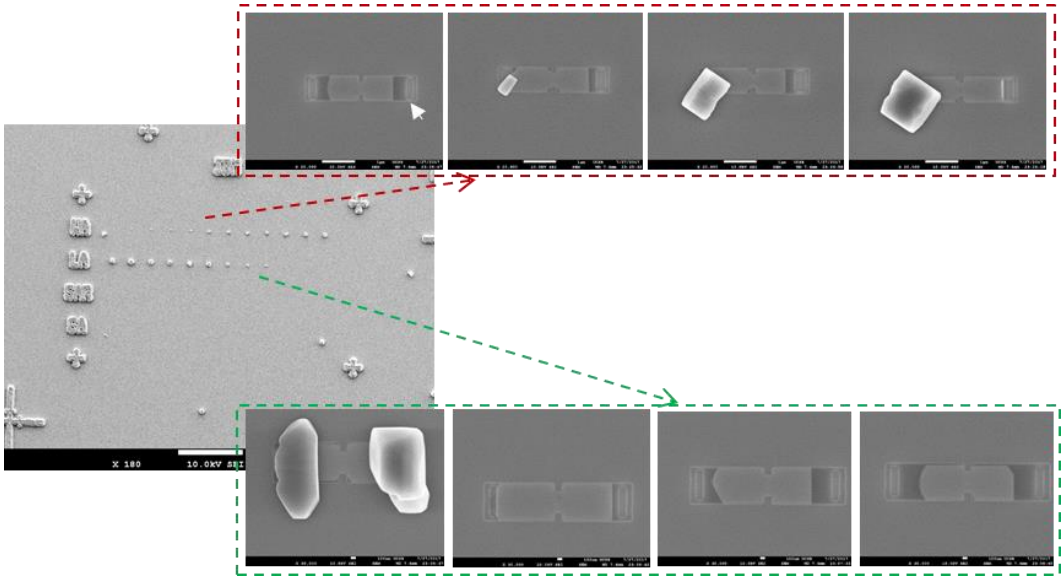

Figure 50. On each die were present several arrays of different characteristic dimension such as length, width, seed hole size.

2.2.2.1 Growth rate vs. length

As alluded to above, the geometry of the templates affects the growth rate of the confined material. Because MOCVD growth rates are determined by diffusion of precursors to the growth surface, it is conceivable that template geometry and packing density could be used to tune growth length and/or composition across a

wafer in a single growth. The effects of template width, length, thickness and packing density were studied.

Because MOCVD growth is generally limited by mass transport of precursors[62], it is expected that in the case of high aspect ratio structures, the template geometry will directly affect growth rate.

An effect of template length on growth length was observed in both process A and R templates. The length of the grown material inside the template was compared for structures of varying lengths, ranging from 2 μm to 4 μm, all simultaneously present on a die, with width and thickness fixed (Figure 51). It was observed that growth rate decreased as template length increased. This growth rate reduction could be intuitively explained by the need for precursor material to cover longer distances, measured from the source hole to the growth front, to initiate/continue growth. The source hole is located at the sample surface where diffusion is dominated by lateral gas phase diffusion driven by partial pressure gradients, typical of SAG [7]. However, this pressure gradient might be diminished or absent at the growth front deep inside the template, as finite element simulations for other TASE growth suggests [42].

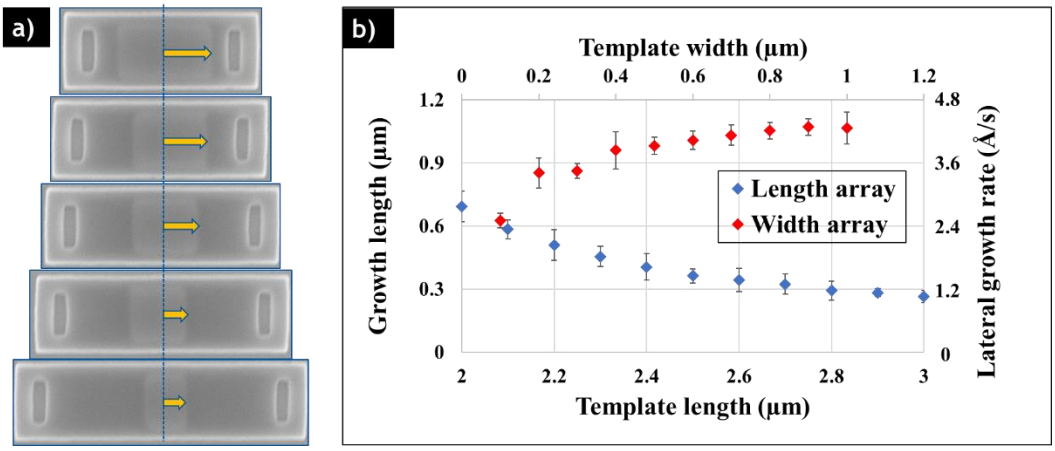

Figure 51. Effect of cavity dimensions on growth rate. a) Representative example of cavities of increasing length, exhibiting reduced growth in longer cavities. The arrows guide the eye to the growth front. b) Growth length in cavities of varying width (L = 1.0 µm) and length (W=0.35 µm). Each point is the average of 10-15 templates. Error bars show standard deviation.

2.2.2.2 Growth rate vs. template width

Growth in templates of identical length but varying widths, ranging from 150nm to 550nm, was also conducted and exhibited an increase in growth rate with increasing template width (Figure 51). It should be noted that while all other template parameters are kept constant, the width of the source hole increases with the width of the template, thus allowing more precursors to reach the wider growth interface.

2.2.2.3 Growth rate vs. density of pattern

Identical templates (0.35 µm wide and 1 µm long) separated by 2.5 µm and 5 µm from template edge to edge, present on the same die, are shown in Figure 52. For identical size template patterns, growth rate decreases with increasing

packing density (i.e. decreasing pitch/separation). This is expected considering loading effects present in SAG which causes growth rate enhancement as the masked/unmasked area ratio increases. It has been previously reported that TASE showed no change in growth rate with pattern density [42] where transport is dominated by surface diffusion. We note that differences in template geometry could be responsible for the discrepancy and hypothesize that the lower sidewall height in this work, compared to tall nanowire templates in Ref.[42], might allow for lateral gas phase diffusion mechanisms to still be noticeable. This effect could be used as an engineering tool to produce devices of different sizes or composition on the same wafer, simply by tuning template geometry.

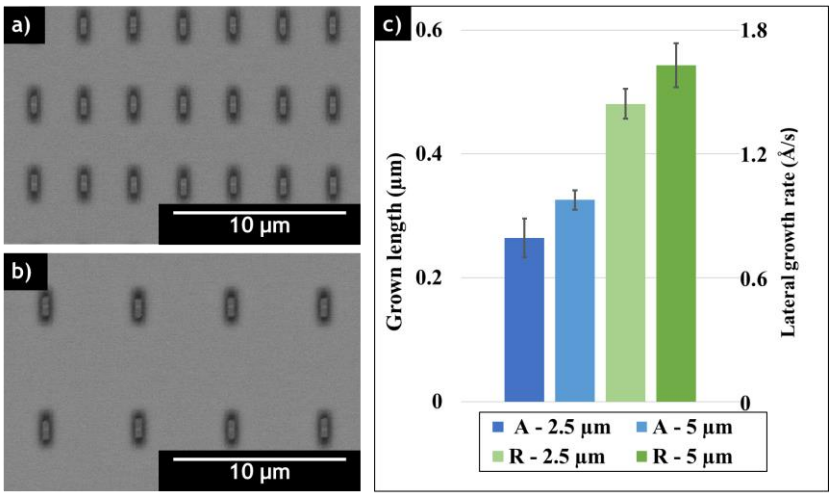

Figure 52. Top-down SEM images of process R TASE structures spaced by a) 2.5µm and b) 5.0µm. c) Average growth length in cavities fabricated by techniques A and R where the width of templates by the respective processes are W=0.75µm and W=0.35µm as process A can sustain wider templates without bowing.

To explore growth behavior on different crystal directions templates were fabricated in two different orientations, rotated 90° from each other. When using (100) substrates this results in cavities aligned along <100>, when using (110) substrates this results in cavities aligned along [010] and [-110]. Observing the grown material after MOCVD reveals how, even across identical templates, the growth front can present different crystal planes, with some templates showing single-faceted growth while others multi-faceted. This is true for both (100) and (110) substrates. Yield of a specific facet though is influenced by growth conditions[42]. Notably, in this work, when using templates fabricated onto (110) wafers, in cavities developed along the [-110], we commonly observe flat vertical (-110) and (1-10) facets[63], [64]. Having vertical facets normal to the direction of growth is of interest because it allows for the formation of horizontal HJs grown directly inside the cavity. This in turn could enable novel electronic and photonic devices[46], [52]. The yield of this specific facet is primarily temperature related, appearing at 580-610°C and disappears, favoring {111} facets, at higher temperatures.

2.2.3 Horizontal heterojunctions

It has been previously observed that under certain growth conditions (580-600°C, 50 torr, 570 V/III ratio), in templates fabricated on (110) InP substrates and oriented along the [1-10], growth can be terminated in flat and vertical (-

110) and (1-10) facets. These facets were chosen to demonstrate the multiple HJs in this work. Additional development is needed to optimize the yield of these facets, which is now low (<30%) and varies between runs possibly because of minute differences in template fabrication which, in turn, influence growth and growth initiation.

Image analysis software to get better statistics from SEM top view images that show enough contrast to allow it is worth considering but likely difficult. It remains true though that facet analysis is also complex because a simple top view can be deceiving. The thickness of the TASE cavity is 50 nm, so while the angle of the facet vs. the plane is obvious, the angle vs. the normal to the plane is barely discernible, showing a vertical facet or a tilted one with almost the same contrast. As of now the yield number claimed is based on a simple manual count of the flat looking facets from top view SEM images like the one here below.

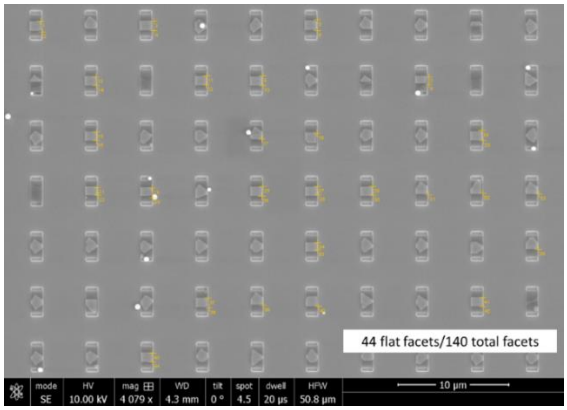

Figure 53. Top view SEM image of TASE of InP. Overlayed on the image are manually executed counts of the flat [110] facets identifiable.

Cross sectional TEM imaging related to the top view SEM allowed us to confirm that these are indeed the [110] facets we talk about in this work when looking at the templates aligned the {110}. More details regarding TEM analysis, plan view TEM samples, and cross section – top view correlations are discussed in detail later.

Both our own trials and published work [42] show facet dependence on temperature and V/III ratio, leading us to believe yield can be increased by optimizing growth parameters.

2.2.3.1 InAs heterojunction

To demonstrate the feasibility of horizontal HJs a single InP/InAs/InP HJ was integrated in the confined channel. The first attempt is shown in Figure 54. Clear contrast in the TEM cross section image clearly identifies the InAs layer. While the heterointerfaces appear abrupt the growth front of the InAs appears somewhat irregular with facet dependence of growth rate.

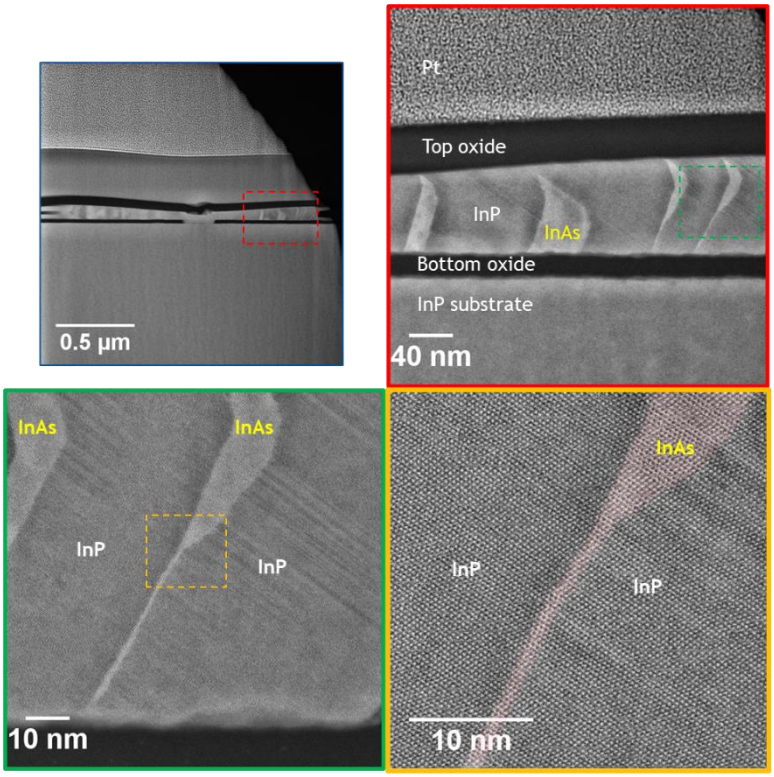

Figure 54.First attempt at introducing an InAs HJ inside the confined growth.

Later attempts after the correlation of the growth front facet and the growth parameters was better understood yielded improved results. The 1.5 nm InAs HJ in Figure 55 was achieved via a single step growth. Figure 55 shows cross sectional STEM characterization of the structure, showing abrupt heterointerfaces on either side of the InAs layer. High-resolution imaging suggests crystallinity of the material, which is confirmed by the diffraction pattern.

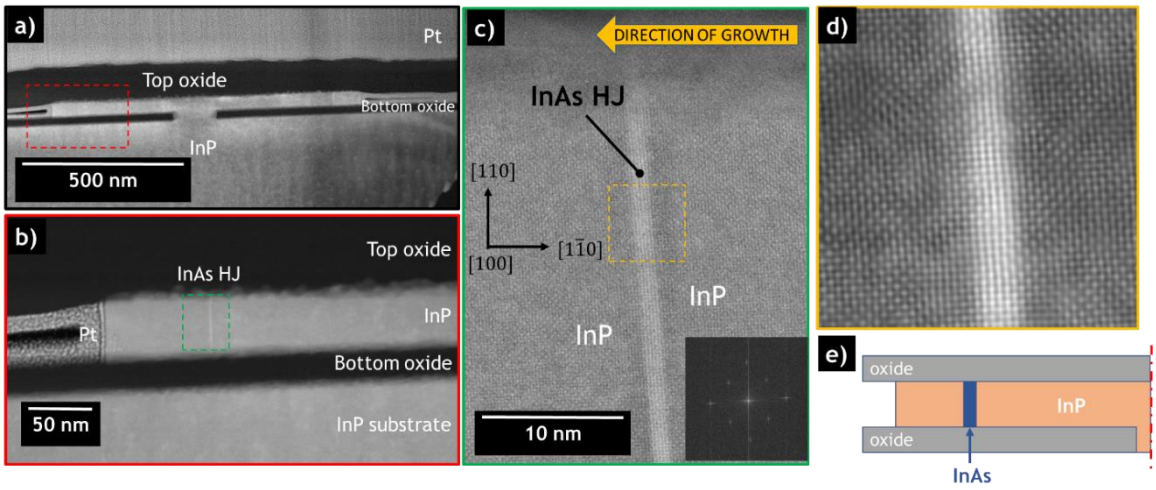

Figure 55. Cross section of a confined growth of InP with an InAs layer. a,b,c) HAADF-STEM imaging. d) Detail of the InAs HJ (with applied Fourier filtering). Inset: Electron diffraction pattern for the InAs. e) Schematic diagram of the structure

Intermixing of As and P is known to be a problem for this interface and obtaining some quantitative data on this for TASE was desirable. In theory TEM EDS measurements executed across the InAs HJ, since they are a chemical analysis type of measurement, could reveal As/P intermixing. The available resolution reveals no apparent intermixing, but we consider the sensitivity of our instrument to be insufficient to provide meaningful information. The HR STEM image of the HJ shows an ordered lattice with clean contrast differences between InAs and InP with no discernible intermixing, especially when compared with a typical As/P intermixed region as the one showed in Figure 36. We believe this is sufficient to substantiate our claim.

A 2 nm InAs layer sandwiched between InP should have considerable level of strain, and possibly also strain relaxation by misfit dislocation formation. The FFT does not show any sign of the InAs spots, but additional data provided by geometric phase analysis, show in Figure 56, confirms the strain situation in the film. The mismatch between InAs and InP is indeed high (~3%) but the Matthew-Blakeslee critical thickness for InAs on an InP substrate is ~2.1 nm, so absence of dislocations is not entirely unexpected for a HJ this thin. The strain visible in the InAs layer confirms lack of relaxion within the layer itself. In the plot it is clear how the strain change across the junction is very abrupt, as expected for a sharp heterointerface.

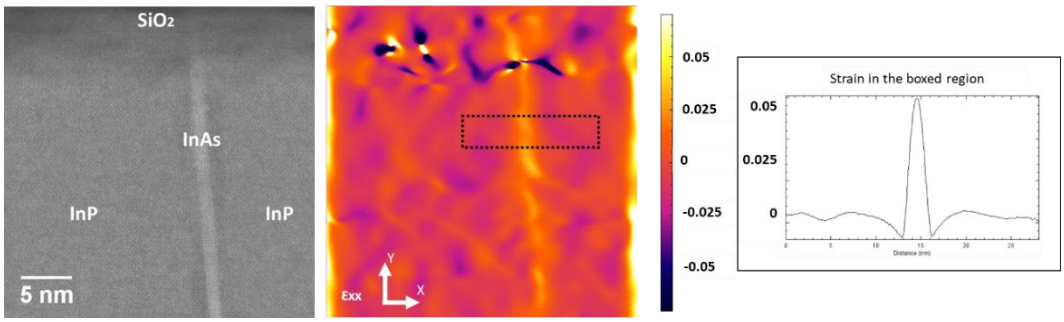

Figure 56. Strain map across the InAs HJ showing presence of strain in the InAs layer and an abrupt change in strain value across the heterointerfaces

2.2.3.2 GaAs heterojunction

A single InP/GaAs/InP horizontal heterojunction was demonstrated. The structure was grown in a single step growth. Reproducibility of results was tested

by including in the same structure multiple InAs layers grown with identical parameters used for the structure shown in Figure 55. The resulting InAs layers, while showing some variations, were mostly consistent in quality and thickness across the two trials. STEM characterization shown in Figure 57 shows abrupt, vertical interfaces, with crystalline order.

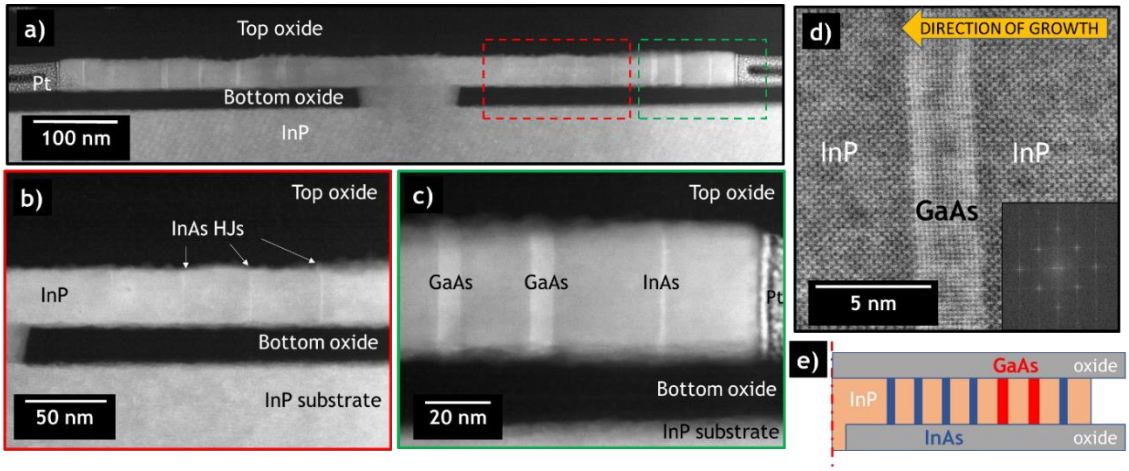

Figure 57. Cross section of a confined InP growth with InAs and GaAs layers. a,b,c) HAADF-STEM imaging. d) Detail of a GaAs HJ (with applied Fourier filtering) from a similar growth. Inset: Electron diffraction pattern for the GaAs. e) Schematic diagram of the structure.

2.2.3.3 InGaAs superlattice

A three-well InP/InGaAs structure, resembling SL energy filters, was demonstrated. By design all InGaAs layers and the first two layers of InP are supposed to be identical (3 nm) while the third InP thinner (2 nm). The resulting growth somewhat deviates from the design as shown in Figure 58.

The thicknesses are somewhat inconsistent with the design, although not by much. It is unclear why this is the case, and it is hard to hypothesize why with the available data. Considering the small deviations from design the differences can be attributed to small variations in the reactor. An example of which could be a slowly rotating sample holder (that helps with homogeneity but is driven by gas flows rather than a motor and sometimes slows down or gets stuck). If the step time for the HJ is less than a revolution, minute differences in flow may then cause differences in the confined growth.

After the SL itself, a thick InGaAs layer is included, to mimic a possible contact layer in a final device. The structure was grown in a single step. The facets are flat and the interfaces quite abrupt even though less so than the previous structures. The reason why the interfaces are not as abrupt is unclear. We think As/P intermixing, a common problem with these materials, while a possibility, is not inherent to the confined growth since it is not present in the other HJs shown here. Damage of the lamella is also a possibility with FIB induced gallium damage causing “blurriness” in the image, and so are small variations in thickness of the lamella.

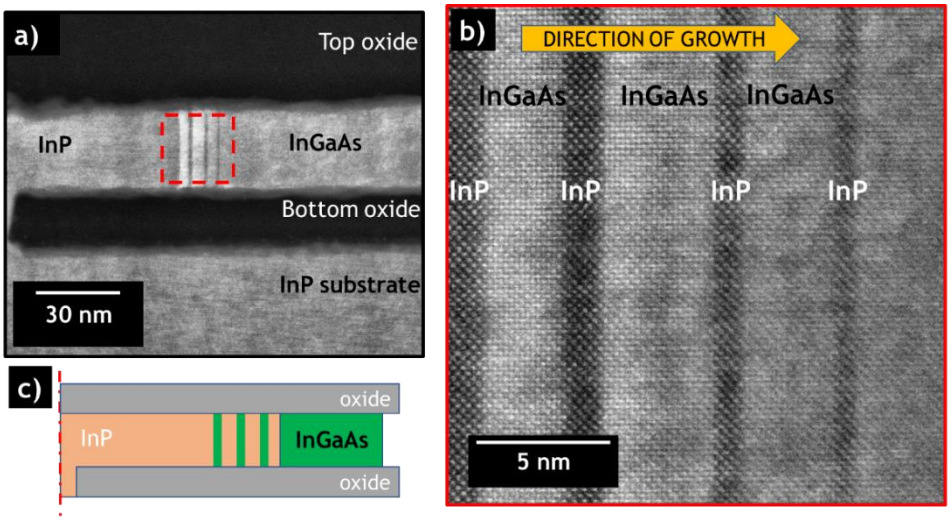

Figure 58. Cross section of an InP and InGaAs growth with InP/InGaAs HJs. a,b) HAADF-STEM imaging. c) Schematic diagram of the structure.

When growing bulk ternary material via confined epitaxy there is the possibility that a compositional gradient exists along the structure due to differences in the diffusion between the group III precursors. We executed an energy dispersive spectroscopy (EDS) measurement to verify this in a confined InGaAs growth. The apparent change in In composition along the cavity suggested by measuring the InL/AsL and the GaK/AsK is 15% and 10% respectively, measured from seed to growth front across 350 nm. The presence of a compositional gradient has also been observed in other reports [43]. It is reasonable to believe that, once the gradient is known, progressively adjusting the molar flow ratio of precursors during the growth should lead to a constant composition within the cavity.

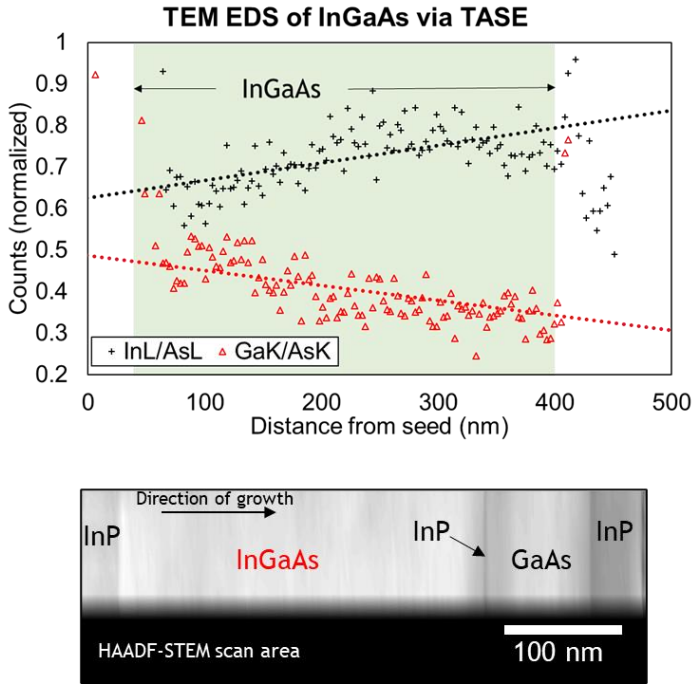

Figure 59. TEM EDS data of an InGaAs growth via TASE. The plot shows InL and GaK counts normalized to AsL and GaK respectively. The green area indicates the position of the InGaAs inside the template. Inset: Schematic diagram of the structure.

2.2.3.4 Triple heterojunction (3HJ)

A 3HJ structure, comprised of an InP/GaAs/InAs/InP sequence was demonstrated and is shown in Figure 60. The structure was achieved in a single step growth using the same parameters used in the structures described above. The 3HJ itself was repeated twice and InAs layers were included as markers.

The entire structure is not symmetrical, with the left side being longer than the right, as clearly seen in Figure 60e. The distance between the geometrical center of the seed and the first HJ is significantly different. Though comparing

the left and right sides of the template, seen in Figure 60a and Figure 60b, the same HJs are present with similar appearance and spacing. It is possible that the growth initiated asymmetrically but ultimately proceeded with some consistency among sides. In fact, if one was to measure the distance between the first InAs layer and an offset virtual point at the seed, the entire structure appears symmetrical. This “single point” nucleation hypothesis is corroborated by results from another horizontal HJ trial where growth initiated nonuniformly and only on one side of the seed. This asymmetric growth behavior is seen in other SAG literature [65] but needs further investigation.

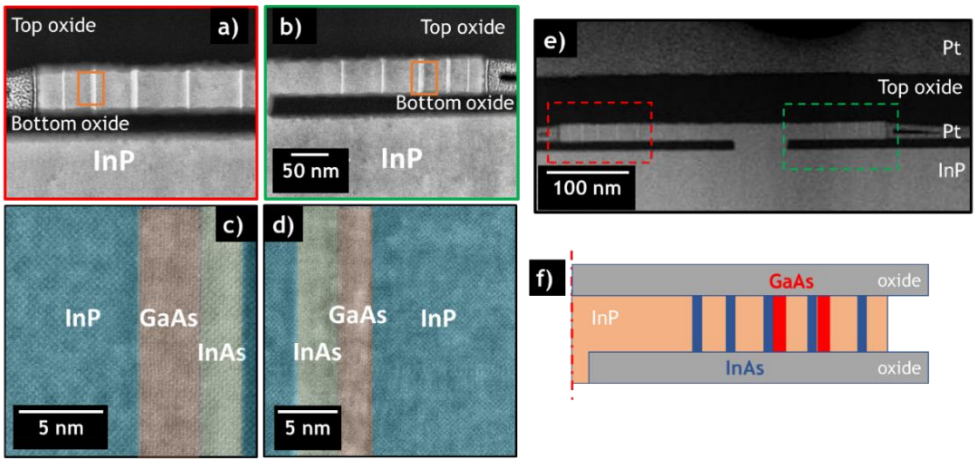

Figure 60. Cross section of an InP growth with InAs marker layers and InP/InAs/GaAs triple HJs. a,b) HAADF-STEM imaging. c) Schematic diagram of the structure.

2.2.3.5 Using HJs to track growth rate inside the template

Including HJs allows to track the progression of growth and observe possible changes in growth rate (*Rg*) within the confined cavity. The presence of different materials does change the surface energy at the growth front, and thus the growth initiation, but on first approximation measuring the thickness of the InP spacers between the HJs will provide an estimate on *Rg* in the cavity.

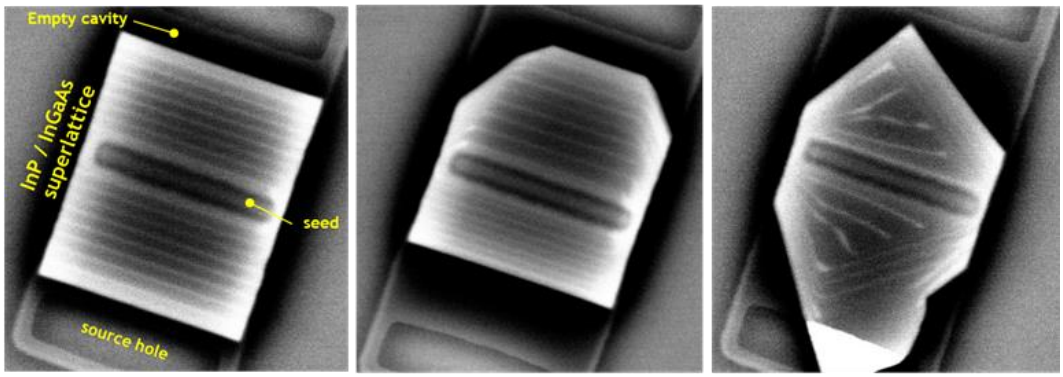

Figure 61. A InGaAs/InP horizontal superlattice via TASE. The difference in contrast allows to track the progression of growth inside the channel. All three structures are imaged form the same sample.

The length of the InP layers between the HJs shown in Figure 57 and Figure 60 has been measured and divided by the individual growth time for that layer to obtain the average growth rate for each. This average growth rate is then plotted versus distance from seed in

Figure 62. When observing the InP spacers in the 3HJ sample in Figure 60, each grown under the same conditions and for the same time, it is clear that the

thickness of each decreases with the distance to the source hole. This is in contrast with expectations. During the confined epitaxy the growth front advances towards the source hole, reducing the distance between them, and since MOCVD growth is driven by diffusion, growth rates are then expected to increase with time, as has been observed in previous studies[64].

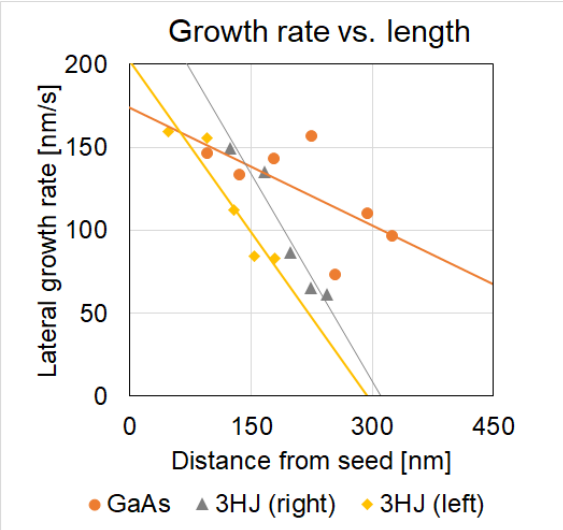

Figure 62. Average lateral growth rates for the individual InP layers between the HJs.

A possible cause of this reduction of *Rg* is the presence of non-selective growth, i.e., parasitic nucleation on the dielectric. While selectivity is almost perfect for InP homoepitaxy, arsenic containing growths have, in our experience, proven more challenging. With the progression of growth these parasitics quickly increase in size due to the low fill factor and consequent strong loading effect typical of SAG. These parasitics are adparticles with most of their surface area

directly exposed to the atmosphere that become disproportionally large, having a higher *Rg,* compared to the confined growth. We hypothesize that these parasitics when located near template source holes, act as capture sites for the metal organic precursors in the nearby gas phase, partially impeding diffusion inside the templates. The effect is a local lowering of the precursor molar flow towards the growth interface, thus reducing *Rg* of the confined growth.

2.2.4 Metal contacts

The parasitic removal process described in 2.2.1.2 was later refined with the addition of a protective ALD alumina layer that better protects the confined growth and expands the selection of wet etch chemistries. The process is described in reference [66] and can be seen in Figure 63. Previously we described how directional RIE was used. While still effective in removing III-Vs, RIE also leads to significant damage to the oxide roughening it, while also being slow, with a typical etch requiring 30-40 minutes. Instead, we opted for a different directional ICP etch using BCl3/Cl2 chemistry, lasting only for 15 s with an approximate etch rate of 80 nm/min, only removing the alumina "shell" from parasitics. This was followed by a $H_3PO_4/H_2O_2/ H_2O$ (1:1:20) solution for 12 min to remove the now exposed III-Vs. A final 2.38% TMAH wet etch (using the commercial developer "AZ 300 MIF") of 5 min will then remove the rest of the alumina protective layer (1.6 nm/min etch rate at room temperature).

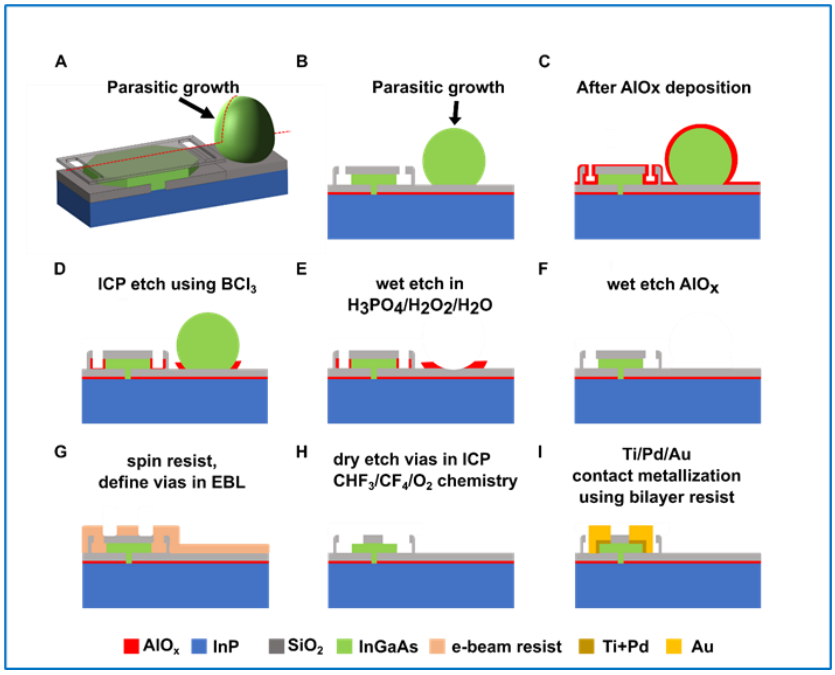

Figure 63. Process steps to remove parasitcs and deposit metal contact on confined growths[66].

The parasitic removal process is important to allow for further processing of the structures. Specifically, it clears up lithography alignment marks from unwanted deposition, necessary for the tight alignments needed to define electrical contacts to the TASE structures. This while leaving the confined growth undamaged. Some dark marks are visible post-removal process in the position where parasitics were, but while unclear what their nature is, they do not seem to impact any following fabrication step.

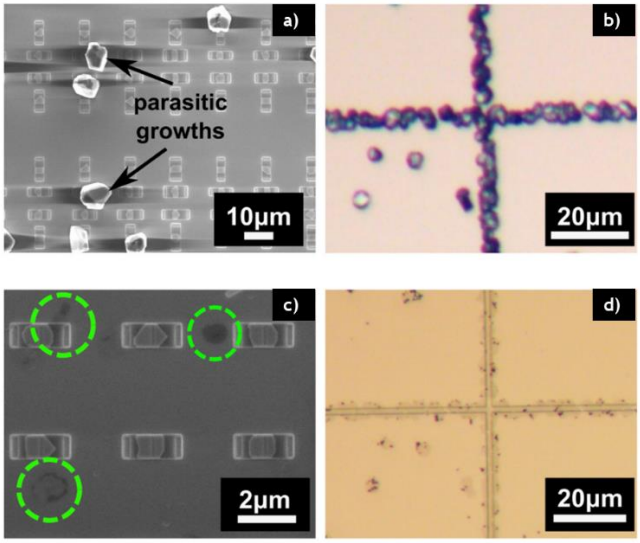

Figure 64. Alignment marks and InGaAs TASE structures exhibiting parasitic nucleation (a,b) and after the parasitic removal process (c,d). Green circles in (c) show where parasitic growths were before the cleaning process.

To fabricate the contacts the photoresist CSAR was used to first define vias, then etched in the SiO_2 top oxide with ICP etch using a $CHF_3/CF_4/O_2$ chemistry. Contacts were then patterned with a bilayer resist process and a stack of 10 nm Ti/ 10 nm Pd/ 200 nm Au was deposited with e-beam evaporator.

Once contacted with metal, it was possible to wire bond the TASE structures wo measurement tools to extract material properties, otherwise hard to measure with typical material characterization tools.

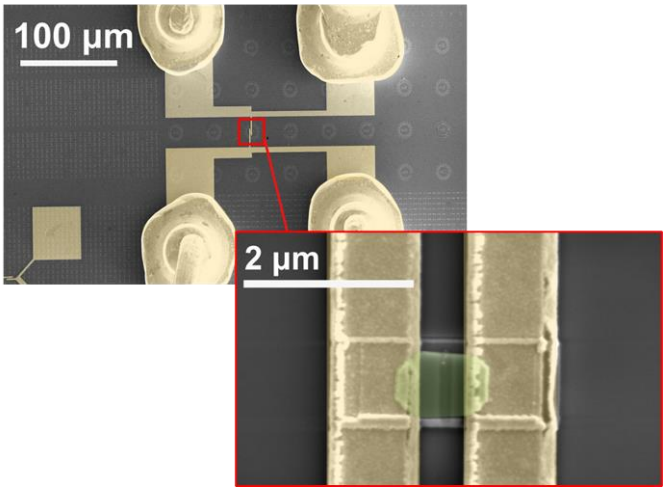

Figure 65. Wire bonded and lithographically defined metal contacts, contacting TASE growths through etched vias in the top oxide [66].

Low-temperature magneto-transport measurements were done showing Shubnikov–De Haas oscillations in the longitudinal resistance of InGaAs TASE nanostructures from which doping concentrations were extracted. We tried comparing doping densities in TASE with planar 100 nm thick InGaAs samples grown with similar parameters. This is not straightforward because of the inherent requirements of using lower group III flows and higher V/III ratios in TASE in order to improve selectivity, and V/III ratios do impact incorporation of Si dopants[67]. Nonetheless, by using the same disilane (the Si dopant precursor) of 1.43 × 10−8 mol/min doping concentration was extrapolated at 2.5×10^{18} cm^{-3} for the TASE sample versus 3.0×10^{18} cm^{-3} for the planar one measured via Hall. Mobility was also extrapolated at 684 $cm^2/V\,s$ which compared poorly to 3900

cm^2/V s of the planar sample. Low density InGaAs nanostructures have been reported to yield 7500 cm^2/V s [68]. This low mobility suggests large amount of defects are present in the laterally grown nanostructure, correlating well with other TEM analysis on similar structures [63].

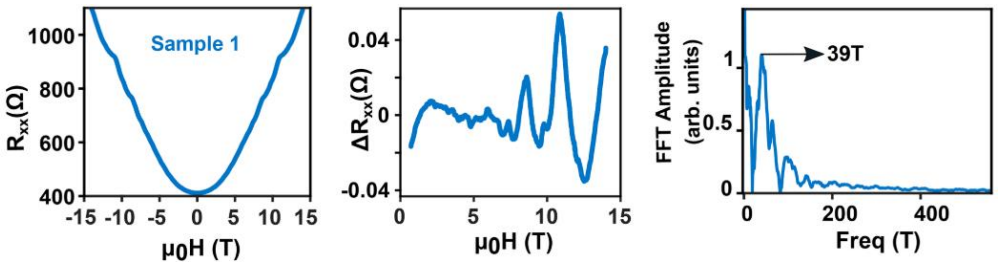

Figure 66. Low temperature magneto transport measurements used to extrapolate doping concentration and mobility form doped InGaAs TASE structures. From [66]

3 Confined epitaxy as virtual substrate for photonic integration

3.1 Introduction

One of the guiding principles behind TASE of III-V materials on silicon substrates is to leverage the already present and mature silicon-based fabrication infrastructure. If targeting high throughput and scalability is a goal, then CMOS compatibility of the entire fabrication process is important. A laterally grown III-V material via TASE, instead of being used to create a nano scale device entirely inside the template as in Chapter 2, could be used as a pseudosubstrate for subsequent growth of III-V based devices, without the need for native substrates (example in Figure 68. After growing long enough inside the template, openings in the top oxide could be created with a selective etch, exposing the III-V material. Samples created this way can be loaded into the MOCVD reactor to add, for example, a laser structure. This would occur in a planar/conventional manner albeit via selective area growth in the openings. Once all the epitaxial layers are in place, fabrication of a device would follow industry standard steps like mesa formation, ion implantation, metal contact deposition and via formation (see Figure 67).

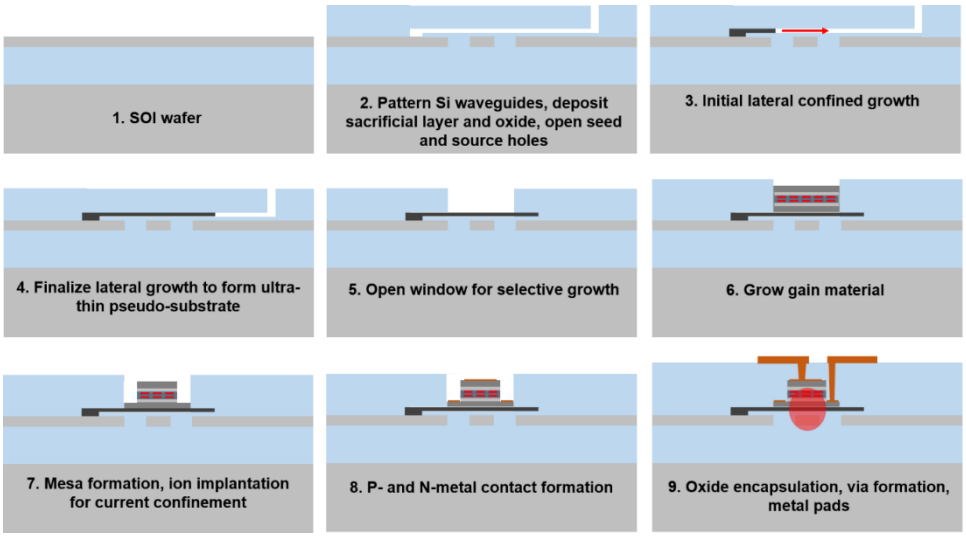

Figure 67. Schematic of an example fabrication process of a laser on a pseudosubstrate grown via TASE on SOI.

The lattice mismatch that exists between silicon and most III-V materials is significant and the resulting critical thickness is very small. The strain that is created must be relieved by the appearance of misfit dislocations. These dislocations are localized near the interface of the dissimilar materials, but once formed, may climb through the epilayers as threading dislocations. These TDs have energetically favorable glide planes dependent on the material. In III-V semiconductors like InP and GaAs they tend to rise at an angle of 60°.

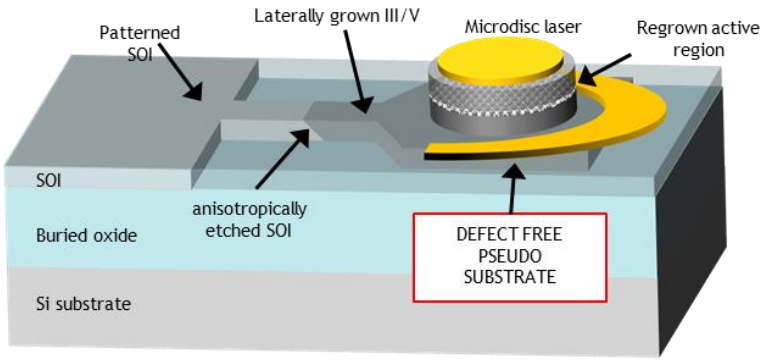

Figure 68. Illustration of a micro disk laser grown on laterally grown pseudosubstrate on SOI.

For SAG techniques that involve high enough aspect ratio structures this means the TDs will end up terminating at the template or mask edge. For TASE this means that the TDs that are generated at the seed hole will be confined in the initial, vertical part of the growth (see Figure 69), leaving the remaining laterally grown material ideally defect free (or at the very least, if defects are present, they will not be due to the Si/III-V interface but will be generated during the growth itself for separate reasons).

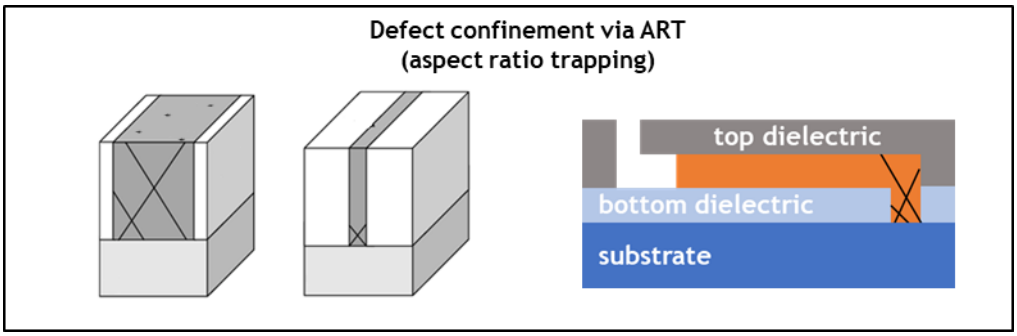

Figure 69. The mechanisms behind ART are also present in TASE, with defect confinement occurring near the seed hole.

The defect confinement mechanisms in TASE are inherent to the lateral nature of the growth so other more conventional defect engineering approaches (thick buffer layers, DFLs, composition gradients) are either unnecessary or inapplicable.

Because growth is driven by diffusion mechanisms, longer and thinner templates lead to lower growth rates. So, while TASE structures were demonstrated as thin as 50 nm, considering the growth rate reducing effects of thinner templates, a 200 nm thick lateral growth is more reasonable in terms of scalability and limiting total growth times. This still makes the TASE grown layer gain the advantage of being an order of magnitude thinner than the state-of-the-art defect engineering for planar growths (see Figure 70). Planar growths of III-V on silicon need to be 4 microns or more to achieve a low enough defect density

that enables devices.

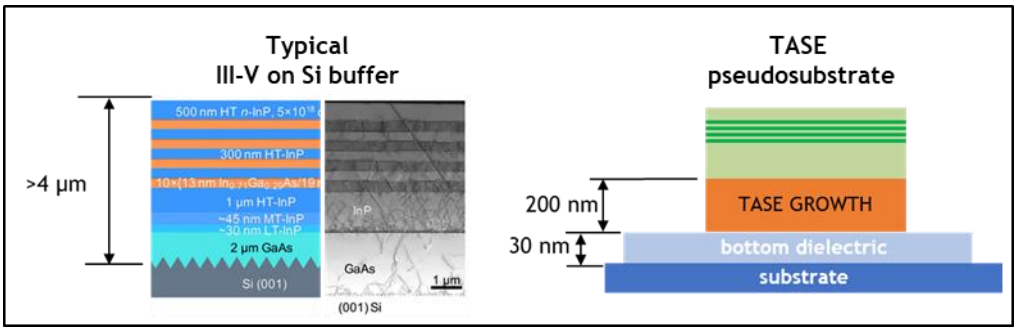

Figure 70. Comparison of III-V on Si pseudosubstrates between planar epitaxy (left) and TASE (right) showing the differences in total thicknesses and hence distance from the future device layers and the substrate.

This proximity facilitates integration between the devices grown on the TASE pseudosubstrate with, for example, any passive waveguide easy to couple to.

3.2 Materials and methods

The fabrication process for TASE on silicon was largely similar to that described in paragraph 2.1.1, with key differences due to chemical compatibility of the substrate with select wet processing, choice of lithography, and overall size of the templates themselves. The description of the fabrication here will be less detailed here and I redirect the reader to previous paragraphs for a more in-

depth discussion, if desired. If reference to the “previous process” or “previous results” are made, then the references are to those described in Chapter 2.

After initial trials that made use of EBL, with scalability and CMOS compatibility of the process in mind, together with cost, the lithography for all layers used in paragraphs 3.2.1.1 and 3.2.1.2 was also developed for the DUV 4” ASML photolithography tool available in our nanofabrication facility. A single lithography plate was used for all patterns because it was able to fit all nine masks necessary for both processes and their variations implemented for development purposes. The nine masks are listed here below. The masks are developed for lithography with positive resist unless specified.

- Si – seed layer – 150 nm seed holes
- Si – seed layer – 200 nm seed holes
- Si – seed layer – 250 nm seed holes
- Si – sacrificial layer
- Si – sacrificial layer – negative resist
- Si – source hole layer
- SOI – sacrificial layer
- SOI – sacrificial layer – negative resist
- SOI – source hole

The rationale was to be enable true side by side comparisons, where different variations of the seed/sacrificial/source hole would be present side by side on the

same samples, seeing the same growth environment at the same time. This would eliminate the need to repeat MOCVD recipes exposing ourselves to the natural but unpredictable variations of the tool. A negative resist mask was also included but never tried.

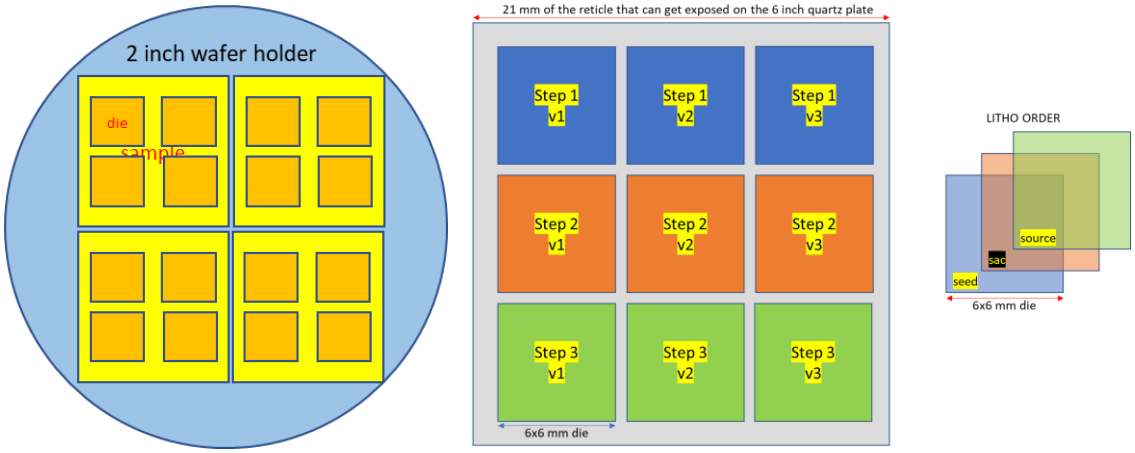

Figure 71. Illustration of the arrangement of the mask layers on the lithography plate.

3.2.1 Fabrication of templates

3.2.1.1 TASE on Si

The starting substrates used were (001) Si 4” wafers that, while arguably small for most modern large-scale manufacturing, are a good proof of concept substrate

to demonstrate CMOS compatible processes and had good compatibility with the tools available at UCSB.

A thin 5 nm Al_2O_3 etch stop layer was deposited via ALD followed by a 20 nm thick PECVD SiO_2 layer. The etch stop layer will allow us to remove the sacrificial layer with a selective wet etch while protecting the substrate and the growth initiation surface from damage. A thicker bottom dielectric would be more forgiving for subsequent dry etch steps, but the rationale was to keep the process as similar to our previous one to minimize changes and capitalize on previous experiences.

Seed holes were lithographically defined, using EBL in earlier trials first, with the DUV ASML in later ones. All lithography development, as per standard practice, goes through focus and exposure parameters optimization via the use of an aptly named “focus/exposure matrix”, that defines the mask in an array of progressive values allowing to identify the optimal parameters.

A positive resist process was used in all cases, mainly because of our familiarity with it. It is worth mentioning though that positive resist allows defining features smaller than the nominal ones of the mask, simply by underexposing or under developing the resist. Small seed holes in our experience were important to yield a good single crystal nucleation and initial growth, so this characteristic of positive resist meant having a tool to further minimize seed hole size beyond the typical resolution of the lithographic tool. The holes themselves were etched using the SLR Fluorine ICP-RIE with a CHF_3/CF_4 chemistry. The

available tool accepted 4” wafers directly streamlining the process with no need for other carrier wafers. Additionally, the etch tool is equipped with an Intellimetrics laser monitoring instrument that allows to monitor the etch as it progresses. The significantly different etch rates of the SiO_2 and the Al_2O_3 makes for an abrupt, easy to monitor, change in the signal. At the same time, small features like our ~200 nm seed holes and the small overall fill factor, would cause for the etch rate to be significantly slower than a blanket etch on a planar sample. So, the laser monitor in this step could be used effectively only for the purpose of having a reference and only if a specific, somewhat larger pattern similar comparable to the spot size of the laser is included in the mask.

The sacrificial layer was sputtered a-Si. It has been previously shown that thickness of the lateral cavity in TASE would influence growth rate because it would limit the largely diffusion-based mass transport of the precursors to the growth front. A relatively thick layer of 150 nm was chosen. This would not significantly impair any efforts with integration with passive photonic element like waveguides, because any active layer grown on top of the TASE virtual substrate would still be in proximity of the substrate itself, especially when compared to planar III-V on Si efforts. Additionally, from a more practical angle, the a-Si sputter deposition times were kept reasonably short at ~1 hour. The sacrificial layer was then etched via the same SLR Fluorine ICP tool as for the seed holes (and with the same advantages) this time with a $C_4F_8/SF_6/CF_4$ chemistry, more selective towards Si. An alternate mask was designed for a

negative resist but never tested, mostly because positive resist trials showed good results.

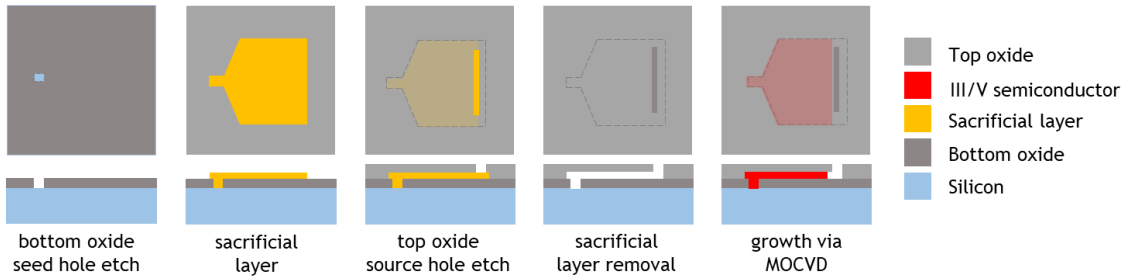

Figure 72. Diagram of the fabrication process for a TASE on Si template.

The top dielectric was layered via PECVD. Most of the templates were 150 nm thick SiO_2. This thickness was tried first on templates whose maximum length was 3 μm yielding overall good results and no issues. Later fabrication of larger templates, namely 4-6 μm in length, showed issues like layer delamination, cracking and deformation or collapsing of the TASE "ceiling". So different thicknesses were also trialed, as was a PECVD Si_3N_4 only layer, and finally a stress compensated $SiO_2/Si_3N_4/ SiO_2$ stack. Details regarding these different approaches and the reasoning behind them are discussed later.

Finally, source holes were etched with the same SLR Fluorine ICP recipe used for the seed hole. A 300 nm space was left from the edge of the template to the edge of the source hole to make sure that the integrity of the sidewall wasn't compromised. Over etching was not an issue both because it was easy to monitor progress with the laser monitor, and because over etching would occur in the a-Si

layer that is a sacrificial one.

3.2.1.2 TASE on SOI

Final TASE on SOI structures strongly resembles the TASE on Si ones, but the process differs substantially.

Starting substrate was a silicon on insulator (SOI) wafer with a 500 nm thick silicon device layer and a 2 μm buried oxide (BOX). Due to availability of the material a single 4" wafer was diced into 1.5 x 1.5 cm square samples, then individually processed. Before dicing the wafer was protected with a layer of photoresist to protect it from dicing dust. Individual samples were spun while sprayed with NMP rinse, and then boiled in piranha solution to remove any organic residues.

The BOX is used as the bottom oxide of the template and the SOI layer itself is used as the sacrificial layer. To create a top oxide, the sample is thermally oxidized partially, with the oxide forming from the outside to inwards. Before the oxidation though the shape of the templates needs to be defined. This was achieved with EBL lithography and a dry etch with the SLR Fluorine ICP tool and a $C_4F_8/SF_6/CF_4$. The thermal oxidation "consumes" the silicon inwards so that needs to be taken into account when designing the feature size and compensating for the loss of material. The goal was to have a 220 nm template cavity so oxidizing 280 of the 500 nm of silicon from the SOI leads to a 637 nm of top oxide.

Source holes are defined and etched as in the TASE on Si process, with EBL lithography and SLR Fluorine ICP etch.

Finally, the template cavity is created by removing the sacrificial layer. This is the step where the major differences from the on-Si process arise. There is no seed hole towards which the cavity reaches down to the substrate here. Instead, the SOI is only partially removed leaving behind some amount of Si to act as the growth initiation seed. This explains the funnel-like shape of the structures. The main body of the cavity would serve as the large area to create the pesudosubstrate, but the seed area is created by etching all the way back into the "neck" so to leave a small area for nucleation. To allow room for etch tolerance and control the "neck" is 1 μm long. The neck then expands into a larger block again that simply provides mechanical stability to the entire template (not visible in the Figure 73 diagram but clear in the Figure 84 images).

The sacrificial layer is removed using a combination of an isotropic XeF_2, to remove most of the material at a fast etch rate, and a slower anisotropic KOH or TMAH etch to better control the final growth initiation surface position inside the template (i.e. cavity length), while also creating a known (111) type facet.

An alternative approach was also trialed as a proof of concept for the process on full 4" wafers. The availability of 4" SOI was limited and time consuming, with coring 12" wafers into 3x4" wafers being the best option in terms of material quality, so to simulate an SOI wafer we used PECVD deposited SiO_2 (100 nm) and sputtered a-Si (150 nm) to recreate the layers. All other steps in the process

would remain as described above. This was only a proof of concept of the fabrication process for the templates though because a-Si, not being crystalline (by definition), is not etchable into smooth facets controllably with anisotropic wet etches, leading to irregular growth initiation surfaces that, in turn, lead to poor growth results.

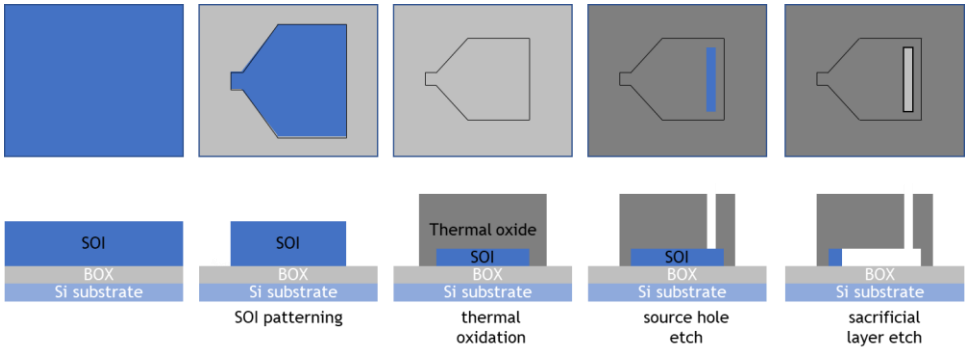

Figure 73. Diagram of the fabrication process for a TASE on SOI template. The remaining silicon of the SOI after the sacrificial layer etch will act as the nucleation seed during growth.

3.2.1.3 Lateral confined ART

A simplified, lateral confined approach was also explored as illustrated in Figure 74. The starting samples and substrate were the same as for the TASE on SOI described above.

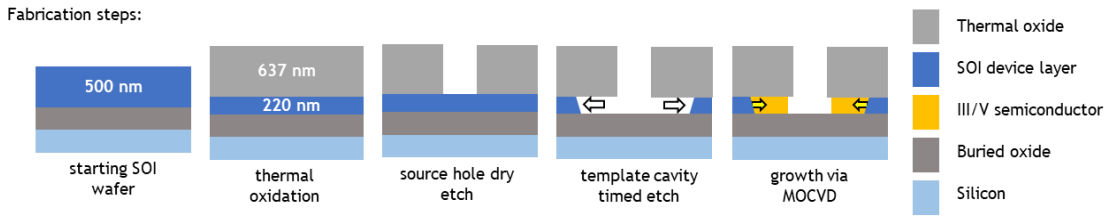

Figure 74. Diagram of the fabrication process of the templates for lateral confined growth.

The entire sample is thermally oxidized at 1000°C for 1 hour and 30 minutes, creating a thick top oxide measured at 637 nm, while leaving 220 nm of the initial 500 nm of silicon from the SOI layer.

A single lithography step is needed to define the high aspect ratio "strips" of various dimensions (0.5, 1, 3, 5 and 10 μm) using a GCA i-line (365 nm) stepper. A dry etch with the SLR Fluorine ICP with a CHF_3/CF_4 chemistry and a 400 nm/min etch rate is used to create the trenches in the thermal oxide, i.e. the source holes, exposing the silicon underneath. Cleaning step is a 30" O_2 plasma clean to remove any etch skins followed by a 10 min boiling piranha solution bath.

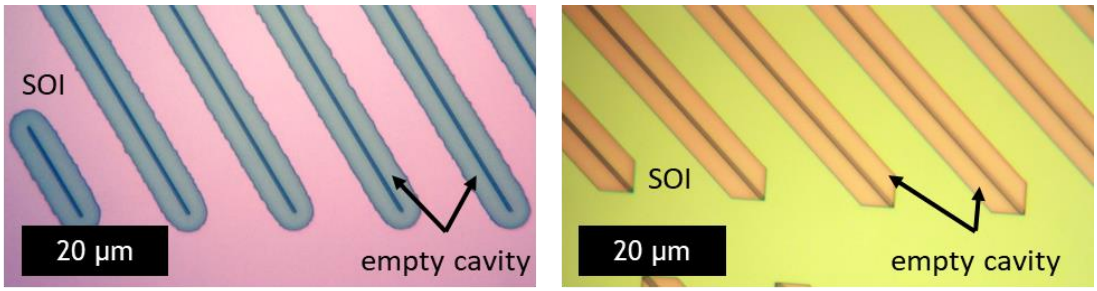

Figure 75. Top view SEM images of the trenches after partial removal of the sacrificial layer with the isotropic XeF_2 etch (left) or with a KOH etch (right) that exposes the crystallographic

planes for growth initiation.

A combination of an isotropic XeF_2 etch (two 30 s cycles at 2 Torr) and an anisotropic KOH etch (4 min, 20% solution at 40°C) is used to create a cavity up to 4 µm deep on both sides of the trench, ending in (111) type facets to act as growth initiation surfaces. XeF_2 is used mainly because of its faster etch rate when compared to KOH, but a KOH only etch is also possible, with the only caveat being the anisotropic nature of the etch having different etch rates and effects based on the orientation of some of the structures.

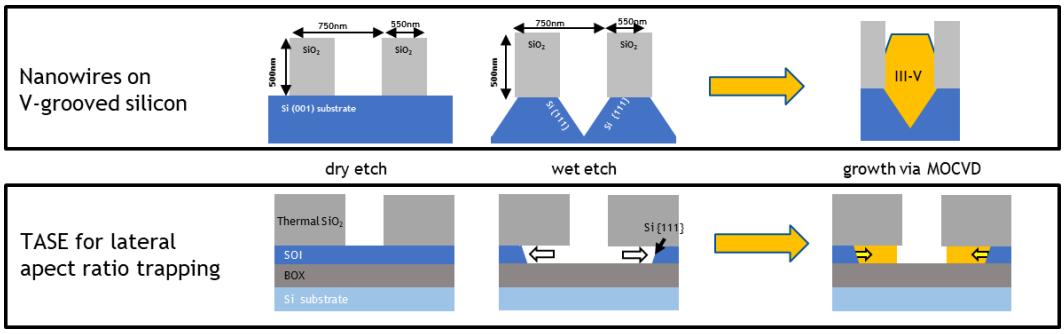

Figure 76. Diagram comparing III-V nanowires grown on v-grooved silicon and lateral confined ART. While the direction of growth is different the lateral template can be visualized as a v-groove rotated 90°.

The motivation behind this approach is twofold: simplicity of fabrication and achieving larger area pseudo substrates.

The single lithography step and the relatively large features reduce the challenge of fabrication and help with both fast turnover and repeatability. The size of the

templates and the thicknesses of the layers involved allow for simple optical microscopy to be used to evaluate most of the steps, including the sacrificial layer removal.

The previous TASE on Si and SOI approaches, as will be shown in the results, proved to be promising only for smaller footprint templates (and hence pseudo substrates grown inside of them). While still useful for a selection of devices it would exclude larger/longer ones like ridge lasers that require an order of magnitude longer structures.

3.2.2 Growth via MOCVD

In chapter 1.4 the challenges of III-V on silicon heteroepitaxy and the common techniques to tackle them are described. While at the highest level TASE on Si, on SOI and lateral ART are very similar, the differences in template shape, initial crystal plane and fill factor required individually developed approaches for successful growth (where achieved).

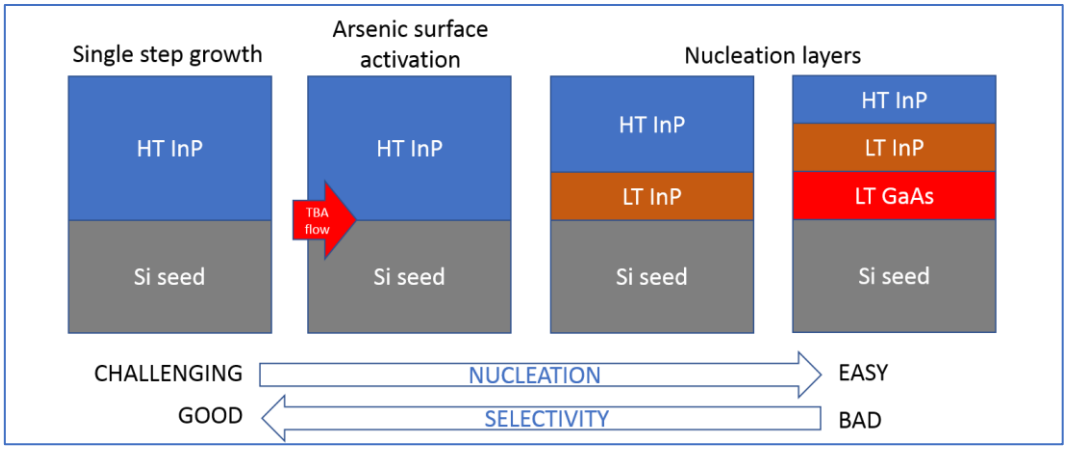

Figure 77. Diagram illustrating the compromise between selectivity and ease/quality of heteroepitaxy on silicon with typical III-V on Si approaches.

Direct high temperature growth of InP on Si yields poor results due to uneven nucleation and high defect density, so for all the SAG on Si trials additional layers or techniques had to be used. Several different growth recipes were attempted differing in some details but sharing the overall approach, compromising between ease of nucleation and selectivity results, as schematically represented in Figure 77.

Right before loading a sample in the reactor, a dilute HF dip was used to remove the oxide on the silicon seed. A high temperature 20 min 800°C in situ anneal introduced before any growth would desorb any additional native oxide that would have formed. Cooling down from the anneal temperature to the growth temperature was done under TBA rich atmosphere as an arsenic soak to prepare for nucleation. For GaAs growths, a low temperature (450°C) GaAs nucleation layer would wet the silicon seed with a 2D type growth layer. This

would be followed by one or more intermediate temperature layers before the final bulk GaAs growth. For InP runs a low temperature InP (<500°C) would precede the final bulk HT InP (600-650°C).

In the lateral confined ART structures the fill factor was significantly higher, ranging from 1% to 25% depending on the pattern, so selectivity issues were not as prominent. Inclusion of low temperature GaAs layers would still cause some parasitics but to a much lesser extent than TASE on Si. The silicon seed area was also considerably larger in size consisting in a large strip of exposed silicon beneath the top dielectric, so as we will see later, homogenous nucleation proved to be harder.

3.2.3 Characterization

The size of the templates made it so that optical microscopy was a sufficient tool to evaluate most of the fabrication steps, easing the fabrication process. When removing the sacrificial layer, the thickness of the top dielectric was sufficiently thin to easily provide enough contrast to distinguish between the empty cavity and the leftover sacrificial silicon. Both the XeF_2 and the KOH/TMAH etch rates suffered from poor repeatability (the XeF_2 because of the tool itself, the wet etches because of temperature instabilities of the bath), so OM helped in empirically determining etch progress. Feature size of the templates themselves, excluded the seed holes for the TASE on Si templates, were also big enough (and

not critical enough) that success of lithography could also be determined through OM inspection only.

While the presence/absence of confined growth was could also be determined via OM, it was better determined with the use of SEM. Thickness of the top oxide was low enough for the primary beam to penetrate through to the confined growth and provide enough contrast to image it. A Monte-Carlo type simulation determined that a primary beam voltage between 10-15 kV was optimal with dielectric thicknesses around 200 nm. To image more specific details of the confined growth, like the faceting of the growth front or the growth initiation interface, removal of the top dielectric was necessary. A simple wet etch with selective chemistry like BHF was sufficient to remove the dielectric without damaging the III-V confined growth, although making SEM imaging a destructive technique.

While a secondary electron detector would already provide clear Z-based contrast differences between III-V and the silicon or the dielectric, the use of a backscatter electron (BSE) detector would provide even more details. Specifically, some samples revealed polycrystalline growth with the different crystal domains being clearly highlighted by BSE imaging (after removal of the top dielectric).

Another SEM technique that could be useful to evaluate the quality of the lateral growth would be ECCI (see paragraph 1.2.5). Even though the grown layer is relatively thin, the backscatter electron signal is collected form only the top-

most few tens of nanometers. The amount of laterally grown material, even in successful trials, was very small in terms area coverage (from a top view perspective), making it impossible to identify diffraction patterns. Instead, one could use Kikuchi lines from the silicon substrates, and relying on existing symmetries between the FCC diamond structure of the silicon and the zinc-blende structure of the III-Vs, to detect deviations from channeling conditions and hence defects. Unfortunately, SOI samples used had a thick 2 μm oxide that shielded any signal from the silicon substrate. TASE on Si sample were the exception here since the bottom oxide is only 25 nm thick, but unfortunately, at the time when experiments were carried out, we were unsuccessful in obtaining meaningful measurements, so none are included here. Other work though shown in Chapter 4 proves that this should be possible so it's worth pointing out.

3.3 Results

3.3.1 TASE on Si

Different types of TASE geometries were always included in all samples and all dies, to evaluate how subsequent growth or nucleation was impacted by the template.

Single-seed/single-source hole templates were functionally a scale up of the templates shown in Chapter 2. Single point nucleation, then progressing into

lateral growth, with maximum theoretical dimensions being a 3x3 μm^2 large square. This, when seen as a pseudosubstrate for further regrowth, was designed to accommodate small footprint photonic devices like microdisk lasers or VCSELs. Longer templates with a multi-seed/multi-source hole approach were the same length (seed hole to source hole) but instead 100 µm wide. This width was arbitrary and results with these dimensions could translate into mm long growths. This geometry would rely again on single point nucleation in each seed, but the various lateral growths, after proceeding through the funnel shape, would coalesce into one larger area pseudosubstrate designed to accommodate high aspect ratio footprint devices like a ridge laser, or multiple devices in a photonic integrated circuit.

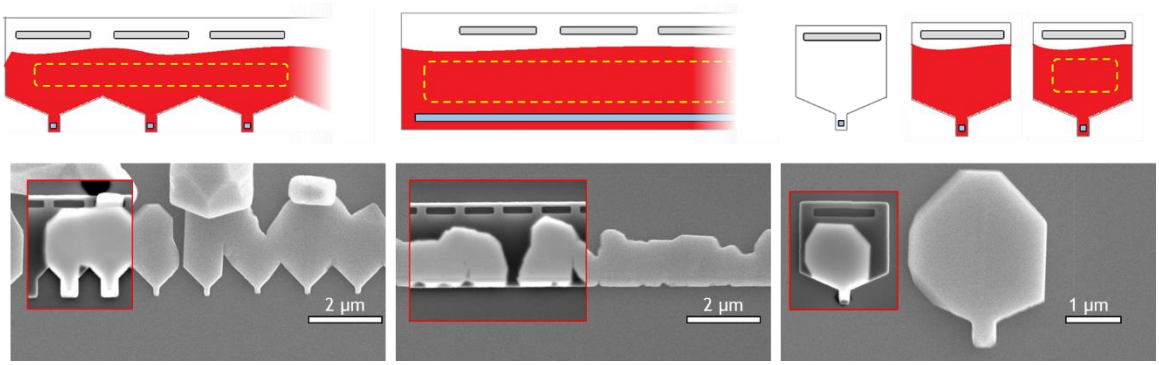

Figure 78. Schematic diagram and representative SEM images of TASE on Si growths of InP before (main images) and after (insets) removal of the top dielectric. The different TASE approaches are shown: multi seed plus coalescence (left), single seed trench (center) and single seed (right). Note images in the insets are similar representative structures on the same sample.

Finally “seed trenches” were included, in wide templates with multiple source holes. The nucleation wouldn’t occur in a single point, but on a long strip of exposed silicon, in a way that is reminiscent of III-V nanowire on silicon[22][69] approaches, with many of the same challenges.

Initial trials were done by using a InP growth recipe for planar substrates with reduced growth rate, to establish a baseline. The lower growth rate was necessary to increase selectivity as learned from previous TASE experiments. The recipe though didn’t include any sort of step designed to aid III-V nucleation on silicon besides the high temperature pre growth H_2 anneal and was a simple HT InP growth. The result was inhomogeneous nucleation and incomplete coverage of the silicon seeds, especially notable in the seed trench design (Figure 79a). The introduction of TBA flow during the cool down from the H_2 anneal and the addition of a short LT InP layer before the bulk HT InP growth improved the nucleation and consequently the rest of the bulk growth (Figure 79b). This multi temperature approach and use of TBA to prime the growth initiation surface is a known aid to nucleation in III-V on silicon literature [5], [20], [70], [71].

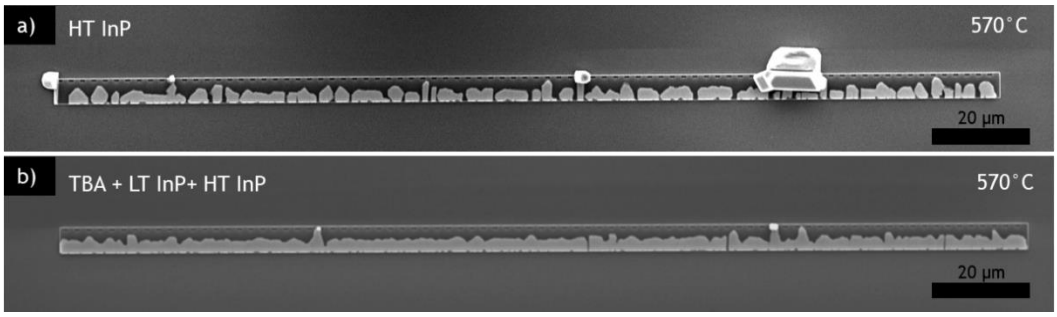

Figure 79. TASE on Si samples grown at the same temperature comparing the improvement on coverage of the initial Si seed from a HT InP only recipe (a) and with the addition of TBA soaking and LT layers (b).

Trying to further improve on nucleation homogeneity, the available literature on III-V on Si would suggest adding LT GaAs nucleation layers. For TASE on Si (and on SOI) approaches the very low fill factor (less than 0.1%) meant that achieving good selectivity was most challenging. Arsenic containing layers, especially at low temperature, would generate parasitics. These layers would occur early in the recipe, having then a lot of time to further grow into micron size particles on the surface of the top dielectric. As described in 2.2.2, these parasitics would act as preferential capture sites of precursors interfering with the confined growth, slowing it down significantly. Because of this a single LT InP was the most overall successful approach to achieve confined growth while maintaining parasitics to a minimum.

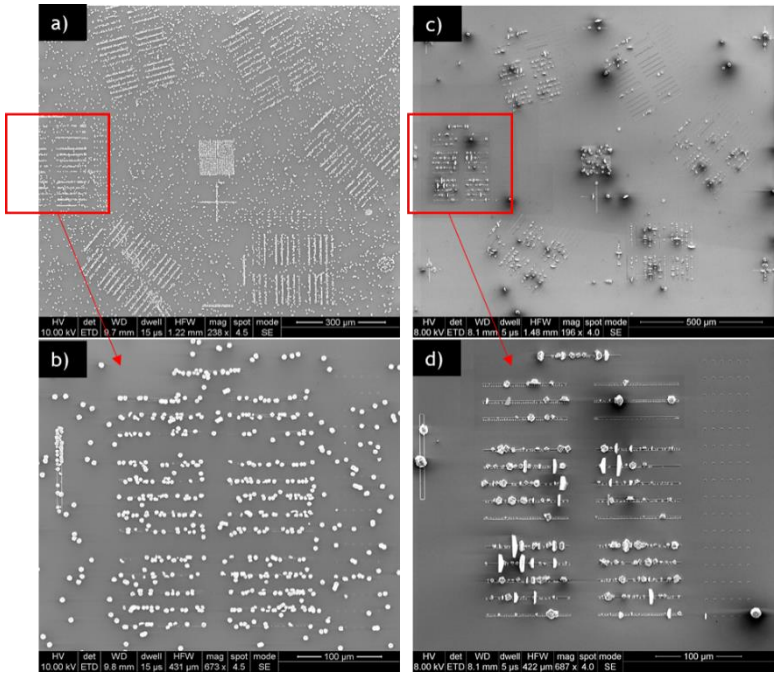

Figure 80. SEM images showing parasitic nucleation in TASE on Si growths of InP that include a LT GaAs nucleation layer (a,b) or omit it (c,d). The GaAs containing recipe results in a more abundant presence of parasitics distributed both on the templates and in the dielectric field.

Different template geometries yielded significantly different results. As it can be seen in Figure 81, templates with initial nucleation occurring on long seed trenches yielded polycrystalline growth, despite coverage of the seed area appearing complete. This is evidenced by the BSE SEM imaging of the lateral growth imaged after the removal of the top oxide. From the same images we can see how single seed type templates yielded somewhat better results with individual growths appearing single crystalline but ultimately failing to coalesce extensively and without clear boundaries appearing.

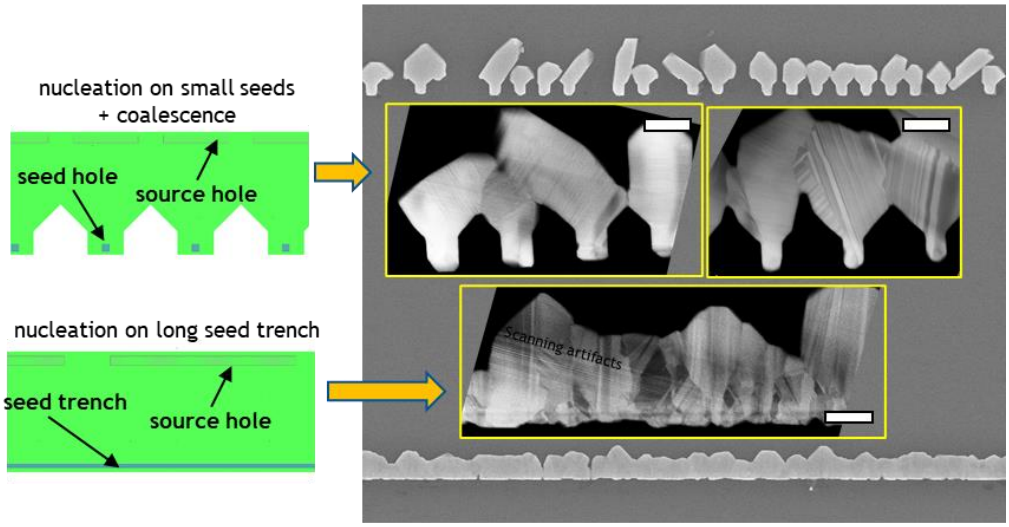

Figure 81. Comparison of structures grown from single seed templates and long seed trench templates. The insets are BSE SEM images showing polycrystalline growth. Scale bar is 1 μm.

Most promising results were yielded by the single seed type templates. The single point seed aiding with nucleation of a single crystal and ample lateral growth with a faceted growth front. For templates oriented towards the <110>, growth rates on the same family of directions being similar thus yielding somewhat symmetric structures. SEM imaging after top oxide removal reveal clear faceting on the edges of the confined growth as seen in Figure 83.

Cross section and STEM analysis in the future will help to further evaluate the material quality of the lateral growth. While some defects like APBs or V-pits appear on the surface as morphology, and thus are identifiable via SEM, others like stacking faults won't be.

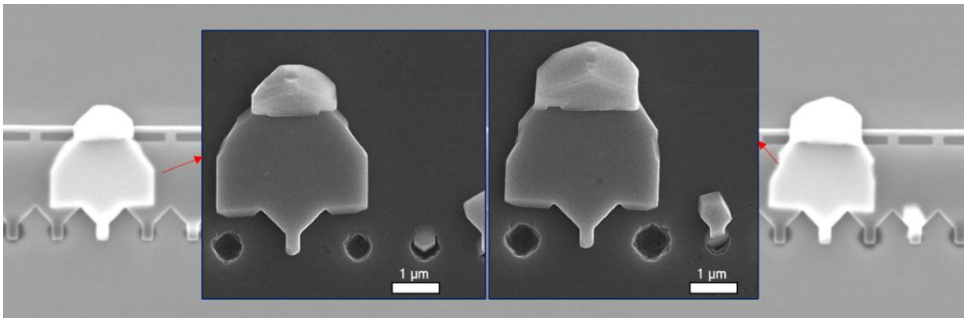

Figure 82. TASE on Si growths of InP as grown (main image) and after removal of the dielectric (insets) with a BHF wet etch. Also visible are over etched seed holes, where the etch stop layer failed.

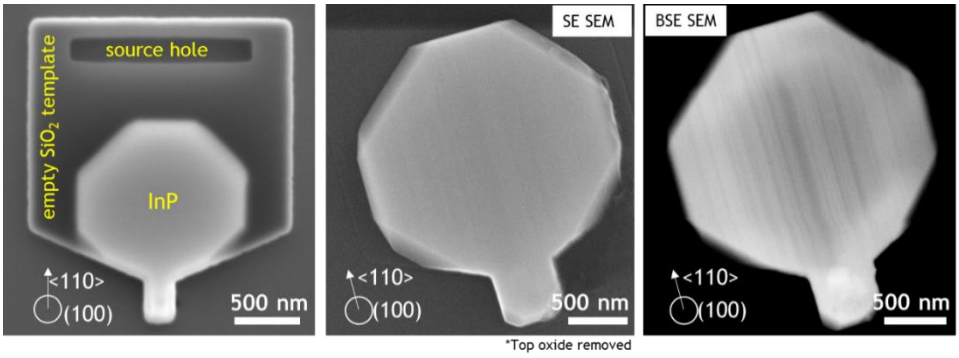

Figure 83. A TASE on Si growth of InP in a single seed type template, as grown (left), and imaged at the SEM after removal of the top oxide with SE (center) and BSE (right) detectors.

Figure 83 shows the best result obtaining throughout our trials, with a single seed TASE template. The lateral growth achieved shows clear faceting and an overall symmetrical structure. Removing the top oxide better reveals the (110) growth fronts aligned with the template with (111) facets appearing in between. BSE imaging shows some striations that might be associated with presence of defects, but have not been further investigated. Commonly in these types of

growth stacking faults may appear on the (111) facets [57], but in this isn't the case because the striations have a different alignment.

3.3.2 TASE on SOI

The TASE on SOI approached proved more challenging and results were limited. Direct comparison of the different structures present on the same die was not possible in the same MOCVD run as for TASE on Si samples. The removal of the sacrificial layer had to be partial in order to leave some amount of Si to act as growth seed. In the TASE on Si structures the sacrificial layer could be over etched because the entire cavity had to be exposed and the etch stop layer at the seed would prevent any damage on the substrate. Here the etch had to be timed until the seed surface was in the narrower channel of the template (Figure 84). The etch times to obtain that were affected by the source hole size, the number of source holes, and the narrow channel width as well. So, the same sacrificial layer etch step would have to be timed somewhat differently when targeting each template geometry (albeit with some tolerance and overlap). Some inconsistencies across identical structures were also present (Figure 85) likely due to the XeF2 partial pressure profile in that etch step, inherent to the tool, at least we the parameters used.

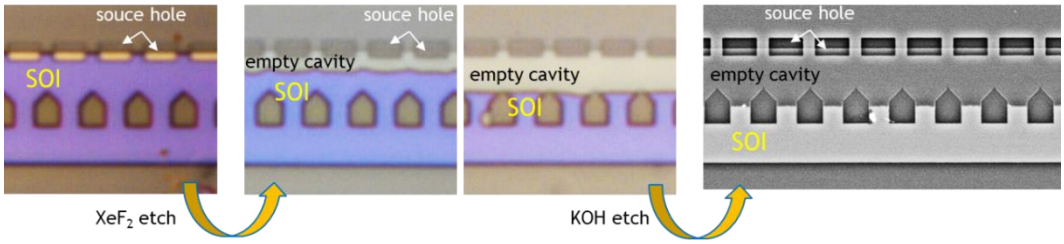

Figure 84. Silicon sacrificial layer being progressively removed by the combination of selective etches leaving a silicon seed surface into the confined channel.

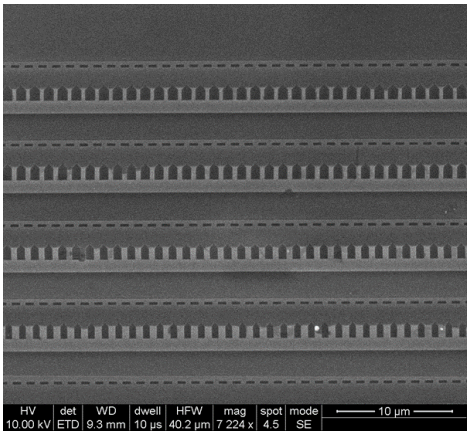

Figure 85. SEM image of a TASE on SOI templates after sacrificial layer removal with leftover silicon to act as a silicon seed. Some inconsistencies between the etches are visible across the image.

Growth near the silicon seed seemed to stem from a single point nucleation when occurring in narrower channels, and hence small seeds. Wider channels with a larger growth initiation area sometimes exhibited growth stemming from more than one point (Figure 86). Insufficient coverage of the silicon seed surface though suggests that improved nucleation steps could solve the problem. As

discussed in 3.2.2 introduction of additional layers like LT GaAs would impact selectivity resulting in no confined growth at all.

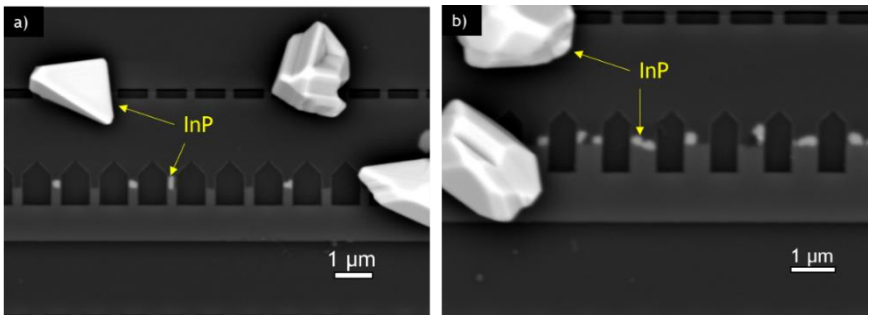

Figure 86. Comparison of InP nucleating on the silicon seeds in the narrowed channels with some visible large parasitics. Nucleation seems to occur as a single point on smaller seeds (a) versus wider ones where two-point nucleation is visible (b).

Few results that showed some promise were achieved with growth recipes similar to the ones used for TASE on Si. Cooldown from the high temperature H2 anneal was done in TBA overpressure. Attempts at including a LT GaAs wetting layer failed due to high amounts of non-selective growth completely suppressing confined growth. LT InP grown at 450°C was necessary to achieve nucleation on most seeds, then followed by HT InP bulk. Some faceting is visible at the growth front suggesting crystalline growth but the areas of no growth and the lack of nucleation on some template seeds suggests that the removal process of the native oxide from the growth initiation surface might have been insufficient. Finally, despite pushing growth times lengthening this HT InP step, extensive lateral growth was never achieved, as seen in Figure 87. This might be due to the

confined cavity being too thin limiting the mass transport of precursors towards the growth front.

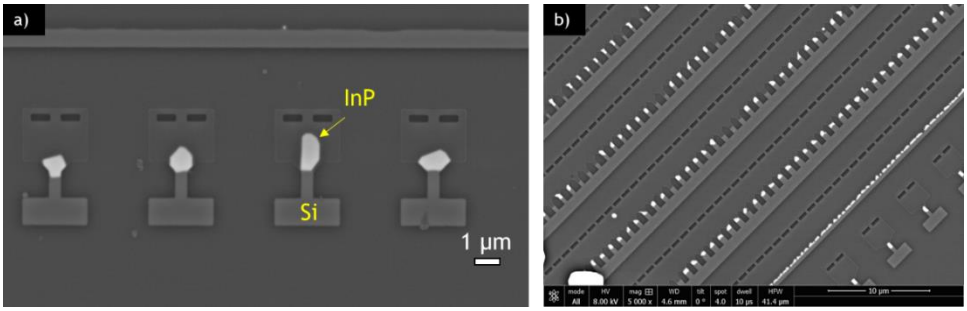

Figure 87. TASE on SOI templates with InP growth in a) single seed isolated templates and b) multi seed templates targeting coalescence of the lateral growth.

3.3.3 Lateral confined ART

Good growth selectivity was in general much easier to achieve in lateral confined ART samples than with TASE. The overall lower fill factor of the dies promotes selectivity. Large source holes are, in this design, wide trenches of 1 to 10 µm providing little constraint to the precursor flow and diffusion towards the bottom of the trench. This led to perfect selectivity over a large area even for GaAs growths (Figure 88).

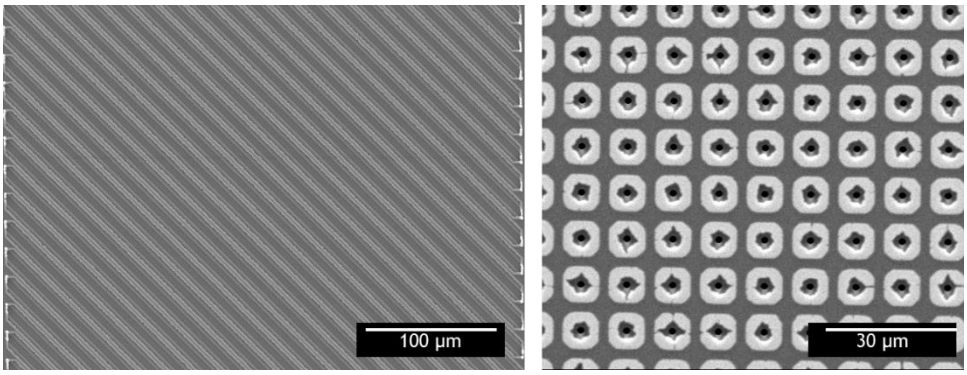

Figure 88. Perfectly selective GaAs growth exhibiting no parasitic nucleation over a large area.

This made possible the use of LT GaAs nucleation layers to initiate growth. The yield in terms of area showing nucleation was 100% with all areas of the silicon seeds covered by III-V growth. High temperature bulk GaAs step would fill up the confined channel.

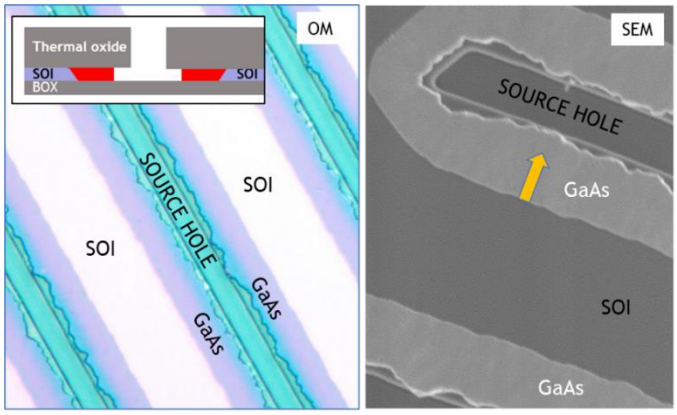

Figure 89. Lateral confined growth of GaAs observed via OM (left) and SEM (right).

While the large source hole allows for mass transport to the bottom of the trench there is still lateral diffusion to overcome to reach the seed and contribute

to growth. The thickness of the channel in this geometry being 220 µm didn't limit growth rate a lot keeping growth times reasonable. There was still a notable effect of the source hole size over the confined growth rate. Arrays of different geometries were included on the sample, including simple round hole arrays of different sizes. When observing the array (Figure 90).it is clear how the lateral cavities were longer for the larger holes and also exhibiting longer lateral growths. This was despite being exposed to the same etch times, XeF2 which is a gas phase etch, and the same growth recipe, also in gas phase. This suggests that the source hole constricts the access to the etch/growth front. All the sizes present on our mask showed this effect.

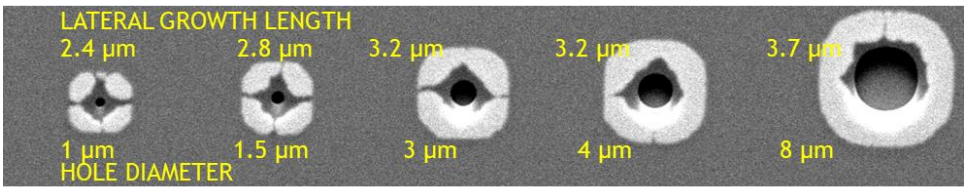

Figure 90. Effect of source hole diameter on lateral growth showing how smaller hole diameter limits growth rate.

While the GaAs growth results were large laterally grown areas that looked promising, imaging with BSE SEM after the removal of the top oxide revealed polycrystalline growth across all trenches. This was also suggested by the very irregular growth front. Initial trials only included the isotropic XeF2 etch so initially we blamed the irregular growth front to an as irregular seed surface. This was largely incorrect because once the anisotropic KOH etch was included to

smooth out the seed surface and promote (111) planes the growth was still polycrystalline.

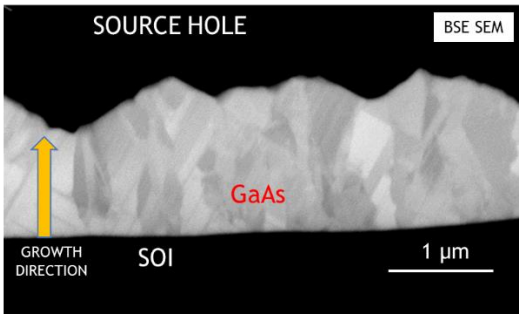

Figure 91. BSE SEM image of laterally grown GaAs after top oxide removal showing polycrystalline growth.

Identical template structures were also used for growth of InP. Initial nucleation was achieved as per the GaAs samples with a LT GaAs initial wetting layer at 430°C, this time followed by HT InP at 550°C and 600°C. There were no issues with selectivity and confined growth appeared successful, sometimes even over growing out of the cavity when growth times were overestimated.

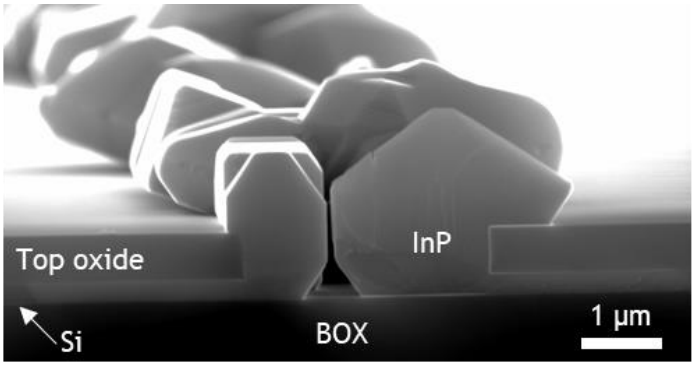

Figure 92. Cross sectional SEM image of confined growth of InP with overgrowth out of the source hole.

Removal of the top oxide and SEM analysis of the laterally grown InP shows area of contrast that might be different crystal domains, but results proved promising. Large InP areas appeared monocrystalline, with overall better appearance of the growth front, some visible faceting. TEM cross section analysis is needed to further study the material quality of these area.

Figure 93 shows these results, also visible are small voids together with a few interruptions in the growth at the seed area. This suggests imperfect nucleation conditions that will affect the rest of the growth, so further optimization of the nucleation layer is necessary.

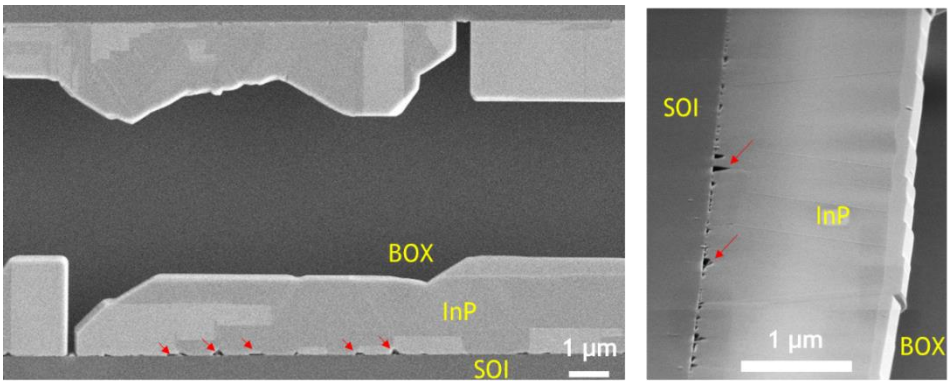

Figure 93. Lateral confined growth of InP observed via SEM after the removal of the top oxide. Red arrows guide the eye to small voids at the growth initiation surface.

We also had the opportunity to compare our in-house samples with thermal top oxide with similar samples provided by a research partner fabricated with deposited oxide, wider and significantly deeper trenches. The depth of the trench was 7 µm and the thickness of the cavity was 400 nm. These were created with a KOH etch in the silicon device layer. The growth initiation surface, because of the anisotropic etch, were (111) silicon planes. The results were largely similar with successful confined lateral growth of up to 3.7 µm of InP and overall good selectivity across the entire sample.

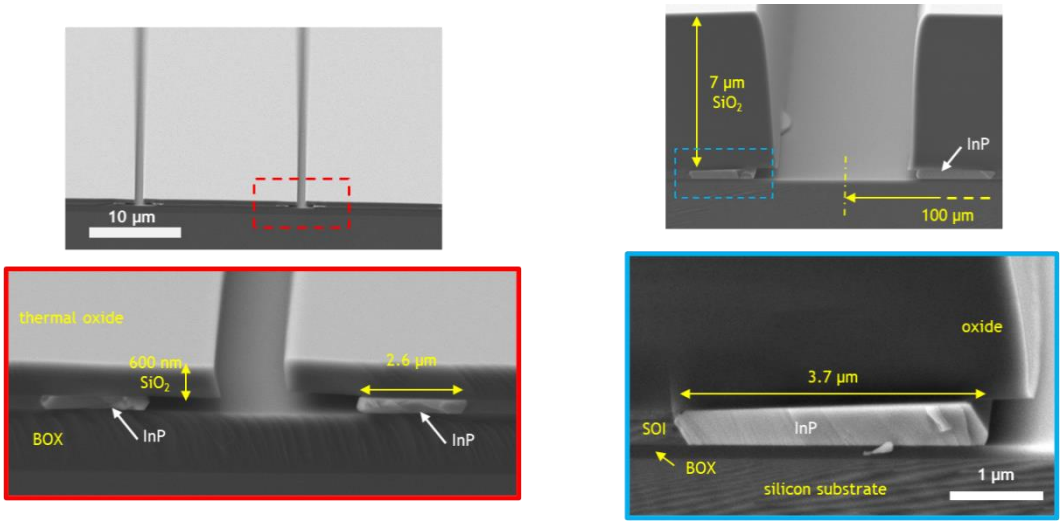

Figure 94. Laterally grown InP in templates of different top oxide thickness

3.4 Future work

When dealing with long templates (great than 3 μm), the major issue we faced was the mechanical reliability of the top dielectric. Deformation and buckling typically occurred after the removal of the sacrificial layer, when that constraint was removed and strain relieved, in addition to after growth (and hence exposure to high temperature and a thermal cycle).

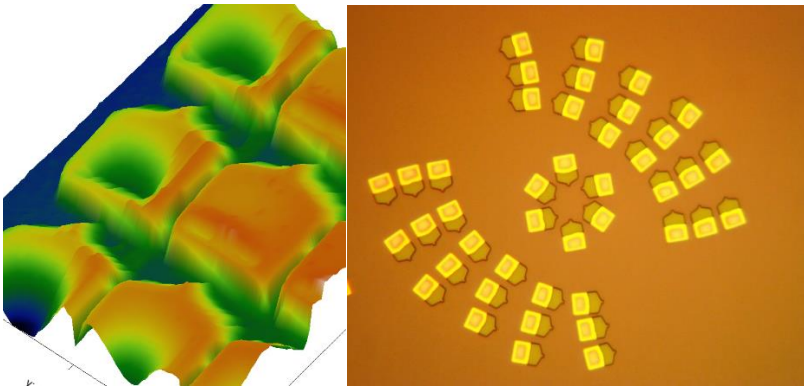

Figure 95. AFM scan (left) of templates with a collapsed top oxide after sacrificial layer removal. OM image (right) of similar templates with sacrificial alyer only partially removed. Visible is thechange in color near the source hole indicating a deformed top oxide.

This was likely due to strain accumulation of the deposited oxide, despite the rest of the template structure being fabricated with the same thicknesses and materials. The high energy environment of PECVD oxides makes them inherently strained, and on average the SiO_2 in the tool we used has around -400 MPa of stress in the 300 nm test layers. To address this, different thicknesses and

materials were tried. A thicker SiO_2 layer solved the delamination, likely from increased sidewall support (typical PECVD sidewalls are half the nominal thickness of the planar layer). This also resulted in deformed convex ceilings, likely due to the increase in overall strain accumulated over the thicker layer.

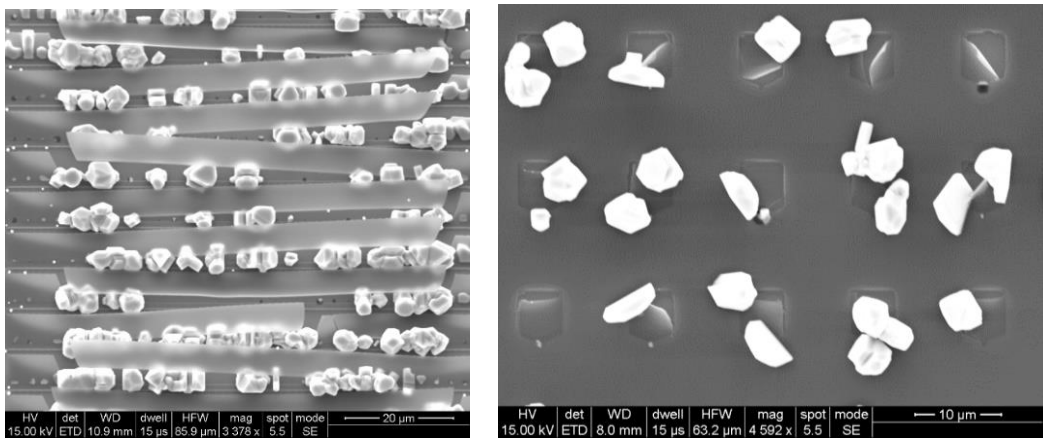

Figure 96. Damaged top oxides of TASE on SOI templates after growth showing cracks (left) and delamination (right).

A thinner SiO_2 layer proved to be fragile with higher instances of cracking and delamination both after growth (due to thermal expansion) and after sacrificial layer removal. A PECVD Si_3N_4 top dielectric was also tested, but despite average stress of 150 MPa, which is lower than the SiO_2 recipes, results were qualitatively similar, with inward buckling and mechanically failing structures. An additional concern with using PECVD Si_3N_4 dielectric was tied to poor growth selectivity outcomes that we had experiences in early trials for TASE templates in Chapter 2.

A multi-layer top oxide comprised of a Si_3N_4 layer sandwiched between SiO_2 layers was attempted to tackle issues with both mechanical stability and growth selectivity. The different sign stress of silicon nitride and silicon dioxide would make this possible. The layers' thicknesses were chosen for stress compensation, aiming at a final total stress of zero, or slightly above zero. At the same time, the material exposed to the growth atmosphere would be SiO_2 only, less prone to parasitic nucleation during growth. A collateral concern was the possible delamination that could occur between layers. While unlikely a problem during the deposition step per se, or template fabrication in general, the thermal cycles during growth could be an issue due to the differences in thermal expansion coefficient between the materials, with SiO_2 having a 6x lower coefficient. In Figure 97 the stress compensated dielectric is shown for a 50 SiO_2 nm/ Si_3N_4 100 nm/50 SiO_2 nm stack. An AFM scan of the final template, after removal of the sacrificial layer, shows no significant bowing or buckling of the template ceiling.

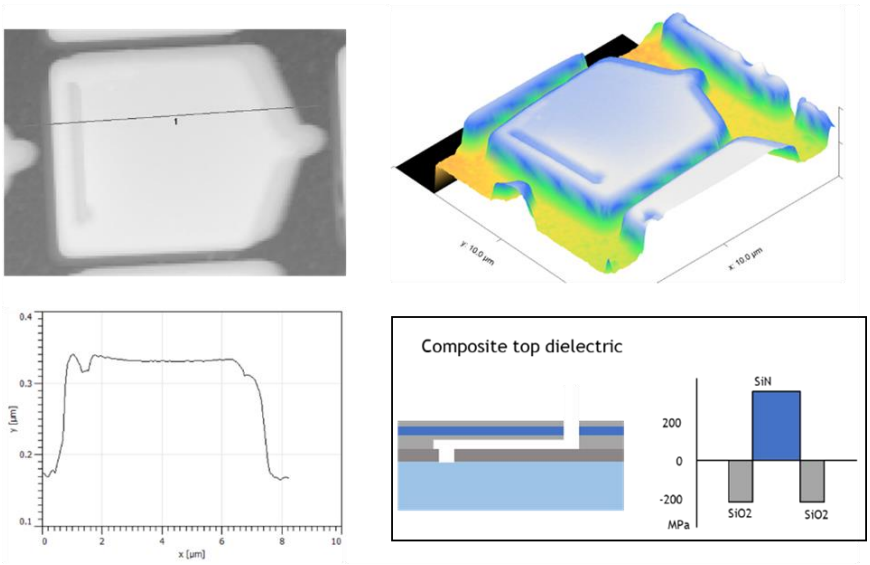

Figure 97. AFM scan of a SiO_2 / Si_3N_4 / SiO_2 composite top dielectric showing minimal bowing. Schematic diagram of the dielectric structure and stress compensation profile (bottom right image).

4 GaAs microridges in a deep recess on (001) Silicon

4.1 Introduction

Selective area growth of III-V semiconductors on standard on-axis (001) silicon (Si) substrates is attractive for large-scale monolithic integration of high-performance active components in silicon photonics. Respectable demonstrations have been reported by growing III-V crystals on intentionally miscut Si wafers or by growing III-V nanowires/nanoridges on patterned Si substrates[72][73]. Either of these approaches though have limitations. Growing on large miscuts, besides

costing more, affects the performance of CMOS devices and makes the process not compatible with standard CMOS processing denying the large scale, high throughput promise of it. Nanoridges, while being relatively mature in their material quality aspect, present issues with insufficient optical gain, high optical loss, and high contact resistance owing to the complexity of device fabrication.

Selective area heteroepitaxy of InP microridges on CMOS-compatible substrates Si were demonstrated, APB free, one of the main challenges of these types of growths[74]. The APB elimination was achieved by creating {111} Si planes via anisotropic wet etching

In this work, we realized APB-free GaAs microridges by SAG on flat-bottom Si (001) recesses on CMOS compatible substrates. Furthermore the addition of strained layer superlattices (SLSs) as dislocation filters achieved a defect reduction down to 8.5×10^{6} cm^{-2}.The final result is a wide and long enough ridge of GaAs that can act as a pseudosubstrate to accommodate an active region that lies still beneath the substrates surface. This enables easy integration with adjacent silicon photonic structures, such as waveguides. This can be achieved in different ways as shown in Figure 98.

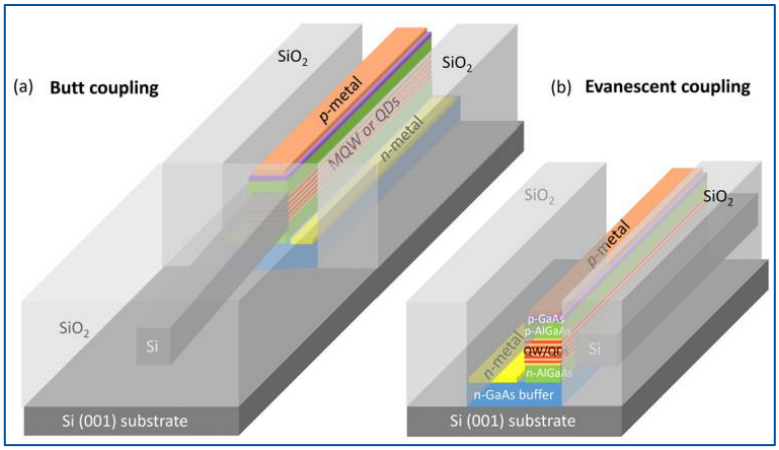

Figure 98. Diagram of full structure SAG in the recess with active regions aligned with passive silicon photonic waveguides via butt coupling (a) or evanescent coupling (b).

4.2 Materials and methods

4.2.1 Fabrication of SAG templates

Starting substrates were either 2” or 4” (001) silicon wafers, which is CMOS compatible (in type, not necessarily size). The choice of the size of the wafer was entirely due to current availability.

To achieve a 5 μm thick oxide, the thermal oxidation at 1100°C requires 64 hours. Even thicker oxides (that would lead to deeper recesses) would be desirable but thermal oxidation is driven by the diffusion of oxygen through the oxide making it a process that follows a power law with required oxidation times growing exponentially with thickness, leading to prohibitively long times.

The oxide was patterned lithographically using a GCA i-line (365 nm) stepper and a positive photoresist. Due to the deep trench design a very thick (7 μm) resist was used leading to some stability issues.

A dry etch in the SLR Fluorine ICP-RIE and with a CHF_3/CF_4 chemistry was used to etch the trenches through the oxide and into the silicon substrate. The etch used was not intended for such thick oxides leading to a relatively long etch time of 45 min but a good overall result. Different trench sizes lead to slightly different etch rates due to loading effects in the chamber. So, while the laser monitor could reveal when the oxide was removed in the probed calibration area, a 20% over etch was used to make sure all patterns had completely exposed silicon bottoms. This led to visible micro trenching effects near the mask edges as seen in Figure 101.

To clean the samples after the long etch samples were exposed to O_2 plasma for 30 seconds, then rinsed in acetone to coarsely remove any residual photoresist, and finally boiled in piranha solution for 10 minutes.

Samples had 5 μm deep trenches with (001) flat bottoms having widths from 5 to 25 μm and lengths of 250 μm. A summary of the fabrication process is illustrated in Figure 99.

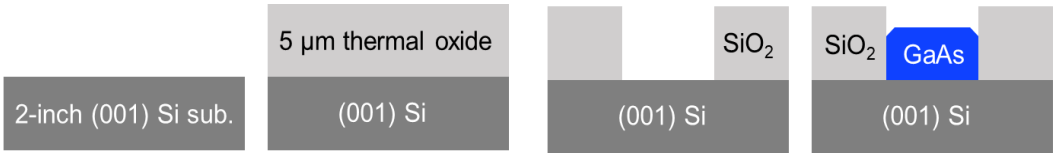

Figure 99. Diagram of the fabrication process of the recess showing the thermal oxidation, ICP etching of the recess, and selective area growth via MOCVD.

4.2.2 Growth via MOCVD

Following the thorough cleaning to remove any residues that could lead to parasitic nucleation during growth, the samples were placed in a 1% dilute HF solution for 1 minute, the rinsed with DI water and blow dried with N_2, before quickly being loaded into the MOCVD reactor.

The growth recipe steps and temperature profile shown in Figure 100. An initial high temperature 815°C step is used for thermal desorption to remove any native oxide that might have formed on the silicon surface in the time between the HF dip and the loading into the chamber. Cooling down to the first growth step is carried out in a group V rich atmosphere, also referred to as an arsenic soak, where surface sites on the silicon are primed with As adatoms and As containing admolecules. The first growth step is a thin low temperature (LT) GaAs nucleation layer grown as low as 355°C. A low pressure of 35 Torr and a high V/III ratio were used to ensure good selectivity for the kinetic-limited growth and effective GaAs nucleation, respectively. The following steps include two intermediate medium temperature (MT) growth at 530°C and a first high

temperature (HT) growth at 580°C, all using TEGa as gallium precursor. A final bulk growth is at a HT step at 640°C and uses TMGa as the group III precursor instead.

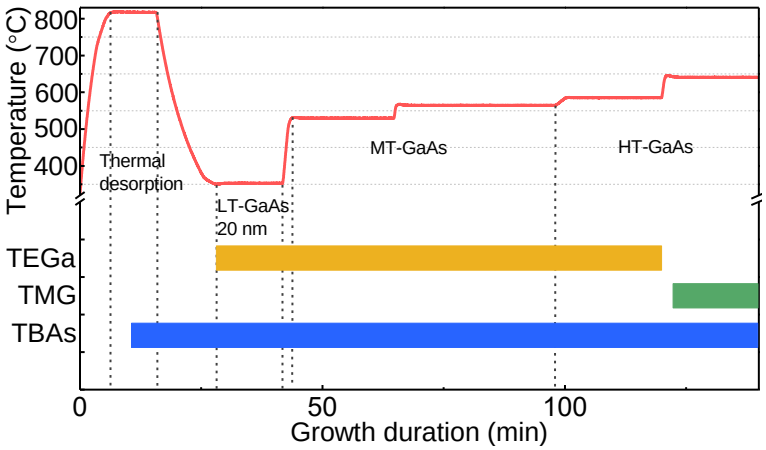

Figure 100. Growth temperature and precursor profile used for the GaAs microridges grown in the silicon recesses.

4.3 Results

Microridges with a flat and smooth surface, selectively grown inside the deep recess, were achieved [75]. The temperature of the initial LT GaAs nucleation layer was critical to this result and had to be optimized, as shown in Figure 101.

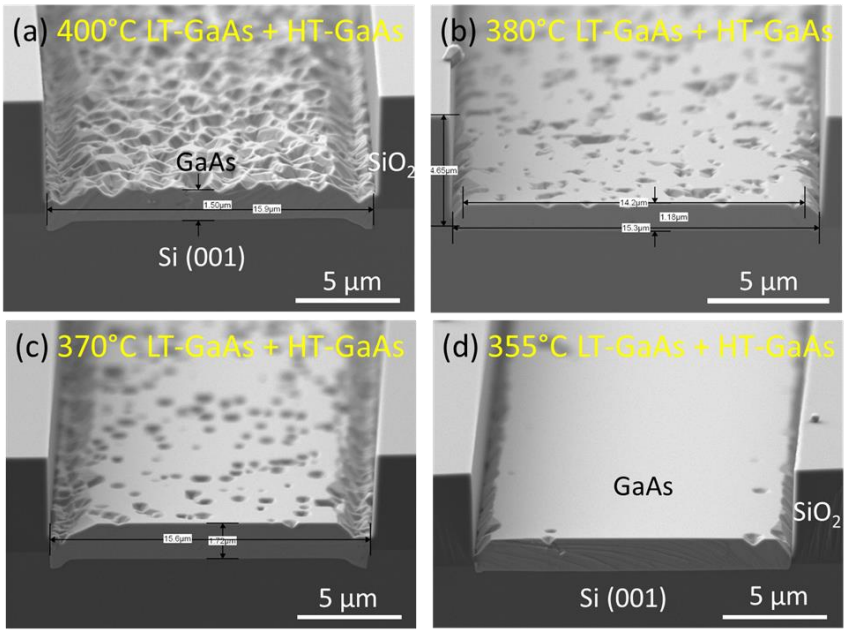

Figure 101. Comparison of different LT GaAs nucleation layers showing the important effect on final surface quality.

The final ridge smoothness was confirmed by AFM measurements showing an RMS roughness of 1.4 nm on a 5 x 5 μm^2 scan area, that also shows an ordered step flow growth. Differential interference contrast (DIC) optical microscope imaging reveals consistency over a large area and suggests absence of clear APB domains on the surface.

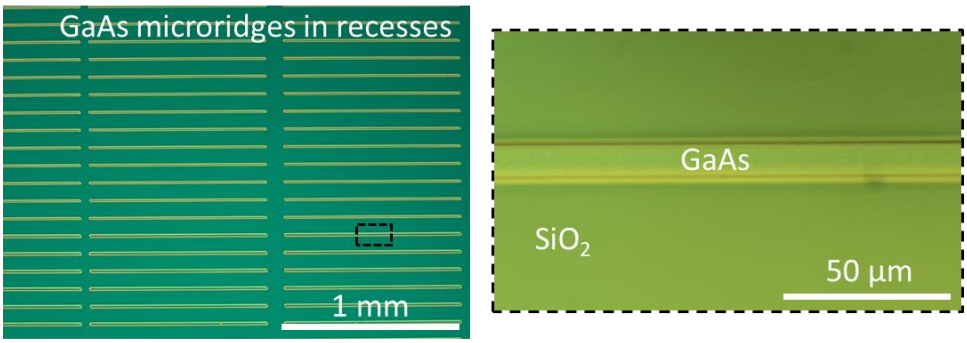

Figure 102. Microscope DIC image of the GaAs microridges.

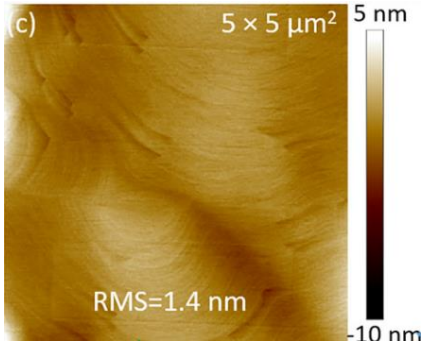

Figure 103. AFM scan taken at the center of a GaAs microridge showing low roughness and step flow growth.

A STEM evaluation and analysis of the cross section of the microridge shown in Figure 104, taken both longitudinally and perpendicularly, show APB formation at the heterointerface. The APB defects though appear to self-annihilate with the progression of growth, and completely disappear after the first 1.7 µm of thickness.

The absence of APBs is primarily attributed to the multi-temperature growth approach with the first low temperature GaAs layer being critical, with APBs formed at the initial heterointerface kinked into higher index planes during the progression of HT growth. Some corrugations at the edges of the microridge (111) facets are visible and are attributed to the local microtrenching due to the ICP dry etch and roughness of the sidewall. A discussion on microtrenching reduction can be found in paragraph 4.4.1. Fortunately, these imperfections are contained at the edge of the structures and do not impact the center of the ridge, which is the important surface for further growth.

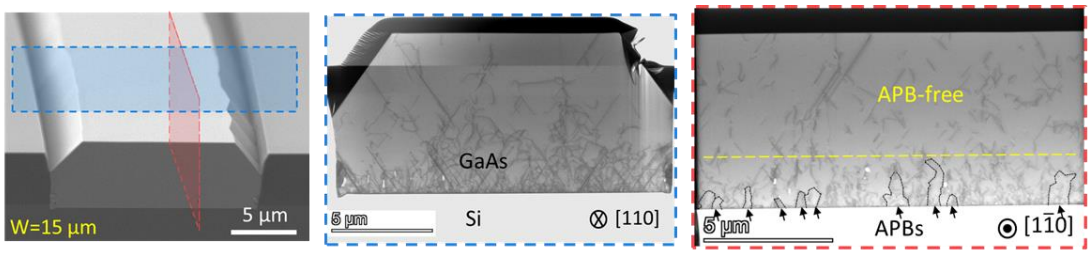

Figure 104. Tilted SEM cross section of the 15 µm wide microridge (left) with highlighted locations of the TEM samples (center and right).

Defect density measured at the surface via ECCI, unlike the TASE samples in Chapter 2, was possible thanks to the large area structures, Kikuchi lines from the substrate were faint but visible, and allowed for alignment to the channeling condition of both {220} and {040}. The threading dislocation density was measured to be 1.3×10^{8} cm^{-2} for a GaAs thickness of 5.6 µm.

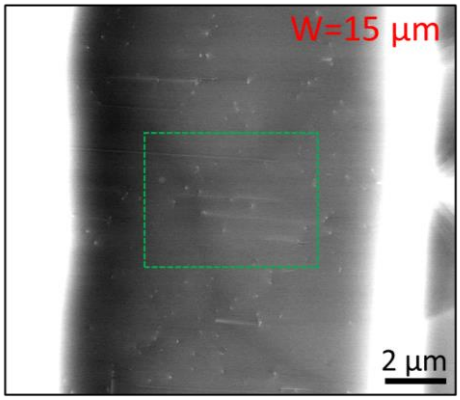

Figure 105. ECCI image of a 15 μm wide ridge of GaAs showing a TDD of $1.3x10^8$ cm^{-2} (extrapolated from the counts in the highlighted area).

While this result was promising in it of itself, there is still the need to further reduce the TDD at the surface, to minimize the impact on the performance of devices grown on top of the pesudosubstrate. Growing thicker buffer layers is an effective method because it does allow for present TDs to statistically self-annihilate. This would come at the expense of longer growth times (and cost) and buffers that would exceed the current trench depth. Other defect filtering methods were then chosen.

Thermal cycle annealing (TCA) was introduced into the growth recipe. Five cycles of temperatures between 735ºC and 355ºC were inserted into the growth stack as shown in Figure 106, followed by multi-stack InGaAs/GaAs strained layer superlattices (SLSs) to filter dislocations[2]. TCA promotes migration of the dislocations bending them and aiding self-annihilation.

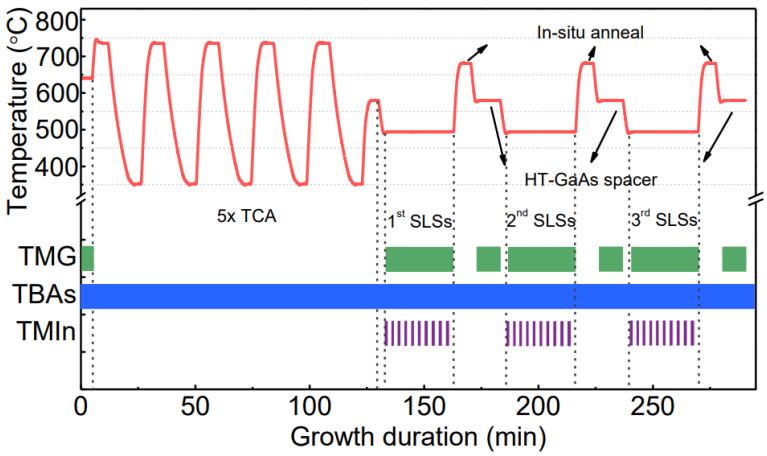

Figure 106. Modified growth temperature and precursor profile for GaAs microridges with the addition of TCA and SLSs for defect engineering. Source: supplementary material of [75]

Likewise, the strain present at the SLSs also bends TDs towards a misfit type dislocation that follows the SL layer sideways, instead of propagating upwards. Different number of SLS stacks were introduced in different samples and effectiveness compared by counting surface defects via ECCI measurements, as seen in Figure 107.

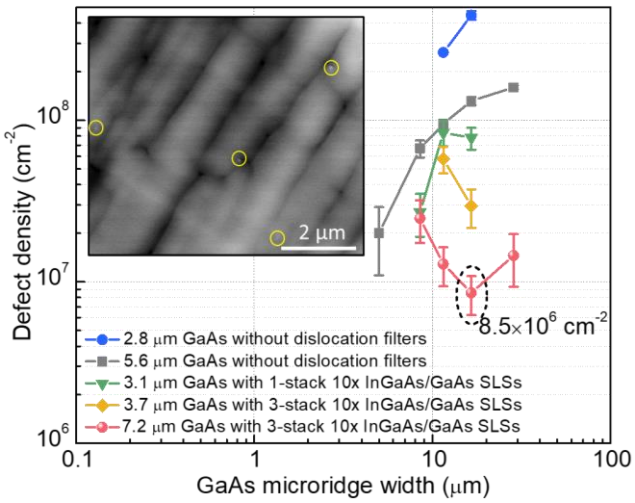

Figure 107. Comparison of different defect engineering efforts on the GaAs microridges, showing number of surface defects measured via ECCI. Inset is a representative ECCI image with TDs highlighted.

With the dislocation filters inserted and the TCA applied, the defect density was lowered to as little as 8.5x10^6 cm^{-2}, with a total thickness of 3.7 μm. No cracks were visible, likely due to the strain alleviation provided by SAG. The best results were achieved for the 15 μm wide trenches. This is not strictly related to the width, but rather to the fact that different trench widths would experience different growth rates due to loading effect inherent to SAG in MOCVD. The developed recipe then simply had the best outcome for that specific trench width, but it should be possible to optimize the recipe for different widths by modifying the growth rates by lowering the group III flows.

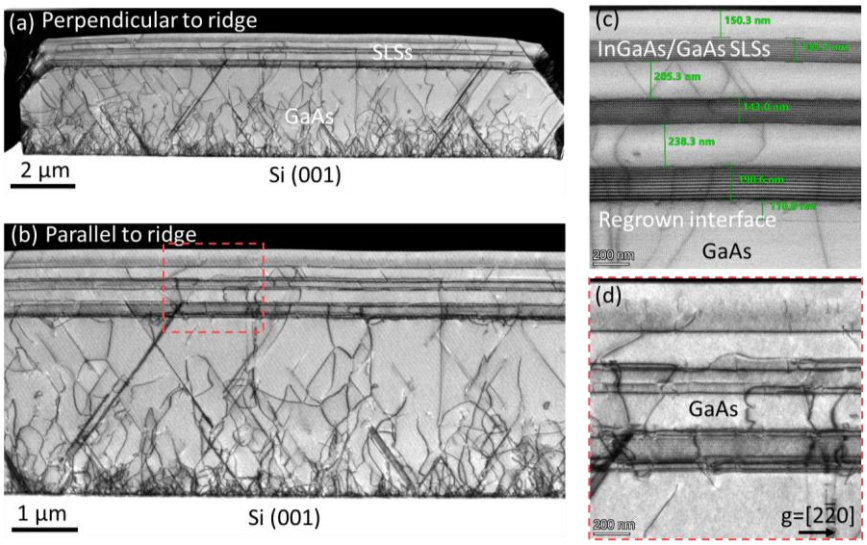

Figure 108. STEM imaging of a cross section of the SLSs grown on the GaAs microridge showing defect filtering. Images are taken a) perpendicular to ridge and b) parallel to it. c) shows the change between the different stacks of SLSs and d) a close up of the defect bending effects.

Observing the TEM cross section of the SLSs we can observe how the dislocations first generate at the initial heterointerface, then reduce in density with the progression of growth. Then they further reduce with every SLS stack they must traverse. Also visible is the bending of dislocations that occurs as soon as the dislocation reaches a strained area near the SLS, propagating laterally instead of vertically.

An EDAX analysis of the SLSs reveal that there is a small composition shift when comparing the various stacks. Specifically, the relative In composition of the layers is reduced with the progression of growth, and so is the thickness. This was attributed to the presence of parasitics present on the sample surface that, by growing larger, capture more and more precursors slowing down the growth

rate down in the recess. Partially this effect can also be attributed to the SAG in a recess itself. The precursors have to diffuse a slightly longer distance when the growth front is nearer to the substrate versus when it is almost near the upper most surface, but we believe this effect is less important considering the overall large size of the trenches, especially when compared to other SAG structures like in Chapters 2 and 3.

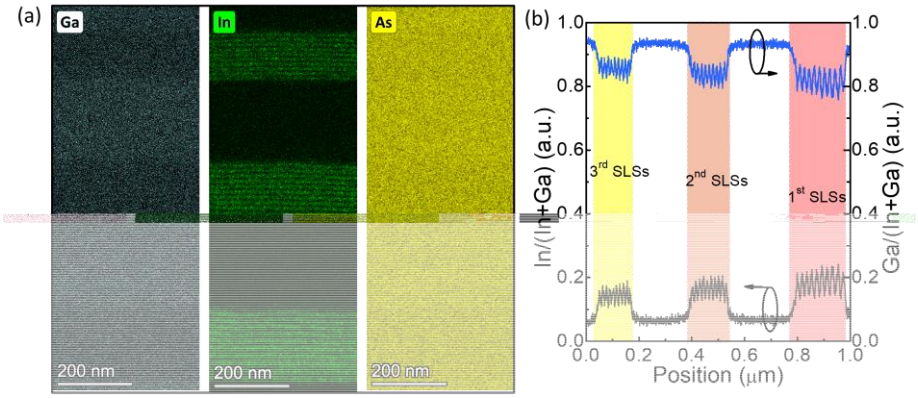

Figure 109. a) EDAX density mapping of In and Ga concentration with As as reference. b) relative counts of In and Ga showing a shift in composition between the SLS stacks. Source: Bei Shi et al., CSW 2021

To further validate the quality of the material beyond characterization, samples with a completed GaAs microridge were loaded into the MOCVD reactor for further regrowth of an active region. After an initial GaAs buffer, a 3x QW InGaAs/GaAs structure was grown. Two samples were prepared, one using a 1.8 μm thick GaAs, the other a 3.4 μm thick. On each growth, sample trenches of 7, 10 and 15 μm were present. After growth PL analysis was done on each size

trench. Results are plotted in Figure 110. When comparing the two initial pseudosubstrate thickness we note how overall intensity increases for the thicker starting substrate, likely due to improved initial material quality. There is a difference in emission peaks between trench widths due to the aforementioned difference in growth rates due to loading effects, leading to a higher InGaAs layer thickness and thus emission of the QW. The recipe for each set of QWs was the same but, for the same loading effect mechanisms, QWs grown at different stages (and hence depths), will have slightly different compositions and stress, leading to some peak broadening.

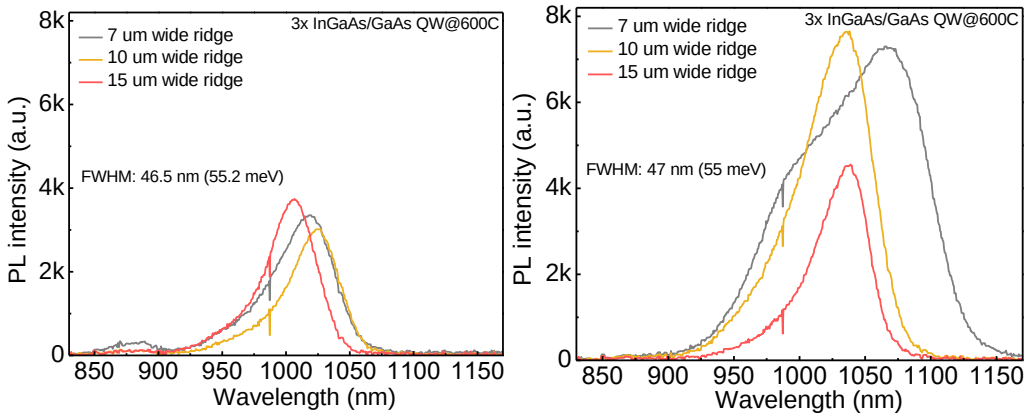

Figure 110. PL of 3xQW InGaAs/GaAs structures grown on 1.8 μm (left) and 3.4 μm (right) thick GaAs microridges.

An additional validation of the viability of the microridge as a pseudosubstrate was done by growing a 1.5-layer quantum dot (QD) region on another 3.4 μm thick GaAs sample. A set of InGaAs QD was grown capped and buried inside the

structure shown in Figure 111, while a second set was grown as the last layer with no capping. This allowed both analyzing the sample via PL by measuring the emission of the buried layer and scanning the surface via AFM to measure the morphology and distribution of the QDs. Room temperature PL showed a relatively narrow peak of QD emission, while AFM imaging showed a high density of QDs with homogeneous distribution. While a more in-depth analysis is not presented here this is nonetheless a promising result to prove the viability of SAG of microridges in a recess as pseudosubstrates for integration with silicon photonics.

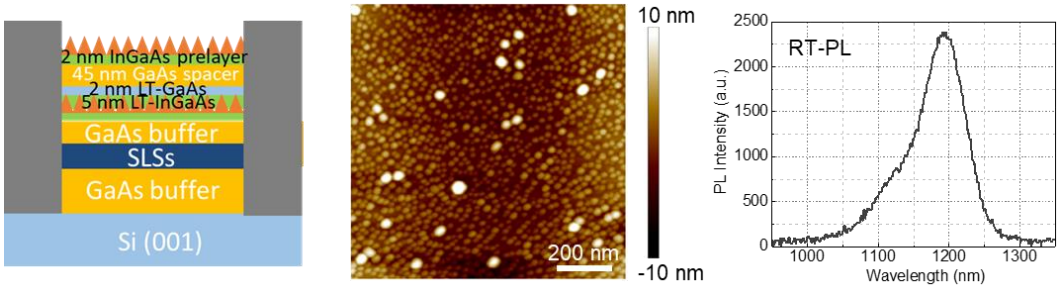

Figure 111. Diagram of QD structure grown in a recess (left), AFM scan of the surface uncapped QDs (center) and PL spectroscopy of the structure (right).

4.4 Future work

4.4.1 Minimizing or removing micro trenching

The ICP-RIE used to create the deep recesses, while showing on average an overall good homogeneity across the wafer or sample, is subjected to localized

loading effects at the mask edge. This led inevitably to some amount of excess etched depth neat the recess edge as visible in Figure 112.

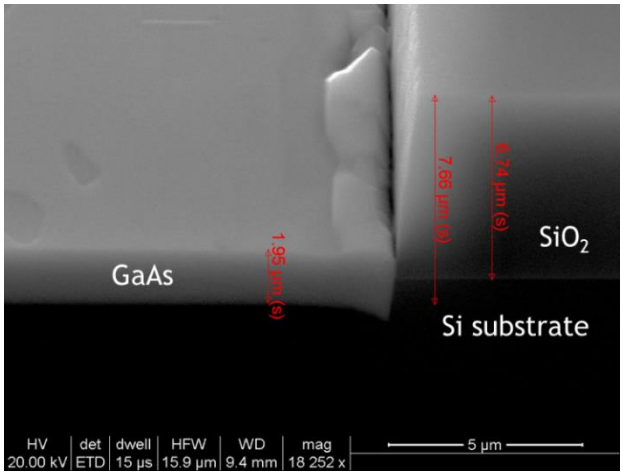

Figure 112. Micro trenching at the trench edge after ICP etch. Also visible is the over etch into the silicon.

It is not entirely clear if this can cause issues to the growth of the micro ridges since good results have been achieved despite the microtrenching. It is worth considering though for future attempts in case even better results are yielded. Microtrenching also depends on the fill factor and mask geometry, so having knowledge on how to reduce this effect is valuable.

Changing the etch chemistry to a fluorocarbon gas mixtures (CF_4/CHF_3 and CF_4/C_4F_8) was shown to reduce microtrenching for both isolated line and grating patterns[76] that, while not exactly the same, have comparable sizes to our recesses. As shown in Figure 113, while microtrenching is reduced with the

addition of C_4F_8 in the gas mixture, there are other effects. The etch selectivity is slightly impacted, but for our purposes this effect can be considered negligible. What also changes is the verticality of the edge, resulting in an increase in the wall slope. This should not affect growth results per se but could impact fabrication of devices and ease of coupling from active regions in the recess to, for example, waveguides buried in the oxide.

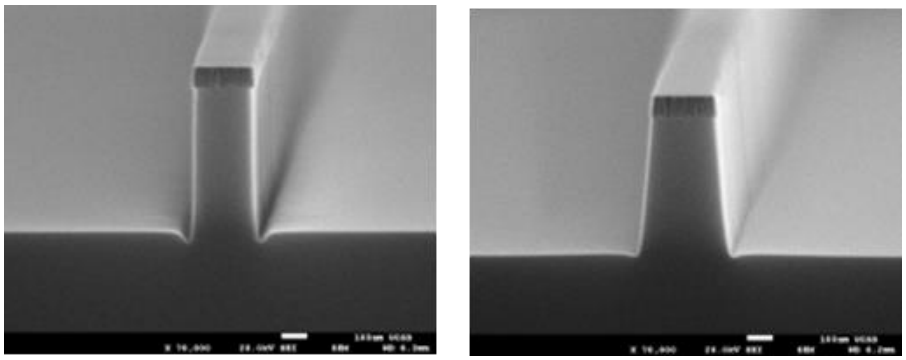

Figure 113. Cross-sectional SEM images of 200 nm wide isolated line subjected to a 600 nm deep ICP etch. Etch chemistry is CF_4/CHF_3 (left) and with added C_4F_8 showing reduced microtrenching (right). Images taken from [76].

4.4.2 Deeper recess in SiO_2 and Si

Deeper recesses than the 5 μm ones described above would be desirable because would simply allow for more space to grow thicker buffer/pseudo substrates and/or to add defect engineering type layers during growth, leading to lower surface final defect density. As said though, thicker thermal oxides require exponentially increasing times to be achieved even at the highest temperatures.

The alternative to this is to etch deep recesses in the silicon itself, while still having an upper thermal oxide layer to align to, for example, buried waveguides and other silicon photonic structures.

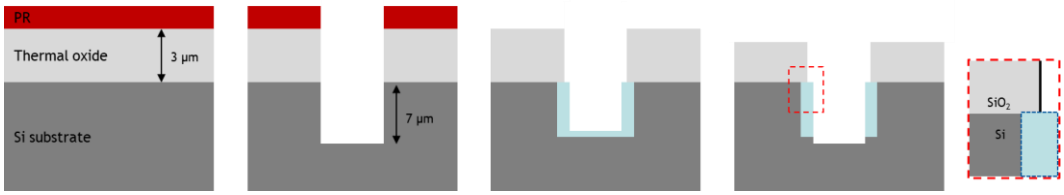

Figure 114. Diagram of the fabrication process for deep silicon recess. The diagram on the right highlights how the thermal oxidation does protect the sidewalls but causes it not to be flat with the presence of a step.

Starting substrates, thermal oxidation and etch of the recess in the oxide is similar as before. This time the thermal oxide was limited to 3 µm, mimicking commonly used thicknesses in silicon photonics.

Once the recess in the oxide was defined a second dry etch, this time selective towards silicon, was carried out in the same SLR Fluorine ICP tool. There was no need for additional lithography since the first trench in the oxide could act as a hard mask, reaching a total recess thickness of 10 µm.

To avoid growth initiation on the now silicon sidewalls of the recess a second thermal oxidation was necessary. A 200 nm oxide was obtained with a 30 min thermal oxidation at 1050°C. The wanted effect is to have the silicon surfaces covered in oxide, but also the unwanted effect of creating a non-flat sidewall,

with a step being present where the second thermal oxidation expanded into the recess itself. This is a potential issue for selectivity during growth with edges, steps, and roughness being preferential parasitic nucleation sites.

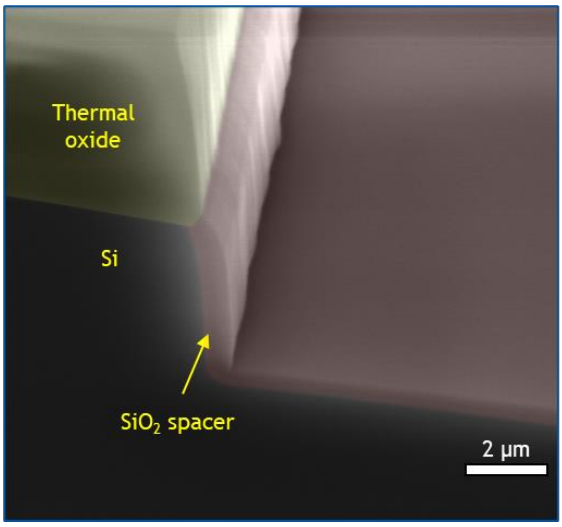

Figure 115. Cross section SEM of a deep recess after the second thermal oxidation that creates the sidewall spacer. False coloring distinguishes between the first and the second thermal oxide. A "step" caused by the spacer can be seen at the Si/oxide height in the sidewall.

Finally, to expose the silicon at the bottom of the trench a final dry etch in the same tool and chemistry as the first was used. This dry etch, being very directional by nature, removes the bottom oxide while mostly preserving the sidewalls. The sidewall itself, having the step created during the thermal oxidation further into the recess, will sustain damage and show signs of shadowing from the mask above, increasing the overall unevenness and roughness, further increasing the risk of parasitics during growth.

To avoid this “step” cause by the second thermal oxidation and achieve a flat sidewall an alternative process was trialed. Just before the second thermal oxidation that creates a spacer, an anisotropic wet etch was introduced to undercut the top oxide. The rationale was to etch back into the silicon trench for the same amount that thermal oxidation would expand the oxide, compensating each other and resulting in a smooth sidewall.

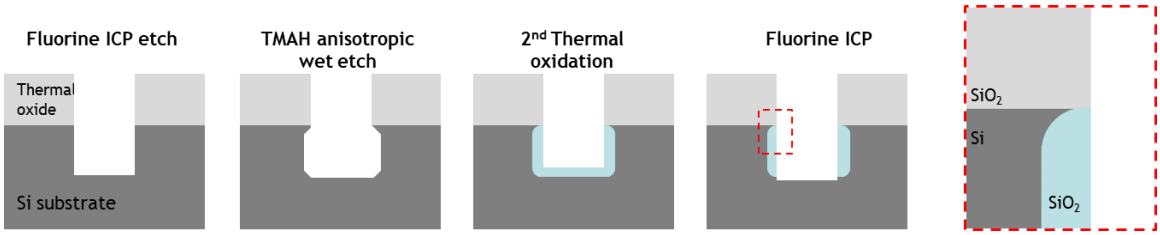

Figure 116. Diagram of the fabrication process of a deep silicon recess with a flat sidewall, where a wet etch undercut and a thermal oxide spacer compensate each other.

A common developer, AZ300MIF (which is a 2.38% solution of TMAH), was used for this undercut etch. From the available data for etch rates at different temperatures and concentrations, a temperature of 60°C was chosen in order to have a relatively low etch and hence a better control of etch depths. We then both estimated and experimentally determined the optimal etch time.

As seen in Figure 117, a 30 seconds etch time followed by a 25 minutes thermal oxidation at 1000°C results in a flat sidewall, after the undercut is compensated by the oxidation. The oxidation time chosen is arbitrary of course,

so compensation could be obtained both ways, but we were targeting 200 nm of oxide.

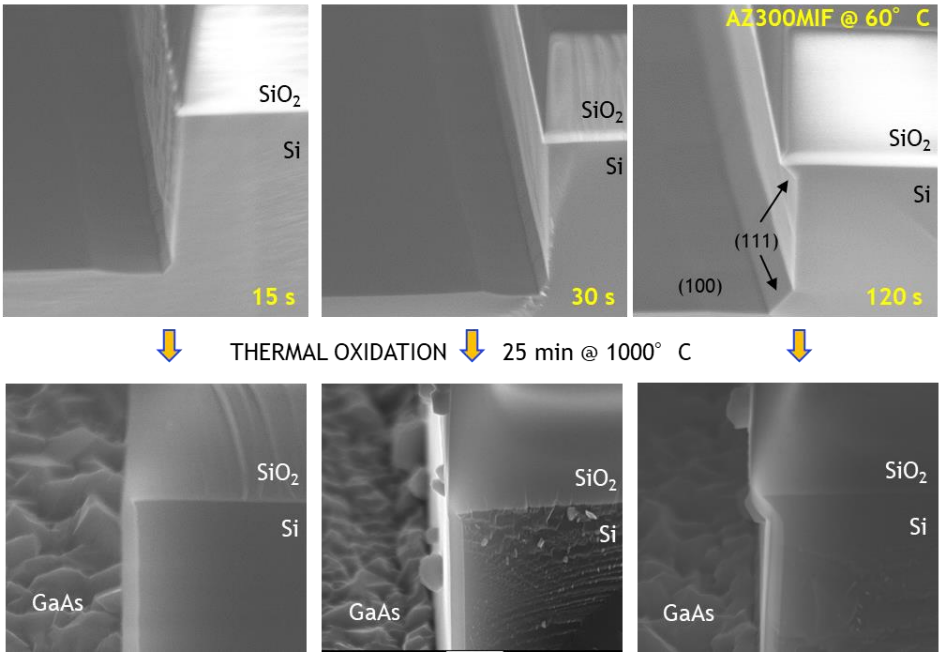

Figure 117. A cross section of the recess sidewall before (top) and after (bottom) the sidewall thermal oxidation for different TMAH etch times. A flat sidewall, with thermal oxidation and etch compensating each other, is seen for a 30 s etch time and 25 min oxidation at 1000°C.

Initial trials using deep recesses with the undercut showed promise. While we did not achieve good quality micro ridges per se (due to the need to redevelop the growth recipes for deeper recesses), we did not observe clear selectivity issues localized at the Si/oxide height as we did in samples without the undercut.

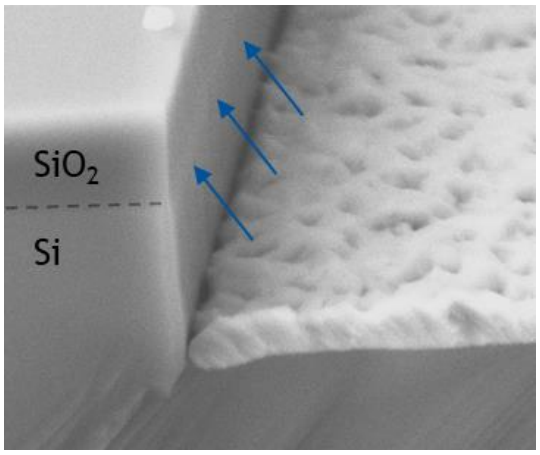

Figure 118. Tilted SEM of a cross section deep recess showing no parasitics on the sidewall. Arrows guide the eye to the Si/SiO^2 interface height.

5 Other works

During my doctorate program I had the opportunity to work on different projects as an MOCVD grower that were not exclusively my own or led by me. I report on a few here below focusing on and describing the challenges related to MOCVD epitaxy that I encountered. In depth discussion of the motivation and results of these projects are beyond the scope of this work and will be better described by the authors of the associated papers that I cite.

5.1 Strained InAs composite channel MOS-HEMT

InP-based transistors are of interest for future high-frequency communication systems [77], [78]. A figure of merit for these devices is f_t, important for future low noise, millimeter-wave communication systems[79], and current state-of-the-art InP based HEMTs exhibit up 610 GHz f_t [77] and 703 GHz ft [80].

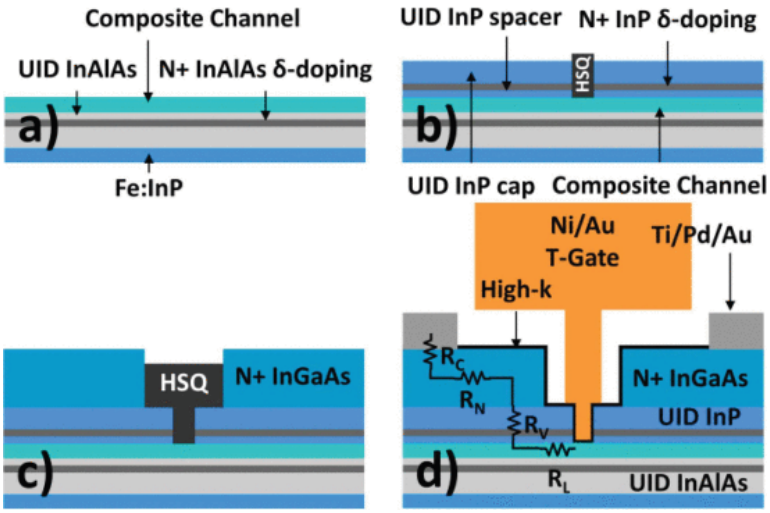

Figure 119. From [81]. Schematic of the RF-MOSFET process flow: a) Buffer and channel epitaxy b) Dummy gate and modulation doped access region regrowth c) Second dummy gate and N+ source/drain contacts d) High-K deposition, T-gate metallization, and source/drain metallization.

A MOS-HEMT based on a InGaAs/InAs/InGaAs composite channel design with a record f_T=511 GHz was demonstrated[81]. The design of the epitaxial stack also included an InAlAs back barrier with modulation doping, either and InAlAs or a InP link region also with modulation doping, and n+ InGaAs source-drain contacts. While different iterations of the structure have been tested a representative stack for the channel epi is shown in Table 4 and for the link region in Table 5. The source-drain contacts were a single layer of highly doped InGaAs, sometimes grown with an additional InP cap of a few nanometers.

S200128B channel epi	*thickness (nm)*	*doping*	*Rg (nm/s)*	*Temperature (°C)*	*time (s)*
InGaAs	7		0.39	490	18
InAs	4		0.18	490	22
InGaAs	3		0.71	600	4
InAlAs	3		0.196	600	15
InAlAs	3	n++	0.1225	600	24
InAlAs	50		0.459	600	109
InP buff	3		0.366	600	8
InP substrate					

Table 4. Representative epitaxial stack for the composite channel epi that includes the InAlAs back barrier with modulation doping.

S200203A link	*thickness (nm)*	*doping*	*Rg (nm/s)*	*Temperature (°C)*	*time (s)*
InGaAs	2		0.71	600	3
InAlAs	15		0.196	600	77
InAlAs	3	n++	0.1225	600	25
InAlAs	3		0.196	600	15
Channel epi					

Table 5. Representative InAlAs link region epitaxial stack with modulation doping.

Results published in [81] have been achieved with the initial channel epitaxy shown in Figure 119a purchased from a supplier, but the same structure has also been grown in-house for other samples.

Regardless of the initial channel epi used the fabrication of the MOS-HEMT requires two subsequent regrowths for the link region with modulation doping and finally the n+ InGaAs source-drain contacts.

Sample preparation after patterning required one cycle of digital etching in HCl:H_2O 1:10 immediately before loading into the MOCVD chamber. The link region was grown at 600°C, consisting in 3 nm UID-InP spacer, 2 nm Si:InP modulation doping, 15 nm UID-InP cap. Hall measurements were performed on simultaneously processed samples without dummy gates and yielded electron sheet carrier mobility of 11,000 cm2/Vs. The high mobility, while not as high as other literature results of similar structures [82] still suggests that there is no strain relaxation in the InAs layer. After a second dummy gate necessary for the semi self-aligned process a single digital etch was again performed immediately prior to re-loading into the MOCVD chamber and growing 60 nm N+ $In_{0.53}G_{a0.47}As$ (target $4\times10^{19}\,cm^{-3}$) source-drain regions.

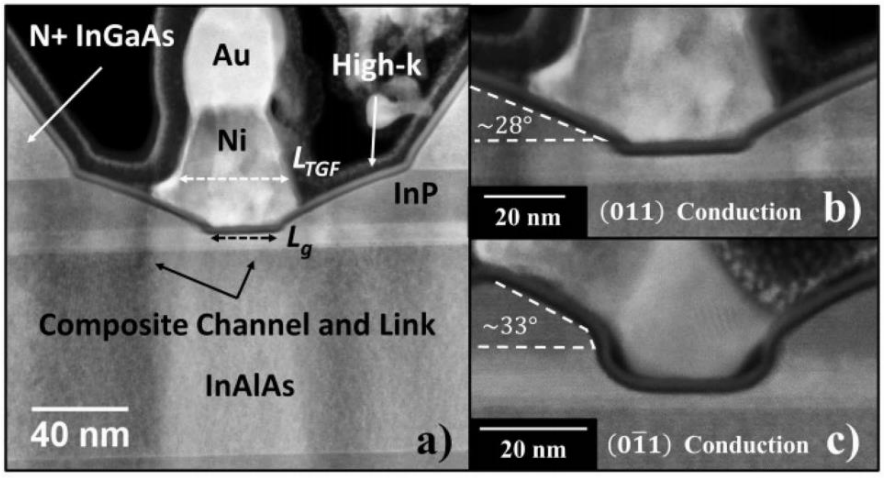

Figure 120. Cross section TEM image of a MOS-HEMT with the InGaAs/InAs/InGaAs composite channel. Image taken from [81]. Visible and asymmetrical faceting can be observed at either side of the Ni gate

5.1.1 Strained InAs

The main challenge related to the composite channel design is the large lattice mismatch that exists between the In0.53Ga0.47As and the InAs, causing the latter to be highly strained and incurring the risk of relaxation. In fact, the nominal Matthew Blakeslee critical thickness for that layer is 2 nm (or 4 nm with an infinite capping layer). The MB critical thickness is a theoretical conservative minimum so real-world layers that surpass that limit with no relaxation are possible. In the literature XRD investigations of growth temperature effects on strain relaxation of comparable composite channel structures show how an upper limit exists after which relaxation occurs. This is shown by growing a series of

identical epi stacks at different temperatures and taking an omega-2theta scan of each sample. A clear envelope with an identifiable peak is observable where the pseudomorphic InAs layer stands, left of the InP substrate peak (see Figure 121). This peak suddenly shifts towards the substrate after a temperature threshold is reached.

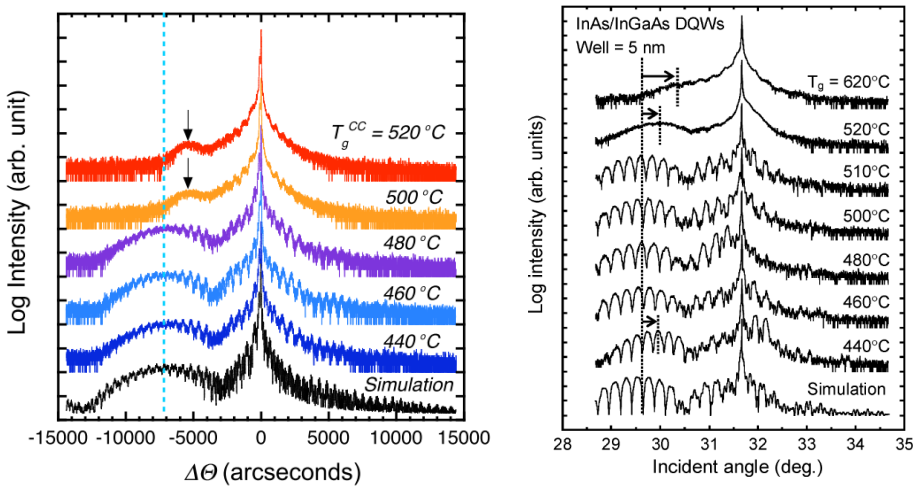

Figure 121. The XRD investigation of growth temperature on the strained InAs in a InGaAs/InAs/InGaAs composite channel for a 3nm layer from [82] (left) and a 5 nm layer from [83] (right). Strain relaxation of the InAs layer at higher temperatures is indicated by an arrow.

In our trials, to verify that the InAs didn't incur in strain relaxation we grew separate samples with identical growth parameters that included both the channel epi and the link region in a single step growth. The samples as grown were cleaved into squares and probed with a four-point contact Hall setup to measure electron mobility. Fully relaxed samples would result in very low

mobility (~10^3 cm^2/Vs) while successfully strained layer would result in high values (>8000 cm^2/Vs). We successfully achieved up to 6 nm thick InAs strained layers exhibiting 9200 cm^2/Vs mobility.

5.1.2 Intermixing in the composite channel

An additional challenged posed by the structure is achieving an abrupt transition between heteroepitaxial layers. As already noted in paragraph 2.1.3 transitioning from arsenic containing layers to phosphor containing ones is not the same as doing the opposite. It is more likely that the resulting interface is less abrupt when growing As->P, with TEM cross section analyses showing a blurred interface. Flowing no precursors for 1 s (approximate gas residence time in our reactor) before switching layers is a way to minimize the group V intermixing. Slow growth rates overall, or temporarily slowing the growth rate just before the interface by reducing group III flows, should also help.

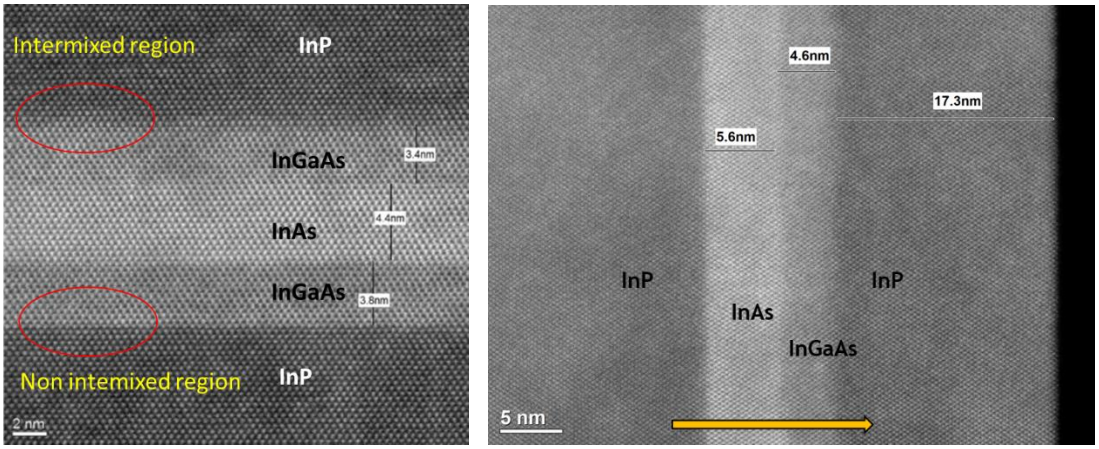

Figure 122. Example of As/P intermixing in a HAADF STEM image. A non-abrupt change in contrast suggests intermixing between the As and P based materials. The arrow indicates the direction of growth.

5.1.3 Modulation doping / Delta doping

The InAlAs link region design required a highly doped delta doped layer. A series of InAlAs test structures were grown having 100 nm of Si-doped InAlAs on semi insulating InP substrates. Thickness of the layer was enough to allow for XRD analysis to check for lattice matching to InP. Different growth parameters were changed aiming at maximizing the doping concentration in the InAlAs layers. Dopant concentration was measured with four-point Hall measurements to make sure the concentration values found were the activated Si and avoided possible instances of Si aggregates and inclusions that would not be discerned in a SIMS measurement. While a systematic study was not possible due to time constraints, doping concentration in the grown samples was eventually increased all the way

to $7x10^{18}$ cm^{-3}. Critical changes were increasing the dopant flow itself of course, lowering the growth rate (by lowering the In precursor flow), increasing the V/III ratio, and maximizing the growth temperature (in our case limited by possible strain relaxation of the composite channel). Best results were achieved at a 110 V/III ratio, $3.75x10^{-06}$ mol/min of TMIn, $2.52x10^{-06}$ mol/min of TMAl, 600°C growth temperature, and 350 torr growth pressure.

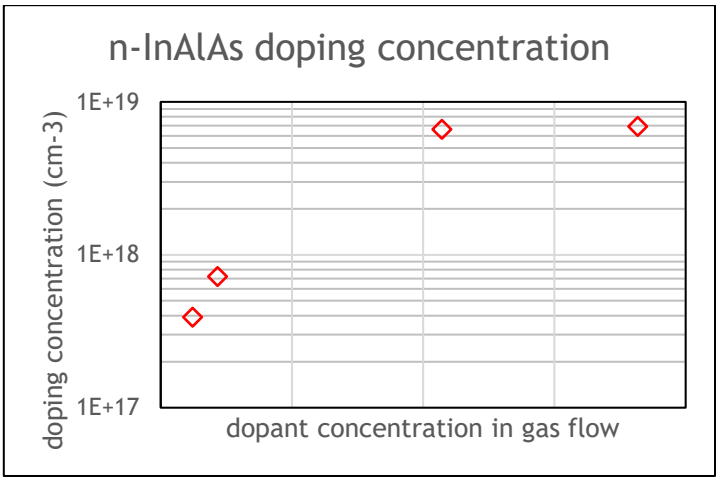

Figure 123. Plot of doping concentration results of trials of n-InAlAs.

6 References

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