UNIVERSITY OF CALIFORNIA,
IRVINE

# Design and Implementation of Configurable Short-circuited SIW Coax Filter and Sideband Suppression Methods

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

by

Shang-Yu (Gary) Hung

Dissertation Committee:
Professor G.P. Li, Chair
Professor Chen Tsai
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# DEDICATION

*To*

*my parents, family, and friends*

*in recognition of your support*

*and unconditional love*

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Hung, S., Guo, Y.: 'Design and modelling of tunable band-stop filter using evanescent mode resonators', *Progress in Electromagnetics Research Symposium*, Toyama, Japan, Aug. 2018, pp. 424-427.

Hung, S., Guo, Y., Li, G. P.,: 'Fully reconfigurable evanescent mode bandpass filter embedded with metallic grid', *Progress in Electromagnetics Research Symposium*, St Petersburg, Russia, pp. 2489-2494, May 22-25, 2017

Hung, S., Guo, Y., Li, G. P., *et al.*: 'Transfer function reconfigurable bandpass filter embedded with metallic grid', *IEEE Electronic Components and Technology Conference*, Orlando, FL, USA, May 2017, pp. 1449-1454.

# ABSTRACT OF THE DISSERTATION

Design and Implementation of Configurable Short-circuited SIW Coax Filter and Sideband Suppression Methods

By

Shang-Yu Hung

Doctor of Philosophy in Electrical Engineering

University of California, Irvine, 2020

Professor G.P. Li, Chair

[According to the literatures and our previous publication, recent researches on bandpass filter design often puts emphasis on configurable center frequency ($f_C$), controllable bandwidth, and multiple moveable notches. However, such designs are frequently inflicted by unwanted stopband transmissions. When such a transmission is too close to the center frequency, it will impact the receiver performance. Especially for the modern receiving modules, unwanted transmission may cause de-sense in other bands. Proposed novel substrate integrated waveguide (SIW) short-circuited coax (SCC) filter demonstrates a passband that has transmission zeros on both the upper and the lower stopbands; therefore, rejections near the passband are greatly improved. Such a filter is inherent with good out-of-band rejection up to three times of the $f_C$. In the design, there are four signal paths from the input port to the output port. The signal routings are done by the slotlines on the top metal layer. Two sets of surface-mount capacitors on the bottom metal layer are used to configure the passband, one set is frequency control capacitors ($C_{Freq}$) while another set is enhance coupling capacitors ($C_E$). The center frequency of the

passband can be determined by $C_{Freq}$, and the transmission zero on the lower-end can be tuned by $C_E$. The phase delay of the signal routings are investigated individually as a way to explain the generation of the transmission zeros around the passband.

To minimize the discrepancy between the ideal simulation and the realization, the structure of the simulated filter from ANSYS High Frequency Structure Simulator (HFSS) can be exported as a touchstone file. Such a file can be later connected to the capacitors' two-port touchstone files provided by the vendor in the Advanced Design System (ADS) circuit simulator. Thereby, simulation results including all the parasitic components from the capacitor can be emulated the real-world measurements.

Due to the fact that the parasitic inductance of the capacitor can trigger resonance above the passband, and degrade the stopband rejection significantly. Multiple parallel capacitors are used to replace the single standalone capacitor in each capacitive loading, such that the equivalent parasitic resistance and the parasitic inductance are further reduced. As a result, inband loss as well as stopband spurs can be minimized. The result of proposed filter design demonstrates a targeted passband centered at 4.84 GHz, with better than 30-dB rejection up to $3f_c$, and has insertion loss of 2.11 dB and the 3-dB bandwidth of 0.46 GHz.]

# INTRODUCTION

With the rapid evolution of mobile communication, the need for a smaller footprint yet higher performance radio frequency (RF) component is urgent. The preselect filter that attenuates out-of-band signals is one of the key components in the RF front-end module. Particularly In the wake of the rapid evolution of mobile communications, the need for a smaller footprint yet higher performance radiofrequency (RF) filter has never ceased. Substrate integrated waveguide (SIW) filter has been extensively studied in recent years [1–13], and such a filter can provide alternative filtering solution due to its reasonable unloaded $Q$-factor ($Q_u$) and insertion loss (IL). Such a filter incorporates SIW vias to PCB substrate as a way to form outer metallic sidewalls as well as center conductors; thus, the fabrication cost of the proposed filter based on the standard single-layer laminated PCB process is low, and such filters can be easily integrated with other planar structures such as microstrip or coplanar waveguide (CPW) [14, 15].

In order to access vacant spectrum resources, future RF modules will be more intelligent [16]. Consequently, the filter needs to have a reconfigurable center frequency; meanwhile, a filter with a flexible bandwidth is also highly desirable, because maintaining a consistent bandwidth throughout the reconfiguring of the center frequency of the passband is crucial given that baseband bandwidth is often designated to a specific value [17, 18]. On the other hand, while carrier frequency is moving to higher spectrums, it is expected that more filters will be added to a given RF module with respect to the increased number of bands. Thus, by deploying fully configurable filters in the front-end, the number of filters used can be potentially reduced [19]. Meanwhile, due to the spectrum being crowded at lower bands, it will be more critical for the filter to have a prescribed transmission zero (TZ) especially at the lower side of the spectrum as to suppress unwanted signals [20]–[23].

Therefore, in recent researches, the reports of bandpass filter design with multiple transmission zeros (TZ) on two sides of the passband are increasing. As the TZs move closer to the passbands, the passband roll-off can be greatly improved. While there are several techniques to introduce TZs to the transfer function, such as deploying none-resonate nodes (NRN) [24], mixed electric-magnetic couplings [25], cross couplings [26]-[27], and bandpass-bandstop cascade [28]-[32], many designs that claim to have multiple TZs also suffer dwindled spurious-free range [33]-[36], such as twice the center frequency ($f_c$) or less. In those designs, usually unwanted transmission near the passband can be observed. In contrast, in the proposed design, we demonstrate a dual-mode compact short-circuited coax (SCC) filter which has targeted center frequency at 4.84 GHz with out-of-band rejection better than 30 dB up to $3f_c$. Such a filter also has predefined notches on two sides of the passband. However, spurious-free range are limited with designs that use SCC resonator, given that the higher resonance modes introduce spurious transmission at higher spectrum. Thus compared with our previous design that used direct coupling scheme, in this paper, a novel side-coupling scheme is devised to reduce the level of unwanted spurs at higher frequencies. In addition, given that the surface mount technology (SMT) capacitors are none ideal but lossy, real capacitors’ s2p files are later used to predict the performance of the filter, such that the in-band loss as well as the stopband rejection can be accurately characterized. Moreover, using multiple SMT capacitors in parallel to replace single standalone capacitor to better off quality factor and minimize parasitic inductance such that improve insertion loss and out-of-band rejection is also investigated.

## SECTION 1: Resonator Design and Simulation

### *1.1 Resonator Prototype*

First and the foremost, all the design info and detailed can be found in [9]. Shown in Fig. 1. (a) is the resonator's layout in HFSS. Such a resonator comprises of one lumped capacitor and one main metal post surrounded by SIW vias. These metallic SIW vias serve as sidewalls to confine energy and create an inductive phase shift to the reflected wave, thus resonance occurs when such a phase shift matches with the phase of the wave inside the resonator [13]. The resonator is weakly coupled with a coplanar waveguide (CPW) feed line; thus $Q_u$ can be accurately extracted by using formulas (1), (2), and (3).

$$Q_{\text{loaded}} = \frac{f_0}{\Delta f} \tag{1}$$

$$Q_{\text{external}} = Q_{\text{loaded}} \cdot 10^{-[S_{21}(\text{dB})/20]} \tag{2}$$

$$\frac{1}{Q_u} = \frac{1}{Q_{\text{loaded}}} - \frac{1}{Q_{\text{external}}} \tag{3}$$

where Δf is the 3-dB bandwidth, and $f_0$ is the resonant frequency and can be represented by (4).

$$f_0 = \frac{1}{2\pi} \frac{1}{\sqrt{(L_{\text{resonator}})(C_{\text{resonator}})}} \tag{4}$$

where $L_{resonator}$ is the equivalent inductance, and $C_{resonator}$ is the equivalent capacitance can be further expressed as (5).

$$C_{\text{resonator}} = C_{\text{lumped}} + C_g \tag{5}$$

where $C_{lumped}$ is the lumped capacitor placed on the top metal of the resonator, and $C_g$ is the capacitance contributed by the annular gap [10], and can be calculated from (6).

$$C_g = \frac{2\pi r \varepsilon_0 (1+\varepsilon_r)}{ln(1+\frac{s}{r})} \int_0^{\infty} [J_0(\zeta r) - J_0(\zeta(r+s))] \frac{J_1(\zeta r)}{\zeta} d\zeta \tag{6}$$

where *s* is the air gap of the ring, *r* is the disk radius, and $J_n$ is the nth order Bessel function of the first kind. In the resonator, *r* and *s* are 320 um and 200 um accordingly.

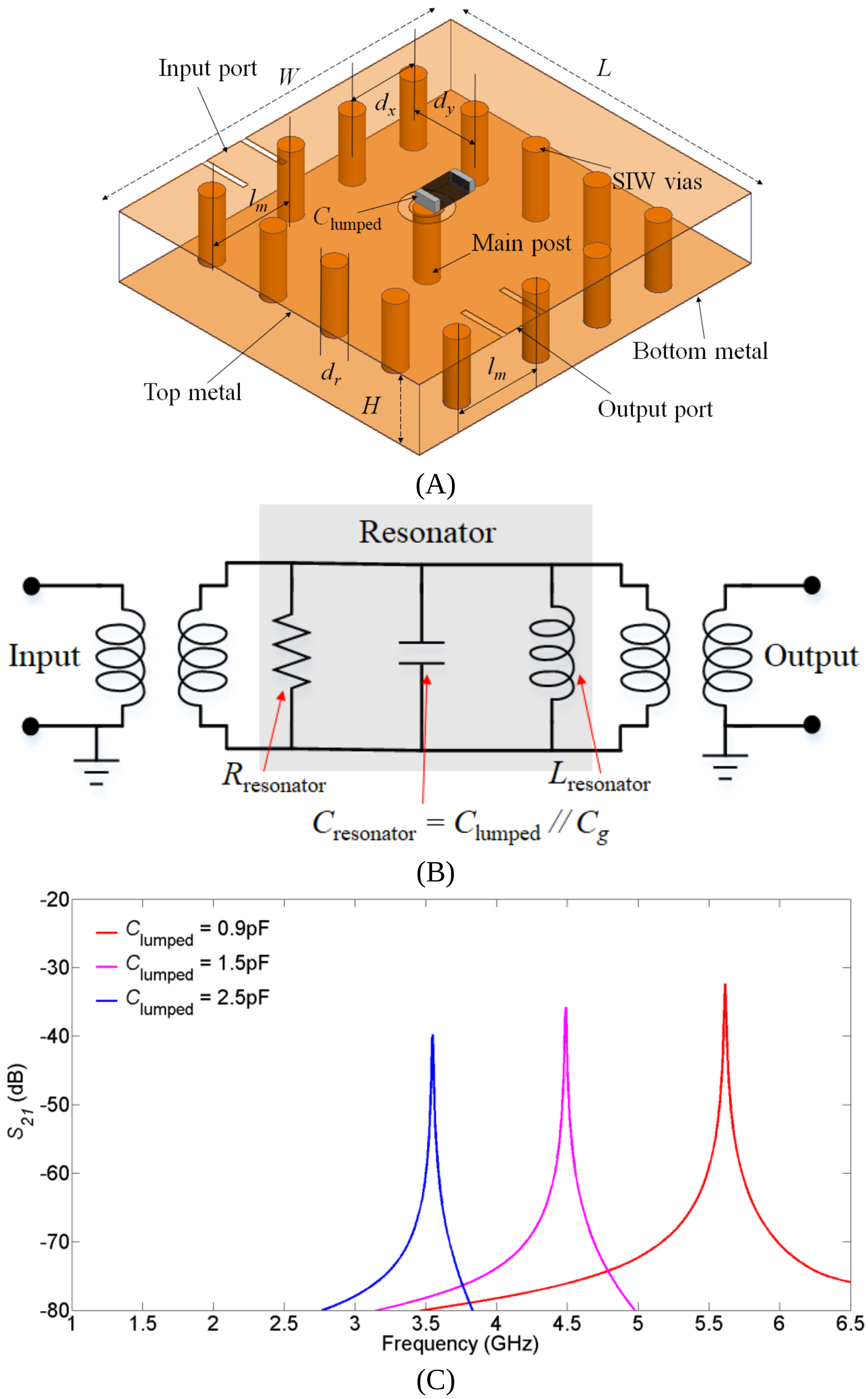



**Fig. 1.** Resonator prototype **(a)** schematic, **(b)** parallel *RLC* circuit model, **(c)** simulated frequency response versus $C_{lumped}$ from full-wave model

At resonant frequency, $L_{resonator}$ is determined by using magnetic energy along with Ampere circuital laws in HFSS field calculator. The peak magnetic power $W_m$ can be computed by formula (7).

$$W_m = \frac{1}{2}\mu_0 \int |H|^2\, dv \qquad (7)$$

where $H$ is the magnetic intensity, and v is the volume of the substrate. With 1 watt of excitation and weak external couplings, calculated Wm is 0.63 nJ at resonant frequency.

Table 1 Dimensions of Prototype Resonator

| Parameters | $W$ | $L$ | $H$ | $l_m$ | $d_x$ | $d_y$ | $d_r$ |
|---|---|---|---|---|---|---|---|
| mm | 8.4 | 7.6 | 1.524 | 2.0 | 1.55 | 1.55 | 0.5 |

In order to calculate current I travels through the main post, one needs to apply Ampere circuital law (8).

$$I = \oint H \cdot dl \qquad (8)$$

where $l$ is the length of the path, and such a path can be defined as a none-model virtual path in the simulator. This current travels to the bottom metal and flows back through the SIW vias such that a loop is formed. The computed magnitude of the maximum current that flows through the conductor is 1.34 A. After both $I$ and $W_m$ are acquired, $L_{\text{resonator}}$ can be obtained by (9).

$$L_{\text{resonator}} = \frac{W_m}{I^2} \qquad (9)$$

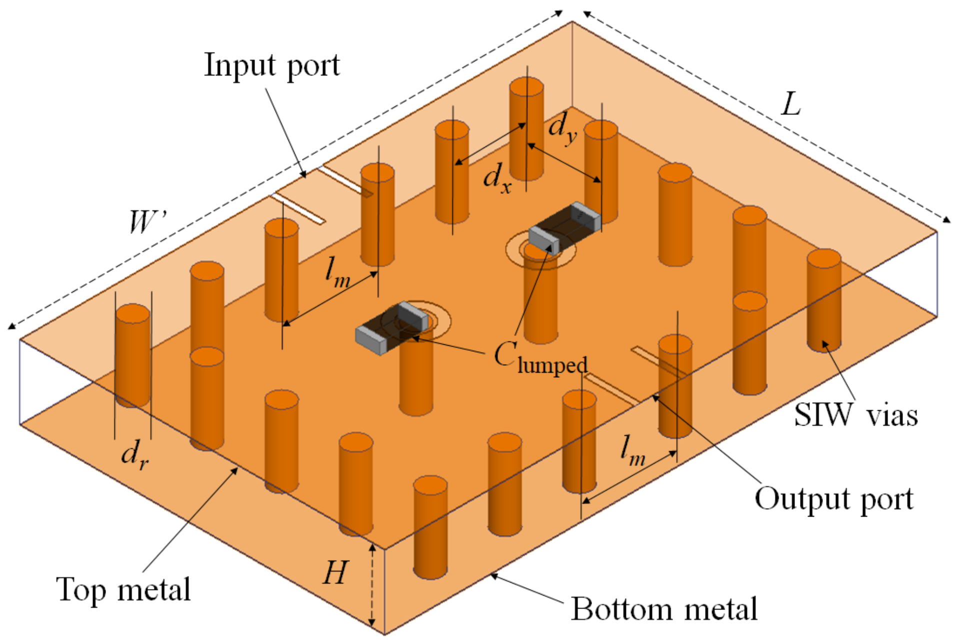
Extracted numerical values of $C_g$ and $L_{\text{resonator}}$ are 0.053 pF and 0.71 nH respectively. When $C_{\text{lumped}}$ = 1.30 pF is applied, $C_{\text{resonator}}$ becomes 1.353 pF; thus, using (4), the calculated $f_0$ is 5.12 GHz. Compared to the simulated result (4.80 GHz), a slight discrepancy is shown partly because surface inductance is not included in the analytical calculation [9], and partly because the analytically calculated $C_g$ from (6) is actually less than a physical $C_g$ given that the metal thickness is neglected. To simulate the loss of the resonator, parallel $R_{\text{resonator}}$ is then included in the resonator, and such a resistor is proportional to $Q_u$. With the ideal capacitor used in the simulation, $R_{\text{resonator}}$ is high; Fig. 1. (d) shows $f_0$ decreases with respect to an increase of the $C_{\text{lumped}}$. $Q_u$, $Q_{\text{loaded}}$, and $Q_{\text{external}}$ from the prototype are extracted as 512, 503, and 29833 respectively ($\Delta f$ = 8.9 MHz, and $S_{21}$ = -35.45 dB at 4.4825 GHz). Although the thicker the substrate the better the $Q_u$, 1.524 mm substrate is chosen mainly because of its compatibility to the 62 mil SMA end launch. Table 1 shows the dimensions of such a resonator. Rogers RO4350 is selected for the substrate material due to its low loss tangent property.

*1.2 Extended Resonator Prototype*

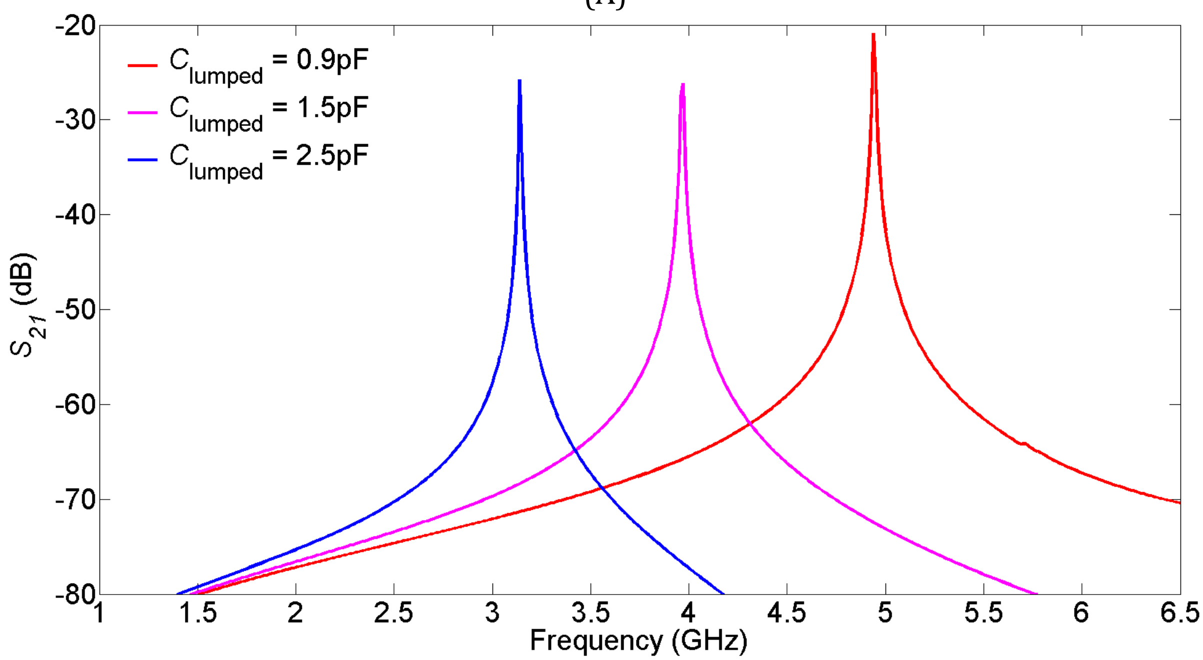
In addition to the prototyped resonator, an extended version is developed and shown in Fig. 2. Such a resonator contains identical upper half and lower half resonators that are separated by the same CPW feed line in the middle. Since $C_{lumped}$ from the upper half and lower half resonators are the same, only one resonance peak is shown. However it is possible to use different $C_{lumped}$ to create dual resonance modes [5]. Nevertheless, throughout the paper, only designs that use the same capacitor for the upper and lower half resonators are of interest. By weakly coupling the resonator, extracted $L_{resonator}$ is 0.45 nH. When $C_{lumped}$ = 1.30 pF ($C_{resonator} = C_{lumped} + C_{lumped} + C_g + C_g$, = 2.71 pF), calculated $f_0$ is 4.56 GHz and 7.5% higher than simulated $f_0$ (4.24 GHz) due to the surface inductance from the metal being omitted as well as the smaller analytically calculated $C_g$. Table 2 shows the dimensions of the resonator, and extracted $Q_u$, $Q_{loaded}$, and $Q_{external}$ are 535, 491, and 5969 respectively (Δf = 9.1 MHz, and S21 = -21.70 dB at 4.4710 GHz).

Table 2 Dimension of Extended Resonator

| Parameters | $W'$ | $L$ | $H$ | $l_m$ | $d_x$ | $d_y$ | $d_r$ |
|---|---|---|---|---|---|---|---|
| mm | 11.5 | 7.6 | 1.524 | 2.0 | 1.55 | 1.55 | 0.5 |

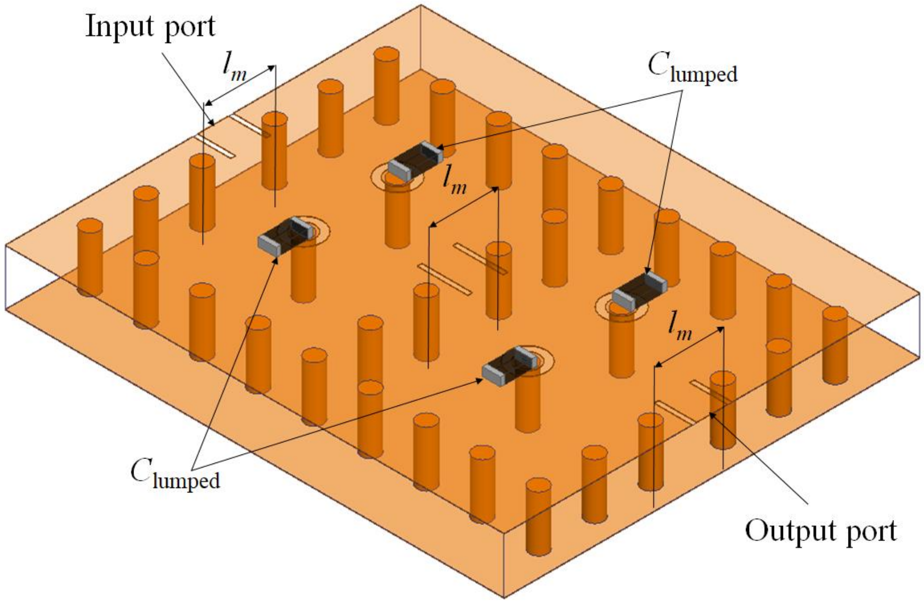



(A)

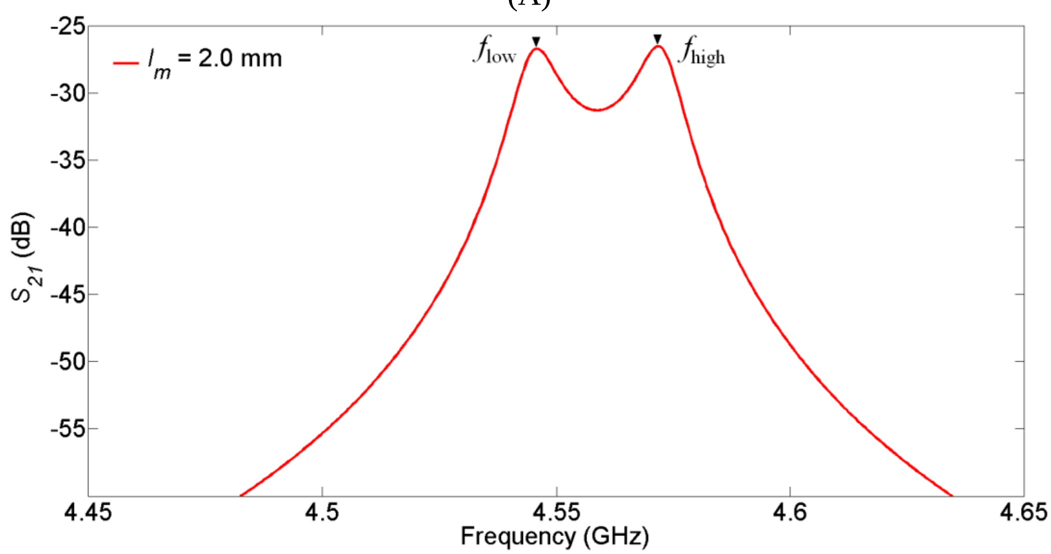



(B)

**Fig. 2.** Extended resonator **(A)** schematic, **(B)** simulated $S_{21}$ versus ideal $C_{lumped}$




(A)

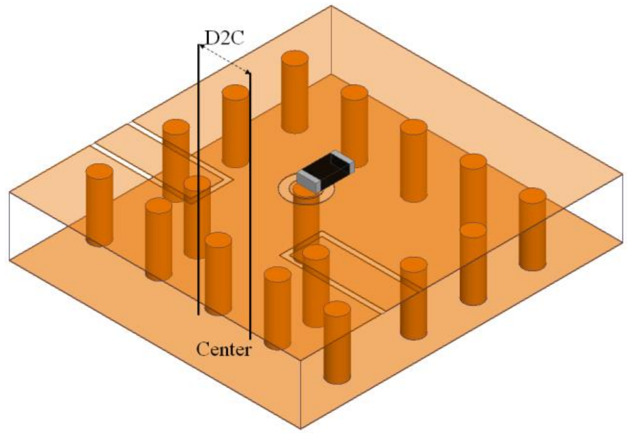



(B)

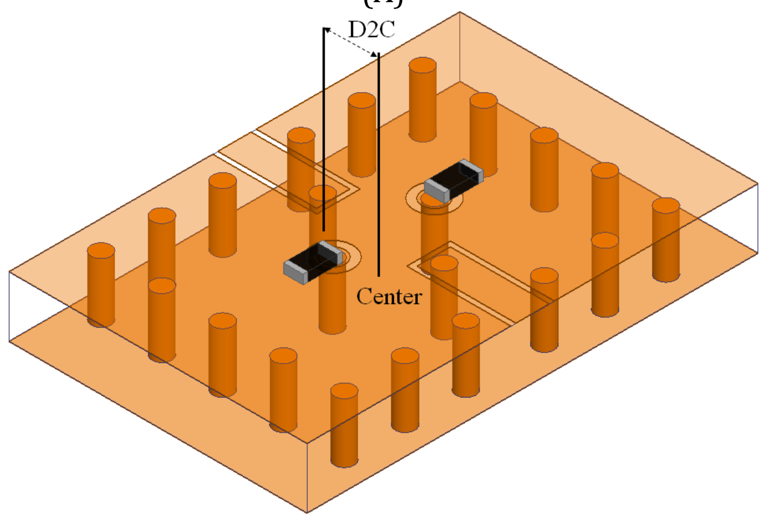
**Fig. 3.** Cascaded resonator **(A)** schematic, **(B)** simulated $S_{21}$ with ideal lumped capacitors

Table 3 Coupling Coefficients $k$ versus $l_m$

| $l_m$ (mm) | 2 | 2.2 | 2.4 | 2.6 | 2.8 |
|---|---|---|---|---|---|
| $k$ (%) | 0.56 | 0.72 | 0.86 | 1.1 | 1.3 |




(A)

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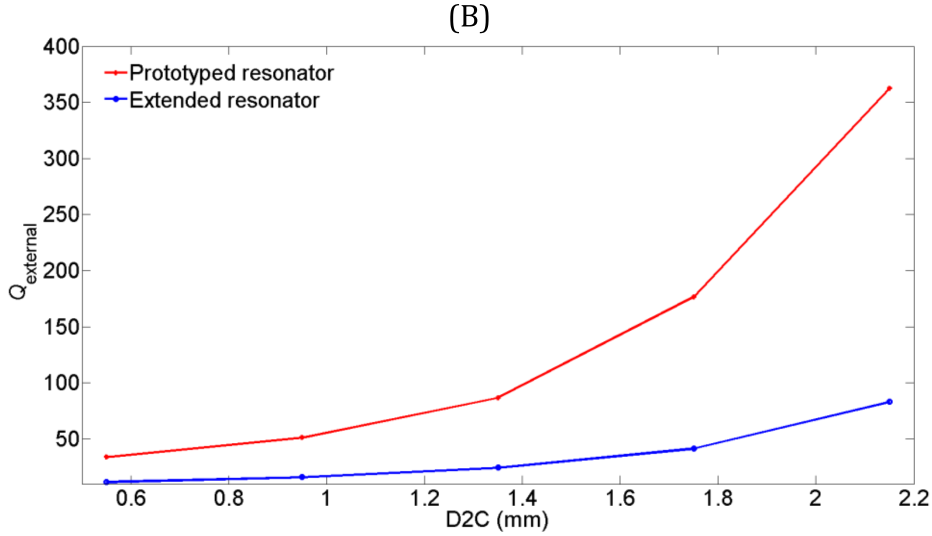


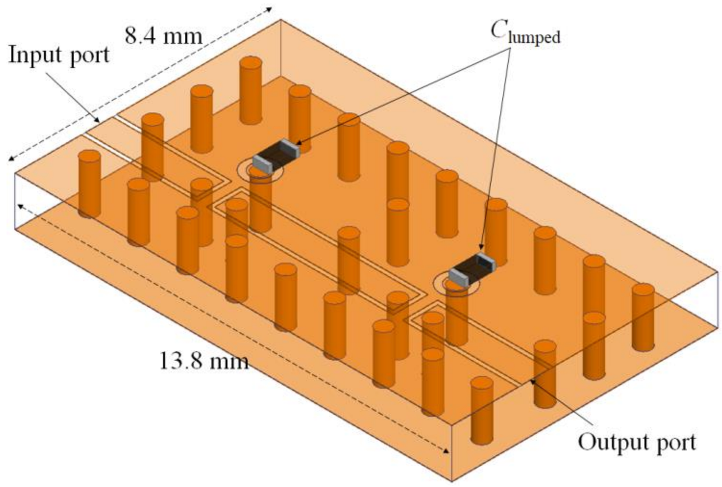

(C)

**Fig. 4.** External coupling investigation **(A)** schematic of prototyped resonator with coupling vias, **(B)** schematic of extended resonator with coupling vias, **(C)** comparisons of external quality factor $Q_{external}$ versus D2C

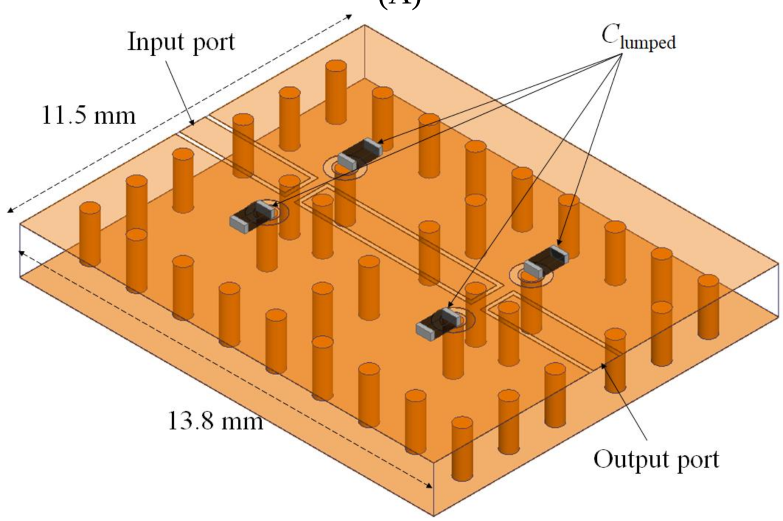
Coupling coefficient $k$ can be extracted by weakly coupling two cascaded extended resonators shown in Fig. 3. The coupling coefficients versus separation between the upper half and lower half resonator $l_m$ are calculated according to the formula given in [11] represented by (10).

$$k = \frac{f_{\mathrm{high}}^2 - f_{\mathrm{low}}^2}{f_{\mathrm{high}}^2 + f_{\mathrm{low}}^2} \tag{10}$$

Additionally, two 2nd order bandpass filters are designed, simulated, and compared side-by-side in Fig. 5. With the CPW feed line further extended into the center of the resonator, a shorting vias is used to connect both the top and the bottom metals. Both designs share the same dimensions of the coupling structure, SIW vias, as well as the pitch. The design uses the original prototyped resonator shows narrower BW, more IL and ripples whereas the design that uses extended resonators shows wider BW, less IL and ripples. Nevertheless, the footprint of using the extended resonators expands roughly 1.40 times. Although $L_{\mathrm{resonator}}$ shrinks by 38% compared with the prototype resonator, $C_{\mathrm{resonator}}$ doubles due to the summation of parallel capacitances. Therefore, given the same $C_{\mathrm{lumped}}$, simulated $f_0$ in the extended resonator is lower than the ones in the prototype resonator. Since original prototyped resonator doesn't offer strong enough external coupling, new extended resonator modifies the structure to increase the coupling without dramatically shifting resonant frequency or affecting $Q_u$, in the following discussions only designs use extended resonator are presented.




(A)

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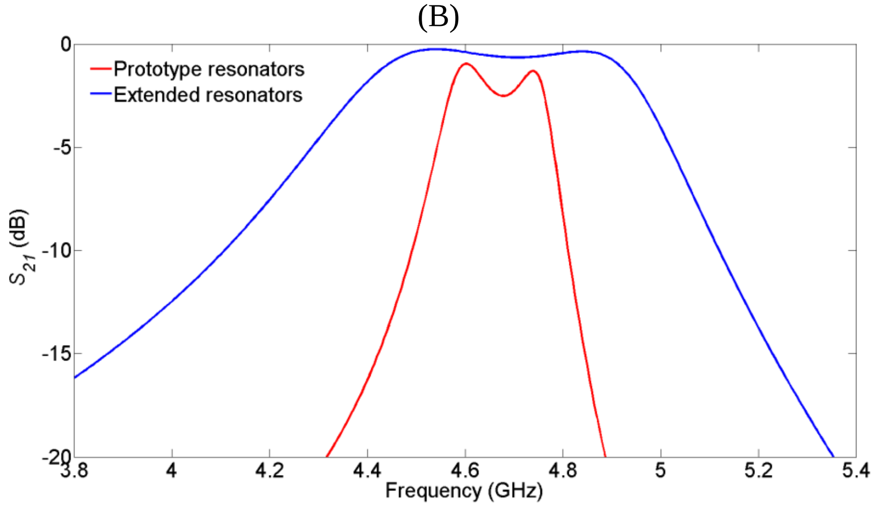



(C)

**Fig. 5.** Comparisons of simulated two-pole filters **(A)** using prototype resonators, **(B)** using extended resonators, **(C)** simulated $S_{21}$

## SECTION 2. Filter Design and Implementation

To begin with, the previous design that uses dual-mode resonator design for this filter can be found in [28]. The design shown in this section is to improve the unwanted transmissions from the previous design. Although it is possible to use two different capacitive loadings in each resonator to create dual passbands, throughout the paper only the design uses the same capacitive loading for each resonator is discussed. Based on three cascaded dual-mode resonators from Fig. 8 from [28], a variant of such a filter is redesigned and shown in Fig. 6. The critical dimensions of the filter are shown in TABLE 1. Compared to the design from [28] that has main signal path in the middle, the signal path in the middle is removed in this design; instead, the signal path is diverted to the sides, and forming two main signal routes. The lower arm and the upper arm are exactly the same but 180 degree mirrored from each other. Each contains two sets of slotlines, one set is short-circuited with the vias, and another set is terminated with SMT capacitors on the backside of the metal. Given that the magnetic coupling is dominant with short-circuited slotlines, the electric coupling is dominant with slotlines that has open-end on the backside. Fig. 7 (a) reveals the frequency response versus $C_E$ of the designed filter when $C_{Freq}$ = 1.0 pF. In ANSYS High Frequency Structure Simulator (HFSS) model, the input and the output are set as wave ports, and each capacitive loading is set as lumped port, and later in Advance Design System (ADS) bench such a lumped port can be assigned to a capacitor which is shorted to ground at the one end. While all capacitors are assumed ideal, they have consistent capacitance, zero parasitic inductance, as well as zero parasitic resistance over the frequency. Since all the capacitors are assumed ideal, the IL of the passband is low; moreover, the out-of-band rejection is better than -40 dB up to 3 $f_c$. Fig. 7 (b) demonstrate

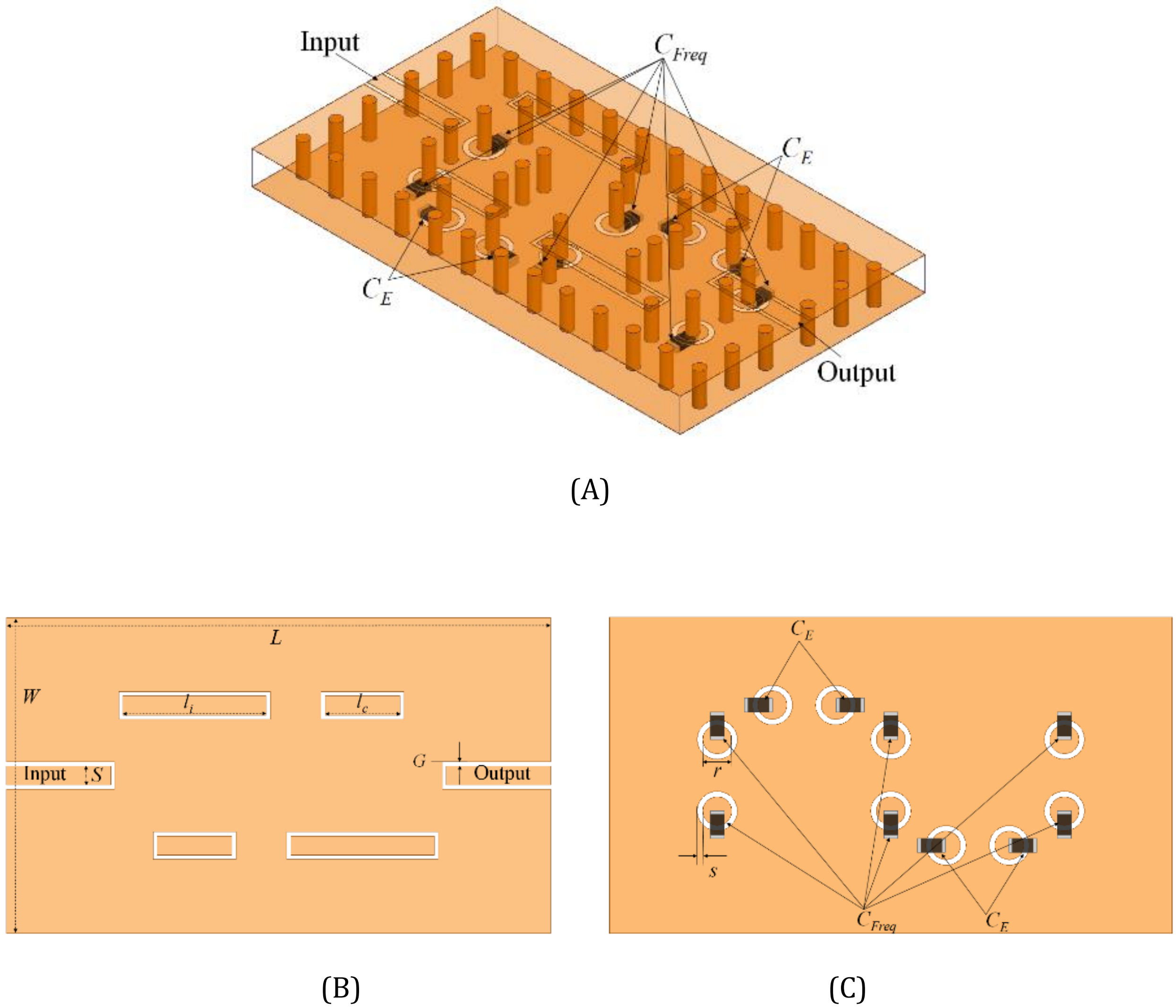
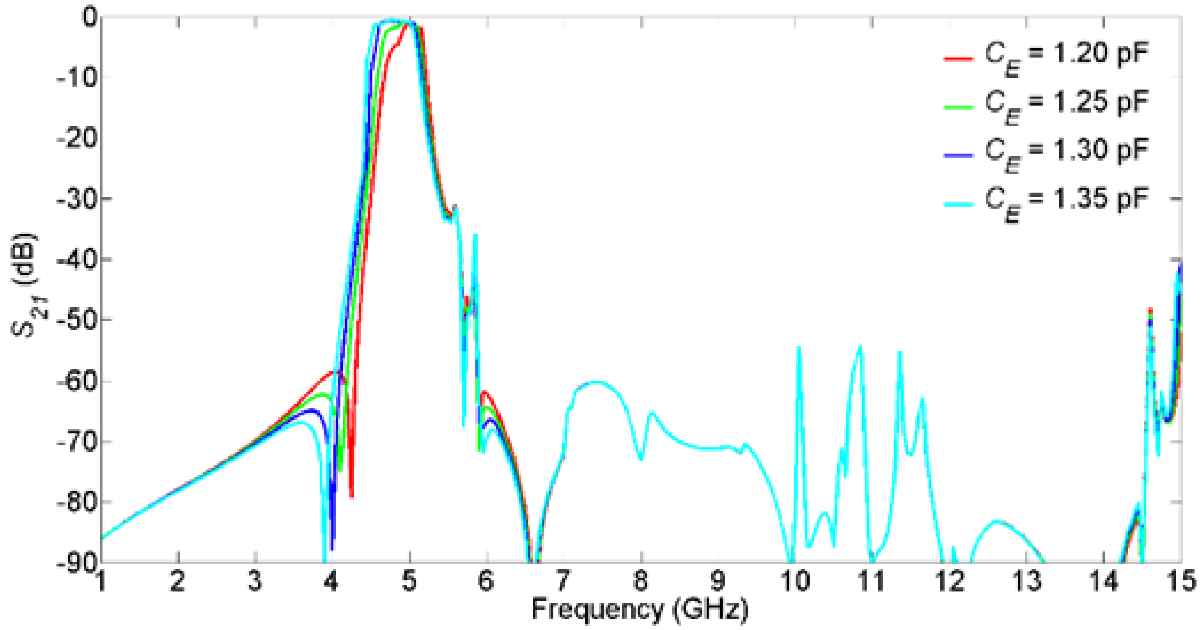



**Fig. 6.** Filter layout **(A)** filter layout, **(B)** top view, **(C)** bottom view

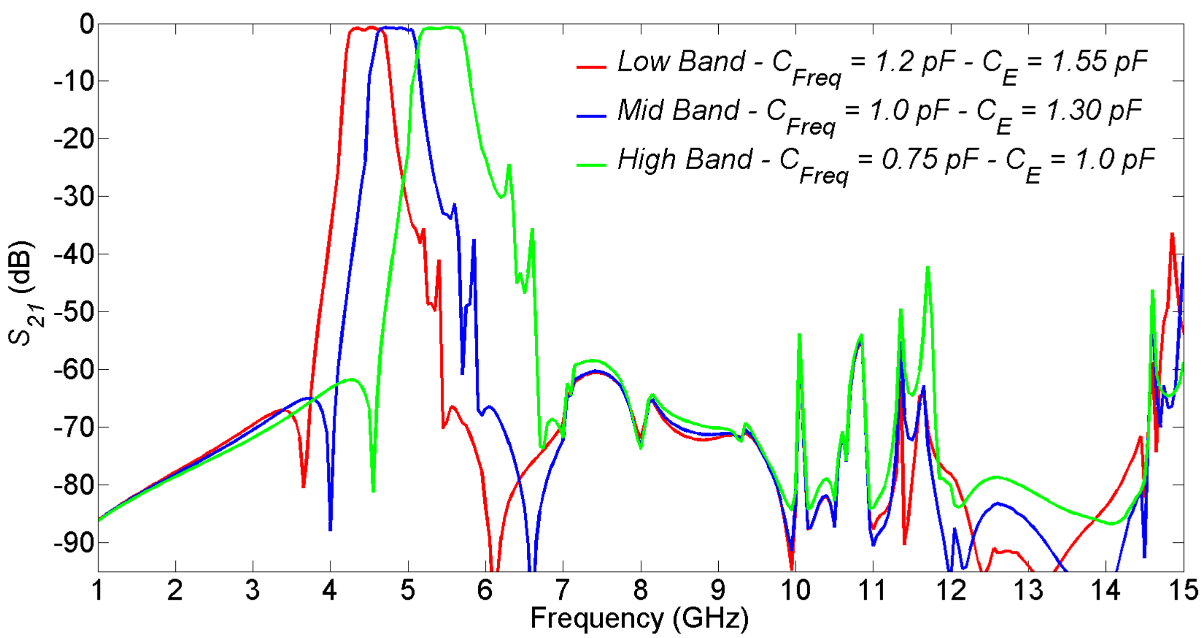
Table 4 Filter Dimensions

| Parameters | $W$ | $L$ | $H$ | $S$ | $G$ | $l_i$ | $l_c$ | $r$ | $s$ |
|---|---|---|---|---|---|---|---|---|---|
| mm | 11.5 | 20.1 | 1.524 | 0.70 | 0.15 | 5.3 | 2.76 | 0.52 | 0.2 |

three bands of the filter can be individually configured with different sets of ideal $C_{Freq}$ and $C_E$ applied. When ideal capacitors are used, some spikes are observed near the upper-end skirt, but such spurs are of little concerns when real capacitors are used due to the parasitic resistance of the capacitor will attenuate out those spurs. While only two signal routes are seemed to be implemented in the design, there are actually four routes. Shown in Fig. 8. are each signal path of the filter. Since each path has different phase delay, the phase delay of each route can be separately plotted to understand how the transmission zeroes are obtained. The phase of $S_{21}$ of each path is studied and illustrated in Fig. 9. Since route 1 is the reverse of route 3, it is no surprised that the phase delay of both routes are identical. When the phase delta reaches to 180 degree, transmission of the signal is ceased; consequently, transmission zeros can be obtained at certain frequencies. When $C_E$ is increased, the cross-point of the phase delay of route 2 and route 4 is relocated to the lower frequency, and such a phase is almost 180 degree deviates from the phase of route 1 and route 2.




(A)




(B)

**Fig. 7.** Filter frequency response with ideal capacitor **(A)** $C_E$ sweep while $C_{Freq}$ = 1.0 pF, **(B)** low-band: $C_{Freq}$ = 1.2 pF, $C_E$ = 1.55 pF; mid-band: $C_{Freq}$ = 1.0 pF, $C_E$ = 1.30 pF; high-band: $C_{Freq}$ = 0.75 pF, $C_E$ = 1.05 pF

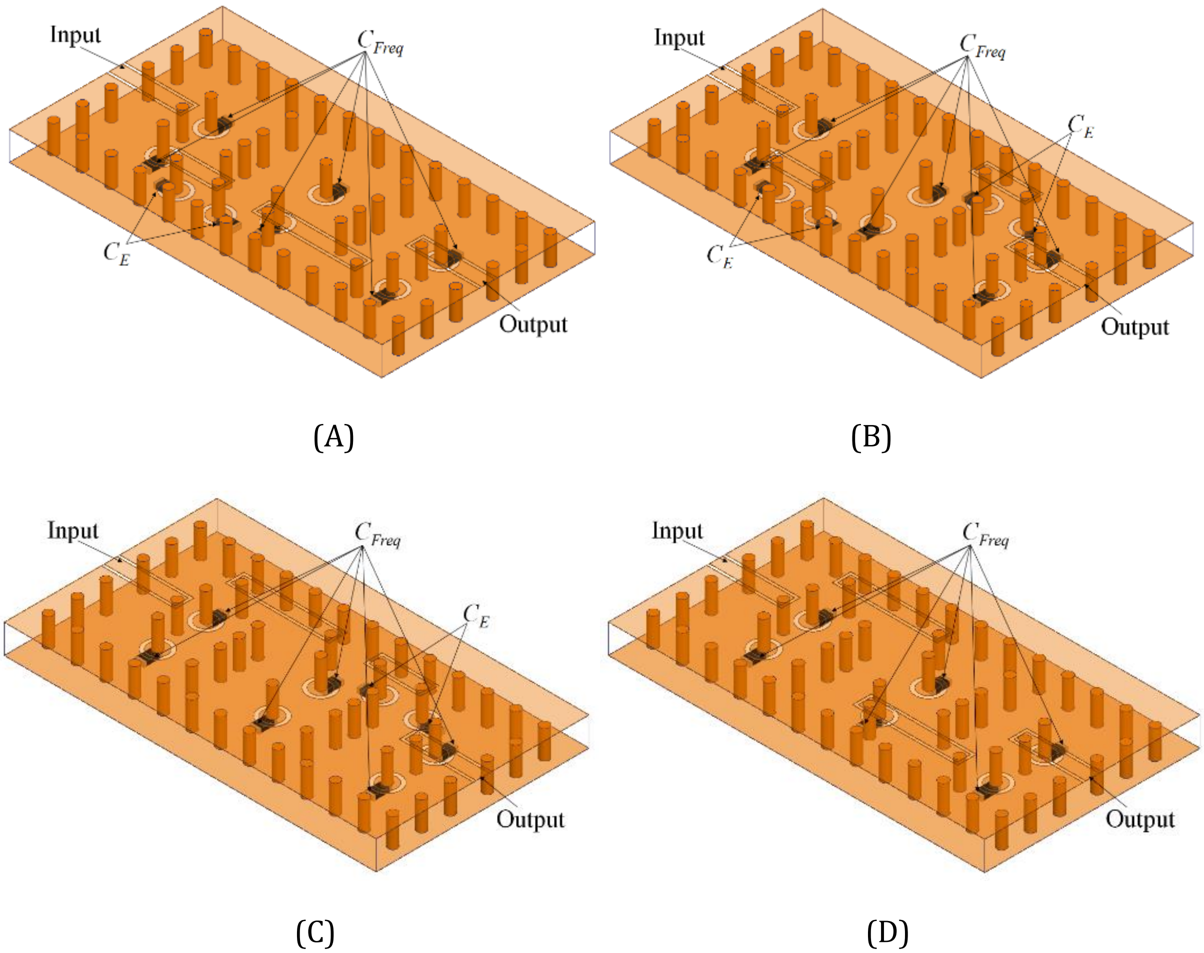



**Fig. 8.** Breakdown of the designed filter **(A)** route 1, **(B)**, route 2, **(C)** route 3, **(D)** route 4

Table 5 Cross-point Frequency of Phase Delay of Route 2 and Route 4

| | $C_E$ = 1.20 pF | $C_E$ = 1.25 pF | $C_E$ = 1.30 pF | $C_E$ = 1.35 pF |
|---|---|---|---|---|
| $f_{cross}$ (GHz) | 4.07 | 4.00 | 3.94 | 3.87 |
| $f_{LTZ}$ (GHz) | 4.25 | 4.10 | 4.00 | 3.90 |

For example, when $C_E$ = 1.30 pF, the cross-point of phase delay of route 2 and route 4 is 3.94 GHz, and the corresponding phase delta to route 1 and route 3 at this particular frequency is 175.10 degrees. When the phase difference reaches to 180 degrees at a particular frequency, transmission of the signal is completely ceased; consequently, transmission zero can be obtained. TABLE 2 shows the cross-point frequency $f_{cross}$ and the corresponding lower-end transmission zero frequency $f_{LTZ}$ versus changes of $C_E$. As $C_E$ increases, both $fcross$ and $f_{LTZ}$ decrease; thereby, the lower-end notch is reconfigured to the lower spectrum. After incorporating all four signal routes into a single design, a filter with zeros on both sides of the passband can be obtained due to the cancelling effect brought by the multipath signals. Furthermore, unlike the previous designed filter that used the direct-coupling scheme, the side-coupling scheme is adapted in this work. The direct-coupling scheme that proposed in the previous design has a drawback of narrowed spurious-free range due to current probes are placed near the center of each resonators and become very close to each other, therefore, energy can propagate through the structure at a higher frequency such as $2f_c$ or so. On the other hand, much wider spurious-free range can be realized by deploying the side-coupling scheme. Note that in previous work, noticeable unwanted transmission can be observed roughly at $2f_c$ whereas in this work, out-of-band rejection holds up well up to $3fc$.

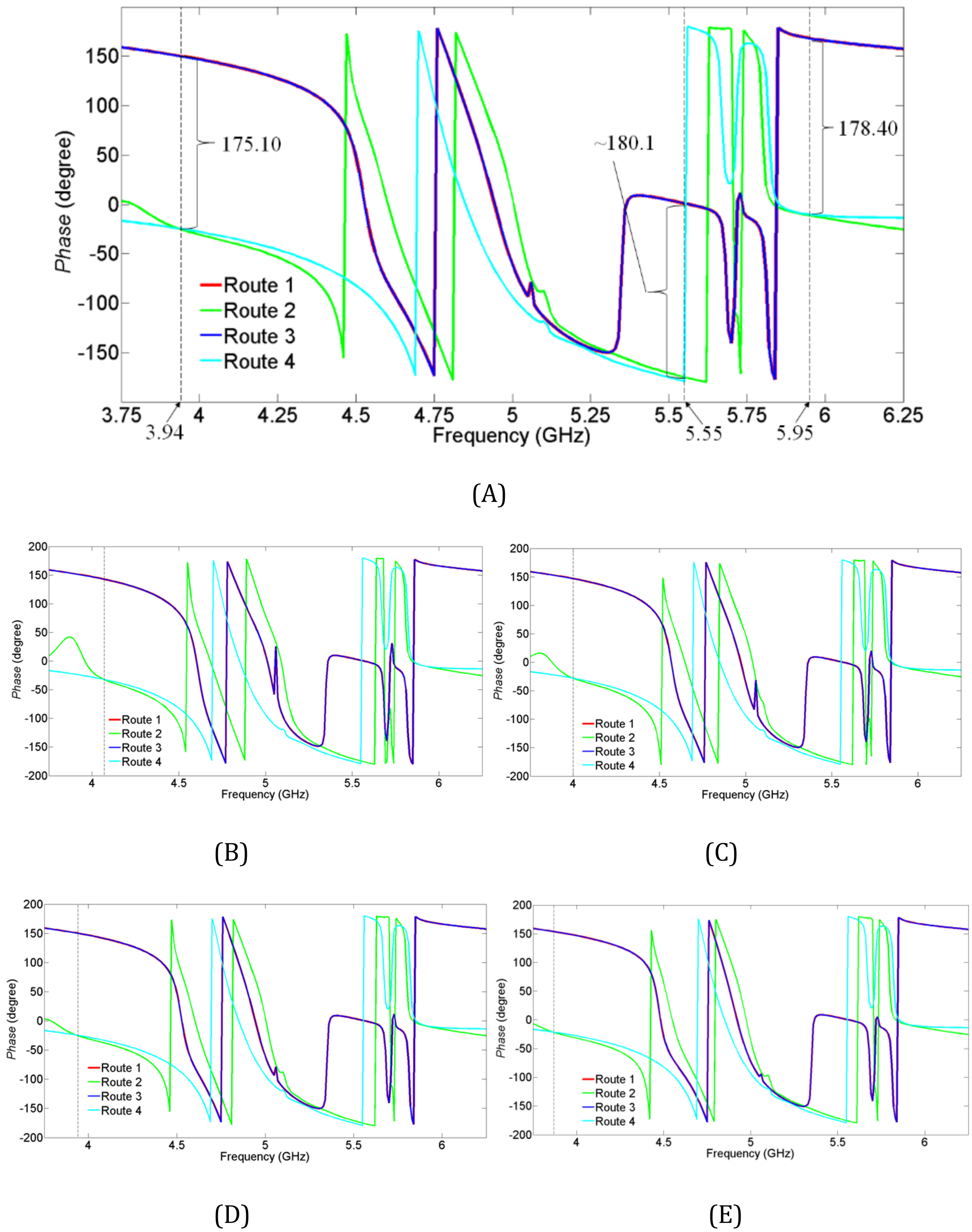



**Fig. 9.** Four routes' phase and phase delta versus TZs **(A)** zoom in: $C_{Freq}$ = 1.0 pF and $C_E$ = 1.30 pF, **(B)** $C_{Freq}$ = 1.0 pF and $C_E$ = 1.20 pF, **(C)** $C_{Freq}$ = 1.0 pF and $C_E$ = 1.25 pF, **(D)** $C_{Freq}$ = 1.0 pF and $C_E$ = 1.30 pF, **(E)** $C_{Freq}$ = 1.0 pF and $C_E$ = 1.35 pF

## SECTION 3. Design Implementation with Real Capacitors

By far, ideal capacitors that have consistent capacitance with zero equivalent series resistor (ESR) and zero equivalent series inductor (ESL) are used in the simulations. However, in reality, equivalent capacitance rises while the quality factor (Q) degrades with respect to frequency increase due to these parasitic elements take effects. According to [9], when multiple parallel capacitors are used, total ESR can be minimized thus improve the overall Q of the equivalent capacitor as a whole. Meanwhile, since the unloaded quality factor ($Q_u$) of a given capacitive-loaded SCC resonator heavily depends on the Q of the capacitor [28], improving overall Q of the capacitor results in better $Q_u$ of the resonator. Conceptually, by deploying multiple smaller capacitors in parallel, the total ESR can be reduced. Borrowing the same idea, we further investigate how the ESL can be reduced in the similar fashion, given that the parasitic inductance can directly impact out-of-band transmission. In order to extract the ESR and ESL, one-port model of a series *RLC* is used, and when the $S_{11}$ contour in the Smith chart from the equivalent circuits matches with the one from the s2p files from the vendor, the component values of the equivalent series *RLC* are recorded accordingly in Table 6. Equivalent capacitance and Q at 4.84 GHz are also calculated, where 4.84 GHz is the center frequency of the passband that serves as an example in the following section. Such a series *RLC* is later used in the ADS bench as a way to emulate the results derived directly from the real capacitors' touchstone files. In Fig, 10., the schematic of the different capacitor configurations are shown.

Table 6 Extracted Equivalent Series *RLC* versus Capacitor Configurations

| | Single | Dual | Triple | Quad |
|---|---|---|---|---|
| $C_{Freq}$ / $C_{Freq}'$ (pF) | 0.75 / 1.02 | 0.85 / 1.01 | 0.90 / 1.01 | 0.90 / 0.99 |
| $ESC_{Freq}$ (pF) | 0.755 | 0.854 | 0.90 | 0.910 |
| $ESR_{Freq}$ (Ohm) | 0.310 | 0.250 | 0.240 | 0.230 |
| $ESL_{Freq}$ (nH) | 0.385 | 0.199 | 0.132 | 0.110 |
| $Q_{Freq}$ | 112.266 | 131.580 | 135.607 | 151.255 |
| $f_{Freq\_res}$ (GHz) | 9.335 | 12.209 | 14.602 | 15.908 |
| $C_E$ / $C_E'$ (pF) | 0.90 / 1.29 | 1.05 / 1.30 | 1.10 / 1.28 | 1.15 / 1.29 |
| $ESC_E$ (pF) | 0.90 | 1.05 | 1.11 | 1.15 |
| $ESR_E$ (Ohm) | 0.250 | 0.203 | 0.19 | 0.185 |
| $ESL_E$ (nH) | 0.362 | 0.196 | 0.115 | 0.105 |
| $Q_E$ | 89.504 | 102.406 | 108.343 | 116.524 |
| $f_{E\_res}$ (GHz) | 8.818 | 11.094 | 14.087 | 14.484 |

$C_{Freq}$ is the labeled value of the capacitance, and can be regarded as an equivalent series circuit of $ESC_{Freq}$, $ESR_{Freq}$, and, $ESL_{Freq}$ where $C_{Freq}'$ is the extracted equivalent capacitance of $C_{Freq}$ at 4.84 GHz; similarly, $C_E$ is the labeled value of the capacitance, and can be regarded as an equivalent series circuit of $ESC_E$, $ESR_E$, and, $ESL_E$ where $C_E'$ is the extracted real capacitance of $C_E$ at 4.84 GHz; $f_{Freq\_res}$ and $f_{E\_res}$ are the self-resonant frequency of the capacitor $C_{Freq}$ and $C_E$ respectively.

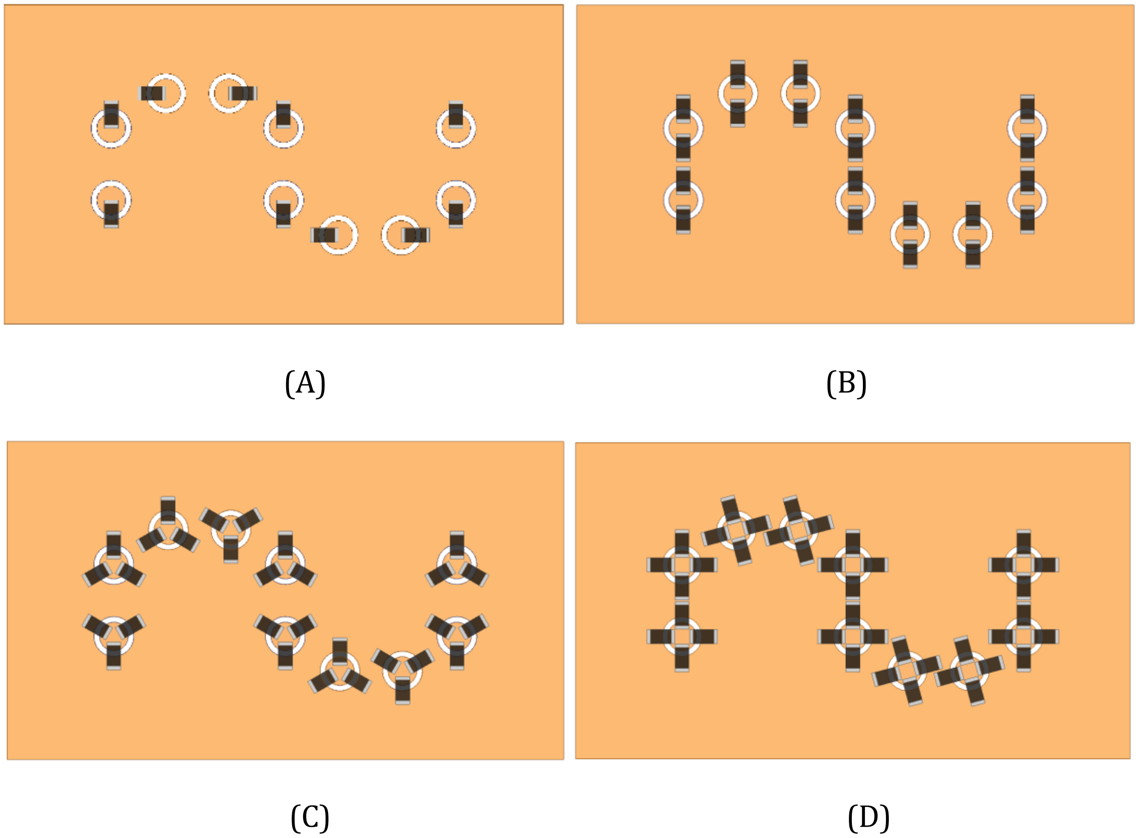
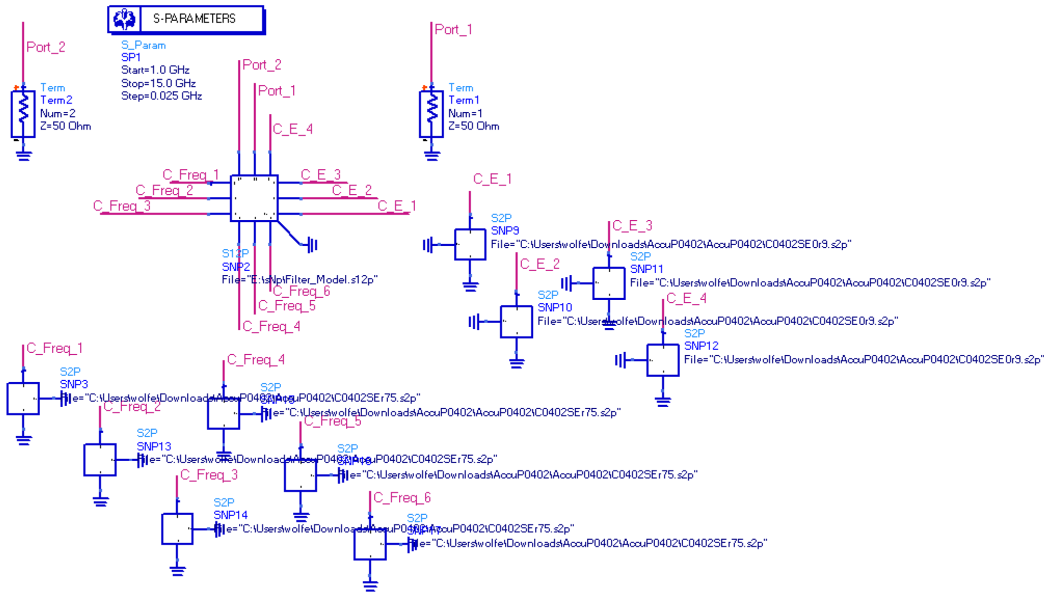


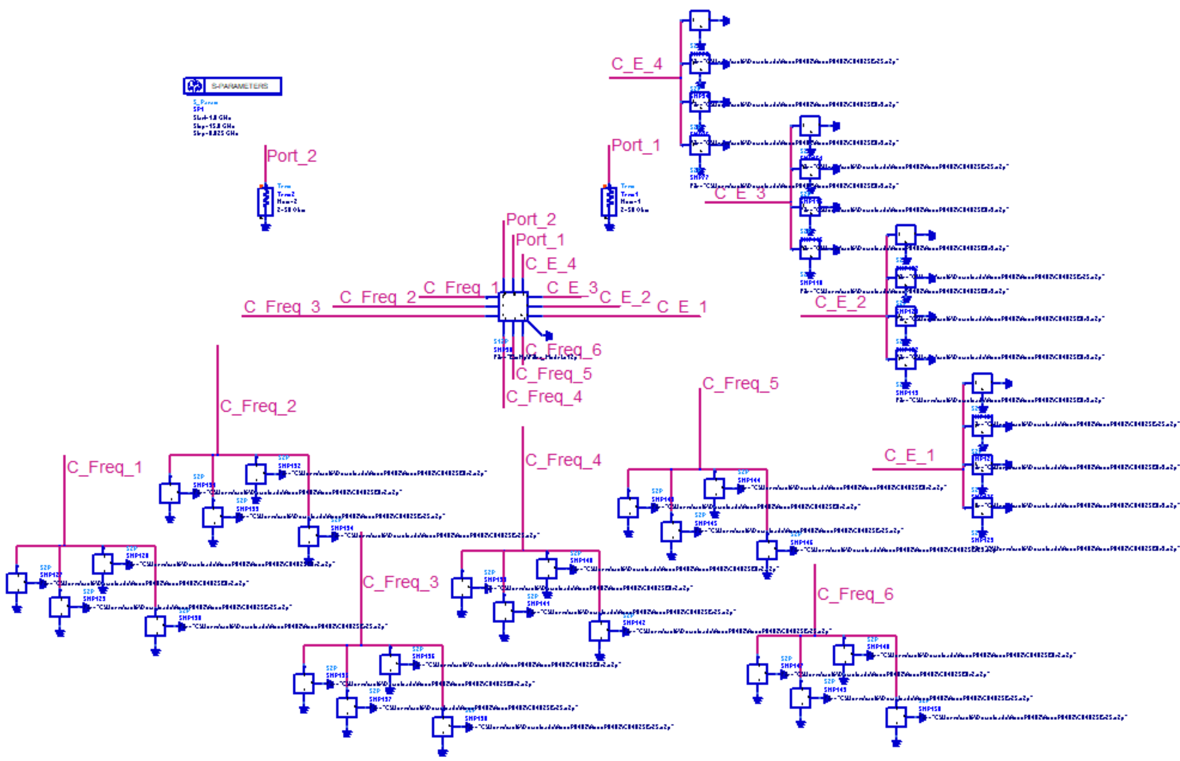
**Fig. 10.** Capacitor configuration **(A)** single, **(B)**, dual, **(C)** triple, **(D)** quadruple

While it is possible to use different parallel capacitor combinations to yield the same equivalent capacitance, we try to use the ones that have similar labeled capacitance in each capacitive loading. Meantime, the extracted equivalent capacitance $C_{Freq}'$ and $C_E'$ of the designed capacitor groups needs to be aligned to 1.0 pF and 1.30 pF respectively at 4.84 GHz as Table 6 suggests, such that fair comparisons can be made. Shown in Fig. 11. is how the capacitor implementation can be done in the ADS bench. In the single capacitor configuration, each net connects to a single data item which contains a s2p file from the capacitor; in the quadruple capacitor configuration, each net connects to four data items. Later, the data items of the capacitors are replaced by series $RLC$ shown in Fig. 12. as a way to further investigate the cause of the out-of-band transmission.

In Fig. 13 (A), the frequency response of the filter versus the capacitor's configuration is illustrated. The 0402 AVX Accu-P series capacitors' s2p touchstone file from the vendor are used in the simulation. With only one single capacitor used, the passband insertion loss is the highest, and the bandwidth is the least. While maintaining the total equivalent capacitance, the total ESR and ESL are reduced as the number of the parallel capacitor adds up. Thus, the equivalent quality factor of the capacitor increases, and such a capacitor has more consistent equivalent capacitance over the frequency due to the self-resonant frequency becomes higher as the parasitic inductance is reduced. When ideal capacitors are applied, the bandwidth is the largest with the least insertion loss due to the capacitor has infinite Q and constant capacitance versus frequency. Both the bandwidth and the in-band loss are the worst with the single real capacitor configuration because the single real capacitor configuration shows the largest ESR and the most inconsistent equivalent capacitance over the frequency due to the lower self-resonant frequency caused by the larger ESL. Moreover, the out-of-band transmission can also be mitigated with higher orders of the capacitor implemented given that the total ESL becomes less. By using extracted series $RLC$ values from Table 6, Fig. 13 (B) demonstrates the results from series $RLC$ are well-correlated to the results derived from the capacitors' s2p files. Obviously, the high frequency spurs are strongly related to the ESL.

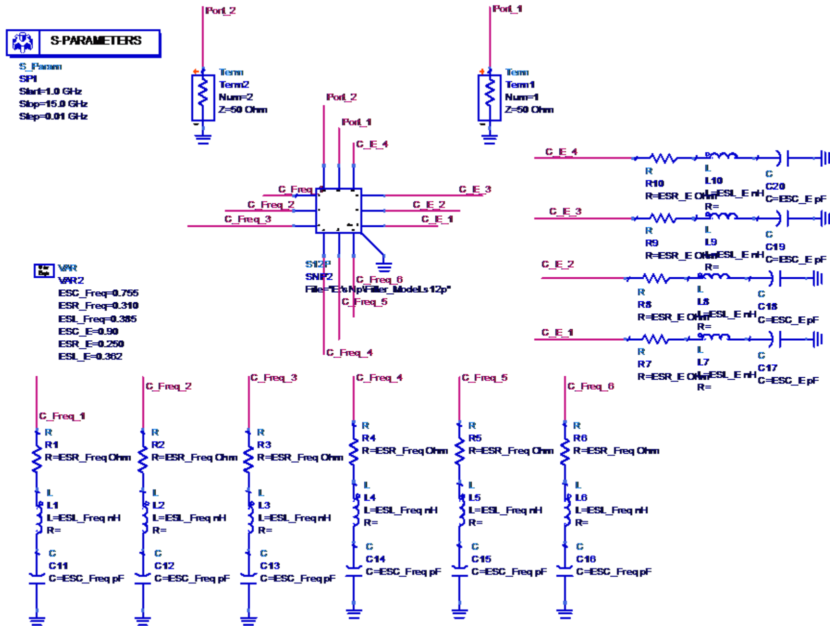



(A)

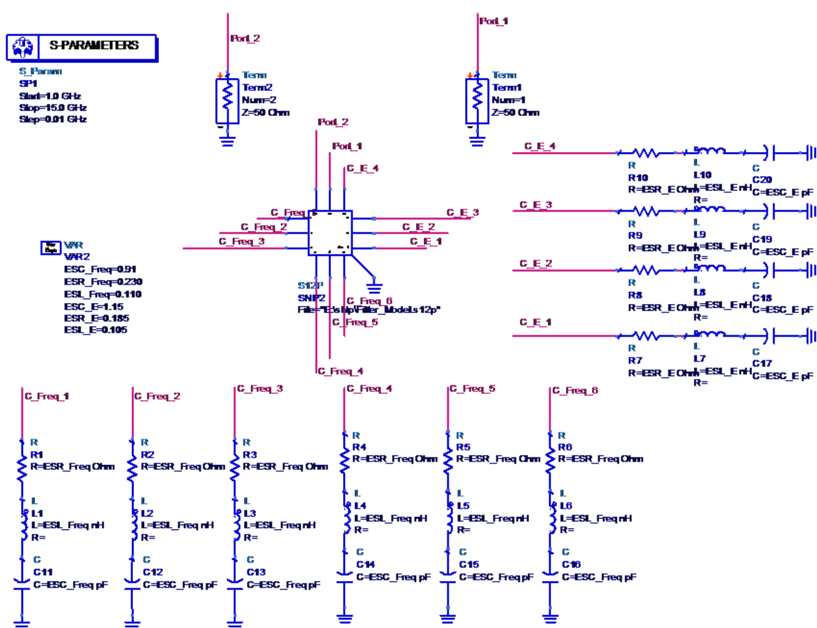


(B)

**Fig. 11.** ADS bench with real capacitor's touchstone files **(A)** single capacitor, **(B)** quadruple capacitor

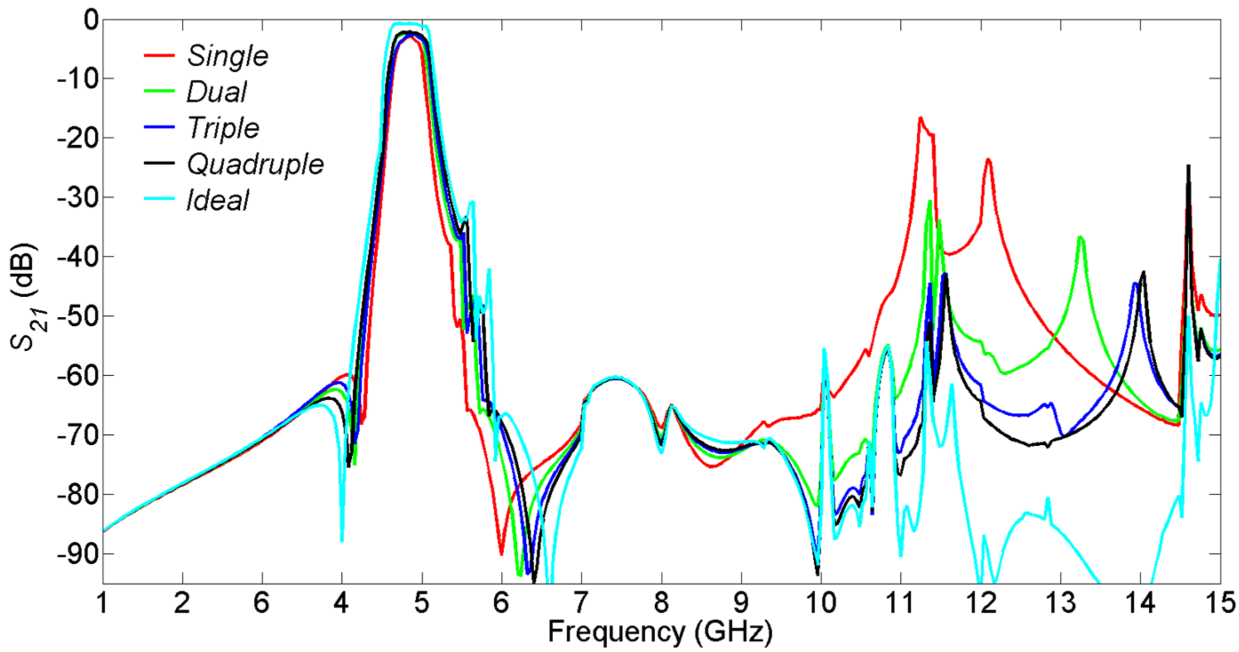


(A)

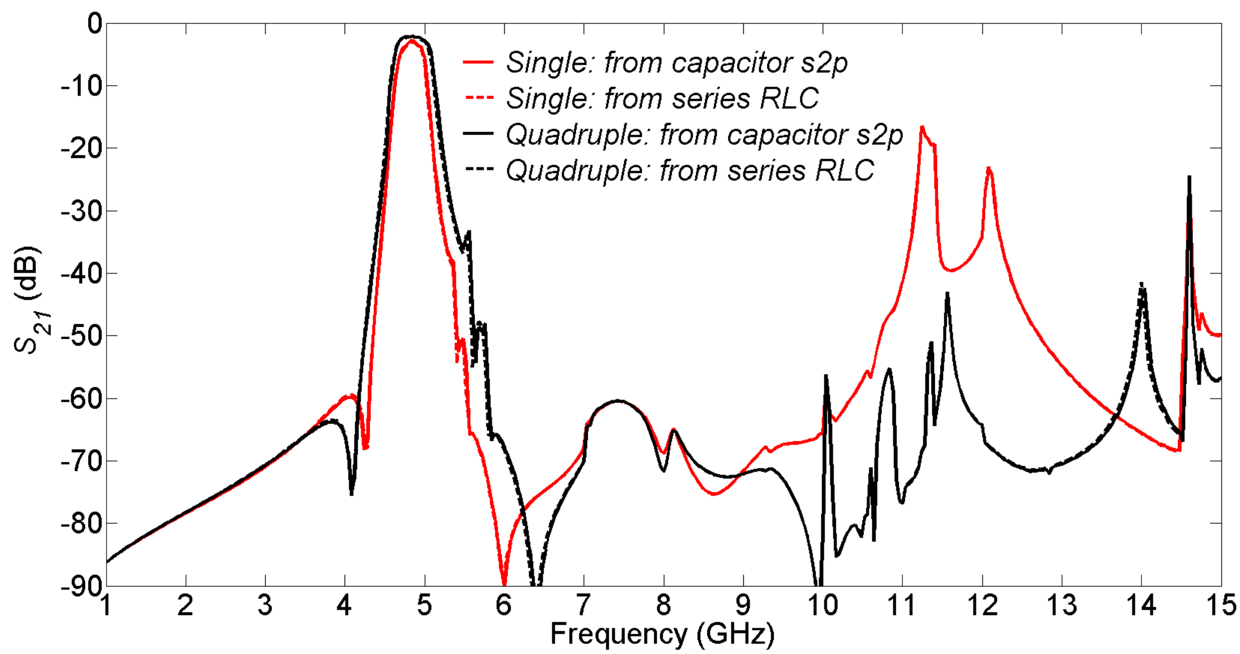


(B)

**Fig. 12.** ADS bench with extracted series *RLC* **(A)** single capacitor configuration, **(B)** quadruple capacitor configuration




(A)




(B)

**Fig. 13.** Filter frequency response with real capacitors implemented **(A)** $S_{21}$ versus capacitor configurations (simulated with real capacitors' s2p files only), **(B)** simulated results from capacitors' s2p files (solid) versus results from series *RLC* (dotted)

A rapid-changing spike can be observed for all four configurations at 11.40 GHz. To verify how parasitic components are introducing the spike, the extracted series $RLC$ value are then converted to parallel $RLC$ at this particular frequency, such that the converted values can be set as lumped $RLC$ boundary in HFSS model. Fig. 14. shows the field plots comparisons between the two configurations at 11.40 GHz. With the single capacitor configuration applied, unwanted parasitic modes are excited inside the substrate and create transmissions; however, in the quadruple capacitor configuration, no field can be observe due to the minimal transmission while the same plotting scale are applied. Needless to say, the main benefit of replacing single capacitor with multiple capacitors in parallel to suppress stopband spikes is evident.

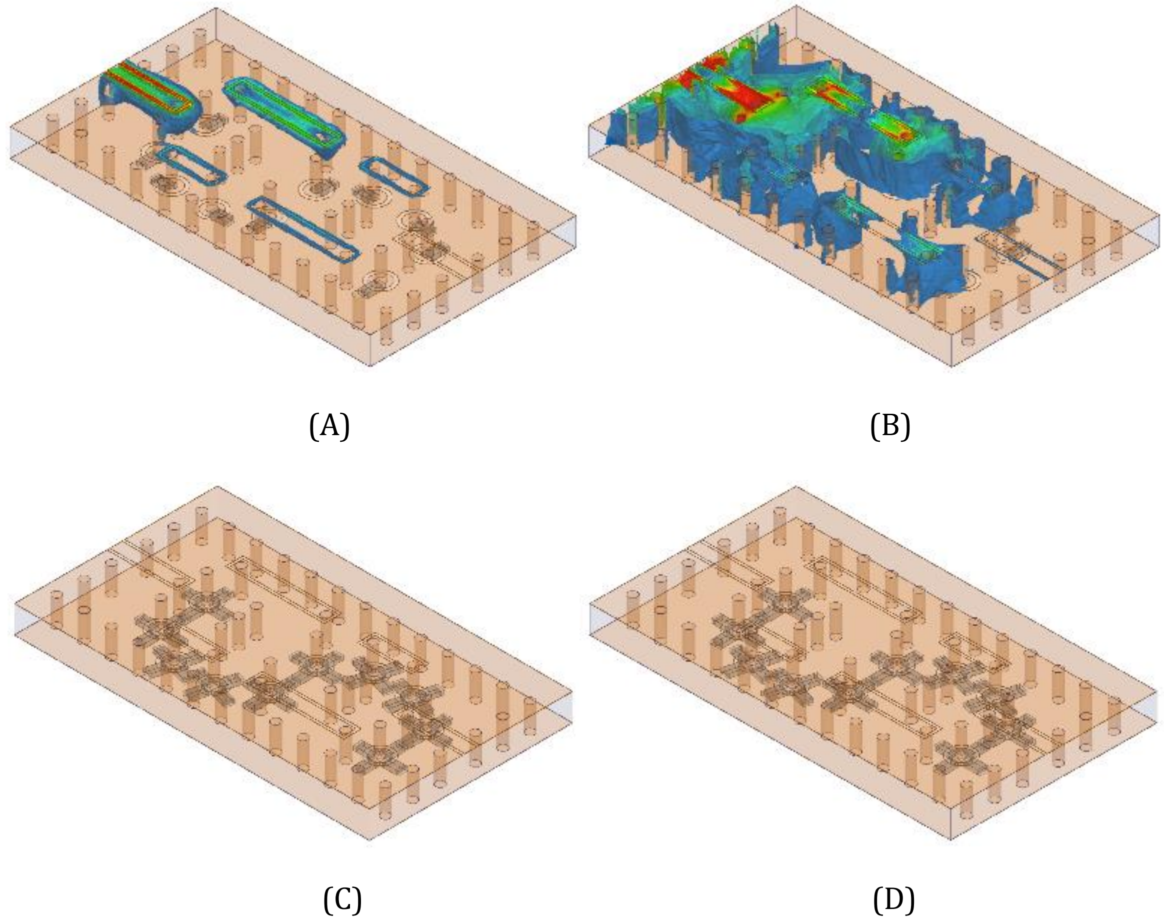
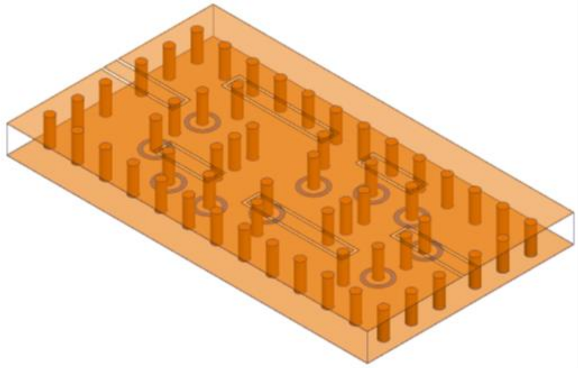


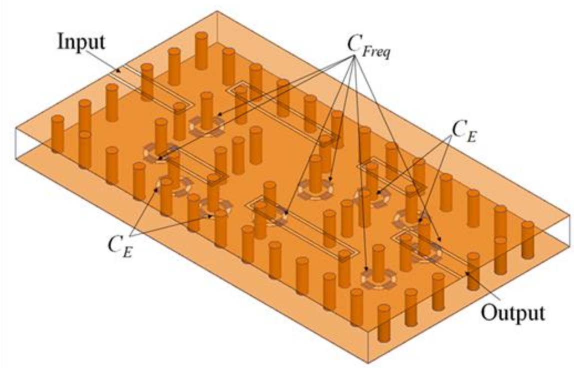

**Fig. 14.** Field plots comparisons at 11.40 GHz **(A)** E-field of single capacitor configuration, **(B)** H-field of single capacitor configuration, **(C)** E-field of quadruple capacitor configuration, **(D)** H-field of quadruple capacitor configuration

## SECTION 4. Conclusion and Future Work

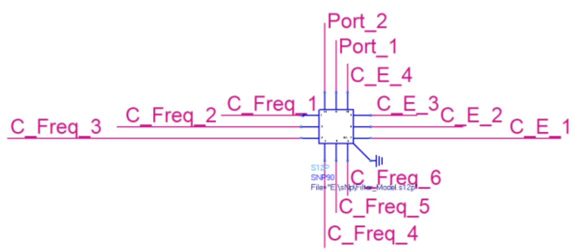
By far, our simulation result did neither include the mutual couplings between the capacitors nor the effect of changing alignments of the capacitor. In order to investigate the couplings between the capacitors, one needs to acquire capacitors' 3D HFSS models, but such models are often proprietary. Nevertheless, it is possible to demonstrate how different the geometry layouts of the capacitor alignment can impact the performance. Shown in Fig. 15. is such an attempt. Now the original single lumped port is now replaced by four lumped ports. Later each lumped port will be connected to a single data item in ADS. Shown here is the frequency response comparison of the two schematic. The one on the left does not include any geometric effect from the capacitors (no coupling) whereas the one on the right includes the geometric effect from the capacitors alignment (2D coupling). But the couplings from the parasitic elements are still omitted in the 2D coupling investigation. The frequency response from the 2D couplings shows higher spur level near 9.0 GHz. This means the isolation between two given lumped capacitors are not ideal. But at least at this stage, no peculiar frequency response like gigantic spike is observed. To better understand how the coupling is happening in the real scenario, 3D models of the capacitors are needed.

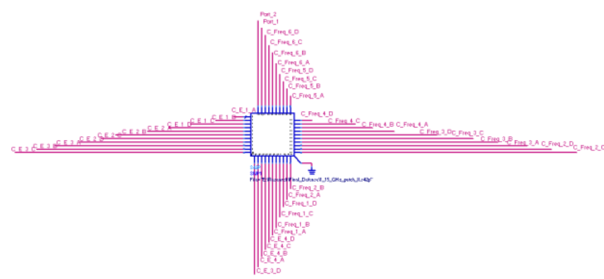
In conclusion, proposed design demonstrates an alternative way to introduce zeros to the two sides of the passband. In general, good out-of-band rejection below -30 dB is extended to three times of the center frequency. By using the vendor provided capacitor's touchstone file, the performance of the filter can be accurately predicted. In addition, using multiple parallel capacitors to replace single standalone capacitor in each capacitive loading to reduce the overall ESR and ESL can improve in-band loss as well as suppress out-of-band spurs. Hence, it becomes more plausible for designing a short-circuited SIW coax bandpass filter that uses SMT capacitors as capacitive loads at higher frequencies. Last but not the least, proposed design can be easily integrated with other planar structures such as microstrip or coplanar waveguide, and the manufacturing cost of the single laminate PCB are comparatively low.



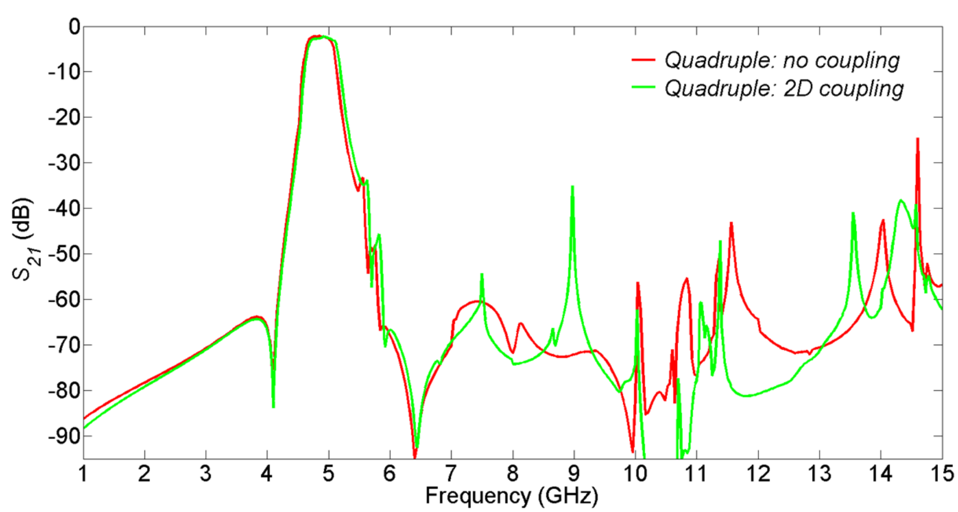



(A) (B)



(C) (D)




(E)

**Fig. 15.** Study of the impact of the capacitor alignment **(A)** layout of no couplings considered, **(B)** layout of 2D coupling considered, **(C)** exported HFSS symbol in ADS for no coupling, **(D)** exported HFSS symbol in ADS for 2D coupling, **(E)** frequency response

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