UNIVERSITY OF CALIFORNIA
SANTA CRUZ

MULTI-FREQUENCY RESONANT CLOCKS

A thesis submitted in partial satisfaction of the
requirements for the degree of

MASTER OF SCIENCE

in

COMPUTER ENGINEERING

by

Benjamin Michael LaCara

June 2014

The Thesis of Benjamin Michael LaCara
is approved:

Prof. Matthew Guthaus, Chair

Prof. Jose Renau

Prof. Martine Schlag

Tyrus Miller
Vice Provost and Dean of Graduate Studies

Table of Contents

List of Figures

List of Tables

Abstract

Multi-Frequency Resonant Clocks

by

Benjamin Michael LaCara

Clock distribution networks consume a significant portion of total chip power in high-performance designs. Of many proposed solutions to this drain, clock resonance has been shown to be an effective method for dealing with chip power and area issues with savings of 20% in modern designs as well as a lower number of required clock buffers. Current resonant solutions come with the limitation of optimal performance at one particular frequency which may be unsuited for the task at hand. For instance, switching from number crunching at work to a kitchen timer at home. If careful tuning is not made then excess power may be spent instead of saved. This thesis introduces the first scheme to produce a clock distribution network with a tunable resonant frequency. Experimental results show the resonant frequency ranges from 1.2GHz to 2.6GHz. This is done while saving up to 41% power on the clock distribution network when compared to the non-resonant distribution.

Chapter 1

Introduction

Power consumption continues to be a major concern for ASIC designs. Recent trends towards mobile applications have underscored the need for more power efficient devices. It has been shown that the on-chip clock distribution network (CDN) draws up to 70% of total chip power [1]. The majority of this drain is due to dynamic switching of sequential elements across the whole chip. The dynamic power can be expressed as

$$P = \alpha C V^2 f \tag{1.1}$$

which consists of switching activity (α), CDN capacitance (C), supply voltage (V) and clock frequency (f).

Strategies such as clock gating, power gating, dynamic voltage scaling, dynamic frequency scaling and multiple threshold voltages have been used to lower the static and dynamic power draws on chip as expressed in the equation above. Along with these, resonant approaches have been explored to reduce power costs by recycling energy on the CDN. Resonance occurs when the capacitive and inductive components cancel at a

particular frequency.

Previously explored resonant approaches include standing wave oscillators [8], rotary/salphasic clocks [3, 12, 14] and resonant inductor-capacitor (LC) tanks [2, 4, 6, 15, 17]. Standing wave resonant clocks result in a constant phase but their amplitude varies depending on placement in the CDN. Conversely, rotary resonant clocks provide consistent amplitude with phase which varies depending on from where the clock is tapped. LC tanks boast the greatest promise as they ideally provide constant magnitude and phase which is similar to non-resonant clocks and allows for similar methodologies.

Due to the increasing power and timing demands of modern chips clock grids are regularly implemented in designs [9, 13]. This is due to their superior skew and robustness when compared to trees. Their drawback is that they consume more power due to an increased capacitance from redundant wires. Placing LC tanks on the global clock mesh reduces this power draw by increasing the input impedance and allowing for smaller drivers.

This thesis explores the automated design of the first tunable, global, resonant clock mesh on an ASIC design. Low area, high quality passive inductor models are used and the designs are verified using hspice on ISPD competition benchmarks.

The thesis is organized as follows. Chapter 2 provides a background on resonant theory, passive inductor models and mesh automation. Chapter 3 discusses the design choices and trade-offs of our model. Chapter 4 showcases our experimental results. Finally, Chapter 5 summarizes our approach and discusses the future direction of the research.

Chapter 2

Background

Before discussing the specifics of our mutli-frequency CDN, this section provides an overview of the components of LC tanks and their typical behavior.

2.1 Resonant Theory

An LC tank consists of an inductor and capacitor connected in series or parallel as shown in Figure 2.1. When an oscillating signal is applied to this circuit an exchange of energy occurs between the magnetic field of the inductor and the electric field of the capacitor. Resonant frequencies are observed where the inductor and capacitor experience equal reactance in series or in parallel. This frequency can be computed using

$$f = \frac{1}{2\pi\sqrt{LC_s}} \tag{2.1}$$

where L is the size of the inductor and C_s is the clock load capacitance. Ideally, this results in an infinite impedance in parallel and a zero impedance in series. This circuit

allows us to recycle energy on the CDN when the inductor is attached in parallel to the clock load.

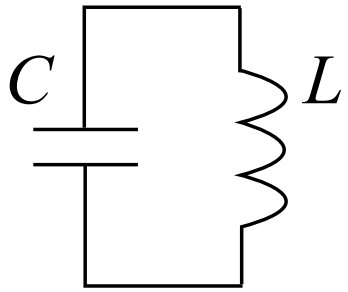

Figure 2.1: At resonance the L and C components cancel which results in a parallel LC tank with infinite impedance.

An LC oscillator will swing between positive and negative voltages which is undesirable given CMOS logic levels of 0 and V_{dd} volts. This issue is addressed by biasing the circuit with a decoupling capacitor (C_d) at the grounded end of the inductor as shown in Figure 2.2 [2]. This capacitance must be sufficiently large in order to cleanly separate the series and parallel resonant frequencies. Considering the clock load and decoupling capacitor we want the resonant frequencies to relate as

$$\frac{1}{2\pi\sqrt{LC_d}} << \frac{1}{2\pi\sqrt{LC_s}}, \tag{2.2}$$

Figure 2.3 shows the characteristic impedance of an ideal LC tank circuit exactly like the one in Figure 2.2. This shows the two resonant frequencies as they are represented in magnitude (db) and phase (deg). This type of representation will be referred to as the *characteristic impedance*. We can see the magnitude tend towards positive and negative infinity at resonance. The phase shifts from about $-90°$ to about $90°$ at the resonant frequencies which represents the circuits transition from functioning

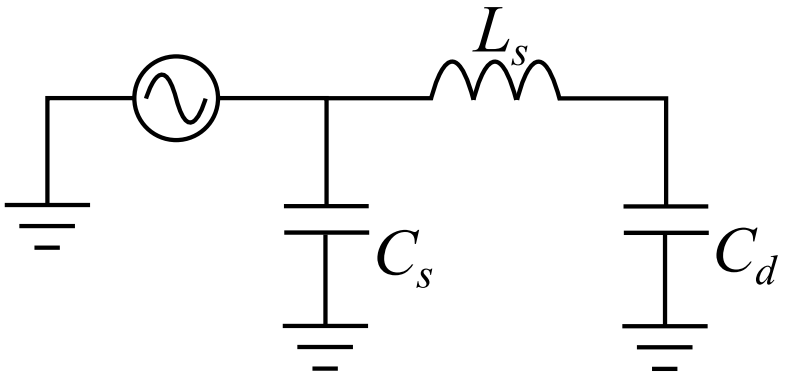

Figure 2.2: Basic LC tank circuit which consists of a series component with L and C_s and a parallel component with L and C_d.

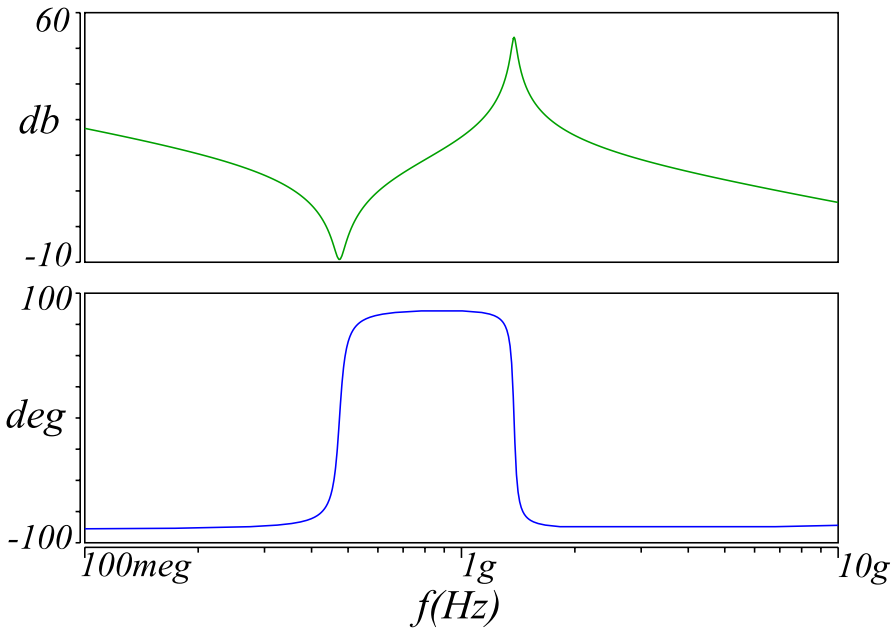

Figure 2.3: The characteristic impedance of an ideal LC tank circuit. The decoupling resonant frequency tends toward $-\infty$ while the series resonance tends towards ∞.

as a capacitor to functioning as an inductor.

In reality, LC tank circuits are RLC circuits. At resonance the capacitive and inductive components cancel out and leave only the resistive component. These resistances exist in passive inductors and capacitors, all clock distribution wires as well

as output drivers to the CDN. Reducing the parasitic capacitance and impedance with an LC tank lowers those parasitics on the whole CDN which mitigates the overall power necessary to drive the load.

2.2 Passive Inductor Models

On-chip inductors are best drawn on top level metal layers. They may be single or multi-layered, they may be square or octagonal and they may or may not include a grounded metal layer beneath the spiral [16]. Each of these options affect the total amount of induction and quality factor (Q) of the inductor. For simplicity we are using single-layered square inductor models with no ground plane much like the one shown in Figure 2.4. Here, n represents the number of full turns, w is the width of the metal traces, s is the spacing between turns and l is the length of the side. We are particularly interested in l as it determines the total chip area which a single inductor occupies.

The Q of an inductor determines the amount of magnetic energy it can store and may be found using

$$Q = \frac{\omega L}{R}. \tag{2.3}$$

This is partially what leads inductors to being on the top-level metals as they are thicker and thus have lower resistances to improve the Q. Having a large Q allows us to store more energy but it is also less able to deal with process variation and frequency miss-match due to a narrow bandwidth. Conversely, a low Q withstands process variation at the cost of retaining less energy.

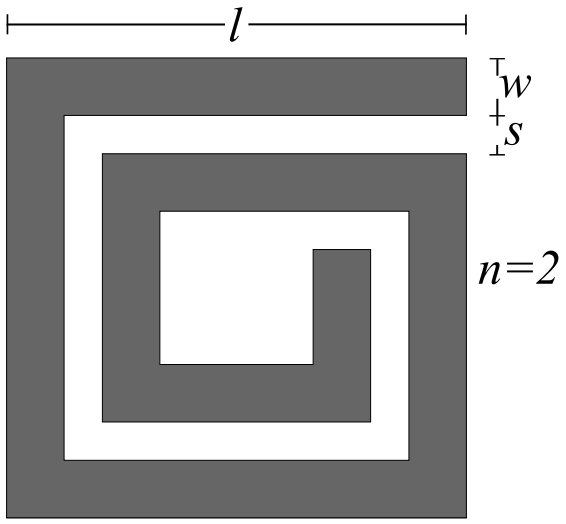

Figure 2.4: Passive inductor metal trace measurements. All are square and have a length no greater than $100\mu m$.

Previous works [10,11] have had Q values around 3.5 to 3.8 at 4GHz with areas within $100\mu m^2$. Our models have been created using the Sonnet EM Suite and output as spice circuits. The *l, w, s* and *n* values for our models were determined after more than ten-thousand steps of simulated annealing while optimizing for area and Q. These models include the parasitic capacitances from the parallel metal traces in the spiral. They also include parasitic resistances from these metal traces. All models have a Q of roughly eight at 1.5GHz and fit within $100\mu m^2$. The spice model is shown below in Figure 2.5.

Figure 2.6 shows the magnitude and phase plots of the characteristic impedance of two individual LC tank circuits. One has an ideal inductor while the other uses a passive inductor model of the same value. The general behavior is clearly the same with the trends towards positive and negative infinity in the magnitude and the 180° shift in the

phase showing the change from capacitive to inductive characteristics. The bandwidth is increased with the passive model due to the parasitic resistance and capacitances it presents.

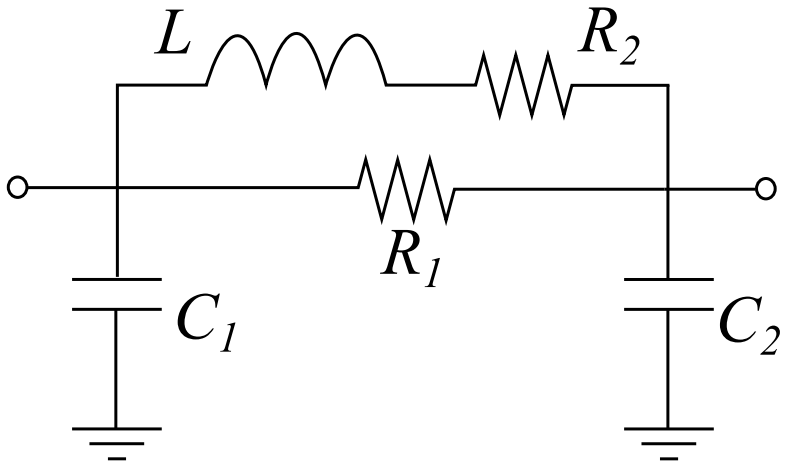

Figure 2.5: Passive inductor models include series resistances and parallel capacitances. These increase the bandwidth of an LC tanks characteristic impedance.

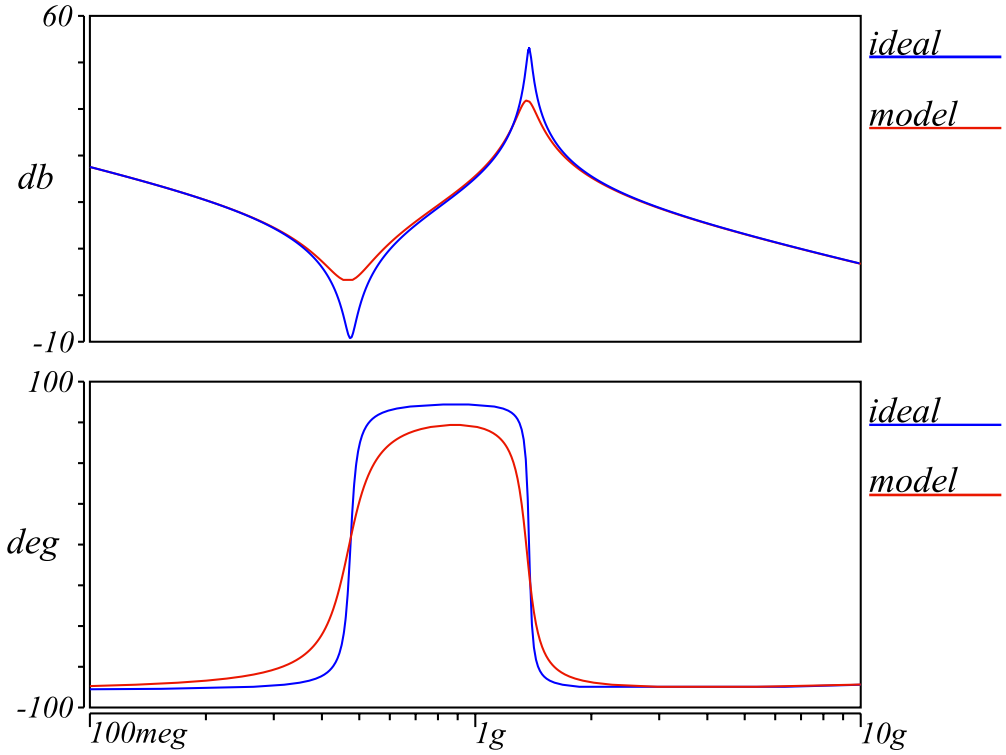

Figure 2.6: Illustrate the parasitic effects of a passive inductor model in an LC tank circuit when compared to an ideal inductor in the same circuit.

Chapter 3

Multi-Frequency Resonant Clocking Setup

Our design enables a clock grid to resonate at multiple frequencies by attaching multiple LC tanks to the grid. Between each LC tank and the grid we include a passgate, a PMOS and NMOS in parallel, which enables us to connect each tank to the CDN or have it disconnected based on a control signal. In this chapter, we discuss how we design and tune the clock grid, LC tanks and passgates.

3.1 Automated Grid Design

Our design uses clock grids due to their superior behavior with process and environmental variations and because they are most common in high performance designs. A clock grid is made up of parallel and horizontal wires and stubs which connect to the clock sinks. Grid buffers are distributed in parallel on the grid while a tree would

attach to the grid buffers from a single source. For our experiments we do not include the single driver to the sinks and instead run simulations with AC signals driving at the clock sinks. This is illustrated in Figure 3.1.

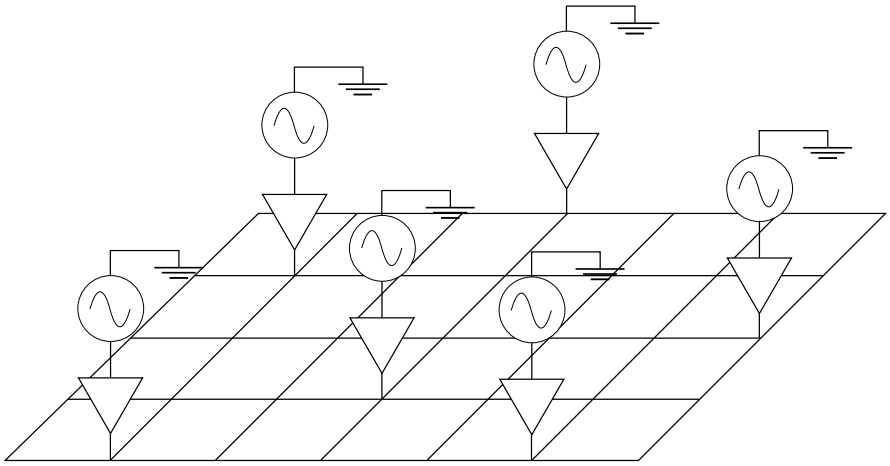

Figure 3.1: Grid buffers are driven by identical AC source.

We refer to a *grid node* as the intersection of horizontal and vertical grid wires. The array of grid nodes does not include the intersections with stub wires. The total number of grid nodes we include in our design is determined by the spacing between grid wires. This spacing will be referred to as the *grid step*. For simplicity, our experiments are done on a uniform grid so the grid steps between all verticle and horizontal wires are equal [5]. The grid step is the single largest contributor to the power consumption of the clock grid as it controls the density of the grid.

To allow the easiest distribution our LC tanks are only attached to grid nodes. A node where an LC tank is placed will be referred to as an *LC node*. Figure 3.2 shows a grid with six LC tanks attached. A concern is how to ensure that the resonance on

the grid is felt relatively evenly across the whole distribution. To best allow for this the LC nodes are evenly distributed across the CDN regardless of how many tanks are implemented in the design. For example, every even column by even row or every third column by third row. This is done for simplicity and is illustrated below in Figure 3.2.

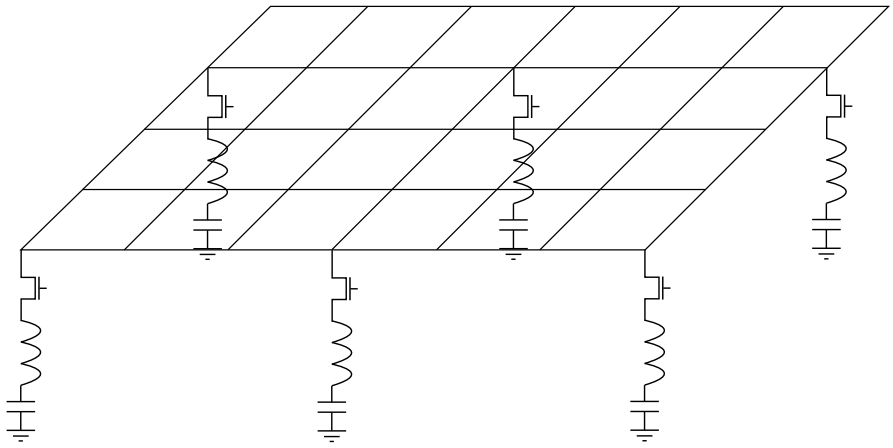

Figure 3.2: LC tanks are always evenly distributed across the grid. This even distribution is maintained when batches of tanks are turned off or on.

When the LC tanks are added to the distribution, they are turned off/on in groups. These groups maintain the even distribution by, for example, turning off every-other-even LC tank in an every even distribution, and so on.

3.2 LC Tank Design

The LC tank circuit we are using is shown in Figure 3.3. This is just like the circuit in Figure 2.2 but we now include our passgate, *pg*, which enables the LC tanks to be attached or detached which, in turn, allows our resonant frequency to shift. We include both a PMOS and NMOS in parallel which allows for the best possible

conduction when we want to connect the circuit. We use gate sizes of 0.95 micron for PMOS and 0.63 micron for NMOS. This sizing ratio and circuit are influenced by AMD and Cyclos [10] as well as [11]. Both gates are sized to be the smallest they possibly can be while maintaining full signal swing in transient analysis.

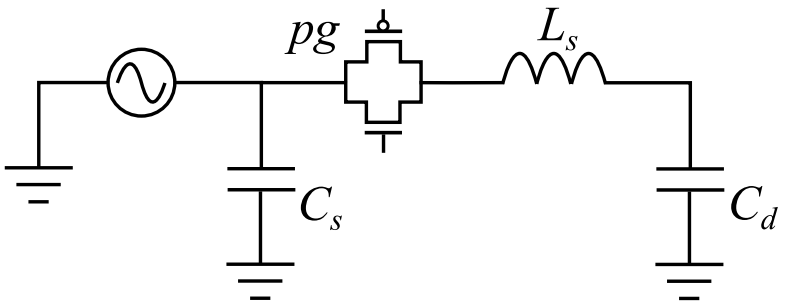

Figure 3.3: Basic LC tank circuit which now includes a passgate, *pg*, to allow it to be connected or disconnected from the CDN.

Figure 3.4 shows the characteristic impedance of the same CDN with four different global passgate sizes. Each line represents a CDN where all LC tank passgate sizes are the same. In this we can see that sizing the passgate to be too small will lead to significant signal attenuation which negates any benefits the LC tanks could hope to provide. Sizing the passgates to be too large leads to smaller power savings and less frequency shifting flexibility.

With respect to the clock grid the LC tanks are in parallel to ground. Recall from basic circuit theory that inductors in parallel reduce their total induction according to

$$L_{total} = \frac{1}{\frac{1}{L} \cdot n} \tag{3.1}$$

where L is inductor size and n is the number of LC tanks. Referring to (2.1) we can see

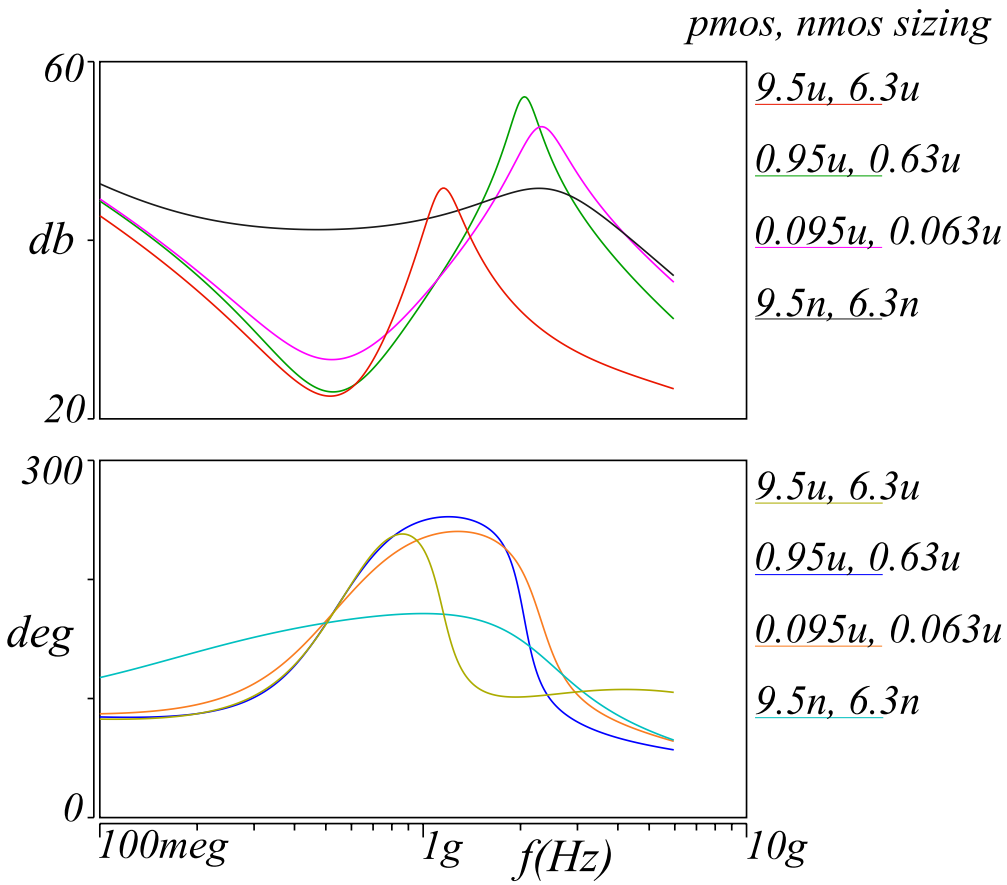

Figure 3.4: The characteristic impedance on a CDN with varying LC tank passgate sizes. When too small the signal attenuates and savings are lost. When too large the frequency range is smaller and less flexible.

that lowering the total induction increases the resonant frequency. Thus, the more LC tanks we have attached to the CDN the higher the grids resonant frequency will be.

To reach a target frequency we can change the number of included LC tanks, change the value of the passive inductor or do both. Our models all fit within the same area so they can be swapped at no cost while providing more precision for honing in on one particular frequency. The number of tanks would be a parameter set by the designer. For example, utilizing a certain percentage of chip area for inductors or only

having space on specific portions of the chip [6, 7].

The grid and decoupling capacitances each influence our resonant frequencies. The total grid capacitance is a fixed value as it is a property of the CDN, therefore the only way to alter the clock grids resonant frequency is to change how much induction is attached. Once the LC tanks are placed the decoupling capacitance should not change regardless of how many LC tanks are attached or detached. This is because all of our decoupling capacitors are in parallel and capacitors in parallel add.

$$C_{total} = C_s \cdot n \tag{3.2}$$

If we put (3.1) and (3.2) together in our resonant frequency equation we see that the number of tanks cancel from the total inductors and the total capacitors.

$$f_{decap} = \frac{1}{2\pi\sqrt{\frac{1}{\frac{1}{L}\cdot n} \cdot C_d \cdot n}} \tag{3.3}$$

This results in the total number of tanks not influencing the decoupling resonance frequency.

The resonance at the CDN and C_d need to be sufficiently far apart regardless of what frequency we currently have the CDN resonating at. The convention is to size C_d to be 6-10 times larger than C_s, the grid series capacitance. This results in a frequency difference between f_{clk} and f_d of about 2.4 - 3 times. After testing on various benchmarks we have found sizing the LC decoupling capacitors such that f_d is between 400 and 600MHz to be sufficient. This allows f_{clk} to go as low as 1GHz with a decoupling capacitance size of roughly ten times that of the clock grid capacitance. Actual numbers will be available in the Chapter 4.

3.3 Benchmarks

Our design is distributed using ISPD benchmarks from their 2010 contest. These are used for CDN case studies and are simple representations of real designs. Their sizes range from $91mm^2$ with 2249 sinks to $1.7mm^2$ with 981 sinks. The distribution is made in C++ and uses 45nm technology files.

Chapter 4

Results

In this chapter, we discuss the effectiveness of the design, the frequencies we can cover, the amount of power we save at various frequencies and the general trend observed across benchmarks of different sizes.

4.1 Connecting and Disconnecting LC Tanks

Before being concerned with displaying a frequency shift we direct our focus to the simple connecting and disconnecting of LC tanks on the CDN. As stated previously, this is done using an NMOS and PMOS in parallel connected between a tank and grid in series.

Figure 4.1 shows the characteristic impedance of a CDN with 16 tanks available. The magnitude and phase of the state where all LC tanks are attached and all are detached are shown. The disconnected tanks coupled through the disabled passgate, *pg*, shows a parasitic resonance. This effect is more pronounced in the presence of more

disconnected LC tanks. This is not a cause of concern because the disconnected grid resonance is more than a gigahertz above the connected grid resonance. We can observe a tiny shift in disconnected grid resonance as more tanks are removed but that shift is so small that it will not interfere with the CDN. The disconnected decap resonance behaves just like the decap resonance so there is no concern of it drifting.

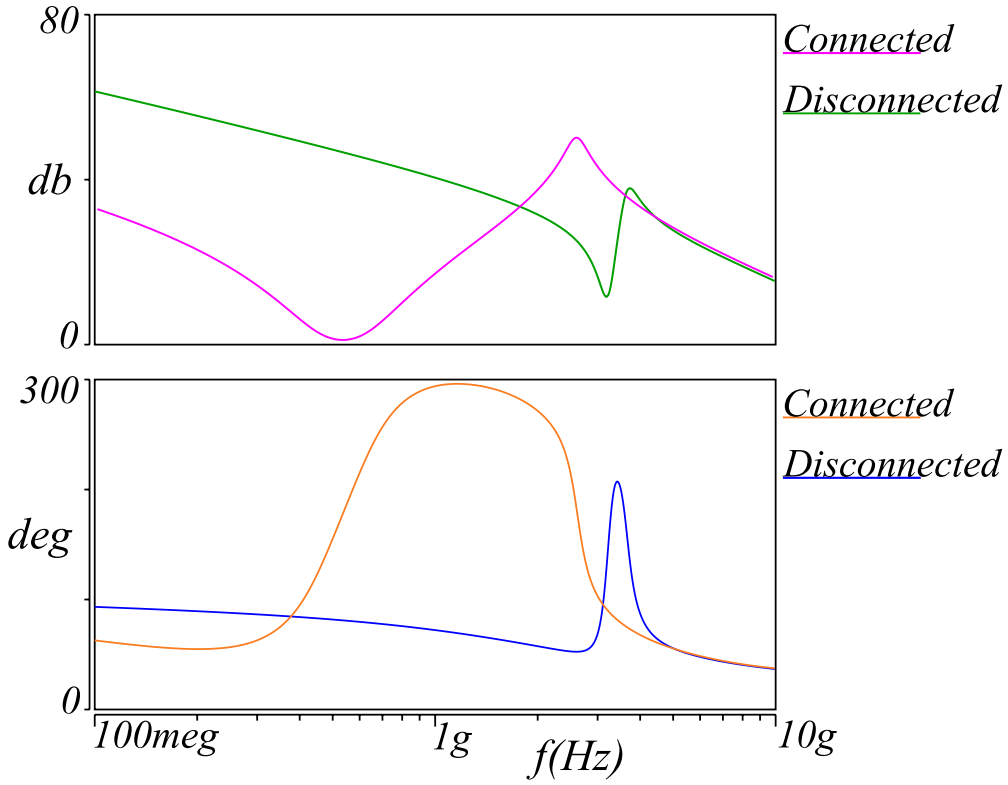

Figure 4.1: A CDN with 16 total tanks. Shows the magnitude and phase of the characteristic impedance when all the tanks are in use and when none are connected to the grid.

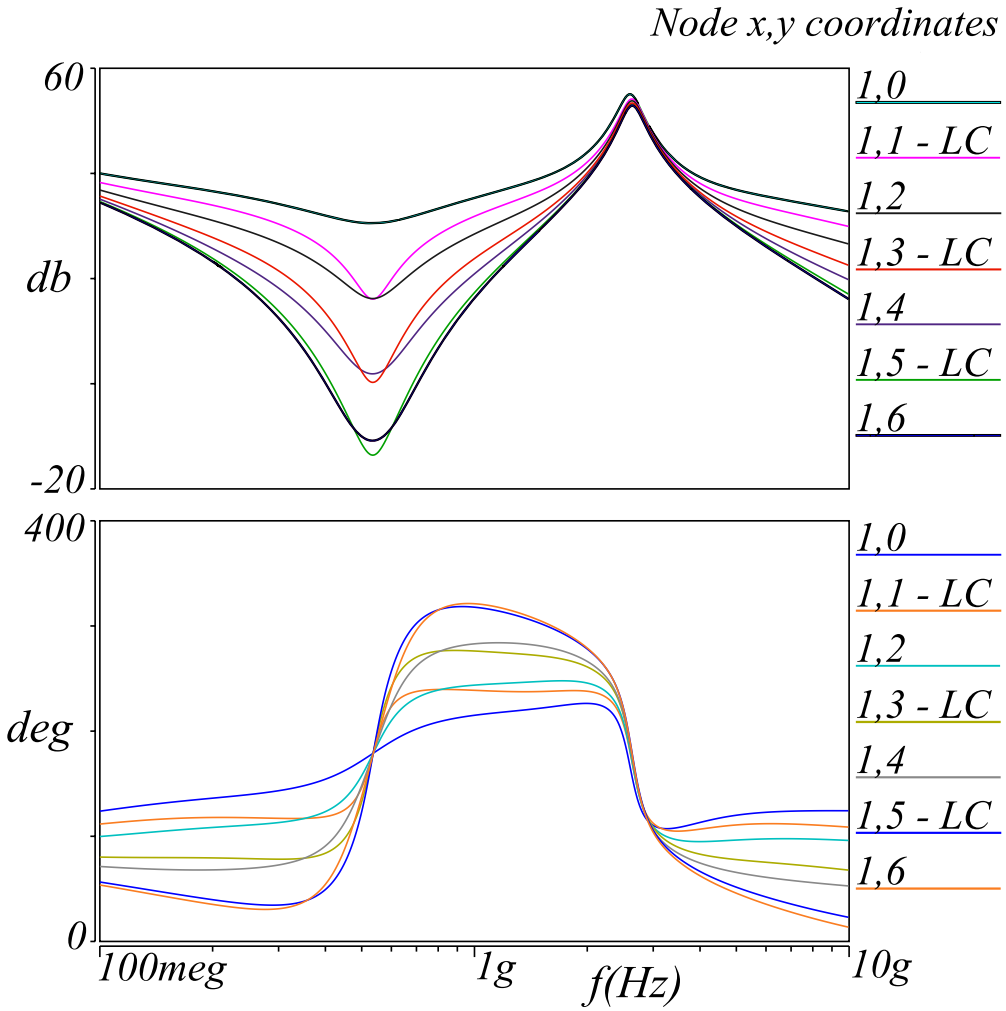

Figure 4.2: The magnitude and phase of the characteristic impedance on grid nodes which are increasingly father away from the nearest sink.

4.2 Effects Across the CDN in a Single State

Given the parasitics of the CDN and LC tanks we expect the resonant frequency and the resonant magnitude to be different from grid node to grid node. As it turns out, this is not an issue in either department. Figure 4.2 illustrates this point. This image shows the characteristic impedance at a series of grid nodes which are in-

creasingly farther away from the nearest sink. We can see that there is a small difference in both the magnitude and the resonant frequency at the grid. The frequency drift is from 2.64GHz to 2.61GHz (1.27%) and the magnitude drift is from 52.89db to 55.08db (3.96%). The decoupling resonance varies in magnitude and degree as the distance from a sink grows. This is not an issue as the resonant frequencies are sufficiently far apart and do not aid in power savings on the CDN.

This effect is not lost as LC tanks are disconnected in order to achieve a frequency shift. Figure 4.3 shows the characteristic impedance when 21 of 36 LC tanks are in use. We can see that the frequency has shifted from 2.6GHz to 1.9GHz and that there is a small frequency and magnitude drift on the grid nodes further away from the nearest sink. The frequency drift is from 1.88GHz to 1.86GHz (1.26%) and the magnitude drift is from 46.64db to 50.42db (7.49%).

4.3 Frequency Shift and Savings

From both Figure 4.2 and Figure 4.3 we can see that the frequency can be shifted by turning off various LC tanks. Figure 4.4 shows this across a greater frequency spread. All states are taken from the same grid node which is three nodes away from the nearest sink. This shows a frequency difference of 1.39GHz between the state where all 36 LC tanks are on and where only seven LC tanks are on. C_d remains steady across all states and is sufficiently far from our lowest state of resonance. Meanwhile, the parasitic resonance of the disconnected LC tanks remains over one gigahertz away

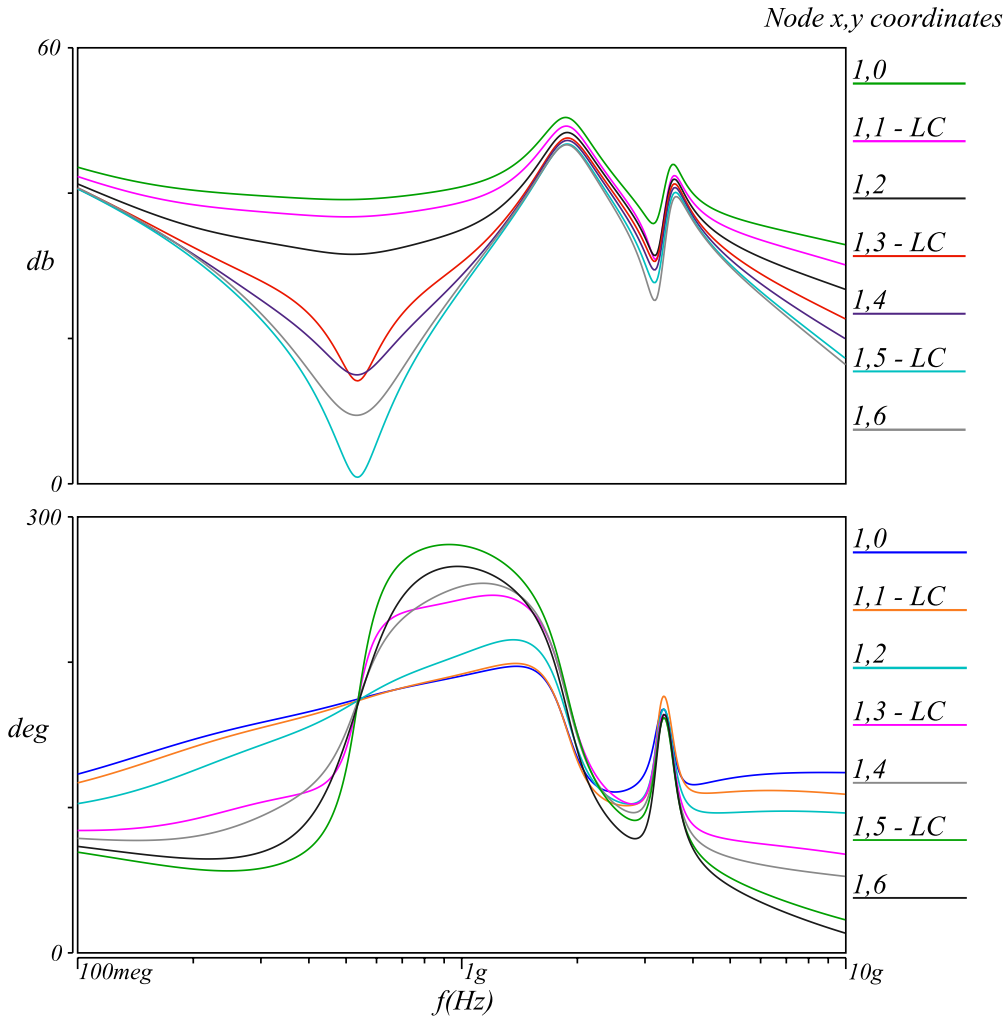

Figure 4.3: The magnitude and phase of the characteristic impedance on grid nodes which are increasingly farther away from the nearest sink when only 21 of the 36 tanks are connected.

from the all-on state.

All states, even when all LC tanks are disconnected, save power. This is found by comparing the average power draw on a CDN with LC tanks ran at the optimal resonant frequency to the same CDN at the same frequency with no tanks built into the design. The power results from a CDN with no built-in tanks at a particular frequency

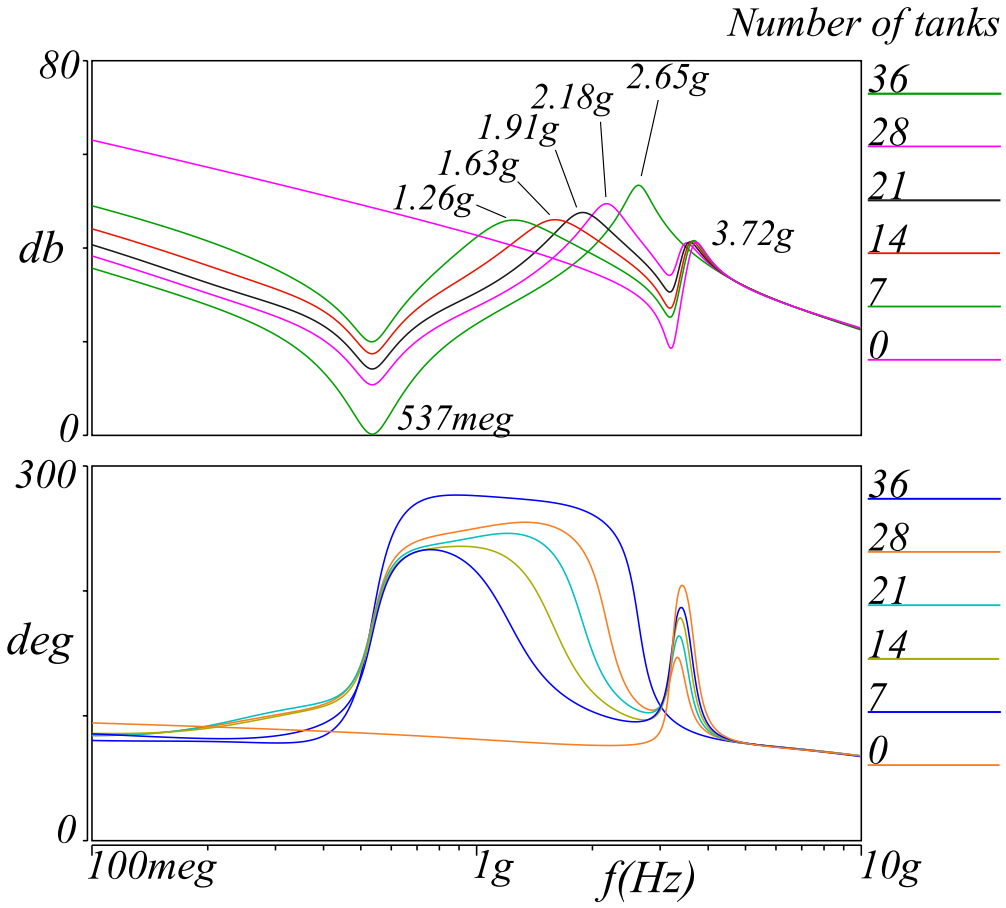

Figure 4.4: Frequency shift across ISPD 2010 benchmark #5 as LC tanks are disconnected.

will be referred to as the baseline power draw for that frequency. We observe that the total power saved declines as the operating frequency decreases. This is likely due to the increased amount of parasitics that exist between the remaining connected tanks. This effect is visualized with the declining magnitude observed in Figure 4.4 and the power data shown in Table 4.1. We are seeing a 39.8% reduction in power costs on the CDN for only the 6.1% chip area costs on this particular benchmark. It should be noted that the state with all tanks disconnected is less predictable than any of the connected

states because the connected states still follow (2.1).

Table 4.1: Resonant Power Savings From ISPD 2010 Benchmark 5 When Compared to the Baseline Power Draw at the Same Operating Frequency.

Tanks (#)	Operating Frequency (GHz)	Baseline Power (mW)	Resonant Power (mW)	Savings (%)
36	2.65	202.8	122	39.8
28	2.18	162.0	103.7	35.9
21	1.91	137.9	96.6	30
14	1.63	135.3	109	19.4
7	1.26	137.3	119.2	13.2
0	3.72	233	151.9	34.8

Table 4.2 illustrates the results we found on ISPD benchmark 3 which is nearly a fourth of the size of benchmark 5. Different choices were made when automating the CDN design. First of all, the grid step size was reduced in order to cover a majority of the sinks. Secondly, we found that the number of necessary tanks did not scale linearly with chip area. Therefore, having nine tanks was not sufficient to provide a gigahertz to safely shift through. This lead to choosing a dense distribution which resulted in thirty LC tanks. Despite this density, the case where only six LC tanks are connected results in a resonant frequency of 870MHz which is too close to the 530MHz decoupling resonance and thus not usable. Also, this distribution has the LC tanks taking up 19.8% of the chip area. This does not take away from the fact that we are saving 41.1% of the CDN power when running at 2.2GHz. Or even that we can save 13.7% at 1.14GHz. This leaves designers to choose their priorities between increasing the number of LC tanks to give the frequency scaling flexibility or limiting the number due to design constraints such as chip resources.

Table 4.3 provides results we found on benchmark 1 which is nearly 11 times

Table 4.2: Resonant Power Savings From ISPD 2010 Benchmark 3 When Compared to the Baseline Power Draw at the Same Operating Frequency..

Tanks (#)	Operating Frequency (GHz)	Baseline Power (mW)	Resonant Power (mW)	Savings (%)
30	2.2	252.7	148.8	41.1
24	1.85	253.5	162.2	36
18	1.48	213	169.1	21
12	1.14	159	137.3	13.7
6	0.87	156.6	143.6	8.3
0	3.58	405.3	236.8	41.6

larger than benchmark 5. While having the greatest number of LC tanks on a CDN the LC node to grid node ratio was the smallest and the total inductor area on the chip was only 2.61%. The total number of LC tanks was chosen in order to supply a similar frequency range as shown in previous benchmarks. While achieving the largest power savings of 41.5% the lower frequencies savings fell off when compared to the other tests. It appears that larger benchmarks can supply the necessary area for significant power savings at higher frequencies while sacrificing power savings in the states with few inductors connected.

Table 4.3: Resonant Power Savings From ISPD 2010 Benchmark 1 When Compared to the Baseline Power Draw at the Same Operating Frequency.

Tanks (#)	Operating Frequency (GHz)	Baseline Power (mW)	Resonant Power (mW)	Savings (%)
168	2.34	1144	668.7	41.5
134	2.04	969.7	681.3	29.7
100	1.75	953.6	719.2	24.6
66	1.43	788.9	687.4	12.9
33	1.09	613	579.4	5.5
0	3.61	1339	907.9	32.2

Chapter 5

Conclusion

This work presents the first tunable resonant frequency CDN. This is achieved with the use of LC tanks which are connected to the CDN by passgates. This enables the removal of tanks to alter the total induction on the CDN and thus move the resonant frequency. Power savings as great as 41.5% and tunable frequency windows of greater than twice the minimum frequency are observed. The run-time configuration removal of LC tanks can be changed to detach each individually to achieve a finer amount of tuning. Given design constraints this methodology is easily tunable and scalable.

Bibliography

[1] C.J. Anderson, J. Petrovick, J.M. Keaty, J. Warnock, G. Nussbaum, J.M. Tendier, C. Carter, S. Chu, J. Clabes, J. DiLullo, P. Dudley, P. Harvey, B. Krauter, J. LeBlanc, Pong-Fei Lu, B. McCredie, G. Plum, P.J. Restle, S. Runyon, M. Scheuermann, S. Schmidt, J. Wagoner, R. Weiss, S. Weitzel, and B. Zoric. Physical design of a fourth-generation power ghz microprocessor. In *Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International*, pages 232–233, Feb 2001.

[2] S.C. Chan, P.J. Restle, K.L. Shepard, N.K. James, and R.L. Franch. A 4.6ghz resonant global clock distribution network. In *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pages 342–343 Vol.1, Feb 2004.

[3] V.L. Chi. Salphasic distribution of clock signals for synchronous systems. *Computers, IEEE Transactions on*, 43(5):597–602, May 1994.

[4] A.J. Drake, K.J. Nowka, T.Y. Nguyen, J.L. Burns, and R.B. Brown. Resonant

clocking using distributed parasitic capacitance. *Solid-State Circuits, IEEE Journal of*, 39(9):1520–1528, Sept 2004.

[5] Matthew R. Guthaus, Xuchu Hu, Gustavo Wilke, Guilherme Flach, and Ricardo Reis. High-performance clock mesh optimization. *ACM Trans. Des. Autom. Electron. Syst.*, 17(3):33:1–33:17, July 2012.

[6] M.R. Guthaus. Distributed lc resonant clock tree synthesis. In *Circuits and Systems (ISCAS), 2011 IEEE International Symposium on*, pages 1215–1218, May 2011.

[7] Xuchu Hu, W. Condley, and M.R. Guthaus. Library-aware resonant clock synthesis (larcs). In *Design Automation Conference (DAC), 2012 49th ACM/EDAC/IEEE*, pages 145–150, June 2012.

[8] F. O'Mahony, C.P. Yue, M.A. Horowitz, and S.S. Wong. Design of a 10ghz clock distribution network using coupled standing-wave oscillators. In *Design Automation Conference, 2003. Proceedings*, pages 682–687, June 2003.

[9] A. Rajaram and D.Z. Pan. Meshworks: An efficient framework for planning, synthesis and optimization of clock mesh networks. In *Design Automation Conference, 2008. ASPDAC 2008. Asia and South Pacific*, pages 250–257, March 2008.

[10] V.S. Sathe, S. Arekapudi, A. Ishii, C. Ouyang, M.C. Papaefthymiou, and S. Naffziger. Resonant-clock design for a power-efficient, high-volume x86-64 microprocessor. *Solid-State Circuits, IEEE Journal of*, 48(1):140–149, Jan 2013.

[11] V.S. Sathe, J.C. Kao, and M.C. Papaefthymiou. Resonant-clock latch-based design. *Solid-State Circuits, IEEE Journal of*, 43(4):864–873, April 2008.

[12] Baris Taskin, Joseph Demaio, Owen Farell, Michael Hazeltine, and Ryan Ketner. Custom topology rotary clock router with tree subnetworks. *ACM Trans. Des. Autom. Electron. Syst.*, 14(3):44:1–44:14, June 2009.

[13] G. Venkataraman, Zhuo Feng, Jiang Hu, and Peng Li. Combinatorial algorithms for fast clock mesh optimization. In *Computer-Aided Design, 2006. ICCAD '06. IEEE/ACM International Conference on*, pages 563–567, Nov 2006.

[14] John Wood, T.C. Edwards, and S. Lipa. Rotary traveling-wave oscillator arrays: a new clock technology. *Solid-State Circuits, IEEE Journal of*, 36(11):1654–1665, Nov 2001.

[15] Zhengtao Yu and Xun Liu. Implementing multiphase resonant clocking on a finite-impulse response filter. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 17(11):1593–1601, Nov 2009.

[16] C.P. Yue and S.S. Wong. On-chip spiral inductors with patterned ground shields for si-based rf ics. *Solid-State Circuits, IEEE Journal of*, 33(5):743–752, May 1998.

[17] C.H. Ziesier, Suhwan Kim, and M.C. Papaefthymiou. Resonant clock generator for single-phase adiabatic systems. In *Low Power Electronics and Design, International Symposium on, 2001.*, pages 159–164, 2001.