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**Authors**

Jiang, Yizhe

Tian, Zishen

Kavle, Pravin

et al.

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Yizhe Jiang ⬤ ; Zishen Tian ⬤ ; Pravin Kavle ⬤ ; Hao Pan ⬤ ; Lane W. Martin ✉ ⬤
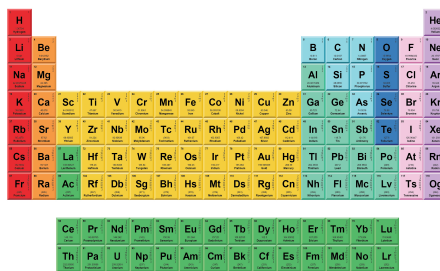
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# Effect of fabrication processes on BaTiO₃ capacitor properties Ⓕ

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Yizhe Jiang,[1] ⓘD Zishen Tian,[1,2] ⓘD Pravin Kavle,[1,2] ⓘD Hao Pan,[1] ⓘD and Lane W. Martin[1,2,3,a)] ⓘD

**AFFILIATIONS**

[1] Department of Materials Science and Engineering, University of California, Berkeley, Berkeley, California 94720, USA
[2] Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, USA
[3] Departments of Materials Science and NanoEngineering, Chemistry, and Physics and Astronomy and Rice Advanced Materials
Institute, Rice University, Houston, Texas 77005, USA

[a)] Author to whom correspondence should be addressed: lwmartin@rice.edu

**ABSTRACT**

There is an increasing desire to utilize complex functional electronic materials such as ferroelectrics in next-generation microelectronics. As new materials are considered or introduced in this capacity, an understanding of how we can process these materials into those devices must be developed. Here, the effect of different fabrication processes on the ferroelectric and related properties of prototypical metal oxide ($SrRuO_3$)/ferroelectric ($BaTiO_3$)/metal oxide ($SrRuO_3$) heterostructures is explored. Two different types of etching processes are studied, namely, wet etching of the top $SrRuO_3$ using a $NaIO_4$ solution and dry etching using an $Ar^+$-ion beam (i.e., ion milling). Polarization-electric-field hysteresis loops for capacitors produced using both methods are compared. For the ion-milling process, it is found that the $Ar^+$ beam can introduce defects into the $SrRuO_3/BaTiO_3/SrRuO_3$ devices and that the milling depth strongly influences the defect level and can induce a voltage imprint on the function. Realizing that such processing approaches may be necessary, work is performed to ameliorate the imprint of the hysteresis loops via *ex situ* "healing" of the process-induced defects by annealing the ferroelectric material in a barium-and-oxygen-rich environment via a chemical-vapor-deposition-style process. This work provides a pathway for the nanoscale fabrication of these candidate materials for next-generation memory and logic applications.

## I. INTRODUCTION

Ferroelectric materials are promising candidates for beyond-complementary-metal-oxide-semiconductor (CMOS) applications,[1] such as non-volatile memories[2] and logic.[3] While a number of ferroelectric materials are being considered for such applications, the perovskite $BaTiO_3$ stands out for its low switching voltage (energy) and high fatigue resistance.[4,5] In this regard, recent studies showed that by carefully controlling the growth parameters, it is possible to synthesize high-quality $BaTiO_3$ thin films where low coercive voltages (<100 mV) and fast switching speeds (approximately nanoseconds) are possible.[4] The realization of actual devices, however, requires further fabricating such films into the desired geometries, which are often based on electrode/ferroelectric/electrode structures.[2,3] For the electrode materials, while common metals such as platinum,

copper, and gold can be used,[6–8] these metals are often associated with degraded performance in ferroelectric capacitors, including fatigue and imprint.[7,8] On the other hand, metal oxides, such as $IrO_2$ or $SrRuO_3$, can alleviate such issues[9] and have become the preferred electrode materials for ferroelectric capacitors.[9,10] While it is possible to reduce deleterious effects on capacitor performance by using the right electrode materials, similar effects can also be induced by fabrication processes, which can introduce defects in the ferroelectric films[10–12] regardless of the electrode materials. In most fabrication cases, the bottom electrode and the ferroelectric layers are deposited first, and the deposition of the top electrode can be achieved via *ex situ* (i.e., in an "additive" sense wherein the top electrode is added by lithography and deposition)[10,13] or *in situ* (i.e., in a "subtractive" sense wherein electrode/ferroelectric/electrode heterostructures are grown before capacitors are defined by lithography

and etching)[4,14] approaches. Common *ex situ* approaches include metal shadow-mask deposition,[8] room-temperature photolithography,[15] and high-temperature stable oxide hard-mask processes.[10] Metal shadow-mask processes are often limited to somewhat large feature sizes due to challenges with misalignment,[8,10] and photoresist masks suffer from degradation at high temperatures.[16] Further efforts also explored photolithography combined with room-temperature deposition of a high-temperature stable (oxide or otherwise) hard-mask,[10] which can subsequently be used for depositing oxide metals at elevated temperatures,[13,17] but such approaches are not applicable to all materials and can still result in imprints,[4,10] which is likely due to interface contamination during the processing. For example, imprints >0.7 V were observed in SrRuO$_3$/BaTiO$_3$/SrRuO$_3$ capacitors fabricated using an *ex situ* MgO hard-mask approach,[4] resulting in asymmetric hysteresis loops and limiting the application of such ferroelectric materials. As a result, *in situ* approaches for top-electrode definition have been explored where the layer interfaces are protected from environmental contamination during the processes. For these approaches, different etching methods, such as wet-chemical etching and dry-ion milling, are used to "subtract" materials from the heterostructures to form capacitors.

Wet-chemical etching utilizes selective chemical etchants to remove materials by transforming unwanted materials from an insoluble solid-state form into a soluble aqueous one via chemical reactions.[18,19] It is, however, challenging to find appropriate wet-chemical etchants with high selectivity for the unwanted materials in a given film stack.[18] Furthermore, the isotropic nature of some chemical etchants can lead to unwanted undercutting,[20] especially in small features. Therefore, it is necessary to explore alternative methods to compensate for the limitations of wet-chemical-etching processes, namely, dry-ion milling, to remove unwanted material. One of the most common approaches is argon-ion milling, wherein atoms or atom clusters of the films are removed by the continuous bombardment of highly energetic Ar$^+$ ions. Argon-ion milling can be used to etch almost any type of material into capacitors,[14] complex structures such as pyroelectric and electrocaloric devices,[21,22] Hall bars,[23] as well as ferroelectric devices in commercial electronics such as memories and logics based on the same.[2] During the etching process, however, the Ar$^+$ ions also have the potential to introduce defects, with previous studies showing (in some cases) the degradation of properties in ferroelectric capacitors (i.e., increased imprint,[24,25] increased coercive field,[25] and suppressed remanent polarization[26]). Therefore, care must be taken when fabricating electrode/ferroelectric/electrode capacitors to ensure the electrical properties of the ferroelectric layers are minimally impacted.

This work explores different manifestations of *in situ* or "subtractive" fabrication of ferroelectric capacitors of the form SrRuO$_3$/BaTiO$_3$/SrRuO$_3$ synthesized using pulsed-laser deposition. The ferroelectric capacitors are fabricated using different etching routes, including wet etching of the top SrRuO$_3$ using a NaIO$_4$ solution and Ar$^+$-ion milling to two different milling depths (milling through the top SrRuO$_3$ electrode just into the BaTiO$_3$ layer and milling through the top SrRuO$_3$ and the BaTiO$_3$ into the bottom SrRuO$_3$ electrode). While the former ion-milling process is often used as an alternative for the wet-etching approach, where only the removal of the top SrRuO$_3$ layer is needed,[4] the latter is what would be necessary for fabricating complex structures where

active ferroelectric devices are separated.[21,22] Subsequent studies of the ferroelectric-capacitor properties reveal negligible imprints in the ferroelectric hysteresis loops from capacitors produced via wet etching; however, for ion-milled devices, larger imprints are observed, with the magnitude of the imprint increasing with the milling depth. Leakage measurements and deep-level transient spectroscopy (DLTS) studies for all heterostructures reveal the same types of intra-bandgap defect trap states located ~0.38 and ~1.2 eV above the valence band, with the concentration of defects increasing with milling depth in ion-milled devices. Post-fabrication treatments are also explored to ameliorate these effects, with annealing the heterostructures in a barium-and-oxygen-rich environment via a chemical-vapor-deposition (CVD)-like process showing the potential to lower the defect level in the devices, thus reducing the imprint in the hysteresis loops.

## II. METHODS

This work focused on 30 nm SrRuO$_3$/100 nm BaTiO$_3$/30 nm SrRuO$_3$/GdScO$_3$ (110) heterostructures, which were synthesized via pulsed-laser deposition (KrF excimer laser, 248 nm; LPX 300, Coherent) following an established procedure.[4] Briefly, the GdScO$_3$ (110) single-crystal substrates (CrysTech GmBH) were adhered to a resistive heater with silver paint (Ted Pella, Inc.) and subsequently heated to a heater temperature of 690 °C at a ramp rate of 20 °C min$^{-1}$ in a dynamic oxygen pressure of 100 mTorr. Once at temperature, a 30-nm-thick SrRuO$_3$ film (which would serve as the bottom electrode) was deposited on the GdScO$_3$ (110) substrate with a laser fluence of 1.34 J cm$^{-2}$ and a repetition rate of 15 Hz in a dynamic oxygen pressure of 100 mTorr. After the SrRuO$_3$ growth, the heterostructures were cooled to 600 °C at a ramp rate of 10 °C min$^{-1}$ at the same dynamic oxygen pressure. Once stabilized at the new temperature, the dynamic oxygen pressure was reduced to 60 mTorr and a 100-nm-thick BaTiO$_3$ film (the ferroelectric) was deposited at a laser fluence of 1.52 J cm$^{-2}$ and a repetition rate of 2 Hz. Following the BaTiO$_3$ deposition, the dynamic oxygen pressure was increased to 100 mTorr while the heterostructures were heated back up to 690 °C at a ramp rate of 15 °C min$^{-1}$, and another 30-nm-thick SrRuO$_3$ film (which serves as the top electrode) was deposited using the same conditions as the other SrRuO$_3$ layer. Once the tri-layer structures were grown, the heterostructures were cooled down to room temperature at a ramp rate of 5 °C min$^{-1}$ at a static oxygen pressure of ~760 Torr. Both the SrRuO$_3$ and BaTiO$_3$ films were grown from stoichiometric ceramic targets (Praxair) in an on-axis geometry with a target-to-substrate distance of 5.5 cm. Following the growth process, x-ray diffraction studies were carried out on the SrRuO$_3$/BaTiO$_3$/SrRuO$_3$/GdScO$_3$ (110) heterostructures using an x-ray diffractometer (Panalytical X'pert Pro3 with copper $K\alpha_1$ radiation of wavelength 1.54 Å). The BaTiO$_3$ films were found to be single-phase and coherently strained to the substrates (Fig. S1).

After growth, five-micron-diameter capacitor structures were defined via photolithography. First, a layer of photoresist (OCG 825, FUJIFILM Electronic Materials) was spun onto the heterostructures in a spin-coater (KW-4A, Chemat Technology) using a spin speed of 1000 rpm for 10 s, followed by 6000 rpm for 50 s. After the spin-coating, the heterostructures were baked at 95 °C for 150 s using a hot plate (KW-4AH, Chemat Technology). Then, the heterostructures were exposed to ultraviolet light through a photomask

in a mask-alignment system (Hybrid Technology Group, Inc.) for 120 s. After the exposure, the heterostructures were developed in a 1:1 water-developer solution (Rohm and Haas Electronic Materials LLC) for 20 s. Once the photolithography was complete, different etching techniques [Fig. 1(a)] were explored to define the capacitor structures. For wet-chemical etching, $NaIO_4$ (prepared in a 0.1M water solution; Sigma-Aldrich Co.) was used to etch through the 30-nm-thick top $SrRuO_3$ electrodes. To control the etching process, the surface resistivity was monitored every 5 s during the etching and, after 30 s, the surface resistivity was measured to be out-of-range, indicating that the etching depth had reached the top $SrRuO_3/BaTiO_3$ interface. An over-etching time of 5 s was performed to ensure any residual top $SrRuO_3$ had been removed.

For dry-ion milling, an $Ar^+$-ion miller (Nanoquest Pico, Intlvac Thin Film) was used to etch the heterostructures. During the milling process, the heterostructures were placed on a sample stage that spun at a constant speed of 15 rpm. The incident $Ar^+$-ion beam had an energy of ~800 eV and a beam-current density of ~0.72 mA $cm^{-2}$. Different milling angles (i.e., the angle between the incident ion beam and the sample surface) could be used; however, previous studies have shown that a milling angle <30° is best used for sample polishing[27] and is not preferred (or should be avoided) in fabricating devices because of the considerable etching on side walls, damaging the geometry and active area of the features.[28] On the other hand, milling at angles >70° can lead to decreased milling uniformity,[29] increased redeposition rate,[30] and low milling speed.[31] In initial testing, we explored milling at different angles and confirmed these observations, and we additionally observed that milling at high angles led to a significant reduction in operational device yield. Therefore, for this study and consistent with observations from prior studies, efforts were focused on a milling angle of 45° since the milling angles of 40°–50° have been shown to provide good milling uniformity as well as increased milling speeds[29,31] (Fig. S2), which can be beneficial for feature fabrication.[28,31] To control the milling depth and (roughly) determine the interface locations, *in situ* end-point detection via secondary-ion-mass spectrometry (SIMS; IMP-EPD, Hiden Analytical, Inc.) was used, where the detector was placed near the sample surface to monitor the signals from barium and strontium ions that were sputtered from the heterostructures. A full milling profile is provided (Fig. S2) for the process of ion

milling through the entire $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructure and into the underlying $GdScO_3$ (110) substrate with SIMS enabled. It should be noted that because of the matrix effect (i.e., the impact of chemical surroundings on the ion yield for different species) during the milling process,[32] especially at the interfaces between different layers, determining the exact interface location can be difficult.[33] Therefore, slight over-milling was required to ensure the unwanted layers were fully removed. For example, in the 45° milling angle geometry used here, an extra milling time of ~40 s was used, corresponding to a total milling time of ~175 s and an expected overmilling of ~8 nm for the heterostructures that were milled just through the top $SrRuO_3$ layer into the $BaTiO_3$ layer and ~645 s or an expected overmilling of ~10 nm for the heterostructures that were milled entirely through the $BaTiO_3$ layer into the bottom $SrRuO_3$ layer. Optical microscope images of some of the fabricated capacitors were taken after different processes to allow for visual inspection (Fig. S3).

Following the fabrication processes, ferroelectric hysteresis loop measurements (i.e., polarization-voltage/electric-field hysteresis loops) were measured using a ferroelectric tester (Precision Multiferroic Tester, Radiant Technologies) using a double-bipolar waveform (+/−1 V) at various frequencies (focusing here on data taken at 10 kHz). Leakage studies (current–voltage measurements) were carried out by applying an unswitched triangular voltage waveform over a temperature range of 300–500 K with a voltage amplitude up to ±3.5 V (Precision Multiferroic Tester, Radiant Technologies; pre-poling pulses were applied to prevent contributions from switching currents). DLTS measurements were performed in a variable-temperature vacuum probe station (PS-100, Lake Shore Cryotronics) using the same tester (Precision Multiferroic Tester, Radiant Technologies) over a temperature range of 100–400 K. The heterostructures were kept at each temperature for 3 min to allow the trapped charge carrier population to reach its thermal equilibrium before the measurement was completed. A voltage pulse of 3.5 V and 8 ms was applied as the trap-filling pulse, and the resulting capacitance transient was monitored. Different time windows were defined to extract the trap energies of the intra-bandgap defects.[34]

For some heterostructures that were ion-milled to the bottom $SrRuO_3$ electrode, post-fabrication treatments were performed in an
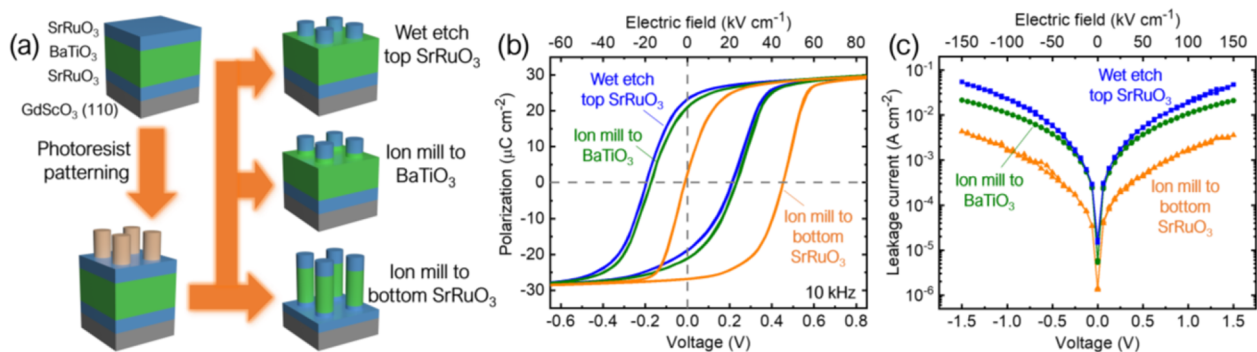


**FIG. 1.** (a) Process flow for fabricating 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) capacitors by wet etching top $SrRuO_3$, ion milling to $BaTiO_3$, and ion milling to the bottom $SrRuO_3$ (top to bottom). (b) Polarization-voltage/electric field loops and (c) room-temperature current–voltage/electric field measurements for the corresponding heterostructures produced in these three ways.

attempt to "heal" or "fix" the properties. The first treatment was annealing under a static oxygen pressure of 760 Torr at 700 °C for 60 min. The second treatment involved placing the sample in an $Al_2O_3$ ceramic boat at the end of the hot zone in a tube furnace, while another $Al_2O_3$ ceramic boat with BaO powder was placed upwind at the beginning of the hot zone. Oxygen was flowed through the furnace tube, first over the BaO powder and then over the heterostructure. The temperature of the furnace was set to ramp to 700 °C at 25 °C min$^{-1}$, held at 700 °C for 60 min, and then ramped to room temperature at 5 °C min$^{-1}$. The heterostructures were then sonicated in 0.1M HCl for 5 min to remove any excess BaO on the surface.

## III. RESULTS AND DISCUSSION

After the fabrication processes, ferroelectric hysteresis loops were measured for the devices made from the 30 nm SrRuO$_3$/100 nm BaTiO$_3$/30 nm SrRuO$_3$/GdScO$_3$ (110) heterostructures [Fig. 1(b)]. For the wet-chemical-etched devices, the ferroelectric hysteresis loops are centered with close to zero imprint (~0.01 V or 1 kV cm$^{-1}$). On the other hand, dry-ion-milled devices show a slightly increased imprint, where upon milling to the BaTiO$_3$ layer and milling to the bottom electrode, the loops are shifted by ~0.03 V (3 kV cm$^{-1}$) and ~0.22 V (22 kV cm$^{-1}$), respectively. While such imprints (~0.22 V or ~22 kV cm$^{-1}$) may be considered "insubstantial" in terms of the ferroelectric hysteresis loop symmetry for many ferroelectric films with similar thicknesses that exhibit larger loop widths (e.g., $\left| E_c^+ - E_c^- \right| >$ 140 kV cm$^{-1}$ in BaTiO$_3$,[13,35] >200 kV cm$^{-1}$ in PbZr$_{0.2}$Ti$_{0.8}$O$_3$,[19,36] >300 kV cm$^{-1}$ in BiFeO$_3$,[37] etc.) for high-quality BaTiO$_3$ films in recent studies, which have very small coercive fields (~23 kV cm$^{-1}$), an imprint of 22 kV cm$^{-1}$ would completely shift the ferroelectric hysteresis loops, rendering one state unstable. Therefore, these "small" imprints can no longer be ignored, and an analysis of the imprint (and how to remove it) is required.

The kinetic energy of the incident Ar$^+$ ions (~800 eV) is comparable to (and likely higher than) the kinetic energy of the adatom species during the pulsed-laser deposition process (which likely have kinetic energies of 10–100 eV depending on the exact growth parameters),[38] and both can introduce knock-on damages (i.e., point defects, defect dipoles, etc.)[17] into the heterostructures.[12] Imprint >0.6 V was reported in PbZr$_{1-x}$Ti$_x$O$_3$ capacitors fabricated using Ar$^+$-ion etching (milling),[24,25] and it is thought to be caused by charged defects (and defect dipoles) and charge-carrier traps introduced by the Ar$^+$ bombardment.[25,26] The imprint was also observed to increase with etching depth,[25] probably due to an increase in the defect density during Ar$^+$ overmilling. Compared to the wet-etched heterostructures, the different electrical behaviors observed in these ion-milled heterostructures are likely to be caused by such defects introduced during Ar$^+$-ion milling, with previous studies suggesting these defects (e.g., $V_{Ba}'' - V_O^{\cdot\cdot}$, $V_{Ba}''$, etc.)[13,35] can align in the direction of polarization[39] and, in the case of ferroelectric films under compressive strain, cause imprints in the polarization-electric-field hysteresis loops[17,35,40] as well as a reduction in the leakage current.[13,17]

To further study these defects, room temperature current–voltage measurements were performed [Fig. 1(c)], revealing that the wet-chemical-etched devices show the highest leakage currents while the dry-ion-milled devices (milled to the

bottom SrRuO$_3$) show the lowest leakage currents. Moreover, it is well known that in dielectric films, different leakage mechanisms can occur, including Ohmic conduction, space-charge-limited conduction, Schottky emission, and Poole–Frenkel emission.[41] The simplest case is Ohmic conduction, where the leakage current density, $J$, is directly proportional to the applied electric field, $E$,

$$J = \sigma E, \tag{1}$$

where σ is the electric conductivity. Another possible leakage mechanism in oxide films is space-charge-limited conduction, where the leakage current density is governed by the movement of bulk space charges within the dielectric film under an applied electric field as[41]

$$J = \frac{9\mu\varepsilon_0\varepsilon_r}{8d}E^2, \tag{2}$$

where $\mu$ is the charge-carrier mobility, $\varepsilon_0$ is the electrical permittivity of the vacuum, $\varepsilon_r$ is the relative optical dielectric constant of the material, and $d$ is the film thickness.

In the above two cases, since $J$ is a power function of $E$, ln($J$) should be a linear function of ln($E$), and for Ohmic conduction, the slope between ln($J$) and ln($E$) should be 1, while for space-charge-limited conduction, the slope between ln($J$) and ln($E$) should be 2. Therefore, ln($J$) is plotted as a function of ln($E$) [Fig. 2(a)], and fittings are performed to extract the slopes from each curve. The fittings show all the slopes have values >2 at large electric fields, based on which we can rule out the Ohmic and space-charge-limited leakage mechanisms.

The third leakage mechanism to consider is Schottky emission, where the charge carriers are injected into the film by overcoming a Schottky barrier at the dielectric/electrode interfaces, and the leakage current density, $J$, is governed by[41]

$$J = AT^2 \exp\left(\frac{-q\phi_B + \sqrt{\frac{q^3E}{4\pi\varepsilon_0\varepsilon_r}}}{k_BT}\right), \tag{3}$$

where $A$ is the effective Richardson constant, $T$ is the absolute temperature, $q$ is the charge of an electron, $\Phi_B$ is the Schottky barrier height at the interface, and $k_B$ is the Boltzmann constant. From Eq. (3), it can be seen that ln($J$) should be a linear function of $E^{1/2}$, and the optical dielectric constant, $\varepsilon_r$, can be extracted. Linear functions are indeed obtained [Fig. 2(b)]; however, the extracted $\varepsilon_r$ values from the slopes fall within the range between 1.81 and 1.88, much lower than the reported optical dielectric constant for BaTiO$_3$ (i.e., $\varepsilon_r = 5.9$).[42] Therefore, the Schottky emission mechanism appears not to be the dominant leakage mechanism.

The last commonly considered leakage mechanism for such oxide films is Poole–Frenkel emission, where there are defect states in the bandgap of the material. These defect states act as trap centers for charge carriers in the dielectric films, and the leakage is governed by a charge-trapping/detrapping mechanism[41] as governed by the equation,

$$J = q\mu N_c E \exp\left(\frac{-q\phi_T + \sqrt{\frac{q^3E}{\pi\varepsilon_0\varepsilon_r}}}{rk_BT}\right), \tag{4}$$
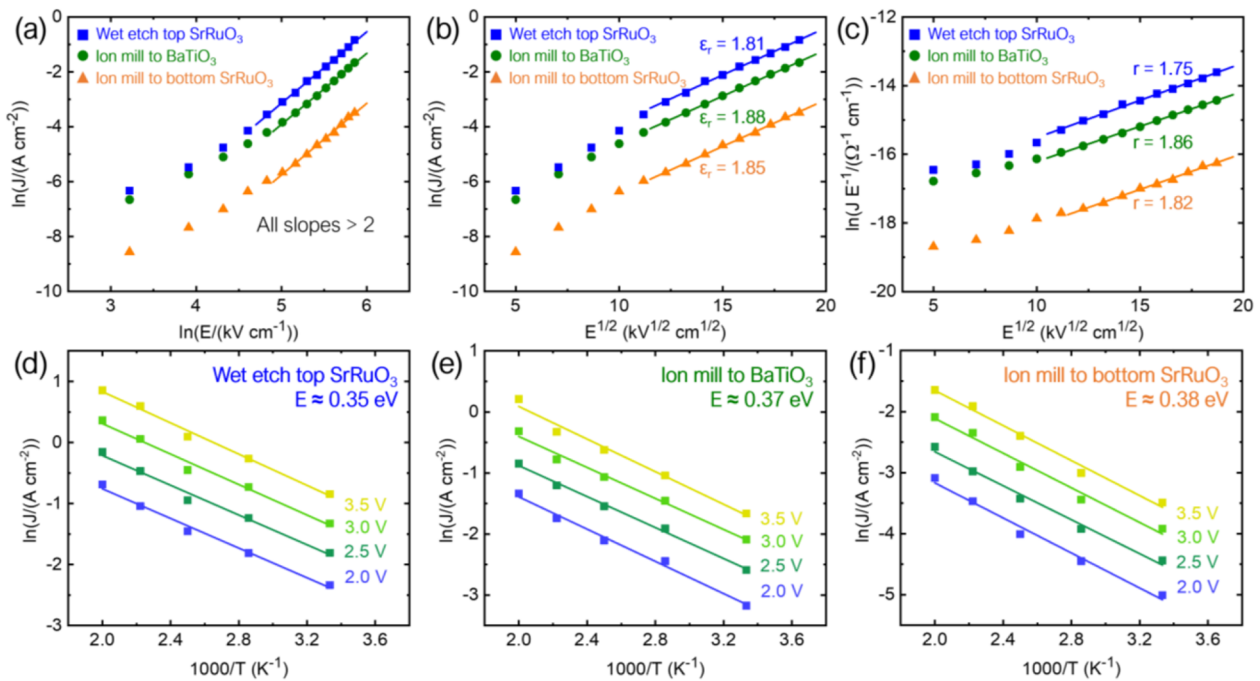
**FIG. 2.** Fittings of leakage current as a function of electric field using (a) Ohmic and space-charge-limited conduction mechanisms, (b) the Schottky emission mechanism, and (c) the Poole–Frenkel emission mechanism. Good fittings are obtained using the Poole–Frenkel equation, suggesting this is the governing leakage mechanism in the heterostructures. Leakage current density is measured as a function of temperature under various voltages to extract the intra-bandgap trap energies for heterostructures fabricated by (d) wet etching top SrRuO$_3$, (e) ion milling to BaTiO$_3$, and (f) ion milling to bottom SrRuO$_3$.

where $N_c$ is the effective density of states of the energy band, $\Phi_T$ is the trap energy of the intra-bandgap defect states, and $r$ is a scaling factor (i.e., $1 \leq r \leq 2$) to accommodate for the large concentration of donor and acceptor states. From Eq. (4), it can be seen that $\ln(J/E)$ should be a linear function of $E^{1/2}$. The data are plotted [Fig. 2(c)], and scaling factors are extracted from the slopes (i.e., the $\varepsilon_r$ is set to be 5.9 in the fitting). The extracted $r$ values for all devices fabricated in all three approaches fall within the range between 1 and 2. The good fitting suggests that the Poole–Frenkel-emission mechanism is (likely) the dominant mechanism for leakage in our BaTiO$_3$ films in all cases.

To extract the trap energy of the intra-bandgap defect states, temperature-dependent measurements were performed on devices produced via all three approaches. $\ln(J)$ is subsequently plotted as a function of $1000/T$ [Figs. 2(d)–2(f)], and the trap energy, $\Phi_T$, is extracted from the slopes. The results show similar trap energies (i.e., 0.35–0.38 eV) for devices produced via all three approaches, suggesting the same type of intra-bandgap defect state dominates the leakage current in the BaTiO$_3$ films. This is logical since the BaTiO$_3$ films are all identical and have only been processed into device structures differently. Since BaTiO$_3$ is commonly reported to be $p$-type[43] and holes are the majority charge carriers, the resulting trap state is, therefore, likely to be located at 0.35–0.38 eV above the valence band and acts as a trap for holes in BaTiO$_3$ films. Previous studies have reported different types of barium-related defects that can exist in BaTiO$_3$ films, including $V_{Ba}'' - V_O^{\cdot\cdot}$, $V_{Ba}'$, and $V_{Ba}''$, which are thought

to be located at ~0.4, ~0.6, and ~1.2 eV above the valence-band edge, respectively.[13,44,45] Therefore, the 0.35–0.38 eV trap state observed in this study is proposed to be of the type $V_{Ba}'' - V_O^{\cdot\cdot}$, which can likely give rise to an internal bias (i.e., imprint) in the polarization-electric field hysteresis loops.[13,17,35]

To further differentiate and understand how the processing impacts the films, the defect levels in the devices and their relations to the observed electric properties (i.e., imprint, leakage, etc.) were probed using DLTS [Figs. 3(a)–3(c)]. For devices that are fabricated via wet-chemical etching of the top SrRuO$_3$ [Fig. 3(a)], the trap state peaks are too small to be measured (i.e., the signal cannot be distinguished from the background noise in the DLTS setup) under the conditions used. This is likely because the heterostructures were not bombarded by Ar$^+$ ions during the fabrication process and, therefore, the defects are just those introduced during synthesis, which, overall, are present at a relatively low concentration. In addition, the wet-chemical etchant, NaIO$_4$, is highly selective, and it does not attack and cause damage to the BaTiO$_3$ layer (a point that is supported by the DLTS). As a result, only a minimal level of defects exists in the BaTiO$_3$ films. For the devices that are produced by ion milling to the BaTiO$_3$ layer (only through the top SrRuO$_3$) [Fig. 3(b)], two weak trap-state peaks can be observed in the DLTS, suggesting a slight increase in the defect level in the BaTiO$_3$ films. For these devices, because of the overmilling at the top SrRuO$_3$/BaTiO$_3$ interface to ensure the top SrRuO$_3$ layer is fully removed, some of the BaTiO$_3$ film is likely also bombarded by the
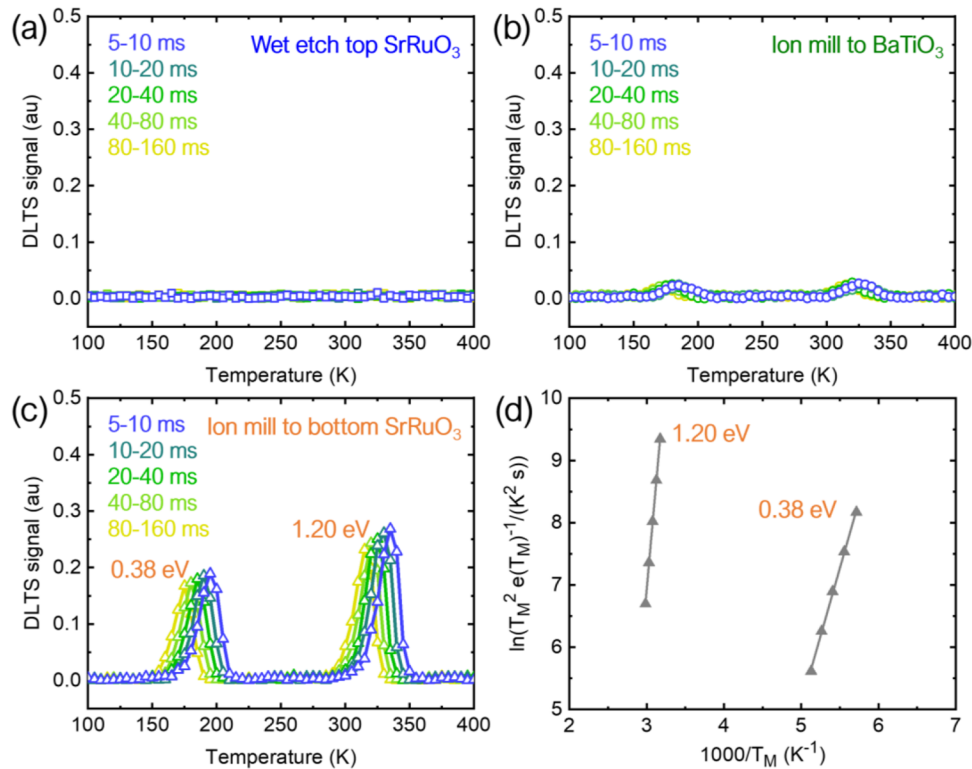
**FIG. 3.** Deep-level transient spectroscopy (DLTS) from 100 to 400 K for heterostructures fabricated by (a) wet etching top SrRuO₃, (b) ion milling to BaTiO₃, and (c) ion milling to bottom SrRuO₃. (d) Fitting to extract the trap state energies for the heterostructure fabricated by ion milling to bottom SrRuO₃.

Ar⁺ ions, leading to a slight introduction of defects in the BaTiO₃ layer. For the devices that are fabricated by ion milling to the bottom SrRuO₃ (entirely through the BaTiO₃) [Fig. 3(c)], two relatively strong trap-state peaks are observed in the DLTS, suggesting a relatively high concentration of defects in the BaTiO₃ layer, likely arising from the continuous bombardment of the capacitor sidewalls while the structures were milled completely through the BaTiO₃ layer and into the bottom SrRuO₃ layer.

Multiple time windows were defined to extract the trap energies of the intra-bandgap defects.[34] For a certain time window from $t_1$ to $t_2$, the capacitance change will reach a maximum at a certain temperature, $T_M$, corresponding to a maximum emission rate,[13,34] $e(T_M)$, which is related to the characteristic thermal emission properties of the trap states,[46]

$$e(T_M) = \frac{\ln\left(\frac{t_2}{t_1}\right)}{t_2 - t_1},$$ (5)

$$e(T_M) = \sigma\gamma T_M^2 \exp\left(-\frac{E_d}{k_B T_M}\right),$$ (6)

where $\sigma$ is the trap capture cross section, $\gamma T^2$ as a whole represents the product of the density of states in the energy band and the thermal velocity of the charge carriers, $E_d$ is the trap energy of the defects,

and $k_B$ is the Boltzmann constant. To extract the trap energies, fittings of the trap-state peaks were performed. From Eqs. (5) and (6), it can be seen that $\ln(T_M^2/e(T_M))$ should be a linear function of $1/T_M$ (or $1000/T_M$). The data are plotted in this fashion [Fig. 3(d)], and the trap energies are extracted from the slope. The two trap-state peaks for the heterostructures that are ion milled to the bottom electrode correspond to trap energies of ~0.38 and ~1.20 eV, which confirms the results from the leakage measurements and matches the trap energies of $V''_{Ba} - V_O^{\cdot\cdot}$ defect-dipole and $V''_{Ba}$ vacancy in previous studies.[13,44,45] For the devices that are ion milled only to the BaTiO₃ layer [Fig. 3(b)], the trap-state peaks, though hard to fit because of the weak signals, show up at roughly the same temperatures in the DLTS spectrum, implying the same type of defects (i.e., $V''_{Ba} - V_O^{\cdot\cdot}$ and $V''_{Ba}$) in the BaTiO₃ layer but present in considerably lower concentrations.

Previous studies have suggested an increase in imprint in ferroelectric hysteresis loops with increasing defect density,[13,35,40] which matches this observation, with the devices that are ion milled to the bottom SrRuO₃ (through the entire BaTiO₃ layer) showing the largest imprint (~0.22 V) and the wet-chemical-etched devices showing the smallest imprint (~0.01 V). This observation also offers a possible explanation for the decrease in the leakage current in the heterostructures [Fig. 1(c)] being related to the increasing defect concentration. Previous studies have suggested that increasing non-donor trap state densities in dielectric films can lead to a decrease in
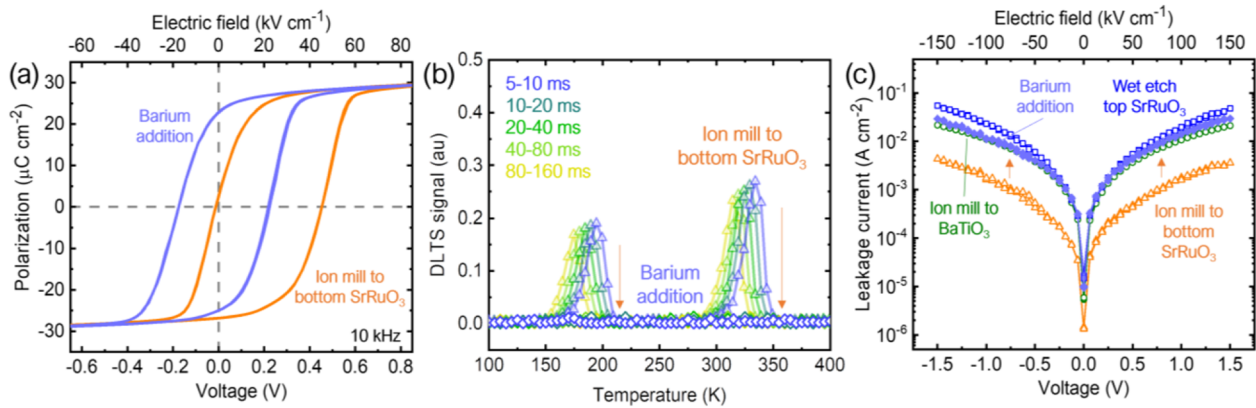
**FIG. 4.** (a) Evolution of polarization-voltage/electric field loop for the heterostructure fabricated by ion milling to bottom SrRuO₃ before and after barium addition via a CVD-style process in a tube furnace. (b) Deep-level transient spectroscopy (DLTS) measured for the same heterostructure after barium addition. (c) Comparison of room-temperature current–voltage/electric field measurements for heterostructures with different fabrication and treatment processes.

the charge carrier mean free path,[17,47] therefore reducing the leakage current, which also matches these observations.

With these observations, concern should be raised about the utility of the dry-ion-milling process, as it may not be compatible with low-coercive-field ferroelectric materials for device production. This would greatly limit the potential uses of these materials and, as such, different post-fabrication treatments to effectively "fix" the induced imprint were also explored herein. For this portion of the study, the focus is on heterostructures and devices that were ion milled to the bottom SrRuO₃ (through the entire BaTiO₃ layer), as they have the highest level of fabrication-induced defects and the biggest change in properties. First, annealing the fabricated heterostructures at 700 °C at an oxygen partial pressure of 760 Torr for 60 min showed no change in the ferroelectric hysteresis loops, probably because of the strong coupling between $V_{Ba}''$ and $V_O^{\bullet\bullet}$ in the formation of energetically favorable $V_{Ba}'' - V_O^{\bullet\bullet}$ defect-dipoles due to electrostatic and strain considerations[48–50] and the fact that barium-related defects cannot be eliminated in an environment rich only in oxygen. In the meantime, other studies have shown the reintroduction of cations into ferroelectric materials via a CVD-like process can greatly reduce the defect density and ease the degradation of electrical properties—an approach pioneered to counter lead loss in PbZr$_{1-x}$Ti$_x$O₃ films grown with sol–gel methods[51,52] and subsequently applied to BaTiO₃ films.[13] Therefore, the heterostructures in question were subjected to annealing in a barium- and oxygen-rich environment at 700 °C via the CVD-style process described (Methods). After the process, ferroelectric hysteresis loops were measured [Fig. 4(a)], and the imprint was found to be reduced significantly (from ~22 to ~2.5 kV cm⁻¹). Subsequent DLTS measurements [Fig. 4(b)] also reveal the suppression/removal of the trap-state peaks (i.e., $V_{Ba}'' - V_O^{\bullet\bullet}$ and $V_{Ba}''$). Finally, a corresponding increase in the leakage current was observed in the treated devices [Fig. 4(c)], likely related to the decrease in trap-state densities, leading to an increase in the charge carrier mean free path and an increase in the leakage current.[17,47] The post-fabrication treatment method shows the possibility of repairing the defects introduced by Ar⁺-ion milling in ferroelectric capacitors.

## IV. CONCLUSIONS

Different processing methods for *in situ* grown SrRuO₃/BaTiO₃/SrRuO₃ heterostructures have been investigated in an effort to explore the best way to fabricate BaTiO₃ capacitor structures with idealized ferroelectric properties. Wet-chemical-etching methods are highly selective and can produce capacitor structures with the best ferroelectric properties with almost no imprint, but such methods alone are likely not suitable for fabricating more complex and realistic device architectures. Dry-ion-milling methods can be used to etch different types of oxide materials at similar speeds. Due to the lack of precision in end-point determination, however, overmilling is often required to assure the full removal of the unwanted material(s). Moreover, because of the high kinetic energy of the incident Ar⁺ ions, milling damage can occur in the ferroelectric capacitors, leading to hysteresis loops with degraded characteristics. An imprint as large as ~0.22 V is observed for heterostructures that are ion milled to the bottom of SrRuO₃ (through the entire BaTiO₃ layer); values large enough to shift the entire loop in BaTiO₃ films with low (~0.23 V) coercive voltages. Post-fabrication treatments to fix this imprint can, however, be performed. Annealing the heterostructures in barium-and-oxygen-rich environments via a CVD-style process can be useful in reducing the imprint of the polarization hysteresis loops as well as reducing the defect levels that are related to barium deficiency. All told, this work shows a pathway forward to produce next-generation devices from thin-films of ultra-low coercive voltage BaTiO₃, which could be key to enabling beyond-CMOS, low-power memory, and logic applications.

## SUPPLEMENTARY MATERIAL

See the supplementary material for additional characterization, including x-ray diffraction, SIMS-based end-point detection during ion milling, and optical microscopy images of fabricated devices.

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## AUTHOR DECLARATIONS

### Conflict of Interest

The authors have no conflicts to disclose.

### Author Contributions

**Yizhe Jiang**: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – original draft (equal). **Zishen Tian**: Formal analysis (supporting); Methodology (equal); Writing – review & editing (supporting). **Pravin Kavle**: Formal analysis (supporting); Writing – review & editing (supporting). **Hao Pan**: Formal analysis (supporting); Writing – review & editing (supporting). **Lane W. Martin**: Conceptualization (equal); Formal analysis (equal); Funding acquisition (lead); Project administration (lead); Writing – review & editing (lead).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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