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Autotuning of Resonant Switched-Capacitor Converters for Zero Voltage Switching

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***Abstract*—By operating resonant switched-capacitor converters at resonance, zero current switching (ZCS) can be achieved to eliminate voltage-current overlap losses. Previous literature has shown that zero voltage switching (ZVS) can also be achieved to further reduce switching losses and attain a higher peak efficiency by recovering the charge stored in the parasitic output capacitance of the switches. Contrary to ZCS operation, ZVS timing is highly dependent on load current even with ideal primary passive components. This paper proposes a novel digital control technique that can dynamically track the optimum ZVS timing across a wide range of load current, through passive component and voltage variations. The proposed concept is validated in a 48-V-to-24-V resonant switched-capacitor (ReSC) converter prototype, demonstrating over 10% power loss reduction compared with the conventional open-loop ZVS, and approximately 30% power loss reduction compared with ZCS.**

I. Introduction

Due to the soft-charging of flying capacitors and the optimal utilization of passive components [1]–[3], resonant switched-capacitor (ReSC) converters can achieve minimal passive component volume and conduction losses at relatively low switching frequencies compared with pure switched-capacitor (SC) converters [4]–[8]. As a result, ReSC converters have seen adoption in data center power delivery where high power densities and efficiencies are desired. Furthermore, many ReSC converter topologies have inherent soft-switching capabilities, which enables switching losses to be greatly reduced. Commonly the dominating loss mechanism in light load operation, switching losses can significantly hinder power delivery performances in data centers where CPUs and GPUs are often operated in low power states.

With zero current switching (ZCS), the voltage-current (V-I) overlap losses can be eliminated. Theoretically, the only requirement to obtain ZCS in a ReSC converter is to set each phase duration to half the resonant period of the LC tank within each phase. In practice nevertheless, non-idealities such as finite input and output filtering capacitances, passive component tolerance, variations and derating can render ZCS timing challenging to estimate with precision [9], [10].

In addition to the elimination of V-I overlap losses, zero voltage switching (ZVS) allows for the recovery of the charge ($Q_{\rm oss}$) stored in the switches' output capacitance ($C_{\rm oss}$) during switching transitions [11]. Without ZVS, the energy associated with the $Q_{\rm oss}$ will be will be drawn from circuit elements and quickly dissipated during turn-on every switching cycle.

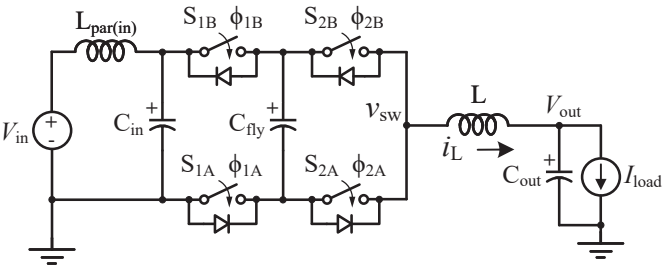

Fig. 1: Schematic of a 2-to-1 ReSC converter. Inductive source impedance $L_{\rm par(in)}$ is represented to model input capacitor voltage ripple.

With ZVS in a ReSC converter, the $C_{\rm oss}$ can be softly charged and discharged by the inductor, therefore preventing energy dissipation.

Although ZVS can enable a higher peak efficiency than ZCS in ReSC converters [12]–[14], ZVS timing is noticeably more dependent on load current in addition to the aforementioned circuit non-idealities. To combat the effect of such non-idealities, previous literature has demonstrated ZCS autotuning techniques for ReSC converters [15]–[17]. However, despite the benefits ZVS holds over ZCS and the load dependency of its timing, no similar closed-loop control has been demonstrated for ZVS operation in ReSC topologies. To maximize the efficiency of ReSC converters across wide load ranges, this work proposes a feedback controller that can dynamically track the optimum ZVS timing in ReSC topologies. Each phase duration is tuned independently, allowing for both the duty cycle and the switching frequency to be time-varying. Therefore, complete ZVS can be maintained through load, voltage and passive component variations. The proposed control technique is studied and verified experimentally on a 48-V-to-24-V ReSC hardware prototype.

II. Theory of ZVS Operation

A. Ideal ZVS

This paper focuses on the ZVS autotuning of the 2-to-1 ReSC converter shown in Fig. 1. The 2-to-1 ReSC converter comprises four switches, with switches $S_{1\rm B}$ and $S_{2\rm B}$ presented at the top, and $S_{1\rm A}$ and $S_{2\rm A}$ at the bottom. There are two main phases, Phase 1 and Phase 2, as labeled in Fig. 2. During each

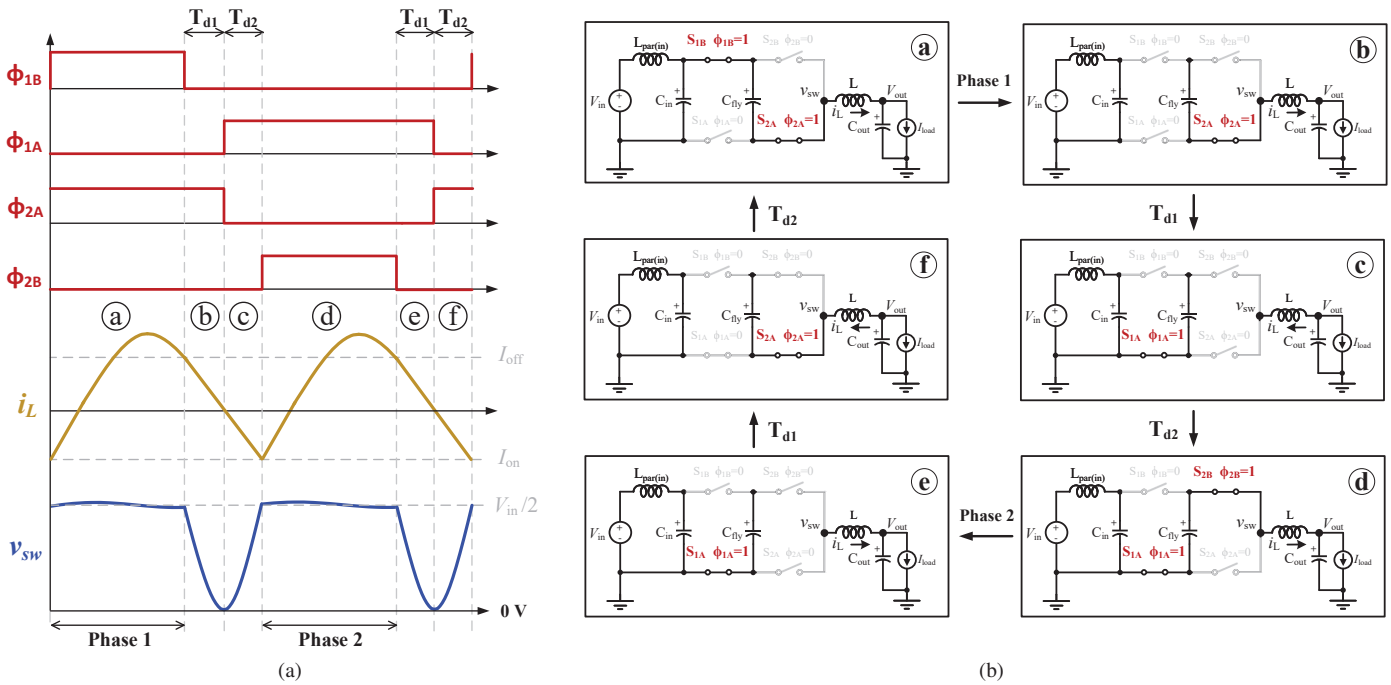

Fig. 2: Ideal ZVS operation of the 2-to-1 ReSC converter. (a) Key waveforms. (b) Equivalent circuits.

phase, one top switch will be conducting simultaneously with its paired bottom switch. For instance, during Phase 1 (top left of Fig. 2b), switches S_{1B} and S_{2A} are conducting while during Phase 2 (bottom right of Fig. 2b), switches S_{2B} and S_{1A} are conducting.

When operating with ideal ZVS, the drain to source voltage (V_{DS}) across every switch is naturally ramped down to 0 V by the inductor current before being turned on. Hence, during a phase transition, the inductor current is used to restore the energy stored in the C_{oss} of the switches that will be conducting in the following phase. Due to the polarity of the blocking V_{DS}, the bottom switches, S_{1A} and S_{2A}, require positive inductor current for C_{oss} recovery, while the top switches, S_{1B} and S_{2B}, require negative inductor current.

To achieve ZVS in this topology, the switching scheme shown in Fig. 2b is employed. The values T_{d1} and T_{d2} represent the time durations required to fully discharge the bottom switch and the top switch after a phase, respectively. T_{d1} and T_{d2}, typically on the order of tens of nanoseconds in this application, are proportional to the resonant period of the inductor and the C_{oss} and are scaled up relative to the phase durations for illustrative purposes in Fig. 2a.

Considering the Phase 1 to Phase 2 transition as an example: at the end of Phase 1, S_{1B} is turned off to force positive inductor current through the C_{oss} of S_{1A}. At the end of T_{d1}, the V_{DS} of S_{1A} has ramped down to 0 V, and it is turned on under ZVS conditions. At the same time, S_{2A} is turned off. Then, during T_{d2}, negative inductor current will be forced through the C_{oss} of S_{2B}. At the end of T_{d2}, the V_{DS} of S_{2B} has ramped down to 0 V, it is turned on under ZVS conditions and Phase 2 will begin.

Because all switches in this topology experience the same voltage and current stress, the same MOSFET can be used to implement all four switches. In this case, they will all have the same C_{oss} and Q_{oss}. Therefore, to obtain ideal ZVS, the turn-off inductor current required to discharge the bottom C_{oss} (labeled as I_{off} in Fig. 2a), and the turn-on inductor current required to discharge the top C_{oss} (labeled as I_{on} in Fig. 2a) must satisfy the following equation (as demonstrated in [11]):

$$I_{off} = -I_{on} \approx \sqrt{\frac{2C_{oss}V_{block}^2}{L}}, \tag{1}$$

where L is the output inductance and V_{block} is the blocking voltage of the switch. When the input and flying capacitor voltage ripple is minimal, $V_{block} = \frac{V_{in}}{2}$ in the 2-to-1 ReSC converter.

Moreover, the discharge time durations, T_{d1} and T_{d2}, must satisfy the following equation (as demonstrated in [12]):

$$T_{d1} = T_{d2} \approx \pi\sqrt{\frac{LC_{oss}}{2}}. \tag{2}$$

Since the parasitic capacitances vary nonlinearly as a function of V_{DS}, the charge equivalent output capacitance ($C_{Q,eq}$) should be used as the C_{oss} value in equations (1) and (2). As discussed in [11], [12], it can be estimated as follows:

$$C_{Q,eq} = \frac{\int_0^{V_{block}} C_{oss}(V_{DS})\, dV_{DS}}{V_{block}}. \tag{3}$$

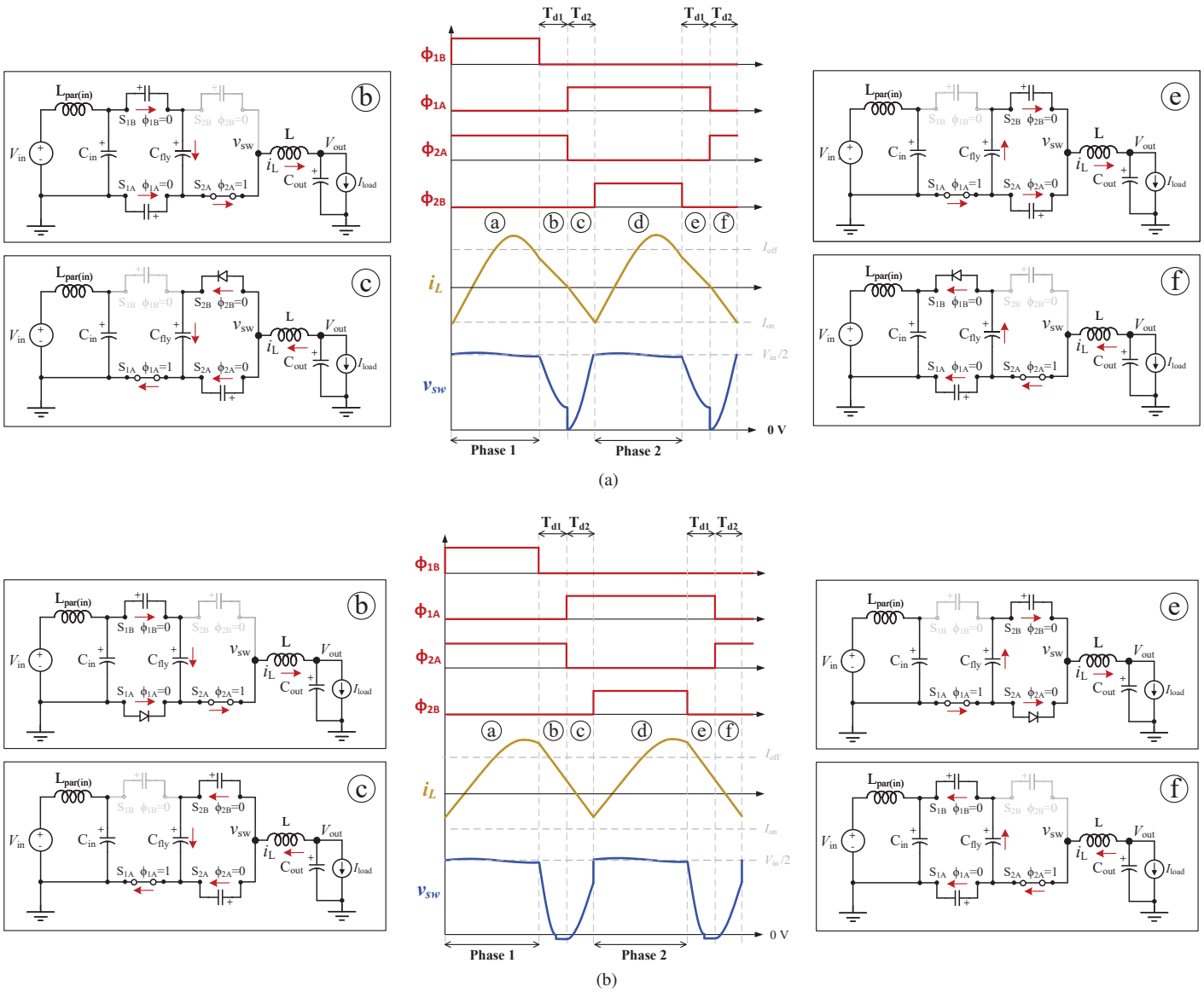

Fig. 3: Key waveforms and equivalent circuits during partial ZVS operation. (a) The switching frequency is too low. (b) The switching frequency is too high.

B. Partial ZVS

It can be observed that under ideal ZVS operating conditions, at the end of T_{d1}, the switch node voltage (v_{sw}) displayed in Fig. 2a will be equal to 0 V. In the case of incomplete ZVS operation shown in Fig. 3, v_{sw} at the end of T_{d1} will be either below or above 0 V. In Fig. 3a, the converter is operated at a switching frequency that is lower than that required for ideal ZVS operation. In this case, the inductor turn-off current is smaller than I_{off} and there will not be sufficient energy to fully discharge the C_{oss} of the bottom switch. As a result, $v_{\mathrm{sw}} > 0\ V$ at the end of T_{d1} and there will be C_{oss} losses associated with the turn-on transition of the bottom switch. The inductor current can still reach the negative peak current I_{on} required to fully discharge the top switch during T_{d2} and its body diode will start conducting before turn-on.

In Fig. 3b, the converter is operated at a switching frequency that is higher than that required for ideal ZVS operation. In this case, the inductor turn-off current is larger than I_{off} and there will be excessive energy to discharge the C_{oss} of the bottom switch. The body diode will start conducting and $v_{\mathrm{sw}} = -V_{\mathrm{f}} < 0\ V$ at the end of T_{d1} (V_{f} being the forward voltage across the body diode of the MOSFET). As a result, the inductor current will not reach the negative peak current I_{on} required to fully discharge the top switch during T_{d2} and there will be C_{oss} losses associated with the turn-on transition of the top switch.

III. Feedback Control

From Fig. 2 and section II-A, it can be summarized that the discharge of the bottom switches' C_{oss} during T_{d1} and the

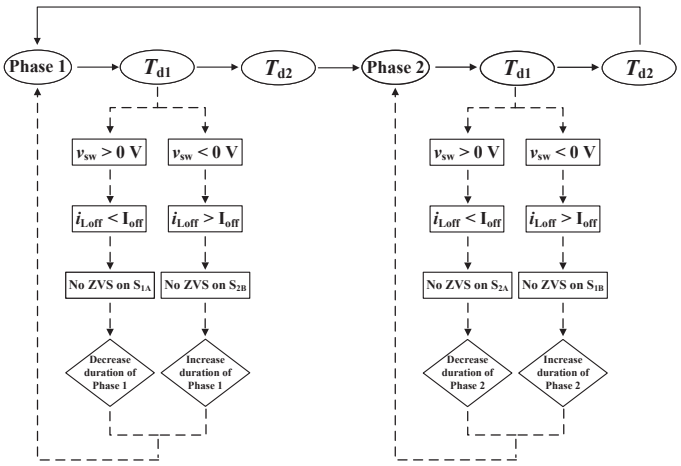

Fig. 4: Flowchart of the proposed control scheme.

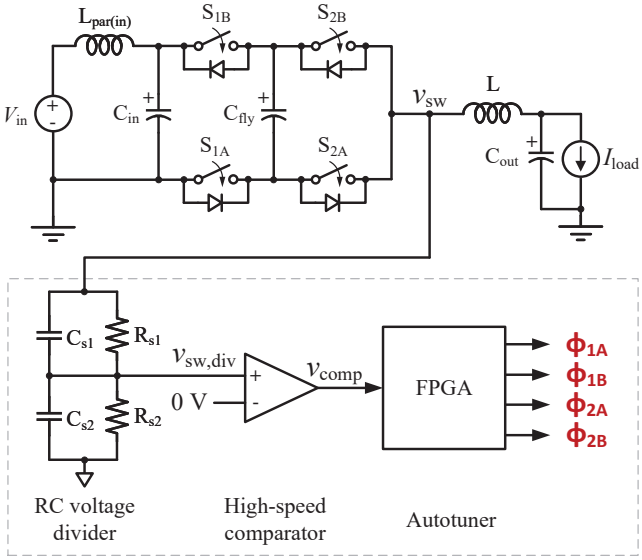

Fig. 5: Block diagram of the proposed autotuner.

discharge of the top switches' $C_{\rm oss}$ during $T_{\rm d2}$ are perfectly symmetric in ideal ZVS operation. As a result, if complete ZVS is achieved, the following observations are made at the end of $T_{\rm d1}$: $i_L = 0$ A and $v_{sw} = 0$ V.

From Fig. 3 and section II-B, it can be summarized that $v_{\rm sw}$ at the end of $T_{\rm d1}$ will be either above or below 0 V in the case of partial ZVS operation. If the duration of $T_{\rm d1}$ and $T_{\rm d2}$ are correctly estimated according to equations (2) and (3), then adjusting the duration of Phase 1 and Phase 2 is sufficient to obtain complete ZVS on all switches. For instance, if $v_{\rm sw} > 0$ V at the end of $T_{\rm d1}$, ZVS was not achieved on the bottom switch indicating the preceding phase was too long (Fig. 3a). The duration of this phase can hence be decreased to obtain ZVS on the corresponding bottom switch. Whereas if $v_{\rm sw} < 0$ V at the end of $T_{\rm d1}$, then ZVS was not achieved on the top switch indicating the preceding phase was too short (Fig. 3b). The duration of this phase can hence be increased to obtain ZVS on the corresponding top switch.

These findings can be used to design a digital hysteretic controller to achieve ZVS by sensing the switch node voltage $v_{\rm sw}$ at the end of $T_{\rm d1}$ and actively tuning the duration of Phase 1 and Phase 2. The proposed control scheme is outlined in Fig. 4. While $T_{\rm d1}$ and $T_{\rm d2}$ are kept fixed, each phase duration is incrementally adjusted by a fixed time step every switching cycle until convergence is reached. In the converged state, the controller will oscillate between a few states. The smaller the time step increment, the closer each converged state can be to the ideal ZVS condition.

Phase 1 and Phase 2 are also tuned independently allowing for both the switching frequency and the duty cycle to be time-varying, and complete ZVS to be maintained on all switches across nearly any operating condition.

IV. Experimental Results

A. Hardware Prototype

A 48-V-to-24-V prototype was built to verify the proposed feedback control technique. The sensing and control network is implemented following the block diagram shown in Fig. 5. An FPGA is used to realize the control scheme illustrated in Fig. 4.

A complete list of the active and passive components used in the hardware prototype is provided in Table I. Annotated photographs of the hardware prototype are shown in Fig. 6. The 40 V MOSFETs and output inductor are on the top side of the board (left), and the gate drive circuitry is on the bottom side (right). The sensing circuitry is highlighted in Fig. 6. A high precision resistor divider, with added capacitors $C_{\rm s1}$ and $C_{\rm s2}$ improving frequency response, is used to attenuate $v_{\rm sw}$ by a factor of 11. The resulting signal, $v_{\rm sw,div}$ as shown in Fig. 5, is fed to a high-speed comparator (AD8611) and compared with a fixed 0 V reference.

B. Convergence Test

Fig. 7 displays the key measured waveforms that verify the convergence process towards complete ZVS. The inductor current $i_{\rm L}$, the comparator output $v_{\rm comp}$, the RC-divided switch node voltage $v_{\rm sw,div}$ and the $Enable$ signal for the controller are recorded. The top left quadrant of Fig. 7 shows an overview of this process.

The initial switching frequency, set to 63 kHz with a duty cycle of 50%, is lower than the ideal ZVS switching frequency for this prototype. The initial condition before enabling the controller is thus similar to the example shown in Fig. 3a. Before the control is enabled, it is observed in the bottom left quadrant of Fig. 7 that the magnitude of the turn-off current is much smaller than the one of the turn-on current, indicating that there is insufficient energy to discharge the $C_{\rm oss}$ of the bottom switches. It is also observed that $v_{\rm comp}$ stays high during $T_{\rm d1}$. Given the bottom switches are not fully discharged before turn-on, $v_{\rm sw}$ and $v_{\rm sw,div}$ will be larger than 0 V at the end of $T_{\rm d1}$. This causes $v_{\rm sw,div}$ to abruptly drop to 0 V at the

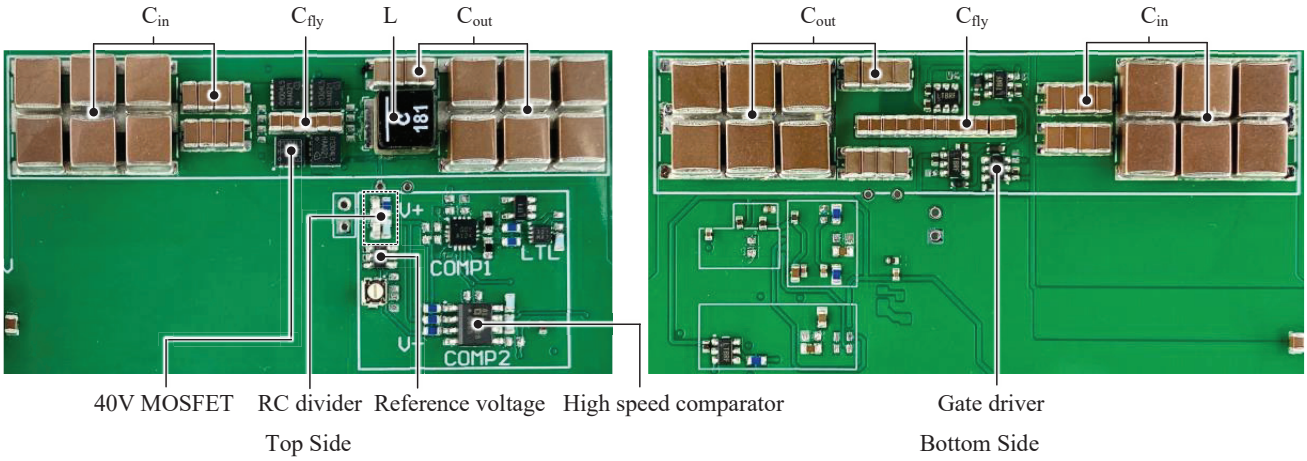

Fig. 6: Annotated photographs of the hardware prototype.

TABLE I: List of the power stage and control circuitry components

Component	Part number	Parameters
MOSFET $S_{1A,1B,2A,2B}$	Infineon IQE013N04LM6ATMA1	40 V, 1.35 mΩ
Flying capacitor C_{fly}	TDK C2012X5R2A475K125AC	X5R, 100 V, 4.7 μF*×18 (in parallel)
Inductor L	Coilcraft XGL6030-181MEC	180 nH, 1.0 mΩ, 43 A
Full Input capacitor C_{in}	TDK C3216X6S2A106K160AC	X6S, 100 V, 10 μF*×16 (in parallel)
	TDK C5750X7S2A226M280KB	X7S, 100 V, 22 μF*×12 (in parallel)
Full Output capacitor C_{out}	TDK C3216X5R1V226M160AC	X5R, 35 V, 22 μF*×12 (in parallel)
	TDK C5750X7R1V476M230KC	X7R, 35 V, 47 μF*×12 (in parallel)
Gate driver	Analog Devices LTC4440-5	High-side gate driver, 80 V
Bootstrap diode	Infineon BAT6402VH6327XTSA1	Schottky diode, 40 V
High speed comparator	Analog Devices AD8611	4 ns single-supply comparator
Resistor divider	Vishay MCT06030D1501BP100	Thin Film, 1.5 kΩ, 0.1 W
	Vishay MCT0603MD1502BP100	Thin Film, 15 kΩ, 0.125 W
Capacitor divider	Kyocera AVX 06031A101FAT2A	C0G, 100 V, 100 pF
	Kyocera AVX 06035A102FAT2A	C0G, 100 V, 1000 pF
Voltage reference for threshold	Linear Technology LT1790ACS6-5	Low dropout voltage reference

* The capacitance listed in this table is the nominal value before DC bias derating.

beginning of T_{d2} (when the bottom switch is turned on) as shown in the zoomed in view of this image.

The bottom right quadrant shows the waveforms during the convergence process, approximately 1.5 ms after the controller is enabled. The turn-off and turn-on inductor currents get closer in magnitude however, v_{comp} is still consistently driven high during T_{d1}.

Finally, the top right quadrant shows the waveforms after convergence is reached. The turn-off and turn-on inductor currents are nearly equal in magnitude, indicating that complete ZVS is achieved on all switches. As expected from Fig. 2a and shown in the zoomed in view of this image, $v_{sw,div}$ has a smooth drop to 0 V confirming the bottom switch is softly turned on at the beginning of T_{d2}. As typical with a hysteretic controller in the converged state, v_{comp} periodically changes between high and low logic levels during T_{d1} from one switching cycle to another. For the FPGA clock frequency of 200 MHz in this implementation, the resulting change in the duration of Phase 1 and Phase 2 is 5 ns every switching cycle.

Fig. 8 shows the V_{DS} and V_{GS} turn-on waveforms for the bottom MOSFET S_{2A}. It is observed in Fig. 8a that before the controller is enabled, S_{2A} is only partially soft-switched as the V_{DS} has not completely dropped to 0 V before the rise of the V_{GS}. However, after convergence, it is observed in Fig. 8b that S_{2A} is fully soft-switched as the V_{DS} has completely dropped to 0 V before the rise of the V_{GS}.

Fig. 9 shows the progression of the duration of Phase 1 and Phase 2 throughout the convergence test shown in Fig. 7. After the activation of the controller at $t = 0$ ms, the controller takes less than 5 ms to converge from a switching frequency of 63 kHz and duty cycle of 50% to a switching frequency of 77.7 kHz and duty cycle of 48.7%.

C. Efficiency Comparison

Fig. 10 shows the measured system efficiency (including gate drive loss) for a light load operation range. All efficiency

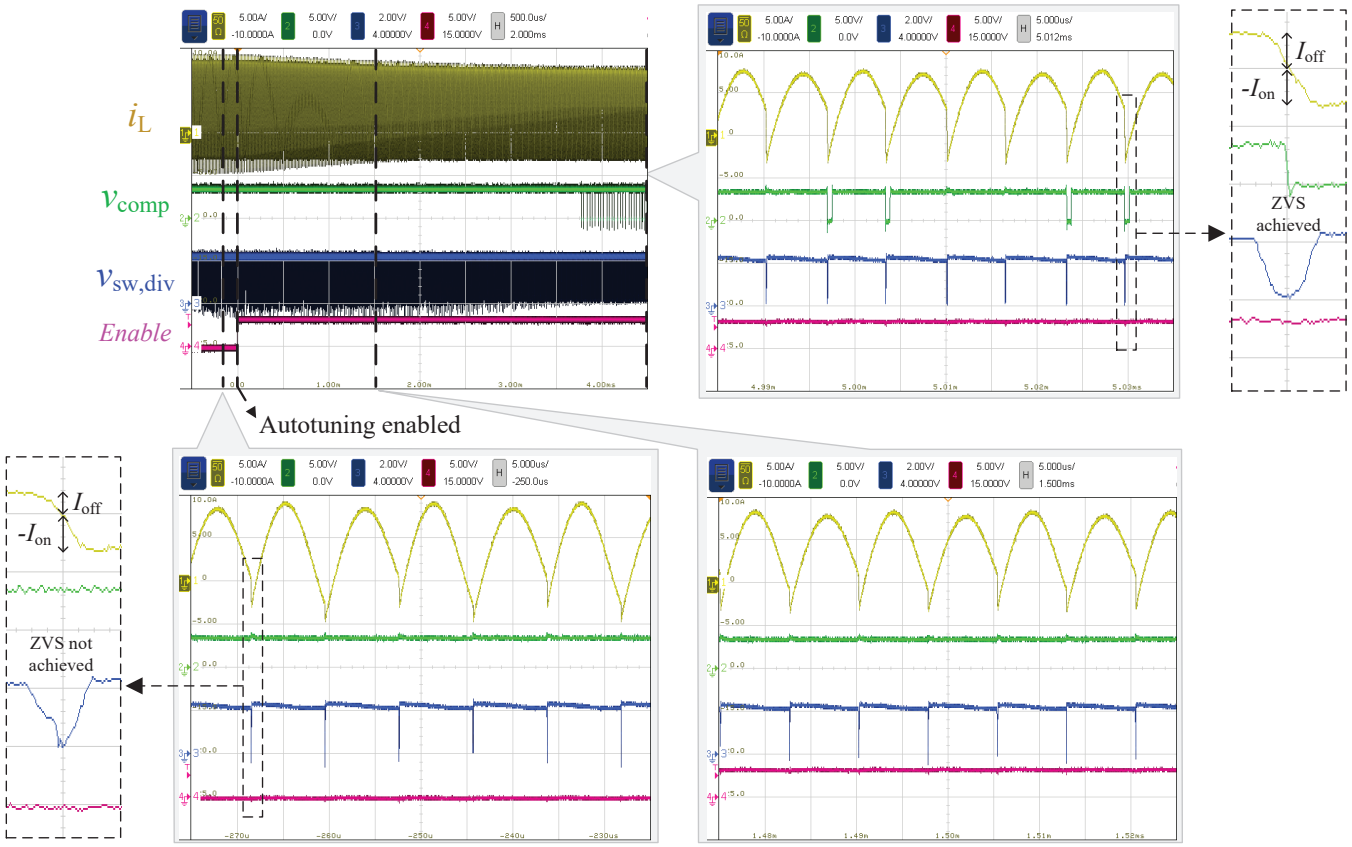

Fig. 7: Measured waveforms of the inductor current i_{L}, the comparator output v_{comp}, the RC-divided switch-node voltage $v_{\mathrm{sw,div}}$, and the control signal *Enable* demonstrating the convergence towards complete ZVS operation at 5 A output current.

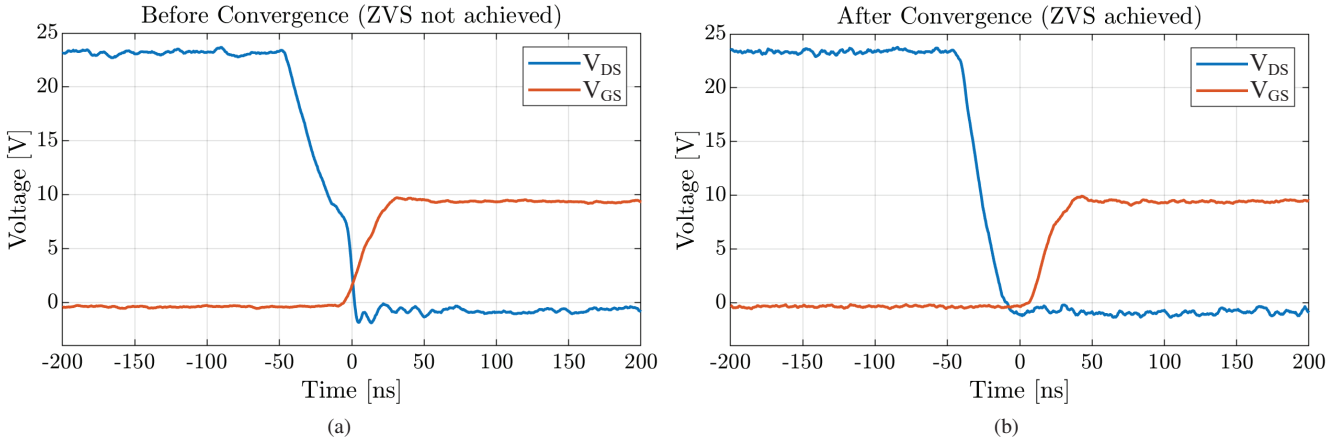

Fig. 8: V_{DS} and V_{GS} turn-on waveforms for the bottom MOSFET $S_{2\mathrm{A}}$. (a) Before ZVS autotuning is enabled (bottom left quadrant of Fig. 7). (b) After ZVS is achieved (top right quadrant of Fig. 7).

measurements were conducted using a high-precision Yokogawa WT3000E power analyzer.

The cases for active ZVS tuning (method proposed in this paper), conventional open-loop ZVS, and ZCS are shown. For the conventional ZVS case, the switching frequency is set to the value that allows complete ZVS to be achieved at the lightest shown output current of 2.0 A. Thus, it is observed from Fig. 10 that the power stage efficiency using active ZVS and open-loop ZVS are the same for 2.0 A output current. However, since the ZVS switching frequency is highly dependent on load, it is observed that as the load current increases, the efficiency with active ZVS becomes larger than

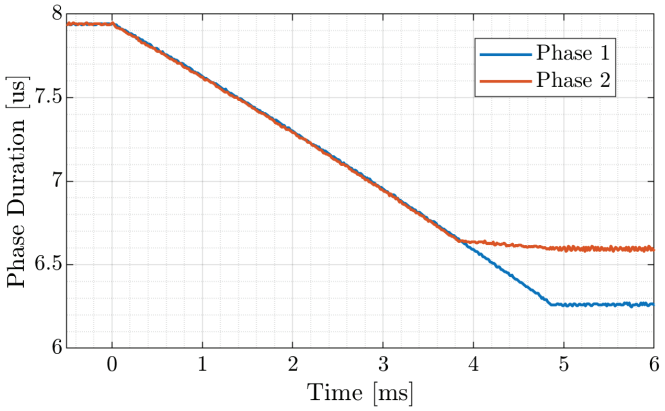

Fig. 9: Phase duration convergence process for the convergence test shown in Fig. 7.

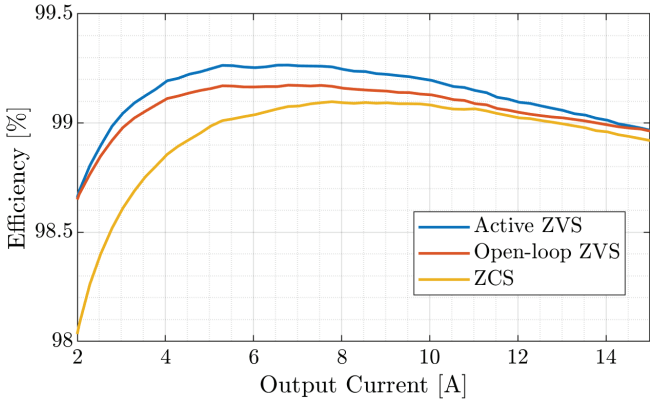

Fig. 10: Efficiency comparison between active ZVS tuning, conventional open-loop ZVS and ZCS.

what is obtained using open-loop ZVS. In fact, complete ZVS is no longer maintained using the conventional technique for output currents larger than 2.0 A. As a result, with a peak efficiency of almost 99.4%, active ZVS achieves better light load performance than the conventional ZVS case for which the peak efficiency is less than 99.2%. Active ZVS tuning can hence allow for more than 10% power loss reduction for the tested conditions.

When the load current becomes large, the converter is dominated by conduction losses rather than switching losses. Since the fixed ZVS switching frequency allows for a lower root-mean-square (RMS) inductor current than the actively controlled ZVS switching frequency, the efficiencies for both techniques converge again at approximately 15 A output current.

While both ZCS and ZVS can greatly reduce overlap losses, ZCS offers no C_{oss} recovery. With ZCS, the energy stored in the C_{oss} is completely dissipated every switching cycle. Thus, both open-loop and active ZVS achieve higher light load efficiencies than ZCS. From Fig. 10, it is observed that ZVS autotuning can allow for up to 30% power loss reduction compared with ZCS on this prototype.

V. Conclusion

With the ability to eliminate both V-I overlap and C_{oss} losses during switching transitions, ZVS is the preferred soft-switching technique to optimize the light load efficiency of ReSC converters. The significant load dependency of ZVS timing in ReSC converters is a practical implementation challenge. In this work, we present a feedback control technique that can dynamically track and achieve optimum ZVS operation in a 2-to-1 resonant switched capacitor (ReSC) converter. The technique was verified on a 48-V-to-24 V prototype and shown to maintain full ZVS on all switches across a wide load range. With active ZVS tuning, over 10% power loss reduction at the peak performance point was achieved compared with the conventional open-loop ZVS, and over 30% power loss reduction was achieved compared with the ZCS case.

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